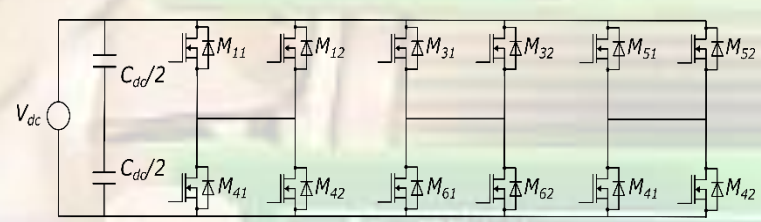
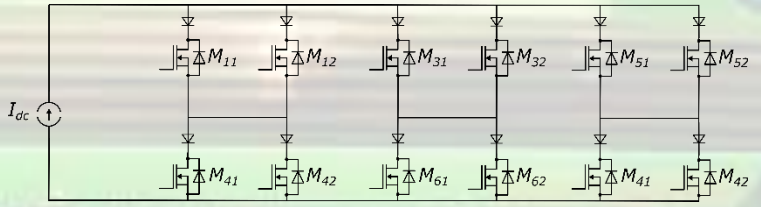
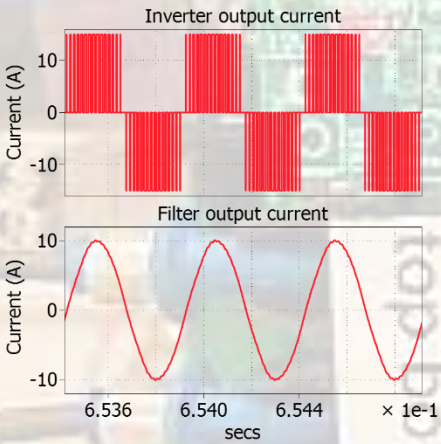
TU Delft

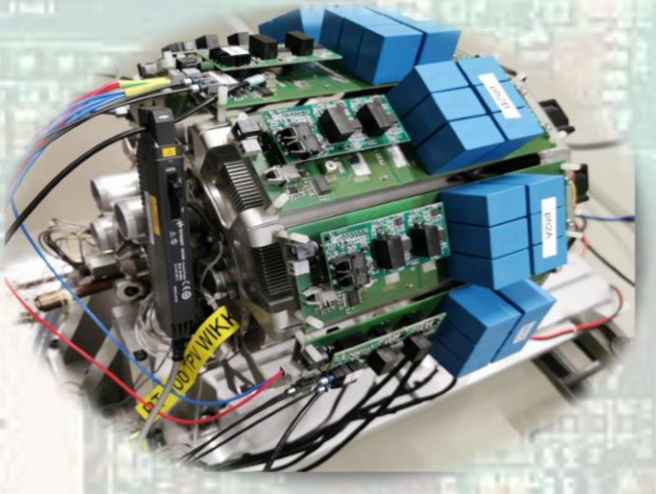
Bench-marking Voltage and Current Source Inverter topologies for Integrated Modular Motor Drives

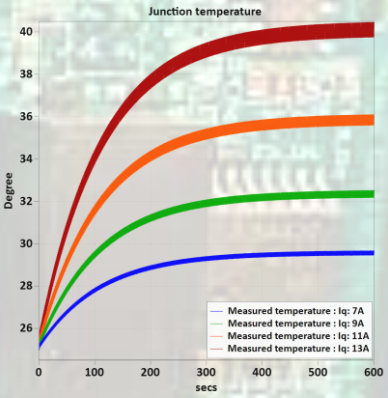
Peeyush Paul

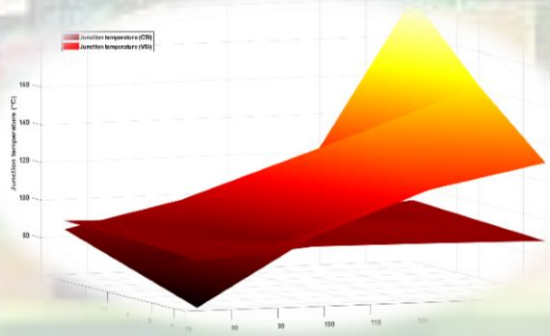












Bench-marking study of Voltage and Current Source Inverter topologies for Integrated Modular Motor Drives

by

Peeyush Paul

in partial fulfillment of the requirements for the degree of
Master of Science
in Electrical Engineering

at
DELFT UNIVERSITY OF TECHNOLOGY,
to be defended publicly on Monday August 29^{th}, 2022 at 09:00 AM.

Student number:	5396557
Supervisor:	Prof. dr. ir. Pavol Bauer
Daily Supervisor:	Dr. Jianning Dong
Thesis Committee:	Prof. dr. ir. Pavol Bauer
	Dr. Jianning Dong
	Dr. ir. José Rueda Torres

ABSTRACT

With the adoption of Wide Band-gap (WBG) switches in Integrated Modular Motor Drives (IMMDs), the size of the drive is rapidly reduced with increase in efficiency and thermal performance. But with the advantages, use of WBG switches as a direct replacement for Si IGBT/MOSFET in Voltage Source Inverter (VSI) posses challenges in the field of steep $\frac{dv}{dt}$ which leads to problems like over-voltage at motor terminal, degradation of cable and motor insulation leading to bearing current and EMI problems. Current Source Inverter (CSI) mitigates the problems associated with WBG usage in VSI but involves additional components like series SiC diodes leading to additional losses and temperature. This thesis explores design of VSI and CSI topology for High Speed Permanent Motor (HiSPEM) IMMD applications conducts bench-marking study of VSI an CSI based on efficiency and thermal performance of converters. .

To begin with, VSI topology for IMMD modelled in PLECS with designing of control strategy. The loss model of SiC MOSFET used in VSI is simulated along with a lookup-table loss model for fast thermal performance evaluation. The current response is verified with the experimental setup with the comparison of loss model and thermal model results.

Subsequently, the CSI topology is modelled with designing of multi-loop control strategy. The decoupling of the D and Q axis is performed using feed-forward decoupling method. The calculation of output capacitor filter is performed based on the cutoff frequency. The stability and bandwidth of different controller in the multi-loop are evaluated using bode plot analysis. Later, the diode loss is modelled and a thermal model is constructed using loss lookup-table for both SiC MOSFETs and series SiC didoes.

The VSI and CSI typologies are bench-marked against each other on parameters such as converter loss, efficiency and thermal performance revealing the optimum topology to use at different current ratings and switching frequencies.

ACKNOWLEDGEMENT

This thesis was accomplished at the TU Delft's DC Systems, Energy Conversion Storage department within the EEMCS faculty. This was a wonderful opportunity for me to obtain research experience, and it couldn't have been achievable without such individuals who have educated and inspired me over my time here.

I'd like to thank my supervisor and committee members, **Prof. dr. ir. Pavol Bauer**, **Dr. Jianning Dong** and **dr. ir. José L. Rueda** for their willingness to devote time in evaluation of the thesis. In particular, as my daily supervisor, Dr. Jianning Dong provided me with numerous helpful and constructive comments during the preparation and execution of this research project. His eagerness for teaching his knowledge to me is invaluable and greatly appreciated. Thanks to his kindness and great direction, I am able to remain motivated during the nine-month duration of my thesis project. Working on the project under his supervision for nine months has been excellent for me.

The completion of this thesis would not have been feasible without the assistance of friends, both in Delft and at home. They have been a continual source of background cheer and have helped me through numerous challenges; I am grateful to everyone of them.

Finally, I would like to express my gratitude to my parents without whom my dream of pursuing my dream wouldn't have been possible. Throughout my time in the Netherlands, they have always encouraged and supported me. My heartfelt gratitude also extends to my partner for her enthusiasm, and words of encouragement during these two fantastic and extensive years. I am glad to have shared this voyage of amusement, frustration, and enlightenment with all of these people.

Thank you for the wonderful memories!

Contents

List of Figures

List of Tables

CHAPTER

1

INTRODUCTION

The physical integration of motor and power electronics eliminates the need of large space demand with special enclosures and connecting cables. Hence making the motor drive more compact, efficient and cost effective. Due to compact size the losses in the converters' components and temperatures play very critical roles in Integrated Modular Motor Drives . With the emergence of SiC and GaN power switches, there has been decrease in switching and conduction loss of the converter, increase in the efficiency of the switches and drop in temperature rise of the components in the enclosure. But with increasing switching frequency in Voltage Source Inverter (VSI) IMMD becomes more prone to steeper $\frac{dv}{dt}$ which may results in over-voltages at motor stator end resulting in insulation degradation. It also induces Common Mode Voltage (CMV) resulting in bearing damage and EMI issues [1]. There are also rising signs that such fast $\frac{dv}{dt}$ values might lead to dynamic interactions between the drive, connecting cables, and the motor load, which results in a considerable drop in efficiency. To reduce these disadvantages in VSI, different modulating techniques are used along with output filters which increases the size and weight of the IMMD [2]. To tackle this situation Current Source Inverter (CSI) could be a possible solution due to its advantages at high switching frequency operation. During the project, the efforts have been made to model a VSI-IMMD setup and design a CSI-IMMD based on multi-loop control and output filter capacitor, and conducting a bench-marking analysis based on the thermal and loss behaviours of the two topologies. Moreover the Space Vector Pulse Width Modulation for CSI has also been modelled.

1.1 Background

The concept of integrating power electronics with electrical machines is very far from new. The concept of IMMD is not new, rather it dates back to 1960s in automotive

industries when automotive alternators were integrated with the diode full wave rectifier [1]. It was until 1987 when IMMD made presence and was used for Heating, ventilation, and Air Conditioning (HVAC). These Integrated Modular Motor Drives (IMMDs) have several advantages to the conventional drive which are discussed below:

- The mass of the motor drive is significantly reduced by eliminating separate enclosures and connecting cables. This reduction in mass is highly desirable in aviation motor drive applications.
- The reduction in volume helps the drive to be physically attached to the structure or very near to its application.
- Higher Efficiency is one of the most intriguing factor for the use of IMMD not only in automotive application but also in industrial processes.
- Since the long connecting cables and separate enclosures are eliminated, the cost of IMMD is significantly reduced,
- The manufacturability of the IMMD is also improved as Original equipment manufacturers (OEMs) of products such as automobiles and home appliances appreciate the opportunity to supply adjustable-speed motor drives packaged in a single assembly rather than two housings with interconnecting wire harnesses, as it simplifies the manufacturing process for installing the IMMDs.
- When compared to conventional motor drives, IMMDs have the potential to significantly improve their fault tolerance thanks to the modular implementations and inverter topologies that are made possible by the integrated motor drive concept. This is especially true when PM synchronous machines are employed in the operation of the system.

With the electrification of all modes of transportation, including automobiles, ships, and airplanes, IMMD has become a research and development topic. Designing of IMMD involves many challenges such as:

- Integration of power electronics with the motor means less space for heat dissipation and this leads to increase in temperature in the enclosure which further increases the loss.
- Placing the converters and controller close to motor also induces Electro-Magnetic Interference and provide hindrance to the converter communication.
- In order for IMMDs to reach their full potential, the integrated power electronics must be able to achieve reliability levels that are equal to or higher than those of the electric machine in which they are embedded, despite the fact that they are subjected to a hostile environment.
- Usage of additional filters to mitigate steep $\frac{dv}{dt}$ increases the size of the converter and size of heat sink.
- In addition, the power electronics must be able to withstand prolonged exposure to mechanical vibrations resulting from the motor and its linked load.

To overcome many of these difficulties in the design of IMMD, the usage of wide bandgap (WBG) switches has been adopted. While SiC has been used in power electronics since the 1950s, commercial development did not begin until the 1990s. WBG switches provides certain advantages such as:

- WBG switches are capable to switching much faster than Si counterparts.
- Due to the greater breakdown electric field, WBG devices are able to be built with far thinner drift layers and/or a higher doping concentration than silicon devices and hence the size and mass of WBG switches is less than traditional Si switches.
- The conduction loss in the converter can be reduced to approximately 1/300 times the loss using Si switches [3].
- The thermal conductivity of SiC switches with same voltage rating is 3 times higher than Si which reduces the thermal stress on switches to a great extent [3].
- The switching loss of WBG devices is lower than that of Si power switches because of the faster rise and fall periods. This allows for significantly greater switching frequencies to be achieved in the majority of applications [4].
- With the increase in switching frequency the passive components such as capacitors and inductors are also reduced [5].

Despite possessing the aforementioned benefits, the Voltage Source Inverter (VSI)-IMMD cannot be shrunk beyond a certain point since DC link film capacitors and frequency do not always follow an inverse relationship. The capacitor RMS current rating decreases as the switching frequency increases. When the RMS current rating of capacitors reduces to the RMS current value of the IMMD module, the capacitor selection reaches an optimal point. The size of the capacitor can no longer be reduced by increasing the switching frequency [6]. To overcome this problem many different approaches have been for VSI topology including use of segmented drives which can greatly lower the ripple current and capacitance requirements of the dc link [7].

The VSI is the most common topology used in the current IMMD industry because of the following advantages:

- The input constant DC supply does not require any controlled rectifier rather a simple diode bridge rectifier can be used.
- The DC capacitor used in the input of the VSI produces constant DC voltage with negligible ripples.
- The manufacturing cost of VSI is low due to simple components requirement and doesn't require a mandatory output filter.
- The output voltage produce is independent of the nature of load.
- The IGBTs and MSOFETs with anti parallel internal body diode are compatible with the VSI.

But the use of WBG switches like GaN, SiC MOSFETs etc. in VSI posses certain disadvantages such as :

- The usage of WBG switches as a drop-in replacement for Si-IGBTs in VSI in order to achieve higher switching frequencies has led to the emergence of a problem with steeper *dv/dt*. [8].
- These high *dv/dt* in the switches leads to over-voltages at the motor terminals and increase the stress on motor insulation resulting in bearing current which may lead to premature motor failure and Common Mode Interference (CMI).[5, 9].

The problem of high *dv/dt* during high switching frequency in VSI poses a number of threats to the machine, which can not only cause damage but also hinder communication within the drive. The high *dv/dt* causes high Common Mode EMI which leads to the following [10]:

- The CM-EMI can lead to cross talking phenomenon among the switches in which both upper and lower switches can be made on at same time leading to short circuit of DC bus and causing dc link shoot-through fault.
- CM-EMI could also trip the digital controller when the machine is running at high speed, which will result in generation of high back emf feeding back to the DC bus and thus creating Uncontrolled Generation (UCG) Fault.

These challenges have generated interest in understanding if alternate inverter topologies might offer advantages over VSIs if WBG power switches are employed. The PWM current-source inverter (CSI) is one of inverter topologies that stands out as a WBG-friendly alternative to the more common VSI inverter. The CSI topology has not gained much attention because of its incompatibility with Si MOSFETs and IGBTs leading to addition of series diodes. The basic topology of both VSI and CSI is shown in the figure 1.1.

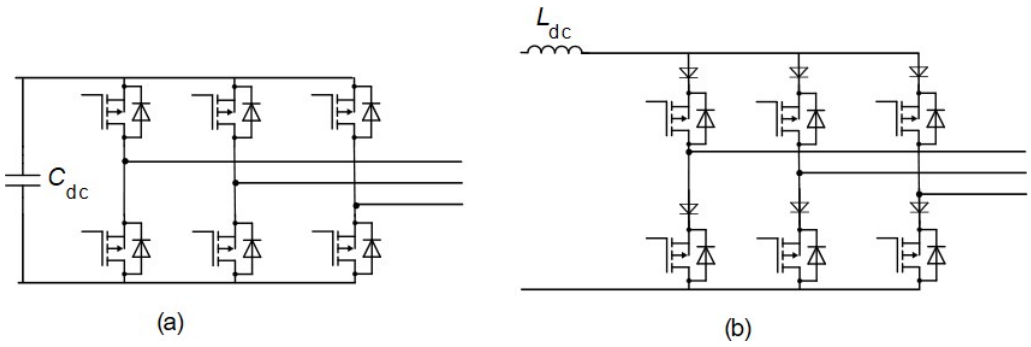


Figure 1.1: Basic topology of (a) VSI, and (b) CSI

In [11], the performance evaluation of VSI and CSI is performed at higher frequencies, where CSI is found out to be more efficient than VSI. During the recent years CSI have become a centre of attraction for applications involving high speed motors such as in industrial compressors and medium speed high switching frequency converters in all electric air-crafts (AEA).

Unlike Electric Vehicles (EVs), electric airplanes are in the initial stage of development and still there hasn't been a commercial passenger airplane in the world [12]. In aviation applications, the operational cost and CO2 emissions are directly affected by the weight

of the power converter. To maximize power density, the power converter must run at a high switching frequency to decrease the size of the filter. [13]. High frequency CSI drive in electric aircraft propulsion have shown high efficiency along with high fault tolerance towards uncontrolled generation faults and good thermal performance [10].

This thesis is inspired by the potential to contribute to high-speed drive applications involving converters with high switching frequencies by developing a PLECS-based assessment platform that serves as a starting point for the development of CSI-based motor drive systems.

1.2 Research Objective

The thesis is the preliminary step in the creation of an IMMD developed specifically for High Speed Motor Drive applications. The primary objective of the thesis is to model the motor drive in order to analyze its thermal behavior and power loss for various inverter topologies.
The research objectives of the thesis project are as follow:

- Modelling of the existing VSI IMMD in ESP laboratory in a simulating environment.
- Modulation, filter and controller design of CSI-IMMD.
- Conducting bench-marking analysis based on power loss and thermal behaviour of VSI and CSI-IMMD model.

1.3 Approach Overview

The motor used in the project is a 6 phase High-Speed Synchronous Permanent Magnet (HiSPEM) machine. For testing purpose, the three phases of the machine is used for motor application and other three for generating application. Hence out of the 6 Power Distribution units (PDUs) connected to each phase three acts as inverter and other three as rectifier. The VSI and the CSI-IMMD are both modeled in the PLECS simulation environment. While the IMMD model is used for the loss analysis, a separate look up table is developed to analyze the thermal behavior in order to reduce computational time in PLECS. The method used to tackle the problem statement is depicted visually in the accompanying figure 1.2.

1.3.1 Project Contribution

The thesis project has contribution in the field of modelling and designing IMMD for different inverter topologies and adds to ways of bench-marking these based on thermal and loss behaviour. In details, the project contributes to:

- The efficiency and junction temperature analysis for the inverter switches has been developed.

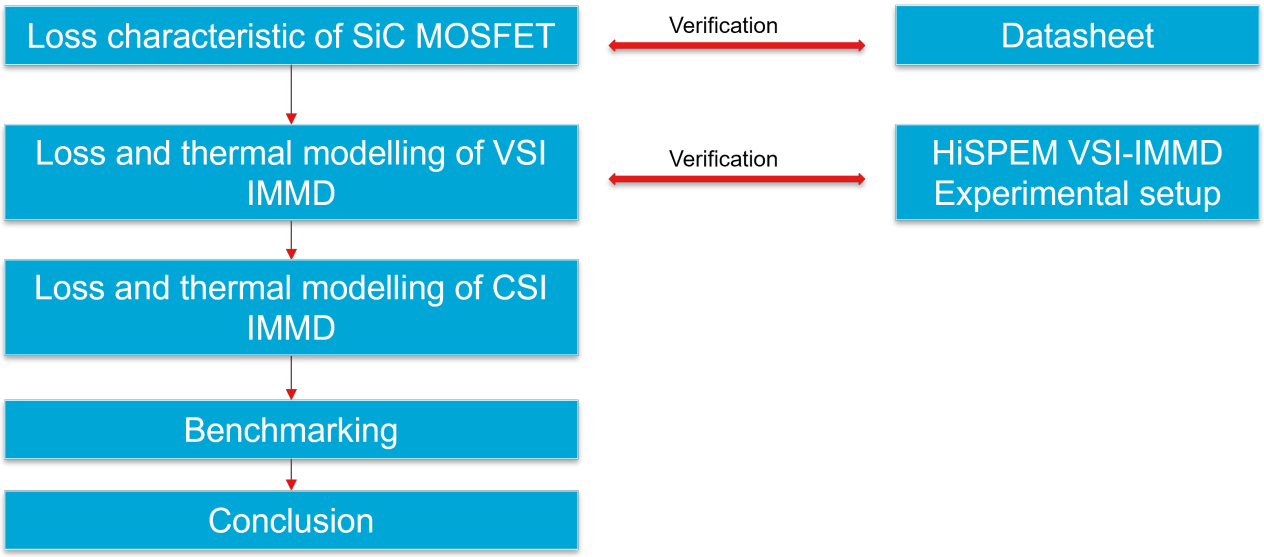


Figure 1.2: Flow chart stating approach towards problem statement

- A method to implement Space Vector Pulse Width Modulation (SVPWM) for Current Source Inverter (CSI).
- A method to design and implementation of controller for CSI topology using multi-loop control strategy and stability analysis.
- Bench-mark study of two different topologies for HiSPEM at different operating parameters.

1.3.2 Work structure

The thesis project has been divided into 5 chapters which are explained below:

1. **Chapter 1** presents the context, the aims of the research, an overview of the inquiry approach, and the contributions made by the thesis project.
2. **Chapter 2** provides the method to model VSI-IMMD system. The loss characteristics of the MOSFET is reviewed using Double Pulse Test (DPT) in LTspice simulation and data-sheet. The motor-inverter loss model and a thermal lookup table model is developed. The developed loss and thermal models are then compared with the VSI-IMMD experimental setup at different operating current to know the accuracy of the model.
3. **Chapter 3** provides the method to design and model of CSI-IMMD system with detailed modelling of SVPWM for CSI and multi-loop control of the IMMD. It also discusses about the designing of output capacitor and its effect on the stability of the system and speed of the HiSPEM machine.
4. **Chapter 4** provides the bench-marking analysis of the VSI-IMMD and CSI-IMMD based on drive loss and thermal behaviour.

5. **Chapter 5** reviews the work, draws conclusions based on the output results of each stage, and discusses potential future work.

CHAPTER

2

MODELLING OF VSI-IMMD SYSTEM

Modelling is considered to be a very important step in every design and development project. It provides an insight to the system which in return contribute to design improvement. Compared to prototyping, modeling assists in viewing the system from numerous angles. It aids in the visual presentation of the system and the evaluation of risk and alternatives at an earlier stage in the system's development life-cycle. For these reasons, modelling is considered to be the first step towards product designing. In this Chapter, the following points will be discussed:

- Modelling of control system for VSI topology for IMMD.
- Power loss modelling of SiC MOSFET and the converter.
- Thermal loss modelling of SiC MOSFET and the converter.
- Verification of thermal and power loss model of VSI-IMMD.

2.1 Control strategy

In today's advanced modern industry and society, motor control systems are vital. From general-purpose variable-speed drives like wind turbines to high-performance robotics, electric automobiles, and CNC machines, it has a wide range of applications. There has been a lot of research on control strategy of Permanent Magnet Synchronous Machines (PMSMs). There are lot of control strategy available for the PMSMs depending on the type of response needed like scalar, Field Oriented Control (FOC), Direct Torque Control (DTC), Unity Power Factor Control (UTC) and many more. In general the scalar, FOC or DTC are used for the control of PMSMs. In [14] these three strategies have been compared where it has been found that Scalar control can only control the steady state

behaviour of the machine, while FOC and DTC can control the dynamic state as well. DTC can be implemented to the machine requiring good dynamic efficiency [15]. The FOC is chosen as the control strategy for the machine because it provides the following advantages:

- The motor torque ripple is less compared to that of DTC.
- When FOC used with Space Vector Pulse Width Modulation (SVPWM), it utilises the DC bus voltage better which adds to better speed-torque performance.
- FOC is available as an embedded algorithm in many of the micro-controllers.

2.1.1 PMSM modelling

A mathematical model of the motor should be built in order to investigate the performance of the control strategy in the simulation. As a result, this subsection contains the modeling of the PMSM motor as stated in [16]. The permanent magnet synchronous machine offers many advantages in this application when compared to other types of motors.

The machine used in the project is a High Speed Permanent Magnet Motor (HiSPEM). The description of HiSPEM used in this thesis project is provided in table 2.1.

Parameters	**Values**
Pole pairs	4
Phases	6
Stator resistance, R_s (Ω)	0.115
Stator Inductance, L_s (mH)	1.31
Flux Linkage, λ_m (V/rad/sec)	0.0187
Viscous friction coefficient (Nm/rad/sec)	0
Max speed (rpm)	60,000

Table 2.1: HiSPEM details

The HiSPEM used is a six-phase machine. The motor winding structure is shown in Figure 2.1

The modelling of HiSPEM is similar to PMSM modelling. The Figure 2.2 shows the single phase equivalent of the PMSM where V_s is the stator voltage, I_s is the stator current, R_s and L_s are the stator resistance and self inductance respectively and E is the induced back emf.

There are some assumptions made while modelling the motor which are as follows:

- The back EMF waveform is sinusoidal.
- There is no saliency in the rotor hence $L_d = L_q$.

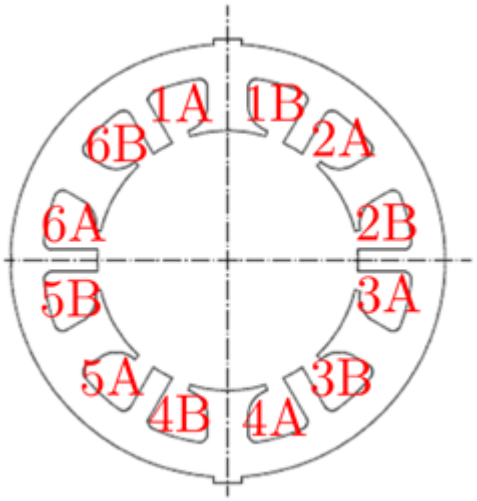


Figure 2.1: Machine stator winding structure

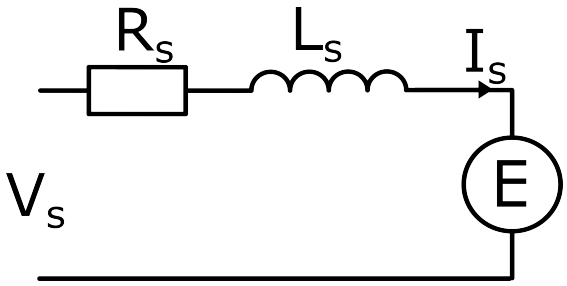


Figure 2.2: Single phase equivalence of PMSM

In three-phase equivalent the stator voltage V_s can be written as follows:

$$V_{abc} = R_s i_{abc} + \frac{d}{dt}(L_s i_{abc} + \lambda_{pm}(\theta)) \tag{2.1}$$

$$\frac{d}{dt}\lambda_{pm}(\theta) = -\omega_e \lambda_{pm} \begin{bmatrix} sin(\theta_e) \\ sin(\theta_e - \frac{2\pi}{3}) \\ sin(\theta_e + \frac{2\pi}{3}) \end{bmatrix} \tag{2.2}$$

Where,

- V_{abc}: Three-Phase voltage
- i_{abc}: Three-phase current
- $\lambda_{pm}(\theta)$: position dependent permanent magnet flux linkage
- θ_e: electrical angle

The equation 2.1 can be transferred to rotating DQ axis reference frame. Then, the dynamic equation of PMSM can written as:

$$V_d = R_s i_d - \omega_e \lambda_q + \frac{d\lambda_d}{dt}$$
$$V_q = R_s i_q + \omega_e \lambda_d + \frac{d\lambda_q}{dt} \tag{2.3}$$

where,

$$\lambda_d = L_d i_d + \lambda_m$$
$$\lambda_q = L_q i_q \tag{2.4}$$

Where,

- V_d, V_q: Voltages in synchronous rotation frame
- i_d, i_q: Currents in synchronous rotation frame
- λ_d, λ_q: Flux linkages in synchronous rotation frame.

As a result the equivalent of PMSM is obtained in DQ reference frame as shown in the Figure 2.3 The torque produced by the PMSM can be modelled considering $L_d = L_q$

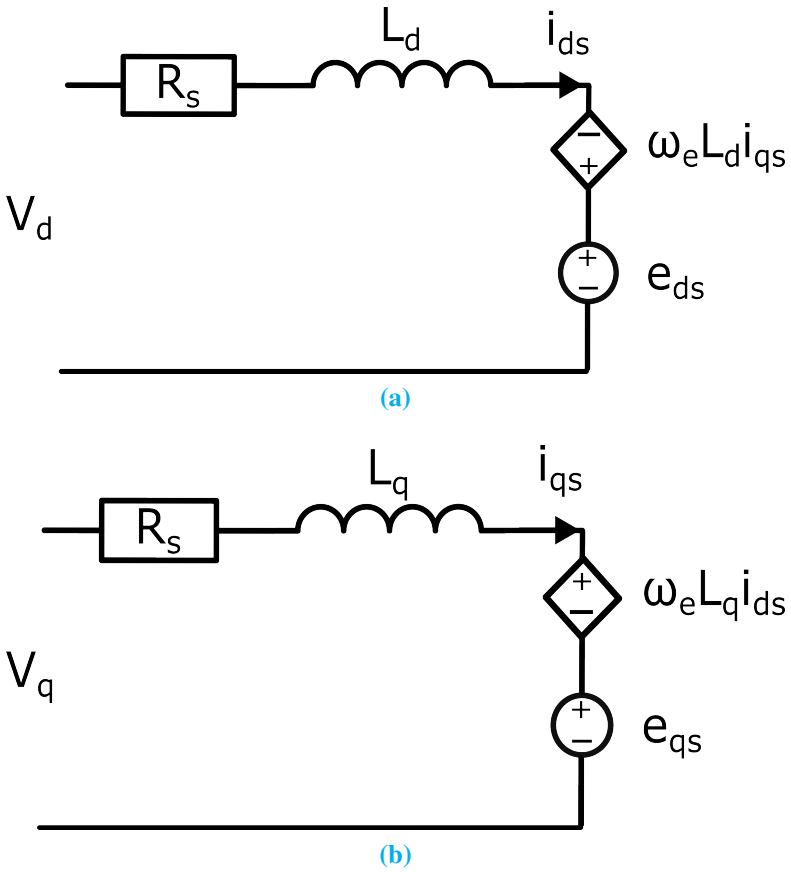


Figure 2.3: (a) D axis, **(b)** Q axis machine equivalent circuit

$$\begin{aligned} T_e &= \frac{3}{2}p(\lambda_d i_q - \lambda_q i_d) \\ &= \frac{3}{2}p((L_d - L_q)i_d i_q + \lambda_m i_q) \\ &= \frac{3}{2}p\lambda_m i_q \end{aligned} \tag{2.5}$$

As stated earlier, HiSPEM is a six-phase machine. For testing purpose, in this thesis to control the torque and speed of the machine simultaneously, the three phases are connected to speed control inverter which is acting as motor and other three phases are connected as current control rectifier acting as generator. In actual practice, the two sets of three-phase power will each be connected to their own independent inverter and will work together as either a motor or a generator.

2.1.2 Field Oriented Control

Field oriented control has been most widespread used motor control strategy and this principle has been introduced in several literature. In FOC the current vectors in abc are transformed to dq0 reference frame, separating the current into two orthogonal components i_q and i_d resulting in independent control of torque and magnetic field respectively. In VSI topology using Space Vector Pulse Width Modulation (SVPWM) the output current is controlled by the output voltage which is given by the DQ voltages in equation 2.6

$$\begin{aligned} V_q &= R_s i_q + L_q \frac{di_q}{dt} + \omega_e L_d i_d + \omega_e \lambda_m \\ V_d &= R_s i_d + L_d \frac{di_d}{dt} - \omega_e L_q i_q \end{aligned} \tag{2.6}$$

It can be noted in the equation 2.6 that the D and Q voltages are coupled with each other and need to be decoupled. This decoupling can be achieved by eliminating the other axis parameters in the respective equations. The decoupling can be achieved as shown in the figure 2.4

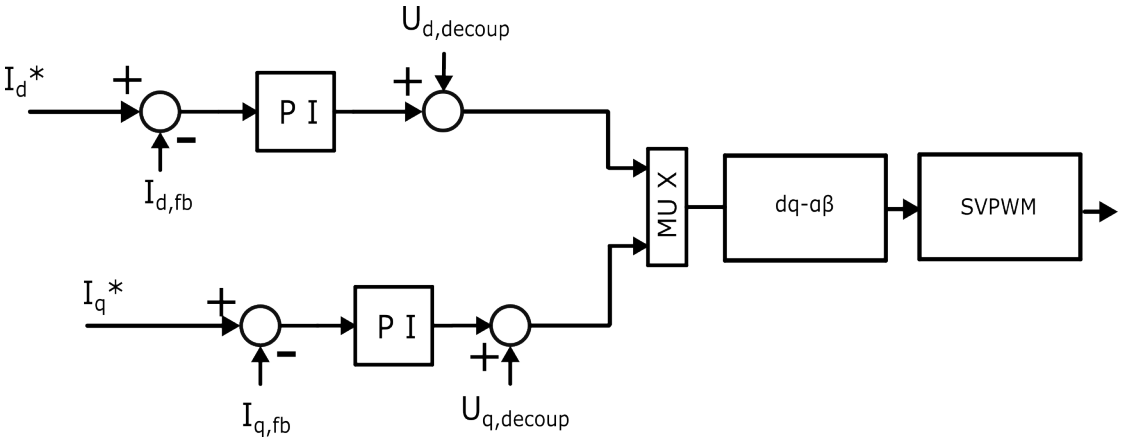


Figure 2.4: Method of decoupling d and q current

The decoupling parameters is provided in the equation 2.7. After the decoupling, these DQ voltages need to be converted in $\alpha - \beta$ reference frame to be fed to the SVPWM modulator to produce gate pulses accordingly.

$$\begin{aligned} U_{d,decoup} &= -\omega_e L_d i_{q,fb} \\ U_{q,decoup} &= \omega_e (L_q i_{d,fb} + \lambda_m) \end{aligned} \tag{2.7}$$

At first the internal PI controller is tuned by giving a step input and keeping the machine stationary. The PI speed controller from the load transfer function as shown in the equation 2.8 where the K_{pi} and K_{ii} are the proportional and integral gain.

$$\begin{aligned} \frac{i(s)}{u(s)} &= \frac{1}{sL+R} \\ PI(s) &= K_{pi}(1+\frac{K_{ii}}{s}) \\ G_{loop}(s) &= PI(s)\frac{i(s)}{u(s)} \\ &= K_{pi}\frac{s+K_{ii}}{s}\frac{1}{sL+R} \end{aligned} \tag{2.8}$$

By pole-zero cancellation in loop gain and forming the closed-loop, K_{pi} and K_{ii} can be set as shown in the equation 2.9 where BW is the bandwidth in rad/sec which should be smaller than the switching frequency bandwidth [17].

$$\begin{aligned} K_{ii} &= \frac{R}{L} \\ K_{pi} &= L.(BW) \end{aligned} \tag{2.9}$$

The tuning of speed PI controller can be achieved by using the transfer function of the speed loop as shown in the figure 2.5 and equation 2.10, where the K_{ps}, K_{is} are the proportional and integral gain, ω_B is the bandwidth of the speed controller and J is the combined inertia of the machine and load assuming the damping coefficient (ζ) of the speed transfer function is 1 [17]. The closed loop frequency bode plot shown in figure 2.6 shows the bandwidth of controller to be less than already decided which is due to straight line asymptotic approximation according to 20 dB/decade gradient.

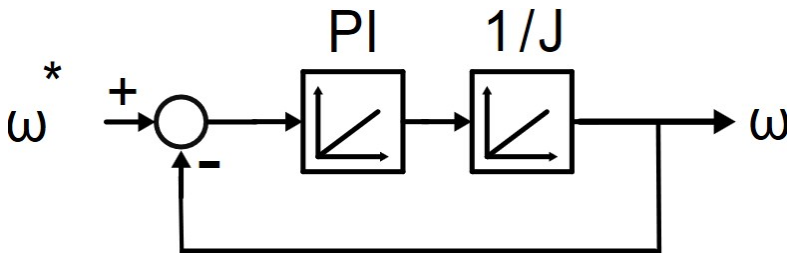


Figure 2.5: Speed feedback loop

$$K_{ps} = \omega_B J$$
$$K_{is} = \frac{(\omega_B)^2}{4} \tag{2.10}$$

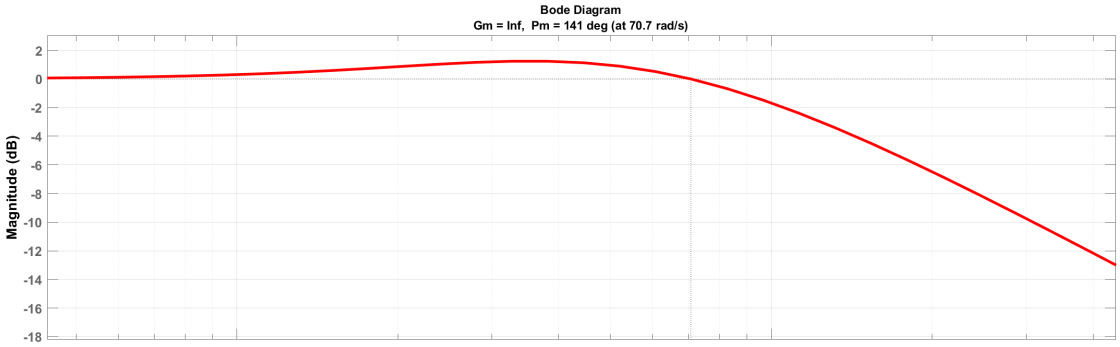


Figure 2.6: Closed loop frequency bode plot for speed controller tuning

The output voltage and current response when the machine is running at a speed of 30,000 rpm is shown in the figure 2.7. The output voltage is a pulsating square wave and while the output current is a sinusoidal with some ripples.

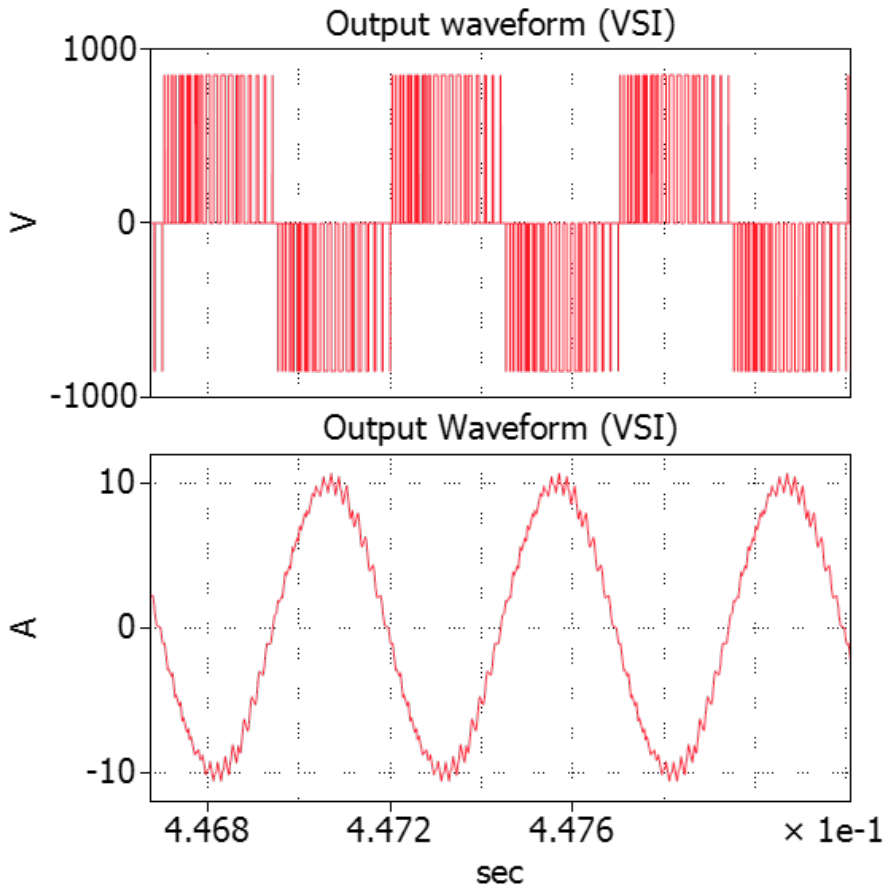


Figure 2.7: VSI output voltage and current waveform

2.1.3 Modulation

Space Vector Pulse Width Modulation is used with Field Oriented Control as it reduces the harmonics and as well as has their inherent connection with FOC. After the decoupling, these DQ voltages as shown in figure 2.4 they need to be converted in $\alpha - \beta$ reference frame to be fed to the SVPWM modulator to produce gate pulses for switches in the inverter.

The Space Vector Modulation for Voltage Source Inverter have six active vectors and two zero vectors as shown in the figure 2.8. The reference voltage vector can be produced by switching the two nearest active vectors for time T_1 and T_2 and the rest time is T_0 is provided to the zero vector [18]. A symmetrical 7 segment SVPWM is used because of its inherent reduction in harmonics behaviour.

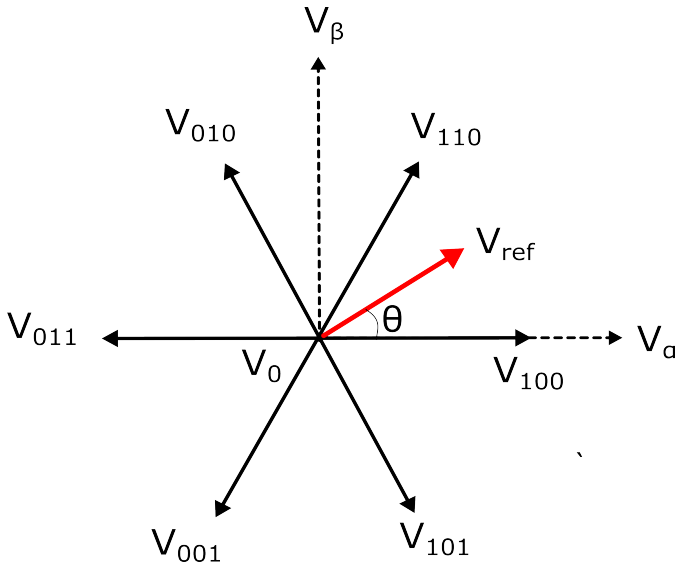


Figure 2.8: Space Vectors for VSI-IMMD

Space Vector is divided into 6 different sectors in $\alpha\beta$ frame. The switching state is then decided on the sector in which the vector currently is. After sector determination, the angle θ is calculated for each switching frequency and then the switching time is calculated for each state as given in equation 2.11. The m_a in the equation is called modulation index and is the ratio of output voltage to reference DC voltage.

As an example, figure 2.8 shows how the reference vector is synthesised in sector 1. The two active vectors are V_{100} and V_{110} and the zero vectors are V_{000} and V_{111}. The reference vector making an angle θ can be synthesize by switching on the active vector V_{100} for T_1 seconds, V_{110} for T_2 seconds and zero vector V_{111} for T_0 seconds.

$$\begin{aligned} T_1 &= m_a sin(\pi/3 - \theta) \\ T_2 &= m_a sin(\theta) \\ T_0 &= T_S - T_1 - T_2 \\ m_a &= \frac{\sqrt{3}V_{ref}}{V_{dc}} \end{aligned} \tag{2.11}$$

2.2 Motor drive loss modelling

2.2.1 MOSFET loss modelling

The MOSFET used in the drive is a silicon carbide (SiC) MOSFET with internal body diode in TO-263-7 package where it has a common drain and case. The overall losses in the drive can be accounted to losses in MOSFET during the operation and hence modelling of MOSFET becomes very critical to determine the thermal and loss behaviour of the drive.
In overview, the loss in MOSFET consists of conduction and switching loss and parasitic loss in the internal diode, which is not very significant. More detail on the losses could be found below:

- Conduction Loss: Conduction loss is the loss occur in the MOSFET when the MOSFET is conduction or switched on. It is caused by the internal resistance $R_{ds,on}$ which is dependent on the current i_{on} as well as the junction temperature T_j. The instantaneous conduction loss can be given by the equation 2.12

$$P_{cond} = R_{ds,on}(i_{on}, T_j) * i_{on}(t)^2 = V_{on}(i_{on}, T_j) * i_{on}(t) \tag{2.12}$$

  The $R_{ds,on}$ is dependent on the on-state voltage between drain and source V_{on} which changes with respect to i_{on} and T_j. From the data-sheet [19] the $R_{ds,on}$ can be calculated and be used for calculation initiation. The loss generated would increase the junction temperature which in turn would increase the $R_{ds,on}$ and increase the losses again till temperature gets steady. At high current levels the temperature can reach at very high level which can lead to thermal runaway condition in MOSFET. SiC MOSFET are less prone to such condition compared with Si MOSFET.

- Switching loss: Switching loss is the loss occur during the turn on (E_{on}) and turn off (E_{off}) of the MOSFET as shown in the figure 2.9 where E_{on} and E_{off} are energy losses in Joules. During switching of the MOSFET, the loss is incurred due to drain-source voltage V_{block}, conduction current i_{on} and junction temperature T_j.

  The switching loss for MOSFET for switching frequency of f_s is given in equation 2.13

$$P_{sw} = f_s[E_{on}(i_{on}, V_{block}, T_j) + E_{off}(i_{on}, V_{block}, T_j)] \tag{2.13}$$

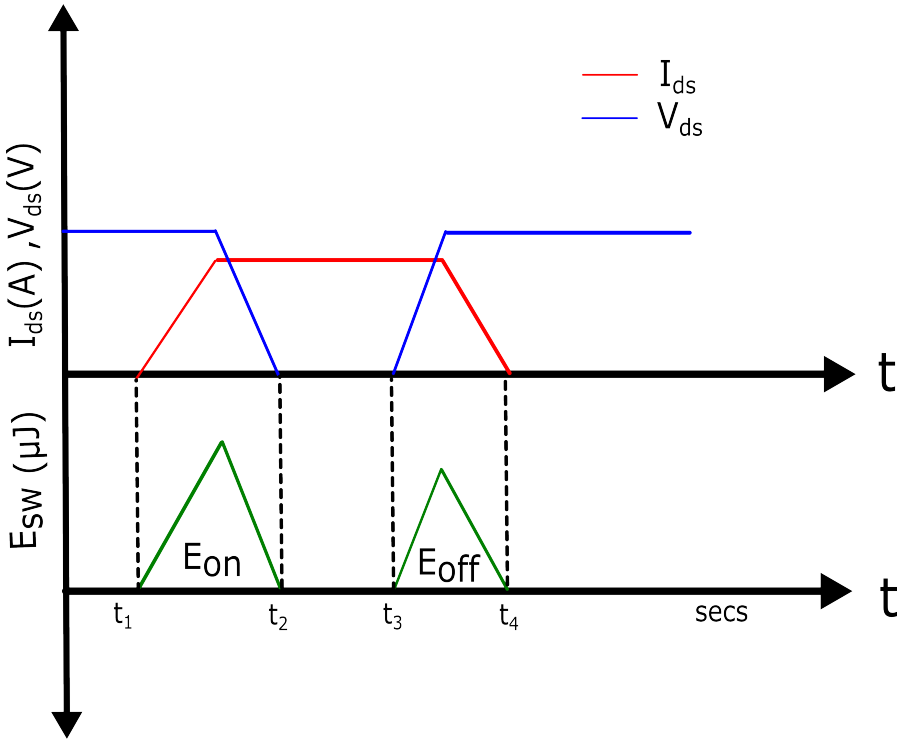


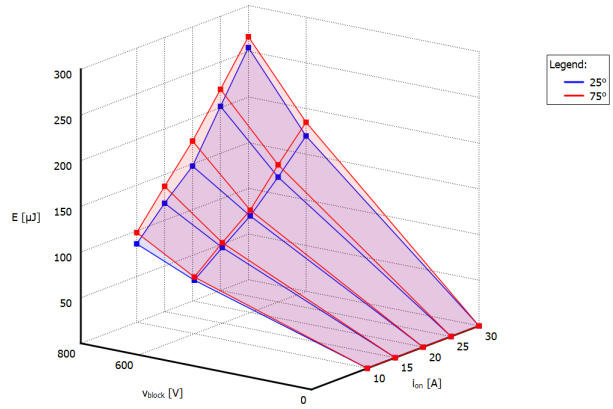
Figure 2.9: Switching loss in one switching cycle of MOSFET

The power losses in the body internal diode is neglected due to following reasons:

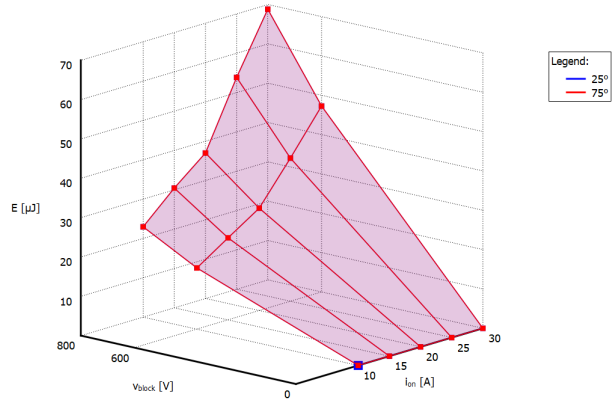
- The diode conduction time is very short for conduction loss

- The reverse recovery charge for the feedback diode in SiC MOSFET is not significant and can be neglected compared with losses in MOSFET itself.

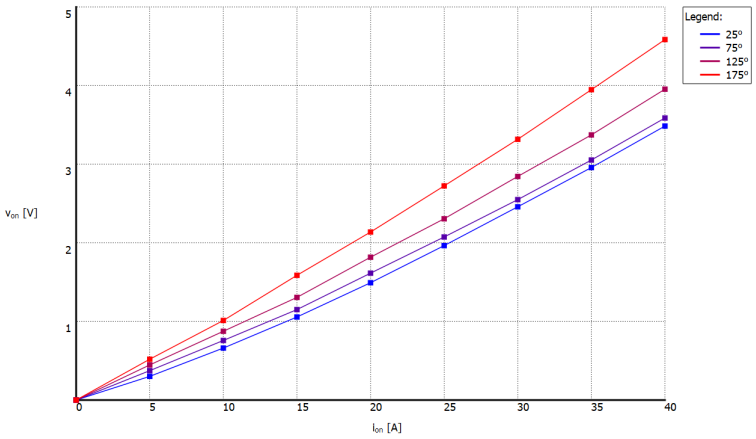
The figure 2.10 shows the 3-D and 2-D lookup graphs for switching and conduction loss respectively.



(a)



(b)



(c)

Figure 2.10: The switching loss during **(a)** on, and **(b)** off at different temperatures and current, **(c)** Conduction loss of MOSFET at different temperatures

Loss characteristics of GenSiC G3R75MT12J

Since the conduction loss is simple to evaluate from the data-sheet, the switching energy loss does not provide a exact losses as the data that has been prepared in data-sheet is at different external conditions as compared to the experimental setup in Electrical Sustainable Power Lab. As a result, measuring is required in order to obtain reliable results [20].
Use of hardware for measurement not only increases cost but also requires time to be built for each different switches. To resolve this issue, a virtual Double Pulse Test (DPT) was established using spice models of the GenSiC G3R75MT12J MOSFET. as shown in the figure 2.11.
Double pulse is an evaluation technique for measuring switching parameters and assessing the dynamic behaviors of power devices. The objectives of conducting a DPT are as follows:

- Ensure that data-sheets for power devices such as MOSFETs and IGBTs are accurate.
- Validate the actual value or variation of the power devices or modules.
- These switching parameters can be measured with a variety of current values and devices.

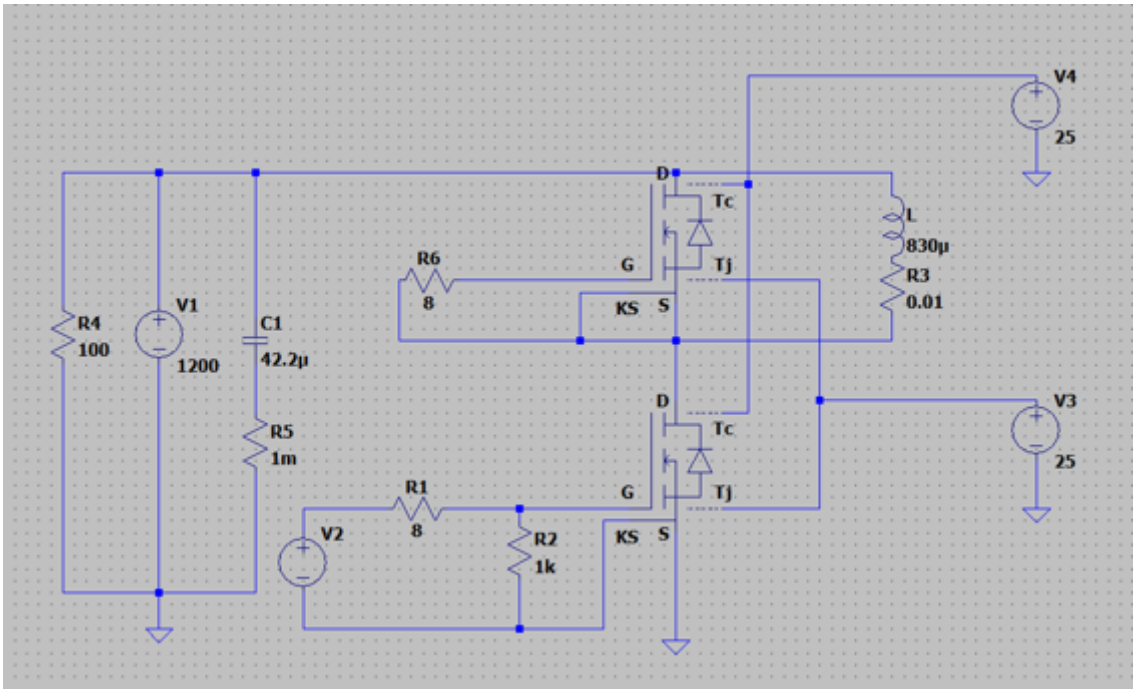


Figure 2.11: Schematics of Double Pulse Test conducted on GenSic G3R75MT12J

In the test configuration, the gate resistances and gate driver voltage are chosen based on manufacturer recommendations. This test arrangement can be utilized in the future to compare various wide band-gap switches based on the rise/fall time and switch losses.

The test can be performed under a variety of situations that can provide insight into the

loss and thermal behavior of the SiC MOSFET. In this project, the test was conducted on 120V and 10 A because the experiments are conducted on the same operating parameters. The behavior of a selected SiC MOSFET and the losses sustained during switching are depicted in 2.12. When the switching frequency f_{sw} is ranging between 10-30 kHz the switching losses are very less compared to conduction loss when the switch is operating at low voltage while at high switching frequencies and high voltage the switching loss becomes larger than conduction loss.

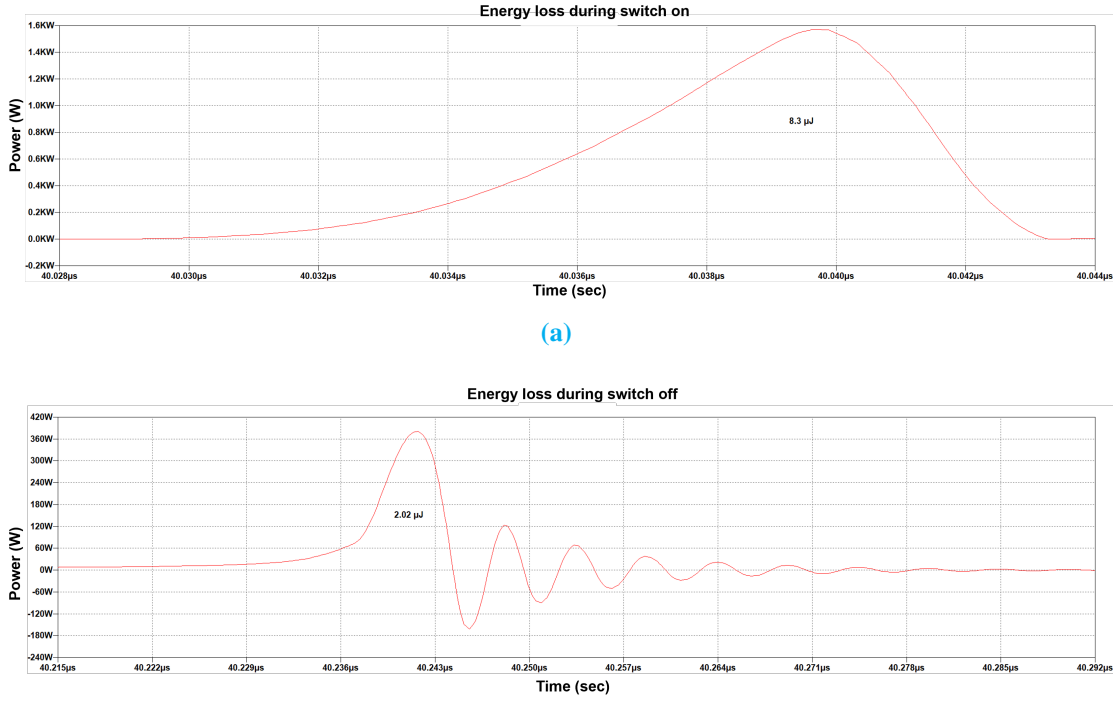


Figure 2.12: **(a)** Turn on energy loss, and **(b)** Turn off energy loss of G3R75MT12J SiC MOSFET at 120V, 10A and 25°C ambient temperature

2.2.2 Detailed inverter loss

In this project, the Voltage Source Inverter uses two SiC MOSFETs (M_{i1} and M_{i2}) in parallel as shown in figure 2.13 in place of a single MOSFET. Using parallel MOSFETs, on one side the conduction loss can be halved while on the other side the switching losses will increase.

The losses of inverter mainly consists of conduction and switching losses in the power semiconductor device which is given by the equation 2.14. The losses in the passive components such as DC link capacitors C_{dc} are not significant since the input voltage doesn't have ripples. The DC link capacitor used in the VSI in this project is film capacitor having very low de-rating factor and Equivalent Series Resistance (ESR). Hence the losses incurred in the capacitor is not significant compared to losses in power semi-

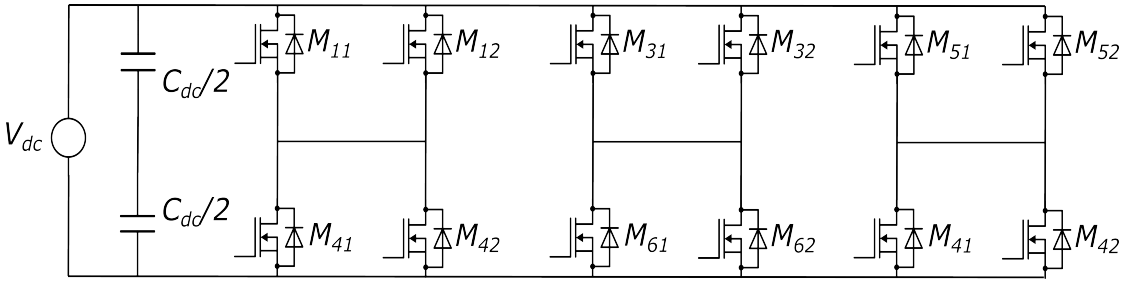


Figure 2.13: Voltage Source Inverter circuit

conductors and thus are neglected in the loss evaluation of the motor drive.

$$P_{loss} = \frac{1}{N} T_1 \left(\int_0^{T_1} \sum_{i=a,b,c} (P_{cond,lower}(t) + P_{cond,upper}(t) + \sum_{1}^{m} \sum_{i=a,b,c} E_{sw} f_{sw} \right) \tag{2.14}$$

Here N is the number of parallel switch, m = $\frac{T_1}{T_s}$,T_1 is the fundamental time period and T_s is the switching time period, f_{sw} is the switching frequency $P_{cond,lower}$ and $P_{cond,upper}$ is the conduction loss in the lower and upper segment of the inverter respectively [21]. The loss model serves as the starting of the thermal model where the junction temperature forms a close loop with the loss model and then a combined model is produced which includes both thermal and loss behaviour of the inverter during the operation .
Two loss models are derived based on the VSI topology. The first model includes the motor inverter model where exact system is modelled in PLECS as shown in the figure 2.14. While a second approximate loss model is prepared using 2D lookup table for conduction loss and 3D lookup table for switching loss for thermal modelling of the system as shown in the figure 2.16. The lookup table model serves as the approximate model for the motor inverter model and saves time in evaluating junction temperature at different operating conditions at course of time, which takes a large amount of time in the motor-inverter model.

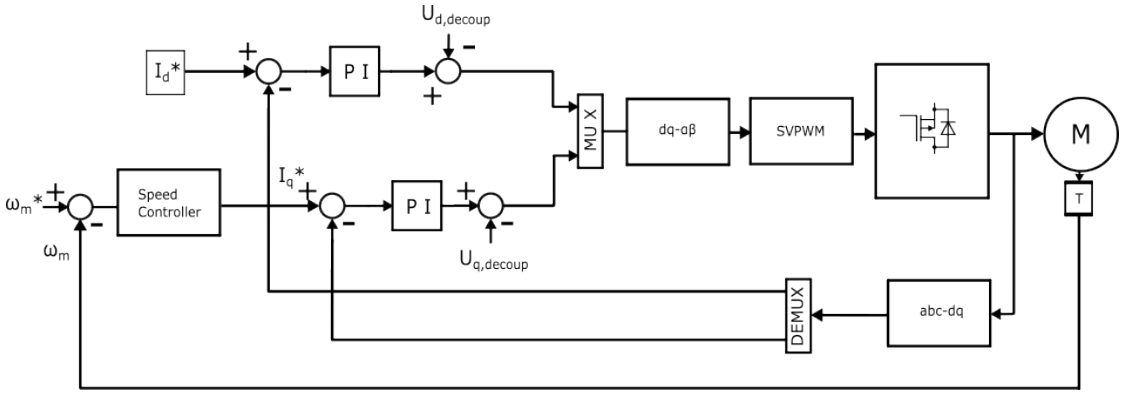


Figure 2.14: Speed controlled motor inverter model

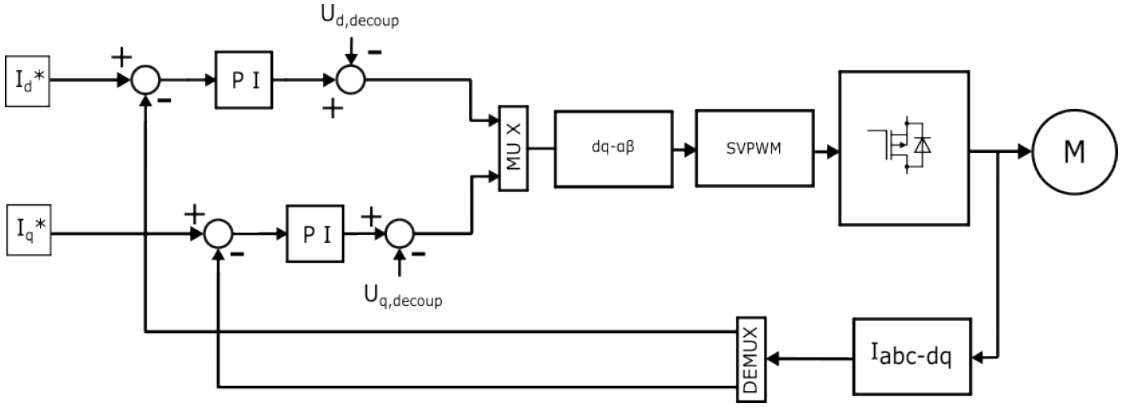


Figure 2.15: Current controlled generator rectifier model

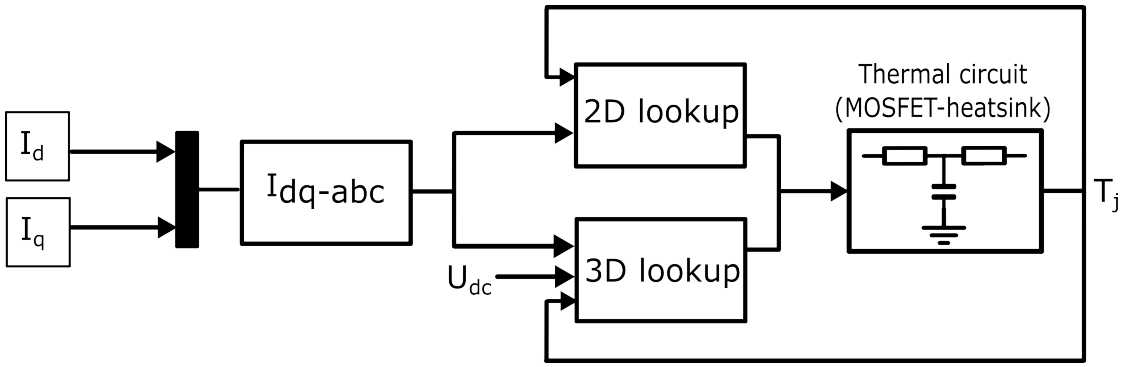


Figure 2.16: Lookup table thermal model for VSI-IMMD

2.3 IMMD system thermal modelling

2.3.1 Thermal modelling fundamentals

To analyze the thermal behaviour of the system, the equivalent thermal circuit based model is the most popular, because of the simplicity of the model and providing approximate thermal states of the drive. In general the thermal model transforms the flow of power and rise in temperature to an electrical network where the power loss is depicted by an ideal current source, temperature as a voltage source and the material through which the heat propagate as a combination of resistors and capacitors. The resistors is analogous to the resistance offered to the heat flow while the capacitor determines the transient state of the thermal circuit.
In 1-D thermal thermal modelling certain assumptions are mode, which are as follows [22]:

- The heat transferring to vertical direction is only accounted for temperature rise while the horizontal heat transfer is neglected.
- Only conduction heat is accounted in the analysis while the convection and the radiation heat transfer are neglected except on the surface of the heat sink.

The figure 2.17 shows the general structure of a SiC MOSFET connected to a heat sink. Since the TO-263 package SiC MOSFET chosen in this project shares the casing and drain section, there is no thermal pad/paste and a direct connection with very low thermal resistance can be assumed between the case and heat sink.

Figure 2.17: Thermal heat dissipation structure of To-263 SiC MOSFET

There are two ways by which 1-D thermal modelling can be achieved. The first one uses a Foster network as shown in figure 2.18. In Foster network the thermal resistance and capacitance are connected in parallel. This model signifies the mathematical interpretation of the system while doesn't provide the physical temperature distribution in the system. On the other hand, the second modelling methods uses Cauer network, in which the thermal resistances and capacitor are connected in T network configuration as shown in the figure 2.19. It provides the information of physical temperature distribution in the thermal network. Since the manufacturer could only provide the thermal impedance of one components instead of whole network, Cauer network seems to be the best model to be implemented as in Foster network no two different model can be added in series rather in Cauer they can be added directly in series with the existing thermal model [23]. The thermal impedance data of SiC MOSFET and heat sink is available separately hence in this project the thermal modelling is performed using Cauer thermal network.

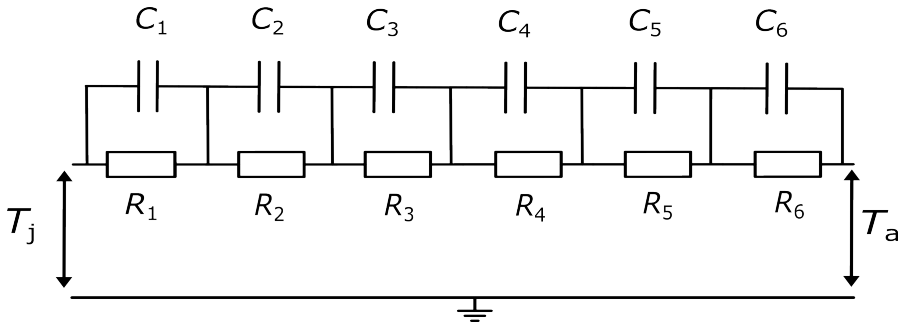


Figure 2.18: Foster thermal network

In the figure 2.19, the Cauer thermal circuit used for modelling is shown. The junction to case thermal resistance is indicated by set of series resistances forming R_{jc}. Expanding the junction to case thermal resistance to several series combinations of thermal resistors and capacitors (R_n,C_n, where n=1...4) improves the modelling accuracy, as it denotes the several points that are taken from the thermal impedance graph of the SiC MOSFET. The case to sink and sink to air thermal resistance in denoted by R_{cs} and R_{sa}

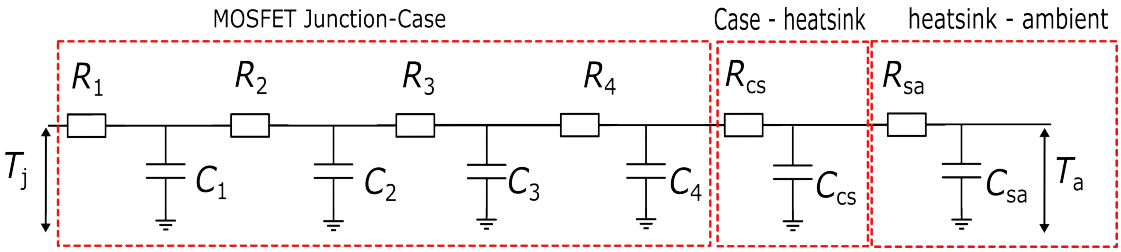


Figure 2.19: Cauer thermal network

respectively.Similarly the thermal capacitance of casing and heat sink is denoted by C_{cs} and C_{sa} respectively.
The thermal resistance is dependent on the length of material, cross area of the the heat flows and thermal conductivity of that material. While the thermal capacitance is dependent on thermal capacity and mass of the material.

2.3.2 Thermal circuit parameters

The thermal parameters of the Gen SiC MOSFET is given in the table 2.2. The thermal parameters are deduced from the thermal impedance graph in the data-sheet. The thermal impedance graph provides the thermal impedance for different duty cycles. The curve with duty cycle corresponding to 0.5 is chosen since the average duty cycle is approximately 0.5. Choosing different points in the curve provides sets of capacitors and resistances which improves the model accuracy and hence the thermal resistance and capacitance can be obtained as shown in the table 2.2.

Thermal Resistance R_{jc}	0.64 - 0.77 K/W
R1 (K/W)	1.248E-02
C1 (J/K)	9.516E-05
R2 (K/W)	7.075E-02
C2 (J/K)	7.2E-04
R3 (K/W)	0.2707
C3 (J/K)	1.647E-03
R4 (K/W)	0.4012
C4 (J/K)	0.0425

Table 2.2: Junction to Case thermal parameters of Gensic G3R75MT12J

The heat sink used in the project is AAVID 7016 [24], which a surface mount board level heat sink designed to cool D2 pak devices (TO-263). It is a tin plated copper heat sink which makes it more thermally conductive as compared to aluminium heat sink. The dimensional property is shown in the table 2.3. The thermal resistance can be calculated from the data-sheet of the heat sink which is based temperature rise and heat dissipated. The graph also shows the relation of thermal resistance with respect to air velocity. Since the cooling of the heat-sink in the project is through natural convection hence the curve at nil air flow velocity is only taken into consideration. The thermal capacitance can be calculated from the mass of the heat sink as shown in the equation

2.15 where c is the specific heat capacity (Joules/Kelvin/Kg) and M is the mass of the heat sink in Kg.

$$C_{thermal} = cM \tag{2.15}$$

Material	copper
Mass	2 g
Thermal resistance	20°C/W

Table 2.3: Heat sink thermal parameter

Since the case is soldered to the heat sink the case-sink thermal resistance, R_{cs} becomes negligible and hence is neglected in the model. To save time during simulation, a lookup table loss model is prepared as shown in the figure 2.16.

2.4 VSI model verification

An experimental setup is set up as shown in the figure 2.20 which is used to verify the loss and thermal model of VSI in PLECS. The table 2.4 shows the operating parameters for both the experiment and PLECS's loss and thermal model. The operational speed is restricted to lower speed ranges due to the defects in bearing of the HiSPEM.

DC bus voltage (V)	120
Reference machine speed (rpm)	3000

Table 2.4: Operating parameters for experimental setup and PLECS model

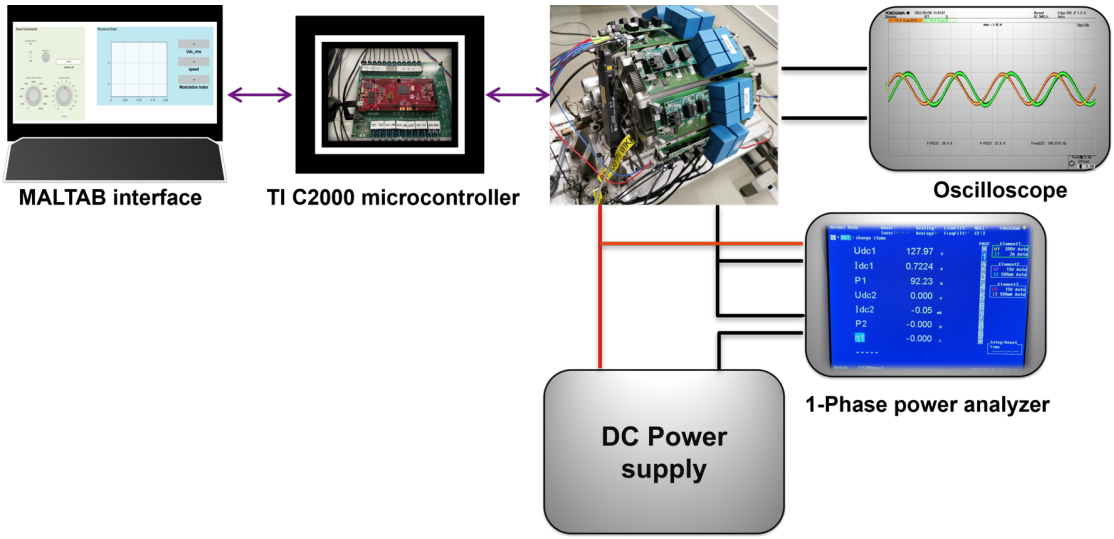


Figure 2.20: VSI-IMMD experimental setup

2.4.1 Experimental setup loss comparison

The figure 2.21 shows the flow of power in the VSI-IMMD system. The HiSPEM machine is divided into two parts, the first part acts like a motor connected to a speed controlled inverter and the second part acting as generator connected to a current controlled rectifier. The power transferred from the motor to the generator is denote by P_{mech}. The copper and rotational losses in the motor are denoted by P_{Cu} and P_r. The losses in the converters is given by P_D for inverter and rectifier.

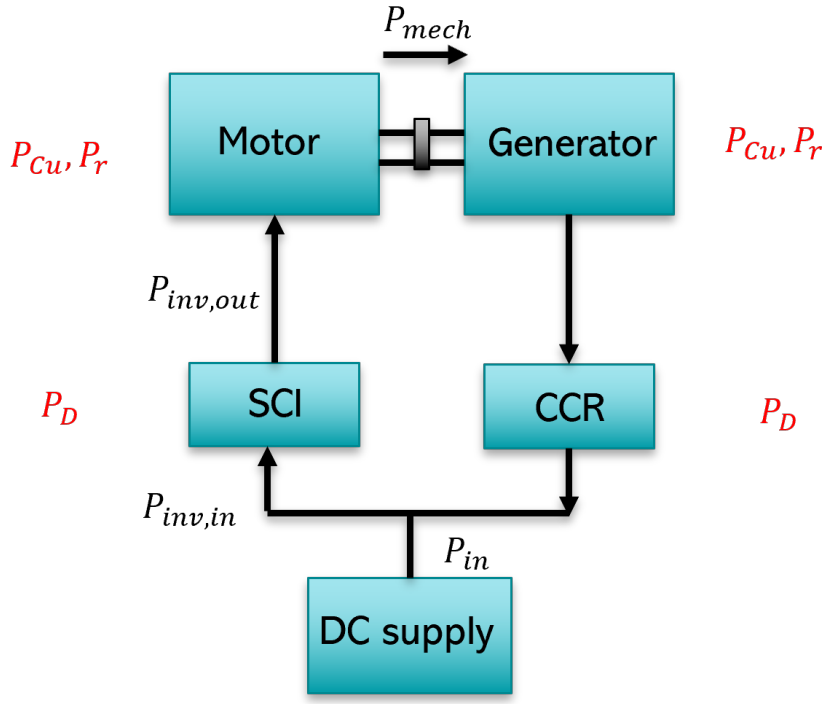


Figure 2.21: Power flow in the VSI-IMMD system

At steady state the input power P_{in} from the DC bus consists of losses in the system. The power transferred from the motor to the generator is given by equation. Since it is assumed that there is no saliency in the rotor, $L_d = L_q$. The mechanical power generated is shown in the equation 2.16

$$\begin{aligned} P_{mech} &= \frac{3}{2} p\omega_m((L_d - L_q)i_d i_q + \lambda_m i_q) \\ P_{mech} &= \frac{3}{2} p\lambda_m \omega_m i_q \end{aligned} \tag{2.16}$$

Taking the inverter side of the system into consideration, the efficiency of the inverter at steady state can be calculated by using equation 2.17.

$$\begin{aligned} P_{inv,out} &= P_{Cu} + P_r + P_{mech} \\ P_{inv,in} &= P_{Cu} + P_r + P_{mech} + P_D \\ \eta_{inv} = \frac{P_{inv,out}}{P_{inv,in}} * 100\% &= \frac{P_{Cu} + P_r + \frac{3}{2} p\lambda_m \omega_m i_q}{P_{Cu} + P_r + \frac{3}{2} p\lambda_m \omega_m i_q + P_D} * 100\% \end{aligned} \tag{2.17}$$

Where P_{Cu} is the three-phase stator copper loss.
The table 2.5 shows the total power loss of the IMMD system in both experimental setup and simulation model. The difference in the experimental and PLECS model is due to the assumptions that have been made while modelling and the fact that during the experiment the temperature of the system continued to rise with time while the PLECS model simulation for done for a shorter time and at constant temperature input of 25°C. Moreover the PCB traces loss and rotor friction loss are neglected, stator iron loss is assumed to be constant and the MOSFET's loss is modelled by assuming linearity in the data points at different temperatures, voltages and current levels. The gate driver in the experiment setup is situated right above the case of the SiC MOSFET and creates a hot-spot in the area leading to additional losses in the inverter than expected. Table 2.6 compares the calculated drive loss from the experimental setup to the PLECS IMMD system model.

I_q (A)	Loss model (W)	Experiment (W)
5	24	30.5
7	34	43
9	48.5	59
11	66.2	80.5

Table 2.5: VSI-IMMD system loss comparison

I_q (A)	Model drive loss (W)	Experimental Drive loss (W)
5	2	4.68
7	3	6.80
9	4.2	9.23
11	6.2	13.13
13	9.8	17.39

Table 2.6: Drive loss evaluation for experiment setup vs IMMD system model in PLECS

The table 2.7 provides the efficiency of the VSI modelled in PLECS at the operating condition. The efficiency ranges from 98-99% is due to operation at low voltage and medium switching frequency levels which reduces the switching losses significantly and use of parallel SiC MOSFET reduces the conduction loss.

I_q (A)	Efficiency (%)
5	99.07
7	98.87
9	98.78
11	98.59
13	98.39

Table 2.7: VSI-IMMD model efficiency at different current level

The graph in the figure 2.22 shows the comparison of the system loss between experimental setup, and IMMD system in PLECS. The difference in system losses starts widening after increasing current which accounts to the linearity considered while modelling MOSFET in PLECS.

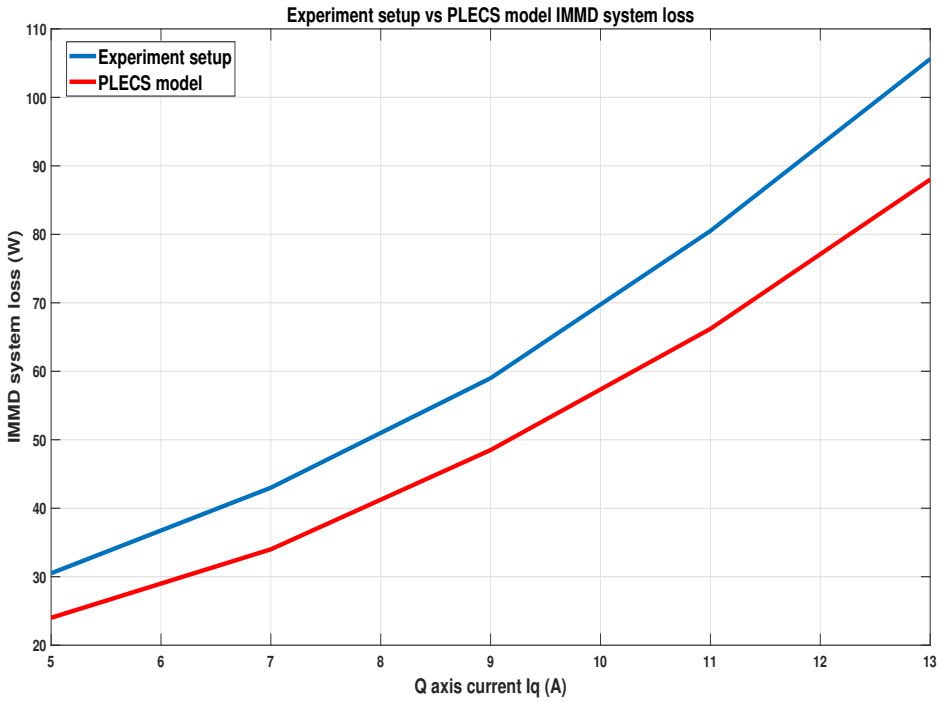


Figure 2.22: Experiment setup and IMMD system model in PLECS

2.4.2 Experiment setup thermal behaviour comparison

The table 2.8 shows the steady state temperature rise in the case temperature of the SiC MOSFET in the experiment setup and in the simulated thermal model. The figure 2.23 shows the temperature rise at different Q axis current levels.

I_q (A)	Thermal model ($^\circ C$)	Experiment model ($^\circ C$)
5	28	35.8
7	30	38.8
9	33	41.9
11	36	44
13	40	46.7

Table 2.8: Experiment vs PLECS thermal model case temperature comparison

The figure 2.23 shows the rise time for steady temperature is around 10 minutes and hence the interval for measuring temperature in the experiment was kept 10 minutes after change in current. The figure 2.24 shows the case temperature at different Q axis

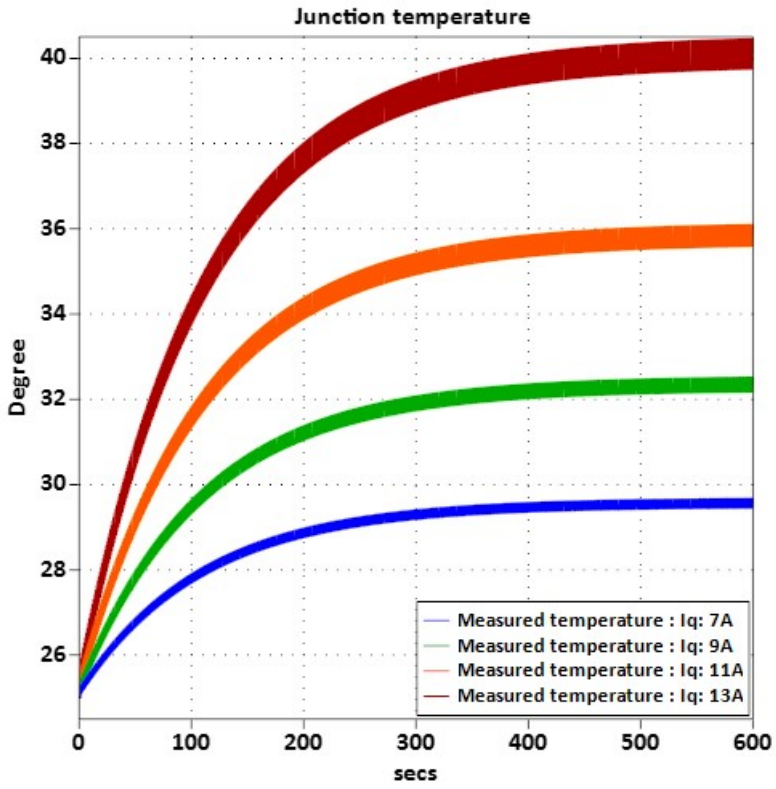
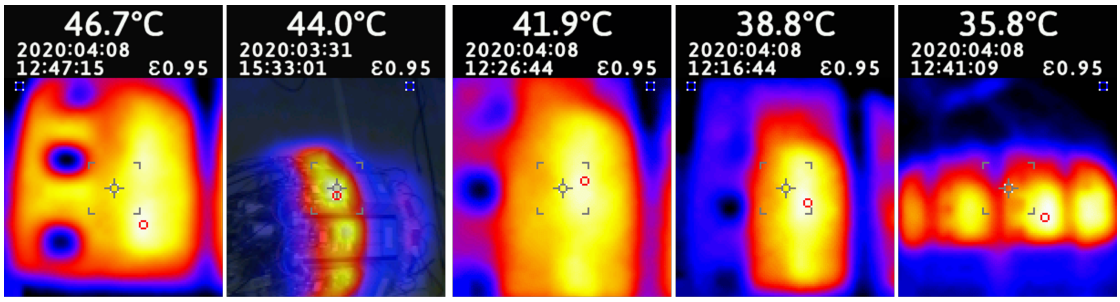


Figure 2.23: Junction temperature rise for SiC MOSFET at different Q axis current levels

current reference. The temperatures measured at the experiment setup are higher than the lookup thermal model, which can be accounted to the hot-spot generated by the gate driver situated just above the case, hence altering the surrounding of case and linearity considered in the loss modelling of the SiC MOSFET.



(a) (b) (c) (d) (e)

Figure 2.24: Case temperature at (a) 13A, (b) 11A, (c) 9A (d) 7A and (e) 5A

Apart from the steady state temperature offset the thermal behaviour depicted by both the experiment setup and PLECS model are similar.

2.5 Summary

In this chapter, 1-D modelling of both loss and thermal of the VSI-IMMD were discussed and following conclusions can be made:

- The accurate loss modelling of the inverter is difficult as several losses contributed by parasitic capacitance and inductance, PCB traces, gate drivers are ignored and assumption of linearity factored into the SiC MOSFET model, constant stator loss.
- 1-D thermal modelling is simple and provide approximate thermal behaviour of the switches in the drives but it doesn't include the thermal hindrance caused by the nearby devices which are not electrically connected to it.
- The speed and current control of the HiSPEM IMMD system was modelled in the PLECS and the response of both current and speed was verified with the experimental setup.
- Overall, the VSI-IMMD model has an excellent dynamic speed response obtained by tuning the PI controller with the help of transfer function of the system as shown in appendix B.1. The loss, and thermal analysis can be performed at greater switching frequencies and machine speeds.

CHAPTER

3

MODELLING OF CSI-IMMD SYSTEM

In this Chapter, the following points will be discussed:

- Modelling of control system for CSI topology for IMMD.
- Power loss modelling of SiC MOSFET and the converter.
- Thermal loss modelling of SiC MOSFET and the converter.
- Loss and thermal behaviour at high speed.

3.1 Control strategy

Before diving into the control strategy used in the modelling of Current source Inverter, it is important to understand the difference in operation of CSI to that of VSI.
The first basic difference is the active vectors in CSI has only two switches in operation compared to three switches in VSI. The second difference is the creation of zero vector by short circuiting one phase. The third major difference is the need to have the output capacitors which help in commutation of the switches and filter out higher order harmonics. The control used in the thesis for CSI is the multi-loop current control methodology. Thus the CSI has an inherent ability of harmonics reduction.

3.1.1 PMSM modelling

The modelling of PMSM is performed exactly as in VSI-IMMD system

The machine used in the project is a High Speed Permanent Magnet Motor (HiSPEM). The description of HiSPEM used in this thesis project is provided in table 2.1.

3.1.2 Multi-loop current control

Since the double-loop FOC is used in VSI-IMMD, in CSI multi-loop FOC is used. The inclusion of the output capacitor in CSI-IMMD leads to multiple loops from both filter output as well as from inverter output [25]. The figure 3.1 shows the control of CSI-IMMD with different loops. At first the speed controller converts the speed error to reference stator current in DQ reference frame using discrete PI controller. This reference current is compared with the sampled feedback stator current in DQ form and the error is fed to current PI controller which provides the stator voltage. The stator voltages in DQ form are still not completely decoupled from each another so in next step decoupling of DQ voltage is performed along with voltage compensation through feed-forward strategy.

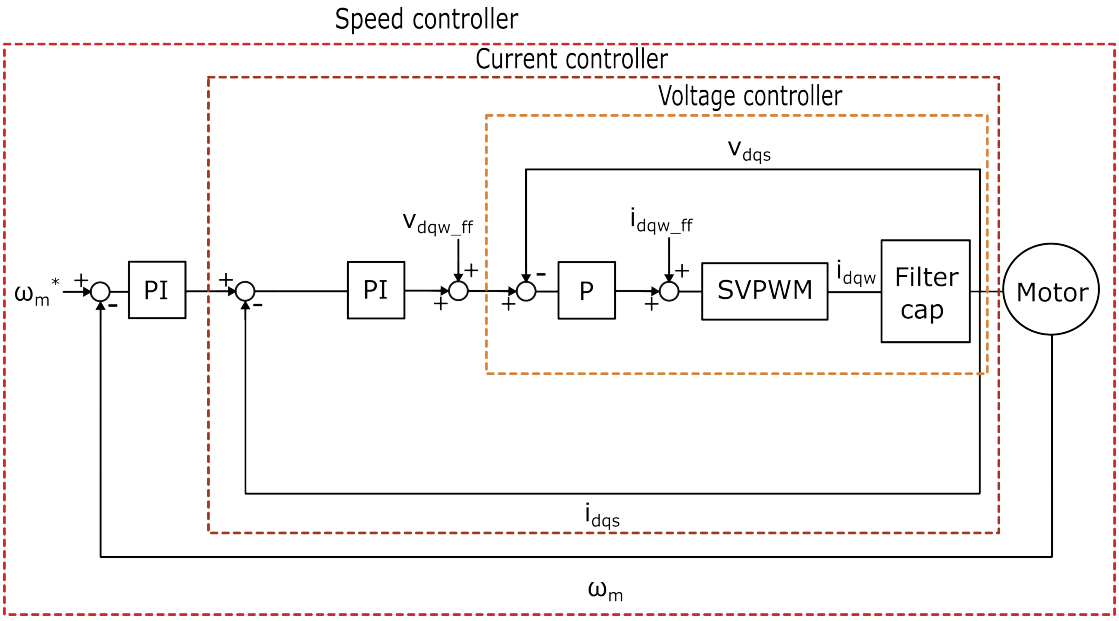


Figure 3.1: Control strategy for CSI-IMMD

After the voltage feed-forward compensation, the stator reference voltage V=v^*_{dqs} is compared with the sampled filter capacitor voltage feedback v_{dqs} and the error is provided to a discrete proportional controller to convert it into inverter output current i_{dqw}. The inner loop merely employs a basic proportional compensator, as steady-state errors do not impact the accuracy of the outer loop [26]. As it can been seen in the figure 3.2, the inverter output current are coupled by the constant current source and hence need to be decoupled.

The control strategy of the CSI-IMMD is shown in figure 3.1. The current feed-forward component i_{dqw_ff} consists of the dependent current source introduced by transforma-

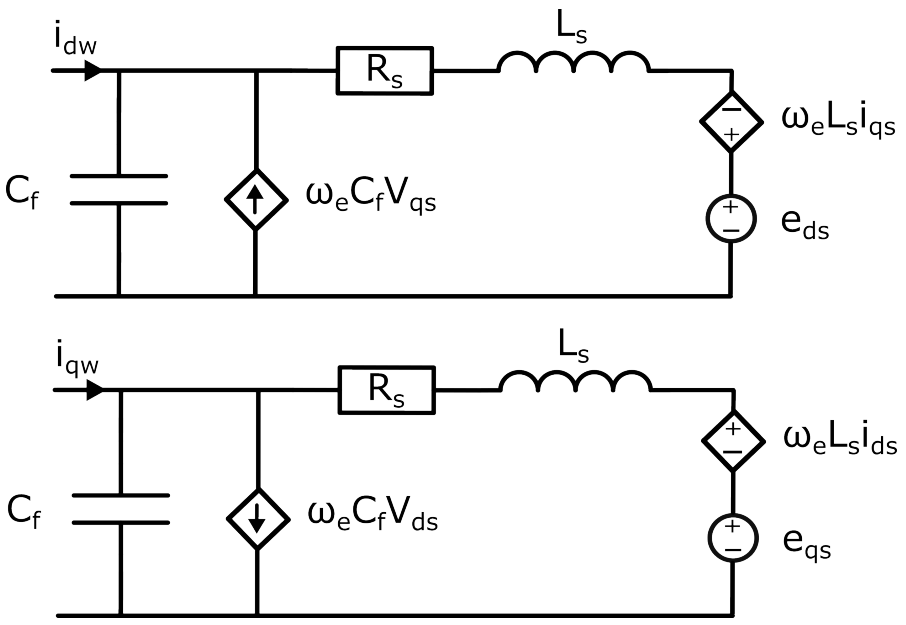


Figure 3.2: Equivalent circuit of CSI's capacitor filter and PMSM system in synchronous reference frame

tion of filter circuit in synchronous reference frame and the stator DQ current as shown in the equation 3.1

$$\begin{bmatrix} i_{dw\_ff} \\ i_{dq\_ff} \end{bmatrix} = \begin{bmatrix} i_{ds} \\ i_{qs} \end{bmatrix} + \begin{bmatrix} 0 & -\omega_e C_f \\ \omega_e C_f & 0 \end{bmatrix} \begin{bmatrix} v_{ds} \\ v_{qs} \end{bmatrix} \tag{3.1}$$

This feed-forward factor is added to the control circuit in order to decouple the D and Q axis reference inverter output current i^*_{dqw} as shown in the figure 3.1.

The output filter capacitor also plays a crucial role in filtering the higher order harmonics. The output capacitive filter along with the stator inductance forms a CL low pass filter as shown in the figure 3.3 with a cutoff frequency given by f_c and a resonant frequency given by f_{res} as shown in the equation 3.2. The cutoff frequency is the frequency at which filtration begins. For a low-pass filter, frequencies below the cutoff frequency are allowed through, while frequencies over the cutoff frequency are excluded. The cutoff frequency can be determined by the bode plot of the filter closed loop system shown in the figure 3.4. The closed loop response of the CL filter is shown in the figure 3.4 where the stator resistance is acting as a damping resistance to suppress the resonance peak.

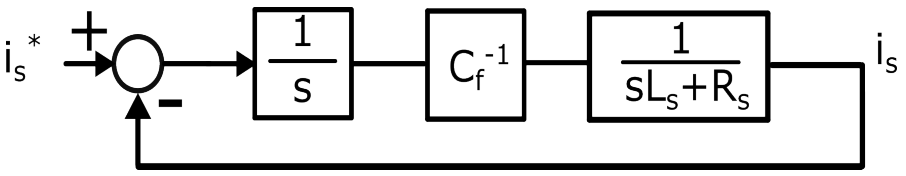


Figure 3.3: LC low pass filter at the inverter output

$$f_{res} = \frac{1}{2\pi\sqrt{L_s C_f}} \tag{3.2}$$

Since the PMSM's rated speed is set to 30,000 rpm, the fundamental frequency is calculated from equation 3.3.

$$f_1 = \frac{30000p}{60} = 2000Hz \tag{3.3}$$

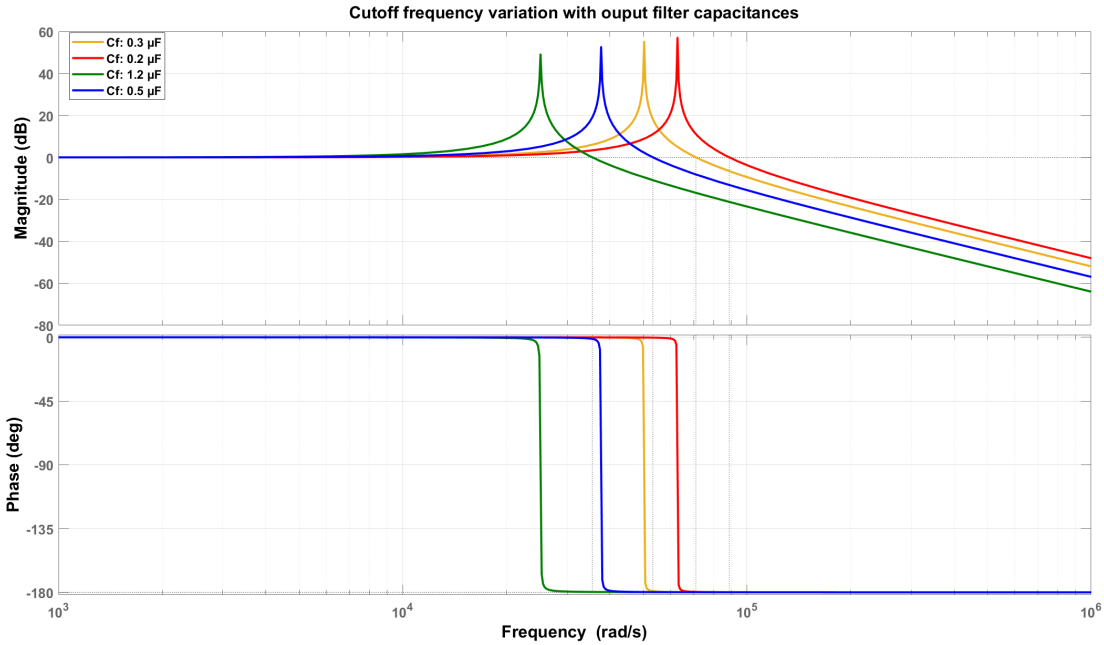


Figure 3.4: Frequency response of output filter

To further prevent the resonance at fundamental frequency the resonant frequency should be kept higher than *2 kHz* and a resistance could be added either parallel to the capacitor or in series with the stator resistors to improve damping and preventing the system to go into the state of oscillation.

The value of capacitor can be evaluated from the equation 3.2 by deciding the value of resonance frequency. There resonant frequency should be sufficiently larger than fundamental frequency in order to avoid resonance in the system and not too far way from the fundamental as the cutoff frequency will also increase leading to smaller value of capacitance but ineffective filtering operation of the capacitor. On the other hand increasing the value to output filter capacitance improves the current and voltage waveform but increases the system to go into resonance. Moreover increasing the capacitance not only degrades the stability but also increses the size of capacitor and

Considering the cutoff frequency of *6 kHz* the capacitance value is calculated to $0.5\mu F$. After deciding the value of capacitance the cutoff of frequency can be evaluated from figure 3.4 which in this case is 8.48 kHz. The unfiltered and filtered output current is shown in the figure 3.5.

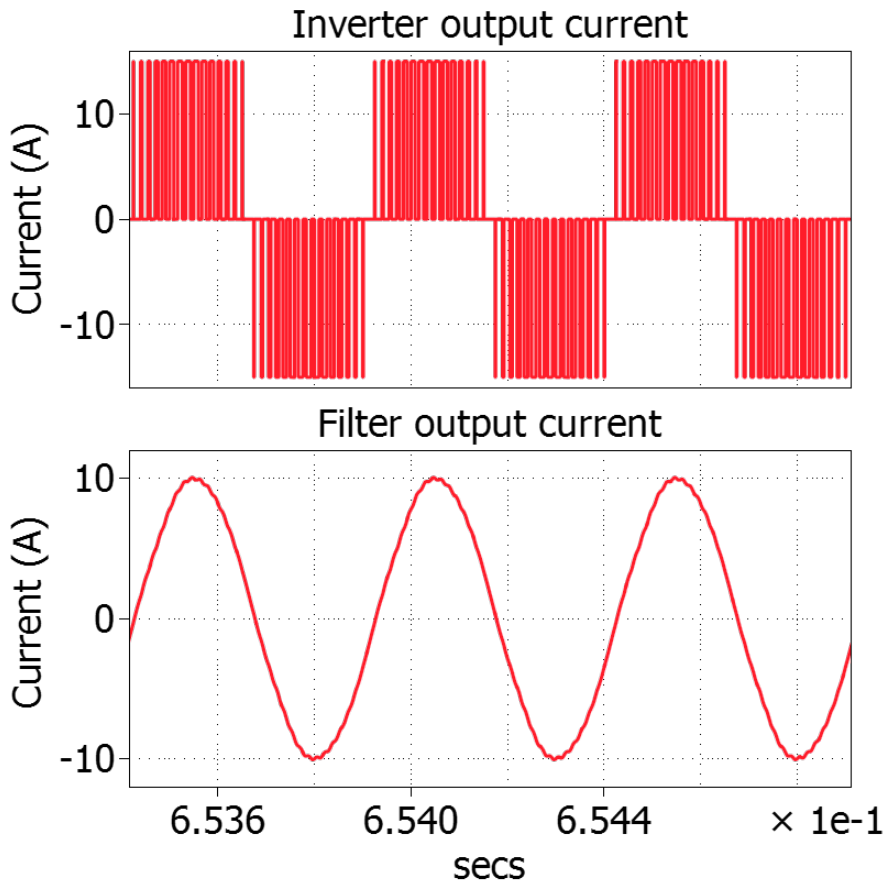


Figure 3.5: Inverter output and filter output current

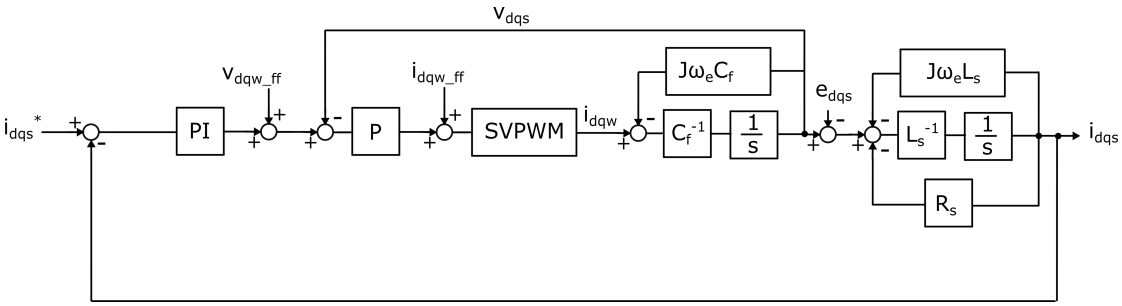


Figure 3.6: Multi-loop current controller

Controller design

The inner loop voltage proportional controller as shown in the figure 3.1 can be mathematically represented in state space form as shown in the equation 3.4. The reference current vectors i^*_{dqw} can be deduced by the difference of stator reference and feedback voltages using a proportional controller. It has been assumed that the average value of the synthesized current produced by pulse width modulation is identical to the value of the current reference. From the figure 3.2, the equation 3.5 can be deduced. The

feed-forward current is given by the equation 3.1.

$$\begin{bmatrix} i_{dw}^* \\ i_{qw}^* \end{bmatrix} = \begin{bmatrix} K_{pv} & 0 \\ 0 & K_{pv} \end{bmatrix} \begin{bmatrix} v_{ds}^* - v_{ds} \\ v_{qs}^* - v_{qs} \end{bmatrix} + \begin{bmatrix} i_{dw\_ff} \\ i_{qw\_ff} \end{bmatrix} \tag{3.4}$$

$$\begin{bmatrix} i_{dw}^* \\ i_{qw}^* \end{bmatrix} = \begin{bmatrix} i_{ds} \\ i_{qs} \end{bmatrix} + \begin{bmatrix} sC_f & -\omega_e C_f \\ \omega_e C_f & sC_f \end{bmatrix} \begin{bmatrix} v_{ds} \\ v_{qs} \end{bmatrix} \tag{3.5}$$

Using equation 3.1 in equation 3.4 the proportional gain K_{pv} can be set to $\omega_{c1} C_f$ where the ω_{c1} is the cut-off frequency for the low pass CL filter at the inverter output.

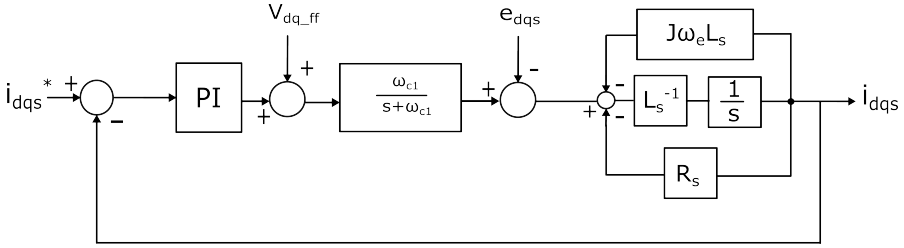


Figure 3.7: Block diagram of the outer current loop

The equation 3.6 shows the transfer function of the voltage inner control loop as shown in the figure 3.7

$$\begin{aligned} \begin{bmatrix} v_{ds} \\ v_{qs} \end{bmatrix} &= \begin{bmatrix} \frac{K_{pv}}{sC_s + K_{pv}} & 0 \\ 0 & \frac{K_{pv}}{sC_s + K_{pv}} \end{bmatrix} \begin{bmatrix} v_{ds}^* \\ v_{qs}^* \end{bmatrix} \\ &= \begin{bmatrix} \frac{\omega_{c1}}{s+\omega_{c1}} & 0 \\ 0 & \frac{\omega_{c1}}{s+\omega_{c1}} \end{bmatrix} \begin{bmatrix} v_{ds}^* \\ v_{qs}^* \end{bmatrix} \end{aligned} \tag{3.6}$$

To create the outer control loop, the inner control loop's closed-loop transfer function must be considered. The inner loop's transfer function can be determined as a first-order low-pass filter. Consequently, the first-order low-pass filter must be considered to decouple the coupling term utilizing the feed forwarding term. If the filtered feed forwarding term decouples the coupling term, the transfer function of the outer control loop, which is the phase current control loop, can be set as a second-order low pass filter.

The outer loop PI controller for current to voltage conversion can be tuned accordingly using equation 3.7 where v_{ds_ff} and v_{qs_ff} are the feed forward voltage for decoupling and compensation of the D and Q axis voltage given in the equation 3.8. The voltage feed-forward can further be evaluated by using the stator voltage equations from the figure 3.2. The mechanical time constant is typically considerably bigger than the electric time constant [25]. During a sampling time, it is safe to assume that the electric speed is constant. As demonstrated in the equation 3.9, with the aforementioned assumptions, the back-emf can be considered a constant value.

$$\frac{\omega_{c1}}{s+\omega_{c1}}[(\begin{bmatrix} K_{pd}+\frac{K_{id}}{s} & 0 \\ 0 & K_{pq}+\frac{K_{iq}}{s} \end{bmatrix})\begin{bmatrix} i^*_{ds}-i_{ds} \\ i^*_{qs}-i_{qs} \end{bmatrix}+\begin{bmatrix} v_{ds\_ff} \\ v_{qs\_ff} \end{bmatrix}] = \begin{bmatrix} sL_s+R_s & -\omega_e L_s \\ \omega_e L_s & sL_s+R_s \end{bmatrix}\begin{bmatrix} i_{ds} \\ i_{qs} \end{bmatrix}+\begin{bmatrix} e_{ds} \\ e_{qs} \end{bmatrix} \tag{3.7}$$

$$\begin{bmatrix} v_{ds\_ff} \\ v_{qs\_ff} \end{bmatrix} = \frac{s+\omega_{c1}}{\omega_{c1}}(\begin{bmatrix} 0 & -\omega_e L_s \\ \omega_e L_s & 0 \end{bmatrix}\begin{bmatrix} i_{ds} \\ i_{qs} \end{bmatrix}+\begin{bmatrix} e_{ds} \\ e_{qs} \end{bmatrix}) \tag{3.8}$$

$$\frac{s+\omega_{c1}}{\omega_{c1}}\begin{bmatrix} e_{ds} \\ e_{qs} \end{bmatrix} = \begin{bmatrix} e_{ds} \\ e_{qs} \end{bmatrix} \tag{3.9}$$

The proportional gain (K_{pd},K_{pq}) could be set to $\omega_{c2}L_s$ while both I gains (K_{id}, K_{iq}) could be set to $R_s\omega_{c2}$ to have a second order transfer function of the outer closed loop as shown in the equation 3.10.

$$\begin{bmatrix} i_{ds} \\ i_{qs} \end{bmatrix} = \begin{bmatrix} \frac{\omega_{c1}\omega_{c2}}{s^2+\omega_{c1}s+\omega_{c1}\omega_{c2}} & 0 \\ 0 & \frac{\omega_{c1}\omega_{c2}}{s^2+\omega_{c1}s+\omega_{c1}\omega_{c2}} \end{bmatrix}\begin{bmatrix} i^*_{ds} \\ i^*_{qs} \end{bmatrix} \tag{3.10}$$

The inner voltage loop with proportional gain controller introduces a frequency bandwidth ω_{c1} which is also the corner and resonance frequency of the output CL filter. The fundamental frequency of the motor input f_1 should be less then the the corner frequency. The bandwidth of the outer current loop should be chosen carefully.

For stable operation the second stage bandwidth ω_{c2} should be chosen such that the bandwidth of the outer current loop (BW_{CC}) should be smaller than the inner loop bandwidth as well as larger than the fundamental current bandwidth ω_{f1} i.e. $\omega_{f1} < BW_{CC} < \omega_{c1}$. Therefore a careful choice should be made while selecting the bandwidth of the multi-loop.

Since the mechanical dynamics remains unchanged in the CSI-IMMD the PI speed controller tuning procedure same as discussed in the section 2.1.2.

The table 3.1 shows the value of the proportional and the integral gains of different controller.

Parameters	**Values**
Voltage controller	
$K_{pv}(\omega_{res}C_f)$	0.02
Current controller	
$K_{pi}(\omega_{c2}L_s)$	39.3
$K_{ii}(\omega_{c2}R_s)$	3.4E+03
Speed controller	
$K_{ps}(\omega_B J)$	0.01
$K_{is}(\omega_B^2/4)$	25

Table 3.1: Proportional and Integral gains for controllers in CSI-IMMD

Controller Stability analysis

The multi-loop control needs to be studied for the stability as there are multiple bandwidths involved in the control system along with the resonant frequency of the CL filter. To inculcate the delay in measurement from the sampling a delay of $e^{-2sT_{sw}}$ is introduced in the feedback of the current control assuming the sampling delay of $2T_{sw}$ as shown in the figure 3.8. The stability of the system can be examined through the open loop transfer function of the inner voltage loop and outer current loop. The open-loop and closed-loop transfer function of the inner voltage loop and outer current loop is shown in the equations 3.11 and 3.12.

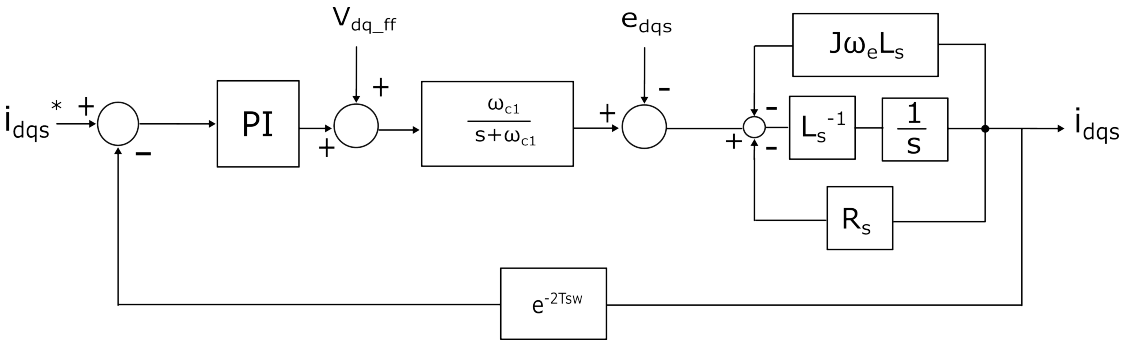


Figure 3.8: Control block diagram for CSI-IMMD with delayed feedback

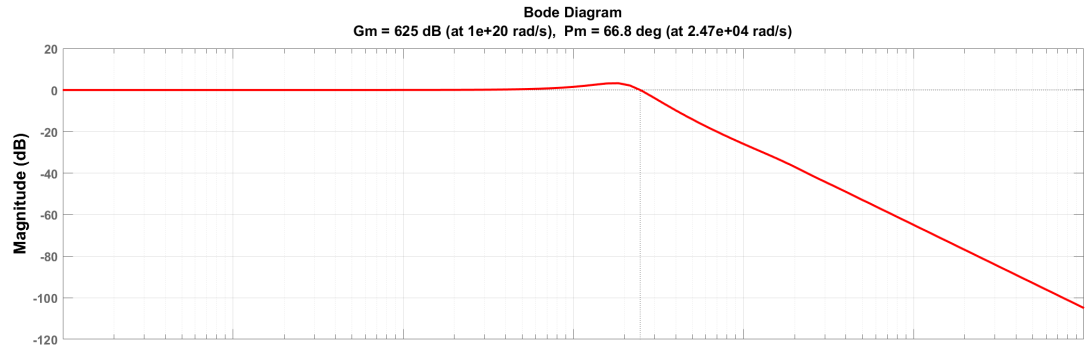
$$
\begin{aligned}
G(s)_{v,ol} &= K_{pv} * \frac{1}{sC_f} \\
G(s)_{v,cl} &= \frac{K_{pv}}{sC_f + K_{pv}}
\end{aligned}
\tag{3.11}
$$

$$
\begin{aligned}
G(s)_{i,ol} &= (K_{pv} + \frac{K_{pi}}{s}) * G(s)_{v,cl} \\
G(s)_{i,cl} &= \frac{G(s)_{i,ol}}{1 + G(s)_{i,ol} H(s)} \\
H(s) &= e^{-2sT_{sw}}
\end{aligned}
\tag{3.12}
$$

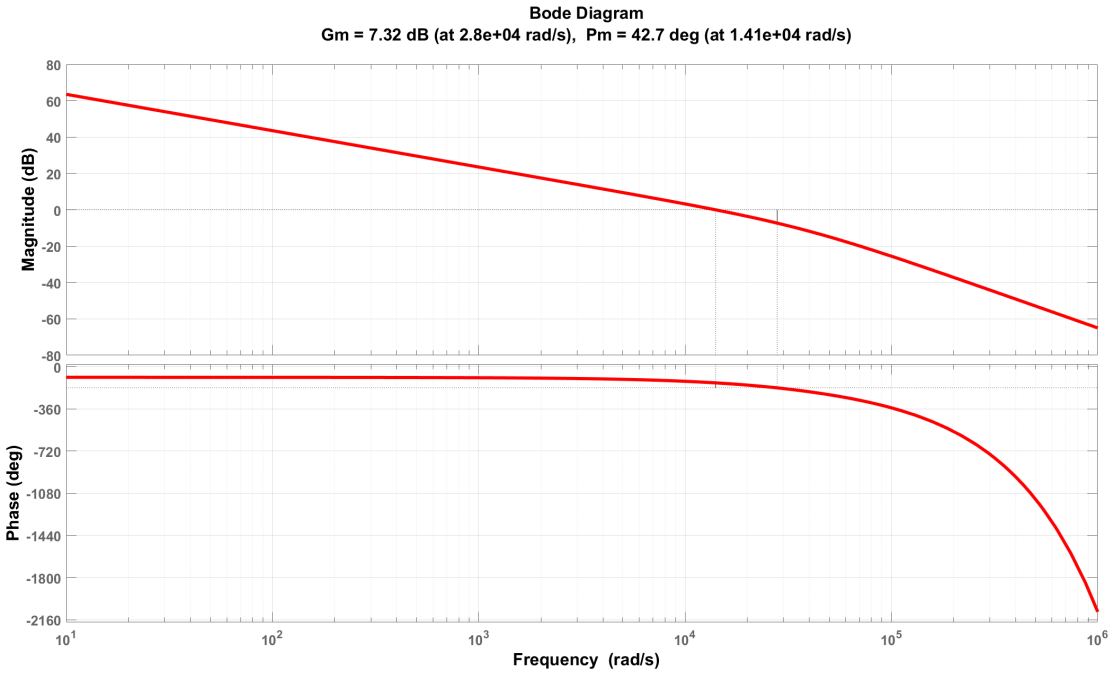
The stability of the controller can be analysed by using bode plot of the open loop transfer function of the current controller and the bandwidth is analysed by the closed loop transfer function.

Since the inner voltage Open loop transfer function has only pole at 0, makes the voltage loop control stable. The closed loop transfer function as shown in the equation 3.11 is a first order system with a bandwidth of $\frac{K_{pv}}{C_f} = 3.77 * 10^4$ rad/sec.

The same procedure can be followed with the current controller with open and closed loop frequency bode plot shown in figure 3.9. The proportional and integral gains values used are given in table 3.1.



(a)



(b)

Figure 3.9: (a) Closed loop bode plot of current controller for bandwidth **(b)** open loop Bode plot for stability of current controller

3.1.3 Modulation

The Space Vector Modulation is used in the CSI-IMMD. The SVPWM in CSI is different from that in VSI. Some of the basic difference includes

- the space vectors in CSI lead the space vectors in VSI by 30°.
- In the CSI each space vector in consists of only two switches instead of three switches in VSI.
- CSI-SVPWM consists of three zero vectors compared to two zero vectors in VSI-SVPWM.

Figure 3.10 shows the space vector diagram of a Current Source Inverter. The sector is determined calculating the angle between I_β and I_α given by the equation 3.13. Then the time of conduction for each active and zero vector is calculated in each switching cycle using the equation 3.14.

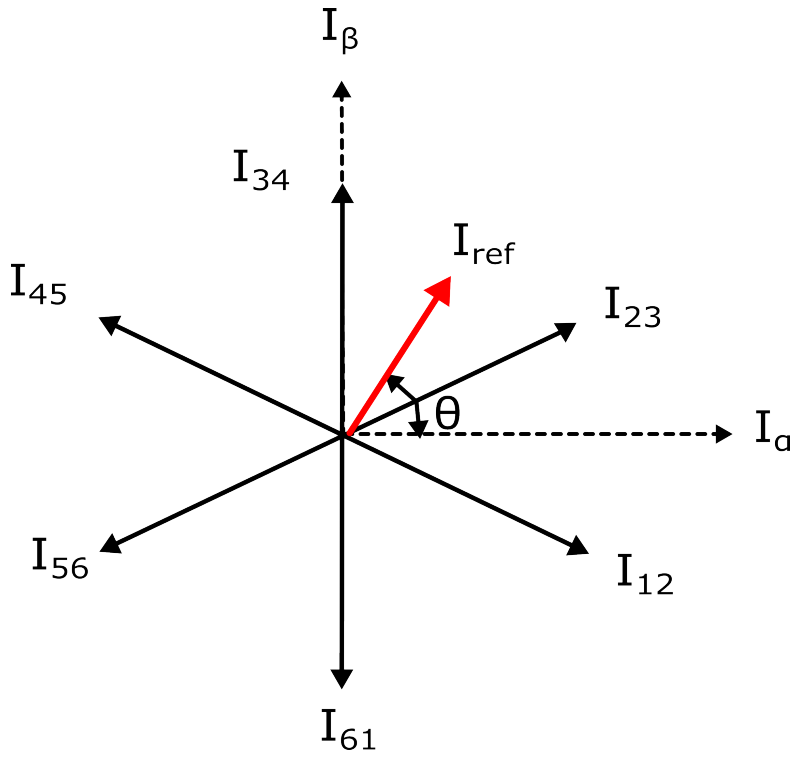


Figure 3.10: Space vector diagram of Current Source Inverter

$$\theta = tan^{-1}(\frac{I_\beta}{I_\alpha}) \tag{3.13}$$

$$\begin{aligned} T_1 &= m_a sin(\frac{\pi}{6} - \theta) \\ T_2 &= m_a sin(\frac{\pi}{6} + \theta) \\ T_0 &= T_S - T_1 - T_2 \\ m_a &= I_{ref}/I_{dc} \end{aligned} \tag{3.14}$$

To implement the space vector modulation in hardware the two reference per switch are produced based on T_1, T_2 and T_0. The first reference is used to make the switch on and the other reference is used to make the switch off as can be seen for phase A upper switch in the figure 3.11.

The gate pulse in the figure 3.11 is produced by comparing it with a saw-tooth waveform where the switch is on when the carrier saw-tooth waveform is larger in magnitude

than the on reference and the switch if off when the carrier waveform is larger than off reference.

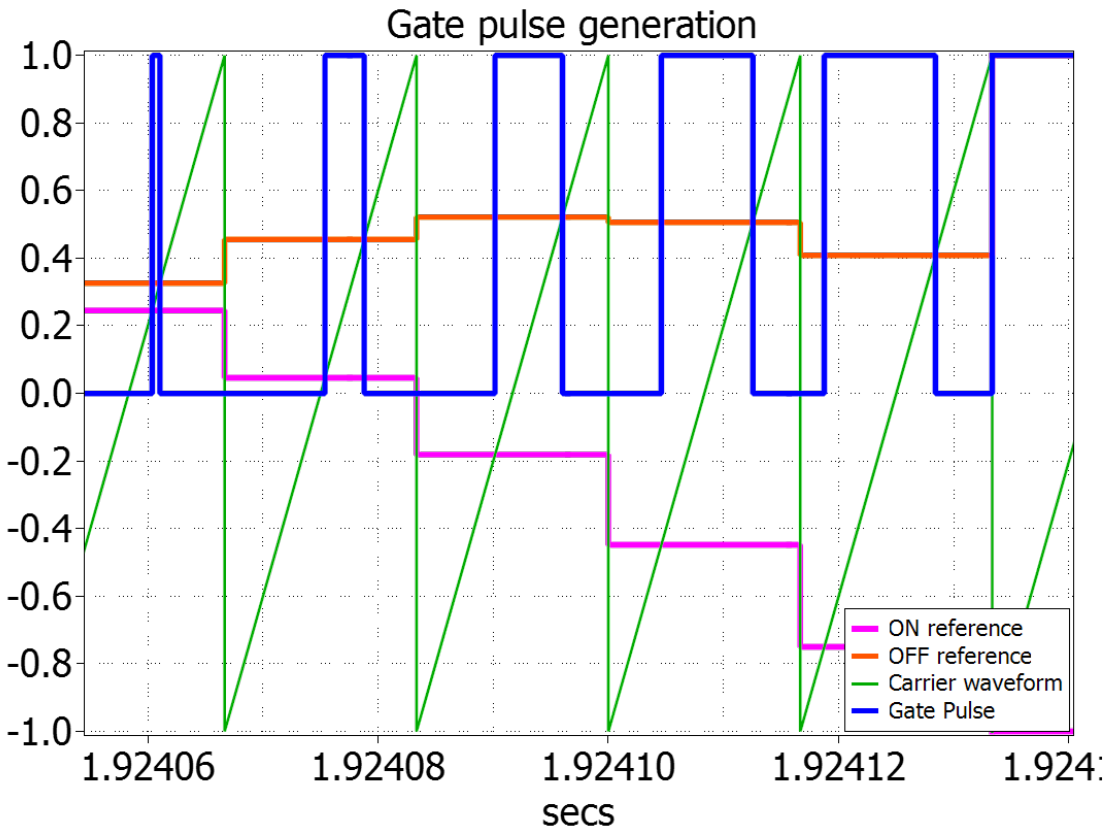


Figure 3.11: Phase A upper switch gate pulse generation with on and off references

The CSI-IMMD system response for output line current and line voltage is shown in the figure 3.12. The plot shows the sinusoidal voltage and sinusoidal current when the machine speed is set at 30,000 rpm with the elimination of both steep $\frac{dv}{dt}$ and $\frac{di}{dt}$. The figure 3.13 shows the harmonic spectrum of the stator voltage and stator current which justifies the filtering process of the output capacitor.

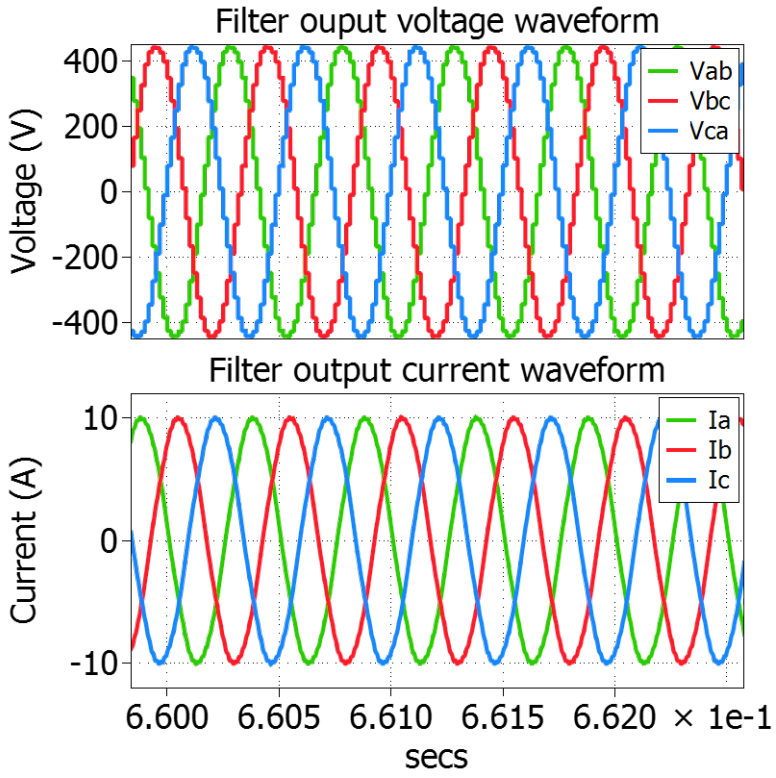


Figure 3.12: Filter output voltage and current of CSI-IMMD system

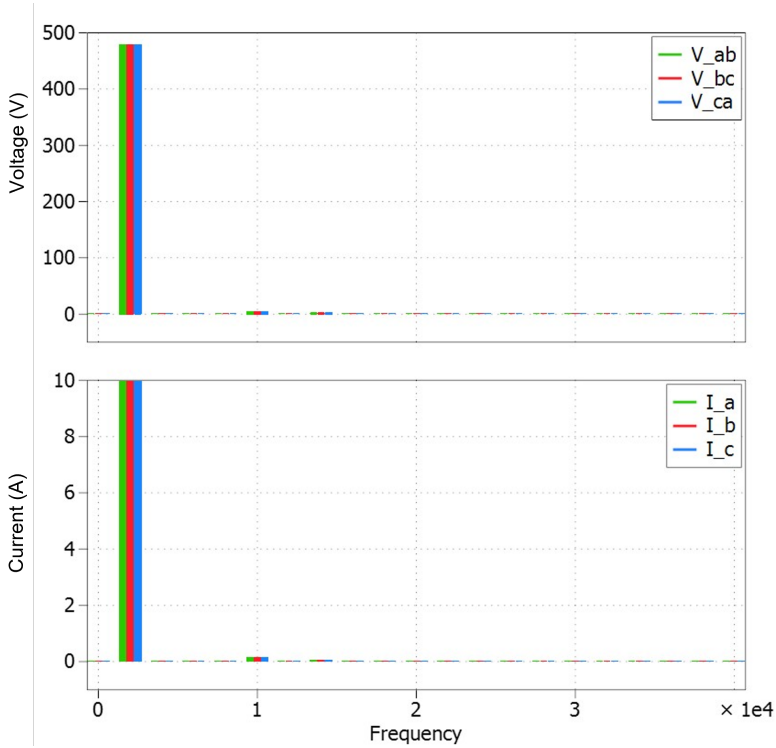


Figure 3.13: Frequency distribution of the output voltage and current in CSI

3.2 Motor drive loss modelling

3.2.1 MOSFET loss modelling

The MOSFET loss modelling is achieved as explained in section 2.2.1.

3.2.2 Diode loss modelling

- The conduction loss in diode is given by equation 3.15 where V_F is the diode forward voltage, i_{on} is the forward current which in case of CSI is the input DC current I_{dc} and T_j is the junction temperature.

$$P_{cond} = V_F(i_{on}(t), T_j) * i_{on}(t) = V_F * I_{dc} \tag{3.15}$$

From the above equation it is evident that the forward voltage V_F is dependent on both junction temperature of diode and conducting current. A SiC series diode is used in the project to provide the MOSFET reverse voltage blocking capability and to block the reverse conduction of the current from MOSFET's internal diode. The SiC diode used in the project is GenSiC GD30MPS12J. The parameters of the SiC diode is provided in table 3.2, where V_{block} is the rated blocking voltage, $I_{F,max}$ is the rated forward current. In CSI since the input current is constant, the conduction loss will also be constant at steady state operation.

V_{block}	1200V
$I_{F,max}$	30A
V_F	f(T_j, I_f)

Table 3.2: Parameters of SiC diode GD30MPS12J

- Switching loss: The switching loss in the diode is only contributed by the turning off operation and capacitive charge stored in depletion layer. The reverse recovery loss during turn of can be calculated using equation 3.16 where I_{rr} is the reverse recovery current peak, t_b is the time taken to reduce the reverse recovery charges to minimum, V_r is the reverse voltage applied across the diode and f_{sw} is the switching frequency of the MOSFET connected in series.

$$P_{sw,off} = \frac{1}{6} I_{rr} V_r t_b f_{sw} \tag{3.16}$$

A parasitic capacitance is evident in the depletion region's boundaries from the semiconductor structure. The charge held in the diode's capacitance is released during the turn on procedure. The loss can be calculated based on the equation 3.17 where C_R is the diode total capacitance.

$$P_{sw,C} = \frac{1}{2} C_R V_R^2 f_{sw} \tag{3.17}$$

Since there is no stored charge in the diode initially, turning on is much simpler. Minority chargers are often injected into the lattice fairly quickly and hence there are no losses during turn on. So the total loss only comprises of turn off loss which includes reverse recovery charge and capacitive charge losses as shown in the equation 3.18.

$$P_{sw} = \frac{1}{6} I_{rr} V_r t_b f_{sw} + \frac{1}{2} C_R V_R^2 f_{sw} \tag{3.18}$$

The switching losses and the conduction loss modelling in PLECS is shown in the figure 3.14.

3.2.3 Detailed inverter loss

The loss incurred in the CSI-IMMD consists of motor loss, power switches loss, and filter loss. The other losses caused by parasitic components, PCB traces and input inductor are not taken into account since it has been assumed that the input current is an ideal current source. The losses in the power switches can be derived as discussed in section 2.3.2 where the conduction loss will remain constant as the switch is conducting even if there is no output current. The figure 3.15 shows the CSI structure where a SiC diode is used to provide a reverse voltage blocking capability to the GenSiC G3R75MT12J MOSFET used in VSI.

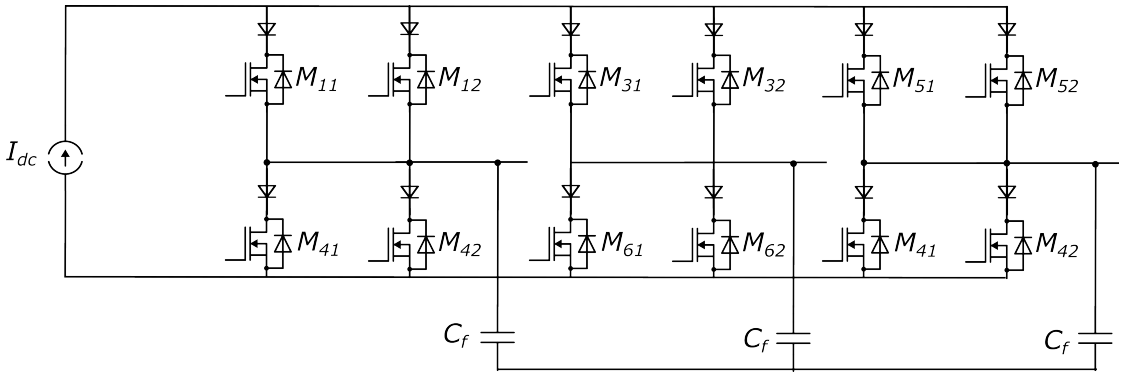
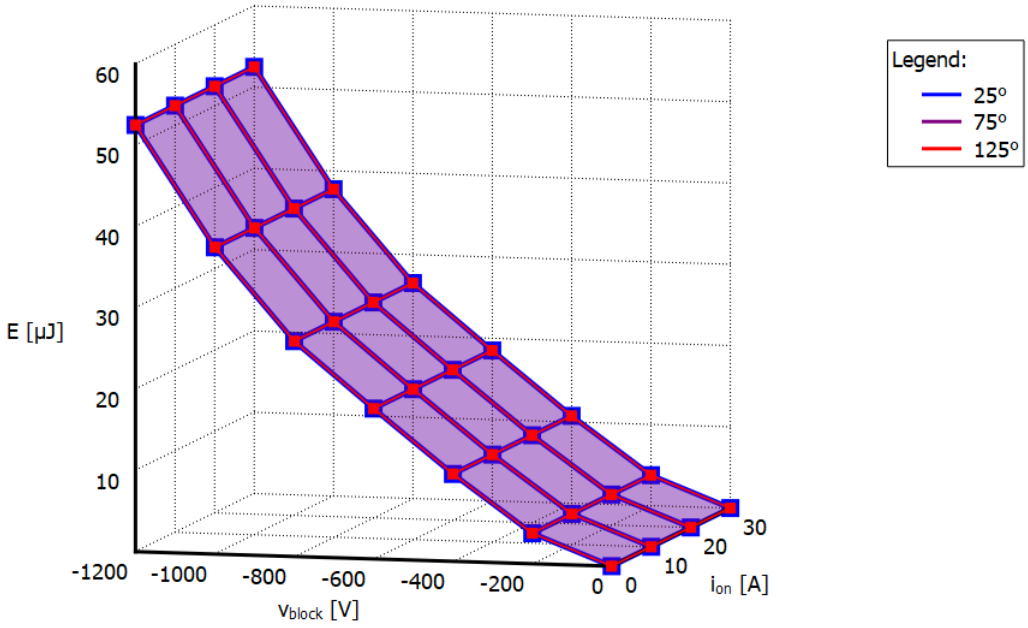


Figure 3.15: Current Source Inverter for IMMD

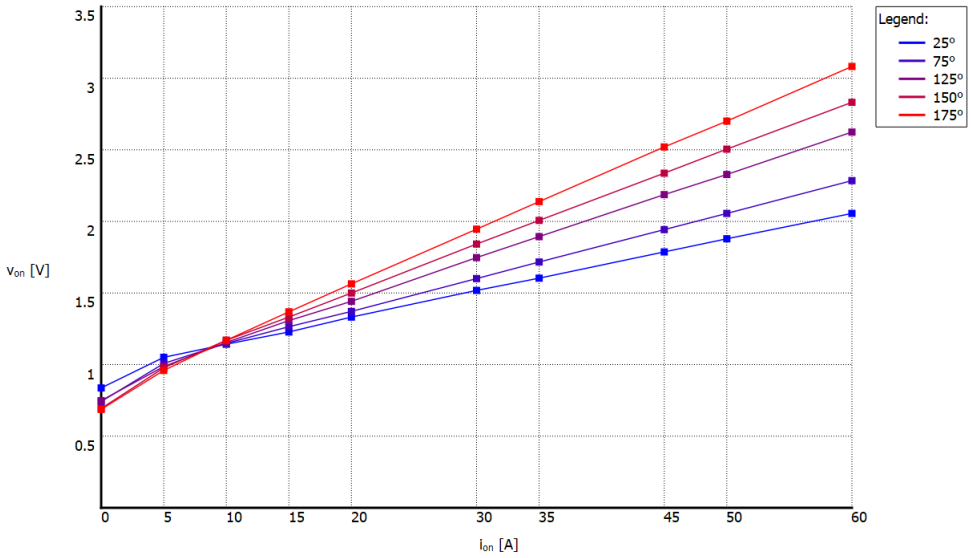
3.3 IMMD system 1-D thermal modelling

3.3.1 Thermal circuit parameters

The thermal parameters of the diode GenSic GD30MPS12J are deduced from the thermal impedance graph in the data-sheet. The thermal impedance graph provides the



(a)



(b)

Figure 3.14: (a) The switching loss at different current and temperatures, and (b) Conduction loss of diode at different temperatures

thermal impedance for different duty cycles. Since the SVPWM in CSI-IMMD has an average duty cycle close to 0.5, hence the graph with 0.5 duty cycle is chosen for ther-

mal behaviour analysis. The thermal network from the junction to the case is divided into three parts by selecting three points on the graph to improve the accuracy as shown in the table 3.3

Thermal parameters	Values (R: W/K, C: J/K)
R_1	0.2231
C_1	9.407E-06
R_2	6.00E-02
C_2	8.31E-03
R_3	0.141
C_3	0.1101

Table 3.3: Junction-Case thermal parameters of the GD30MPS12J

Since in CSI the losses are contributed from both MOSFET and series diode, their respective lookup tables are produced for both conduction and switching losses. The thermal network for the CSI is shown in the figure 3.16.

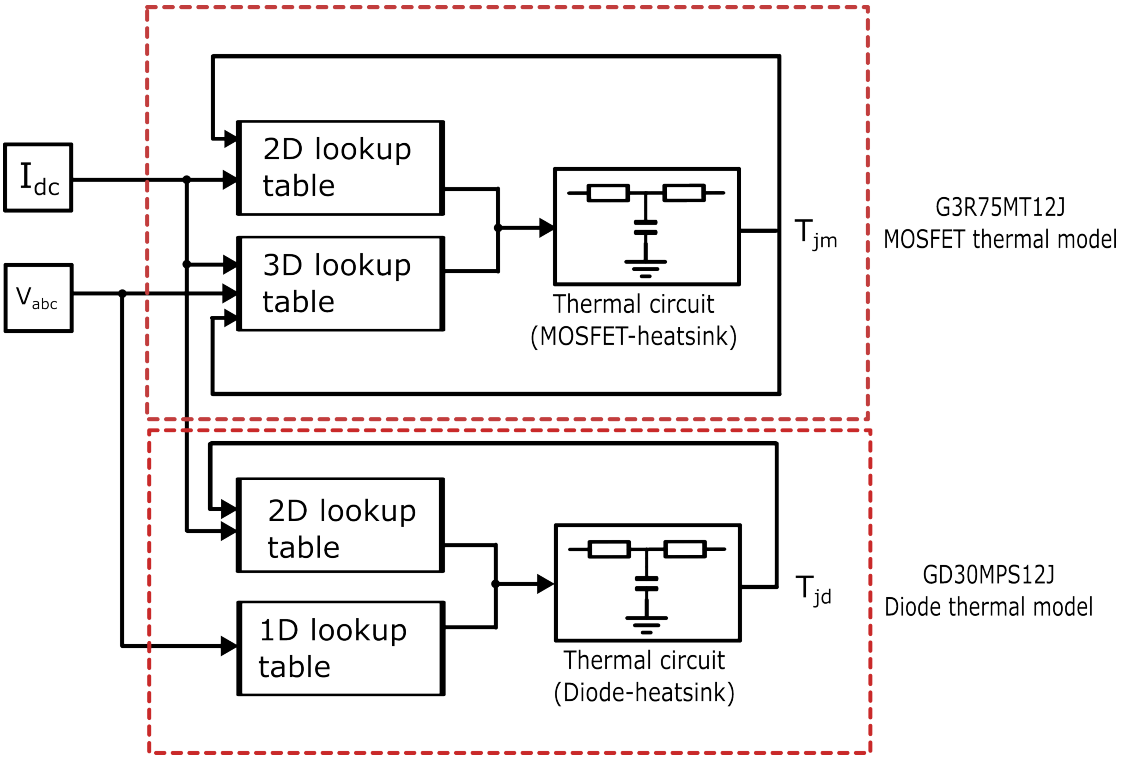
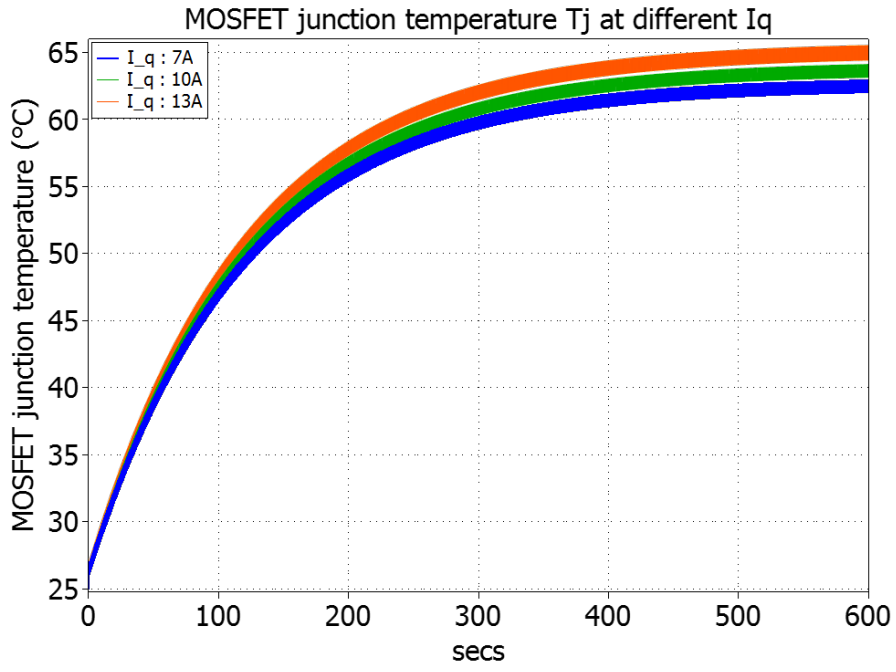
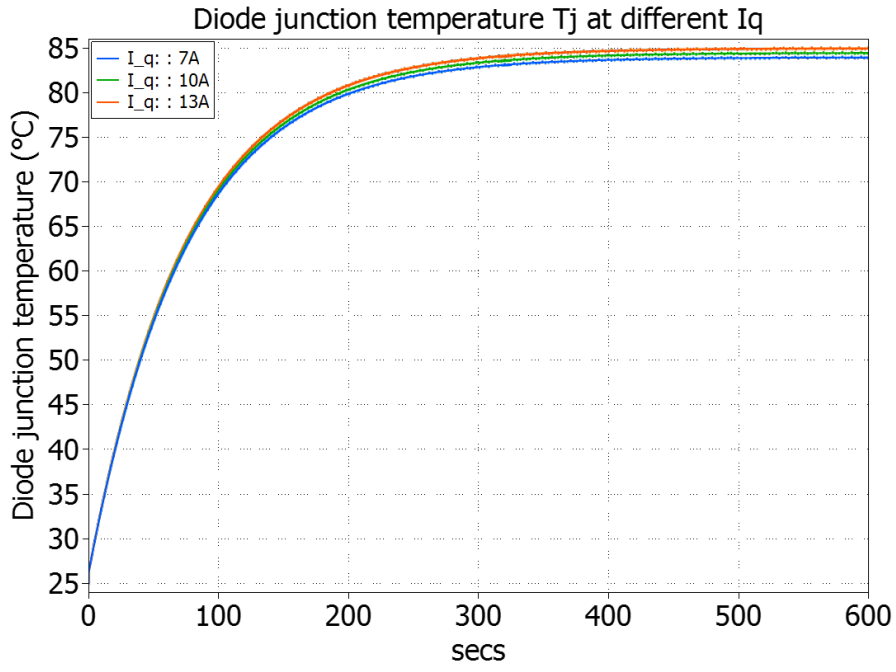


Figure 3.16: Thermal model for CSI

The figure 3.17 shows the junction temperature variation of the MOSFET and diode at different current settings. The DC link current I_{dc} is set to 15A and switching frequency f_{sw} to 60 kHz. Since the conduction losses in MOSFETs and diodes are constant throughout the operation, and switching losses are very low, hence a very less variations in steady state temperatures are observed with changing current requirements.



(a)



(b)

Figure 3.17: Junction temperature variation at different reference current settings **(a)** MOSFET G3R75MT12J and **(b)** diode GD30MPS12J

3.4 Summary

In this chapter, modelling of both loss and thermal of the CSI-IMMD were discussed and following conclusions can be made:

- The accurate loss modelling of the inverter is difficult as several losses contributed by parasitic capacitance and inductance, PCB traces and gate drivers are ignored.
- The multi-loop control strategy for the CSI-IMMD has been established with feed forward decoupling method.
- The stability analysis of the controller has been established with respect to output capacitor and bandwidth of the current controller.
- Overall, the CSI-IMMD model has an excellent dynamic responsiveness as shown in appendix B.4.
- The loss model in prepared by using same power switch used in VSI-IMMD and adding an SiC diode in series with the switch.
- The thermal network using lookup table for conduction and switching loss is modelled.

CHAPTER

4

BENCH-MARKING ANALYSIS

After modelling the VSI and CSI IMMD setup respectively, a bench-marking study has been carried out to determine the best topology for high speed motoring operation at different parameters. In this chapter the following points will be discussed:

- Analysis and comparison of switching losses in CSI and VSI at different switching frequencies.
- Analysis and comparison of conduction losses in CSI and VSI.
- Comparison of thermal performance of CSI compared with VSI-IMMD drive.
- Comparison based on the stability of the system.

4.1 Bench-marking model

To make a model for bench-marking analysis, a current controlled VSI is connected to the generator side and speed controlled CSI is connected to the motor side of the HiSPEM IMMD as shown in the figure 4.1. The CSI-IMMD is fed through a constant DC current of 15 A while the VSI-IMMD has a constant DC input voltage supply of 850 V.

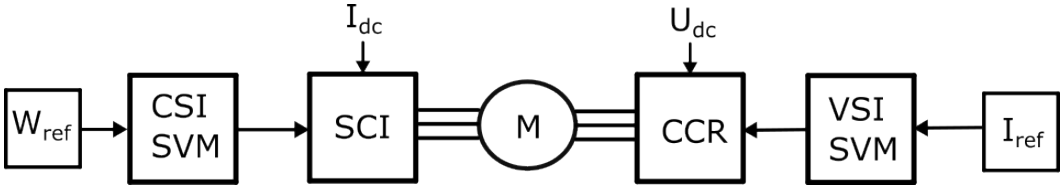


Figure 4.1: Bench-marking model of VSI coupled CSI IMMD

The maximum reference current on VSI-IMMD is limited to $\frac{\sqrt{3}}{2}$ times I_{dc}, where I_{dc} is the dc input current at the CSI-IMMD, to avoid over-modulation in the CSI-SVPWM as T_0 will become negative. The rated speed of the machine is maintained at 30,000 revolutions per minute while the value of the current and switching frequency can be altered.

4.2 Switching loss analysis of VSI and CSI

The switching loss is dependent on the energy loss per switching cycle. The switching loss in CSI consists of both SiC MOSFET and SiC diode while only SiC MOSFET in VSI. Furthermore, modulation strategies play a crucial influence in determining switching loss.

The Q axis reference current $I_{q,ref}$ is fixed at 12A and the switching loss is evaluated at different frequencies with CSI DC link current ($I_{dc} = 15A$).

f_{sw} (kHz)	CSI s/w loss (W)	VSI s/w loss (W)
30	6.8	9
60	10.5	18
90	14	26.5

Table 4.1: Switching loss comparison at different f_{sw}

The figure 4.2 shows the trend of changing switching frequencies with respect to switching loss for both CSI and VSI topology. The switching loss in VSI is increased with the same factor as the change in f_{sw} while the change in CSI is lower than VSI and overall switching losses are also low which can be accounted for the operating pattern of switches in CSI-SVPWM.

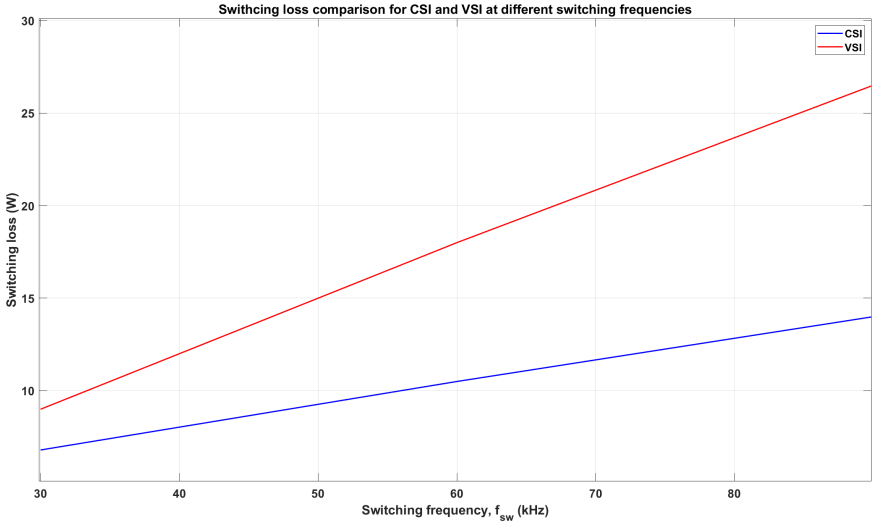


Figure 4.2: Switching loss of CSI and VSI at different f_{sw}

4.3 Conduction loss analysis

The conduction loss in motor drive is dependent on the switch and diode current, forward voltage during conduction, and temperature of the diode and MOSFET. Since both the VSI and CSI-IMMD setup uses two parallel switches instead of one,it decreases the overall conduction losses compared to one MOSFET and diode. Even though just one upper and one lower switch conduct simultaneously in CSI, as opposed to three switches in VSI, the CSI drive leads to conduction loss during zero vectors. In contrast to the VSI, in which conduction loss occurs solely via active vectors, the CSI has a constant conduction loss during its operation. The table4.2 shows the conduction loss at different current settings in VSI and CSI-IMMD.

I_q (A)	CSI cond loss (W)	VSI cond loss (W)
9	45.8	2.76
11	45.8	4.26
13	45.8	6.24

Table 4.2: Conduction loss comparison between VSI and CSI at f_{sw} = 60kHz

In addition to MOSFET conduction loss in CSI, the series SiC diode also plays an important part in conduction loss contribution. The forward voltage V_f for the series diode ranges from 0.8-3V depending on the forward current I_f and junction temperature of the diode T_j. In fact in the above CSI conduction loss, diode conduction loss amounts to almost 70% of the total conduction loss in CSI.

The CSI conduction losses are independent of modulation and is only dependent on the DC link current because the zero vectors also contribute to the conduction loss. For this the reason, the conduction loss for CSI remains constant irrespective of output current.

The conduction loss in CSI can be reduced by following methods:

- Dynamic control of DC link current I_{dc} according to modulation as discussed in [27].
- Using bi-directional four quadrant switches instead of MOSFET and series diode as discused in [28].
- Using soft switching techniques along with bi-directional SiC/GaN switches as discussed in [29].

4.4 Drive loss analysis

In CSI drive, the losses are contributed by the series SiC diodes, SiC MOSFETs, DC link inductor and output filter capacitor. Since the DC link inductor is not inducted in the modelling hence the losses are not accounted. The equivalent series resistance of the output capacitor is very low and hence the losses can be neglected. Hence the drive loss evaluation is done on the basis of losses in the diodes and MOSFETs in both VSI and CSI.

The table 4.3 shows the total drive loss for CSI and VSI typologies at different frequencies. The DC link current I_{dc} is set to 15 A , reference current $I_{q,ref}$ from current controlled VSI is set to 13 A and DC link voltage U_{dc} is set to 850 V.

Topology	f_{sw} **(kHz)**	**Conduction Loss (W)**	**Switching Loss (W)**	**Total Loss (W)**	**Efficiency (%)**
CSI	100	45.8	15.36	61.16	98.69
	120	45.8	18.52	64.32	98.62
	150	45.8	22.2	68	98.54
	200	45.8	30	75.8	98.38
VSI	100	6.24	48	54.24	98.83
	120	6.24	57.6	63.84	98.63
	150	6.24	72	78.24	98.33
	200	6.24	96	102.24	97.83

Table 4.3: Drive losses at different switching frequencies

The figure 4.3 shows the variation of drive loss with switching frequencies. The CSI drive losses are more than VSI drive losses when the switching frequency f_{sw} is below 121 kHz. The VSI drive loss becomes greater than CSI drive loss when the switching frequency is made greater than 120 kHz. Also the drop in efficiency of CSI is **0.3%** which is less than the drop in efficiency of VSI, where its efficiency drops is **1%** when switching frequency increased from 100 kHz to 200 kHz.

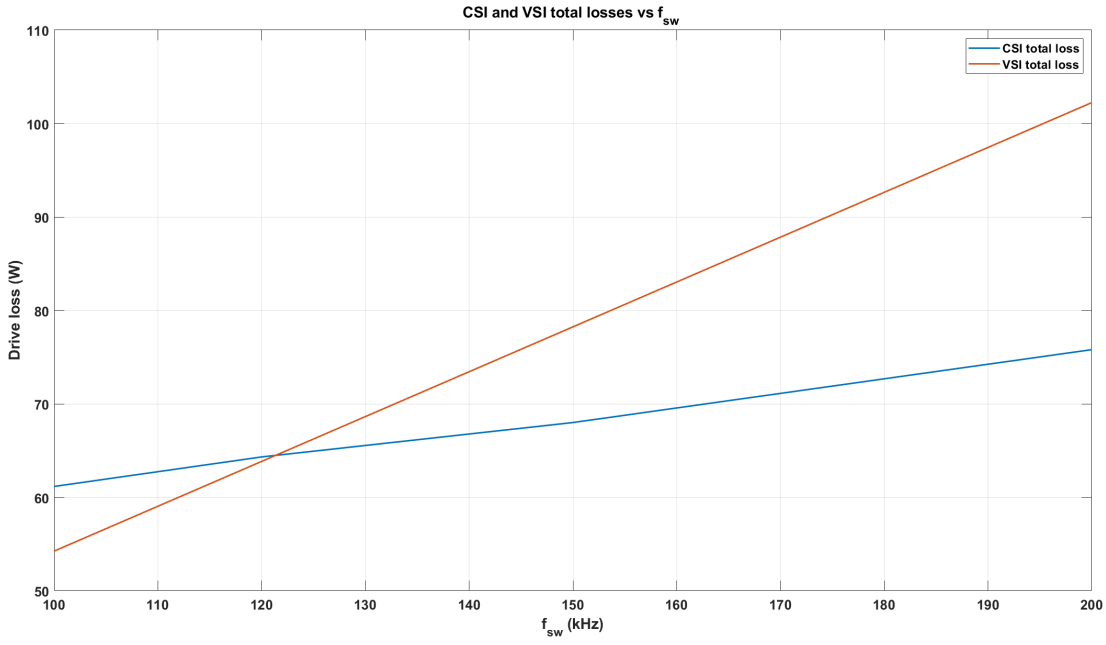


Figure 4.3: Drive loss variation with switching frequency f_{sw} for VSI and CSI

Hence, the comparison implicates that the losses are significantly reduced for CSI compared to VSI when the switching frequency higher than 121 kHz is used. Along with the losses, the size of DC link inductor and output filters are also reduced significantly

when higher switching frequencies are considered for the converters and the goal of a high power density converter can be achieved.

4.5 Thermal behaviour analysis

The parameters at which the thermal behaviour analysis is performed is given in the table 4.4 for both CSI and VSI. In CSI, additional heat-sinks are required for series diode cooling. The figure 4.4 shows the variation of temperature at 100 kHz for both VSI and CSI.

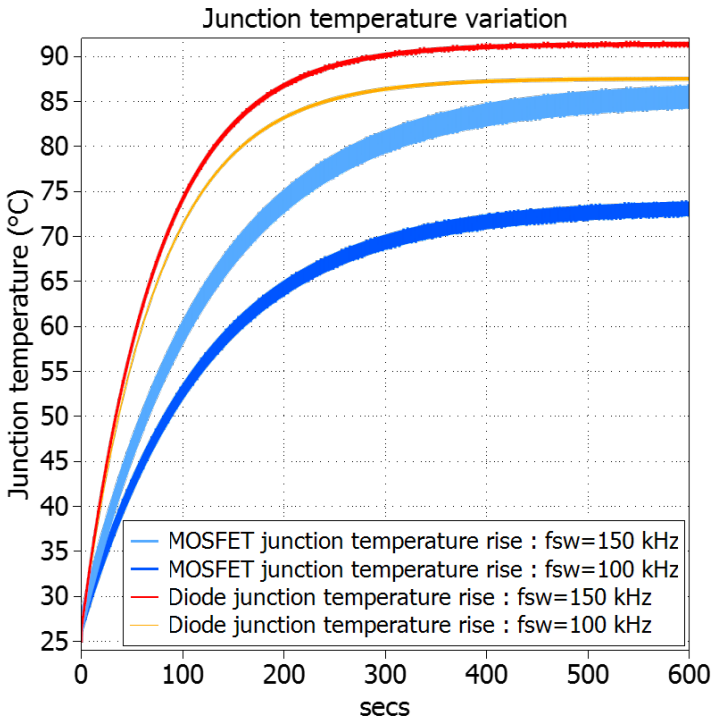
Parameters	**Values**
I_q	13A
I_{dc}	15A
U_{dc}	850V
f_{sw}	100, 150 kHz

Table 4.4: Operating parameters for CSI-VSI IMMD system

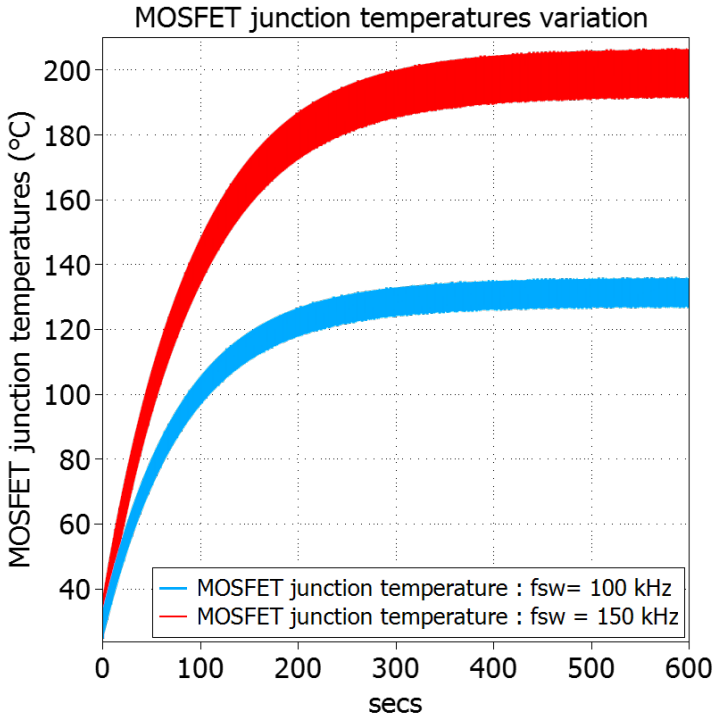
From the figure 4.4, the maximum junction temperature in CSI is at diode junction which is at 91°C at a switching frequency of 150 kHz while in VSI the junction temperature of MOSFET is 200°C. Hence, it can be concluded that the CSI topology is more thermally stable compared to VSI at higher switching frequencies which can be accounted to following reasons:

- A separate heat sink for the diode helps in distribution of thermal load on both heat sinks (MOSFET and diode).
- The major losses in CSI are due to series diode GD30MPS12J and junction to case thermal resistance of the diode is less compared to MOSFET G3R75MT12J which helps in better heat dissipation at diode's end.
- As the switching frequency is increased from 100 kHz to 150 kHz the overall losses in VSI surpasses CSI loss, hence the thermal load increases on the MOSFET junction in the VSI.

Moreover, figure 4.5 shows the variation of junction temperature at different conduction currents and switching frequencies for both MOSFETs in VSI and diode in CSI. The junction temperature variation for CSI is very less compared to VSI.



(a)



(b)

Figure 4.4: Junction temperature rise at f_{sw}=100 kHz and 150 kHz and I_q=13A for (a) MOSFET and diode in CSI, (b) MOSFET in VSI

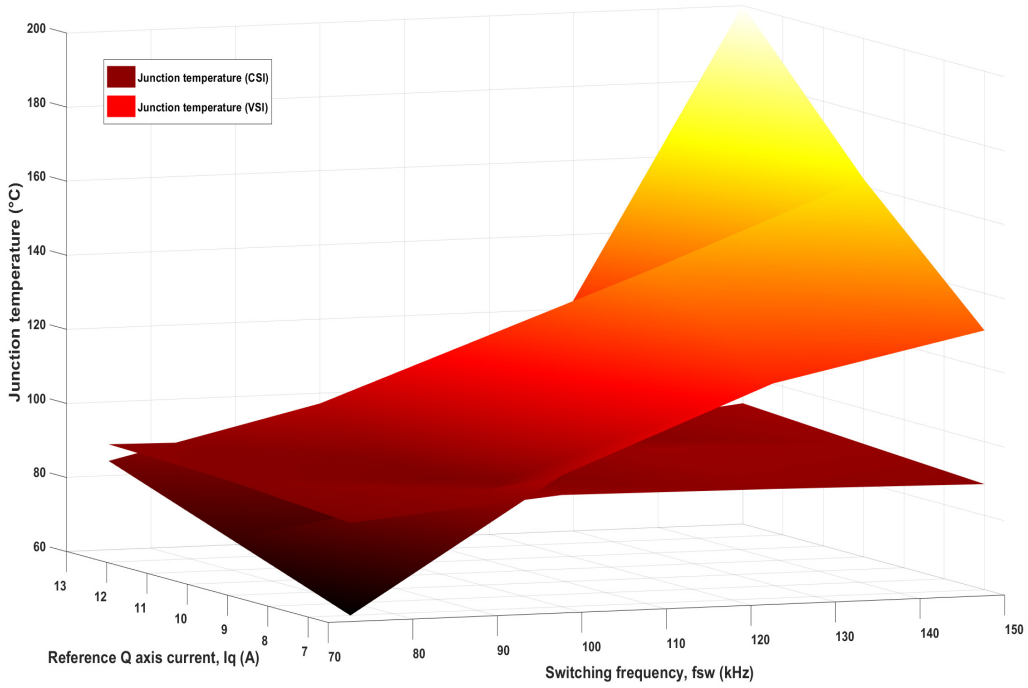


Figure 4.5: Junction temperature variation with conduction currents and switching frequencies

4.6 Summary

In this chapter, the bench-marking analysis has been conducted and following conclusions can be deduced:

- The switching loss analysis of VSI and CSI concludes the rise in switching loss with respect to switching frequency is greater than that in CSI and switching loss dominates in VSI drive loss.
- The conduction loss analysis concludes that CSI conduction loss is constant and doesn't change with modulation. The conduction loss in VSI is very less compared to that in CSI and it increases with conduction current.
- The total drive loss analysis concludes that VSI is more efficient than CSI at lower switching frequency operation while as the switching frequency increases above 121 kHz the losses of VSI becomes greater than that of CSI and hence CSI becomes more efficient when the operating switching frequencies are greater than 121 kHz.
- Thermal analysis concludes better thermal performance of CSI compared to VSI which is evident from figure 4.5 at different modulation index and switching frequencies. CSI's better thermal performance is due to introduction of extra heatsinks for series diodes and less switching losses in MOSFET + diode at higher switching frequencies compared to that of MOSFET in VSI.

CHAPTER

5

CONCLUSION & FUTURE WORKS

5.1 Conclusion

A systematic approach for the design and modelling of VSI and CSI-IMMD system along with a bench-marking study based on efficiency and thermal model has been presented. The bench-marking model consisting of current controlled VSI and speed controlled CSI is modelled and bench-marking study is conducted on different current levels and switching frequencies.

1. From the modelling of VSI-IMMD in the chapter 2, following can be concluded:
    - from the control strategy of VSI, it is evident that the tuning of current and speed controller can be performed efficiently using transfer function approach which was supported by the current and speed response of the experimental setup.
    - from the loss model of SiC MOSFET in VSI-IMMD and verification by experimental setup at 120V DC supply shows a difference in the simulated and measured loss in drives which can be accounted to several neglected losses contributed by parasitic capacitance and inductance, PCB traces and assumption of linearity in the loss characteristics of the MOSFET.
    - from the thermal modelling of the VSI-IMMD using lookup table loss model, it should come as no surprise that this modeling approach is appropriate for use in providing a rough estimate. However, this is not sufficient for doing an in-depth study on the thermal aspect.
2. From the modelling of CSI-IMMD in the chapter 3, following points can me concluded:

- from the control strategy of CSI-IMMD, multi-loop control using transfer function and bode plots for stability and determining the bandwidth of the controller has been proposed along with the value determination of output filter capacitance giving smoother sinusoidal current and voltage waveform.
- a detailed study on the selection of bandwidth of the controllers and resonance frequency has been performed for stable operation of CSI-IMMD system.
- According to the loss model of CSI-IMMD, the conduction loss in SiC MOSFETs and diodes remains constant throughout operation, however switching loss varies slightly with modulation index, rendering CSI-IMMD inefficient when modulation index is small. The high conduction loss can be accounted to the high diode forward voltage V_f as compared to that of SiC MOSFET.
- from the thermal model, individual heat-sinks are taken into the consideration for the series diodes which show improvements in thermal performance of the system.

3. From the bench-marking analysis of VSI vs CSI at U_{dc}: 850 V, I_{dc}: 15A in chapter 4, following can be concluded:
   - from the switching loss analysis, it can be concluded that the switching loss and its variation in VSI is more comparatively to CSI at different switching frequencies and as the f_{sw} increases the switching loss.
   - from the conduction loss analysis, it can be concluded that the conduction loss in CSI is more than VSI, and the conduction loss in CSI remains constant at different output current which accounts to the flow of current in the MOSFET and diode during zero vector operation of SVPWM.
   - Based on the drive loss analysis of CSI and VSI, it can be stated that VSI works better at low switching frequency ranges, whereas CSI operates more efficiently at high switching frequencies (higher than *121 kHz* in this project). Different operating parameters have little effect on the loss in CSI compared to that in VSI.
   - from the thermal analysis of VSI and CSI, it can be concluded that the CSI performs well as compared to VSI as the loss power is distributed between the heat sink of diode and MOSFET, wherein the diode shares major part of the loss power with lower junction to case thermal resistance R_{jc} compared to that of MOSFET in VSI.

5.2 Future works

This thesis offered a thorough introduction to the design of VSI and CSI for loss and thermal analysis model. Nonetheless, the design provided here is fundamental, and numerous enhancements are possible. Following are some recommendations for future work based upon the work.

1. Due to restriction at the operating speed of the HiSPEM motor due to rotor bearing degradation, the tests were not conducted at rated parameters. Hence after the overhauling of the machine, test should be conducted at rated parameters for VSI.
2. The modelled thermal circuit based on the loss of MOSFET only provide a rough estimation and hence a 3-D thermal model should be prepared to study the thermal performance more accurately.
3. Simulation of the CSI-IMMD system has been the exclusive focus of this project. The results and operation of the converter can be validated in a realistic environment with the assistance of a hardware implementation.
4. The study can be conducted on CSI performance improvement by controlling DC link current using DC-DC converter and use of Bi-Directional switches in H7 or H8 configuration as given in [29].

APPENDIX

A

VSI AND CSI MODELS

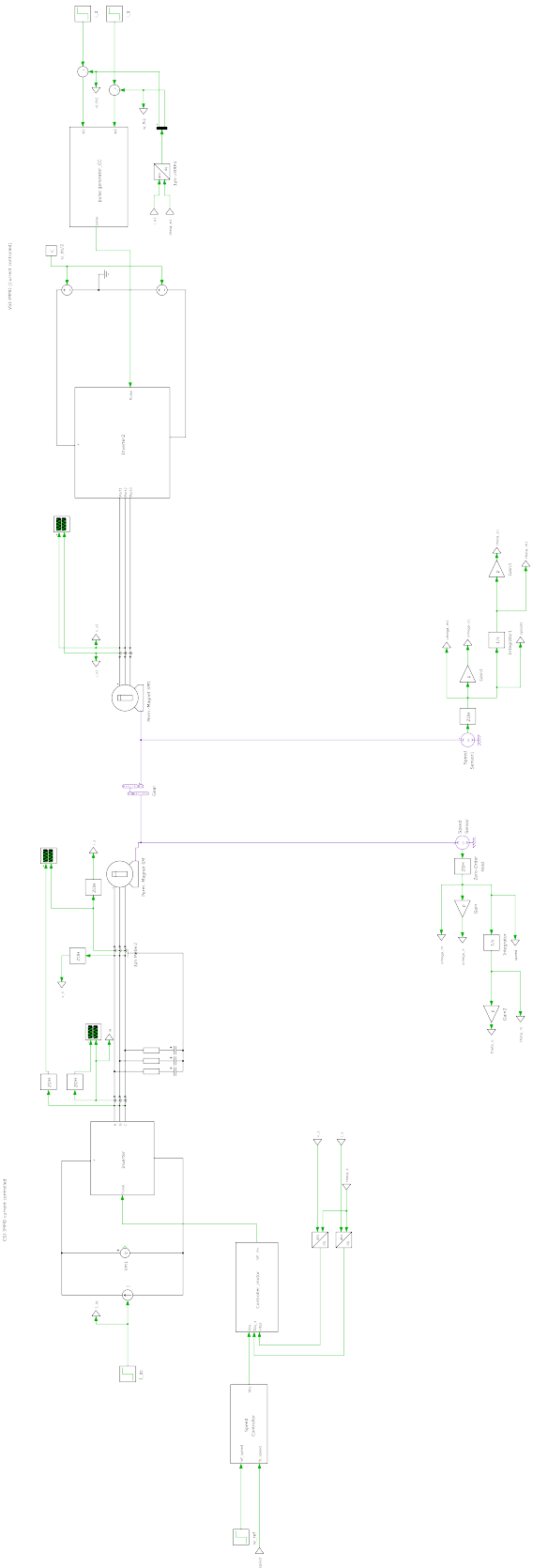


Figure A.1: CSI and VSI bench-marking setup PLECS model

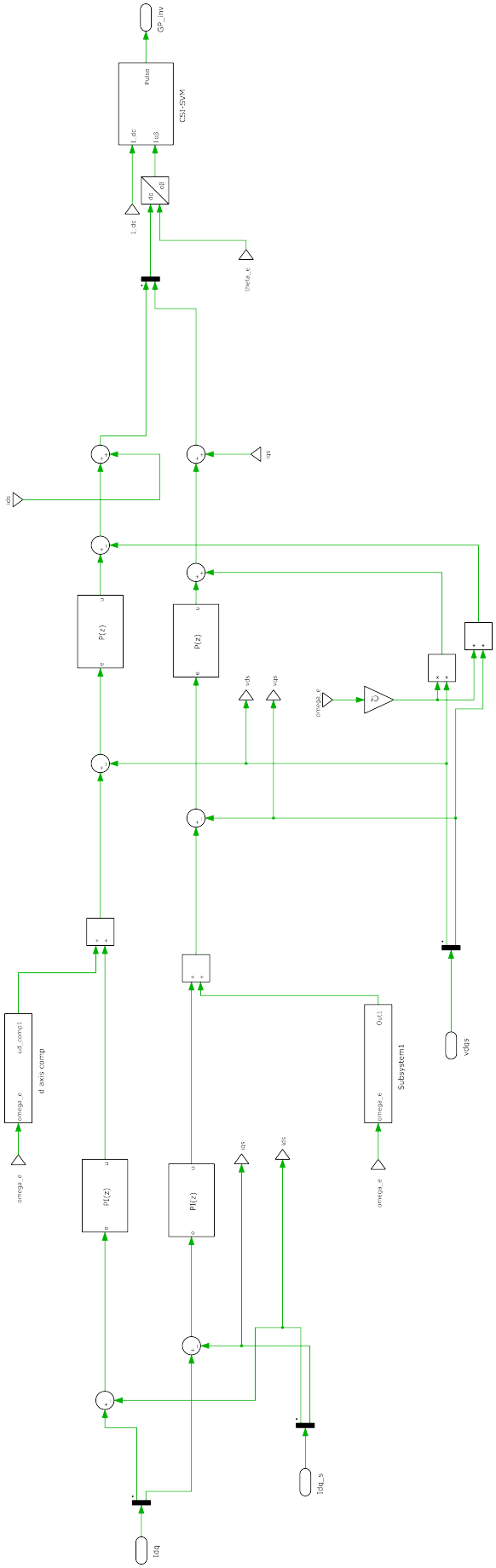


Figure A.2: Current controller for CSI

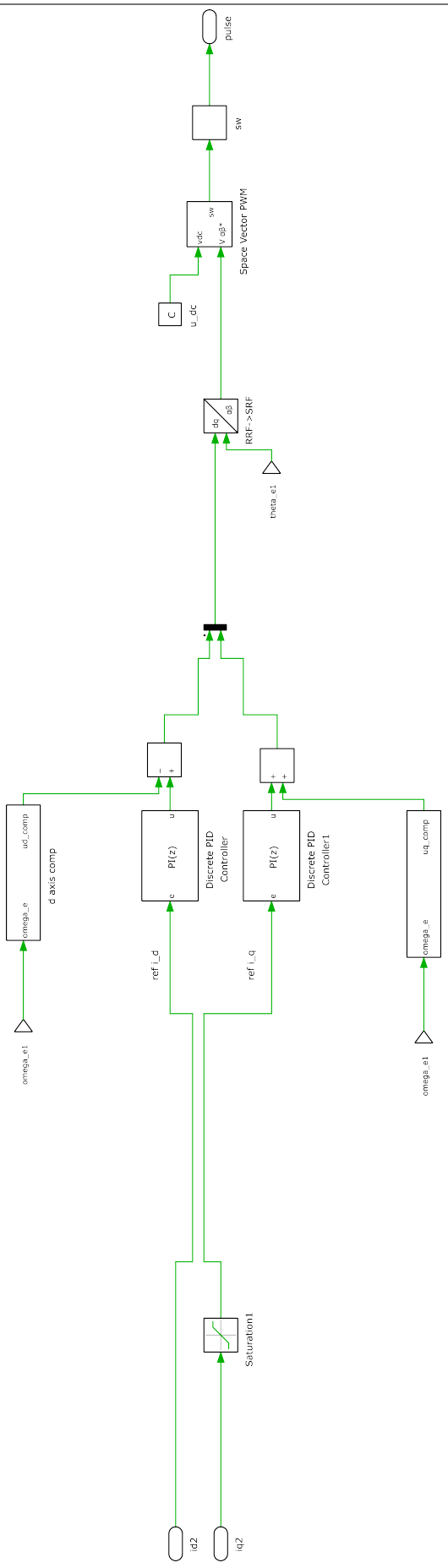


Figure A.3: Current controller for CSI

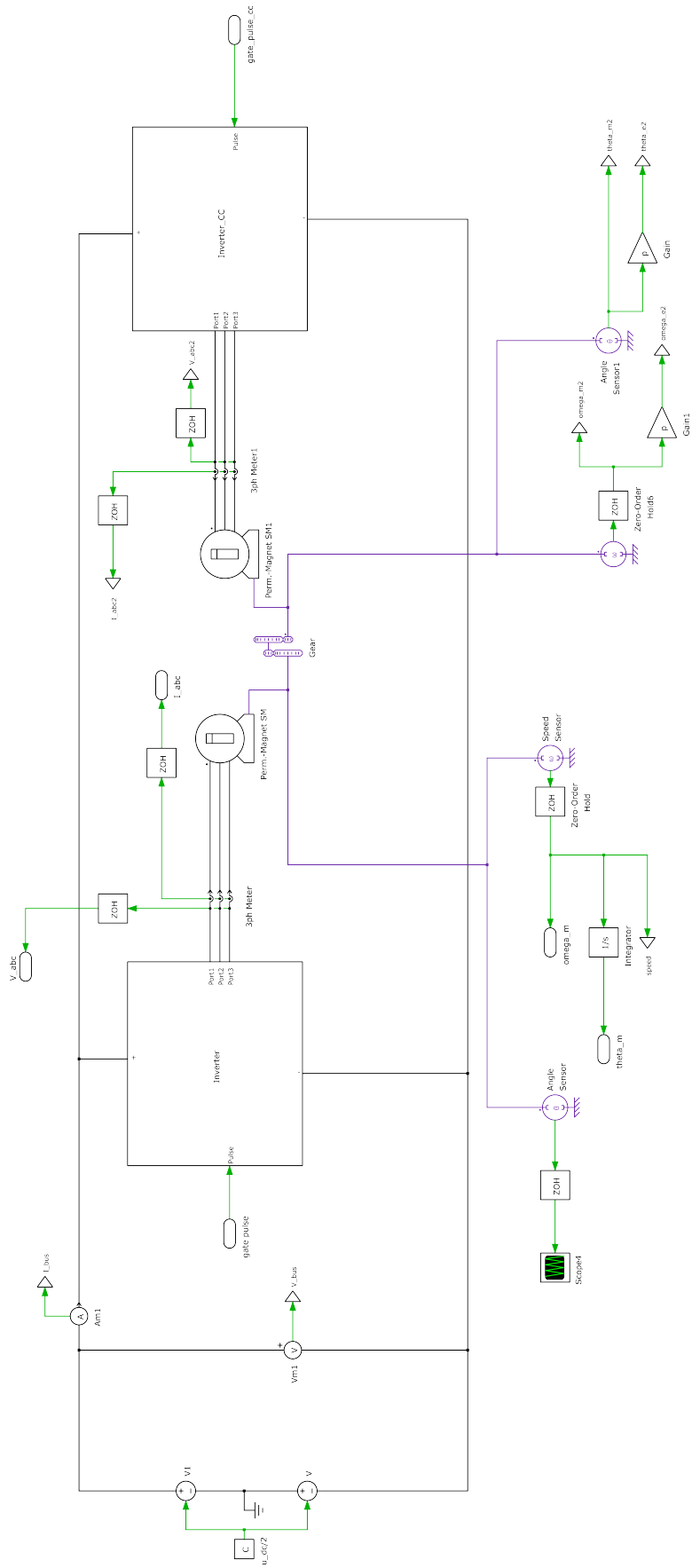


Figure A.4: Speed and current control model of VSI-IMMD

APPENDIX

B

SPEED AND CURRENT RESPONSE

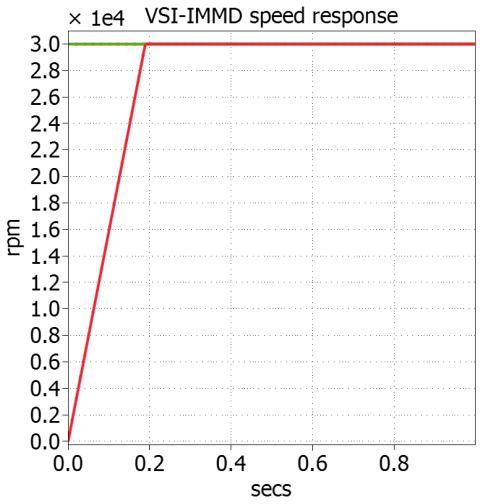


Figure B.1: Speed response of VSI-IMMD

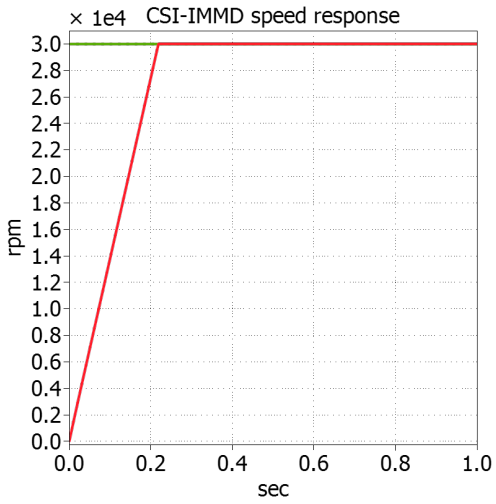


Figure B.2: Speed response of CSI-IMMD

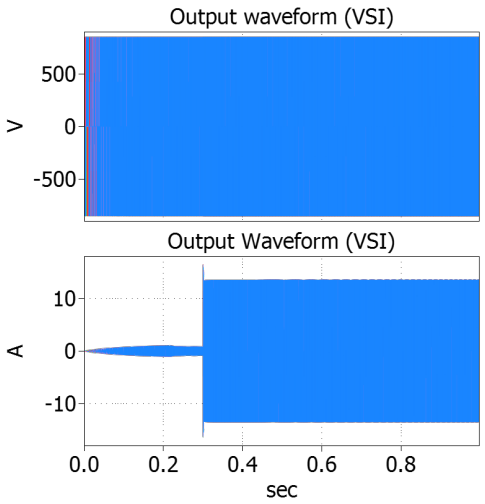


Figure B.3: Transients voltage and current waveform for VSI-IMMD

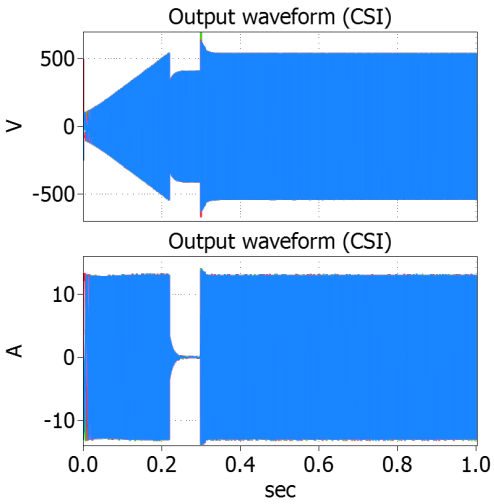


Figure B.4: Transients voltage and current waveform for CSI-IMMD

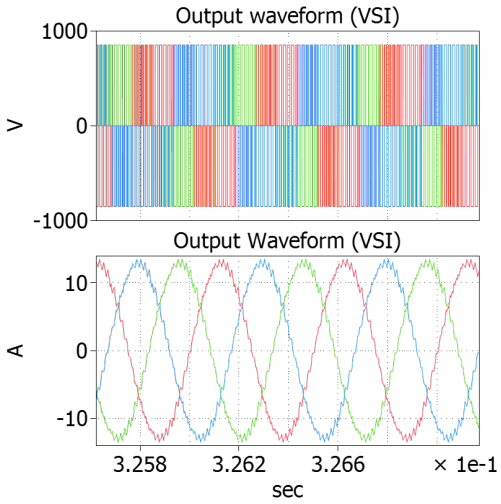


Figure B.5: Stator input voltage and current waveform for VSI-IMMD

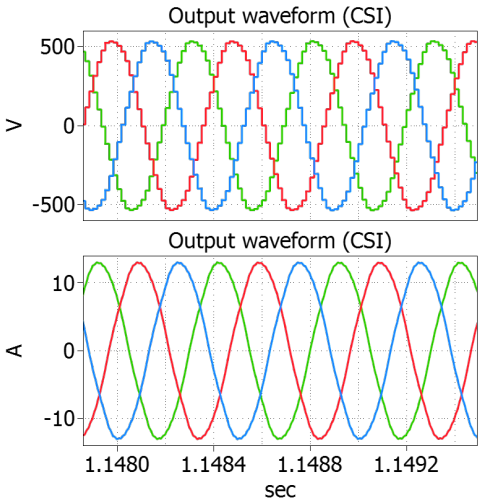


Figure B.6: Stator input voltage and current waveform for CSI-IMMD

APPENDIX

C

ENERGY LOSS

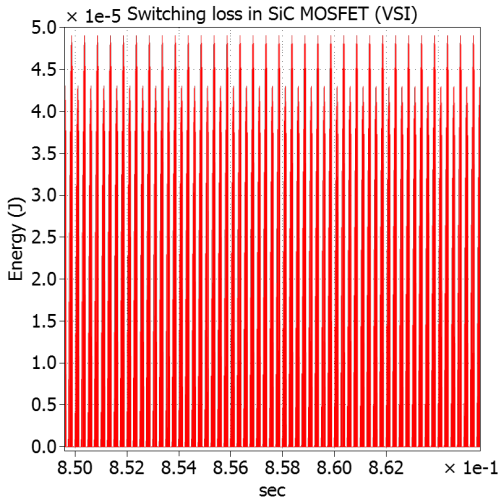


Figure C.1: Switching energy loss in VSI

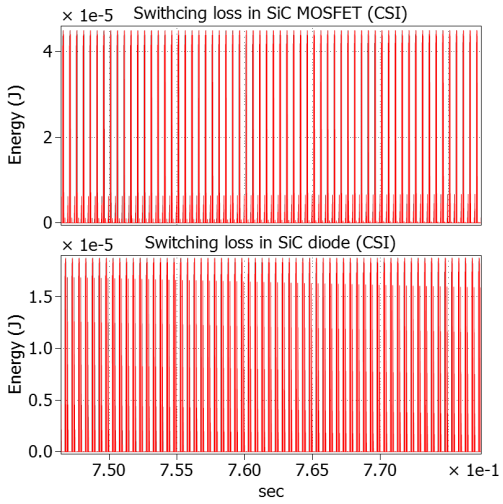


Figure C.2: Switching energy loss in CSI

APPENDIX

D

CODE FOR CSI SVPWM

```
#include <float.h>
#include <math.h>

#define I_dc      Input(0)
#define I_alpha    Input(1)
#define I_beta    Input(2)


#define PI        3.14159265358979323846
#define S_Aon  Output(0)
#define S_Aoff  Output(1)
#define S_A_on  Output(2)
#define S_A_off  Output(3)
#define S_Bon  Output(4)
#define S_Boff  Output(5)
#define S_B_on  Output(6)
#define S_B_off  Output(7)
#define S_Con  Output(8)
#define S_Coff  Output(9)
#define S_C_on  Output(10)
#define S_C_off  Output(11)
#define sector  Output(12)


int sect_pll = 0;

double T0,T2,T1;
double i_angle, i_mag, alpha;
```

```
double angle;


i_mag = fabs(sqrt((I_alpha)*(I_alpha)+(I_beta)*(I_beta)));
i_angle = fmod(atan2(I_beta, I_alpha)+2.*PI, 2.*PI);

//convert radient to degree
angle = 180.0 * i_angle / PI-30.;


if ((angle >= 0)&&(angle < 60)) {sect_pll=0;}
else if ((angle >= 60)&&(angle < 120)) {sect_pll=1;}
else if ((angle >= 120)&&(angle < 180)) {sect_pll=2;}
else if ((angle >= 180)&&(angle < 240)) {sect_pll=3;}
else if ((angle >= 240)&&(angle < 300)) {sect_pll=4;}
else if ((angle >= 300)&&(angle <= 330)) {sect_pll=5;}
else if ((angle >= -30)&&(angle < 0)) {sect_pll=5;}

sector = sect_pll;
alpha = (angle - (sect_pll)*60.)*PI/180.;

   T1 = fmin(sqrt(3.)/2.*i_mag/I_dc*sin(PI/3.-alpha),1.);
   T2 = fmin(sqrt(3.)/2.*i_mag/I_dc*sin(alpha), 1.);
   T0 = fmax(1.-T1-T2, 0.);

switch (sect_pll)
{
   case 0:
      S_Aon = -1;
      S_Aoff =-1+2.*T1;
      S_A_on = -1;
      S_A_off =-1;
      S_Bon = -1+2.*T1;
      S_Boff =-1+2.*(T1+T2);
      S_B_on =-1;
      S_B_off =-1;
      S_Con =-1+2.*(T1+T2);
      S_Coff =1;
      S_C_on = -1;
      S_C_off =1;
      break;

   case 1:
      S_Aon = -1;
      S_Aoff =-1;
      S_A_on =-1+2*T1;
      S_A_off =-1+2*(T1+T2);
      S_Bon = -1;
      S_Boff =1;
      S_B_on =-1+2*(T1+T2);
      S_B_off =1;
      S_Con =-1;
      S_Coff =-1;
      S_C_on = -1;
      S_C_off =-1+2*T1;
      break;
```

```
58      case 2:
59         S_Aon = -1+2*(T1+T2);
60         S_Aoff = 1;
61         S_A_on =-1;
62         S_A_off =1;
63         S_Bon = -1;
64         S_Boff =-1+2*T1;
65         S_B_on =-1;
66         S_B_off =-1;
67         S_Con =-1+2*T1;
68         S_Coff =-1+2*(T1+T2);
69         S_C_on = -1;
70         S_C_off =-1;
71         break;
72
73      case 3:
74         S_Aon = -1;
75         S_Aoff =-1;
76         S_A_on =-1;
77         S_A_off =-1+2*T1;
78         S_Bon = -1;
79         S_Boff =-1;
80         S_B_on =-1+2*T1;
81         S_B_off =-1+2*(T1+T2);
82         S_Con =-1;
83         S_Coff =1;
84         S_C_on = -1+2*(T1+T2);
85         S_C_off =1;
86         break;
87
88      case 4:
89         S_Aon = -1+2*T1;
90         S_Aoff =-1+2*(T1+T2);
91         S_A_on =-1;
92         S_A_off =-1;
93         S_Bon = -1+2*(T1+T2);
94         S_Boff =1;
95         S_B_on =-1;
96         S_B_off =+1;
97         S_Con =-1;
98         S_Coff =-1+2*T1;
99         S_C_on = -1;
100        S_C_off =-1;
101        break;
102
103     case 5:
104        S_Aon = -1;
105        S_Aoff = 1;
106        S_A_on = -1+2*(T1+T2);
107        S_A_off = 1;
108        S_Bon = -1;
109        S_Boff = -1;
110        S_B_on = -1;
111        S_B_off = -1+2*T1;
112        S_Con = -1;
113        S_Coff = -1;
114        S_C_on = -1+2*T1;
115        S_C_off = -1+2*(T1+T2);
116        break;
```

REFERENCE

[1] Thomas M. Jahns. "The Past, Present, and Future of Power Electronics Integration Technology in Motor Drives". In: *CPSS Transactions on Power Electronics and Applications* 2 (3 Sept. 2017), pp. 197–216. ISSN: 2475742X. DOI: 10.24295/CPSSTPEA.2017.00019. URL: http://tpea.cpss.org.cn/uploads/soft/171027/20173197.pdf.

[2] Zhe Zhang and Ali M. Bazzi. "Common-Mode Voltage Reduction in VSI-Fed Motor Drives With an Integrated Active Zero-State Switch". In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 10.3 (2022), pp. 3371–3382. DOI: 10.1109/JESTPE.2020.3037886.

[3] Jiyao Wang. "Design of Multilevel Integrated Modular Motor Drive with Gallium Nitride Power Devices". In: 2015.

[4] Armin Jafari et al. "Comparison of Wide-Band-Gap Technologies for Soft-Switching Losses at High Frequencies". In: *IEEE Transactions on Power Electronics* 35.12 (2020), pp. 12595–12600. DOI: 10.1109/TPEL.2020.2990628.

[5] H Dai and T M Jahns. "Comparative investigation of PWM current-source inverters for future machine drives using high-frequency wide-bandgap power switches". In: 2018, pp. 2601–2608. ISBN: 2470-6647. DOI: 10.1109/APEC.2018.8341384.

[6] Jiyao Wang, Ye Li, and Yehui Han. "Integrated Modular Motor Drive Design With GaN Power FETs". In: *IEEE Transactions on Industry Applications* 51.4 (2015), pp. 3198–3207. DOI: 10.1109/TIA.2015.2413380.

[7] Iqbal Husain et al. "Electric Drive Technology Trends, Challenges, and Opportunities for Future Electric Vehicles". In: *Proceedings of the IEEE* 109 (6 June 2021), pp. 1039–1059. ISSN: 15582256. DOI: 10.1109/JPROC.2020.3046112.

[8] Hirofumi Akagi. "Influence of high dv/dt switching on a motor drive system: A practical solution to EMI issues". In: vol. 16. Institute of Electrical and Electronics Engineers Inc., 2004, pp. 139–142. DOI: 10.1109/wct.2004.239866.

[9] Michael Antivachis. "Input/Output EMI Filter Design for Three-Phase Ultra-High Speed Motor Drive GaN Inverter Stage". In: *CPSS Transactions on Power Electronics and Applications* 6 (1 Mar. 2021), pp. 74–92. ISSN: 2475742X. DOI:

10.24295/CPSSTPEA.2021.00007. URL: http://tpea.cpss.org.cn/uploads/allimg/210331/10.24295CPSSTPEA.2021.00007.pdf.

[10] Benjamin Luckett, Jiang Biao He, and Xinmei Yuan. "Investigation of SiC Current Source Inverter for Medium-Voltage High-Frequency Electric Aircraft Propulsion Applications". In: Institute of Electrical and Electronics Engineers Inc., Nov. 2020, pp. 3476–3481. ISBN: 9781728153018. DOI: 10.1109/IPEMC-ECCEAsia48364.2020.9367841.

[11] Qiuyang Tan, Baoyu Zhang, and Zhaozhong Ruan. "Performance Evaluation of WBG-based Devices in VSIs and CSIs". In: Institute of Electrical and Electronics Engineers Inc., 2022, pp. 40–45. ISBN: 9781665410977. DOI: 10.1109/ICoPESA54515.2022.9754416.

[12] Robert Cameron Bolam, Yuriy Vagapov, and Alecksey Anuchin. "A Review of Electrical Motor Topologies for Aircraft Propulsion". In: *2020 55th International Universities Power Engineering Conference (UPEC)*. 2020, pp. 1–6. DOI: 10.1109/UPEC49904.2020.9209783.

[13] Shan Yin et al. "A 50-kW High-Frequency and High-Efficiency SiC Voltage Source Inverter for More Electric Aircraft". In: *IEEE Transactions on Industrial Electronics* 64 (11 Nov. 2017), pp. 9124–9134. ISSN: 02780046. DOI: 10.1109/TIE.2017.2696490.

[14] Vishesh Biyani et al. "Comparative Study of Different Control Strategies in Permanent Magnet Synchronous Motor Drives". In: *2021 IEEE 5th International Conference on Condition Assessment Techniques in Electrical Systems (CATCON)*. 2021, pp. 275–281. DOI: 10.1109/CATCON52335.2021.9670516.

[15] Najib El Ouanjli et al. "A comparative study between FOC and DTC control of the Doubly Fed Induction Motor (DFIM)". In: *2017 International Conference on Electrical and Information Technologies (ICEIT)*. 2017, pp. 1–6. DOI: 10.1109/EITech.2017.8255302.

[16] Sheshadri Shekhar Rauth and Banshidhari Samanta. "Comparative Analysis of IM/BLDC/PMSM Drives for Electric Vehicle Traction Applications Using ANN-Based FOC". In: *2020 IEEE 17th India Council International Conference (INDICON)*. 2020, pp. 1–8. DOI: 10.1109/INDICON49873.2020.9342237.

[17] Rik de Doncker, Duco W.J. Pulle, and André Veltman. "Advanced Electrical Drives: Analysis, Modeling, Control". In: *Power Systems* 52 (2011), pp. 1–443. ISSN: 16121287. DOI: 10.1007/978-94-007-0181-6.

[18] Euzeli Santos. *Advanced Power Electronics Converters: PWM Converters Processing AC Voltages | IEEE eBooks | IEEE Xplore*. 2017, pp. 243–247. URL: https://ieeexplore.ieee.org/book/7022272.

[19] "GenSiC G3R75MT12J MOSFET N-channel enhancement mode". In: (). URL: https://www.digikey.nl/en/products/detail/genesic-semiconductor/G3R75MT12J/13280392.

[20] Elektronik Verband der Elektrotechnik, Institute of Electrical, and Electronics Engineers. *PCIM Europe digital days 2020 ; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. ISBN: 9783800752454.

[21] Lu Wang. *Modelling and design of a GaN based motor drive for the Nuna solar car*.

[22] Hui Huang, A T Bryant, and P A Mawby. *Electro-thermal modelling of three phase inverter*. 2011.

[23] *Transient thermal measurements and thermal equivalent circuit models*. URL: www.infineon.com.

[24] "Board-Level-Cooling-Surface-Mount-7106". In: (). URL: www.boydcorp.com/aavid-datasheets/Board-Level-Cooling-Surface-Mount-7106.pdf.

[25] Hak-Jun Lee, Sungho Jung, and Seung-Ki Sul. "A current controller design for current source inverter-fed PMSM drive system". In: *8th International Conference on Power Electronics - ECCE Asia*. 2011, pp. 1364–1370. DOI: 10.1109/ICPE.2011.5944414.

[26] Poh Chiang Loh and D.G. Holmes. "Analysis of multiloop control strategies for LC/CL/LCL-filtered voltage-source and current-source inverters". In: *IEEE Transactions on Industry Applications* 41.2 (2005), pp. 644–654. DOI: 10.1109/TIA.2005.844860.

[27] Yang Xu et al. "A Soft-Switching Current-Source-Inverter-Fed Motor Drive With Reduced Common-Mode Voltage". In: *IEEE Transactions on Industrial Electronics* 68.4 (2021), pp. 3012–3021. DOI: 10.1109/TIE.2020.2978691.

[28] Renato Amorim Torres et al. "Current-Source Inverter Integrated Motor Drives Using Dual-Gate Four-Quadrant Wide-Bandgap Power Switches". In: *IEEE Transactions on Industry Applications* 57.5 (2021), pp. 5183–5198. DOI: 10.1109/TIA.2021.3096179.

[29] Hang Dai et al. "Integrated Motor Drive using Soft-Switching Current-Source Inverters with SiC- and GaN-based Bidirectional Switches". In: *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2020, pp. 2372–2378. DOI: 10.1109/ECCE44975.2020.9236394.