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Microfabricated albedo insensitive sun position sensor system in silicon carbide with integrated 3D optics and CMOS electronics

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ABSTRACT

The next generation of satellites will need to tackle tomorrow's challenges for communication, navigation and observation. In order to do so, it is expected that the amount of satellites in orbit will keep increasing, form smart constellations and miniaturize individual satellites to make access to space cost effective. To enable this next generation of activities in space, it is vital to ensure the ability of these satellites to properly navigate themselves. This control starts with attitude measurement by the dedicated sensors on the satellite, commonly performed by sun position sensors. The state-of-the art is confronted by large signal distortions caused by light reflected by the Earth's albedo as well as keeping up with the satellite miniaturization trend. This work aims to address both these issues, by presenting a microfabricated albedo insensitive sun position sensor in silicon carbide with wafer-level integrated optics. The presented $10\,\text{mm} \times 10\,\text{mm} \times 1\,\text{mm}$ system reaches a mean angular accuracy of 5.7° in a ±37° field-of-view and integrates an on-chip temperature sensor with a $-3.9\,\text{mV}\,\text{K}^{-1}$ sensitivity in the 20 °C to 200 °C range.

1. Introduction

The well known miniaturization trend in the semiconductor industry, and its challenges [1], has set the stage for other industries to follow. A similar trend is also true for space satellites [2–5], which implies that their instrumentation must miniaturize with it. But with the cheaper access to space, comes the additional challenge of maneuverability and the tolerance of mistakes. Both these challenges must be addressed by the semiconductor industry, through adaptation of new materials and wafer-level packaging techniques. This article addresses this need for the sun position sensor device, by implementation of a miniaturized microsystem in silicon carbide.

A vital functionality for the vast majority of satellites is the control of the spacecraft direction and position, better known as the attitude control. The attitude control starts with the attitude measurement, which is typically determined with respect to a known reference. Common examples of attitude sensors are magnetometers, sun position sensors, earth horizon sensors and star sensors [6]. The sun position sensor is the most widely used solution as it achieves high accuracy attitude determination, and is typically implemented in conventional silicon technologies. It comes in four architecture types, which are the collimating (Fig. 1(a)), sun-pointing (Fig. 1(b)), tilted mount (Fig. 1(c)) and hybrid types [7]. The sensitivity to the sun direction is often implemented by integration of 3D optics in the package of the device.

The implementation of the sun position sensor in conventional silicon is a sensible cost-effective approach, but renders the device sensitive to a wide spectral band. As such, the reflection from the Earth's albedo can cause large distortions in the signal, that gives errors ranging up to tens of degrees in sunset or sunrise conditions. Future devices should therefore operate in wavelength ranges in the solar spectrum that are not reflected by the Earth's albedo. On top of this, the silicon-based integrated readout electronics are prone to the cosmic radiation in space, thus requiring proper shielding that adds to the size and weight of the device.

In contrast to the cost-effective approach of the integrated photodetectors and readout electronics is the semi-automatic fabrication of the 3D optics during the device packaging. This results in the need for device calibration due to overlay misalignment and is not

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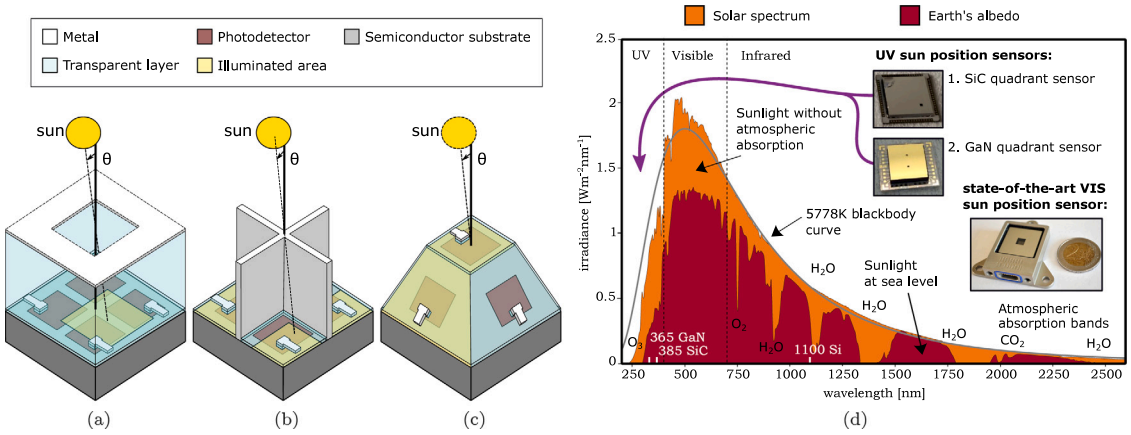

Fig. 1. The schematic depictions of the three types of sun position sensors generally used [7,8], including the (a) collimating sensor, (b) sun-pointing sensor and (c) tilted mount sensor. Spectral intensity information [9,10] of (d) the Sun and the Earth's reflection, with indication of the absorbed spectral bands and responsible molecules in the atmosphere. Two images of albedo insensitive demonstrators in the UV range are provided, along with a state-of-the-art silicon-based device from Lens R&D.

a scalable solution for further miniaturization of the device. Future devices should therefore be fully fabricated using microfabrication and wafer-level packaging techniques, to exploit the industry's capabilities of high overlay accuracy and scalable process flow. Additional care must be taken to ensure optical transmission of the selected spectral band, which may limit the materials and processes used for the optics integration.

There are several spectral bands in the solar spectrum that are not reflected by the Earth, located in the ultraviolet and infrared parts of the spectrum (see Fig. 1(d)). Employment of spectral filters is proposed for the infrared band [11] and basic quadrant sun position sensors are demonstrated in gallium nitride (GaN) [12] and silicon carbide (SiC) [13] for the ultraviolet band. None of these implementations have a scalable wafer-level process or on-chip integrated readout for signal conditioning. From these two materials, technologies in SiC are deemed the most mature option at present. Such technologies include viable application for other sensors or microelectromechanical systems (MEMS) [14–17] and are considered for application in microsystems for harsh environments such as outer space [18].

With the emergence of UV sensors, that are inherently insensitive to the Earth's albedo due to implementations in a wide-bandgap material, the challenge of ensuring optical UV transmittance of the 3D optics is added. Optical windows can be implemented in sapphire, which has excellent UV transmission and is at present competitively priced with glass. Attachment of the optics to the device wafer should not introduce an interface layer in the optical path, but instead place such interface layers selectively by means of lithography. The optical stack benefits from selecting planar configurations, as this is the nature of microfabrication.

This article is the culmination of the technology developed by our research group over the past years, which started with the report of an open 6 µm 4H–SiC CMOS technology [19] in 2021, demonstrating basic circuit blocks. This technology was then complemented by implementation of photodetectors, which led to the demonstration of the first UV opto-electronic system in SiC CMOS [20] in 2022, that incorporates a 64 pixel image sensor. This opto-electronic system is now complemented with advanced wafer-level packaging to integrate 3D optics on top, to implement a high performance and albedo insensitive sun position sensor for satellite attitude control. This devices tackles the two main challenges for the next generation of sun position sensors, which are; (1) signal distortion by the albedo and (2) a scalable integration of the sensor optics. The presented device competes well with the commercially available state-of-the-art, with a mean angular accuracy of 5.7° in a ±37° field-of-view, but is significantly better with dimensions of 10 mm × 10 mm × 1 mm, low power consumption of <60 µW and operation at higher temperature in the 20 °C–200 °C range.

2. Design of the pixel array sun position sensor

From the three main sun position sensor architecture types in Figs. 1(a)–1(c), the collimating sun position sensor is most widely adopted in industry. Its architecture intrinsically allows for shielding against stray light, while the other types do not. It also lends itself best for microfabrication technology, as it is built from a stack of planar layers. It is therefore selected in this work to work towards a scalable implementation.

Digital sun position sensors reach the highest performance in literature and offer some capability towards albedo rejection. Such devices offer a large amount of pixels to effectively capture images through a light mask. Signal processing solutions in software or on-chip hardware can help distinguish between the light spot cast by the sun and the much larger horizon of the albedo. Where there has been progress on digital sun position sensor solutions in conventional silicon, using pixel arrays [21,22] or pixel lines [23], the connections to wide bandgap and scalable optics integrations remain underdeveloped. In order to achieve inherent albedo insensitivity and high performance, digital sun sensors in wide bandgap material are required. These principles are now combined in a pixel array in SiC.

The 8 × 8 pixel array schematic overview at perpendicular exposure is given in Fig. 2(a), indicating rotation axis x and y along with dimensions of the aperture L, optical window h and active area a. For an arbitrary direction within the sensor field-of-view, the light spot moves over the pixel array as indicated in Fig. 2(b). The location of the light spot is directly related to the light source direction through

$$\angle\theta = \tan^{-1}\left(\frac{\Delta x}{h}\right) \quad \text{and} \quad \angle\varphi = \tan^{-1}\left(\frac{\Delta y}{h}\right). \tag{1}$$

It is important to note that Snell's Law must be taken into account when implementing the optical window in anything other than air (see Supplementary Information). To calculate the direction vector, the location of the light spot is extracted by performing a weighted average of the pixel output with their respective coordinates, through

$$\Delta x(\theta) = \frac{1}{S}\sum_{i=1}^{M} I_{\mathrm{PD,i}}(\theta,\varphi)\, x_{\mathrm{i}} \quad \text{and}$$
$$\Delta y(\varphi) = \frac{1}{S}\sum_{i=1}^{M} I_{\mathrm{PD,i}}(\theta,\varphi)\, y_{\mathrm{i}}, \tag{2}$$

where $I_{\mathrm{PD,i}}$ is the generated photo current of each respective pixel, S the sum of generated photo current and M the total amount of photodetectors in the array. Finally, the photo current generation in each pixel is calculated by

$$I_{\mathrm{PD}}(\theta,\varphi) = \frac{A(\theta,\varphi)}{A_{\mathrm{tot}}} I_0 \cos(\theta)\cos(\varphi), \tag{3}$$

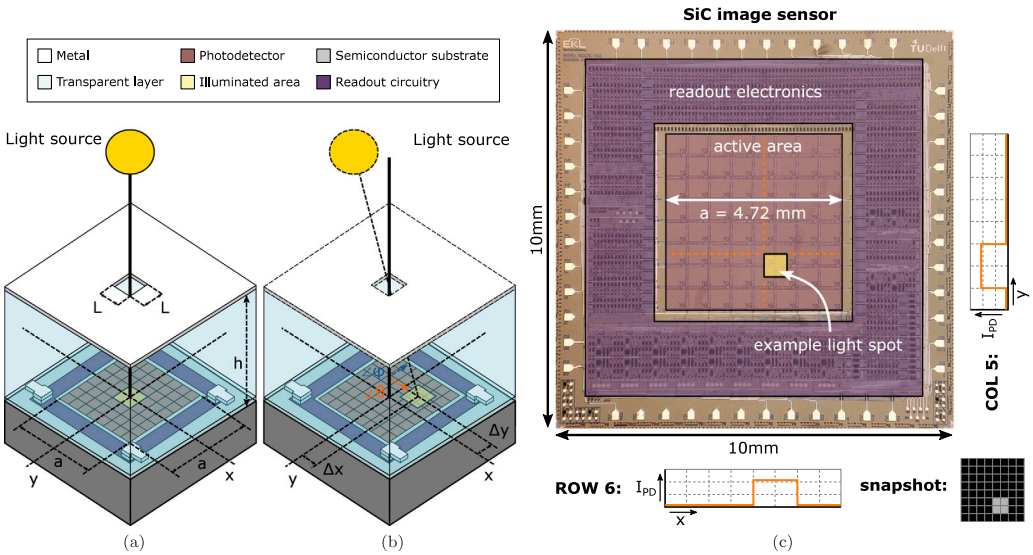

Fig. 2. Schematic overviews of the pixel array collimating sun position sensor at (a) perpendicular and (b) arbitrary direction of the exposure direction. The microphotograph of (c) the integrated 8×8 pixel 4H–SiC image sensor [20] with highlighted active area and on-chip readout electronics. An example light spot of roughly the pixel size is indicated on the sensor active area, with the corresponding pixel responses of the relevant row and column, resulting in the indicated 8-byte snapshot.

where $A(\theta, \varphi)$ is the pixel illuminated area, A_{tot} the pixel total area and I_0 the maximum generated photo current.

3. Preparation of the silicon carbide device CMOS wafers

At present, there are two open accessible silicon carbide technologies for integrated circuits that can be used to implement a UV selective opto-electronic system. These are the bipolar junction transistor technology developed at KTH in Sweden [24,25], which demonstrated a 16×16 pixel array [26], and the complementary metal–oxide–semiconductor technology developed at Fraunhofer IISB in Germany [19,27], which in turn demonstrated an 8×8 pixel array [20].

Integration of CMOS readout electronics is favored for the area efficient implementation of digital logic and the low power consumption. Regarding device miniaturization and the application in space electronics, the choice is made here to use the 4H–SiC CMOS opto-electronic system for the implementation of the sun position sensor. This system is integrated with a complementary to absolute temperature (CTAT) temperature sensor [28], which adds more functionality to the sun position sensor.

The CMOS fabrication on 100 mm 4H–SiC wafers of 350 µm thickness is performed at Fraunhofer IISB and covers a double-well process inside an n-type doped epitaxial layer, with doped guard rings for electrical isolation of individual devices. The devices have polysilicon gates, that are also used for local routing, and sophisticated silicides to form ohmic contacts to the source and drain areas. At present, a single Ti/Al/Ti interconnect layer is available for routing. The cross-sections of the incorporated devices in the opto-electronic system are depicted in Fig. 3(a).

Taking the processed device wafers from Fraunhofer IISB as starting material for the wafer-level integration (Fig. 3(b) step 1), one should note that the top interconnect layer is exposed for probing and wire bonding. To protect the internal connections of the system and avoid potential short circuits, the wafer is coated with a 0.8 µm silicon oxide passivation layer by tetraethyl orthosilicate (TEOS) plasma-enhanced chemical vapor deposition, and patterned to expose the bond and probe pad openings (Fig. 3(b) step 2). No polishing is performed to planarize the wafer front side, leaving step heights of ~1 µm as a result of the CMOS layers.

4. Wafer-level integration of the 3D optics

The 3D optics of the sun position sensor are the vital component that make the sensor angle sensitive. Its implementation and alignment determine the two most important device specifications, which are the field-of-view and sensitivity. Radically different sensor implementations (outside of the common architecture types) that do not require 3D optics in the miliscale can further increase manufacturability and miniaturization. For example, monochromatic light source tracking is demonstrated using angle sensitive pixels based on diffraction gratings [29]. However, such devices face other challenges and have no track record in space missions, so the optical window integration is desired.

The challenge of the integration is in the miliscale dimension of the optical window thickness, that renders microfabrication deposition tools unfeasible. It is furthermore vital to keep access to the front side of the device chip for electrical contacting, as through SiC vias are considered still immature technology. For this reason, pick-and-placing of the optical windows on the CMOS chips is employed, followed by wafer-level bonding to secure them in place. Choosing to pattern the light mask on the optical windows before the bonding procedure, puts tight tolerance on the overlay accuracy to avoid calibration of each device. Though pick-and-place tools can also achieve high overlay accuracy, this comes at the cost of throughput. Therefore, the bare optical window is first secured in place, which is then followed by implementing the light mask using lithography (see Supplementary Information).

There are various means of performing wafer-level bonding, such as direct, anodic, thermocompressive or glass frit bonding. Direct bonding or anodic bonding are considered not compatible with CMOS device wafers [30], and are therefore not compatible with the microfabrication of the sun position sensor. Glass frit bonding is processed up to 450 °C by means of screen printing to obtain selective deposition. Downsides of glass frit bonding are the general need for lead-containing glass and the complex screen printing process, which is time consuming, makes rough mechanical contact to the substrate and requires application specific setups [31]. Finally, the thermocompressive bonding is a more recent trend often used in wafer-level packaging of microelectromechanical (MEMS) devices, and is divided in two classes, which are adhesive and metallic thermocompressive bonding. Metallic thermocompressive bonding, or eutectic bonding, is the formation of a bond through diffusion of typically gold-containing metal layers

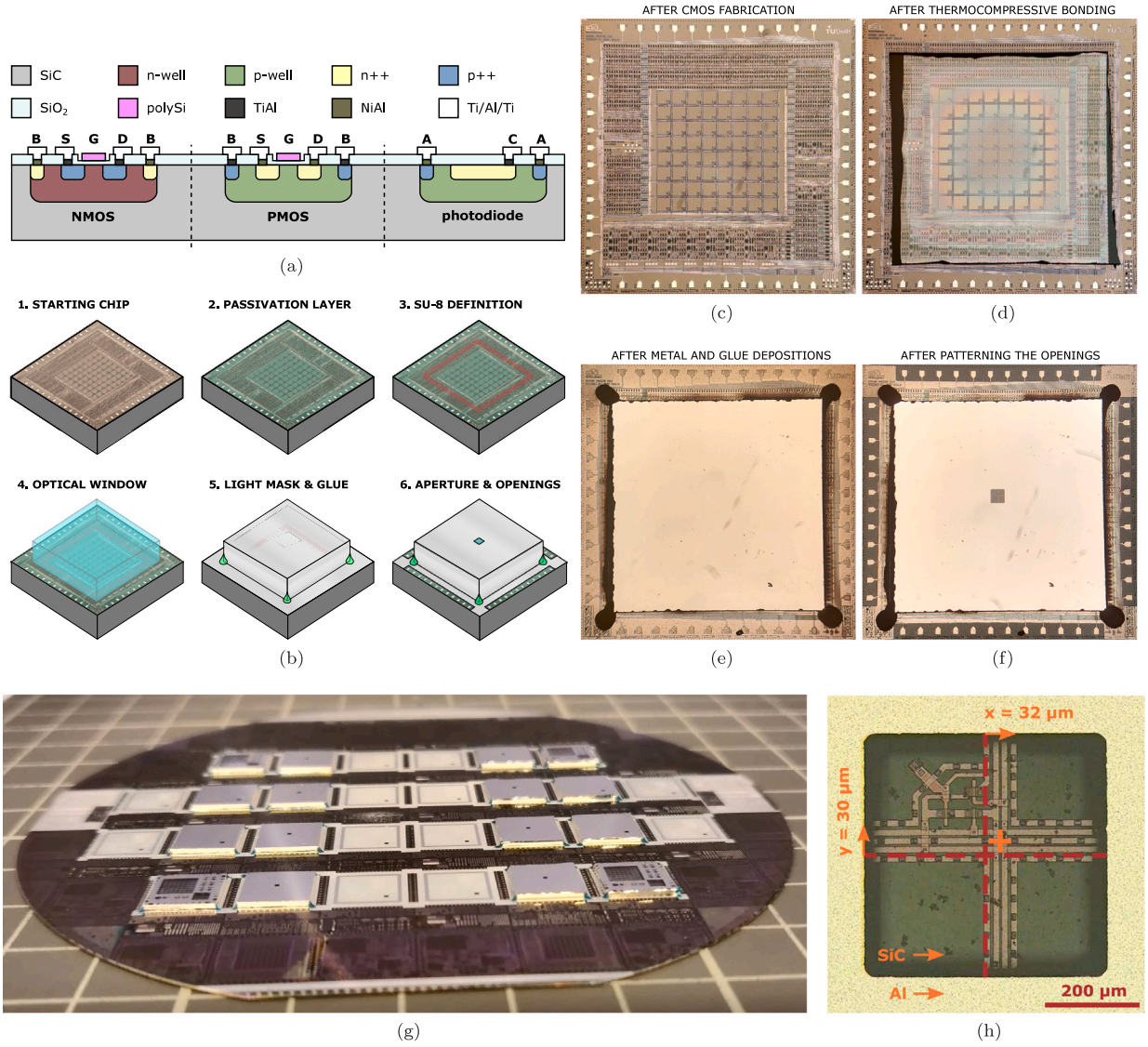

Fig. 3. Schematic overviews of (a) the device cross-sections incorporated in the 4H–SiC opto-electronic system and (b) the 3D optics integration steps. The fabricated results of the key wafer-level fabrication steps in micro photographs, including (c) after the CMOS fabrication, (d) after the thermocompressive wafer bonding, (e) after sputter coating of Al and glue placement and (f) the patterning of the aperture and bondpad regions. The wafer-level process on a (g) 100 mm multi-project device wafer that incorporates 16 optical windows, with the (h) aperture alignment by mask aligner indicated.

into typically a semiconductor interface layer, at elevated temperature and controlled joining force [32]. Adhesive thermocompressive bonding joins two interfaces by activating an adhesive at elevated temperature and controlled joining force, typically using the polymer benzocyclobutene (BCB) [33] or epoxy-based SU-8 photoresist [34]. The integration in this work is based on adhesive thermocompressive bonding, with the adhesive patterned directly on top of the CMOS readout circuits to mitigate the need for more chip area (Fig. 3(b) step 3), and is favored over the metallic counterpart as no metal diffusion barriers are needed.

Sapphire optical windows are used due to the excellent optical transmission in the target UV range (60%–80% for 200 nm–300 nm). To keep access to the front side bondpads, the optical windows are 8 mm × 8 mm × 0.65 mm and centered on the larger chip (Fig. 3(b) step 4). The complete wafer is coated by sputter deposition of 2 µm Al, which has good sidewall coverage (Fig. 3(b) step 5). The aperture and bondpad clearance openings are then patterned and wet etched to complete the device (Fig. 3(b) step 6). It was found that this procedure works well on representative silicon device wafers, but has reproducibility issues for the silicon carbide device wafers with optical window detachment during the wet etching step. A possible reason is the much larger wafer bow of silicon carbide wafers compared to silicon wafers. To counteract this, an additional wafer-level glue deposition step is performed right after the metal sputter deposition. Additionally, future work can optimize the bonding process, taking into account that silicon carbide CMOS wafers are costly.

Micro photographs (Figs. 3(c)–3(f)) indicate the results of the key steps on chip level in the integration process, which is run on wafer-level (Fig. 3(g)). The light mask is patterned using a mask aligner in the current integration, of which the alignment result is indicated in Fig. 3(h). The wafer-level fabrication would benefit from the high overlay alignment accuracy of a wafer stepper for the pattern on the optical windows to achieve monolithic integration of the complete sensor (see Supplementary Information). The microsystem is 10 mm × 10 mm × 1 mm after dicing of the wafer (see Fig. 4).

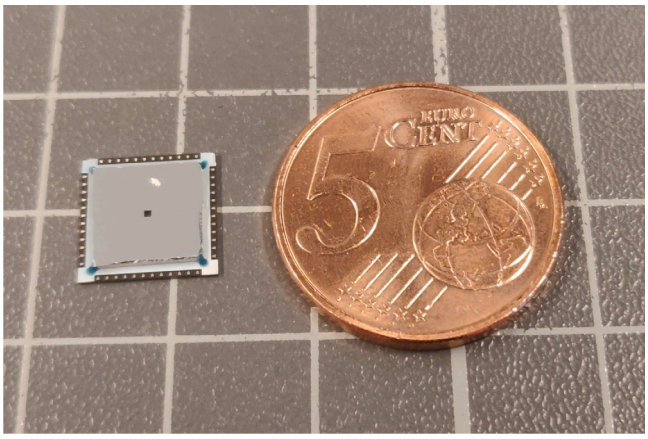

Fig. 4. Photograph of the fabricated sun position sensor chip next to a 5 eurocent coin for size reference, which successfully integrated 3D optics on the opto-electronic system in silicon carbide. The metal light mask on top of the integrated optics conceals the 1263 transistor system.

5. Electrical measurement and operation of the sensor

The 4H–SiC opto-electronic sequential sun position sensor system operates at a 20 V supply voltage, and requires control by correct biasing, a system reset and an asynchronous clock for optimal operation. It offers three output modes that can be read out in parallel, which are; (1) analog, (2) 2-bit and (3) comparator mode. The measurement setup in Fig. 5(a) incorporates off-chip analog level-shifters to allow for interfacing with a conventional microcontroller that controls the measurements. Each level-shifter channel includes LM358 industry standard dual operation amplifiers [35] and resistive feedback (using resistor values >10 kΩ) to implement the factor four increase or decrease for DUT input or output signals respectively. Other external supply signals, such as the power supply and bias pins, are directly provided by TTi EL302RD power supplies. The ultraviolet light source is a mounted discrete 5 mW SMD3535 265 nm UV-C LED, with a full width half maximum (FWHM) of 10 nm. Temperature controlled measurements are performed in a Tenney TPS chamber, with additional temperature monitoring by a TENMA 72-7780 multimeter. Finally, the data is communicated to a laptop for data processing and visualization.

Each output mode is readout sequentially on the clock signal to output all levels in the 64 pixel array. An example of the sequential data is given in Fig. 5(b) for an arbitrary direction to a UV light source, indicating that the outputs are normally HIGH until exposed to UV light. Fixed pattern noise due to pixel mismatch is filtered by correction through a measurement in dark environment (see Supplementary Information). The corresponding captured 8×8 images are shown in Figs. 5(c)–5(e) for all three output modes. The measurements are repeated at 200 °C by placement of the chip and UV LED in a temperature controlled chamber, resulting in the images reported in Figs. 5(f)–5(h), that have no signal degradation of the sequential data nor visible damage to the chip. This would allow for application of the sun position sensor in even harsher environments up to 200 °C, and future reliability work allows for specific classification and further improvement of the device operation at these temperatures. Moreover, improved test setups that allow for characterization at even higher temperatures allow future work to explore the breakdown limit of the device. Note that the UV light source was placed very close (~1 cm) to the device due to limitations of the oven setup, which completely saturates the illuminated pixels and thus mitigates any degradation effects of the UV light source at the high temperature point.

Finally, the integrated CTAT temperature sensor response is measured over the 20 °C–200 °C temperature range. Previous report [28] on its operation was through current biasing, with best results below 1 μA, and measurement of its differential output. For integration in systems for harsh environments such as outer space, operation through voltage bias is preferred. As such, in this work the sensor is biased at voltages that correspond to the best performing current biases at room temperature. The effect of this is that the differential output no longer shows a linear dependency over this temperature range, as the bias current changes over temperature. Fortunately, the single-side output does provide a linear response, with the best linearity at a bias of 9.65 V that yields a $-3.9\,\mathrm{mV\,K^{-1}}$ sensitivity. This is just over half the sensitivity of what is possible through current biasing, and therefore future work should integrate on-chip current biasing.

6. Angular response verification and comparison

The optical measurement setup with automated rotation stage for controlled light source direction is depicted in Fig. 6(a), electrically connected as illustrated in Fig. 5(a). The UV light source is spaced at ~7 cm from the sensor, which is larger than used in the previous section to ensure that no signal is lost due to saturation of pixels. The incident light angle is swept over a ±70 ° range with 201 steps, and the raw sensor outputs of all three modes is provided in Fig. 6(b). These angular outputs are extracted using the transformed 8×8 images at each point in the weighted average algorithm in Eq. (2).

The comparator output mode results in just five levels for the extracted angle, which could be useful for quick verification if the direction towards the sun is perpendicular, under a medium angle or a high angle. The 2-bit mode allows for much more output levels, which scaled proportionally with the added signal levels per pixel. Finally, the analog mode reveals the response curve of the sun position device, which shows non-linearity and deviation from the model prediction. Though the analog mode is most accurate, application in harsh environment would benefit from a digital communication interface to mitigate environmental distortion effects. The comparator mode response is improved by scaling the amount of pixels in the array, but this is challenging considering the technology feature size constraints. Another approach is to increase the amount of bits in the analog-to-digital converter (ADC), which is less demanding on area consumption.

The analog output mode of both rotation axes is corrected by a cosine function (see Supplementary Information) and given in Figs. 6(c) and 6(d). Considering a refraction index for sapphire of $n_2 = 1.8$ at 265 nm, optical window thickness $h = 0.65$ mm, active area $a = 4.72$ mm and aperture dimension $L = 0.5$ mm, a full capture of the ±90 ° field-of-view is predicted. However, the measured response only matches the model prediction in a ±62 ° range, which is caused by a combination of increased reflection and the cosine drop-off, that results in a reduced signal at high incident angles. In particular, the cosine drop-off (see Supplementary Information) predicts that half of the signal is lost at an incident angle of 60 °. Future work can address this by upgrading the presented static range to a readout mechanism that performs a dynamic range, ensuring that large signals do not saturate pixels and small signals stick out from inter-pixel deviations. Such a mechanism may rely on varying the readout frequency, effectively changing the integrating time per pixel, or even on dynamic control of bias levels to optimize both cases.

The measured response follows the model prediction within the ±62 ° range, including the flat response at the higher incident angles. The effective field-of-view therefore becomes ±37 °, as this flat response range is caused by blind spots whenever the cast light spot is completely inside a single pixel. This validates the design, but to make full use of the captured range the aperture dimension should be larger than the dimension of a single pixel (i.e. $L > (a/8)$) in future implementations. The resulting mean angular accuracy is 5.7 ° over both rotation axes within the defined field-of-view, which is calculated for N sets of angular information by

$$\varepsilon_{\mathrm{MAA}} = \frac{1}{2N} \sum_{n=1}^{N} \left| \angle\theta_{\mathrm{n}} - \angle\theta_{\mathrm{n,ideal}} \right| + \left| \angle\varphi_{\mathrm{n}} - \angle\varphi_{\mathrm{n,ideal}} \right|. \tag{4}$$

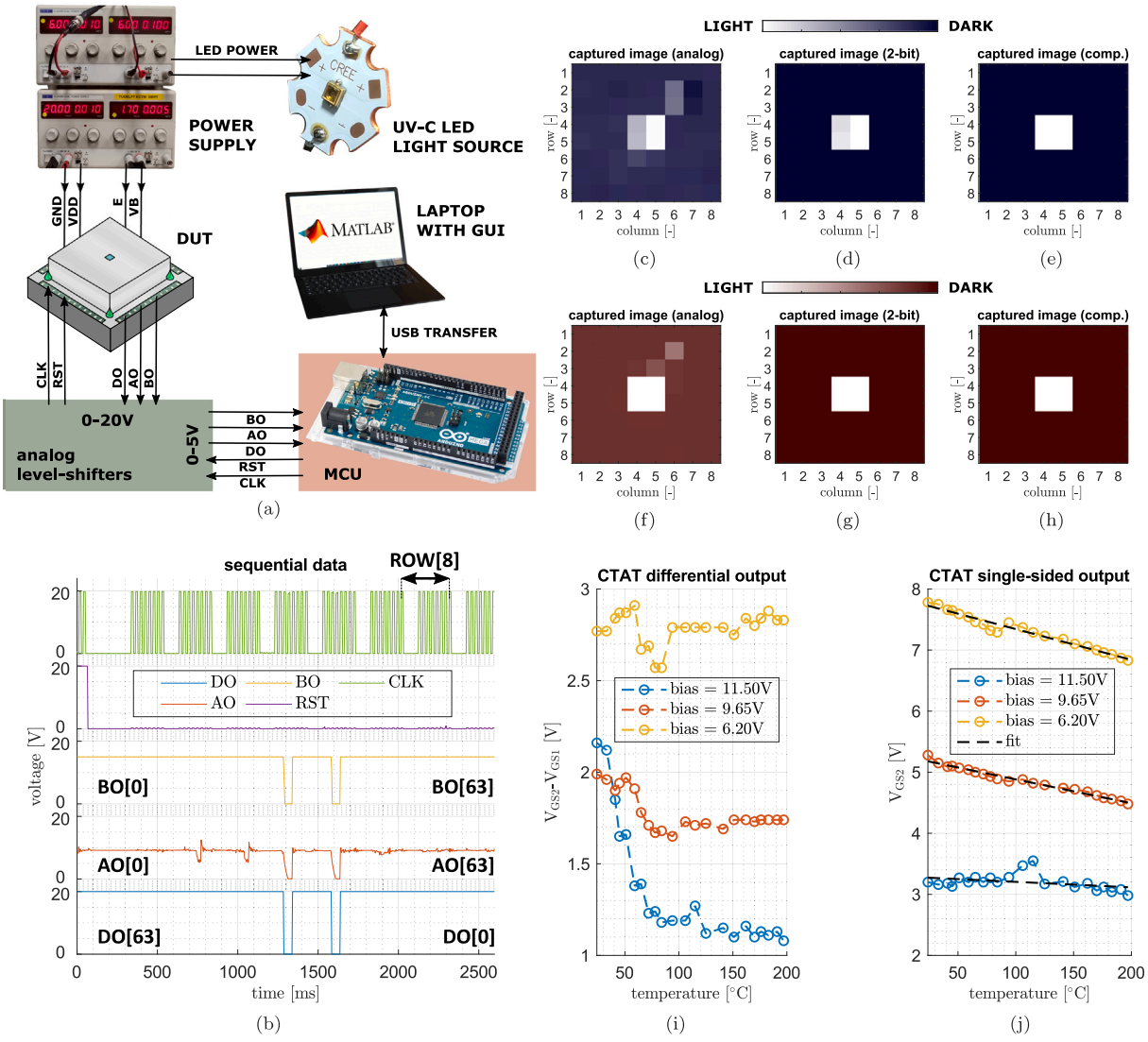

Fig. 5. Overview of electrical measurements on the sun position sensor system, with (a) the system signal connection diagram to control each measurement. The image sensor output for UV illumination at arbitrary direction (b) as sequential raw data and corresponding captured 8×8 pixel images of the (c) analog (AO), (d) 2-bit (BO) and (e) comparator (DO) output modes. The measurement is repeated at 200 °C, resulting in the captured (f) analog, (g) 2-bit and (h) comparator images. The integrated CTAT (i) differential and (j) single-sided temperature responses are captured for the 20 °C–200 °C range.

For future research, the accuracy is increased by optimizing the individual photodetectors, using a thicker optical window for increased sensitivity, reducing the photodetector pixel size, and employing a larger photodetector array.

Finally, an analytic model is considered to find the angular information by direct comparison of pixels in the region of interest. In this case, the light spot always illuminates one, two or four pixels and can be identified by the pixels with the largest response. A basic quadrant algorithm is used to find the centroid [13] and the result is given in Fig. 6(e), reaching a mean angular accuracy of 3.1 ° in the same field-of-view. Although the performance is increased, such analytic algorithms should be used with care as misidentification of the region of interest results in large errors in the extracted angular information.

7. Conclusions

The demonstrated sun position sensor system is implemented in a silicon carbide opto-electronic design, with 3D optics added on wafer-level by thermocompressive bonding and patterning of optical windows. High fabrication yield is ensured by the addition of wafer-level glue dispension, that secures the optical windows for the final fabrication steps. The device offers three output modes that are sequentially read out, and transformed in 8×8 images. The captured light spot under UV exposure is used to extract the angular information through a weighted average algorithm, yielding a mean angular accuracy of 5.7 ° in a ±37 ° field-of-view. The device is furthermore validated for correct operation at 200 °C, and its integrated CTAT temperature sensor response is reported in the same range. The next generation of space instrumentation benefits from this work in twofold; (1) the inherent UV selective response of silicon carbide photodetectors mitigates signal distortion from light reflected by the Earth, and (2) the miniaturization of the device by development of a scalable fabrication on wafer-level. Large scale manufacturing will also bring cost reduction.

Future work on the image sensor sun position sensor in silicon carbide would benefit from optimizing the design parameters to increase the sensor sensitivity and accuracy, while ensuring a wide field-of-view. This can be achieved by using a thicker sapphire optical window or reduction of the active area dimension to inherently increase the sensitivity, while also exploiting the full active area of the sensor which increases the accuracy. Increasing the performance further, demands for increasing the amount of pixels in the image sensor, which implies

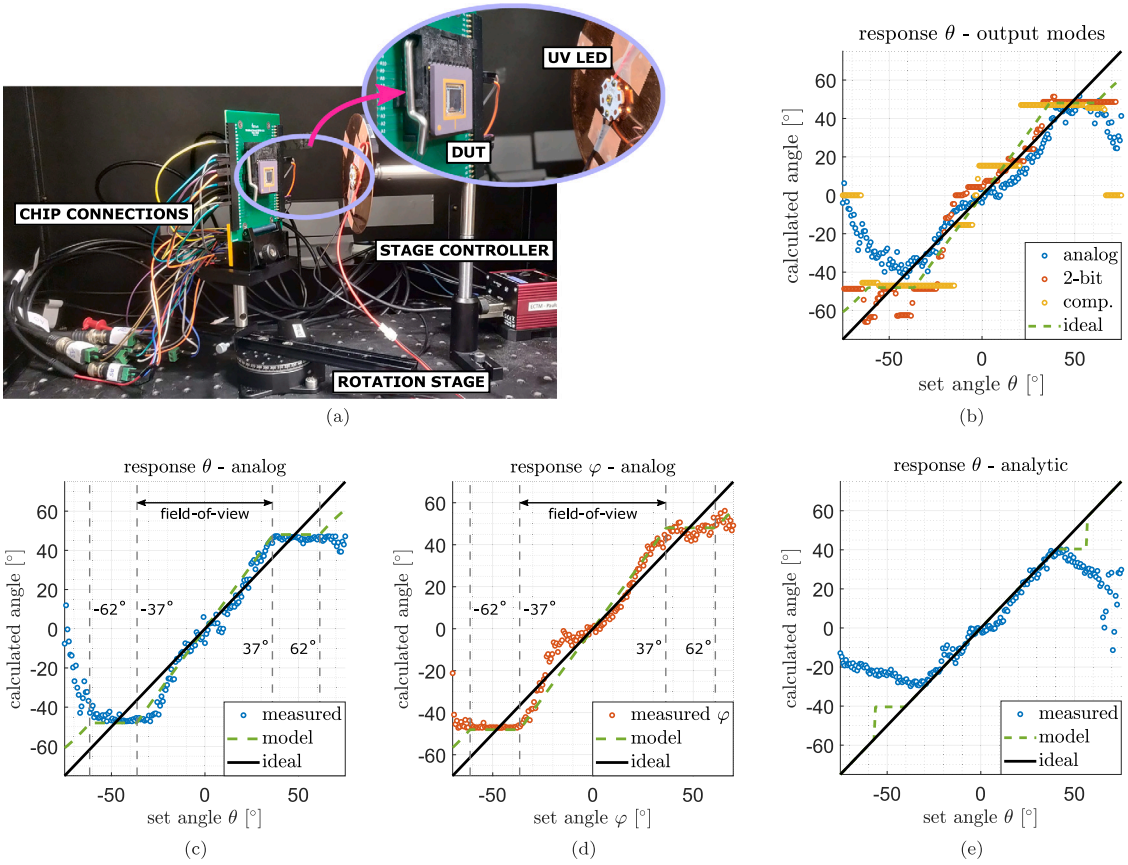

Fig. 6. Overview of angular response measurements on the sun position sensor system, with (a) the overview picture of the measurement setup that resides in a dark enclosure. The extracted angular information of rotation over the θ axis (b) for all three output modes without any data processing. The analog output mode is selected and corrected using a cosine function, for rotation over the (c) θ and (d) φ axes. An indication of (e) using an analytic model instead of the weighted average model.

further reduction of the footprints of the integrated circuit blocks. Lastly, the field-of-view is improved by considering the strong reduction of optical power at increased incident angles, with half of the optical power at an angle of 62 °. Adjusting the pixel integration time, in a dynamic range scheme, is recommended. The field-of-view also suffers from blind spots in the sensor response, which are caused by the smaller light spot than the pixel dimension.

The monolithic integration of the sensor is improved by alignment of the aperture in a wafer stepper, though its misalignment has negligible effect on the current performance limit. Furthermore, the wafer-level packaging benefits from improved bond strength after the wafer-level thermocompressive bonding, to omit the need for the presently employed wafer-level glue dispense step.

CRediT authorship contribution statement

Joost Romijn: Simulated, designed, fabricated and measured all devices, with technical contributions of S.V. in all steps. Investigated the thermocompressive bonding procedure, to define the fabrication of the optics integration. Wrote the manuscript with comments from all authors. **Sten Vollebregt:** Conceived and supervised the project. **Vincent G. de Bie:** Investigated the thermocompressive bonding procedure, to define the fabrication of the optics integration. **Luke M. Middelburg:** Contributed to the design and fabrication as part of the multi-project wafer work flow. **Brahim El Mansouri:** Contributed to the design and fabrication as part of the multi-project wafer work flow. **Henk W. van Zeijl:** Conceived and supervised the project. **Alexander May:** Fabricated the silicon carbide CMOS wafers and ensured the quality. **Tobias Erlbacher:** Fabricated the silicon carbide CMOS wafers and ensured the quality. **Johan Leijtens:** Contributed technical guidance from an industry perspective. **Guoqi Zhang:** Conceived and supervised the project. **Pasqualina M. Sarro:** Conceived and supervised the project.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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Appendix A. Supplementary data

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