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An On-Chip Self-Characterization of a Digital-to-Time Converter by Embedding it in a First-Order $\Delta\Sigma$ Loop

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***Abstract*— To characterize an on-chip programmable delay in a low-cost and high-resolution manner, a built-in self-test based on a first-order $\Delta\Sigma$ time-to-digital converter with self-calibration is proposed and implemented in TSMC 28-nm CMOS. The system is self-contained, and only one digital clock is needed for the measurements. A system self-calibration algorithm is proposed to calibrate nonlinearities of the analog circuitry. The operation is robust over PVT variations since the delay information is normalized to the input clock period. To verify the proposed idea, two different digital-to-time converters performing the on-chip delay are measured and analyzed at 50-MHz clocking frequency with 0.65-ps standard time deviation per measurement.**

***Index Terms*— Digital-to-time converter (DTC), time-to-digital converter (TDC), buit-in selft-test (BIST), first-order delta-sigma modulator, noise shaping, self calibration, PLL.**

I. Introduction

DTC and TDC are two fundamental converters in the time-domain signal processing. In all-digital phase-locked loops (ADPLL) [1], DTC serves as an important building block to control phase of its clocks [2]–[5]. It can relax the TDC linearity and range requirements by bringing reference and variable clocks closer together. It can also facilitate the inherently integer-N PLL to operate in a fractional-N mode by periodically delaying the reference clock edge to be aligned with the variable clock at each comparison cycle. When placing the DTC in the reference signal path, its nonlinearity will proportionately affect the ADPLL's fractional spur levels [8]. Precision of the DTC delay transfer function is essential to estimate the PLL's fractional spur performance, especially given the strong tradeoff between the DTC's linearity and power consumption.

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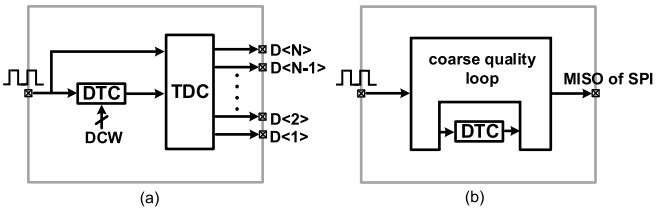

Fig. 1. Direct on-chip measurement of DTC transfer function: (a) conventional method with an ultra-high-resolution TDC, (b) proposed method in which the DTC forms the high-resolution TDC.

To conveniently measure such a DTC transfer function directly on a chip (i.e. autonomously and preferably automatically, e.g. in a high-volume production line), in a way that the sensitive DTC timing output does not have to leave the IC boundary to an external measurement instrument [6], [7], one approach, as illustrated in Fig. 1(a), is to measure it with a TDC of an order-of-magnitude better resolution and linearity, while maintaining sufficiently wide range. However, just as with DTCs, on-chip TDCs equally suffer from nonlinearity, gain and offset errors. Moreover, the resolution is easily affected by the PVT variations [10]–[12], [15]–[22].

The ultra-fine resolution requirement of the instrumentation-quality TDC limits the potential TDC architectures to several choices. A vernier TDC breaks through the gate delay limitation [11]. It even exhibits a 1st-order shaping of its delay line mismatches. However, to achieve, for example, a measurement range of 5 ns and 5 ps resolution, it would require 2000 delay units and 1000 flip-flops. Meanwhile the overall nonlinearity is hard to optimize. To mitigate the range versus resolution trade-off, a vernier ring TDC was proposed in [12], but it still inherits poor linearity with longer range. A 2-D vernier architecture is another step forward, which features a reduced number of delay elements and higher conversion rate. Based on that architecture, Wang *et al.* [21] achieve a solution with good linearity by a spiral comparator array, $\Delta\Sigma$ randomization and two LMS calibration loops. The SAR TDCs explore another direction. A time-domain SAR is implemented in [18]. The range and linearity are limited by the embedded DTC. Another voltage-domain SAR TDC presented in [19] shows same resolution with better linearity, thanks to the high performance of SAR ADC. It translates the information from time domain into voltage domain so it can be processed with a variety of analog signal

processing techniques. However, the information gets distorted to some extend by this transformation. Kim *et al.* [25] use stochastic phase interpolation to achieve a very good resolution and 10-bit range, at the expense of huge area allocated mainly for 2^{10} delay units. Noise-shaping TDCs mainly based on a ring oscillator [22]–[24], [27], [28] and $\Delta\Sigma$ [5], [14]–[17], [26] are quite popular for fine resolution and large range, e.g., 13 ENOB with 6 ps resolution [17], but their measurement accuracy still suffers from process, voltage and temperature (PVT) variations.

To overcome the aforementioned issue of testing a DTC with an instrumentation-quality TDC of ultra-fine precision, which is necessarily sharing the same die in a likely 'hostile' system-on-chip (SoC) environment, we propose to wrap-around the DTC in a loop of low hardware complexity, as shown in Fig. 1(b), in order to create a 1st-order $\Delta\Sigma$ TDC. The resulting resolution is fine enough to be able to characterize the embedded DTC in a built-in selft-test (BIST) manner [6], [7]. Thus constructed TDC requires only one reference clock. Since the TDC range is automatically aligned with a period of this reference clock, it can be of any frequency and quite noisy, which is rather the case in an SoC environment. Even though these clocks may suffer from jitter, with the help of noise shaping, the proposed TDC precision can go beyond the clock jitter.

This paper is organized as follows. Section II explains the proposed 1st-order $\Delta\Sigma$-TDC and its self-calibration. The non-ideal effects are discussed in Section III, followed by the circuit implementation in Section V. The conclusions are summarized in Section VI.

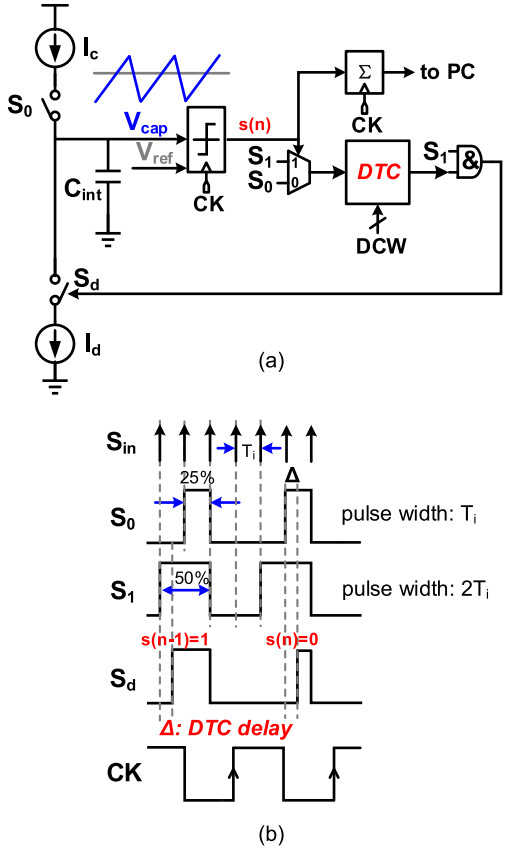

Fig. 2. Proposed first-order $\Delta\Sigma$ TDC architecture. (a) Top level architecture. (b) Timing diagram.

II. Proposed First-Order $\Sigma\Delta$ Time-to-Digital Converter

A. Operational Principle

Inspired by a $\Delta\Sigma$ pulse-width digitizer architecture [9], a 1st-order $\Delta\Sigma$ architecture is proposed in this paper to achieve the required high precision. The proposed TDC, shown in Fig. 2, consists of the DTC under test, a charge pump generating charge (I_c) and discharge (I_d) currents into an integrating capacitor (C_{int}), a comparator and digital logic. An external input clock S_{in} with period T_i is used to generate S_0, S_1 and CK timing signals, all with a period of $4 \times T_i$. S_0 rising edge is triggered by the 2nd consecutive rising edge of S_{in} (as illustrated by Fig. 2 timing diagram) and its falling edge is triggered by the 3rd rising edge of S_{in}. This yields a 25% duty cycle for S_0. S_1's rising edge is triggered by S_{in}'s first rising edge while its falling edge is triggered by S_{in}'s third rising edge. Thus, S_1 is expected to have exactly 50% duty cycle. CK is obtained by inverting S_1 and delaying it for one T_i period.

Without any loss of generality, we designate the rising edge as the critical edge to be delayed by the delay control word (DCW) of DTC. The non-significant (i.e. falling) DTC edge could be unaffected, or delayed with a fixed offset independent of DCW, or yet delayed proportionally to DCW. To avoid any ambiguity across the various DTC implementations, an AND gate is inserted after the DTC output to align the falling edge of the delayed clock with that of S_1. As a result, the DTC and the AND gate reduce the effective DTC input signal pulse width by the DCW commanded delay, which is denoted as Δ. The comparator output stream is $s(n)$, where n refers to the n_{th} cycle of operation. As illustrated, when the comparator's output $s(n-1) = 1$, S_1 is selected to be fed into the DTC. After being delayed by Δ, S_d has a pulse width of $2T_i - \Delta$. In the charge pump, its charging current is always controlled by S_0 with a pulse width of T_i. The charging current I_c and discharging current I_d are expected to be of the same value. Thus, $I_d(T_i - \Delta)$ amount of charge is removed from C_{int}. When $s(n) = 0$, S_0 is chosen to be fed into the DTC input. Then S_d has a pulse width of $T_i - \Delta$. Thus, $I_c\Delta$ amount of charge is added to C_{int}. When the loop is settled, due to the existence of a pole at dc, the average current of the charge pump integrating on the C_{int} capacitor must be zero. Hence, the capacitor voltage must hover above and below a certain fixed voltage level, which is established by the reference voltage V_{ref} of the following comparator. The comparator's 1/0 bitstream information $s(n)$:

$$s(n) = 0.5\left[\text{sgn}(V_{cap}(n) - V_{\text{ref}}) + 1\right] \tag{1}$$

is fed into an integrator. Its completes the TDC functionality with a low hardware complexity. The developed voltage by

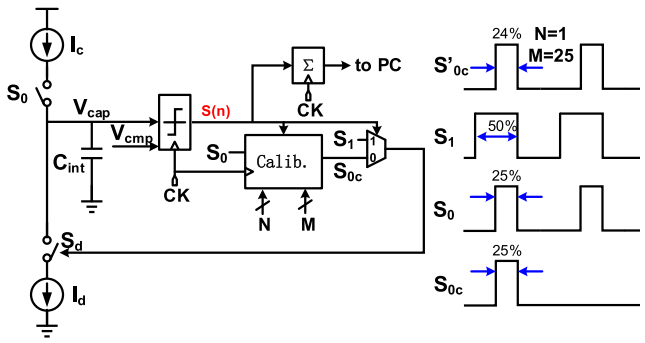

Fig. 3. Proposed system calibration scheme.

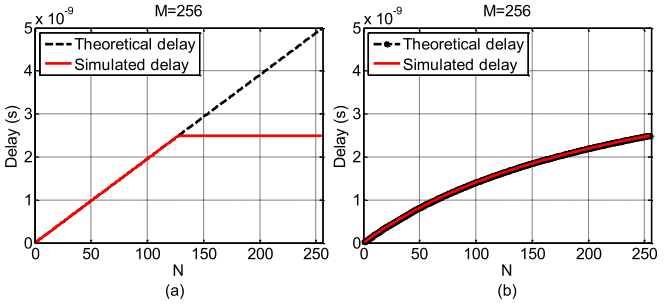

Fig. 4. Calibration mode with two different strategies. (a) Calibration strategy 1. (b) Calibration strategy 2.

the charge pump is:

$$V_{cap}(n) = V_{cap}(n-1) + \frac{I_c T_i - I_d T_i + I_d(\Delta - s(n-1)T_i)}{C_{int}} \tag{2}$$

When the loop runs in a settled state, we get

$$\frac{V_{cap}(k) - V_{cap}(0)}{k} = \frac{I_c T_i - I_d T_i + I_d \Delta}{C_{int}} - \frac{\bar{s} I_d T_i}{C_{int}} \tag{3}$$

where $\bar{s}$ is the average value of $s(n)$. Since the V_{cap} voltage is bounded, both sides of Eq. (3) approach zero when $k \to \infty$. Then, we can obtain the DTC delay expressed as

$$\Delta = \bar{s} T_i - \frac{(I_c - I_d)T_i}{I_d} \tag{4}$$

When $I_c = I_d$, the probability of the occurrence of 1s in the comparator output bitstream, $\bar{s}$, multiplied by T_i results in the DTC delay, Δ.

B. System Self-Calibration

In reality, however, we expect many non-ideal effects. For example, I_c and I_d will be perturbed by the charge-pump output node voltage, V_{cap}. Thus, $I_c(V_{cap})$ is not always the same as $I_d(V_{cap})$. The system performance will be affected by this charge-pump charging/discharging mismatch, as well as the comparator's static and dynamic offsets, noise in the charge pump and comparator. Those systematic non-ideal effects will become part of the measured DTC transfer function, preventing us from getting the intrinsic performance of the DTC. This subsection introduces a way to suppress and de-embed such effects.

As shown in Fig. 3, in the proposed system calibration mode, the DTC under test is bypassed from the measurement path. A digital calibration block is inserted between S_0 and the mux to help generate an equivalent time-averaged delay of the DTC, by omitting some pulses from S_0 in response to the N and M inputs. The comparator output still chooses either of the two different pulse width signals. One is S_1 with a fixed pulse width of 50% (equivalent to 2 T_i), while the other is S_{0c} with an equivalent tunable pulse width, controlled by M and N digital values. Assuming no mismatch between the charging and discharging currents, $I_c = I_d$, $S_d = S_0$ can make V_{cap} stable. Define P_0 as the pulse width of S_0 and P_1 as the pulse width of S_1. Then, ideally:

$$M I_c P_0 = M I_d P_0 \tag{5}$$

The calibration block works in the following way: it takes in S_0 with exactly 25% pulse width (equivalent to a single input period, T_i) and try to bypass N S_0 pulses from every number of M periods. Note that S_0, S_1 and CK have the same period, which is 4× of T_i. For example, when $N = 1$ and $M = 25$, one S_0 pulse is omitted every 25 periods. In this case, to keep V_{cap} stable in the steady-state, one S_1 will be chosen every 25 periods:

$$25 I_c P_0 = 23 I_d P_0 + I_d P_1 \tag{6}$$

The equivalent delay of 1% pulse width equals $0.04T_i$. As the number of 1s over the length of bitstream is denoted as $\bar{s}$, the counter will also give a ratio of 0.04. Thus, the theoretical delay $(N/M)T_i$ and the measured delay $\bar{s}T_i$ should be the same. When the input signal is chosen as 200 MHz, $T_i = 5$ ns. By fixing $M = 256$ and sweeping N from 0 to 255, we can obtain the simulated results in Fig. 4. It can be found that when $N > 128$, the theoretical and simulated delays do not match anymore. That is because for $N > 128$ the omitted pulses stay at 128 for $M = 256$, which can be explained from the following formula.

$$M I_c P_0 = (M - 2N) I_d P_0 + N I_d P_1 \tag{7}$$

To keep the loop stable ($M - 2N$ should be ≥ 0), the maximum N can only be half of M. Then the calibration range is half of T_i. That is to say, the calibration shrinks the measurement range by half. In our chosen implementation, another strategy is adopted. Instead of omitting N pulses among M cycles, we omit N pulses among M S_0 pulses. Based on the above condition, we have:

$$(M + N) I_c P_0 = (M - N) I_d P_0 + N I_d P_1 \tag{8}$$

The theoretical delay $(N/(M + N))T_i$ and simulated delay $\bar{s}T_i$ are also matched, as shown in Fig. 4(b). Similarly, the calibration range still stays at $0.5T_i$. The curvature can be easily corrected in a digital manner.

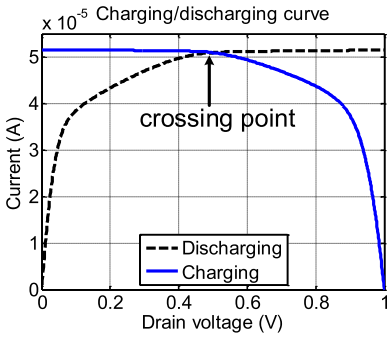

Fig. 5. Post-layout simulation result of charge-pump charging/discharging curve vs. drain voltage.

III. Analysis of Non-Ideal Effects

With the presence of charge-pump current mismatches, comparator offset and noise, the measured delay will deviate from the actual value. In this section, these non-ideal effects are analyzed.

A. Charge-Pump Nonlinearity

We start with the charge-pump (CP) charging/discharging mismatches. To help with visualizing the analysis, Fig. 5 shows post-layout simulation results of the produced CP current vs. its output voltage (i.e., drain voltage of the nMOS/pMOS current-source transistors). As the output voltage changes within the working range (from 0.45 V to 0.55 V at the 0.5 V comparator reference voltage in this context), the charging/discharging current varies slightly due to the channel-length modulation. To improve the current matching, Bou-Sleiman and Ismail [33] overview two main ways: forcing the current match or compensating for the current mismatch. It uses a local feedback and a replica CP to force the current match. Long-channel devices can be used at the expense of speed and increased area and parasitics. Gain boosting [32] and cascoding structure can also help suppressing the channel-length modulation with smaller voltage range for current matching. The above techniques could be helpful in this design with an extra design effort and cost. However, to demonstrate the benefits of the proposed TDC, we choose a conventional CP without resorting to any such techniques.

In this design, the crossing point where the charging and discharging currents precisely match is chosen at 0.5 V, as shown in Fig. 5, which also aligns with the nominal comparator reference voltage V_{ref}. As a result, V_{cap} toggles around 0.5 V when the loop is running. By feeding the Fig. 5 data into a behavioral model, it can be seen that with the nominal $V_{\text{ref}} = 0.5$ V, the simulated delay matches well with the theoretical delay, as shown in Fig. 6.

When V_{ref} is reduced to 0.35 V, the simulated delay has an overall positive offset in both calibration strategies. That is because when V_{cap} toggles around 0.35 V, the charging current is on average larger than the discharging current. V_{cap} is more likely to be above V_{ref}. It can also be explained from Eq. (4): a positive offset expressed as $(\bar{I}_c - \bar{I}_d)T_i/I_d$ is added to the DTC delay.

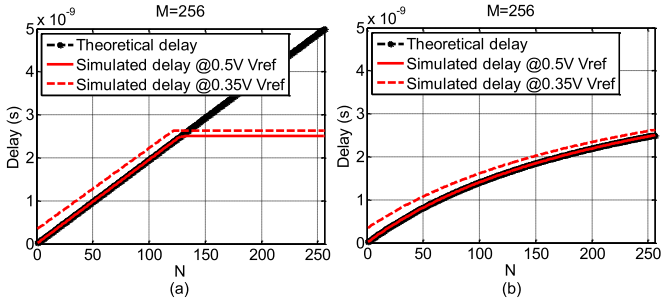

Fig. 6. System calibration due to charge-pump charging/discharging mismatch. (a) Calibration strategy 1. (b) Calibration strategy 2.

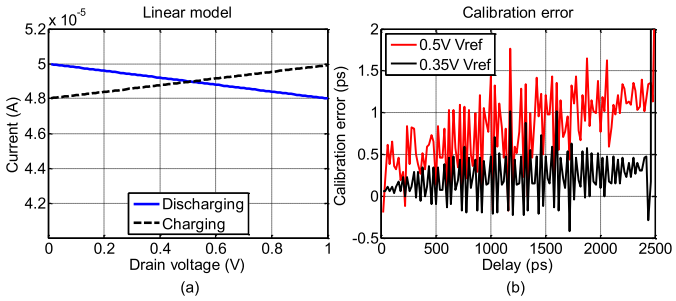

Fig. 7. Linear model and simulation results of charge pump. (a) Simplified model of current mismatch. (b) Calibration error with current mismatch.

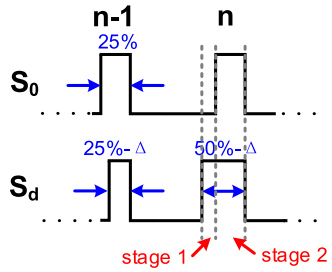

Fig. 8. Working mode from $(n-1)$ cycle to n cycle when $s(n-1) = 0$ and $s(n) = 1$.

As stated above, $I_c(V)$ and $I_d(V)$ are not constant but continuous functions of V_{cap}. Equation (2) cannot hold for the relationship between $V_{cap}(n)$ and $V_{cap}(n-1)$ in face of current mismatches. Assume the charging/discharging curves are linearly related with the drain voltage as illustrated in Fig. 7(a). The following shows the mathematical expressions for the voltage change on V_{cap} per cycle. As shown in Fig. 8, when $s(n) = 1$, the discharging switch first closes for time $T_i - \Delta$ in stage 1. Then both charging and discharging switches close for T_i in stage 2. In stage 1, the charge-pump behavior can be re-written as

$$-dV \cdot C = I_d(V)dt \tag{9}$$

where $C \equiv C_{int}$ for the ease of notation. The voltage integrates from $V(n-1)$ to a temporary voltage V_x at the end of stage 1. The integration time is from 0 to $T_i - \Delta$. The above equation is rewritten as

$$-\int_{V(n-1)}^{V_x} \frac{dV}{I_d(V)} = \frac{T_i - \Delta}{C} \tag{10}$$

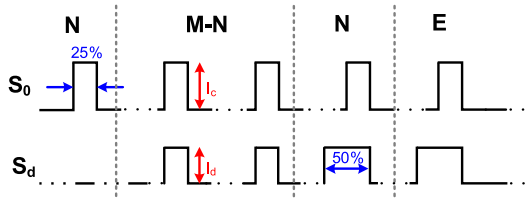

Fig. 9. Calibration mode with charge-pump current mismatch.

V_{cap} is designed to toggle within the range from 0.45 V to 0.55 V. In this small range the charging and discharging curves are assumed linear. The discharging current curve is modeled as a line: $I_d = I(1 + m_1 V)$, where m_1 is a positive slope. Under this assumption, V_x is expressed as

$$V_x = \frac{[1 + m_1 V(n-1)]e^{-(T_i - \Delta)Im_1/C} - 1}{m_1} \tag{11}$$

In stage 2, the charging current curve is modeled as $I_c = I(1+m_2V)(1+0.5m_1)/(1+0.5\,m_2)$, where m_2 is a negative value. In this way, the charging and discharging curves cross at 0.5 V.

$$V(n) = \frac{(2V_x - 1)e^{-2(m_1 - m_2)T_i I/(2+m_2)C} + 1}{2} \tag{12}$$

From the above two equations, (11) and (12), it can be concluded that V_{cap} voltage change from $(n-1)$th cycle to nth cycle is not constant when the current mismatch exists, but a non-linear function of $V_{cap}(n-1)$. By plugging them into the behavioral model, it can be verified that the current mismatch can be tracked by the system self calibration. Under the 0.35 V reference voltage, a higher charging current on average brings a positive time offset to the delay under test, both in the normal working mode and in the system calibration mode. This offset can be suppressed to below 2 ps as shown in Fig. 7(b).

In this work, the system calibration strategy #2 is adopted. Fig. 6(b) is further explained as follows. In Fig. 9, charging and discharging pulses are illustrated under the calibration strategy #2. N S_0 pulses are omitted during M S_0 pulses as desired by the loop. Thus, the discharging control signal S_d has no pulses during N cycles, and 25% pulses during $M-N$ cycles. For the illustration sake, the heights of S_0 and S_d are denoted as the I_c and I_d currents. Hence, the area of these pulses stand for the charge transfer to/from C_{int}. The loop forces the areas of S_0 and S_d pulses to be the same. Ideally, when $I_c = I_d$, omitting one S_0 pulse pushes the loop to choose one S_1 pulse as a compensation. Thus, omitting N S_0 pulses results in extra N S_1 pulses. In total, $N + M$ cycles can be regarded as one period to give the desired delay. After that, a new round of omitting the N S_0 pulses starts. However, when the charging current is on average higher than the discharging current, the loop forces extra E S_1 cycles to compensate the current mismatch. This is reflected by the following equation:

$$T_i I_c(N + M + E) = T_i I_d(M - N) + 2T_i I_d(N + E) \tag{13}$$

The average E can be solved as:

$$E = \frac{(I_c - I_d)(N + M)}{2I_d - I_c} = m_3(N + M) \tag{14}$$

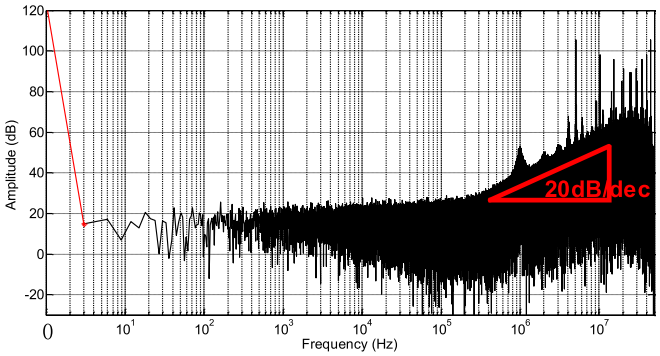

Fig. 10. Noise shaping.

where $m_3 = (I_c - I_d)/(2I_d - I_c) = 1/(2 - I_c/I_d) - 1$. Denote the simulated delay as t_s and the real delay as t_r, then

$$\begin{aligned} t_s &= \frac{N+E}{M+N+E}T_i = \frac{(1+m_3)N + m_3 M}{(1+m_3)(N+M)}T_i \\ t_r &= \frac{N}{M+N+E}T_i = \frac{N}{(1+m_3)(N+M)}T_i \end{aligned} \tag{15}$$

Solving equations (14) and (15), the relationship between t_s and t_r can be obtained as

$$t_r = t_s - \frac{m_3}{1+m_3}T_i \tag{16}$$

$\frac{m_3}{1+m_3}$ is a non-linear function of t_s and depends on the flatness of charging/discharging curves. This is the drawback of calibration strategy #2. Although the curve compression due to the extra E cycles could be corrected digitally, the calibration strategy #1 appears overall a better choice.

B. Noise Sources

The TDC suffer from noises mainly from the comparator transistors, charge-pump current mirrors, input signal jitter, noise of DTC itself and power supply noise of the analog blocks embedded in this TDC loop. To simplify the analysis, only white noise of the comparator 0.1 mV input-referred) and input signal jitter 5 ps rms) are modeled. Frequency of the input clock, S_{in}, is 200 MHz and the loop is running at 50 MHz for 2^{24} cycles. The charge-pump current and integrating capacitor values are 25 μA and 8.9 pF, respectively. The comparator output bitstream clearly exhibits a 20 dB/dec noise shaping slope at higher frequencies, as shown in Fig. 10 based on a system-level model. After averaging the 50 MHz bitstream over 2^{24} cycles, only the noise integrated from DC to 3 Hz is taken into the delay estimation, as shown by the red line in this example. The more cycles the loop runs, the lower effective noise bandwidth we can obtain, thus resulting in better resolution.

In this example, the delay under test is 510 ps and the simulated estimation delay error is within 5 fs. Since the input clock period is 5 ns, $\bar{s}$ is about 0.1. It can be deduced that the C_{int} voltage behaves like a sawtooth curve with roughly one peak per ten cycles. Thus, this pattern manifests itself as a spur around 5 MHz in the frequency spectrum. The amplitude and frequency of the tone change together with the delay

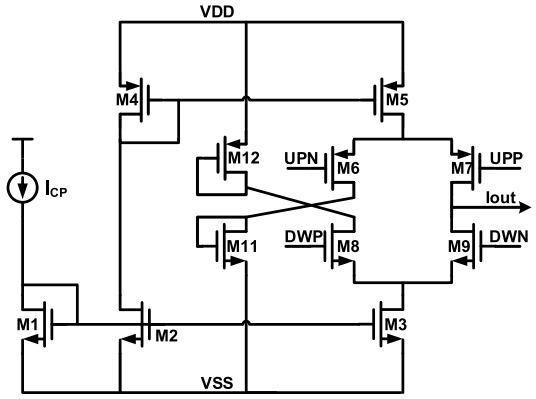

Fig. 11. Charge pump schematic.

under test. Fortunately, with the average operation on the bitstream, those effects have little impact on the delay measurements. By reducing C_{int}, or increasing the charge-pump current, the loop gain is increased which helps suppressing the in-band noise. As a result, the TDC resolution is improved. However, C_{int} voltage variation is enlarged, resulting in more current mismatch from the charge pump.

IV. Circuit Implementation

A. Charge Pump

The DTC delay information is contained in the charge pump (CP) discharging control signals DWN and DWP which are complementary. The CP here converts the pulse width difference into charge sourcing/sinking of its integrating capacitor C_{int}. Thus, the charge pump acts the Δ in this $\Delta\Sigma$ system. The C_{int} capacitor adds or removes a certain amount of charge, and also acts as an integrator, i.e. the Σ.

In this work, a current-steering CP is adopted as shown in Fig. 11. This architecture is favored for its fast switching speed. The control signals are isolated from the current mirror nodes, thus avoiding the large loading capacitances. Both the charging and discharging currents are derived from the same current source I_{CP}, helping to reduce the current mismatch, while also eliminating the uncorrelated noise from two current sources. M_3 and M_5 are always on during the operation. UPP and UPN are the charging control signals, also complementary. During the charging process, M_7 is on and M_6 is off, so the charging current into C_{int} is steered through M_7. If M_9 is off and M_8 is on, the the discharging current I_{out} is steered through M_8. When M_7, M_9 are both on and M_6, M_8 are off at the same time, the CP current will flow to the ground and none of it should go to I_{out}, thus leaving C_{int} unaffected. The size ratio of M_3 and M_5 over M_1 is designed to be 10, making the charging and discharging current ten times of I_{CP}. 2.5 μA is allocated for I_{CP}. 8.9 pF is chosen for C_{int} as the charge pump loading.

Due to the system self-calibration, the current mismatch requirement is eased. Smaller channel length and width can be chosen to reduce the area. No additional opamp is required to enhance the current matching property, thus saving additional power and design complexity.

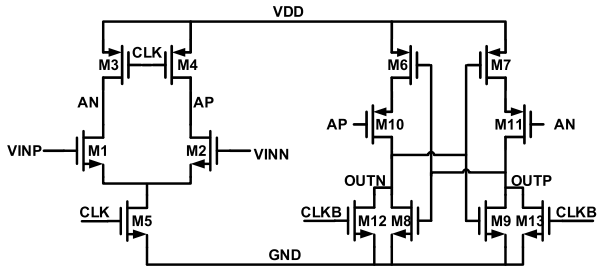

Fig. 12. Comparator schematic.

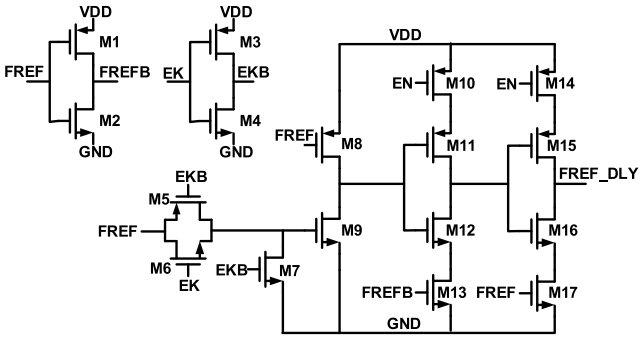

Fig. 13. DTC 1 unit stage schematic.

B. Comparator

A dynamic comparator is chosen in this design for its immunity to supply noise and low-power characteristics [29]. Without any biasing currents, its power scales with the sampling frequency. Shown in Fig. 12, the comparator consists of two stages: the pre-amplifier (M_1–M_5) and latch (M_6–M_{13}).

At the rising edge of CLK signal, the pre-amplifier boosts the voltage difference of the two input signals (i.e., V_{cap} and V_{ref} in Fig. 2). The noise from the following latch is suppressed by this pre-amplifier's gain. CLKB is the inverse of CLK. Before the comparison starts, the comparator's output nodes, OUTP and OUTN, are shorted to the ground. They are then released from the ground during the comparison (regeneration) phase. The complementary pre-amplifier output AP and AN triggers the latch formed by M_6–M_9, speeding up the comparison. An offset cancellation is not required as in [29] due to the system's self-calibration. The noise from the comparator can be pushed to high frequencies thanks to the first-order noise shaping, leaving the dc value largely unaffected.

C. DTC #1

There are two DTCs implemented in this IC chip with entirely different architectures. The first one adopts the architecture from [31]. It comprises 32 cascaded identical delay units. The unit schematic is shown in Fig. 13. It consists of two sub-blocks, which are the clock feeder (M_5–M_9) and delay element (M_{10}–M_{17}). The input signal (FREF) is fed to all the clock feeders, dictating cascaded buffers at the clock input to increase their driving capability. In order to distribute FREF with equal delay to each clock feeder, a balanced clock tree is implemented. Two control signals are needed for this DTC:

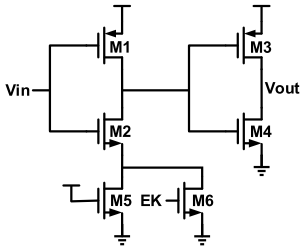

Fig. 14. DTC 2 unit stage schematic.

EK and EN. EK selects which clock feeder to enable, allowing FREF to propagate to the delay element. EN enables the delay elements in the delay unit, whose delay value determines the DTC resolution.

Considering that it is the FREF's rising edge to be delayed, the clock feeder reverses the critical edge to that of the falling edge. Thus, the size for M_9 should be large enough in order to suppress the noise. However, its gate capacitance partially loads the input signal, putting more pressure on on the FREF's driving ability. The EN-gated delay element has a high output impedance. The units those are enabled precharge the source node of M_{11} and M_{15} to VDD. Since the falling edges are critical for the definition of propagation delay at the input/output of the delay unit (M_{10}–M_{17}). Thus, M_{11}, M_{16} and M_{17} are the critical MOSFETs. Their sizes dominate the unit delay. Finer DTC resolution demands larger sizes. That, in turn, demands stronger FREF driving capability from the FREF buffer. Moreover, when M_{17} is larger, the unit delay is also affected by the enabling speed of M_{17}. In other words, after the rising edge reaches the gate of M_{16}, when its drain's falling edge to ground is also determined by when M_{17} is completely enabled. This could explain why the measured transfer function in [31] is not monotonic even though the architecture indicates so. To exclude any possible interference due to the original off-chip measurement method in [31], such as signal distortions caused by bonding wires or PCB interference, this DTC transfer function is checked again with the proposed method.

D. DTC #2

The second DTC is also a cascade of 32 unit stages, whose schematic is shown in Fig. 14. M_5 and M_6 are connected in parallel. The impedance seen from M_2's source to ground is determined by whether EK is enabled or not. M_5 is always on and its on-resistance dominates when M_6 is disabled. When EK $= 1$, the in-parallel on-resistance of M_5 and M_6 is obviously lower than the one when EK $= 0$. The larger resistance between the M_2's source to ground, the longer propagation time for this unit. There are fewer transistors in this DTC architecture, thus lower expected mismatch. This architecture certainly guarantees the transfer function monotonicity. Compared to DTC #1, however, it suffers from a long fixed delay offset. The input signal must go through all the delay units regardless of the DTC control word. The power consumption, on the other hand, should not be substantially higher than in DTC #1, mainly because it does not need a huge buffer to enlarge the input's driving ability. The schematic level simulation results indicate that DTC #1 and DTC #2 consume 11.2 μW and 11.3 μW on average, respectively, at the speed of 50 MHz.

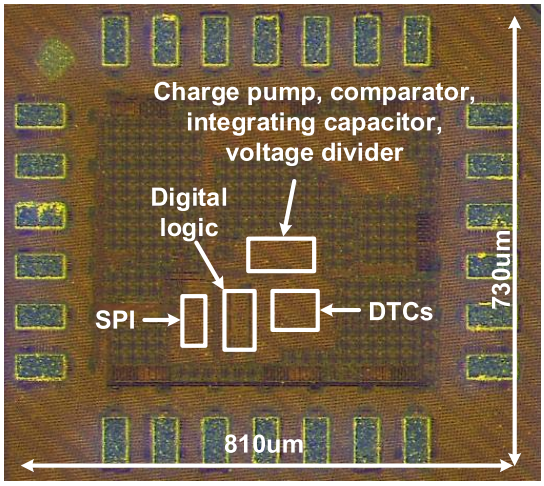

Fig. 15. Die photo.

E. Control and Calibration Logic

The digital block takes in the external high-frequency clock S_{in} and generates all the required timing signals: S_0, S_1 and CK. During the calibration procedure, the summation time of the comparator's output bitstream is controlled by the programmable start and stop events. Thereafter, the summer output can be read out through a serial-to-peripheral interface (SPI). The readout and processing itself are immune to noise or interference, which is not the case in the prior art. For the calibration logic, N and M are programmable for test purposes.

Two DTCs share the same surrounding self-test circuitry but only one is selected during the measurement with a multiplexer (for further details see [8, Fig. 2]). The charge pump discharging signal S_d comes from the selected output, as controlled by the calibration mode enable signal and DTC select signal. Except for the charge pump, comparator and DTCs, all other functions are implemented using a fully digital flow.

V. Measurement Results

A. Experimental Setup

Fabricated in TSMC 28 nm LP CMOS, the chip micrograph is shown in Fig. 15. The measurement setup is drawn in Fig. 16. Only a power supply and a clock generator of moderate jitter are needed to operate the proposed DTC/TDC. A laptop is used to communicate with the chip via SPI. The setup takes much fewer lab resources and shorter measurement time than other measurement methods.

In contrast, the off-chip measurement methods usually need a high-end oscilloscope [36], [37]. A recently published frequency-domain measurement method [38] requires a spectrum analyzer to measure spur levels which are converted to

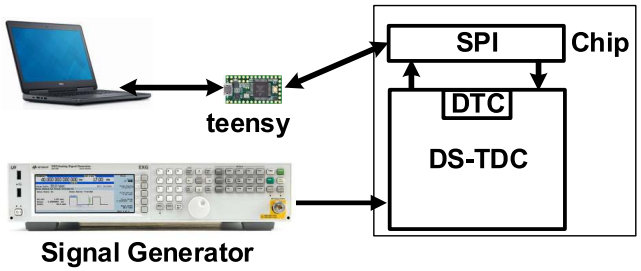

Fig. 16. Measurement setup.

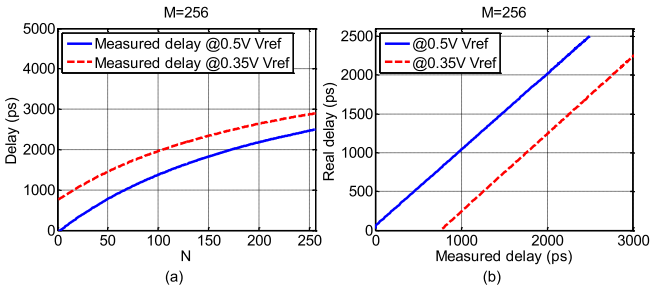

Fig. 17. System calibration measurement results and mapping relationship. (a) Measurement results of system. calibration (b) Mapping of real delay and measured delay.

the delay difference information. As a result, better resolution can be achieved but at the expense of external laboratory equipment and long measurement times, which is especially critical for mass production test. Furthermore, those methods cannot measure the absolute delays because: 1) the DTC signal has to go through the test circuitry and PCB introducing extra delays, 2) such methods are fundamentally based on the time difference measurements. The proposed method, on the other hand, can precisely measure the absolute on-chip delays.

B. System Calibration and DTC Transfer Function

We first calibrate the TDC's own nonlinearity. In the calibration mode, M can choose any value smaller than 2^{32}. To align with the above analysis, it is chosen as 256 here. The calibration mode is run at two different comparator reference voltages, V_{ref}, also for the sake of comparison with the above simulated results. The system calibration results are shown in Fig. 17. In agreement with the simulated case, when V_{ref} drops to 0.35 V, the measured delay curve should shift up. The fact that the actual shift is a bit larger than the simulated one indicates that the current mismatch is larger.

The x-axis, N, corresponds to the real equivalent delay by $t_r = N/(M+N+E)T_i$. Assuming E is constant, we could get the relationship between the measured delay $t_m = (N+E)/(M+N+E)T_i$ and the real delay t_r. The mapping between the real delay and the measured delay is shown in Fig. 17(b). It is evident that the above assumption of E = constant is responsible for most of the nonlinearity. However, this will not cause any issues with monotonicity for the delay being measured. Calibration strategy #1 should be preferred in the future work as it is simpler and does not have to make the above assumption.

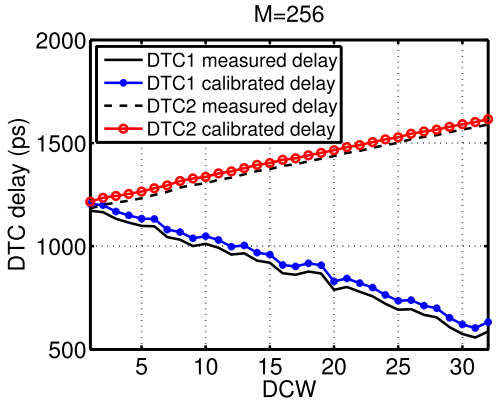

Fig. 18. Measured and calibrated DTC transfer function. (The coincidence of two transfer function origins is accidental.)

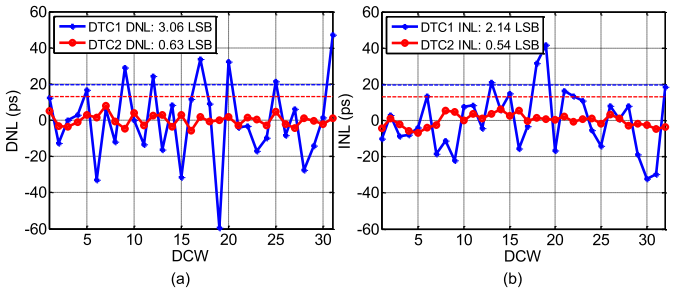

Fig. 19. Measured DNL and INL after calibration. (a) Measured DTC DNL. (b) Measured DTC INL.

Choosing the mapping relationship under $V_{\text{ref}} = 0.5$ V, we can calibrate the measured DTC transfer functions shown in Fig. 18. DTC #1 manifests a clearly worse nonlinearity. It is indeed not monotonic, coinciding with the measurement results in [8] and [31]. As a comparison, the nonlinearity of DTC #2 is much better than expected. It should be noted that the fixed delay offset for DTC #1 is smaller, i.e., 0.6 ns vs. 1.2 ns for DTC #2. This is caused by the input buffers, output inverters (due to opposite critical edge is propagated through the delay units) and delay unit dummies besides the delay units. They altogether contribute around 0.6 ns fixed offset for DTC #1. The measured DTC DNL and INL, after the calibrations, are shown in Fig. 19, in which the dashed lines correspond to the 1 LSB level.

In the measurement, the TDC loop runs for 2^{24} cycles which is less than 0.5 s at 50 MHz frequency. For the two DTC measurements, under each DTC control word (DCW), the measurements are repeated 20 times. The standard time deviation σ_t from the averaged delay can be obtained. The histogram information is shown in Fig. 20(a). The same operation can be done in the calibration mode, in which the DTC under test is bypassed from the loop, so noise from the DTC would be absent. The measurement result is shown in Fig. 20(b). It is centered around zero with σ_t of only 0.65 ps, which indicates that the total noise contributions from input clock jitter, charge pump and comparator are well below 1 ps with 2^{24} measurement cycles. The DTCs dominate the noise contributions. Therefore, by using this method we can judge which DTC's noise is larger. Separate histogram calculations

TABLE I
PERFORMANCE COMPARISON OF DELAY MEASUREMENTS

	[39]	[37]	[10]	[38]	**This work**[1]
Method	off-chip frequency domain	off-chip oscilloscope	on-chip TDC	on-chip TDC	on-chip BIST TDC
Technology (nm)	65	28	90	40	28
Precision (ps)	<0.01	<0.01	∼10	<2	<1
Calibration	No	No	Yes with ADPLL	Yes off-chip	Yes on-chip
Absolute delay	No	No	Yes	Yes	Yes
Power (mW)	NA	NA	6.9/1.8	1.32	0.6

[1] 200 MHz input clock, 2.5 μA charge pump bias current and 2^{24} running cycles are adopted in the above comparison.

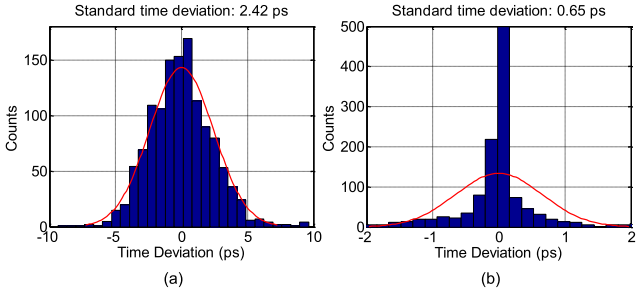

Fig. 20. Histograms of measured DTCs and system self-calibration. (a) Histogram of measured DTCs. (b) Histogram of system self-calibration.

for σ_t for DTC #1 and DTC #2 (including system jitter) show 2.3 ps and 2.54 ps, respectively. Loop measurement with DTC #2 has larger noise due to the smaller transistor sizes and longer propagation time of DTC #2.

Powered by a 1 V supply, the digital logic part consumes 196 μW in both normal measurement mode and self-test calibration mode. There is no appreciable power difference due to the fact that the calibration block keeps running in the normal mode even though its output is not selected. The total power consumption of charge pump, comparator and DTCs (only one DTC is active per measurement) is 402 μW and 391 μW in the normal measurement and self-test calibration modes, respectively. The 11 μW power difference is because in the normal mode one DTC is enabled while in the self-test mode no DTC is enabled.

Table 1 provides comparison with other measurement methods. The off-chip techniques can offer better resolution but require external laboratory equipment, complex setup and long measurement times. Furthermore, they cannot measure the absolute delay. The on-chip TDC methods in [10] and [38] have the potential to measure the absolute delay. However, the TDC gain normalization needs an ADPLL or off-chip measurement support. The proposed measurement method can yield theoretically unlimited precision but practically better than 1 ps as limited by the low-frequency noise.

VI. CONCLUSION

Digital-to-time converters (DTC) play an increasingly important role in PLLs. To precisely characterize their delay and nonlinearity in an on-chip built-in self-test (BIST) manner, first-order $\Delta\Sigma$ TDC containing the DTC under test is proposed and implemented. The entire circuitry is fully integrated in 28 nm CMOS, thus avoiding any issues with off-chip noise and transition time degradation. The resulting $\Delta\Sigma$ TDC can measure absolute delay of its embedded DTC with pico-second level accuracy within 0.5 s when it operates at 50 MHz, regardless of PVT variations.

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