A PV-assisted 10-mV Startup Boost Converter for Thermoelectric Energy Harvesting

Liang, Yansong ; Wang, Ruizhi ; Chen, Zhongsheng ; Du, Sijun

DOI
10.1109/ISCAS48785.2022.9937311

Publication date
2022

Document Version
Final published version

Published in
Proceedings of the 2022 IEEE International Symposium on Circuits and Systems (ISCAS)

A PV-assisted 10-mV Startup Boost Converter for Thermoelectric Energy Harvesting

Yansong Liang[1], Ruizhi Wang[1], Zhongsheng Chen[2] and Sijun Du[1]
[1] Department of Microelectronics, Delft University of Technology, Delft, The Netherlands
[2] College of Electrical & Information Engineering, Hunan University of Technology, Zhuzhou, China
Email: sijun.du@tudelft.nl

2022 IEEE International Symposium on Circuits and Systems (ISCAS) | 978-1-6654-8485-5/22/$31.00 ©2022 IEEE | DOI: 10.1109/ISCAS48785.2022.9937311

***Abstract*—This paper presents a boost converter for thermoelectric energy harvesting with photovoltaic (PV)-assisted startup. The converter employs a new two-phase startup architecture and the PV cell is used in the first phase to provide an initial high voltage for startup. This high voltage drives the boost converter to charge a startup capacitor, which powers the main control block to continue self-startup in phase 2. The proposed system is designed and simulated in a 0.18μm BCD process. The simulations show successful cold-start from 10 mV thermoelectric voltage. In addition, maximum power point tracking and zero current switching techniques are adopted in the system to achieve 91% peak efficiency. The proposed system can finish the cold-start within 250 ms.**

***Index Terms*—thermoelectric energy harvesting, startup, boost converter**

I. INTRODUCTION

Energy harvesting has become a topic with much research interest in the past decade, for its great potentials in power stringent applications, such as IoT sensor nodes, wearable devices, and implantable medical devices. Thermal energy is one of the major sources of ambient energy and is well suited to power wearable devices with body heat. However, thermoelectric generators (TEGs), which convert thermal energy into electrical energy, generally produce a voltage of only tens of millivolts under temperature difference of 1-2 K. This necessitates a DC-DC converter to provide proper voltage to the load circuitry and brings the challenge of cold-start.

Much work has been done with the focus on the cold-start problem[1][2][3][4] in the past years. Low voltage ring oscillator and charge pump are used in [1] and [3] to provide an intermediate voltage for the DC-DC boost converter to start working. No extra off-chip components are needed in these two works, and the minimum startup voltage of [1] and [3] is 50 mV and 60 mV, respectively. Although the circuits are intricate and compact, the startup voltage is still restricted by the lowest voltage a modified ring oscillator can operate. [2] adopts a Colpitts oscillator and [4] uses a transformer to help the boost converter to startup. By introducing different mechanisms as well as extra off-chip components, the minimum startup voltage is reduced to 40 mV in both of the works. However, there is still some room in further reducing the startup voltage.

The proposed startup method in this paper employs a miniature PV cell that provides initial high voltage to drive the switches in the boost converter, thanks to the nonlinear I-V curves of PV cells. The proposed system has been simulated to successfully start from the cold state even when the short circuit current of the PV cell is 100 nA, which represents a 16 mm^2 PV cell in an indoor environment. With the aid of the output voltage and current from this small PV cell, the startup voltage can be significantly decreased to 10 mV.

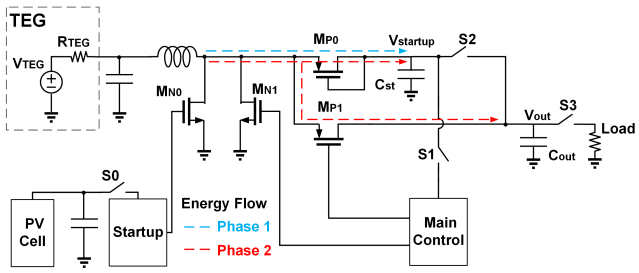

Fig. 1. Operation principle during startup period

This paper is organized as follows. Detailed startup process and the proposed system architecture will be introduced in Section II. Section III will present the implementation of key blocks. Simulation results will be shown in Section IV while Section V concludes the paper.

II. STARTUP PROCESS AND PROPOSED SYSTEM ARCHITECTURE

A. Startup Process

The simplified system architecture is shown in Fig. 1 and there are two phases during the cold-start process. In phase 1, a miniature PV cell provides high enough voltage for the startup block to drive an auxiliary switch M_{N0}. As power from the miniature PV cell is limited, the frequency of M_{N0} gate-driving signal generated by the startup block is unregulated, and the boost converter will not be tracking the maximum power point. The boost converter transfers energy from the TEG to an intermediate startup capacitor C_{st} through a diode-connected PMOS M_{P0}, which prevents energy from back-flowing. During this stage, switches $S1, S2, S3$, and M_{P1} remain OFF.

As $V_{startup}$ rises to a preset voltage at 1.55 V, the main control block is connected to $V_{startup}$ with $S1$ turned ON and the startup block is disabled by shunting PV cell to the

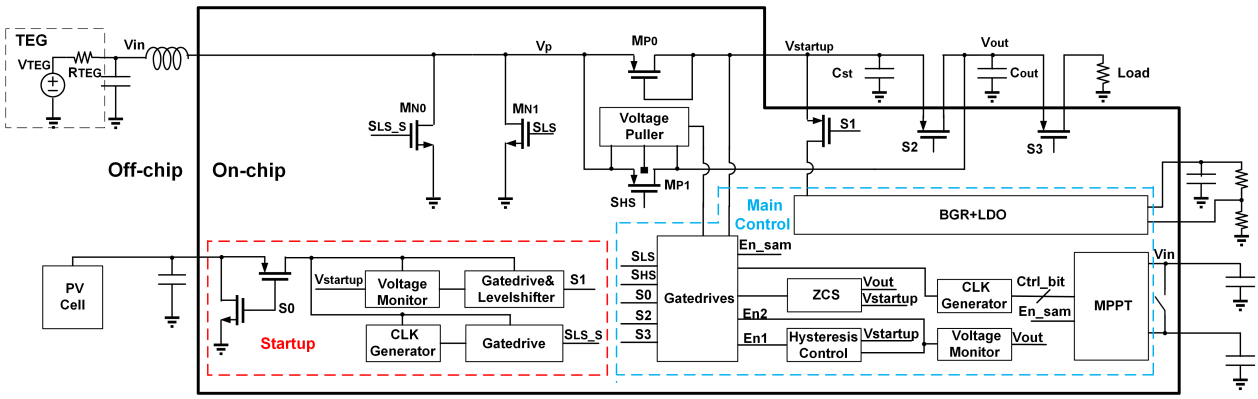

Fig. 2. Proposed system architecture

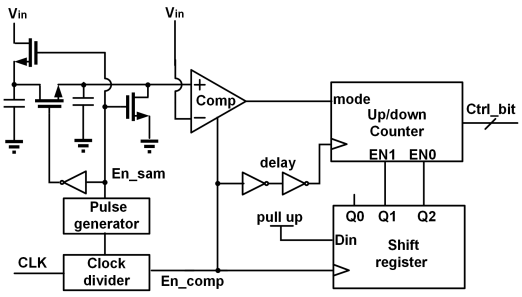

Fig. 3. MPPT block

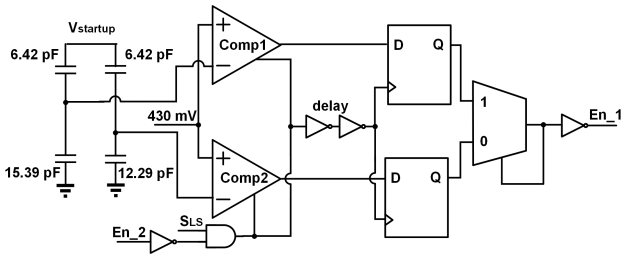

Fig. 4. Hysteresis control block

ground, which marks the beginning of phase 2. In phase 2, the startup capacitor, C_{st}, powers the main control block, which enables the boost converter to extract energy from the TEG with maximum power point tracking (MPPT) and zero current switching (ZCS) techniques. While transferring energy to output reservoir capacitor C_{out}, $V_{startup}$ will decrease due to the consumption of the main control block. The digital parts within the main control block are designed to work under a constant power supply of 1.2 V. Therefore, it is necessary to charge $C_{startup}$ again before $V_{startup}$ falls below 1.2 V. In the proposed design, $V_{startup}$ is regulated in a hysteresis loop: once $V_{startup}$ falls below a preset lower threshold 1.25 V, M_{P1} goes OFF and $C_{startup}$ is charged again until $Vstartup$ rises back to a preset upper threshold 1.45 V. When $V_{startup}$ is between 1.25 V and 1.45 V and C_{out} is charged, little energy is leaked to C_{st}, as turning on M_{P0} requires another threshold voltage over $V_{startup}$, which is always higher than V_{out} during the startup process. Once C_{out} is charged to 1.2 V, S2 and S3 turn ON. C_{out} and $C_{startup}$ are connected together and the load is connected to the system. At this moment, the cold-start process finishes.

B. Proposed System Architecture

The proposed system architecture is shown in Fig. 2, which contains switches of the boost converter and two major control parts: the startup block and the main control block. In the startup block, only necessary circuits to provide switch signal and monitor startup progress are designed, as available power from a miniature PV cell is rather limited. A level shifter is incorporated in the $S1$ gatedrive, which is to make sure that the PMOS to be driven can be completely turned OFF during startup. After phase 1, the startup block will be completely disabled by shunting PV cell to the ground. This does not contradict sending out a proper $S1$ signal, since the signal is always a logic "0" after phase 1.

The main control block is responsible for adjusting the boost converter to extract the most power during startup phase 2 and steady-state operation. The bandgap reference and low dropout regulator provide a stable 1.2 V voltage for the digital blocks, including the voltage monitor, the hysteresis control, the clock generator, the MPPT and the ZCS block. The MPPT block stops the operation of the boost converter periodically through signal En_sam and samples one-half of the TEG open-circuit voltage as a reference. It compares V_{in} and the voltage reference every 64 clock cycles during operation of the boost converter and adjusts switching frequency through a 4-bit signal $Ctrl\_bit$. The ZCS block adjusts the ON time of S_{HS} cycle by cycle to track the zero current point as environment or load condition varies. The circuit implementation of these two blocks will be presented in Section III.

Both hysteresis control block and voltage monitor block are only used in the startup process, which minimizes power consumption of the main control during steady-state operation. The hysteresis control block changes the flowing direction of harvested energy through signal En_1 based on the working

principle mentioned in Section II-A, which maintains $V_{startup}$ in a reasonable range higher than the supply voltage of the digital parts of the main control block. Once V_{out} reaches 1.2 V, signal En_2 becomes high, which disables both hysteresis control block and voltage monitor block.

It is worth mentioning that a pair of cross-coupled PMOS voltage puller, which selects the higher voltage between $V_{startup}$ and V_p, is used to provide body control and gatedriving voltage for M_{P1}. Other gatedrives in the main control block are powered by $V_{startup}$. This is to ensure that corresponding PMOS remain OFF when needed according to the aforementioned working principle.

III. CIRCUIT IMPLEMENTATIONS

A. MPPT

Maximum power is extracted from TEG when the resistance of TEG R_{TEG} matches with the equivalent input resistance of boost converter R_{BC}, which is expressed as (1). f_s is the switching frequency of the boost converter, t_{LS} is the on-time of M_{N1} within one period, and L is the inductor value. In the proposed design, R_{BC} is adjusted through adjusting f_s.

$$R_{BC} \approx \frac{2L}{t_{LS}^2 f_s} \tag{1}$$

The implementation of MPPT block is shown in Fig. 3. En_comp and En_sam become high every 64 and 4096 clock cycles respectively, and each En_sam pulse lasts $\sim$ 630 μs. At every rising edge of En_comp, the output of the up/down counter $Ctrl\_bit$, is increased or decreased based on the output of the clocked comparator. The shift register controls whether the last two bits of $Ctrl\_bit$ are locked or adjustable, the output of which is reversely connected to the enable ports of the up/down counter. During steady-state operation, every bit of the up/down counter is enabled. However, during the startup process, the bits of the up/down counter are enabled gradually to perform a dichotomy settling of switching frequency. Initially, the up/down counter and shift register are reset to 4'b1000 and 3'b000 respectively. At the first rising edge of En_comp, the last two digits of the up/down counter are not yet enabled and only the first two digits are up/down adjusted. As the second and the third rising edge of En_comp arrive, the third bit and the fourth bit are enabled respectively, and all bits are enabled since.

B. ZCS

The ZCS block of the proposed design is adopted from that of [5]. A gate-controlled PMOS is used together with a capacitor as the delay element. By adjusting the gate voltage of the PMOS through a current source, the ZCS block is able to generate pulses with a wide range.

C. Hysteresis Control

Hysteresis control of $V_{startup}$ during startup phase 2 is realized by the circuits shown in Fig.4. Comparator 1 and comparator 2 are responsible for monitoring the upper threshold and lower threshold respectively at the rising edge of S_{LS}

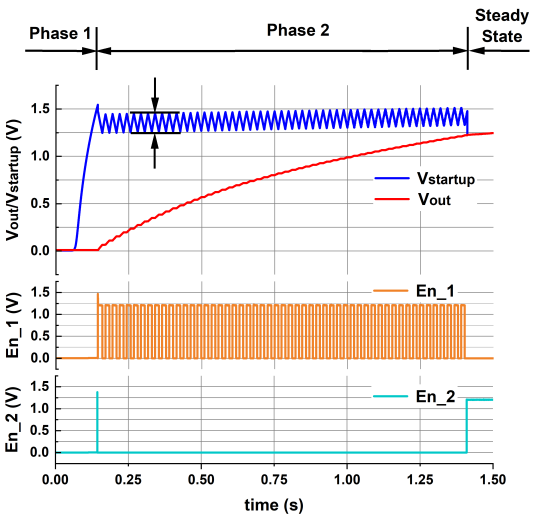

Fig. 5. Simulated waveform during startup period

every cycle until the startup process finishes. The 430 mV reference voltage is generated through a current source and a diode-connected NMOS. Series connected capacitors instead of resistors are used as voltage dividers to reduce off-chip element. Although the accuracy of capacitor voltage divider degrades in long term due to leakage current, this implementation is still acceptable when only used for a relatively short startup process.

At the beginning of phase 2 of the startup process, $V_{startup}$ is high enough for operation and the two D flip flops are reset to zero so that the signal En_1 is high. As $V_{startup}$ decreases, the feedback of MUX makes En_1 lock on high, until $V_{startup}$ falls below 1.25 V and the output of comparator 2 flips. Similarly, En_1 locks on low as $V_{startup}$ increases until it reaches 1.45 V and the output of comparator 1 flips. In this way, hysteresis control of $V_{startup}$ is realized.

IV. SIMULATION RESULTS

The proposed system is designed and simulated in a 0.18 μm BCD process. TEG is represented as a Thevenin source with V_{TEG} ranging from 10 mV - 150 mV and R_{TEG} of 3.6 Ω. The boost converter adopts a 100 μH inductor, a 40 μF input capacitor and a 100 nF startup capacitor. Simulation of miniature PV cell adopts a four-parameter model as [6]. The small resistance is neglected in the I-V characteristic as that has been done in [6], and the I-V characteristic is expressed as (2).

$$I_{out} \approx I_L - I_0 \left[exp\left(\frac{V_{out}}{n_s V_t}\right) - 1 \right] \tag{2}$$

Parameters in (2) are extracted from the datasheet of a commercial miniature PV cell[7], and I_L together with I_0 are further scaled down. In simulation, I_L is 100 nA, I_0 is 0.424 nA and n_s is 15.479, which represents a $\sim$ 16 mm^2 PV cell under 50 lux illumination, equivalent to an indoor environment.

TABLE I
COMPARISON WITH STATE-OF-THE-ART WORKS

References	JSSC'21 [1]	JSSC'18 [2]	TCAS-I'18 [3]	JSSC'12 [4]	**this work**
Process	0.18-μm CMOS	65-nm CMOS	0.18-μm CMOS	0.13-μm CMOS	**0.18-μm BCD**
Startup method	Ring oscillator & charge pump	Colpitts oscillator & charge pump	Ring oscillator & charge pump	Transformer-reuse	**PV cell assistance ($\sim$ 16 mm^2)**
Startup Integration	On-chip	Off-chip inductor	On-chip	Off-chip transformer	**Off-chip PV cell**
Intermediate Capacitor	200 pF	4.7nF	-	-	**100 nF**
Output capacitor	1 μF	4.7 μF	10 nF	10 μF	**470 nF**
Peak efficiency	80%	75%	47%(1)	61%	**91%**
Output voltage	1.2 V	1.1 V	1 V(3)	2 V	**1.4 V - 2.5 V(3)**
Startup voltage	50 mV	40 mV	60 mV	40 mV	**10 mV**
Startup time @startup voltage	252 ms	180 ms(2)	-	-	**250 ms**

(1) Only the efficiency of boost converter, in which a diode is used instead of a PMOS
(2) Estimated from startup waveform
(3) Unregulated output voltage

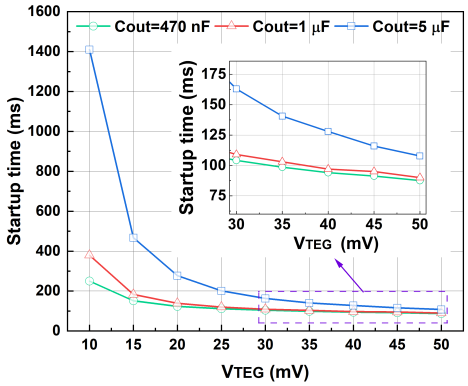

Fig. 6. Startup time for different V_{TEG} and C_{out}

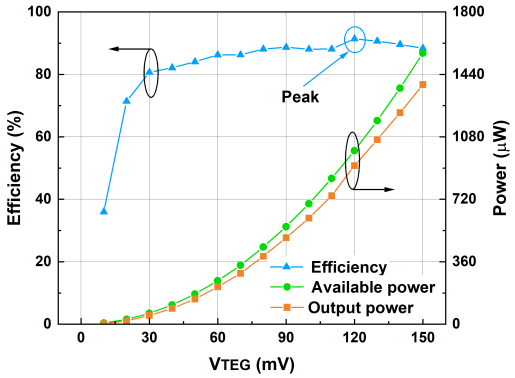

Fig. 7. Harvesting efficiency for different V_{TEG}

The waveforms of key signals during startup with 5 μF C_{out} are shown in Fig.5. In phase 1, $V_{startup}$ increases with the aid of the miniature PV cell. The main control block is not enabled in this phase so En_1 and En_2 remain low. In phase 2, En_1 toggles between high state and low state to control whether C_{out} or $C_{startup}$ is charged. The pulse seen in En_2 waveform is sent out during reset transient of the main control block, which has little effect on the following startup process. V_{out} steps up gradually and $V_{startup}$ is controlled within a hysteresis loop, although the thresholds drift a little due to the circuit implementation mentioned in Section III-C. Finally, the startup process ends when V_{out} reaches 1.2 V and En_2 becomes high to turn on $S2$ and $S3$.

Fig.6 illustrates the startup time versus TEG open circuit voltage V_{TEG} with different C_{out}. Startup time is significantly longer when V_{TEG} are 10 mV and 15 mV, because in both cases, the available power and harvesting efficiency are very limited. As V_{TEG} increases, the startup time decreases sharply at first and decreases at a much slower rate after V_{TEG} exceeds 30 mV. This is because when available power and harvesting efficiency is higher, the shortest startup time is determined by the less efficient stage in the cold-start process, which includes phase 1 and the initial tracking period of MPPT block and ZCS block.

The relationship between harvesting efficiency, defined as output power divided by maximum available power in steady-state, and V_{TEG} is shown in Fig.7. The harvesting efficiency remains high when V_{TEG} is higher than 30 mV. Peak efficiency of 91% is achieved when V_{TEG} is 120 mV based on pre-layout simulations. Table.I shows the comparison with state-of-the-art works. With comparable startup time and harvesting efficiency, the proposed cold-start method enables our design to startup at a thermoelectric voltage of 10 mV.

V. CONCLUSIONS

This paper presents a novel thermoelectric energy harvesting boost converter with PV-cell-assisted startup. With the PV cell providing initial high voltage, the limiting factor for startup becomes power instead of voltage. Proving this theory, the simulation result shows that the startup voltage can be as low as 10 mV, which is the lowest to the best of our knowledge. The startup time is 250 ms and the peak efficiency is 91%, which is comparable to the state-of-the-arts works.

REFERENCES

[1] S. Bose, T. Anand and M. L. Johnston, "A 3.5-mV Input Single-Inductor Self-Starting Boost Converter With Loss-Aware MPPT for Efficient Autonomous Body-Heat Energy Harvesting," in IEEE Journal of Solid-State Circuits, vol. 56, no. 6, pp. 1837-1848, June 2021.

[2] B. Lim, J. Seo and S. Lee, "A Colpitts Oscillator-Based Self-Starting Boost Converter for Thermoelectric Energy Harvesting With 40-mV Startup Voltage and 75% Maximum Efficiency," in IEEE Journal of Solid-State Circuits, vol. 53, no. 11, pp. 3293-3302, Nov. 2018.

[3] M. Dezyani, H. Ghafoorifard, S. Sheikhaei and W. A. Serdijn, "A 60 mV Input Voltage, Process Tolerant Start-Up System for Thermoelectric Energy Harvesting," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 10, pp. 3568-3577, Oct. 2018.

[4] J. Im, S. Wang, S. Ryu and G. Cho, "A 40 mV Transformer-Reuse Self-Startup Boost Converter With MPPT Control for Thermoelectric Energy Harvesting," in IEEE Journal of Solid-State Circuits, vol. 47, no. 12, pp. 3055-3067, Dec. 2012.

[5] J. Kim and C. Kim, "A DC–DC Boost Converter With Variation-Tolerant MPPT Technique and Efficient ZCS Circuit for Thermoelectric Energy Harvesting Applications," in IEEE Transactions on Power Electronics, vol. 28, no. 8, pp. 3827-3833, Aug. 2013.

[6] Y. K. Tan and S. K. Panda, "Energy Harvesting From Hybrid Indoor Ambient Light and Thermal Energy Sources for Enhanced Performance of Wireless Sensor Nodes," in IEEE Transactions on Industrial Electronics, vol. 58, no. 9, pp. 4424-4435, Sept. 2011.

[7] Panasonic Battery. AM-1456-CA. [Online]. Available: https://www.mouser.cn/datasheet/2/315/panasonic_AM-1456CA-1196920.pdf