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Optimization of microporous PDMS membranes for Organ-on-Chip devices

TU Delft

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By

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Abstract

Organ-on-chip (OOC) devices are micro-engineered three-dimensional (3D) biomimetic systems that can be used to create *in vitro* models of human tissue. They provide an alternative for conventional cell culture tools in pharmaceutical R&D. Moreover, these devices can contribute in research focused on understanding complex disease processes. OOC often includes porous membranes made of polydimethylsiloxane. The conventional method to create these membranes has drawbacks such as a limited achievable porosity. A novel approach to create porous PDMS membranes is to use micro-electro-mechanical systems (MEMS)-based fabrication technologies such as etching. With this method, the porosity of the membranes can be finely tuned. Quirós-solano *et al.*[1] used this method and created a thin (>10 μm) highly porous membrane and 3D scaffolds. Furthermore, their membrane could be easily transferred from its substrate to an OOC. In order to achieve this transfer, they incorporated a sacrificial layer of poly acrylic acid (PAA). The high porosity of the scaffold was created by introducing lateral gaps between the vertical pores of the scaffold. The dimensions of the gaps can be tuned by changing the etching time. However, this resulted in complete etching of the underlying layer. In order to reduce the etching time, this project is focused on the mechanism that created the lateral gaps. The contribution of bias power, chamber pressure and chuck temperature to that mechanism are investigated. With the knowledge gained from these experiments, the dimensions of the gaps were tuned by changing the aforementioned parameters.
Furthermore, in this work the fabrication process of Quirós-Solano *et al.* is adapted to create thick (>20 μm) PDMS membranes. These membranes were successfully fabricated and employed by researchers at the University of Technology in Eindhoven.

Acknowledgements

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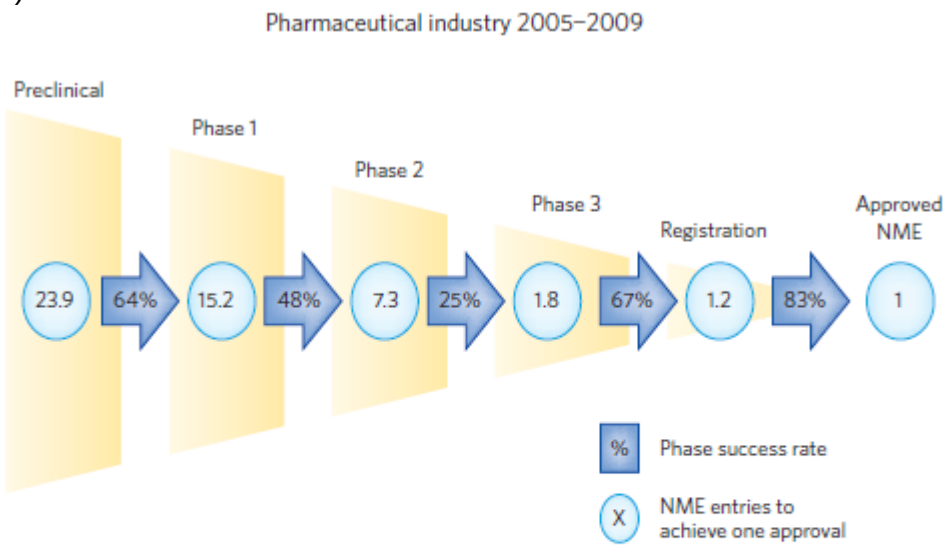
1. Introduction

1.1. Organ-on-Chip device

Drug discovery is a complex, time-consuming and extremely costly procedure. The costs of developing a new drug can take as much as 1 billion USD, depending on the therapeutic area[2]. The high costs are mainly due to high failure rates in the drug development process. Figure 1.1 shows the success rate by phase, although these success rates are likely overestimated as they include new agents against known targets (so-called me-too drugs)[2].



NME success rate by phase. Combined R&D survival by development phase for 14 large pharmaceutical companies (Abbott, AstraZeneca, Bayer, Bristol-Myers Squibb, Boehringer-Ingelheim, Eli Lilly, GlaxoSmithKline, Johnson & Johnson, Merck, Novartis, Pfizer, Roche, Sanofi-Aventis and Schering-Plough). Data from the Pharmaceutical Benchmarking Forum (http://kmrgroup.com/ForumsPharma.html). Approval data is based on approval of NME by a regulatory authority in a major market (EU, US or Japan).

Figure 1.1: Success rate by drug development phase[2]

Ineffective research methods in the preclinical phase are a contributing factor of drug failure and following high costs[3]. The first type of research method consists of *in-vitro* tests. These tests are usually two-dimensional (2D) models where human cells are cultured in a petri dish or well-plate. Only one cell type can be cultured, and the cells are unable to differentiate in more specialized cell types as they would *in-vivo,* because of the lack of environmental cues. Three-dimensional (3D) models, in which several cell types are cultured within a scaffold that works as a supporting environment, better represent the spatial and chemical complexity than 2D models. However, organ-level functionalities such as active tissue-tissue interface and dynamic forces such as tension in skin or breathing movements in the lungs do not occur in 2D nor in 3D models.[4] Therefore, after these *in-vitro* tests the preclinical phase continues with *in-vivo* tests where animal models are used.

OOC's are micro-engineered fluidic devices in which living cells are cultured. They mimic the complex structure and physiology of human organs. The goal of OOCs is to overcome the limitations described above by recapitulating tissue-tissue interfaces, spatiotemporal chemical gradients, and dynamic mechanically effects into one model. It is already possible to fabricate micromodels of brain[5], liver[6], vessels[7], kidney[8], gut[9,10], bones[11],

lungs[12], muscles[13], heart[14] and blood-brain-barrier[15]. As each human organ is characterized by its own architecture and functions, each organ is mimicked with a particular OOC. These are highly simplified models in which one kind of cell is cultured in a single, perfused microfluidic chamber, for instance renal tubular epithelial cells in a Kidney Chip or hepatocytes in a Liver Chip[16]. Cell culturing is not possible in case of brain tissue, so a slice of brain is cultured on a membrane [5].
In more complex designs, two or more microchannels are connected by porous membranes. Huh *et al.* developed a Lung-on-Chip which mimics a human alveolar-capillary interface. On one side of the membrane, human alveolar epithelial cells were cultured and stimulated with air flow. On the opposite side, capillary endothelial cells were cultured with flowing medium representing the blood flow. Mechanical relevant forces were simulated by two lateral microchambers in which vacuum could be applied. This vacuum causes an elastic deformation of the wall separating the cell-containing parts of the model, stretching the cells on the membrane. Releasing the vacuum results in an elastic recoil of the cells. These actions mimic the normal inspiration of the lungs in which the alveoli expand[12] (Figure 1.2). Similarly, Huh *et al.* developed a Gut-on-Chip (Figure 1.3) in which the vacuum chambers simulates peristaltic motions[9]. These studies showed that the mechanical stimulations improved the *in vitro* tissue architecture and strongly promoted differentiation of the cell lining[9,12,16,17].

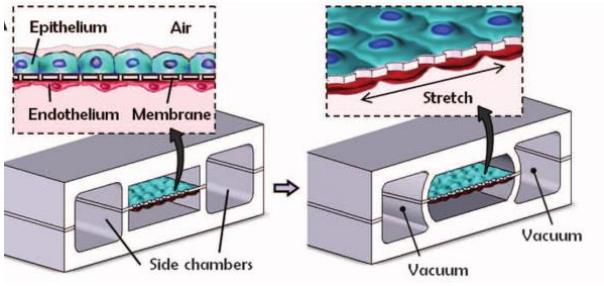


Figure 1.2: Lung-on-Chip[12]

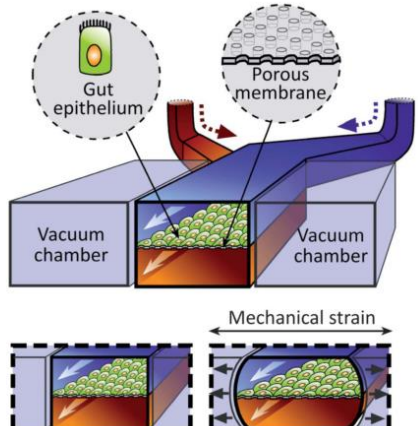


Figure 1.3: Gut-on-Chip[9]

After creating microsystems that represented human physiology, OOC have been used for studying disease mechanisms. For example, after micro-engineering a Lung-on-Chip Huh *et al.* used a similar chip for a pulmonary edema disease model [18]. In addition, multiple models of Cancer-on-Chip are being developed[19–21].
Ultimately, human physiology is a manifestation of interactions between different organs. It is particularly interesting in drug R&D to study not only efficacy, but absorption, distribution, metabolism, excretion and toxicity (ADMET) as well as efficacy. A 'human-on-chip' or 'Body-on-Chip', in which every organ necessary for drug R&D is integrated within a single device, has not yet been created. Nevertheless, in 2015 Maschmeyer et al. developed a Four-organ-Chip with four tissue culture compartments for intestine, liver, skin, and kidney[22].

1.2. Polydimethylsiloxane in Organs-on-Chips

The materials commercially available for porous membranes are often not compatible with OOC applications. These porous membranes are often made from polycarbonate (PC) or polyethylene terephthalate (PET) and they have been used in devices such as a blood brain barrier on chip[15] and a Four-organ-chip which combines an intestine, liver, skin and kidney in one device[22]. Another material that can be used to create porous membranes is PDMS. This is a polymer with a silicon backbone with the following structure: $CH_3[Si(CH_3)_2O]nSi(CH_3)_3$ with 'n' being the number of repeating monomers. It is optically transparent, bio-compatible and it has a high permeability to oxygen[23]. PC and PET lack a low Young's modulus, necessary for elasticity, and therefore are not suitable for mechanical deformation[24]. In contrast to PC and PET, PDMS has an elasticity that is more suitable for OOC devices because the membranes need to undergo mechanical deformation[10]. Due to the advantages of PDMS, many OOC devices with dynamic and mechanical effects have been created, such as the lung-on-chip[12], heart-on-chip[14] and gut-on-chip[9]. Next to the mechanical effects, the pore size and porosity of the membrane influences cell behavior[25–28]. In PC and PET, exerting control over the pores is a complex process[1]. Improved control over pore size and porosity of the membranes is achieved when PDMS is used. Next to their application for OOCs, PDMS membranes have proved to function as filters to separate white blood cells or circulating tumor cells from blood[29–31].

1.3. The fabrication of porous PDMS membranes

The most conventional method to create PDMS membranes is soft lithography and replica molding[32]. This method is depicted in Figure 1.4.

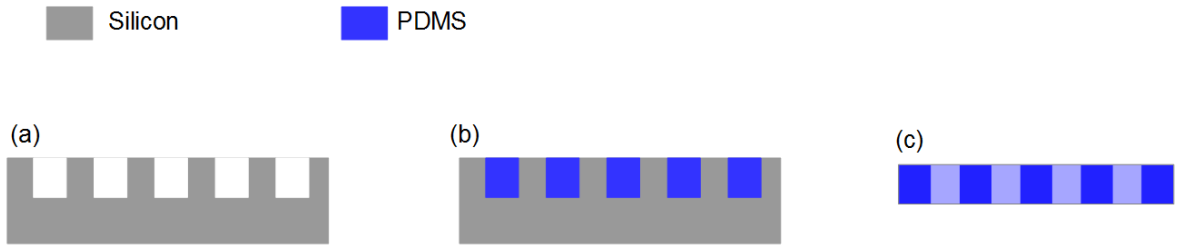


Figure 1.4: Soft lithography for PMDS membranes. a) A silicon master mold is patterned by conventional lithography. b) Uncured PDMS is poured on the mold and cured. c) The membrane is peeled off from the master mold

This method is low-cost fast and easy to learn[33,34]. However, it requires a number of manual steps which hinders the commercialization of the devices[35,36]. Furthermore, the porosity of the membrane cannot be fine-tuned with this process. In addition, the mold can break or the membrane can tear when the membrane is manually removed from the mold[37].

In order to create porous PDMS membranes it is also possible to use micro-electro-mechanical systems (MEMS)-based fabrication technologies, also referred to as photo-lithography. Quirós-Solano *et al.* used this method to create a PDMS membrane with a porosity of 65%, and the possibility to adjust the pore size and pore to pore distance[1]. This method consisted of photo-lithography steps followed by dry etching of the PDMS. This process will be discussed in depth in the next chapter. It is important to consider the thermal budget of this process since PDMS has a high coefficient of thermal expansion.

Consequently, the photoresist layer on top of the PDMS can crack and fracture[38]. Furthermore, a hard metal mask is needed since photo-resist de-wets from the PDMS surface and this can create an uneven surface topology[38]. A drawback of MEMS-based fabrication is that it is less suitable for rapid and low-cost fabrication due to the necessary facilities to produce the membranes.

1.4. Highly porous PDMS membranes

In unpublished work, Quirós-Solano *et al.* were able to produce a scaffold by creating an array of lateral gaps between the vertical pores using a similar method. Figure 1.5 shows this scaffold. This scaffold may be useful in OOC because of its higher porosity and the reduction in PDMS material. In order to obtain these scaffolds, the pores were brought in close proximity during the design phase. Moreover, during the fabrication the etching time was extended. This method allowed to tune the dimensions of the gaps by changing the etching time. However, this results in a complete etching of the layer underneath the PDMS. Therefore, this work aims at investigating other parameters that can be used to tune the dimensions of the gaps and the porosity of the scaffold.

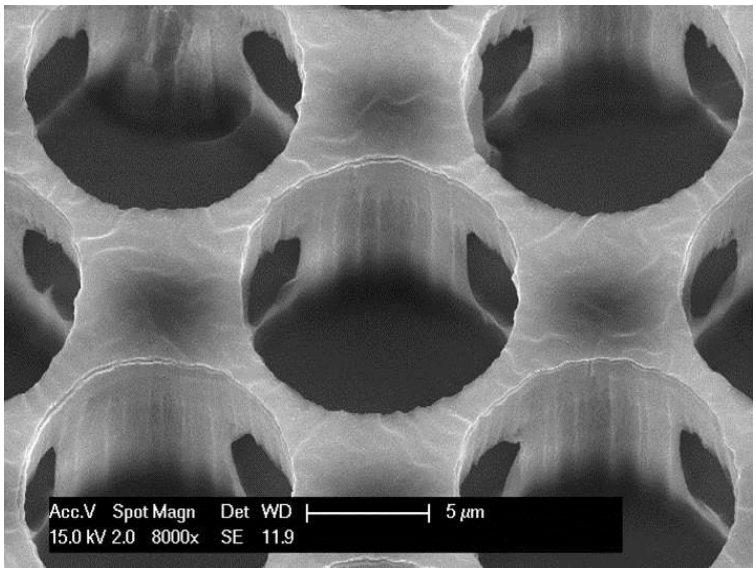


Figure 1.5: SEM image of a scaffold with 8 µm wide holes which are 1 µm apart from each other. This membrane was fabricated by Quirós-Solano et al.

In addition to the fabrication of the scaffold, Quirós-Solano *et al.* developed a process to transfer PDMS membranes with greater precision than the standard method. They employed a sacrificial layer of poly acrylic acid (PAA) between the silicon substrate and the PDMS membrane. With this fabrication method they were able to create thin (<10 µm) transferrable membranes[39]. However, thicker membranes could not be fabricated with their process flow.

1.5. Technical background

Etching allows to selectively remove a material from a substrate, such as a silicon wafer. During this process, part of the wafer is protected by a masking layer so that only material is removed in the unprotected parts. This process is employed to create the pores of the membrane presented by Quirós-Solano *et al.* Dry etching (also known as plasma etching) employs plasma to remove the material, while in wet etching a fluid is used. In this report wet etching is not going to be discussed since controlled wet etching of PDMS is nearly impossible. Plasma etching takes place within a plasma etcher. This machine contains a chamber where a gas-mixture is introduced via an inlet. The electrons of the molecules in this gas are accelerated through a switching electrical field. This electrical field is generated by a radio frequency generator. When the electron energy reaches a certain value, the molecules in the gas are dissociated and a plasma is created. The plasma consists of ions, free radicals, electrons and neutrals.

Two types of plasma etchers are most commonly used for PDMS etching: the inductively coupled plasma (ICP) etcher and the capacitively coupled plasma (CCP) etcher. In both types, plasma ions are bombarding and sputtering the surface of the substrate (which is the PDMS membrane in our case), while radicals in the plasma chemically etch the surface. The main difference between CCP and ICP etchers is that in a CCP reactor the plasma is created within two parallel plates while in an ICP reactor the plasma is created by inductive coupling. The voltage difference between the plate and the plasma depends on the plasma power and the pressure in the CCP reactor. With an ICP reactor the voltage is between the plasma and the chuck and it can be tuned separately with a bias power generator. The result is that with a CCP reactor, less control can be exerted over the process compared to ICP reactors[40]. Therefore, an ICP etcher is more favorable than CCP etcher for this study. During the work of Quirós-Solano *et al.*[1] an ICP reactor was employed. Therefore, we restrict this report to dry etching performed in an ICP reactor. In the following section we specifically discuss the process parameters related to the dry etching of PDMS.

1.5.1. ICP etching

Figure 1.6 shows an example of a plasma chamber. The central part of the reactor is the chamber where the plasma is contained, and the wafer is located. The inlet and outlet

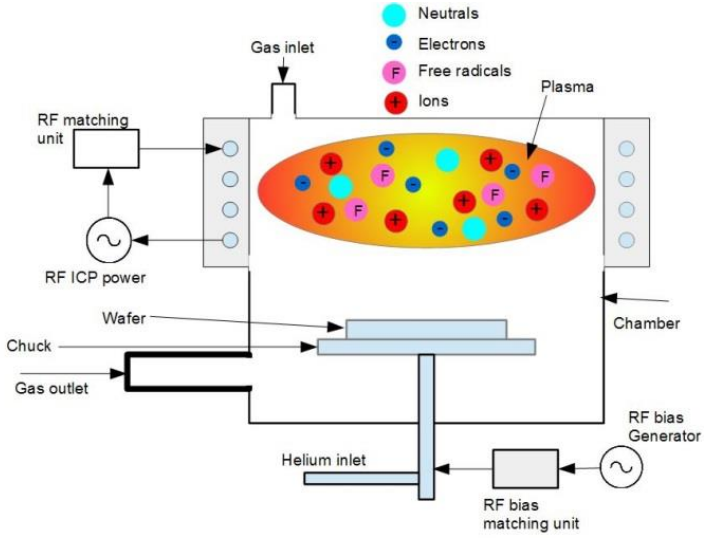


Figure 1.6: ICP Plasma etcher

ports and their valves regulate the gas flow and the chamber pressure. An electrostatic chuck is used to constrain the location of the wafer. This chuck is cooled by a cooling liquid

and helium is used to enhance the thermal contact between the cooled chuck and the wafer. Furthermore, a bias power can be applied to the chuck.
The radio frequency (RF) power generator is connected to a RF antenna, which generates the plasma via inductive coupling. Inductive coupling works as follows: the power generator and antenna produce a magnetic field inside of the chamber, which in turn creates an electrical field in the chamber. This electrical field energizes the electrons. As soon as the electrons contain sufficient energy, the highly energized electrons break the bonds of the molecules of the process gasses, and the molecules are disassociated. A fraction of the total amount of molecules breaks down into ions and free radicals. Thus, there are four species within the plasma: neutrals, ions, electrons and radicals. Ions and radicals contribute to the etching process and their contribution is given below.
Ions are charged molecules. They are accelerated towards the wafer surface due to the potential between the plasma sheet and the wafer surface. When the ion energy is high enough they sputter material at the surface. However, if the ion energy is too low, the ions will only activate the surface, which lowers the energy required for chemical reactions to take place. The ions have a high directionality because they follow the electrical field between the plasma and the chuck. The potential can be controlled with the bias power of the chuck[41]. Increasing the bias power, increases the directionality of the ions and the ion energy. An increase in the directionality results in an increased vertical etch rate. An increase in ion energy results in a higher vertical and lateral etch rate. Therefore, the etch will be more isotropic with a higher bias power[42–44].
The pressure in the chamber is another factor that influences the ion directionality and ion energy, but in an opposite manner as compared to bias power. Increasing pressure causes the ions to collide more with other particles in the plasma upon which they lose energy. The reduction in energy will decrease both etch rates. Furthermore, their direction changes due to the collisions and the etch will become more isotropic[42].
The radicals are uncharged species that chemically etch the wafer substrate by reacting with the molecules on the surface. They are moving isotropic as they are not bounded by the electrical field between the plasma and the wafer. Radical direction is determined by the random collisions with other particles in the plasma. The chemical etch rates of the radicals depends on the temperature of the substrate and the activation energy necessary to start the reaction. A lower activation energy increases the chemical etch rate. Now, it is clear that etching is a process of ion bombardment and chemical etching with radicals. When both processes are combined, the etch process is faster than the summation of both processes separately[45].
The ICP power that is needed to fully disassociate the gas depends on the gas flow. With an increase in gas flow, the ICP power has to increase in order to keep the gas fully disassociated[46]. For a fixed gas flow, the etch rate does not increase with increasing ICP power after the ICP power is sufficient to disassociate[47]. An increase in gas flow also increases the removal of volatile reaction products. However, there is an optimum for gas flow because with a further increase in gas flow the residence time of the reactive species will be lower than the reaction time. Residence time is the time between a molecule entering and leaving the chamber, and it depends on the gas flow and pressure.

1.5.2. PDMS etching

In this section, we explain the specifications of ICP etching of PDMS materials. Previous work concerning plasma etching of PDMS has been performed by multiple research groups[40,48–56]. Although they used different reactor systems to study the etching process of PDMS, all of them used a gas mixture which contained molecules (mainly CF_4 or SF_6 gasses) to build a Fluorine based plasma. Fluorine is a radical that can react with the silicon back bone in the PDMS. This is the chemical reaction that induces PDMS etching[49]. Unfortunately, when the gas mixtures consist of CF_4, fluorocarbon polymers can redeposit on the sidewalls[50,51]. This may influence the etch rate and sidewall roughness. In addition

to CF_4 and SF_6, oxygen (O_2) is often added because it can increase the fluorine concentration in the plasma[57].

Additionally, the mask that was used is often made of aluminum. Aluminum does not etch in a Fluorine plasma [58]. However, it is sensitive to ion bombardment. When an ion impacts the aluminum, aluminum molecules are redeposited on the substrate. This can create micro-masking which can increase the surface roughness of a PDMS etch [48,51–53].

1.5.3. Wafer temperature

Domanski *et al.*[52] studied the effect of temperature on the etch rate of PDMS, and they found a linear relationship between the vertical etch rate and substrate temperature for temperatures between 10°C and 70°C. When the PDMS reaches a temperature over 200°C it starts to decompose[59].
To know the wafer temperature, it is important to know how the substrate is heated and cooled. The cooling of the wafer is done with the cooling liquid of the chuck and the effectiveness of the cooling is depended on the thermal contact between the wafer and the chuck [60]. Heating of the wafer happens when the radicals are reacting with the substrate[61]. Especially the reaction between Si and F, which creates SiF_4, is highly exothermic [62]

In summary, the ions and radicals are the most contributing plasma species in ICP etching. Their contribution can be controlled mainly by the bias power, the chamber pressure and the chuck temperature. Increase of the bias power results in a more isotropic etch and increased vertical and lateral etch rates. Increase in pressure also results in a more isotropic etch, but with decreased etch rates. Lastly, the wafer temperature is found to increase both vertical and lateral etch rates.

1.6. Thesis contribution

The general goal of this thesis research is to improve upon the work Quirós-Solano *et al.* In their work, they created a thin transferrable membrane with lateral gaps between the vertical pores. The porosity of this scaffold was tuned by changing the process time.
This research is focused on two main topics:

1. To understand the mechanism that creates the lateral gaps between the pores of the scaffold and to understand the contribution of bias power, chamber pressure and chuck temperature to that mechanism in order to tune the process.
2. To create thick transferrable PDMS membranes for the use of cell research.

1.7. Thesis outline

The remainder of the thesis is structured as follows: In Chapter 2, simulations are performed. In the first simulation the effect of temperature on the shape of the pores is studied. In the second simulation the temperature of the wafer during etching is estimated. In the last part of Chapter 2, the wafer temperature is empirically determined. Chapter 3 is focused on quantifying the relationship between the process parameters and the vertical and lateral etch rates. It is separated into three sections. Replicating the scaffold, quantifying the relationships and tuning of the porosity of the scaffold. In Chapter 4, the process flow of Quirós-Solano *et al.* is adapted to create thick transferrable PDMS membranes that were used for cell research. Finally, in Chapter 5, the results and conclusions of the different chapters are summarized and recommendations for future work are given.

2. Wafer Temperature

This chapter investigates the effect of the temperature on PDMS structures during PDMS etching. In Chapter 1, temperature was included in the list of parameters that can influence the etch rate. Section 2.1 describes two simulations. The first simulation was performed to test if a pure anisotropic etch could create the lateral gaps between the walls. In the second simulation the temperature of the PDMS structures was simulated. This simulation was performed to validate the results of the first simulation and to estimate the wafer temperature during etching. In Section 2.2, the temperature of the PDMS structures was empirically determined to validate the results of the second simulation.

2.1. Simulations

The simulations were performed with a multiphysics simulation tool (COMSOL Multiphysics). COMSOL is computer software that forms a bridge between the thermal and mechanical domain using finite element analysis. For example, if an object is heated, it will expand due to the thermal expansion. If the coefficient of thermal expansion is set to zero, the object will not expand in the simulation and will not behave like the physical device. The simulation is bound by the conditions and relations the user sets.

2.1.1. Anisotropic etching

The goal of the first simulation was to understand the effect of a pure anisotropic etch on the rounding of the pores. This effect is presented in Figure 2.1**Fout! Verwijzingsbron niet gevonden.**. During etching, the wafer temperature increases, and the wall of the pores expand due to thermal expansion. If they expand beyond the aluminum mask (Figure 2.1b), the walls are etched (Figure 2.1c). After cooling, the walls will contract and by having lost material, the walls will be concave instead of straight (Figure 2.1d). This simulation was performed to examine if the thermal expansion is high enough to be a potential cause for the formation of the lateral gaps between the pores. The temperature was set at 207°C to maximize the visibility of this effect. Furthermore, 207°C is close to the possible upper limit of the temperature before PDMS starts to decompose[59].

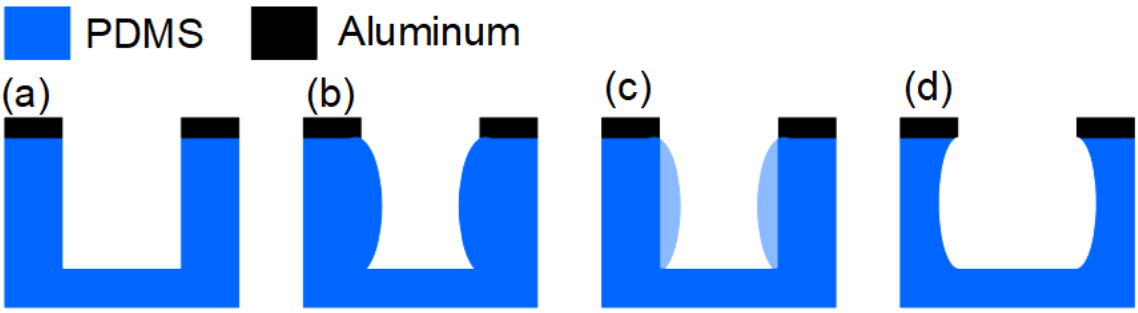


Figure 2.1: A single pore that is being etched. A) The pore at room temperature. B) The pore at an elevated temperature. The walls are expanding beyond aluminium mask. C) The material that is extended beyond the mask is etched away by the plasma. D) After cooling down, the walls will contract. Due to the removal of the material of the walls, the walls will be concave. The shape of the pore is similar to pores that have been etched isotropically.

Model creation

Due to the complexity of this simulation, a 2D-model was used instead of a 3D-model. Furthermore, only a part of the wafer was simulated. The 2D-model consisted of a 90 μm-wide and 20 μm-high silicon base with a 10 μm-thick silicon-oxide layer on top. Above the silicon-oxide layer a 10 μm-thick PDMS layer was placed. The top layer consisted of a 500

nm-thick aluminum layer. The aluminum layer and the PDMS layer contained 8 pores, which were 8 μm wide. The pore to pore distance was 1 μm.

The simulation was a time dependent study which was simulated for a total of 14 seconds. During the simulation, the mesh was adjusted to simulate the removal of the PDMS due to etching. The simulation conditions were defined and performed as follows:

- The temperature of the model was 27°C at the beginning of the etch and increased to 207°C within 8 seconds. The model was then cooled down 27°C within 4 seconds.
- The pores were etched away with a speed of 0.82 μm/sec in the vertical direction for the first 8 seconds.
- The expansion of the side walls of the pores caused by the thermal expansion was cancelled out by the reduction in mesh thickness.
- The bottom line of the silicon substrate was set as a fixed point in space.

Results of the anisotropic etch simulation

By heating the sample to 207°C, the thermal expansion of the sidewalls in the lateral direction was 0.09 μm for both sides. Thus, a total of 0.18 μm out of 1 μm was etched away. In Figure 2.2, the thermal expansion in the lateral direction is visible. The walls are still 1 μm wide, because they were expanded with 0.18 μm, while the mesh was reduced by 0.18 μm to keep the wall thickness equal to 1 μm. The material of the wall that extended beyond 1 μm was simulated as being etched away.

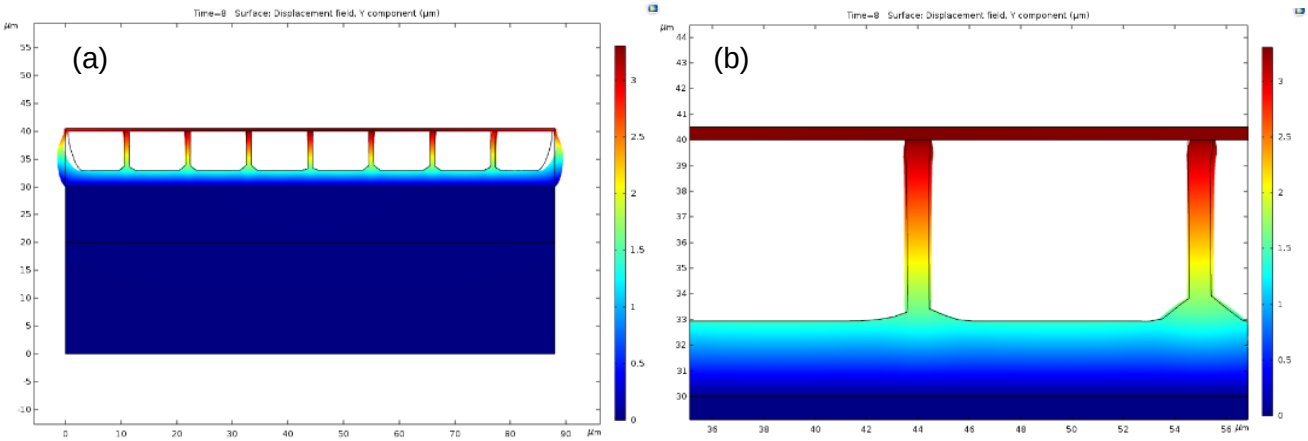


Figure 2.2 A) Overview of the model after simulations. B) Close up of a wall on a single pore with a temperature of 207°C. The thermal expansion in the lateral direction is 0.09 micron. This expansion is cancelled out by the reduction in sidewall thickness. The expansion in the vertical direction is 3.5 micron

Conclusion

The thermal expansion in the lateral direction is below 0.1 μm when the temperature is raised to 207°C. Thus, if the wafer reaches a temperature of 207°C during etching, the pores will have some lateral removal of material even though the etch is purely anisotropic. This reduction in sidewall thickness is considered to be too small to be responsible for the lateral gaps between the pores.

2.1.2. Wafer temperature estimation

The second simulation was performed to estimate the temperature of a wafer during etching. The simulation was simplified and only the wafer temperature was simulated and not the etching process. The simulation included cooling of the chuck and the heat flux due to etching of PDMS as they determine the temperature.

In this simulation a 3D-model was used and only a small section of the total wafer was modeled. The model is presented in Figure 2.3.

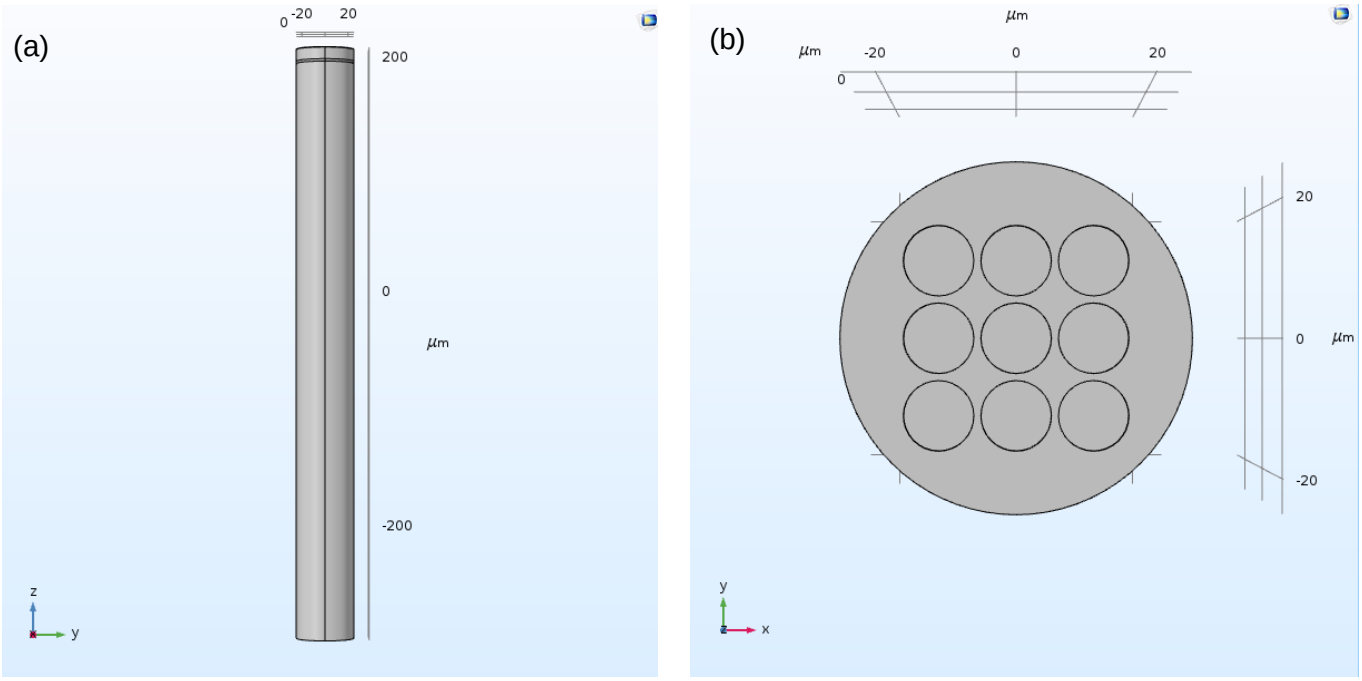


Figure 2.3: Side view (a) and top view (b) of the model. The chuck is located at the bottom of the silicon rod, however, the chuck is not modelled. The membrane is located at the top of the silicon rod. In the top view, the aluminum mask is visible together with the array of pores. On the bottom of the pores a heat flux of 80.000 W/m^2 is present.

The first layer was a silicon rod with a radius of 20 μm and a length of 500 μm. Directly on top of the silicon rod was a silicon oxide layer with a thickness of 2 μm was modeled. The silicon oxide layer is covered with a PDMS layer with a thickness of 10 μm. This included 9 pores with a depth of 7 μm in a 3 by 3 array with a 9 μm center to center spacing. The top layer consisted of a 400 nm-thick aluminum layer with the same 9 pores. Figure 2.3 shows the side view and the top view of the model.

A stationary study was performed to determine the temperature at equilibrium. It was assumed that this equilibrium could be reached during etching. The boundary conditions and the initial values were defined as follows:

- The bottom of the silicon rod was kept at a constant 27°C, which was the chuck temperature.
- To eliminate edge effects, the heat flux among the shaft of the rod was set at zero.
- Convex airflow was present on the top of the wafer with a sphere of air of 0.5 meter with a pressure of 5 mTorr and a temperature of 27°C. This simulates the cooling with convex flow.
- The heat flux on the bottom surface of the pores in the PDMS was set to 80.000 W/m^2. This value was based on the work of Pichon *et al* [61].

Results

The result of the simulation is presented in Figure 2.4. The highest temperature was 36°C and it was measured in the center of the pores. Due to the high thermal conductivity of silicon, the temperature of silicon-oxide is only 3°C higher than that of the chuck.

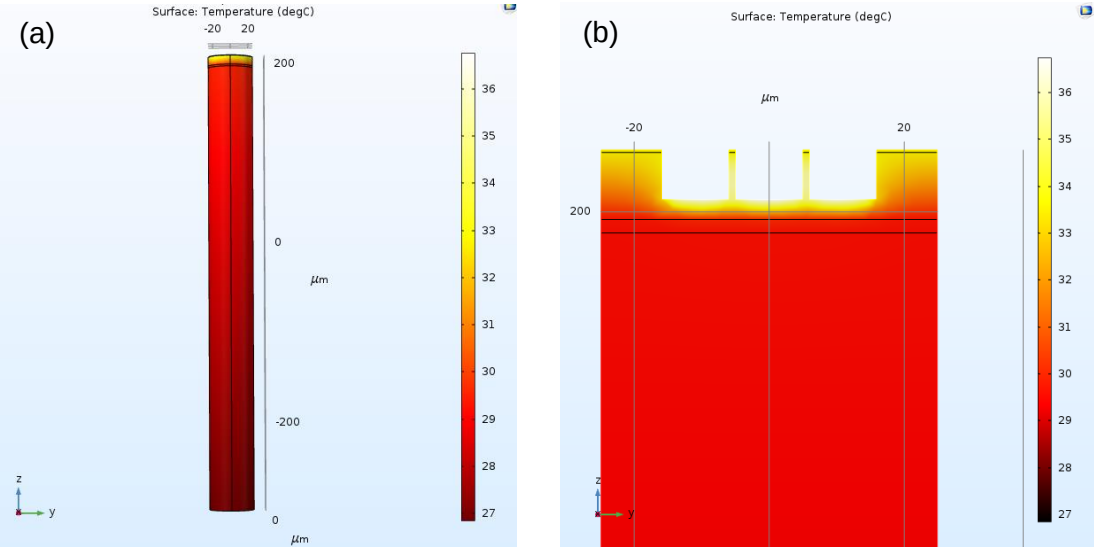


Figure 2.4: Results of the COMSOL simulation. A) side view of the silicon rod with the membrane on top. B) Cross section of the top quarter of the silicon rod. The maximum temperature is 36°C in the PDMS membranes.

Conclusion

The maximum temperature reached was 36°C, which is an increase of 9°C with respect to the initial temperature. The simulated temperature of 36°C was lower than the temperature set at the first simulation which was 207°C. Therefore, it is unlikely that the process described in the anisotropic etch simulation is indeed what was observed by Quirós-Solano *et al.*

However, the temperature of the wafer can influence the etch rate, as was noted in Chapter 1. Thus, this increase in temperature may increase the etch rate, especially considering the strong linear relationship between temperature and etch rate[52]. Furthermore, it can be seen that the chuck temperature has a great influence on the wafer temperature if a good thermal contact is made.

2.2. Wafer Temperature Measurements

To validate the simulations, the wafer temperature was also empirically determined. A temperature measurement setup was developed that can measure the temperature of the wafer during etching. This setup and the results of the tests are presented below.

2.2.1. Method

A temperature strip was placed upon a wafer and was fixed with Kapton tape as seen in Figure 2.5. This wafer was then etched with the plasma etcher. During etching, the wafer together with the temperature strip heated up. After etching, the maximum temperature that the strip reached could be read out. Unfortunately, the time dependency of the temperature was lost with this method.

Set up

The test was done on two bare silicon wafers and on four wafers with a PDMS layer. Three of the PDMS wafers were bare wafers with a 17 μm thick PDMS layer, and the fourth wafer had a high porosity mask as used in the simulations. The thickness of the bare PDMS wafers was chosen such that they could be etched for a sufficient amount of time. To save time in fabrication, some of the wafers were used more than once. The temperature strips were provided by Omega and they had a temperature range of 40°C to 83°C with steps ranging from 3°C to 6°C. The strips were 18 mm wide and 54 mm long. They were placed at the center of the wafer and then secured with Kapton tape as shown in Figure 2.5.

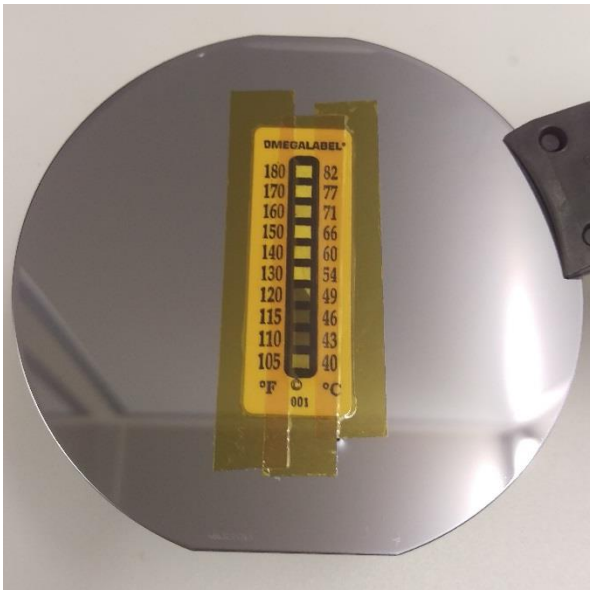


Figure 2.5: Bare silicon wafer with a temperature strip attached after etching. The maximum temperature the strip reached was 49°C.

Etch recipes

The wafer temperature was measured during etching with a control recipe. The bias power of the control recipe was 10 W and the chuck temperature was 25°C.In addition, the wafer temperature was also measured for recipes with different bias powers and different chuck temperatures. These two parameters were selected as they can influence the wafer temperature as seen in Chapter 1.

2.2.2. Results

Table 2.1 and

Table 2.2 summarizes the results of the temperature tests.
The highest temperature reached for a bare silicon wafer was 49°C when it was etched with 50 W of bias power for 10 min. The highest temperature reached for a bare PDMS wafer was 46°C when it was etched for 25 min with 50 W of bias power. The temperature of the PDMS wafer with an aluminum mask did not increase above 40°C.

Table 2.1 The results of the temperature test for the bare silicon wafers

Top layer	Wafer number	Bias power (W)	Chuck temperature (°C)	Time (min)	Temperature (°C)
Silicon	1	10	25	10	43
Silicon	1	50	25	10	49
Silicon	2	50	25	25	46

Table 2.2: The results of the temperature test for the PDMS wafers

Top layer	Wafer number	Bias power (W)	Chuck temperature (°C)	Time (min)	Temperature (°C)
PDMS	1	10	25	10	40
PDMS	1	10	25	25	40
PDMS	2	50	10	10	40
PDMS	2	50	25	10	43-46
PDMS	3	50	25	25	43
PDMS	4	50	25	25	40

2.2.3. Discussion

A difference between the temperature of the silicon and PDMS was noticed when they were etched with the same recipe. This difference can be explained by the fact that silicon has a higher thermal conduction compared to PDMS. Thus, the strip is representing the temperature better on a silicon wafer than on a PDMS wafer. Another explanation is that the etch rate of silicon is higher than the etch rate of PDMS for this recipe and a higher etch rate indicates that more exothermal reactions have taken place which can increase the wafer temperature.

An unexpected result occurred in the test. The temperature of the silicon wafer that was etched for 25 min was lower than the temperature of the silicon wafer that was etched for 10 min. This discrepancy may be due to differences between the two wafers in thermal contact of the strip to the wafer, surface area of the Kapton tape and thermal contact between the wafer and the chuck.

2.2.4. Conclusion

From Table 2.1 and

Table 2.2 it can be concluded that with an increase in bias power the temperature rises. The maximum temperature is 49°C which is reached by using the recipe with the highest bias power. The effect of increasing bias power is twofold: first, it raises the amount of sputtering, which will increase the etch rate. Secondly, the increase of sputtering leads to a rise in temperature. Subsequently, a high temperature raises the rate of the chemical reactions which will increase the etch rate.

Another conclusion is that temperature of the chuck influences the temperature of the strip. When the chuck temperature is 10°C, the wafer temperature does not reach 40°C. This shows that thermal contact between the chuck and the wafer is good. Furthermore, an increase in time does not influence the maximum temperature indicating that the

equilibrium is reached within the first 10 minutes of etching. With an aluminum mask, the wafer temperature is reduced, resulting in a lower etch rate.
The temperature of the PDMS wafer with the aluminum mask was below 40°C. The temperature during simulation was 36°C, thus it seems that the simulation was accurate.

Recommendations for future work

An improvement to the test would be to reduce the thermal loading of the strips by using smaller strips. Furthermore, more locations on the wafer could be tested if the strips are smaller. In addition, strips with a temperature range extending below 40°C are recommended as the lowest temperature reached in the test was below 40°C.

3. Influence of process parameters on the etch isotropicity

The goal of this Chapter is to understand the mechanism behind the creation of the scaffold-like membrane of Quirós-Solano *et al.*
The proposed research objectives were:

1. Replicating the scaffold.

The first objective was to replicate the membrane and investigate whether it is possible to replicate it by varying process parameters, based on the results of the literature study.

2. Finding the parameters related to etch isotropicity

The second objective was to find the relationship between the process parameters and the lateral and vertical etch rates.

3. Tuning the porosity of the membrane

The last objective was to use the obtained knowledge to tune the porosity of the membrane and to identify an ideal combination of process parameters for the desired porosity.
This chapter can be divided in four main sections: The first section presents the methodology where a general overview of the process flow is provided together with the adaptions that were made during the experiments.
The last three sections are focusing on different research objectives. Each of them presents its research goal, the difference in method and the results.

3.1. Methodology

For every research objective, a set of experiments was conducted. In these experiments the membranes were created, and the process parameters were tuned. The experiments were performed in the Else Kooi Lab Clean Room in Delft.
The process flow to create the membranes was based on the process flow of Quirós-Solano *et al.*, and standard clean room processes such as photo-lithography and etching. The process flow to make the membranes is similar for the three research objectives, hence a summary is presented in Subsection 3.2.1. There were some limitations in the etching process and those limitations are presented in Subsection 3.2.2.

Base process flow

A summary of the steps is depicted in the list below.

- Deposition of silicon oxide[1]
- Backside coating of the wafer with resist.
- Mixing of PDMS and top side wafer coating with PDMS by spin coating
- Curing of PDMS in the oven
- Backside wafer cleaning with acetone
- Aluminum depositing by evaporation
- Lithography
- Etching of aluminum mask
- Etching of PDMS
- Removing aluminum by a PES bath
- Imaging of the wafer with a SEM

[1] In the process flow of Quiros *et al.* they used a sacrificial layer of PAA. In this work it is replaced with silicon oxide layer which served as an etch stop layer.

3.1.1. Adaptions

Before the experiments of the second research question could be started, the lithography step had to be adapted because the pores were not completely open after the PR development. The first step in the lithography process is the spin coating of resist. Subsequently, the wafer is exposed through the mask with a contact aligner. The last steps include baking of the wafer and developing the resist. The developing recipe was the single puddle recipe for the first set of experiments. The results with that recipe are shown in Figure 3.1a. During the experiments this recipe became invalid and the pores were not opened completely after developing (Figure 3.1b). Therefore, the development recipe was changed to double puddle. This resulted in pores that were completely open again as shown in Figure 3.1c

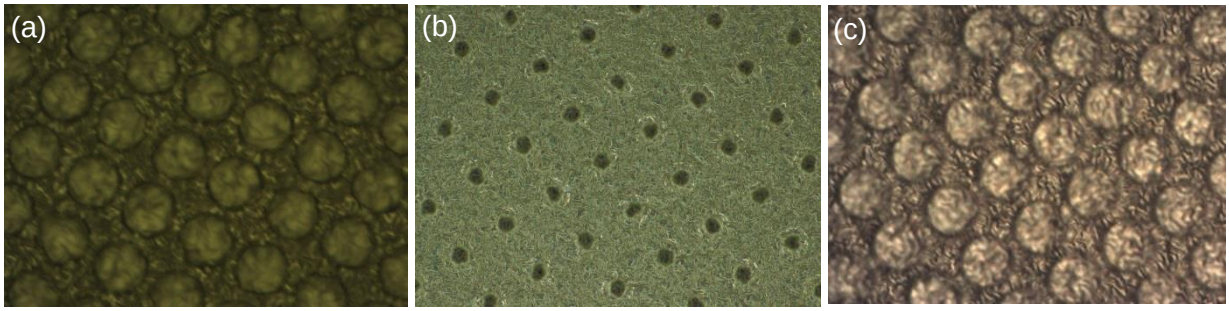


Figure 3.1: A) Image of the pores after developing for the first research question. In this figure the pores are open. B) Image of the pores after developing for the second research question. Taken at a lower magnification. In this figure the pores are not completely open. C) Image of the pores after developing for the third research question. Here the pores are open again after changing the developing recipe.

It remains unclear why the pores did not open completely after development. Potential causes for this problem are listed below.
The conditions inside the developer tool might have changed. The humidity can swing between 48% and 52%. However, this swing in humidity was still within the recommended range, and should therefore not have caused this underdevelopment of the pores.
Another cause of underdeveloped pores could be the thickness of the resist. When measured, the resist layer on top of the aluminum layer was 2.2 μm instead of 1.5 μm. However, the difference in thickness might be due to the difference in surface properties of the aluminum layer since with a bare silicon wafer the thickness of the resist layer was indeed 1.5 μm, thus the recipe itself did not change.
Other potential causes are differences in thermal contact of the hot plates, differences in energy or focus of the manual contact aligner or a change in the developer recipe. However, none of these potential causes were tested. Instead, the developer recipe was changed to a recipe with a longer developing time. This change in recipe had the desired outcome and the pores were fully open again.

3.1.2. Limitations in the etching process

As the ICP tool was rather old and malfunctioning at times, some care had to be taken while using it. Some challenges arose during the conduction of the different experiments, which made exact replication of the porous membranes challenging. The following sections represent several of the issues with the tool, and the proposed way-to-deal with them the best way possible.

1. Reflected power

A major issue with the machine for the first two set of experiments was a broken capacitor, which is used to compensate for the inductive behavior of the bias power generator. With the broken capacitor some of the bias power was reflected back in to the generator. With

a bias power of 10 W this reflected power was displayed as zero. With 30 W the reflected power was around 15 W, and with 50 W the reflected power was around 29 W.
Nevertheless, even when a new capacitor was installed, the issue of reflection power was still in place with high power recipes used in combination with high pressure. The effects of the reflected power on the process was that the etch rates were severely reduced. Consequently, only an estimation could be made of the actual bias power.
Due to the reflected bias power, the aluminum etch recipe that was used, was unable to completely etch the aluminum mask. The incomplete etch created aluminum micro-masks that influenced the surface roughness of the pores [63].

2. Cleaning of the chamber every few months

The etching tool is not only used to etch PDMS and other polymers, but also silicon and metals as well. During etching, etch residues were deposited on the reactor walls. Every few months, the reactor walls were cleaned, and the residues were removed. After cleaning, it took around a week to stabilize the machine, while new residues were deposited on the reactor walls. During the stabilizing period, the machine could not be used for experiments as that it could affect the experiments as seen in Figure 3.2. In this Figure, two membranes are visible, which have been etched with the same recipe, but at a different moment in time.

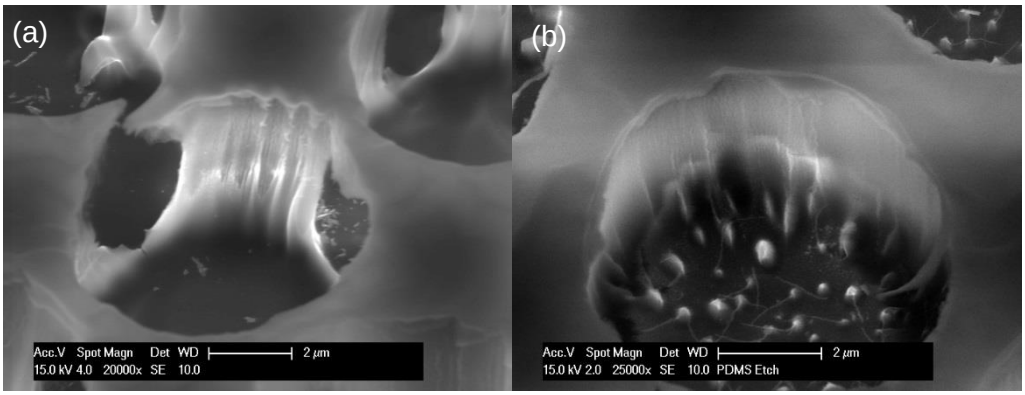


Figure 3.2: A) A close up image of a pore. This wafer was etched for 16 min with the standard recipe. B) A close-up image of a pore. This wafer was etched for the same time with the same recipe two weeks later. There is a difference in surface roughness and there are no lateral gaps in the second image.

3. Chuck cooling

At the end of the first experiments the machine was unable to decrease the pressure in the load lock when the chuck was cooled down to a temperature of 10°C. The load lock is the location where the wafers are stored in the machine before they are processed.
A solution would be to first decrease the pressure in the load lock and thereafter decrease the chuck temperature. However, the machine blocked when this procedure was done in an incorrect manner, resulting into that the machine was unavailable
Furthermore, this solution did not result in an instant temperature decrease to 10°C. Instead, the temperature decreased from 13°C to 10°C over the course of the first few minutes of the process time.
If all the experiments were conducted according the proposed solution, it is expected that there would not have been a significant influence on the experiments.

4. Pressure

In the second research question the machine was unable to reach pressure below 6 mTorr with a gas flow of 45 sccm. Therefore, the solution was to decrease the gas flow with 20%

for the affected recipes. A possible cause for this issue is that the layer of re-deposited etch-residues was too thick.
In order to test whether a reduction in gas flow had influence on the etch result, some etches were performed with a reduction of 50%. Here, it was indeed visible that reduction in gas flow influenced the etch result. Yet, it was still unclear whether this influence would be significant in a reduction of only 20%.

5. Start-up time with each process

In the first minute of etching the chamber is still stabilizing. During stabilization of the chamber the etch rate is lower than the etch rate when the system is stabilized. Therefore, it is expected that there will be a difference in etch rate when a wafer is etched in a single run or in two separate runs.

3.2. Replicating the scaffold

The first research objective was to repeat the fabrication of the scaffold. Moreover, it was investigated whether the results could be replicated when the process parameter are varied.

3.2.1. Adaption to the process flow

The base process flow is used as described earlier without any adaptations. The parameters of the etching process were changed in order to investigate the effects of these parameters on the formation of the pores.
The following three etching process parameters were varied and the corresponding recipe with which the membrane was etched, is listed in Table 3.1.

1. Bias power
2. Chamber pressure
3. Chuck temperature

Table 3.1: Etch recipes for the first research question

Recipe number	Recipe name	Bias power (W)	Chamber pressure (mTorr)	Chuck temperature (°C)
1	Control	10	5	25
2	High power	50	5	25
3	High pressure	10	50	25
4	Low temperature	10	5	10
5	High power, low temperature	50	5	10

As a starting point the control recipe was set a bias power of 10 W, chamber pressure of 5 mTorr and a chuck temperature of 25°C. Recipe nr. 2 until 4 are combinations between the standard parameter values and one of the parameters set to its maximum value (according to clean room allowance), or minimum value (in case of chuck temperature). Recipe nr. 5 is a combination of high bias power and lower chuck temperature. This recipe was chosen as Chapter 2 of this study showed that the chuck temperature influences the wafer temperature when the wafer is etched with a higher bias power.

The following hypotheses were made for the different recipes:

1. Recipe nr. 2: It is expected that a higher bias power leads to higher vertical and lateral etch rates compared to the control recipe;
2. Recipe nr. 3: It is expected that a higher pressure leads to higher lateral etch rates and lower vertical etch rates to compared to the control recipe;

3. Recipe nr. 4: It is expected that a lower temperature should decrease the etch rates compared to the control recipe;
4. Recipe nr. 5: It is expected that the use of low temperature will decrease the effects on the use of high bias power. Hence, the vertical etch rates are expected to be lower than for recipe nr. 2.

Process time

The process time was based on the time of Quirós-Solano *et al.* to etch through the PDMS and on the extra time needed to achieve the gaps between the pores. The times were respectively 16 and 26 min. However, the process time was extended as it was not possible to etch through the membrane within 26 min. The time to etch completely through the PDMS layer differed for each recipe.

3.2.2. Results

The images (Figure 3.3) were taken when the PDMS was completely etched through. The results of the time needed for breakthrough are presented below in table 3.2.

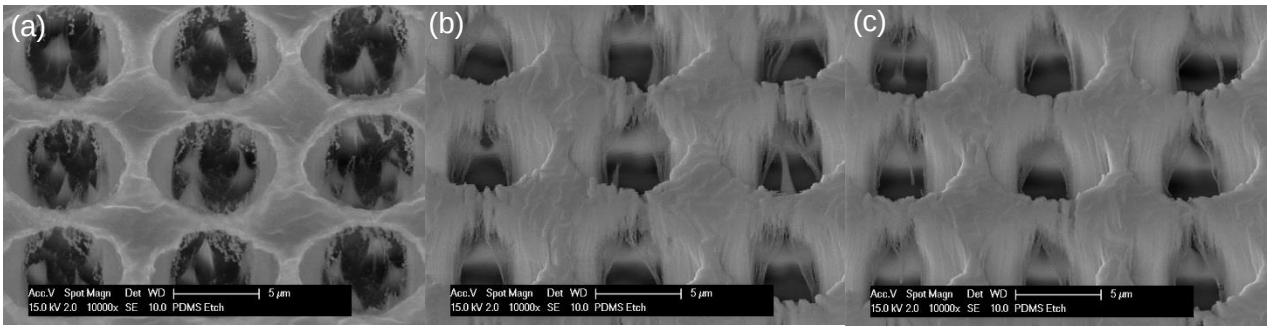


Figure 3.3: SEM images of the membrane taken when the PDMS was etched through at a magnification of 10.000x. A) membrane etched with the standard recipe. B) membrane etched with the high-power recipe. C) Membrane etched with the high power and low temperature recipe.

Table 3.2: Time to etch through the PDMS layer for the different recipes.

Recipe number	Recipe name	Time to etch through the PDMS layer (min)
1	Standard	54
2	High power	36
3	High pressure	-
4	Low temperature	-
5	High power, low temperature	34

3.2.3. Discussion

Influence of chuck cooling

As seen in Chapter 2, there is an effect of chuck cooling on the temperature of the wafer. In addition, bias power is also influencing the temperature of the wafer.
The location of the chuck cooling canals became visible when the wafer recipe nr. 2 was etched, as depicted in Figure 3.4.a. This was due to the difference in silicon oxide thickness, which resulted in a difference in the color of the silicon oxide. The change in color indicated that the etch rate was different per region on the wafer. The difference in etch rate from Figure 3.4a could not be quantitatively estimated. In order to quantify the difference in etch rate, a SEM image was taken at the center of the wafer as well as at a region that was not cooled. Figure 3.4b shows an image of the membrane taken at the

center of the wafer. Figure 3.4c shows an image taken at the periphery of the wafer. No differences were observed.

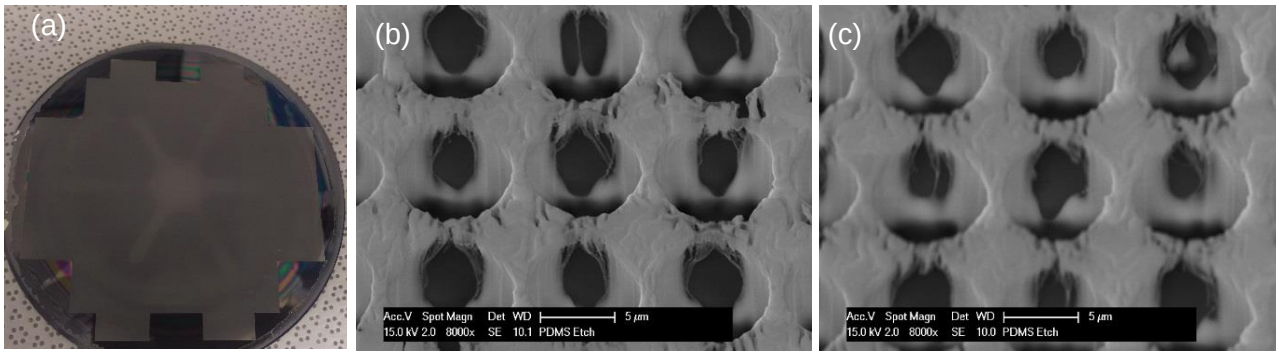


Figure 3.4: A) Image of the wafer after 36 min of etch time with the high-power recipe (nr.2). B) SEM image of the pores at the centre of the wafer. C) SEM image of the pores at the peripheral of the wafer.

3.2.1. Conclusion

To conclude, the scaffold could be replicated within an acceptable time frame using the control recipe and with the high-power recipes.
In this study, it was impossible to etch through the PDMS layer using the high-pressure recipes within 80 min. Hence, this etch procedure was discontinued.
The low temperature recipe was terminated earlier because the machine could not load the 10°C recipes anymore, as explained in Subsection 3.1.2.
Compared to the control recipe, the higher bias power recipe (recipe nr 2) has a higher lateral and vertical etch rate: the vertical etch rate was increased by 50%. In addition, we observed that the aluminum is etched away due to the sputtering of the aluminum mask by the highly energized ions.
The results of recipe nr. 4 (low temperature only) could not be obtained, because the machine was unable to handle 10°C recipes for a long period of time[2].
The results of recipe nr. 5 (low temperature, high power) could be obtained as the membrane was etched through much quicker.
A potential reason for the fact that recipe nr. 5 etches much faster than recipe nr. 2 could be that the etch time for recipe nr. 2 was determined by using etch steps of 2 minutes. During determination of this etch time, the conclusion was drawn that an etch step of 2 minutes was too small to accurately determine the etch time. Therefore, the etch was divided into steps of 4 minutes for recipe nr. 5. However, this possibly resulted in a faster overall etch rate.
When using the higher-pressure recipe for etching, the PDMS was not etched through within 80 min etching time. This amount of etch time was exceptionally high, and therefore the test was discontinued.

Change in research objective.

It was not entirely possible to duplicate the results of Quirós-Solano *et al.* in this experiment. A significant difference between their work and this work was the time to reach breakthrough of the membrane with his recipe. With the fastest recipe the time to breakthrough was at 34 min compared to 16 min in their work. Additionally, the first gaps appeared before breakthrough for all recipes in this study. Therefore, the last research objective in this Chapter was amended to show that with the correct parameters a membrane without lateral gaps could be fabricated.

[2] Redoing the test later, after the proposed solution of the previous section was found, would influence the outcome too much: the condition of the chamber had been changed and the temperature could not be established within the first 3 minutes with the temporary solution.

3.3. Quantifying the effect of process parameters on PDMS etching

The second research objective was to quantify the effects of variations in the process parameters on the vertical and lateral etch rates.

3.3.1. Adaption to process flow

The set-up of the process flow was changed for the second set of experiments as it was necessary to create thicker membranes. Hence, the thickness was increased from 9 μm to 17 μm. Furthermore, a different lithographic mask was used to obtain the required large pore-to-pore distance.

Etch time, membrane thickness and mask porosity

The etch time was set at 36 min. This time was chosen such that sufficient material was etched in the lateral direction to estimate the lateral etch rate. Furthermore, for selected parameters an extra time moment at 26 min was chosen to determine the effect of process time on the lateral and vertical etch rates.

The thickness of the membrane was increased to 17 μm to allow for sufficient etch time. With the fastest recipe of the previous research, a 9 μm membrane was etched through within 36 min. However, it was expected that the etch rates would be higher in this case, as the etch was performed in a single step. A further increase in membrane thickness beyond 17 μm would reduce the thermal conduction of the PDMS, and therefore it could influence the etch rate too much.

A low porosity mask was selected, so that no pore could overlap with another pore during etching. The reason for this was to be able to create a clear cross section of a single pore. Furthermore, the lower porosity increased the mechanical stability of the membrane that was needed for a clear cut.

Lithography step

As mentioned before, the recipe used for the developer was no longer adequate and the pores were not completely open. Figure 3.5a shows a part of the membrane with holes that were not completely open. Figure 3.5b shows its close-up. Both figures show that the shape of the hole is not round, and the diameter is too small: 4 μm instead of 8 μm. To ensure that the resulted difference in pore-size would not affect the rest of the process, only images with a pore diameter of at least 7.5 μm were used for the coming experiments.

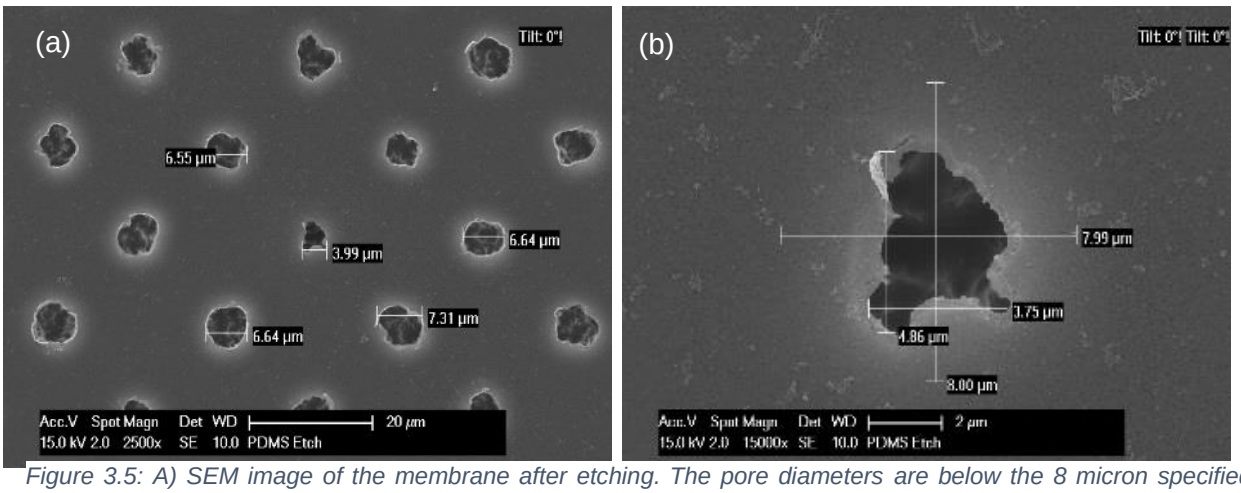


Figure 3.5: A) SEM image of the membrane after etching. The pore diameters are below the 8 micron specified diameter. B) Close up of a single pore.

Process parameters to study

For this research objective the effect of the same parameters from the previous research objective were studied. These parameters were: bias power, chamber pressure and chuck temperature. Furthermore, gas flow was added as a parameter and the combination of an increase in power together with an increase in pressure was tested. Not only the process parameters were changed, also the effect of PDMS base to curing agent mixing ratios was studied (20:1,10:1 and 5:1). The experiments are summarized in Table 3.3.
The wafers were etched continuously. Thus, a wafer was etched for 26 min and another was etched for 36 min. The choice for 36 sccm of gas flow was due to the change in reactor conditions. The standard gas flow of 45 sccm could not be used with recipes with a pressure of 5 mTorr. However, the higher-pressure recipes were etched first and the change to a lower gas flow was made after the wafers were already etched.

Table 3.3: Etch recipes for the second research objective.

Recipe number	Bias power (W)	Chamber pressure (mTorr)	Chuck temperature (°C)	PDMS Mixing ratio	Gas flow (sccm)	Time (min)
1	10	5	25	10:1	36	26, 36
2	20	5	25	10:1	36	36
3	50	5	25	10:1	36	26, 36
4	10	20	25	10:1	45	36
5	10	50	25	10:1	45	26, 36
6	10	5	10	10:1	36	26, 36
7	10	5	25	5:1	36	36
8	10	5	25	20:1	36	36
9	30	5	25	10:1	22.5	36
10	50	50	25	10:1	45	36

Imaging

After etching the next step is to assess the shape of the pores. In this experiment, the wafers were cleaved before imaging, to create a clear cross section of the pores. While cleaving, the wafers were emerged in liquid nitrogen. The reason was that PDMS is a soft material and will stretch before breaking and that can deform the pores. The liquid nitrogen cooled the membrane and made them brittle and non-compliant, so that a clear cut can be created.

3.3.2. Results

Below the results on how the process parameters influence the lateral and vertical etch rates are given. The process parameters that were studied, were bias power, chamber pressure, temperature, mixing ratio, gas flow and time.
The figures below show a cross section of the pores taken with the SEM under a 45-degree angle. The tables below provide the vertical etch rate (Vr), the lateral etch rate (Lr), the isotropicity (Is) and the depth of the bowing (Bd). The etch rates are shown in μm/hr. Here, isotropicity is defined as the lateral etch rate divided by the vertical etch rate and multiplied by one hundred. The bowing depth is the depth where the lateral etch rate was the highest.

Bias power

Table 3.4: The effect of bias power on the lateral and vertical etch rates (micron/hour).

	10 W				30 W				50 W			
Time (min)	Vr	Lr	Is	Bd	Vr	Lr	Is	Bd	Vr	Lr	Is	Bd
26	16.3	0.5	3.1	—	—	—	—	—	31.2	1.9	6.2	8.5
36	14.1	0.94	6.7	—	26.5	1.31	5.0	8.9	>29.3	1.5	<5.2	10.9

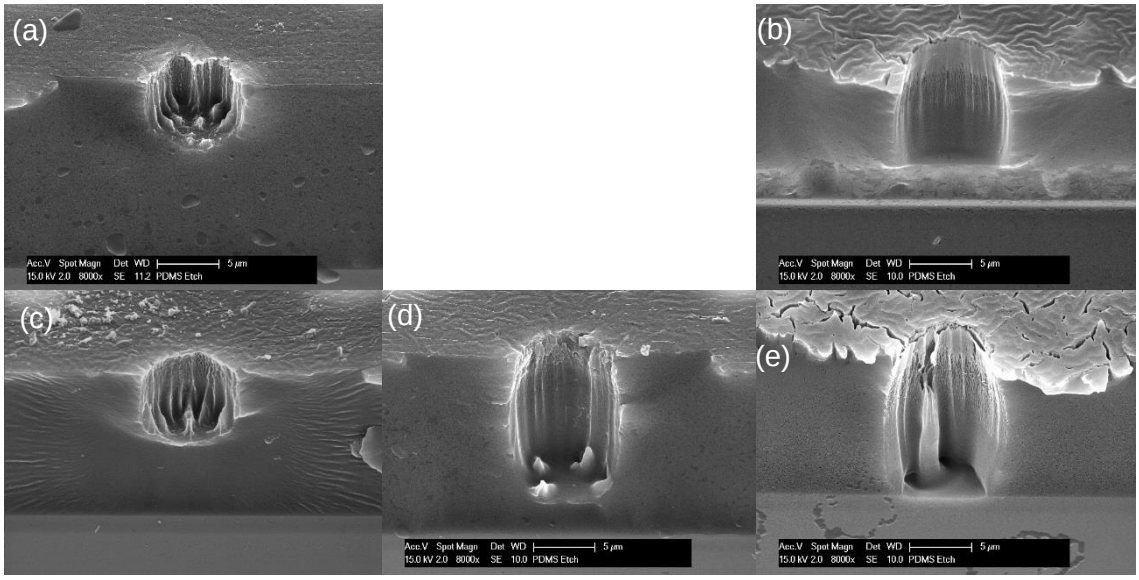


Figure 3.6: Cross sections of a single pore in the membrane, taken with an SEM at a magnification of 8000x.A) Bias power: 10 W, time: 26 min. B) Bias power: 50 W, time: 26 min. C) Bias power: 10 W, time: 36 min. D) Bias power: 30 W, time: 36 min. E) Bias power: 50 W, time: 36 min.

At 36 min, the PDMS was etched through with the 50 W recipe. Therefore, the vertical etch rate could not be determined. Table 3.4 shows that the vertical etch rate increases by 88% between 10 W and 30 W bias power. Between 30 W and 50 W bias power the vertical etch rate increased by at least 10%. The lateral etch rate increased by 39% between 10 W and 30W bias power. Between 30 W and 50 W the lateral etch rate increases by 15%. The surface roughness is decreased with increasing bias power.

Chamber pressure

Table 3.5 The effect of chamber pressure on the lateral and vertical etch rates (micron/hour).

	5 mTorr				20 mTorr				50 mTorr			
Time (min)	Vr	Lr	Is	Bd	Vr	Lr	Is	Bd	Vr	Lr	Is	Bd
26	16.3	0.5	3.1	—	—	—	—	—	9.9	0.5	5.0	1.1
36	14.1	0.94	6.7	—	12.5	0.6	4.8	2.1	9.0	0.6	6.6	1.4

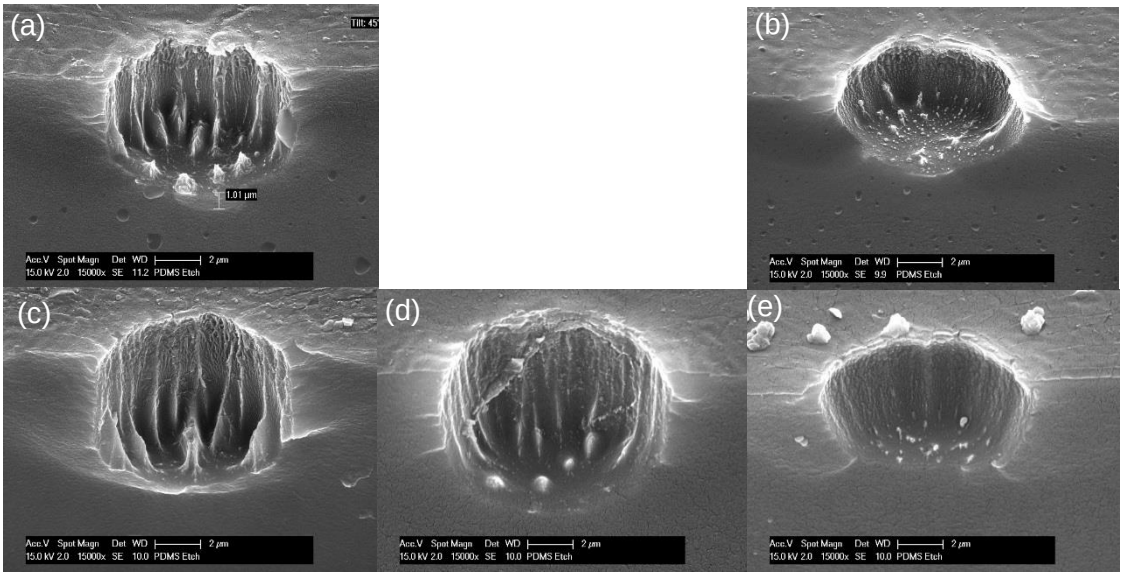


Figure 3.7: Cross sections of a single pore in the membrane, taken with an SEM at a magnification of 15000x. A) pressure: 5 mTorr, time: 26 min. B) pressure: 50 mTorr, time: 26 min. C) pressure: 5 mTorr, time: 36 min. D) pressure: 20 mTorr, time: 36 min. E) pressure: 50 mTorr, time: 36 min.

Influence of pressure

Table 3.5 shows that the vertical etch rate decreased by 11% between 5 mTorr and 20 mTorr chamber pressure. Between 20 mTorr and 50 mTorr chamber pressure the vertical etch rate decreased by 28%. The lateral etch rate decreased by 36% between 5 mTorr and 20 mTorr chamber pressure. Between 20 mTorr and 50 mTorr the lateral etch rate was unchanged. The surface roughness decreased with increasing chamber pressure.

Temperature

Table 3.6: The effect of temperature on the lateral and vertical etch rates (micron/hour).

	25°C				10°C			
Time (min)	Vr	Lr	Is	Bd	Vr	Lr	Is	Bd
26	16.3	0.5	3.1	—	18.2	1.0	5.7	3.0
36	14.1	0.94	6.7	—	14.1	0.8	5.9	5.0

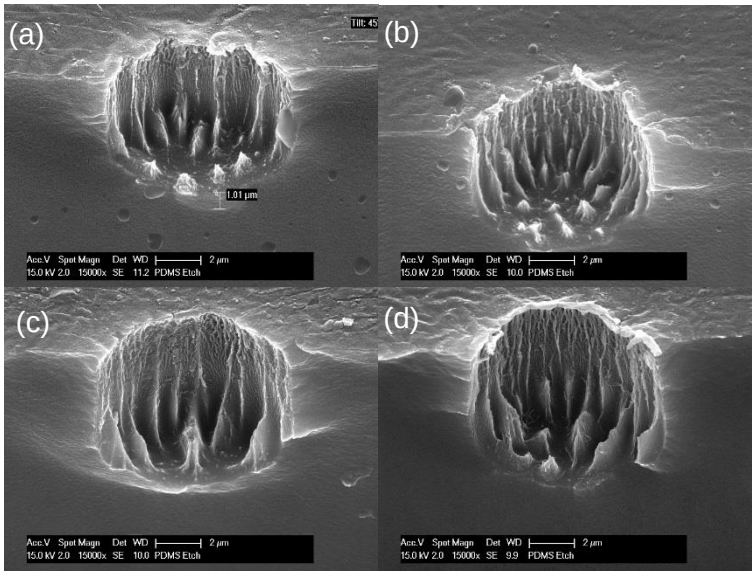


Figure 3.8: Cross sections of a single pore in the membrane, taken with an SEM at a magnification of 15000x. A) chuck temperature: 25°C, time: 26 min. B) chuck temperature: 10°C, time: 26 min. C) chuck temperature: 25°C, time: 36 min. D) chuck temperature: 10°C, time: 36 min.

Influence of temperature

Table 3.6 shows that at the 26min-mark the vertical etch rate increased by 12% when the temperature was reduced to 10°C. At 36 min there is no difference between the vertical etch rates of both recipes. At the 26min-mark the lateral etch rate increased by 100% when the temperature was reduced to 10°C. At the 36min-mark the lateral rate was reduced by 15% when the temperature was reduced to 10°C. The surface roughness was similar for both recipes.

PDMS mixing ratio and aluminum over etch

Table 3.7: The effect of PDMS mixing ratio and aluminum over etch on the lateral and vertical etch rates (micron/hour).

	5:1				10:1				20:1			
Time (min)	Vr	Lr	Is	Bd	Vr	Lr	Is	Bd	Vr	Lr	Is	Bd
36	12.7	0.4	3.4	2.5	12.0	0.43	3.6	3.3	12.1	0.19	1.6	2.4

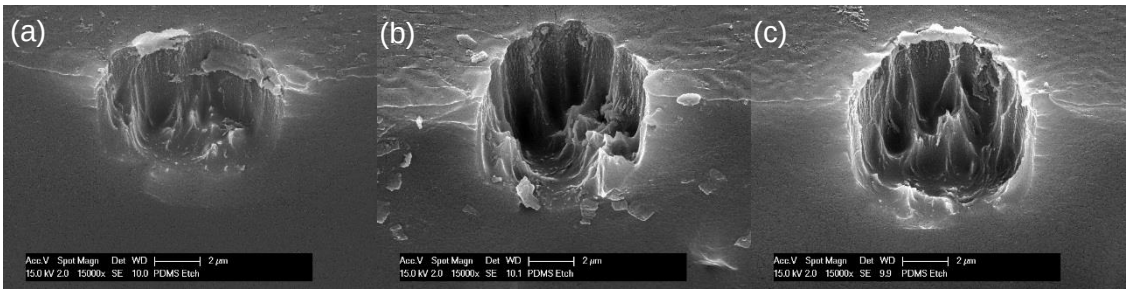


Figure 3.9: Cross sections of a single pore in the membrane, taken with an SEM at a magnification of 15000x. A) PDMS mixing ratio: 5:1, time: 36 min. B) PDMS mixing ratio: 10:1, time: 36 min. C) PDMS mixing ratio: 20:1, time: 36 min.

Influence of PDMS mixing ratio's

Table 3.7 shows an increase of 6% in the vertical etch rate when a 5:1 PDMS mixing ratio was used compared to the 10:1 PDMS mixing ratio. With a 20:1 PDMS mixing ratio the

vertical etch rate increased by less than 1% compared to the 10:1 ratio. The lateral etch rate decreased by 7% with a 5:1 PDMS mixing ratio compared to the 10:1 ratio. The lateral etch rate decreased by 56% when a 20:1 mixing ratio was used compared to the 10:1 ratio.

Influence of aluminum over etch

The was no aluminum over etch for these wafers. The wafer with the 10:1 mixing ratio had the same mixing ratio as the wafer that was etched with the standard recipe in the previous results. However, there is a reduction of 15% for the vertical etch rate and a reduction of 54% for the lateral etch rate for this wafer compared to the other wafer that had an aluminum over etch. Furthermore, the surface roughness was increased when there is no aluminum over etch.

Gas flow

Table 3.8: The effect of gas flow on the lateral and vertical etch rates (micron/hour).

	36 sccm 30W				22.5 sccm 30W			
Time (min)	Vr	Lr	Is	Bd	Vr	Lr	Is	Bd
36	26.5	1.2	4.6	8.9	24.0	1.7	7.0	7.9

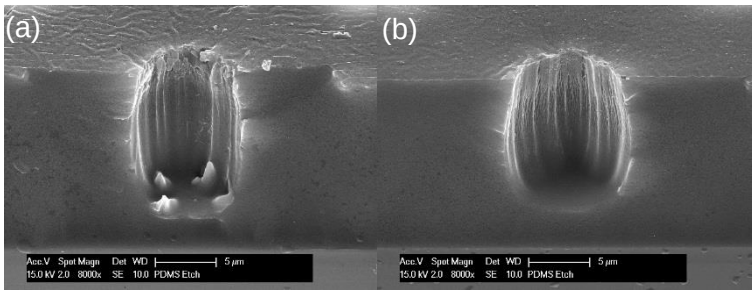


Figure 3.10: Cross sections of a single pore in the membrane, taken with an SEM at a magnification of 8000x. A) gas flow:36 sccm, time: 36 min. B) gas flow:22.5 sccm, time: 36 min.

Influence of gas flow

Table 3.8 shows that the vertical etch rate decreased by 10% when the gas flow is reduced to 22.5 sccm. However, the lateral etch rate is increased by 40% when the gas flow is reduced to 22.5 sccm.

Combination of high bias power and high pressure

Table 3.9 The effect of combined high bias power and high pressure on the lateral and vertical etch rates (micron/hour).

	5 mTorr 50 W				50 mTorr 50 W			
Time (min)	Vr	Lr	Is	Bd	Vr	Lr	Is	Bd
36	>29.3	1.5	<5.2	10.9	17.0	0.3	1.9	4.7

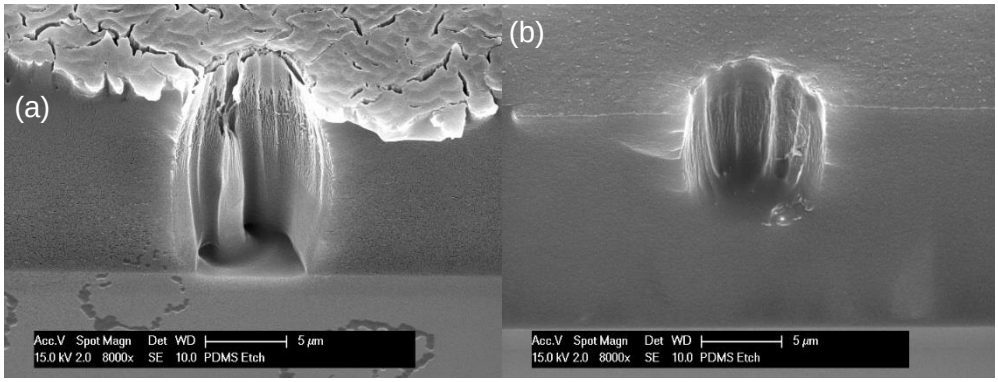


Figure 3.11: Cross sections of a single pore in the membrane, taken with an SEM at a magnification of 8000x. A) pressure: 5 mTorr, time:36 min. B) pressure: 50 mTorr, time:36 min.

Combination of high power and high pressure

Table 3.9 shows that vertical etch rate of the 50 mTorr, 50 W-recipe is reduced with at least 42% compared to the 5 mTorr, 50 W-recipe. Furthermore, the lateral etch rate is reduced by 80%. The lateral etch rate of the 50 mTorr, 50 W-recipe is also lower than that of the standard recipe, while the vertical etch rate is higher compared to the standard recipe.

Influence of time

When the etch time increases the vertical etch rate decreases. This effect is less noticeable with higher power or pressure and more noticeable for a lower temperature. There is however, no noticeable pattern for the time dependency of the lateral etch rate.

3.3.3. Discussion

In this section the results are compared against the previous experiments and studies. In addition, some recommendations for improvements that could be made to increase the accuracy of the tests.

In the first experiment it took 36 min for the 50 W-recipe to etch through a 9 µm-thick membrane. With this setting, it took under 36 min to etch through a 17 µm-thick membrane. There is also an increase in vertical etch rate for the standard recipe in this experiment compared to the first set of experiments. This increase in etch rates can be explained by the fact that they were etched in a single step.
In this study, an increase in the vertical etch rate with decreasing chuck temperature was observed. On the contrary, a previous study performed by Domański *et al.* [52] observed an increase in etch rate for a higher wafer temperature.
Not only the etch rate for PDMS is increasing for a higher power, the etch rate for aluminum is also increasing, and thus the selectivity is decreasing. Consequently, with a higher aluminum etch rate, a thicker aluminum mask has to be used. This will increase the depositing time. Furthermore, the aluminum will be redeposited during etching on the sidewalls of the PDMS and that can influence cell biology in a later stage. The quantification of the amount of aluminum sputtering is recommended for future work.
As seen in the Section 3.3.1, the pores were not completely open after developing. Thus, the images were selected based on the opening of the pores. Only pores with a width greater than 7.5 µm were selected. However, for some wafers the openings were larger than 8.5 µm on average. A reason for the increase in pore width could be that when the wafers are cleaved, the PDMS is stretched. In this case, the pore appears to be wider. This raises the question whether the lateral etch rate was overestimated because probably not only the top of the pore is wider, but the complete pore is stretched.

3.3.4. Conclusion

The aim of this research objective was to investigate the influence of the process parameters on the lateral and the vertical etch rate, and to quantify their influence. To conclude, it was found that the influence of the variables is not independent and that there is an interaction among the variables.
The lowest isotropicity etch was achieved with a combination of high pressure and high power. Not only had this recipe the lowest isotropicity, it was also faster than the standard recipe without having the lower selectivity of a high-power recipe.
The highest isotropicity etch was obtained with reduced gas flow at 30 W. The vertical etch rate was reduced by only 10% compared to the 30 W-recipe, while the lateral etch rate was increased by 40%. This recipe also had the highest later etch rate at 36 min. The 50 W-recipe had the second highest lateral etch rate and the standard recipe had the second highest isotropicity.
The shape of the hole is also dependent on the etch recipe. With a higher power the bowing effect will be located closer to the bottom of the hole as compared to the standard recipe. With a higher pressure the bowing effect will be closer to the surface. This can be useful when the membranes have a different thickness.

Improvements related to the experiments

Only a single wafer was tested for each recipe and this is a small sample size. Especially considering that there are many factors apart from the process parameters that can influence the etch process. Increasing the number of wafers and datapoints is recommended for in future work preferably executed on a well-functioning machine.
Not only the number of wafers per recipe could have been increased, also the number of recipes tested should be increased. During this study there were two or three data points per parameter. The relationship between a variable and the etch rate can be extracted better when more than three data points are known. However, an indication of a relationship was the main objective of this research and not the absolute value of the relationship. This was because the machine was not functioning as it should and therefore the relationship will change when the experiment is repeated at a later stage.
For future studies it is recommended to repeat the tests with a proper functioning machine. With the machine in its current status there was reflection of bias power. Furthermore, the gas flow had to be changed during the course of the experiments because the low-pressure recipes could not be run with the standard gas flow of 45 sccm. The need to change the gas flow, indicates that also the chamber wall conditions were changed. This may have influenced the etch rates as well.

3.4. Tuning the porosity of a membrane

The last research objective was to use the information gathered in the previous experiments to tune the porosity of a membrane. For this experiment the same process flow as in the first research objective is used. However, a new matching capacitor was installed in the ICP tool. With the new matching capacitor, the reflected bias power was reduced. The thickness of the membrane was 9 μm for this experiment.
With this research the aim was to answer the following research questions: Is it possible to again create a scaffold with lateral gaps between the pores now that the reflected power is reduced. Furthermore, can a membrane without the lateral gaps between the pores be created?

3.4.1. Adaption to process flow

The process flow for this research question is the same as in Section 3.1.

New matching capacitor for the etching machine

The start of this experiment also marked the installation of a new matching capacitor. This capacitor is part of the matching circuit of the bias power generator. The capacitor compensates for the reactance created by the inductive coupling between the antenna and the plasma. This matching reduces the bias power that was reflected. For recipes with a pressure of 5 mTorr, the reflecting power was zero for a bias power up to 50 W. At 50 W the reflected power was 9W. Furthermore, for 20 W recipes the reflected power increased with increasing pressure. At a pressure of 20 mTorr the reflected power was between 0 W and 9 W. The reflected power increased up to 12 W at a pressure of 30 mTorr. The recipe with high power and high pressure was the recipe with the lowest isotropicity. Due to the reflected power the pressure was reduced to 20 mTorr from 50 mTorr.

Process parameters

The choice of process parameters that were used to create a specific membrane was based on the experiments in the previous sections. The three different recipes that were tested are shown below in Table 3.10. Recipe nr. 1 was chosen, as it had the least amount of mask sputtering in the first research question. Recipe nr. 2 was chosen because it had the highest vertical and lateral etch rates based on the previous experiment. Finally, recipe nr. 3 was chosen because it has the lowest isotropicity in the previous experiment.

Table 3.10: Recipes for research question 3

Recipe number	Recipe name	Power (W)	Pressure (mTorr)	Temperature (°C)
1	Standard	10	5	25
2	High power	20	5	25
3	High power, high pressure	20	30	25

3.4.2. Results

Figure 3.12 shows the SEM images of the membrane at breakthrough. The time it took to etch through the membrane is depicted in
Table 3.11.

Table 3.11: Time until breakthrough for the recipes of research question 3.

Recipe number	Recipe name	Time to break through (min.)
1	Standard	32
2	High power	10
3	High power, high pressure	20

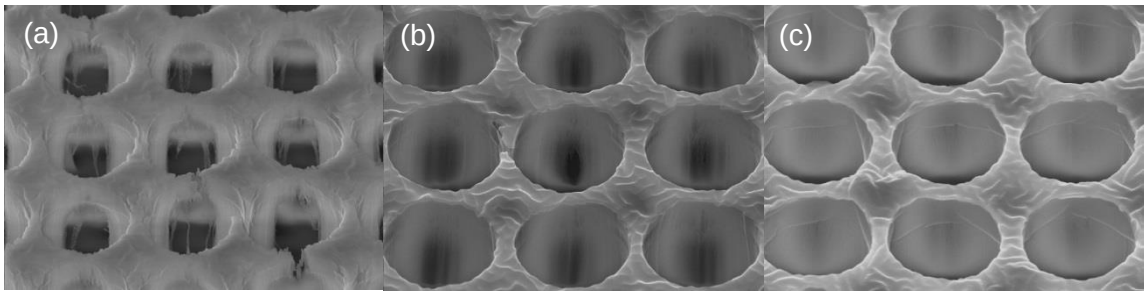


Figure 3.12: SEM images of the membrane taken under a 45 degree angle at 10.000x magnification. A) membrane etched with the standard recipe at breakthrough. B) Membrane etched with the 20W-recipe at breakthrough. C) Membrane etched with a 20W- and 20 mTorr-recipe at breakthrough.

3.4.3. Discussion

When comparing the results of this study to the results of Quirós-Solano *et al.,* the main difference that was noticed is that the surface roughness of the membranes of Quirós-Solano *et al.* is lower compared to the surface roughness of the membranes from this study. In addition, the required time until breakthrough is still increased compared to the results of Quirós-Solano *et al.*

The results of this experiment can be compared to the result of the first experiment. In the first experiment the time to land on the oxide for the control recipe was 54 min compared to 32min for this experiment. This is an increase in etch rate of almost 70%. This number was unexpected because the machine showed zero reflected power for the standard recipe in both runs. Thus, it is likely that the reflected power was above 0 W in the first set of experiments.

3.4.4. Conclusion

The isotropicity can be tuned by tuning the different process parameters. With the control recipe there are large gaps between the pores at breakthrough. These gaps are smaller when a higher power is used. If both power and pressure are increased the gaps between the pores disappear.
Thus, in order to eliminate the gaps between the walls, the following recommendations are given:

1. Use a high power and high-pressure recipe.
2. Use a membrane with a lower pore density.

However, if high porosity is required the fastest method would be to use a high-power recipe. With this recipe the vertical etch rate is the highest and the lateral etch rate is also higher compared to the standard recipe.

4. Optimizing the PAA process flow for thick (>20μm) membranes

This chapter describes in details the process flow of fabricating thick transferrable membranes. The current process is based on the technique presented by Quirós-Solano *et al* [1]. This work fabricated and transferred thin transferrable membranes. However, with this fabrication process and the tooling available at TU Delft, it was not possible to fabricate membranes thicker than 10 μm. A research group at the Technical University in Eindhoven (TU/e) requested thick (> 20 μm) PDMS membranes for their research in cell cultures. They placed cells within the pores of the membranes and the thickness of the membrane had to be such that the cells where constrained inside the pores.
Hence, the aim of this study was to adapt the process flow of Quirós-Solano *et al.* in order to fabricate 20-μm thick transferrable PDMS membranes. The PDMS membranes of this study were fabricated in the Else Kooi Lab clean room at TU Delft. Testing of the transferability of the membrane and its suitability for cell research was performed in collaboration with TU/e. First, the major adaptions that were done to the process are described. Secondly, the results of the membrane transferability tests and membrane suitability tests for cell research are discussed.

The method of Quirós-Solano et al.

The transferring method presented in Figure 4.1 consists of adding a sacrificial layer of PAA between the silicon wafer and the PDMS membrane. This makes it easier to transfer the membrane onto an OOC microfluidic chip. Before transferring, the wafer is diced. The membrane and base of the OOC are both irradiated by an oxygen plasma to improve the bonding [64]. After the oxygen plasma treatment, the base and the membrane are combined and pressed together (Figure 4.1i). Due to the presence of the silicon substrate, the membrane is kept straight during these operations, making it easier to be aligned. The merging is followed by placement into an ultrasonic bath filled with water. After ten minutes the PAA is dissolved and the silicon substrate can be removed (Figure 4.1m). The base

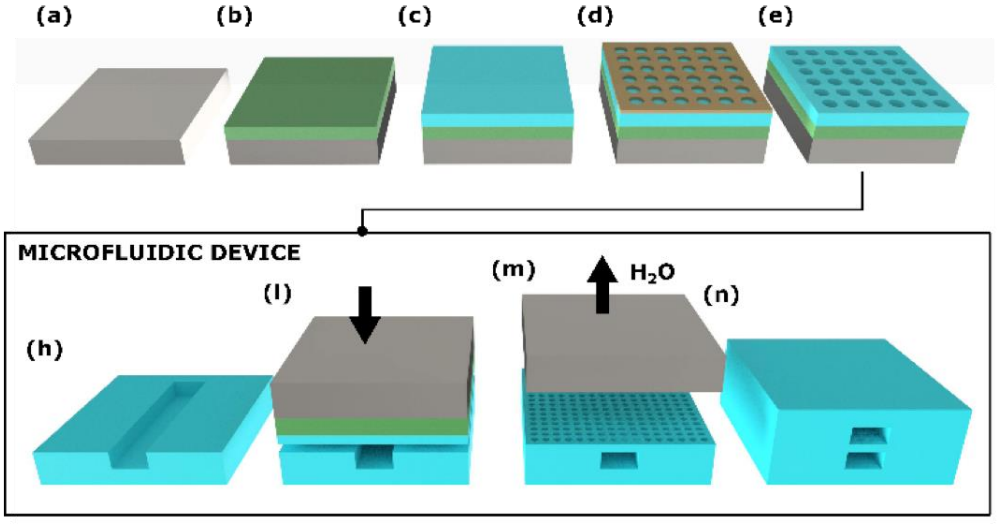


Figure 4.1 Fabrication and transferring of a porous membrane. (a) to (e) depicts the fabrication of the membranes. (h) to (n) shows the transferring and device assembly.

(a) Silicon substrate; (b) PAA depositing; (c) PDMS depositing; (d) aluminum mask depositing and patterning by lithography; (e) dry etching of the PDMS and removal of the mask; (h) base of the OOC; (l) transferring of the membrane with the rest of the layer to the OOC; (m) removing of the silicon substrate after the PAA is dissolved in the water; (n) final assembly of the device.

with the membrane can then be withdrawn from the water bath, which finalizes the transfer. The device is ready for the next process steps.

Research of TU/e

The research group of TU/e studies the influence of cell strain on cell proliferation. Therefore, they employed a Flexcell device shown in Figure 4.2a. In the Flexcell device, the rubber membrane is stretched whereupon strain is created on the cells (Figure 4.2b). Both the effect of cell strain on individual cells as on clusters of cells are studied. The pores of the thick PDMS membrane will compose a microwell in which the individual cells or the cluster of cells could be seeded. The bottom of the wells are formed by the rubber membrane of the Flexcell device. The preferred PDMS membrane has a thickness over 20 μm, with pores ranging from 100 to 1000 μm. The width of the pores was chosen because the estimated cell diameter was around 100 μm. Although the thickness of the membrane was sufficient to constrain a single cell within the micro well, a thicker membrane had their preference. Only, a further increase in thickness would have increased the fabrication time.

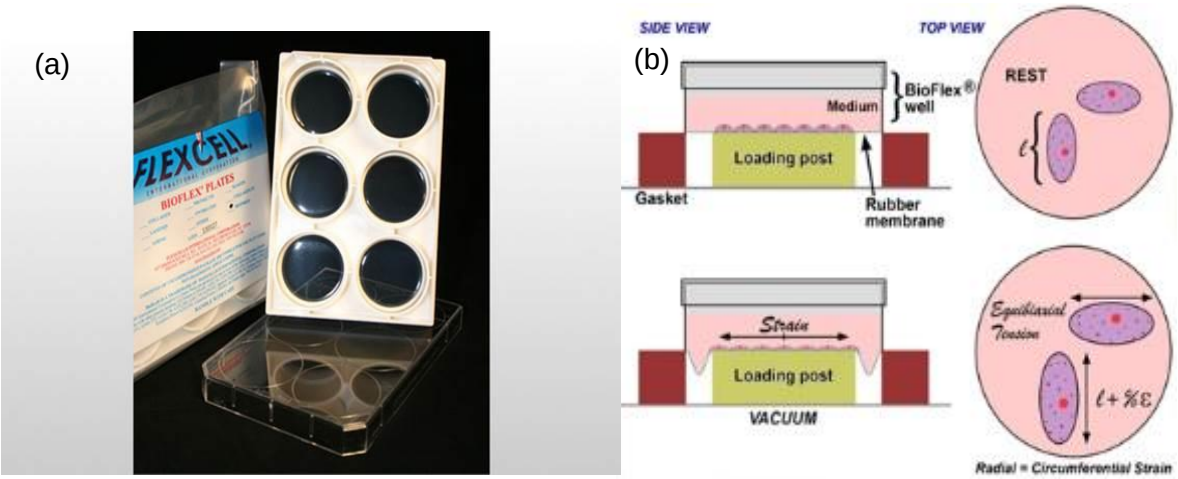


Figure 4.2: A) Bioflex plates from Flexcell with six wells. B) The proposed cell test. The influence of cell strain on cell proliferation can be tested by creating a vacuum beneath the rubber membrane of the BioFlex plate. The vacuum creates a strain on the membrane and on the cells cultured on the membrane. In this research the cells are human vascular-derived cells. The location of the cells is additionally constrained with a PDMS membrane on top of the rubber membrane of the Bioflex plate. The cells are seeded within an individual pore in the membrane.

Membrane specification

Figure 4.3.a shows the layout of the membrane. The dimensions of the membrane are 17 mm by 17 mm and it is divided into three parts. The first part has five 1 mm wide holes, the second part has an array of 18 mm by 36 mm with two overlapping 100 μm wide holes and the last part has an array of 18 mm by 72 mm with 100 μm wide holes. A mask for the contact aligner was designed in house with Tanner L-EDIT IC Layout software and fabricated by Compugraphics International Company. Only a single mask was needed. A total of 12 membranes can fit on a mask as seen in Figure 4.3.b.

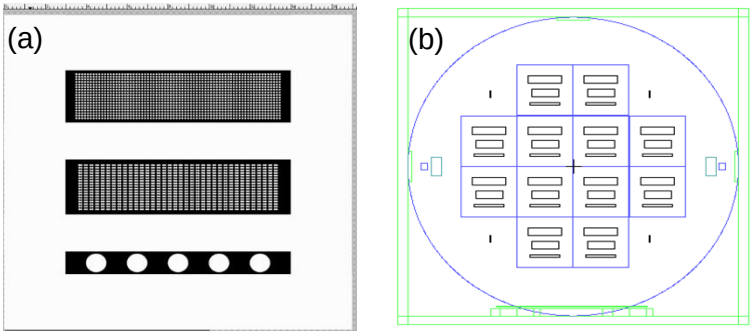


Figure 4.3: A) lay-out of the membrane with the three different sections. B) Design of the chrome lithographic mask with a total of 12 membranes per wafer.

4.1. Process flow and the adaptions to the process flow

The adaptations made in the process flow of Quirós-Solano *et al.* resulted in the following process summary. The adaptations are described in detail after the summary. One of the most relevant changes performed in this research was the change in aluminum depositing (step 3). This was changed from sputtering to evaporating, due the PAA and the thick PDMS layer. Unfortunately, this change added extra complications in the process.

The process flow summary

Step 1

The fabrication process is performed on a silicon substrate. A 1.5 μm thick photoresist layer is spin coated on the backside of the wafer. Then, a PAA layer[3] with 0.5 μm thickness is deposited by spin coating on the frontside. The spin-speed for the PAA deposition is set to 2000 RPM, and the time is set to 30 sec. The spin coated wafer is subsequently cured in an oven at 100°C for one hour.

Step 2

The PDMS is mixed at a 10:1 base to curing agent ratio and degassed afterwards. The degassed PDMS is then deposited on top of the PAA layer by spin coating. The spin speed to spread the PDMS on top of the PAA layer is set to 300 RPM during 30sec. Next, the spin speed is increased to 4000 RPM during 60 sec. to create the desired thickness of the PDMS layer.

Before continuing to step 3, the edge of the wafer is cleaned with acetone and the wafer is cured in the oven for one hour at 100°C. This step is followed by a cleaning of the backside of the wafer with acetone.

Step 3

A 300nm-thick aluminum layer is evaporated on the front-side of the wafer, serving as a hard mask. On this mask, a 2-μm thick photoresist layer is deposited. This photoresist layer is exposed by proximity exposure, to light that shines through the chrome photolithographic mask.

Step 4

3

[3] The PAA was purchased from Sigma Aldrich and the PDMS (Sylgard 184) was purchased from Dow Corning. The kit from Dow Corning contained a base monomer and a curing agent.

The aluminum is etched in a chloride-based plasma to transfer the pattern in the photoresist layer to the aluminum mask.
Step 5
The PDMS is etched in an ICP reactor.
Step 6
At the end, the aluminum is removed in a wet etch bath filled with a buffered solution of acetic acid, nitric acid and hydrofluoric acid. The wafers are cleaned in deionized water. Subsequently, the wafers are diced and packed.

Optimization of the PAA spin coating process (Step 1)

The first step in the new process was spin coating of PAA onto the silicon wafer. For this process the backside of the wafer was covered with photoresist, which served as a protection layer. The photoresist was removed with acetone after PAA and PDMS deposition. Residues of PAA and PDMS on the backside were removed with the removal of photoresist. Without the photoresist layer, the backside had to be cleaned manually from the residues with a cotton swab. The first step in the spin coating step was to load the wafer on the chuck of the machine. Subsequently, a vacuum was applied and the PAA was poured on top of the wafer. Next, the wafer was spun coated with the required speed and time to get a 0.5 μm thick layer. Afterwards, the wafer was cured in the oven to harden the PAA layer. With this process a 0.5 μm thick layer was created. Unfortunately, two issues were identified. The first issue was that the PAA moved out from the inner circle of the wafer and thus, part of the wafer was not covered in PAA, as seen in Figure 4.4.Figure 4.4: Wafer after PAA depositing with a removal of PAA in the middle of the wafer due to airflow after depositing. In the outer ring there is also removal of PAA due to cleaning the

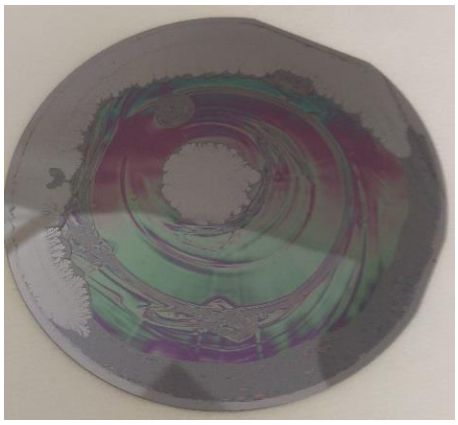


Figure 4.4: Wafer after PAA depositing with a removal of PAA in the middle of the wafer due to airflow after depositing. In the outer ring there is also removal of PAA due to cleaning the wafer with acetone and the impurities on the wafer created during the photoresist depositing.

wafer with acetone and the impurities on the wafer created during the photoresist depositing.The second issue was that PAA moved away from the edges of the wafer. These complications reduced the yield of a single wafer.
The first issue was due to the air ducts in the lid of the spin coating machine. These airducts allowed air to rush in the machine and the air pushed the PAA away. There were four airducts on the lid and by taping three of them, the location of the hole could be influenced. By taping all four of them, the PAA did not move away which resolved the issue. Further in the process, extra tape was applied to prevent air entering via the airducts.
The second issue had two separate causes. First, uncured PAA is sensitive to acetone. When the edges of the wafer were cleaned with acetone, it also removed some of the PAA. One solution was to clean the edges after the curing step. Unfortunately, PAA was difficult to remove with acetone after cleaning, so this solution was not optimal. Instead, the amount of acetone was reduced. Second, photoresist was present on the edges and

the front side of the wafer after spin coating the backside. PAA has the tendency to withdraw from unevenness. Therefore, a solution was to skip the photoresist step and clean the wafer afterwards manually. Again, this was not the preferred solution because it was harder to clean the wafer after curing. Furthermore, the outer ring did not contain the membrane as seen in Figure 4.3 so it was accepted that there was some removal of PAA at the edges of the wafer.

Spin coating PDMS (Step 2)

After spinning and curing of PAA, PDMS was deposited by spin coating on top of the PAA layer. The spin speed and spin time needed to get a 20 μm thick membrane was unknown and was determined during a test. To define the upper limit and lower limit for the spin speed, data from previous tests on SiO_2 were used. The lower limit for this test was set at 3500 RPM and the upper limit at 5000 RPM. The time was kept constant over 60 sec and a total of 4 data points were measured.
Table 4.1 shows the results of the spin speed tests. A spin speed of 4000 RPM was chosen to obtain a 20 μm-thick PDMS layer. The thickness together with the PAA layer was 21 μm.

Table 4.1: Spin speed to PDMS thickness

	Spin speed (RPM)	**Thickness (μm)**
Previous data	3000	30
Measured	3500	23.8
Measured	4000	21.1
Measured	4500	19.4
Measured	5000	17.7
Previous data	6000	9

Evaporation of Aluminum (Step 3)

The next step in the process was depositing of a 300nm-thick aluminum layer on top of the PDMS layer. This is normally performed by sputter coating, but this was not possible due to the PAA and thick PDMS layer. There was too much outgassing during the leak up rate (LUR) test to allow the wafers to be used by the machine for sputter coating. To reduce the out gassing, two options were tested. First, curing time was increased by another hour as uncured PDMS usually results in higher out gassing. Unfortunately, the wafers still failed the LUR test. A further increase in the curing time would have been detrimental to the PDMS and PAA properties, so this option was discarded. The second option was to bring the wafer under vacuum for an hour, so that it had time to outgas in the vacuum chamber. Increasing the time under vacuum showed improvements in the LUR test for PDMS in the past. However, increasing the vacuum time would delay the total process too much, which was unfavorable. Therefore, the depositing of aluminum could not be performed with sputtering.
An alternative to sputtering of aluminum is evaporating. However, the machine at the laboratory had been used in the past for evaporating other metals such as copper and could therefore contaminate the wafers. In order to avoid this issue, the backside of wafers were covered with aluminum foil before being inserted in the machine. It is worth to notice that this machine does not have any temperature control during evaporation. This is problematic when PDMS is thermally expanded while a noncompliant layer is deposited on top. This top layer will buckle after cooling down due to mismatch in coefficient of thermal expansion[65,66].

This was the first time that this machine was used for depositing aluminum on PDMS and therefore a standard recipe was employed for the first tests. This recipe deposited the aluminum in one step with a deposition rate of 1nm/sec for a total of 300 sec to get a 300 nm-thick aluminum layer. After two wafers were processed in the machine, their top layer was buckled, yielding a wave-like appearance as seen in Figure 4.5a. The effects of the waves on the rest of the process flow were still unknown, and the wafers were processed further. As the severe PDMS-Al buckling might affect the lithography, a solution to reduce this problem was developed.

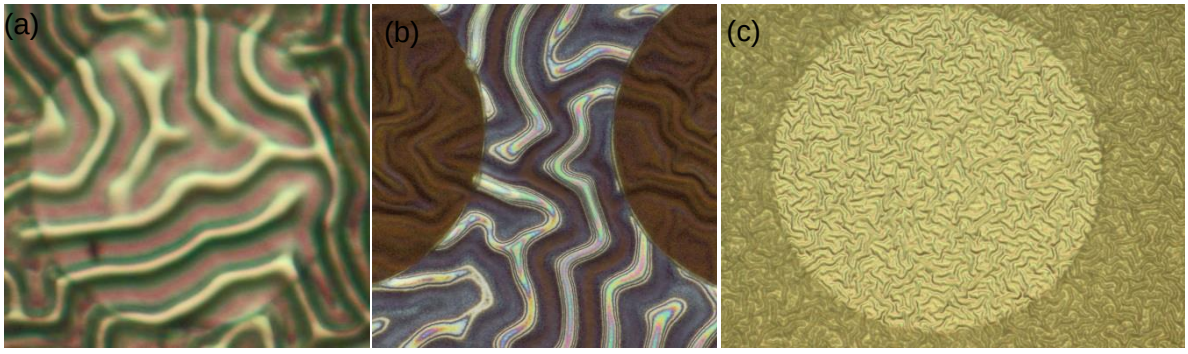


Figure 4.5: A) Wave pattern on the top aluminum layer for a 100-μm pore with the standard recipe. B) Mask etched away in the grooves after the aluminum etch between two pores. C) Single 100-μm wide pore where the waves have a wave length of 2.7 μm.

It was hypothesized that reducing the maximum temperature would reduce the size of the waves. Therefore, the deposition rate was decreased to 0.1nm/sec in order to reduce the heat flux. Furthermore two 15 min breaks were inserted in the deposition step to let the wafer cool down. With these adaptions, the maximum temperature was reduced. The result was that the wavelength was reduced to 2.7 μm as seen in Figure 4.5c. This value was considered acceptable and sufficient as a further reduction in depositing rate and a further increase in time between depositions would increase the processing time too much.

Lithography and aluminum etching (Step 4)

The lithography step was kept similar to the process in Chapter 3 for the wafers with large buckling. However, during etching of aluminum with a standard recipe for a 300 μm thick layer, the aluminum in the grooves was also etched away as seen in in Figure 4.5b. To solve this problem, the waves were reduced as described in the previous paragraphs. In addition, the photoresist recipe was changed to a recipe which was more suitable for wafers with this topography. This recipe used a thicker photoresist layer and additionally, the developing time was increased. After these changes, every pore could be opened without affecting the aluminum mask.

PDMS etching (Step 5)

In order to etch the PDMS, the control recipe from Chapter 3 was chosen. This recipe used a bias power of 10 W, chamber pressure of 5mTorr and a temperature of 25°C. This recipe was chosen as it had the least amount of mask sputtering. The estimated time for the first etch was based on the etch rates of the scaffolds (14 μm/hr). The etch rate for the thick PDMS membranes was around 14 μm/hr to 16 μm/hr at first. However, it increased to 18 μm/hr due to unknown reasons. With the new capacitors installed, the etch rate was 40 μm/hr. This was higher than the etch rate for the porous membrane. The explanation is that this occurred due to the larger openings of the holes. The selectivity for PDMS to PAA is not as high as the selectivity for PDMS to SiO2. Therefore, the PAA layer could not be used as a landing layer. The difference in selectivity would result in etching the silicon layer when the wafer is over etched. The color of the holes as seen through a microscope

changed from white to black, indicating that the PDMS was etched through and that the silicon was being etched. The depth of the holes in the silicon layer were measured after over etching to see if the PDMS was indeed etched away. With an estimated over etch time of 10 min, the silicon substrate was etched to a depth of 15 μm, indicating that the PDMS was indeed etched away and that the selectivity for Si to PDMS is high for this recipe.

Aluminum wet etch and dicing (Step 6)

After the PDMS etch, the aluminum was removed by wet etching in a PES bath for 12 min. Subsequently, the wafers were put in a de-ionized water bath for 4 min to remove the PES residues. The wafers were optically inspected to see if there was no aluminum left. The time in the water bath was reduced from the standard of 10 min because PAA is water soluble. If the PAA under the PDMS gets in contact the water bath for too long, it dissolves, releasing the membranes into the water bath.
After removing the aluminum, the wafers were diced and packaged. The dicing process was done manually because the automated dicer uses water to clean the wafers. Therefore, the automated dicer is not compatible with the PAA. Unfortunately, by manual dicing the wafer got covered in silicon shards. It is unclear whether this has any unfavorable effects. Figure 4.6: A) Diced and packaged membranes B) Single membrane

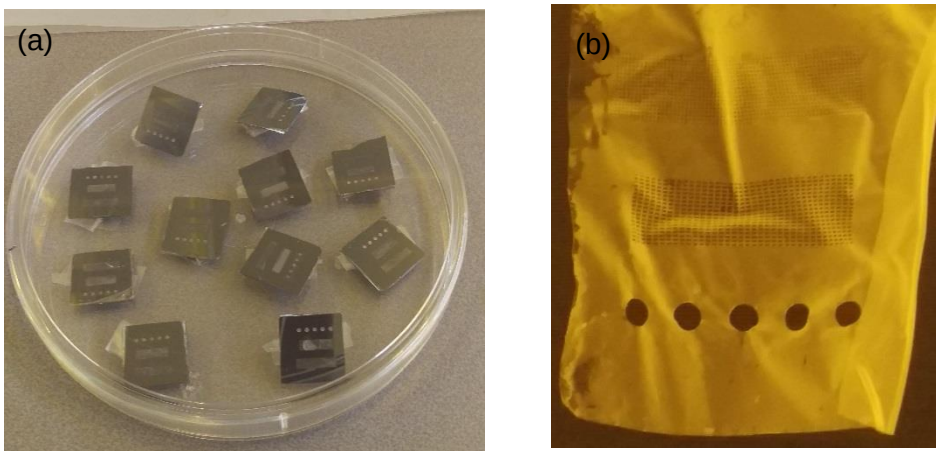


Figure 4.6: A) Diced and packaged membranes B) Single membrane removed from the silicon substrate.

removed from the silicon substrate.

4.2. Results

The membranes fabricated with the process presented in Section 4.1 are presented in Figure 4.6. A released membrane is shown in Figure 4.6b.
The tests performed in TU/e consisted of two steps: testing the transferring of the membranes and testing the location of the cells in the wells.

4.2.1. Transfer of the membrane test

The adapted process flow was tested by transferring the membrane from the silicon substrate to the Flexcell device. First, the surface of the Flexcell and the membrane were activated with an oxygen plasma treatment. Subsequently, the membranes were placed upon the Flexcell substrate and a slight force was exerted from a fingertip on the silicon back side. Next, the membranes were covered with water for 5 min. After 5 min., the membrane adhered to the Flexcell substrate and the silicon substrate could be removed easily without damaging the membrane.

4.2.2. Cell culture test

The second test was performed to verify whether it was possible to seed the cells inside the wells composed by the membrane's pores and the Flexcell membrane. The first step was to place fibronectin inside the wells. Fibronectin is a cell adhesion molecule that serves as a matrix for the cells to attach to. A fluorescence image was taken in order determine the position of the fibronectin after depositing (Figure 4.7). This Figure shows that the fibronectin is sticking to the walls of the pores, instead of the Flexcell surface. The fibronectin should be located at the Flexcell surface to promote the adhesion of the cells. Moreover, the cells should be located in the center of the well and not sticking to the walls. The reason that more fibronectin was located at the PDMS membrane is because fibronectin adheres badly to the Flexcell surface[67]. Moreover, the surface roughness of the membranes was higher than the surface roughness of the Flexcell, and fibronectin adheres better to rough surfaces. The last issue can be resolved by reducing the sidewall roughness. As noted in the previous chapter, a higher bias power leads to a smoother surface. Unfortunately, during the fabrication of these membranes, we did not get the desired output.

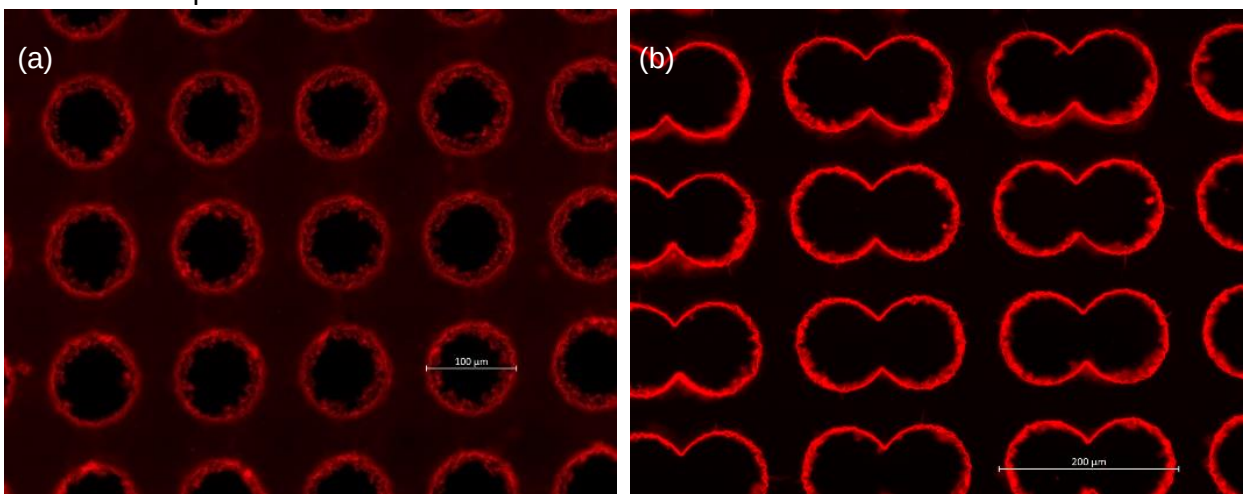


Figure 4.7: A) A fluorescent image of the membrane with the 100-µm wide pores displayed. The fibronectin in red is located at the membrane walls and not on the Flexcell substrate. B) Similar image for the double pores.

4.3. Conclusion

The purpose of this research was to make transferrable membranes by adapting the process flow of Quirós-Solano *et al.* The major adaptions from their process flow were:

- Optimization of the PAA coating recipe.
- Change of the PDMS spin recipe to create a 20 µm membrane.
- Evaporation and optimization of an evaporated aluminum hard mask.
- Change of the photoresist coating recipe compatible with the topography caused by the buckling of the aluminum top layer.

With this new process is was possible to create membranes with a 20 µm thickness and a sacrificial layer of PAA. However, the process time is longer due to slow deposition of aluminum. Evaporation of six wafers is as fast as sputtering 25 wafers and it takes around two hours of process time. With the adaption of the process flow, it was still possible to transfer the thick membranes. However, the surface roughness of the membranes was too high, and the fibronectin did adhere to the walls of the PDMS membrane and not to the bottom of the microwell.

4.4. Discussion

In this study, significant contributions have been made to adapt the process flow of Quirós-Solano *et al.* However, some outputs are not optimal, and these outputs require further improvement. These outputs and suggestions for future research are described below:

Etch back stop

By over etching, the silicon that was etched away was deposited on the walls of the chamber of the machine. The first improvement suggested is using SiO_2 as an etch back stop in order to reduce the depositing of etch residues. The etch rate of SiO_2 is significantly lower than the etch rate of silicon for the etch recipe that was used.

Machine with temperature feedback and cooling

Another improvement would be to use a machine with temperature feedback and with a cooling function for the evaporation of aluminum. With this solution, the process time could be reduced as the process does not have to be stopped to let the wafers cool down. The machine used for sputtering has temperature feedback together with a cooling function.

Improvement related to cell research

Regarding the cell research, an improvement would be to reduce the adhesion of fibronectin to the walls of the pores. This can be achieved by using an etch recipe with higher power, which reduces the surface roughness of the walls.

5. Summary and future work

5.1 Summary

This master project is the continuation of the work of Quirós-Solano *et al.*, partially presented in[1]. Their work has shown that it is possible to create PDMS scaffolds for OOC applications, with standard MEMS fabrication processes. They originally created a 9 μm-thick membranes with pore sizes of 8 μm and pore to pore distances of 1 μm. By extending the PDMS etching time, they could create lateral gaps in the walls between the pores and therefore create a scaffold. The high porosity of this scaffold makes them useful in OOCs. In this work it is investigated whether it is possible to fabricate these scaffolds tuning other fabrication parameters, besides extending the etching time. Therefore, a literature review on PDMS etching with ICP reactors is conducted. From this review, the most important process parameters of ICP etching were determined. These parameters are: the bias power, chuck temperature and pressure. Subsequently, the proposed research objectives are:

- Replicating the scaffold fabricated by Quirós-Solano et al.;
- Quantifying the effect of process parameters on the lateral and vertical etch rates;
- Tuning the porosity of the membrane.

Besides presenting a new technique to fabricate highly porous PDMS membrane, Quirós-Solano *et al.*[39] introduced a novel process flow to transfer thin (<10 μm) PDMS membranes onto microfluidic devices. The process of transferring a membrane was improved compared to the standard method, resulting in less misalignment and breakage of the membranes. In order to transfer the membrane, they added a sacrificial layer of PAA between the silicon wafer and the PDMS membrane. However, their process flow could not be used to create thick transferrable membranes, as requested by multiple OOC applications and by the biological partner in this project (TU/e). Therefore, another research objective was to adapt the process flow in order to fabricate 20-μm thick transferrable PDMS membranes.

The thesis is divided in three parts.
Chapter 2 investigates the effect of temperature on PDMS structures during PDMS etching. First, a simulation was performed to test if a pure anisotropic etch could create the lateral gaps between the walls of the pores in the PDMS membrane as observed by Quirós-Solano *et al.* During etching, the wafer temperature increases, and the wall of the pores expands due to thermal expansion. If the walls expand beyond the aluminum mask, the walls are etched. After cooling, the walls contract and as material is has been etched, as a result the walls will be concave instead of straight. When the wafer temperature reached 200°C, the lateral wall removal was 0.09 μm. This is considered to be too small to be responsible for the lateral gaps between the pores. A second simulation was performed to estimate the temperature of a wafer during etching. During this simulation, the chuck temperature and the heat flux due to etching were used as input parameters as they determine the temperature of the wafer. The temperature of the wafer reached 36°C with this simulation. This was lower than the temperature set at the first simulation and therefore it is unlikely that the process described in the first simulation is indeed what was observed by Quirós-Solano *et al.*
To validate the simulations, the wafer temperature was also empirically determined. The results of that test showed that the wafer temperature was below 40°C during etching and that the wafer temperature is dependent on the chuck temperature and the bias power. Therefore, it can be concluded that the second simulation gave a good estimation of the wafer temperature.

In Chapter 3, the influence of the process parameters on the vertical and lateral etch rate was determined. In the first experiment, the process of Quirós-solano *et al.* was repeated. However, an etch stop was required and therefore a small adaption was made. The sacrificial PAA layer was replaced by a silicon oxide layer to create a reliable etch stop. Unfortunately, the state of the etching tool made it impossible to replicate the membranes exactly. Moreover, the process time had to be extended even further to replicate the results. Furthermore, the gaps in the walls appeared before the PDMS was completely etched in the vertical direction. In order to prevent the early-formation of the gaps, the research objective was changed to: find the parameters that could reduce the lateral etch rate and thus reduce the isotropicity of the etch.
In the second experiment, the influence of process parameters was tested. It was shown that (i) an increase in bias power gave a higher vertical and lateral etch rate, (ii) an increase in pressure decreased both the vertical and the lateral etch rate and (iii) a decrease in temperature increased the vertical etch rate.
Furthermore, it was shown that the combination of an increase in pressure together with an increase in bias power reduced the lateral etch rate, while it increased the vertical etch rate. This last combination resulted in the lowest isotropicity of all the recipes tested. The highest isotropicity and lateral etch rate was created with a bias power of 30 W at half gas flow. The highest vertical etch rate was with the 50 W recipe.
In the third experiment, it was shown that with the standard recipe presented in unpublished work by Quirós-Solano *et al.* the gaps in wall appeared before the membrane was etch through as already seen in the first set of experiments. However, with the knowledge gained from the second experiment, the membrane could be etched through before the gaps in the sidewalls appeared by using a recipe with higher bias power and pressure.

In Chapter 4, the process flow of Quirós-solano *et al.* was adapted to create thicker membranes that could be transferred by their method as well. One of the most relevant adaptions was to replace aluminum sputtering with aluminum evaporation, as sputtering is not allowed on thick PDMS membranes. Furthermore, the evaporation step was optimized and included in the process. The membranes were successfully fabricated and employed by TU/e in their biological research. They tested the influence of cell strain on cell proliferation. In their research, they used a Flexcell device which has a rubber membrane that can be stretched. The thick PDMS membranes was placed upon the rubber membrane and the pores were used as microwells in which the cells were seeded. Fibronectin was used to improve the adhesion of the cells on the bottom of the microwells. Unfortunately, the fibronectin strongly adhered onto the walls of the pores instead of the bottom surface of the microwells due to the surface roughness of the membrane. Therefore, the cell research was discontinued.

5.2. Recommendations for future work

The membranes and scaffolds should be further improved before being successfully used in OOC applications. Firstly, in order to transfer the highly porous membranes presented in Chapter 3, the sacrificial layer of PAA has to be reintroduced. Additionally, it is recommended to keep the SiO_2 layer as an etch stop underneath the PAA.
In this study, no simulations or measurements were done to determine whether the scaffolds are strong enough to be used in an OOC. With the array of lateral gaps between the pores, the mechanical strength is very likely reduced, and the scaffold might break during the cyclic stretching of the scaffold during OOC application. Therefore, it is recommended to test the mechanical strength of the scaffold.
The sidewalls of the PDMS membrane created in Chapter 4 were very rough and therefore fibronectin adhered to the walls of the membrane and not to the bottom surface of the

rubber membrane. A solution to reduce the surface roughness is to use an etch recipe with a higher bias power. It is recommended to test if this indeed will reduce the adhesion of fibronectin to the side walls. The fabrication time of the PDMS membranes could be further reduced if the membranes could be cooled during the evaporation of the aluminum. Reduction of fabrication time reduces the cost of fabrication.

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