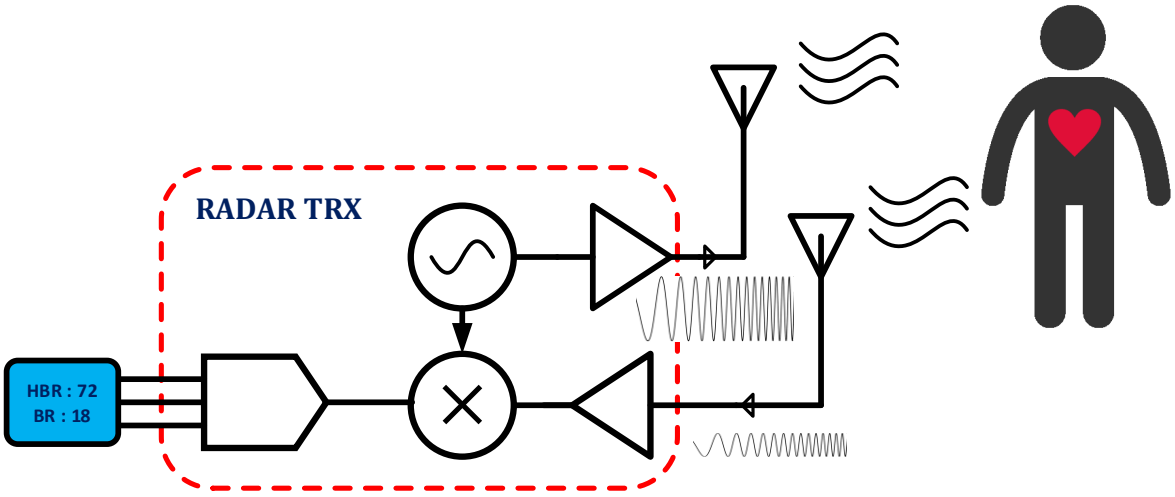
Design of Frequency locked loop and Receiver front-end for Burst-Chirp UWB Radar Transceiver for Vital Signs and Occupancy Sensing by monitoring the respiration and heartbeat rate



MASTER OF SCIENCE THESIS

For the degree of Master of Science in Electrical Engineering
at Delft University of Technology

Sunil Sheelavant

November 22, 2018

Faculty of Electrical Engineering Mathematics and Computer Science (EEMCS).
Delft University of Technology

Supervisors:	Dr. Masoud Babaie	TU Delft
	Dr. Yao-Hong Liu	IMEC-NL
	Dr. Marco Mercuri	IMEC-NL

Committee members:	Prof. dr. L.C.N. de Vreede	TU Delft
	Prof. dr. A. Yarovoy	TU Delft
	Dr. Masoud Babaie	TU Delft
	Dr. Yao-Hong Liu	IMEC-NL
	Dr. Marco Mercuri	IMEC-NL

Contents

Acronyms

ADC	-	Analog to digital converter
BW	-	Bandwidth
C	-	Velocity of light
CMOS	-	Complementary metal-oxide-semiconductor
CW	-	Continuous wave
DAC	-	Digital to analog converter
DCO	-	Digitally controlled oscillator
EIRP	-	Equivalent isotropically radiated power
ETSI	-	European Telecommunications Standards Institute
FCC	-	Federal Communications Commission
FCW	-	Frequency command word
FLL	-	Frequency Locked Loop
FMCW	-	Frequency modulated continuous wave
FPGA	-	Field programmable gate array
Gm	-	Trans-conductance
GND	-	Typical name for ground (zero reference)
HPF	-	High pass filter
I/Q	-	In-phase/Quadrature phase
IC	-	Integrated circuit
IF	-	Intermediate frequency
KCC	-	Korea Communications Standards Commission
LDO	-	Low dropout
LNA	-	Low noise amplifier
LNTA	-	Low noise trans-conductance amplifier
LO	-	Local oscillator
LPF	-	Low pass filter
LSB	-	Lease significant bit
MSB	-	Most significant bit
NF	-	Noise figure
OTW	-	Oscillator tuning word
PA	-	Power amplifier
PCB	-	Printed circuit board
PD	-	Phase detector
PLL	-	Phase locked loop
PRF	-	Pulse repetition frequency
PRI	-	Pulse repetition interval
PSD	-	Power spectral density
PVT	-	Process voltage temperature

Q	-	Quality factor
RADAR	-	Radio detection and ranging
RCS	-	Radar cross section
RF	-	Radio frequency
RF-FE	-	Radio frequency front end
RX	-	Receiver
SDM	-	Sigma delta modulator
SNR	-	Signal to noise ratio
SPI	-	Serial peripheral interface
TIA	-	Trans-impedance amplifier
TSPC	-	True single-phase clock
TX	-	Transmitter
UART	-	Universal Asynchronous Receiver/Transmitter
UWB	-	Ultra-wideband
VDD	-	Typical name for supply voltage

Abstract

While there are many technologies and electronic systems used to detect the human vital signs by monitoring the heart beat rate & respiration rate, all these systems rely on physical contact with the human body. Furthermore, each measuring system can only be used for a single person thus increasing the cost and complexity of integrated systems to monitor many persons simultaneously. For remote vital signs and occupancy detection in many smart home/building applications, radar sensors are a preferred option over cameras, due to privacy preservation and robustness to ambient light conditions. These radars not only need to provide precise range and vital signs information over meters distance, but also preferably can operate on a battery up to a few months or even years, for cost and practical reasons (like smoke detectors). This project aims at sensing the vital signs and estimating the heart beat rate and respiration rate with no physical contact with the person and single system can be employed to monitor the parameters for multiple persons powered by battery that can last for months. Thanks to radar technology and signal processing algorithms that enable to implement such a hardware efficiently.

In this work [1], the fast settling frequency locked loop(FLL) and Receiver front-end are designed and evaluated for the radar transceiver following the various design trade-offs obtained by comprehensive system simulations to derive the specifications for the related circuit design blocks in 40 nm CMOS technology to detect the vital signs of multiple persons as close as 20 cm till the distance of 15m from the radar system by consuming a total average power of 680µW and satisfying the spectral regulations in US, Europe, Korea, China and Japan.

List of Figures

Chapter 1 Introduction

While many conventional techniques have been employed for measurement of heart beat rate and vital sensing, this project aims at vital sign detection without being in physical contact with the person to estimate the of parameters of heart beat rate and respiration rate. This single system can be employed to monitor multiple people as close as 20 cm.

1.1 Current systems for vital sign monitoring

One of the current systems is shown in Figure 1.1 [2]. This system is used in the hospitals for monitoring the heart beat rate and the respiration rate of the patient. This system relies on the sensor which is attached to the patient's finger and remains in contact with the patient all the time. The signal from the sensor is routed to acquisition electronics where it is adapted to suitable voltage levels of electronic systems placed near the patient. However, such a system is not completely reliable since there exists a possibility of sensors being detached in the scenarios like sleep which can lead to potential loss of life.

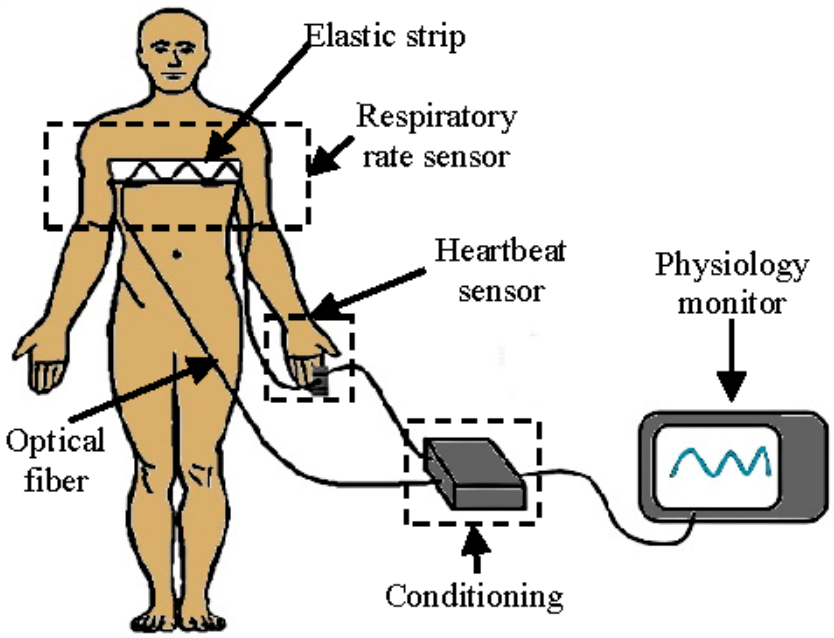


Figure 1.1 Conventional respiration rate & heart beat rate monitoring system-1 [2].

In another approach as shown in Figure 1.2 [3], the system is designed with wireless communication capability, hence the signal captured by the sensor and data is transferred to an electronic system for conditioning, acquisition and displaying the data

in the form that the doctor can understand. However, such a system needs the sensor to be in physical contact with a human being and requires a battery-powered wireless sensor node to be attached to the human body.

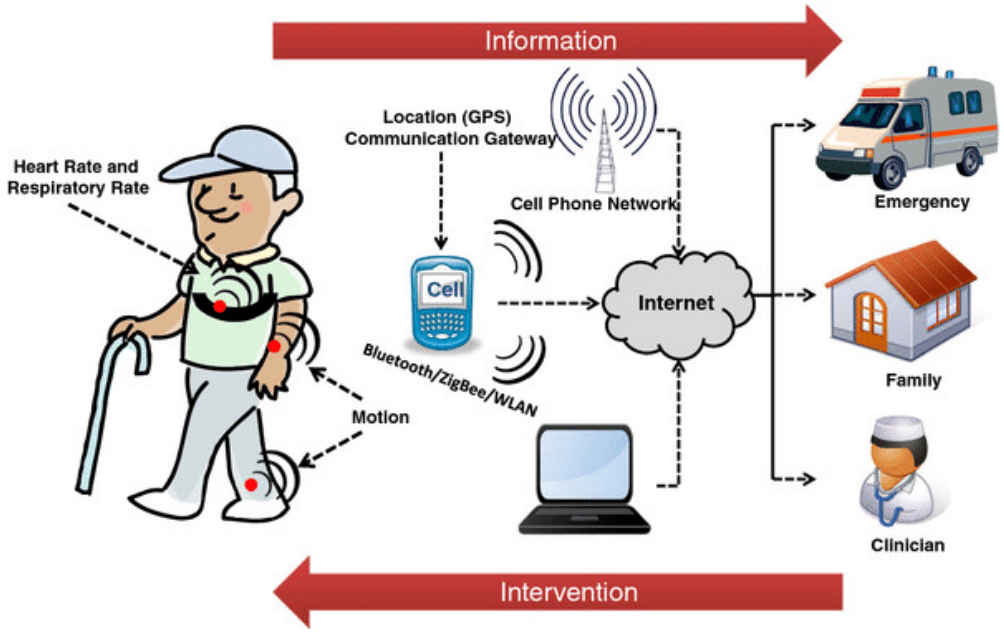


Figure 1.2 Wireless monitoring of respiration and heart beat rate [3].

This project aims to develop a non-contact system for monitoring the respiration and heart-beat rate of multiple persons in the room. One of such scenarios is shown in Figure 1.3.

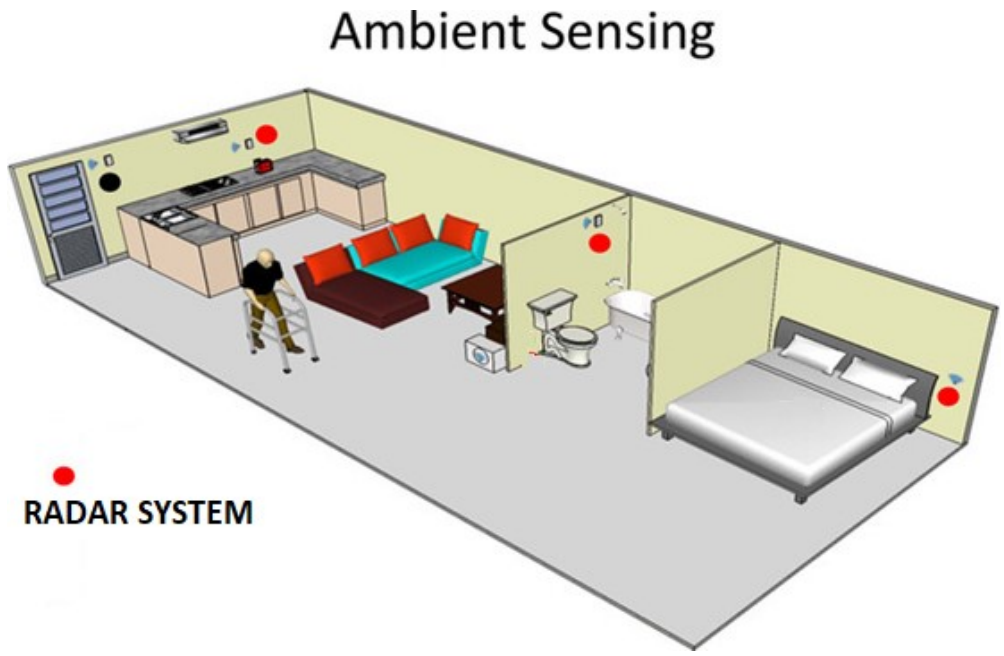


Figure 1.3 Proposed method for ambient sensing using radar.

Radar systems installed in the rooms and powered with batteries are continuously monitoring the heart-beat rate and respiration rate.

The benefits of applying radar-based vital sign monitoring compared to other technologies (example of camera-based technology) as follows:

- ✓ Independent of the environment and lighting:
  In conventional sensor based vital monitoring systems, the sensor response can be a function of the environment like temperature, humidity and cannot be operated in ambient light conditions when considering the camera-based technology, while the radar operation is entirely independent of such variations.

- ✓ Privacy conserving
  While there are technologies to extract the information from continuous capturing of the frames in the form of video and extract the information on the small periodic movement of the chest, these systems do not preserve the privacy of the human beings.

- ✓ Good penetration property (for through - wall detection)
  Since the radar system relies on transmission and reception of electromagnetic waves which can penetrate the obstacles like walls, the system can be used for the vital monitoring and presence of human beings in remote rooms. One such application can be disaster management and military combat management to detect the presence of an opponent.

- ✓ Speed detection capability
  The radar operation basically relies on frequency shifts due to the movements of the target. Hence, can be helpful in the possible scenarios like fall detection, irregular events for the elders who are not able to move and inform in case of un-foreseen accidental circumstances.

- ✓ 3-D localization
  The radar provides the information on range and movement. Employing the radar signal processing algorithms and plotting the processed data on a suitable display can provide spatial information's in terms of azimuth and elevation.

- ✓ Large coverage
  A single radar system can be employed for monitoring the multiple people and signal processing can be used to differentiate the ranges of persons to display the processed information in an understandable format.

- ✓ Reduced Bill of Materials(BOM) with a higher level of integration:
  A single chip with minimum number of off the shelf components assembled on a PCB achieves a highly integrated system with a minimum

bill of materials compared to conventional bulky complex electronics systems.

The functional block diagram of the system is as indicated below:

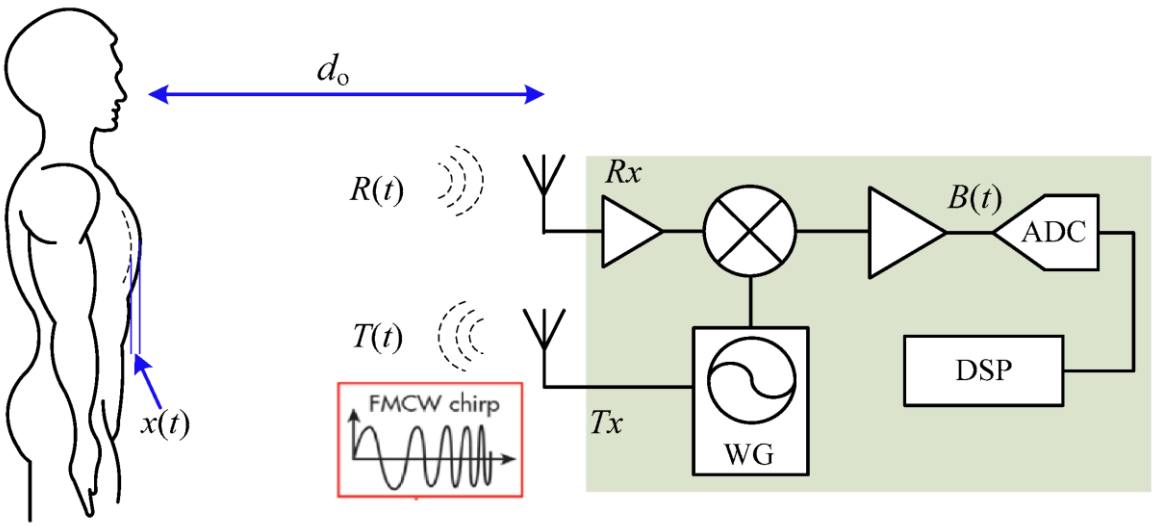


Figure 1.4 Functional block diagram of the radar.

The radar consists of Transmitter which radiates the electromagnetic energy by transducing the frequency modulated signals, called chirps, which are reflected by a person. The Doppler shift caused by the mechanical movements of the heart and lungs on the chest wall surface can be detected and in this way heart beat rate and respiration rates can be measured. The received signals are mixed with copies of the transmitted signals (i.e., LO signals) obtaining intermediate frequency signals B(t) (called beat signals) whose phase changes continuously due to mechanical movement of the chest wall surface. The vital signs information (heart-beat and respiration rate) can be determined by extracting the phases of the consecutive intermediate frequency signals B(t). In doing that, those signals are the first digitized using an analog-to-digital converter (ADC) controlled by an FPGA which also transfer the data to a PC for digital signal processing.

While the current are radar systems realized on chip previously for vital signs detection [4] [5] consume relatively high power and cannot be powered from the battery, this work contrasts current state-of-art reducing the average power consumption by 100 times and achieving a longer-range detection with better range resolution.

1.2 Research contribution

The Thesis first focuses on the design and analysis of the optimum transmitted wave-form satisfying spectral mask specifications of various international telecommunication standards like FCC, ETSI, KCC. Furthermore, comprehensive system simulations are carried out to understand various trade-offs in radar system design and estimate the effect of circuit non-idealities on the system performance. The dissertation then concentrates on the circuit implementation of radar's different blocks.

In the first phase of the project, a power efficient frequency locked loop is designed with settling time less than 10 µs while consuming 625 µW. In the second phase of the project, the radar receiver front end consisting of low noise amplifier and mixer is designed consuming 6 mW which is integrated with baseband signal processing chain leading to total power consumption of 19 mW and average power consumption of 680µW by the entire radar transceiver while detecting the respiration rate up to 15 meters and heart beat rate up to 6 meters with a range resolution of 20 cm.

1.3 Thesis outline

The thesis is organized as follow. Chapter 1 introduces the current systems used for vital sign detection. Chapter 2 gives an overview of types of radar systems. Chapter 3 deals with system level simulations and derivation of key specifications while introducing to the radar terminologies. Chapter 4 describes the transmitter architecture and FLL design and Implementation along with simulation results. Chapter 5 describes the receiver focusing on receiver front-end designed and integrated with baseband signal processing circuits. Chapter 6 describes the measurement set-up with FPGA Interface and measurement results. Chapter 7 is reserved for conclusions and suggestions for future development.

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Chapter 2 Introduction to Radar Systems

This chapter gives a brief introduction to radar systems and an overview about the types of radar systems.

2.1 Radar and Its classification

The word RADAR stands for Radio Detection and Ranging. It is an electronic system that uses the high frequency modulated signals and directive antennas to transmit and receive an electromagnetic energy into a specific volume where targets are present in the space. The targets in this space reflect the portion of incident energy (generally referred as echoes or radar returns) in the direction towards the radar. The information such as range, velocity is derived by processing the echoed signals received by the radar receiver.

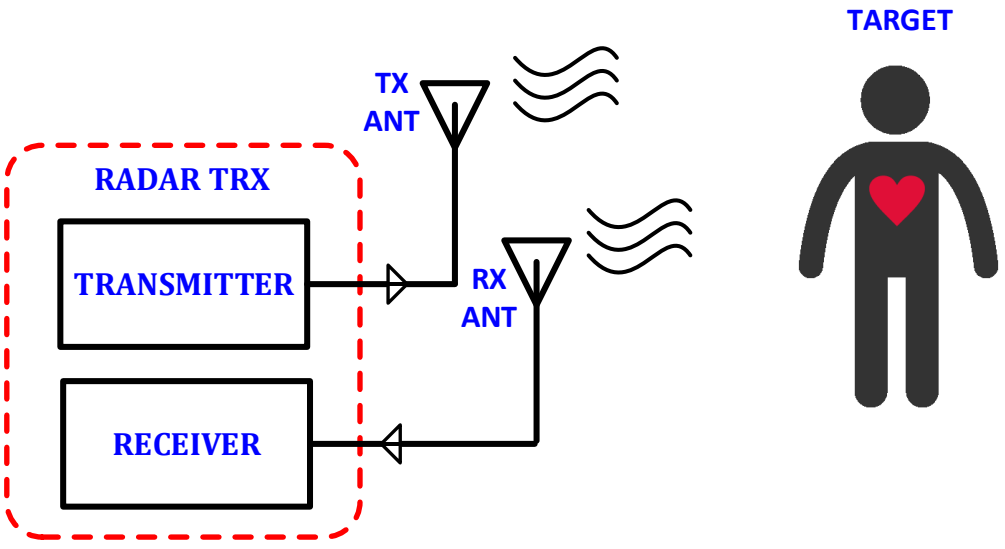


Figure 2.1 block diagram of the radar system.

Figure 2.1 shows the general block diagram of a radar system.

The main blocks of the radar are

1. The transmitter which generates the frequency modulated wave-form and amplifies it to a reasonable amplitude.
2. Transmit-antenna which acts a transducer between the transmitter and space converting the electrical signal into the electromagnetic waves.
3. Receive-antenna which acts as a transducer to convert echoed electromagnetic waves back to electrical energy and
4. finally, the receiver which conditions the low amplitude signal to optimum signal level by amplification and frequency translation which is finally digitized to run the signal processing algorithms to extract the information about the targets.

2.2 Classification of Radar systems based on type of transmit waveform

When the type of waveform is used as a classifier of radar systems, there are two types of radars namely CW Radar system and Pulsed radar system.

2.2.1 Continuous wave (CW) Radars

Continuous wave radars are those that continuously emit electromagnetic energy and receive the reflected signals from the moving targets. Unmodulated CW radars can accurately measure target radial velocity (Doppler shift) and angular position. Continuous wave waveforms can be viewed as pure sinewaves of the form $\cos(2\pi \cdot fo \cdot t)$. Spectra of the radar echo from stationary targets and clutter will be concentrated around fo. The center frequency for the echoes of a moving target will be shifted by fd, the Doppler frequency. Thus, by measuring this frequency difference, CW radars can very accurately extract target radial velocity. Because of the continuous nature of CW emission, range measurement is not possible without some modifications to the radar operations and waveforms. Target range information in fact cannot be extracted without utilizing some form of modulation. The primary use of CW radars is in target velocity search and track like autonomous driving cars, and in missile guidance operations.

2.2.2 Pulsed Radar system

Pulsed radar uses a train RF modulated pulsed waveforms. Using pulsed operation, - gives a time stamping by which the range information about the target can be extracted. In this category, radar systems can be classified based on the Pulse Repetition Frequency (PRF), as low PRF, medium PRF, high PRF, and Dual PRF radars.

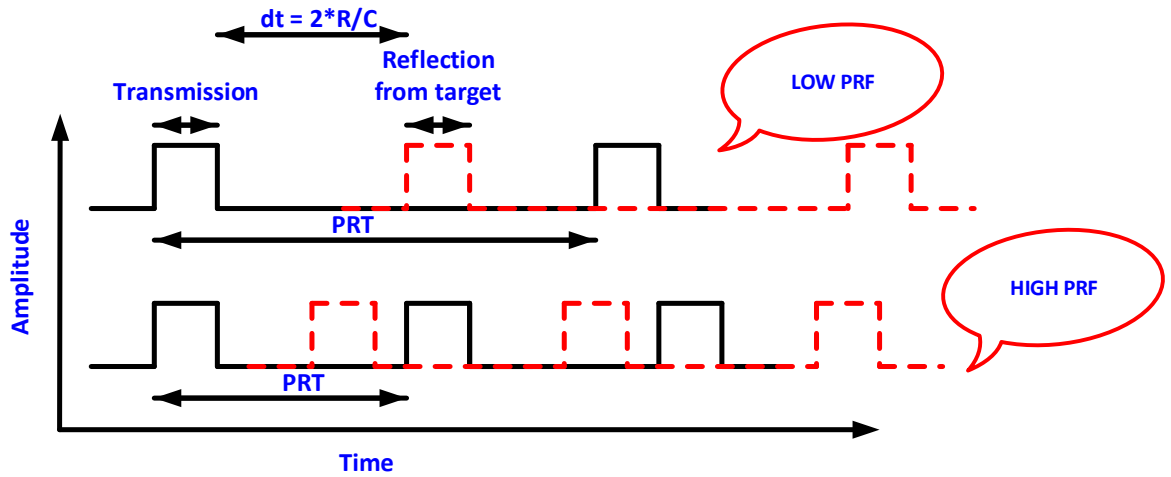


Figure 2.2 Pulse repetition frequency cases.

- Low PRF radars are primarily used for ranging where target velocity (Doppler shift) is not of interest.

- High PRF radars are mainly used to measure target velocity. Continuous wave as well as pulsed radars, can measure both target range and radial velocity by utilizing different modulation schemes.

- Dual PRF radars combines the advantages of both high PRF and Low PRF systems to estimate range and velocity.

2.2.3 Frequency Modulated Continuous Wave FMCW Radar

FMCW Radar is a special case of continuous wave radar that radiates power over a time like continuous wave radar, except that FMCW radar changes its operating frequency during the transmission and measurement. In other words, the transmission signal is frequency modulated. The extraction of information like range, and the velocity of the target relies on the property of instantaneous change in the frequency.

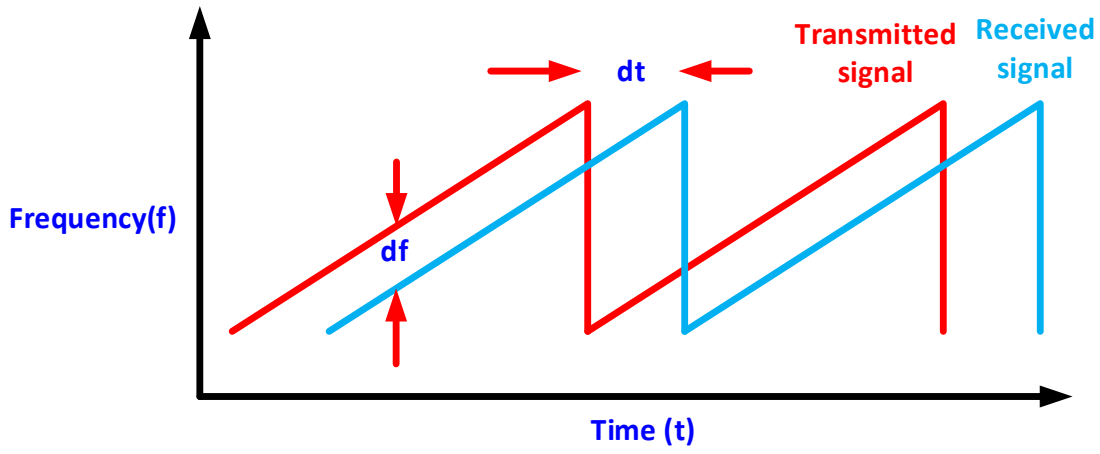


Figure 2.3 FMCW radar frequency profile versus time.

It would not be possible to determine the target range without frequency modulation since it lacks the time stamp necessary to determine the time required for the entire transmit and receive cycle. The round-trip time of the signal over the range R would be $2R/c$. c being the velocity of light.

The range is calculated as

$$Range = \frac{2 * dt}{C} = \frac{C}{2} * \frac{df}{(BW/Tc)} \qquad \text{Equation 2.1}$$

The velocity can be measured from the phase shift from multiple and consecutive chirps.

Chapter 3 Waveform Design and System specifications

This chapter introduces to FMCW principle of radar operation after which the key specifications are derived regarding system requirements along with introduction to key radar terminology.

There is an increasing demand for radars in indoor applications that also happen to have strict regulations on transmit emissions. Often the peak transmit power is limited in these areas. So, the job for the radar is to somehow illuminate its targets using longer pulses at lower power. The problem, of course, is that a simple long pulse lacks the ability (bandwidth) to discern targets in range. The remedy is to increase the Tx bandwidth by modulating in frequency, so that a reasonable range resolution is restored. The exceptional fidelity of the radar wave form generation module can accomplish this without introducing any of the spurious modulation components. The resulting wave form is shown below in Figure 3.1 in time.

3.1 FMCW Theory

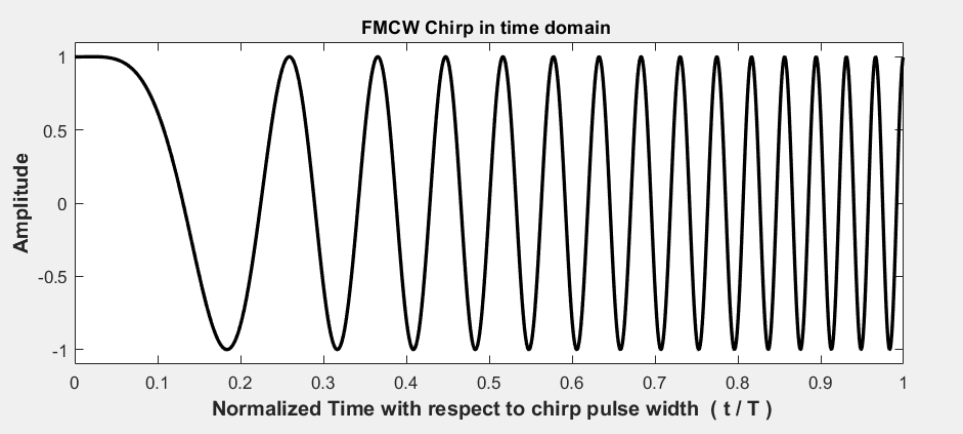


Figure 3.1 Time domain waveform of FMCW chirp over the chirp pulse width showing the frequency variation.

Figure 3.2 shows the variation of instantaneous frequency of transmitted signal (in blue) and reflected signal (in red).

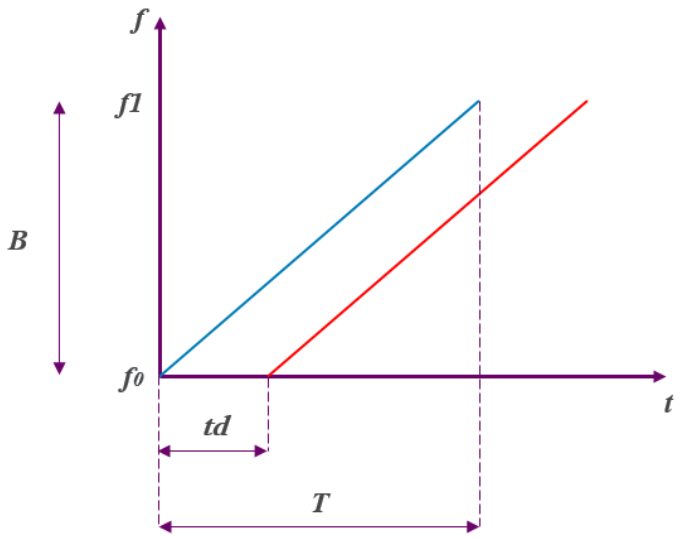


Figure 3.2 Single FMCW chirp- showing the variation of frequency over the duration of pulse width.

A linear FMCW radar transmits a waveform, called chirp, whose instantaneous transmitting frequency ft varies linearly over time (the blue trend in Figure 3.2).

Instantaneous frequency of transmitting signal can be expressed as:

$$f_t = f_0 + \frac{B}{T}t \qquad \text{Equation 3.1}$$

where f_0 is the initial frequency of the chirp, B is the total band of the waveform, while T is the chirp duration. B/T is defined as ***sweeping rate***. The corresponding phase is:

$$\phi = 2\pi \int_0^t f_t dt = 2\pi\left(f_0 t + \frac{B}{2T}t^2 \right) \qquad \text{Equation 3.2}$$

The transmitting signal $T_s(t)$ can be expressed as:

$$T_s(t) = A\sin\left[2\pi\left(f_0 t + \frac{B}{2T}t^2 \right) \right] \qquad \text{Equation 3.3}$$

A target reflects it at a distance Do. Assuming a stationary target, the reflected signal R(t) (the red trend in Figure 3.2) can be expressed as:

$$R(t) = B(t)\sin\left[2\pi\left(f_0 (t - t_d) + \frac{B}{2T}(t - t_d)^2 \right) \right] \qquad \text{Equation 3.4}$$

where

$$t_d = \frac{2D_0}{c} \qquad \text{Equation 3.5}$$

t_d - Round-trip time required for transmission and reception of an echo from the target.
c - Velocity of light.

Mixing $T_s(t)$ and $R(t)$ and following a low-pass filter results in a *beat signal BS(t),* can be expressed as:

$$BS(t) = C(t)\cos\left[2\pi\left(\frac{2BD_0}{cT}t + \frac{2f_0D_0}{c} + \frac{B}{2T}\left(\frac{2D_0}{c}\right)^2\right)\right] \quad \text{Equation 3.6}$$

The only time-varying term is the first which is called ***beat frequency f_b***. The other two terms are phase components. The squared term is essentially zero especially for short-distances. This means that Equation 3.6 can be expressed as:

$$BS(t) \approx C(t)\cos\left[2\pi\left(\frac{2BD_0}{cT}t + \frac{2f_0D_0}{c}\right)\right] \quad \text{Equation 3.7}$$

This means that for a static target, the resulting baseband signal is a sinusoidal waveform whose frequency (*beat frequency*), depending on the target's absolute distance, is $2BD_o/cT$ and the initial phase is $2f_oD_o/c$. As will be clear later, the *beat frequency* will be used to determine the target's absolute distance while the initial phase will provide the Doppler information. Although the initial phase also depends on the range D_o, this information cannot be used to determine the target's absolute distance, while it can be used to determine the Doppler, as in a pure CW radar. In fact, $2f_oD_o/C$ is periodic of 2π, meaning that the maximum unambiguous range will be $D_o=c/(2f_o)$, which is few millimeters/centimeters at microwave frequencies.

In case of moving target with the velocity '*v*' m/s, the target's absolute distance becomes D = $D_o + v{\cdot}t$, and the ***beat signal*** can be expressed as:

$$BS(t) = C(t)\cos\left[2\pi\left(\frac{2BD_0t}{cT}\left(1-\frac{2v}{c}\right) + \frac{2f_0vt}{c} + \frac{2Bvt^2}{c}\left(1-\frac{v}{c}\right) + \frac{2D_0}{c}\left(f_0 - \frac{BD_0}{cT}\right)\right)\right] \quad \text{Equation 3.8}$$

This generates range/velocity ambiguities. In fact, the distance to a target is calculated from the received frequency shift. In the case of moving target, there will also be a frequency shift because of the Doppler effect. This makes hard to say if the range or the velocity causes the shift. However, considering human speeds, if the chirp duration *T* is made sufficiently short, it can be assumed that the target speed is essentially o m/s during T, meaning the target is frozen at D_o.

This means that Equation 3.8 can be approximated as Equation 3.7. This statement can be easily demonstrated by simulations and experiments and no range/velocity ambiguity is experienced.

To reduce the range/velocity ambiguities, the FMCW signal consists of linear up-sweep and down-sweep. It is observed that in the case of Doppler shift, a higher velocity causes greater frequency shift during the up-sweep and smaller frequency shift during the down-sweep. So, by exploiting both the up-sweep and the down-sweep, the Doppler

shift can be separated from the range-induced shift. This way, the FMCW radar is capable of both range and velocity measurements, but only when a symmetrical sweep is used. However, this technique works well if the target is moving at a constant speed during the waveform transmission, like in automotive applications. This cannot be always assumed for human movements. For that reason, the previous idea considered to work much better.

3.2 System Requirements

3.2.1 Range resolution

Considering the indoor room situation, where multiple persons can be as close as 20 cm, the radar should be able to resolve between two closely spaced persons as 20 cm. Hence the range resolution of the radar was chosen to be 20 cm.

3.2.2 Bandwidth

After knowing the range resolution (ΔD), It directly determines the bandwidth of the radar as follows in accordance with FMCW theory [6],

$$B = \frac{C}{2\Delta D} = 750 \text{ MHz} \qquad \text{Equation 3.9}$$

3.2.3 Potential frequency bands

With the use case of presence detection in the smart building context, it is most desirable to use globally available ISM band for the radar. If we take a close look at the potential frequency bands with the desired band width of 750 MHz for the range resolution of 20cm, there are mainly the following options:

- UWB
- 60GHz ISM band/ unlicensed band
- 120GHz ISM

The table below shows the potential frequency bands that can use available bandwidth. We can observe that attenuation is higher as we go up in the frequency through the frequency bands are available and increases the design complexity and power consumption of the radar operation at very high frequencies.

	UWB (7-8 GHz)	60 GHz ISM	60GHz unlicensed	122 GHz ISM
Power limit (Indoor)	0 dBm	20dBm	10 dBm	20 dBm
Bandwidth	1 GHz	500 MHz (61-61.5 GHz)	7 GHz (57 – 64 GHz	1 GHz (122-123 GHz)
Range Resolution (C/2*BW)	15 cm	30 cm	2 cm	15 cm
Attenuation on Reflected signal for target @ 10m with RCS [7] = 1 m²	101.5 dB (@ 8 GHz)	119 dB (60 GHz)	119 GHz (@ 60 GHz)	127 dB (@ 120 GHz)

Table 3.1 Potential frequency bands available [8] [9].

when we overlap the regional regulation on EIRP for UWB as shown in the Figure 3.3, It can be found that the sub-band from 7.25GHz to 8.5GHz is available in all the regions with highest Equivalent Isotropically Radiated Power (EIRP) limit of -41.3dBm/MHz. EIRP is the product of transmitter power and the antenna gain in a given direction relative to an isotropic antenna of a radio transmitter Furthermore, starting frequency of 7.4 MHz is chosen to with margin on the lower side with bandwidth of 750 MHz fulfilling the tough UWB spectral requirements with a peak power of odBm/50 MHz, average power of -41.3 dBm/MHz and side band power level below -70 dBm/MHz.

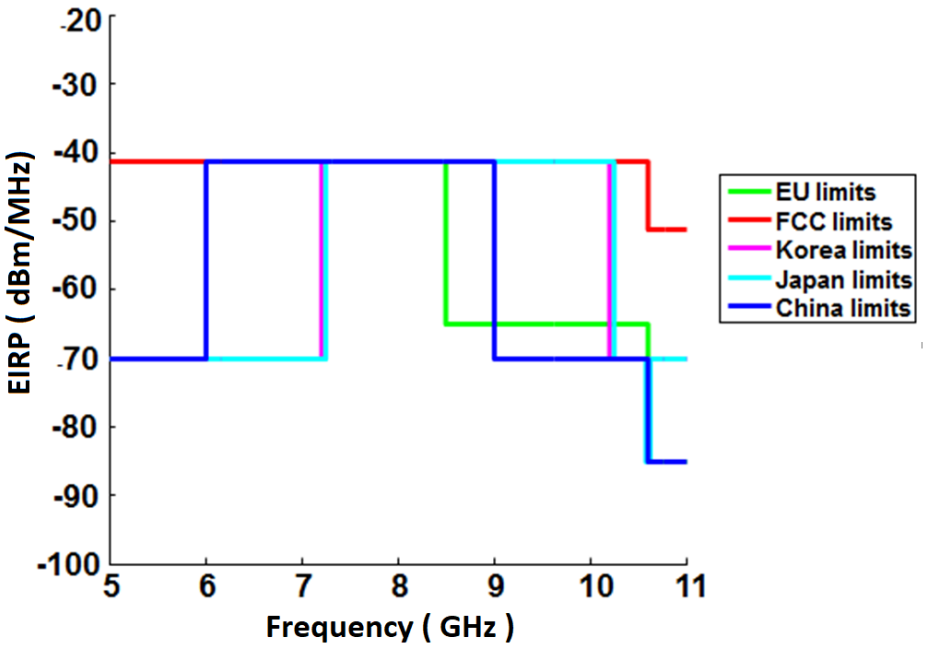


Figure 3.3 spectral mask requirements in different regions [8] [9].

To simultaneously satisfy UWB spectrum requirements and reach the longest range, the maximum output power specifications of Power Amplifier (PA) to be 0 dBm. The analysis of the continuous FMCW with peak power of 0 dBm whose frequency profile shown in the Figure 3.4 and spectrum shown in the

Figure 3.5 with Power Spectral Density(PSD) of -28.750 dBm/MHz, clearly indicates that the necessity to reduce the average power to fulfill the UWB spectral requirement. Since the radar system is a using EM spectrum in UWB and needs to co-exist with available wireless communication systems, it must comply with the regulations from telecommunication regulatory bodies like FCC in the United States, ETSI in Europe, KCC in Korea for the acceptance of the system internationally. So, we need a duty-cycling to reduce the average power spectral density below -41.3 dBm/MHz

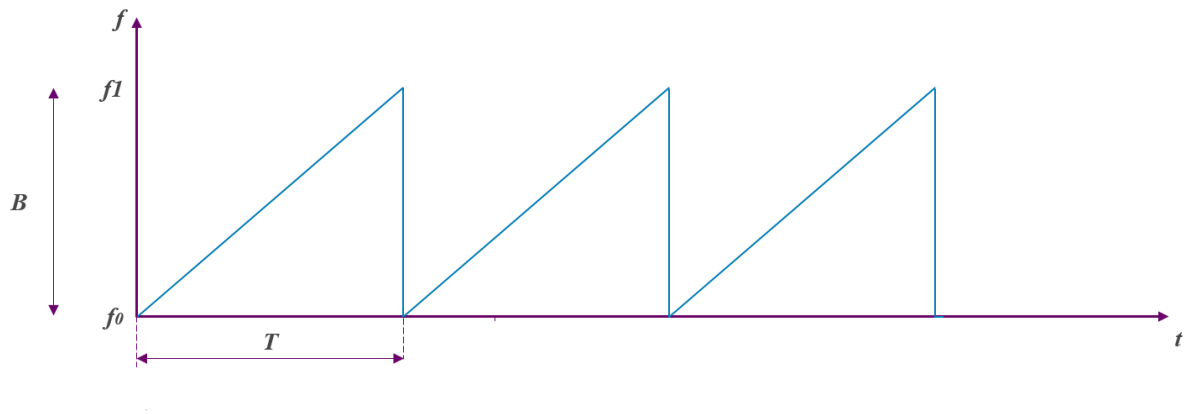


Figure 3.4 FMCW-sawtooth signal pattern (frequency v/s time).

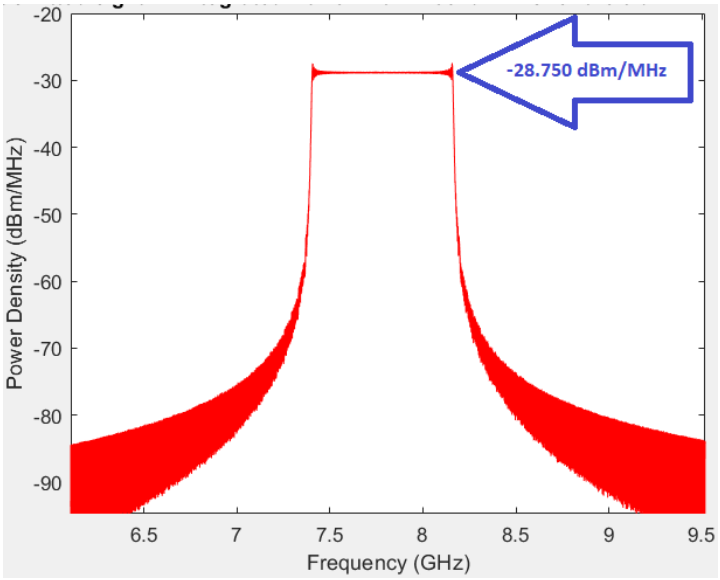


Figure 3.5 PSD of FMCW-sawtooth signal pattern.

3.2.4 Necessity of duty-cycling in addition to FMCW.

After understanding the peak power and average power regulations, it is necessary to reduce the average power from -28.750 dBm/MHz to below -41.3 dBm/MHz, we need to reduce the average power by duty-cycling.

$$10 * log\left(\frac{T_C}{T_{PRI}}\right) < \{(-41.3\ dBm/MHz) - (-28.750\ dBm/MHz)\}$$ Equation 3.10

$$10 * log\left(\frac{T_C}{T_{PRI}}\right) < -12.55$$

$$\left(\frac{T_C}{T_{PRI}}\right) \quad < \quad 0.0556$$

Where, Tc and T_{PRI} are respectively the chirp period and the pulse repetition interval. With some margin and to exploit the advantages of short Tc, selected Tc = 0.03 T_{PRI}

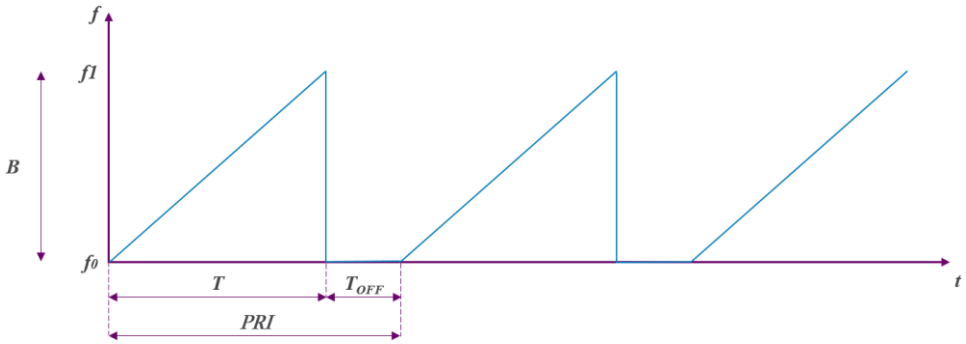


Figure 3.6 Series of multiple linear chirps indicating frequency v/s time.

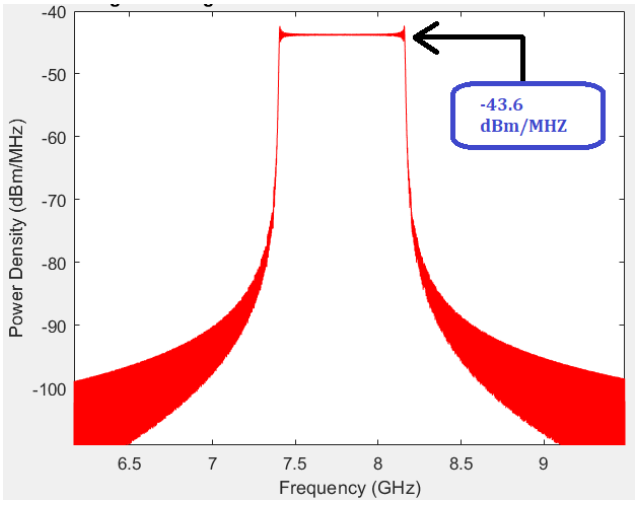


Figure 3.7 spectrum of transmitted signal after duty-cycling.

Figure 3.6 shows the frequency profile over time after duty cycling and Figure 3.7 shows the power spectral density after duty cycling which meets the spectral regulations on the average power level.

3.2.5 Chirp period and PRI selection.

The velocity of the target that the radar can detect is limited by sampling time (Ts=1/PRF).

General equation for Doppler frequency $f_D = 2 * V_r * \frac{f_{tx}}{C}$

For the unambiguous detection of radial velocity(V_r), $PRF > f_D$

$$Vr < C * \frac{PRF}{2 * f_{tx}}$$ Equation 3.11

Above equation is valid if the direction of doppler shift is known.
If the direction of doppler is unknown which is generally the case,
The unambiguous velocity (without folding):

$$V_u = \frac{C}{f_{tx}} * \frac{PRF}{4} = \frac{\lambda}{4*Ts}$$ Equation 3.12

Good choice of PRF to achieve a long unambiguous range will be a poor choice of low unambiguous velocity and vice versa. The maximum unambiguous velocity of the targets determines the required pulse repetition interval (PRI) in FMCW radars. The fastest possible movement of an indoor object with doppler velocity up-to 7 m/s.

$$\left(\frac{\lambda}{4 * T_{PRI}}\right) = 7\ m/s$$

λ – Wavelength = $\frac{C}{f}$

T_{PRI} – Total period of pulse repetition interval

$$T_{PRI} = 1.3\ ms$$

Calculating the Chirp period with duty-cycling of 3%.

$$\left(\frac{T_C}{T_{PRI}}\right) = 0.03$$

$$T_C = 40\ \mu s$$

3.2.6 Selection of chirp sweep rate:

After deriving the T_{PRI}, many combinations of T_C and T_{PRI} are possible still meeting the spectral regulations. Various tradeoffs are involved in the selection of chirp rate. Targeting the range 1m-10m, the base band beat frequency versus the range for the different chirp rates is plotted in the Figure 3.8.

Main tradeoffs in this selection are as follows:

- Flicker noise corner
- Noise bandwidth
- settling time of HPF
- Area of HPF
- ADC Sampling rate
- Range-velocity ambiguity

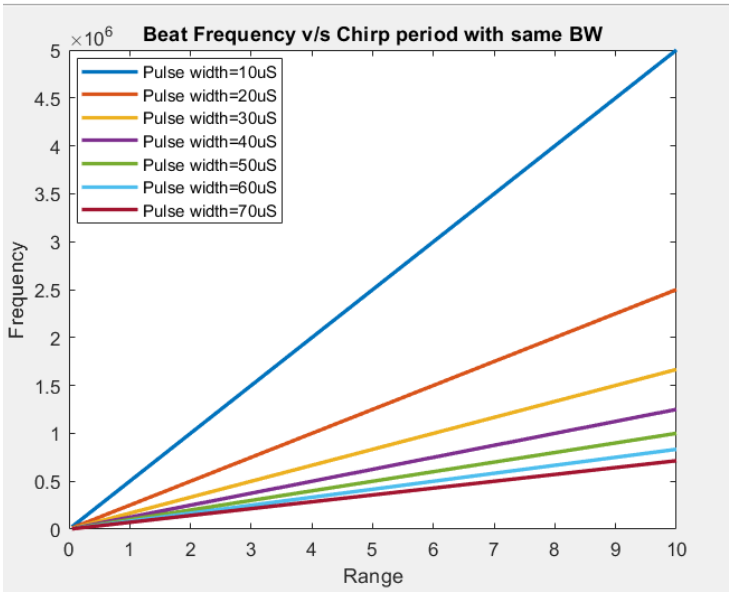


Figure 3.8 beat frequency of baseband across the range for various chirp periods.

3.2.7 Advantages and overheads of high chirp rates.

By increasing the chirp rate, the receiver experiences higher beat frequencies, far from the 1/f noise corner [10] of baseband analog circuits. Hence, the receiver will only be limited by its thermal noise [11]. Furthermore, higher beat frequencies would make it possible to choose a higher cut off frequency for the high pass filter which will decrease the receiver's settling time, thus reducing the receiver's energy overhead during power-up. Besides, HPF needs lower capacitance and occupies less area. However, the advantages of fast chirp sweep rate resulting in high beat frequency also come with the overhead of higher sampling rate for the ADC meeting the Nyquist criterion hence leading to higher power consumption. Fast chirp generation also poses the design challenge in terms of requirement of fast switching between the frequencies to generate a linear frequency slope by the frequency synthesizer. After considering all the above factors, the chirp sweep rate of 750 MHz/40 µs was chosen

Table 3.2 shows the beat frequencies generated after the down-conversion in the receiver considering the minimum and maximum distance to the target in addition to direct leakage of signal form TX antenna to RX antenna.

	Range	$T_{DELAY} = 2 * \frac{Range}{c}$	$f_{BEAT} = \frac{2 * R}{C} * \frac{df}{dt}$
Direct Leakage from TX to RX antenna	4cm	266.67 ps	5kHz ($f_{b,leakage}$)
Nearest Target	1m	6.67 ns	125kHz ($f_{b,min}$)
Farthest target	15m	100 ns	1.875 MHz ($f_{b,max}$)

Table 3.2 Time delay and beat frequency for all possible cases.

As per Nyquist-Shannon sampling theory [12], The minimum sampling frequency required for successful re-construction of any signal is twice the maximum frequency component of the signal. since the maximum beat frequency is 1.875 MHz, the sampling frequency of 12.5 MHz is selected which is can also be easily derived by 50 MHz signal. As we can observe from Table 3.2, we need a band pass transfer function to effectively filter only the desired signal in the frequency band from 125KHz to 1.875MHz. The chosen chirp period(T_C) of 40 µs results in the frequency resolution of 25 KHz ($1/T_C$) and number of FFT points to be around 12.5 MHz / 25 KHz = 500 ≈ 512.

After discussing extraction of range information, the estimate of heart beat rate and respiration rate are calculated from the relative change in the phase due to the doppler effect caused by moving heart and chest.

3.3 Radar Cross section(RCS):

Electromagnetic waves, with any specified polarization, are normally diffracted or scattered in all directions when incident on a target. These scattered waves are broken down into two parts. The first part is made of waves that have the same polarization as the receiving antenna. The other portion of the scattered waves will have a different polarization to which the receiving antenna does not respond. The two polarizations are orthogonal and are referred to as the Principal polarization (PP) and Orthogonal Polarization (OP), respectively. The intensity of the backscattered energy that has the same polarization as the radar's receiving antenna is used to define the target RCS. When a target is illuminated by RF energy, it acts as an antenna, and will have near and far scattered fields. Waves reflected and measured in the near field are, in general, spherical. Alternatively, in the far field the wave fronts are decomposed into a linear combination of plane waves. RCS for chest is considered to be 36.76e-3 m^2 (-14.43 dBsm) for the chest-wall surface of a human target.

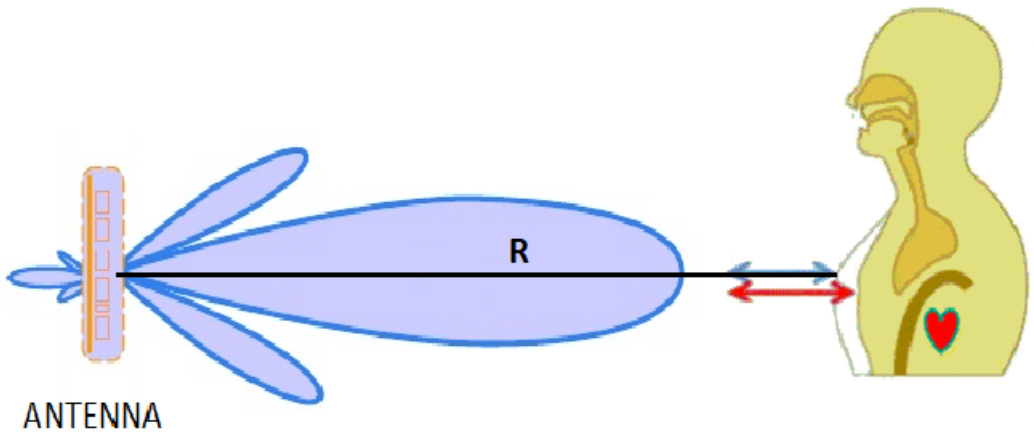


Figure 3.9 The chest at a distance R acts as a target with RCS=36.76e-3 m^2

3.4 Required Receiver Sensitivity

Receiver sensitivity is the lowest power level of a signal that the receiver can detect which corresponds to the power level of signal reflected from a target at the longest range(15m). The amount of power reflected by a target depends on total transmitted power, Radar cross section area and range of the target.

3.4.1 Received Power:

The power received back at the receiving antenna after reflection from the target depends on many factors and is given by the classical radar equation [7].

$$P_{RX} = \frac{P_{TX} * G_{TX} * G_{RX} * \lambda^2 * \sigma * \gamma}{R^4 * (4\pi)^3} \qquad \text{Equation 3.13}$$

P_{RX} – Receiver Power at the radar after reflection from the target.
G_{TX} – Gain from transmitting antenna.
G_{RX} – Gain from receiving antenna
λ - Wave length of the transmitted signal.
σ - Radar cross section area of the target(RCS).
P_{TX}- Total transmitted power.
γ – Reflection coefficient at air-skin interface.

If we plot the Received power versus range as shown in the figure, substituting P_{TX}= 0 dBm, σ = 36.76e-3 m^2, γ = 0.7, G_{TX} = G_{RX}= 5.

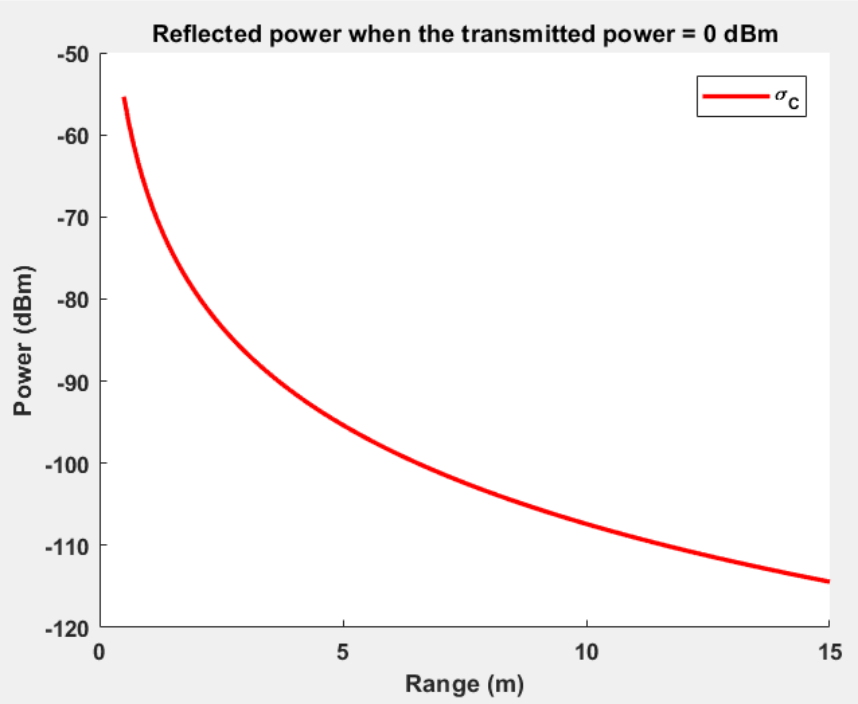


Figure 3.10 Power received from a target when transmitting odBm power versus range

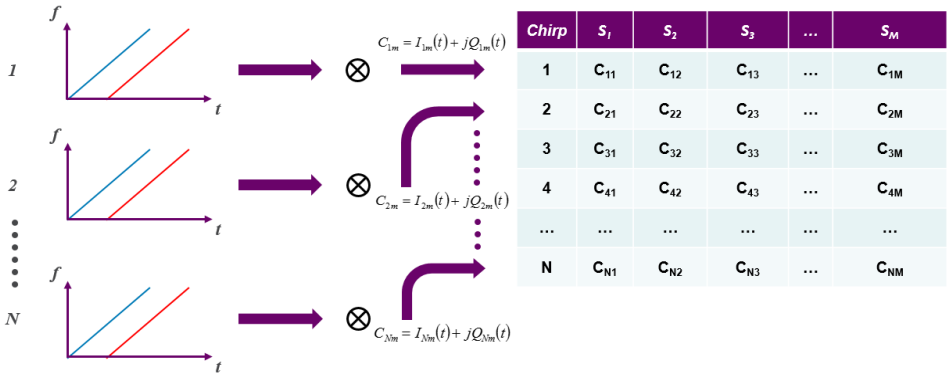
So, sensitivity required for the Receiver is around -114 dBm.

3.5 Signal and Data Processing

For FMCW, A series of *N* chirps is transmitted as shown in Figure 3.6 . The interval T_{OFF} can be o sec (with no duty cycling) or any values depending on the application and requirements. In this application it is used to provide a duty cycle to fit the spectral masks. T_{PRI} indicates the pulse repetition interval.

The baseband signal at beat frequency produced by each chirp is digitized to produce M samples. For quadrature receiver, the M IQ samples are related to produces M complex samples while we deal with real samples for the single-channel receiver which is chosen here. M depends on the ADC sampling rate. The N·M samples produced by N beat signals are arranged in a data matrix as in

Figure 3.11. The M samples are acquired during the fast time, meaning during T. Each chirp is repeated for every PRI, which represents the slow time (rows of the data matrix).



Chirp	S_1	S_2	S_3	...	S_M
1	C_{11}	C_{12}	C_{13}	...	C_{1M}
2	C_{21}	C_{22}	C_{23}	...	C_{2M}
3	C_{31}	C_{32}	C_{33}	...	C_{3M}
4	C_{41}	C_{42}	C_{43}	...	C_{4M}
...	...	...	...	...	...
N	C_{N1}	C_{N2}	C_{N3}	...	C_{NM}

Figure 3.11 Data matrix

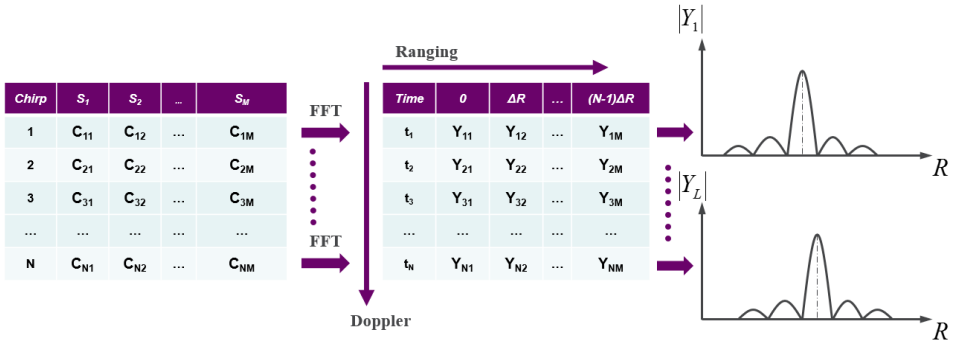


Figure 3.12 Matrix data processing

3.5.1 Ranging

The range information, namely the *range profile*, is determined by performing the FFT by row. As demonstrated by Equation 3.7, each target produces a *beat frequency* f_b which is proportional to the range as:

$$f_b = \frac{2 * B * R_0}{C * T} \qquad \text{Equation 3.14}$$

This means that at each time interval corresponding to a PRI, a new target's absolute distance is estimated. The range resolution ΔR depends on the chirp bandwidth B as $\Delta R = c/(2B)$. So, depending on its position, the target will be localized to a *range bin* corresponding to nearest FFT bin where the target's *beat frequency* will be resolved.

The result of the FFT for each row of size M is a complex value of size M by which we can extract magnitude and phase information. This means that if we apply the FFT over N rows (namely N chirps), we have the Doppler information. For example, if the target is at R_0 (for example $R_0 = 10.2*\Delta R$), it will be located to the nearest resolution in the range profile (for example $10*\Delta R$). Looking at the column corresponding to $10*\Delta R$, it is possible to extract the Doppler information by which vital signs and speed information can be determined. The number of chirp N to estimate the Doppler depends on the application, namely speed detection, vital signs monitoring.

3.5.2 Vital Signs

The Doppler information can be extracted determining the phase of Equation 3.7 over time as,

$$\frac{\partial \phi}{\partial t} = \omega_d = \frac{4\pi f_0}{c} x(t) \qquad \text{Equation 3.15}$$

Where $x(t)$ varies due to the doppler shifts caused by the mechanical movements of the heart and lungs on the human chest-wall and that can be expressed as:

$$x(t) = x_r(t) + x_h(t) = X_r \sin(2\pi f_r t) + X_h \sin(2\pi f_h t) \qquad \text{Equation 3.16}$$

where $x_r(t)$ and $x_h(t)$ indicate respectively the mechanical displacements produced by the respiration and the heart and are approximated as periodic functions, X_r and X_h are the maximum mechanical displacements of the lungs and the heart which are on average about 0.8 mm and 0.08 mm, respectively, while f_r and f_h are the vital signs frequencies which represent the information to be extracted. Depending on the subject and on the health condition, these frequencies are within 0.1 – 3 Hz.

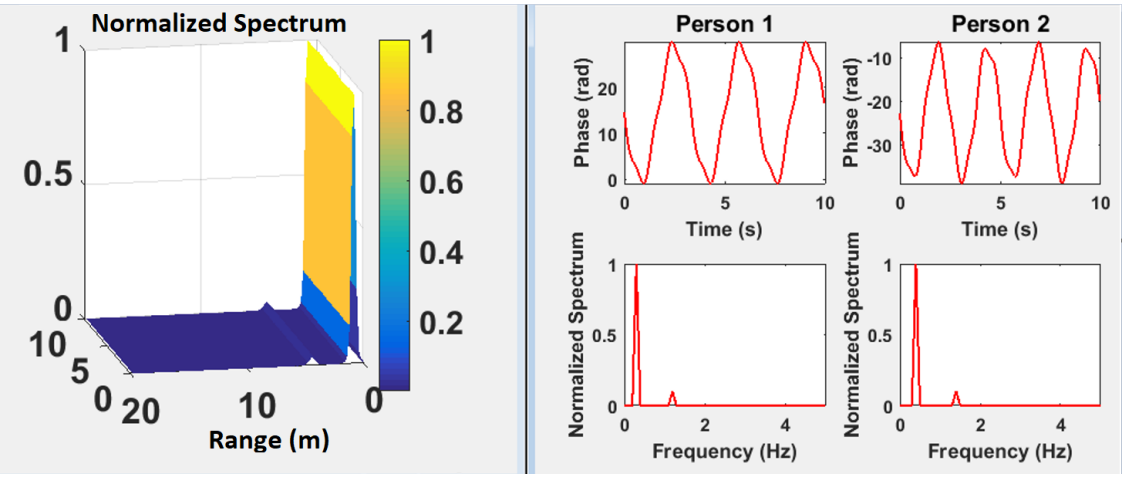


Figure 3.13 range profile and frequency components corresponding to heart beat rate and respiration rate.

3.5.3 Range/Speed Profile

The speed of a target can be determined by measuring the Doppler frequency f_d as:

$$\frac{\partial \phi}{\partial t} = \omega_d = 2\pi f_d = \frac{4\pi}{\lambda_0}\frac{\partial R_0}{\partial t} = \frac{4\pi}{\lambda} v(t) \qquad \text{Equation 3.17}$$

$$v(t) = \frac{2}{\lambda_0} f_d = \frac{2}{c} f_0 f_d \qquad \text{Equation 3.18}$$

A range/Doppler(speed) profile can be therefore be obtained by applying the FFT first by the row and then for the column to the matrix in Figure 3.12. An example of range/Doppler(speed) profile is shown in Figure 3.13 . As it can be understood, the speed and absolute distance of the target change during its motion. Depending on the application, the data processing unit should detect when the subject crosses different range bins and, at the same time, determine properly the corresponding speed.

A series of N chirps is transmitted and received before any processing is initiated over a slow time *Td*. For each chirp, the resulted baseband signal S(t) is acquired and digitized, producing M samples per chirp duration, referred to as fast time. After the slow time interval, *Td*, total of 'N' number of pulses each of duration T_{PRI} are accumulated making the total duration of slow time, $Td = N * T_{PRI}$.

we have *N·M* samples that are arranged in a matrix. Although the maximum velocity that we can detect with this T_{PRT} is 7 m/s, the speed resolution and range resolution are to be considered in case of people tracking. In order to detect the velocity of 0.2 m/s, the total time required to acquire consecutive chirps is approximately 100 ms for which the target person should be present in the same bin. So, to detect the velocity of 0.2 m/s accurately, the maximum speed of the movement should be limited to 2 m/s with the velocity resolution of 0.2 m/s.

$$\Delta v = \frac{\lambda_0}{2T_d} \qquad \text{Equation 3.19}$$

where $\lambda_o = c / f_o$. Since the range-speed profile is extracted using an Fast Fourier Transform (FFT) engine, the maximum speed is combined with the resolution and rounded up to the nearest power of 2 for efficient hardware implementation. With observation time of 100ms corresponding to radial velocity resolution and T_{PRT} = 1.3ms, N = 77.

For single channel radar, the theoretical maximum unambiguous range D_{max}:

$$D_{max} = \frac{cT}{4} \qquad \text{Equation 3.20}$$

However, in practical situations, the range where a person can be detected will be limited by the receiver's sensitivity and noise.

Chapter 4 Design and implementation of Frequency locked loop

4.1 Introduction and Requirements:

The Radar Transmitter's function is to generate the continuous FMCW chirps as shown in Figure 3.6. As already discussed, the FCC and ETSI regulations on spectral mask which needs a precise generation of continuous FMCW chirps. It's necessary to lock the output frequency of a Digitally Controlled Oscillator to accurate initial frequency before starting the frequency modulation. Frequency Locked Loop (FLL) is used for this purpose. 50 MHz external crystal oscillator is used as a reference to provide accurate timing to lock the DCO frequency to the desired frequency with fast settling behavior.

Figure 4.1 shows the generic block diagram of the transmitter. It consists of Oscillator, PLL and Power Amplifier. The Oscillator is the core block of the transmitter which generates the desired RF signal but is sensitive to process, temperature and supply variation. Hence a negative feedback loop around the oscillator is required to precisely control the frequency of generation. As shown in Figure 4.1, the oscillator frequency is first divided down to a lower frequency which can be compared with phase/frequency of the reference by a phase detector(PD) followed by the loop filter to integrate the error between desired output frequency and actual output frequency. Oscillator's output frequency is increased/decreased based a on negative or positive frequency error until the actual output frequency converges to the desired output frequency.

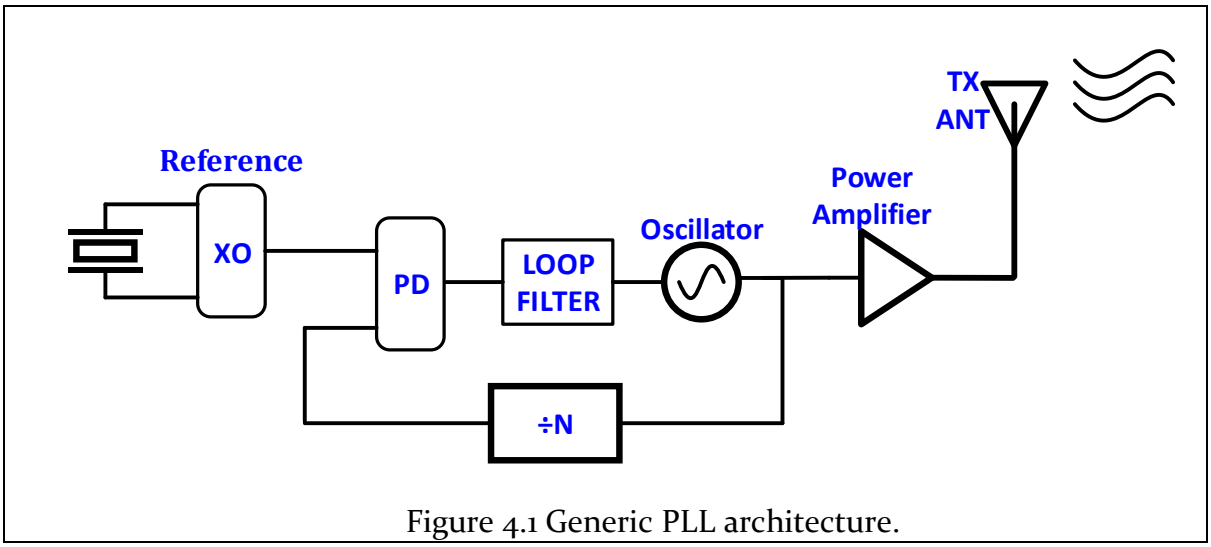


Figure 4.1 Generic PLL architecture.

Figure 4.2 shows the implemented top-level block diagram of the Transmitter with digitally intensive Frequency locked loop. DCO's frequency is scaled down and measured by the counter and then down sampled by 50 MHz reference. The measured frequency is then compared with desired frequency which is set by Frequency Control Word (FCW). Oscillator Tuning Word (OTW) is generated based on the difference in the desired and actual instantaneous frequency of the DCO and determines the output frequency of the oscillator.

Since the system's low power consumption is achieved mainly by aggressive duty cycling, it is necessary to control the ON/OFF cycles of all transmitter's blocks precisely. Timing to all the transmitter blocks is generated with respect to 50 MHz reference which gives the precision of 20 ns.

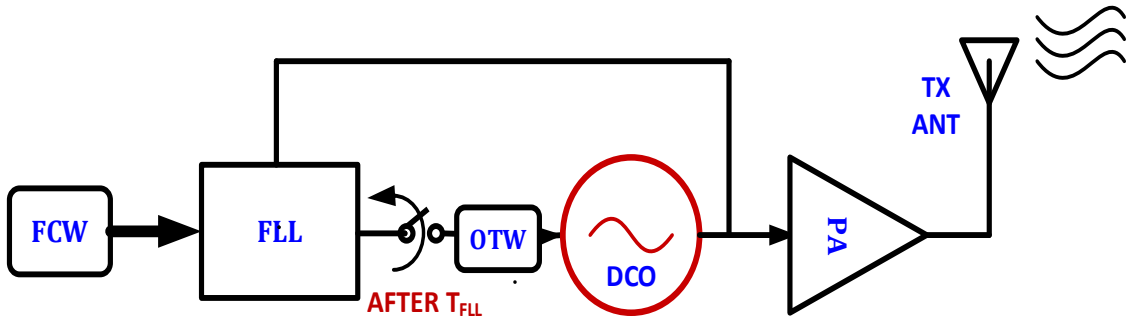


Figure 4.2 Simplified block diagram of the transmitter [13].

4.1.1 Output power

The peak output power along with the receiver's sensitivity defines the RANGE of the Radar. Hence to achieve long range with good SNR, higher output power is better since it results in longer radar range. But for the indoor UWB regulations impose the higher limit on the peak output power of 0 dBm and -41.3 dBm/MHz on average power. So, PA has to effective deliver 0 dBm power to 50 Ohm load which is transmitting antenna.

4.1.2 Settling time for the FLL

Frequency locked loop's settling time is one of the critical design requirements. DCO's output frequency is determined by the oscillator tuning word(OTW) which defines the capacitance of the LC tank. FLL generates the OTW with closed loop operation with negative feedback bringing the DCO's frequency to desired initial frequency(fo) of 7.4 GHz. The output power amplifier is off during FLL settling to avoid violating the requirements on the output power spectral density.

To reach a higher system energy efficiency, FLL settling time should be much shorter than chirp time (~40 µs). In this design, we aim to set the initial frequency of the DCO accurately to 7.4GHz within settling time(T_{FLL}) of <10 µs.

4.1.3 Initial frequency error

The heartbeat rate is determined by monitoring of the phase of the reflected signal from a person over consecutive chirps. Very small heart displacement results in very low phase change which is hard to detect if the initial frequency changes from chirp to chirp. DCO is also duty cycled to save the energy, which may cause the drift in the output frequency since it is very sensitive to supply and temperature variations.

The figure below shows the effect of initial frequency error for the two different initial frequency errors. In both cases, person-1 and person-2 are respectively located at a distance of 1m and 5m from the radar. It can be seen from the figure on the left that having an initial frequency error of 5 MHz makes it almost impossible to detect the vital signs at a distance of 5m. The detection capability is improved when the frequency error is reduced to 0.5 MHz in the figure on the right. Consequently, a frequency-locked loop(FLL) is required to adjust the oscillator frequency right before transmitting each chirp.

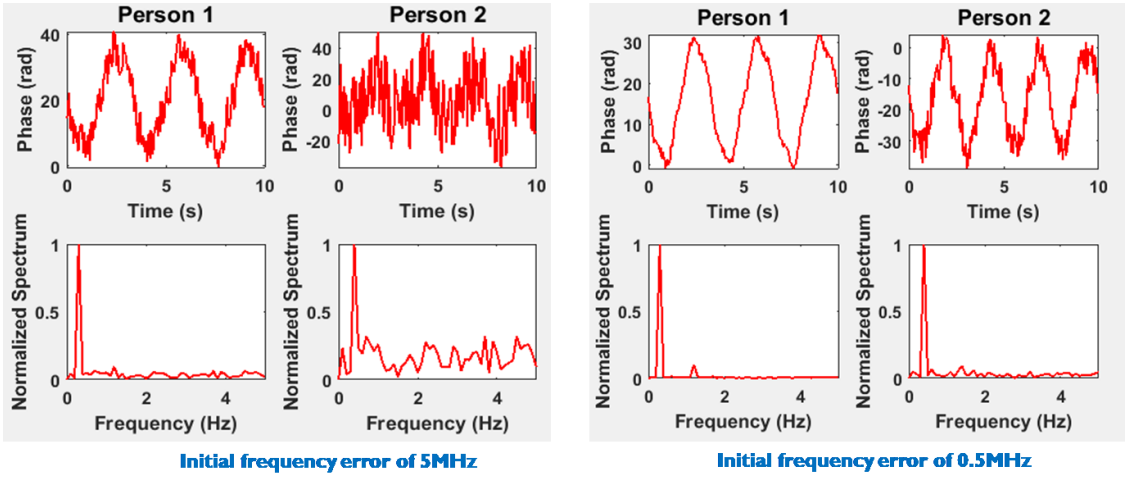


Figure 4.3 effect of initial frequency error on detection of vital signs.

4.1.4 Open loop modulation

The operation of FMCW radar relies on frequency modulation of transmit signal. There are two ways of modulating the frequency. First being, operating in FLL in closed loop and changing the FCW fractionally so that the frequency of the DCO increases based on the FCW. Second method being open loop modulation in which the loop is opened after the frequency of the DCO is locked to desired frequency and directly modulating the oscillator tuning word which in-turn switches the capacitor units in the modulation bank directly varying the frequency of the signal generated by DCO.

The choice of open loop modulation makes the frequency modulation power-efficient and less complex compared to closed loop modulation even though closed loop modulation gives the precise control over the frequency due to closed loop operation.

4.1.5 Problem of PA pulling and violating spectral mask

One of the major problems in the transmitter is frequency pulling during which the frequency of oscillator drifts when the PA is powered ON or when the amplitude of PA output is varied significantly. When the output power amplifier is enabled, it will start drawing significant current and can cause a drop in the supply voltage or induce a

ground current which momentarily introduce transient frequency drift [14] since oscillator's frequency is very sensitive to such variations. Even through FLL can you be used to lock the frequency after switching ON the PA, it would lead to violation of spectral mask regulations since PA is on for a longer time and DCO is at single frequency. So, the PA is turned on gradually in smaller steps of amplitude with programmable slope after the FLL is locked.

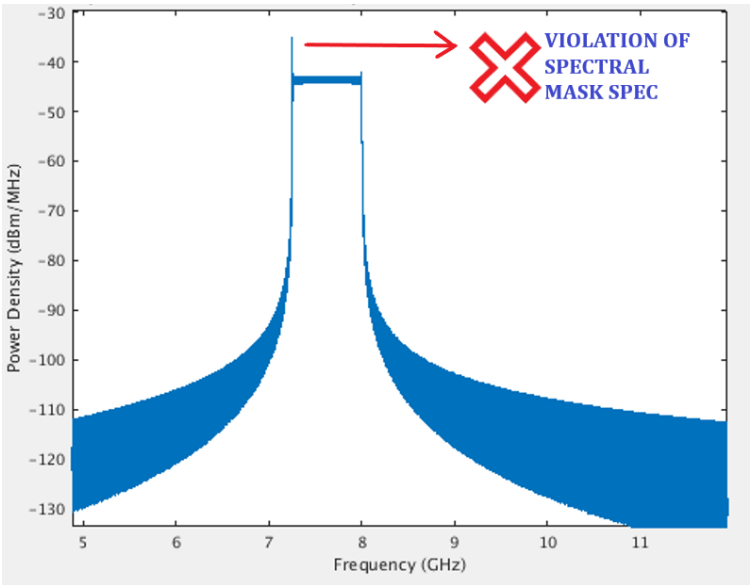


Figure 4.4 spectral mask violation due to FLL settling time after PA is ON.

Figure 4.4 shows the output spectrum when the PA is turned ON during the settling time of FLL which violates the spectral mask regulations.

4.1.6 PA ramping

The desired peak power that must be delivered to load is 0 dBm. If the PA is turned ON in a single step, it can lead to higher drift in the frequency of the digitally controlled oscillator since both are connected in transmit signal chain. In order to reduce the effect of PA pulling, the amplitude of the signal at the output of the PA has to be increased gradually towards 0 dBm from OFF state during each chirp generation cycle.

4.2 Analog Blocks:

The main analog blocks in FLL are digitally controlled oscillator, divider and counter. Digitally controlled oscillator's output frequency is defined by the LC tank in which Capacitance in variable and controlled by a binary code that is generated by the FLL. The scaled down version of DCO frequency is compared with that of the reference frequency and error frequency moves the Acquisition bank code in the right direction and finally ensure that the DCO output frequency settles to 7.4 GHz.

4.2.1 Divider

Divider's functional role is to bring down DCO frequency to suitable lower frequency range which can be compared with an accurate reference. Since divider operates at RF frequency and Dynamic power consumption is proportional to frequency of operation, an optimum trade-off between speed and power dissipation is necessary. Many factors contribute to speed of CMOS circuits which include device dimensions, logic circuit styles & architecture, clocking strategies, clock distribution. There are two class of circuits from the digital world namely static and dynamic logic circuits. Dynamic circuits are suitable for a higher frequency of operation while consuming more power. Static circuits are slow but power efficient. By combining both static and dynamic circuit topologies, it's possible to have a power-efficient solution. Combination of the divider implemented using the dynamic logic of TSPC and ripple counter implemented using standard logic cells makes is power efficient and fast.

Figure 4.6 shows the fast divide by two circuit. Its modified version of True Single-Phase Clocking (TSPC) dynamic circuit which is tested to operate in 10 GHz range. Two of such blocks are cascaded do form a divide by 4 circuit while consuming total average power of 160 µW.

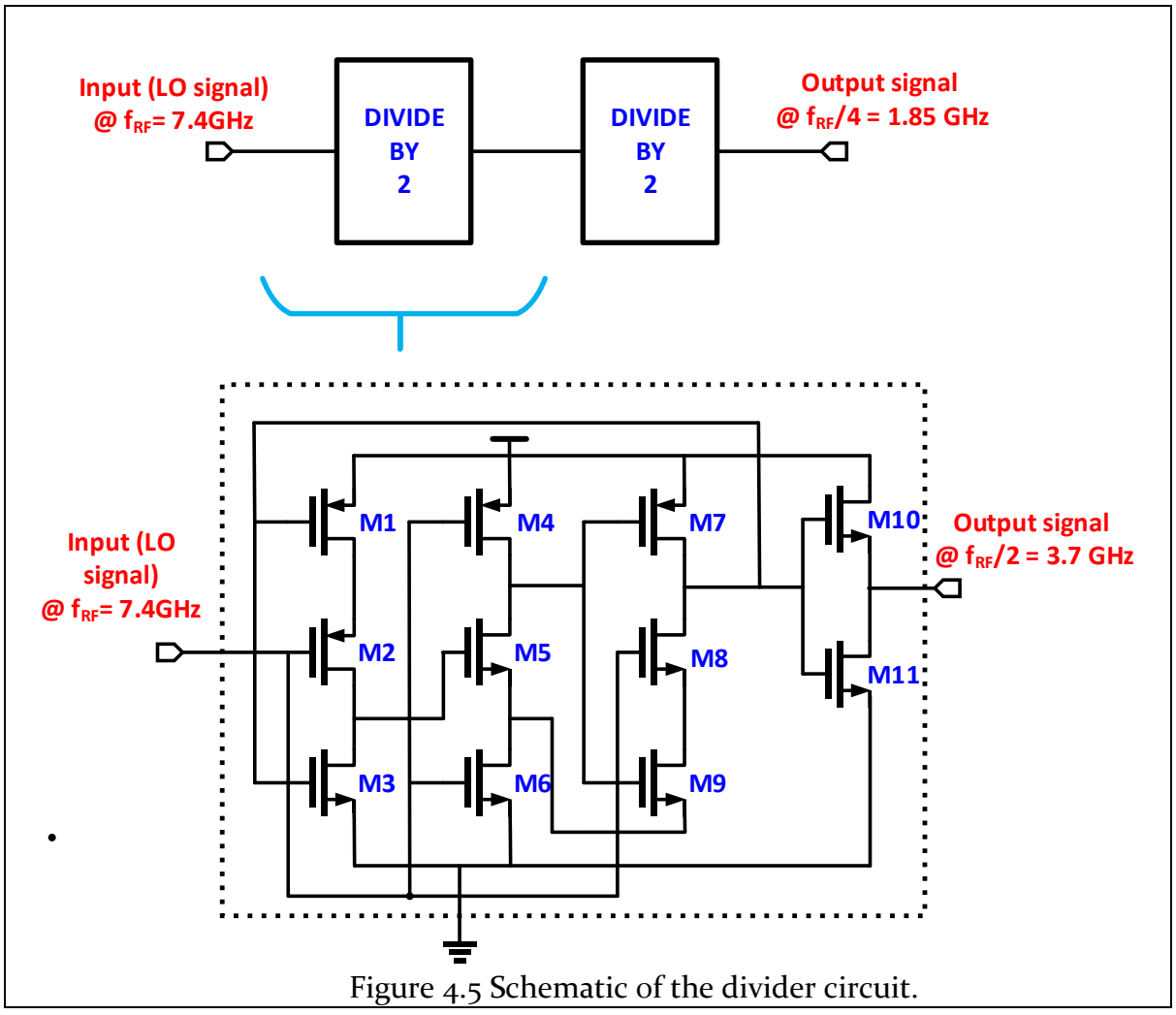


Figure 4.5 Schematic of the divider circuit.

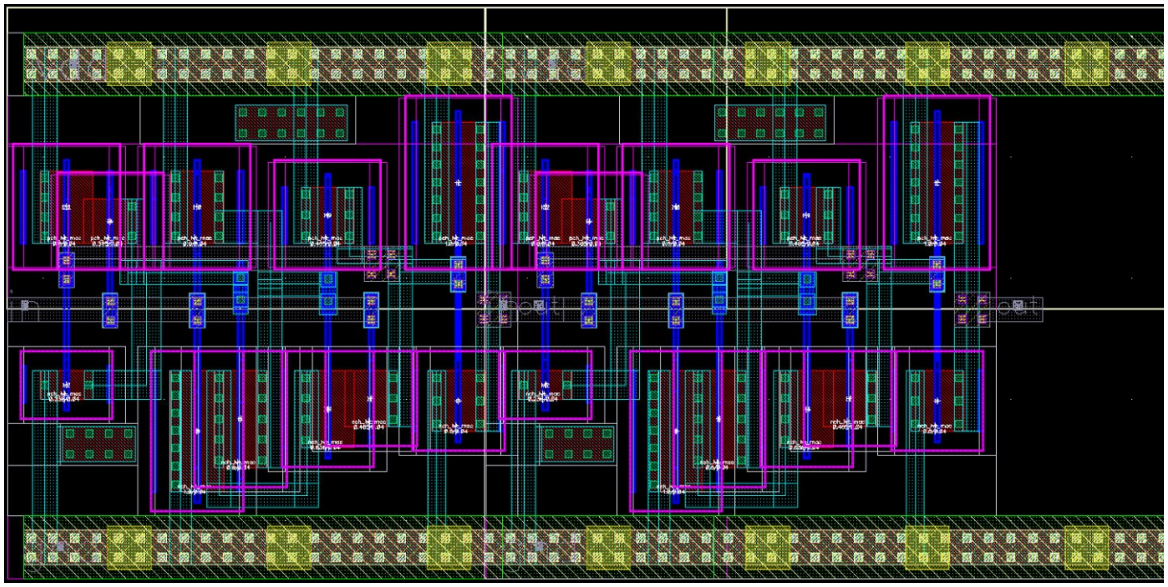


Figure 4.6 Layout of the divider circuit

M1, M4	600 nm/40nm	M7	465 nm/40nm
M2	365 nm/40nm	M8	465 nm/40nm
M3	235 nm/40nm	M9	635 nm/40nm
M5	465 nm/40nm	M10	1000 nm/40nm
M6	635 nm/40nm	M11	500 nm/40nm

Table 4.1 Sizes of the transistors in the divider circuit.

Figure 4.7 shows the result of the transient simulation of divide-by-4 circuit. The division factor of 4 from input frequency to output frequency can be observed. Figure 4.8 shows the phase noise simulation for divider indicating the value of -128 dBc/Hz at 1 MHz offset which is sufficiently low.

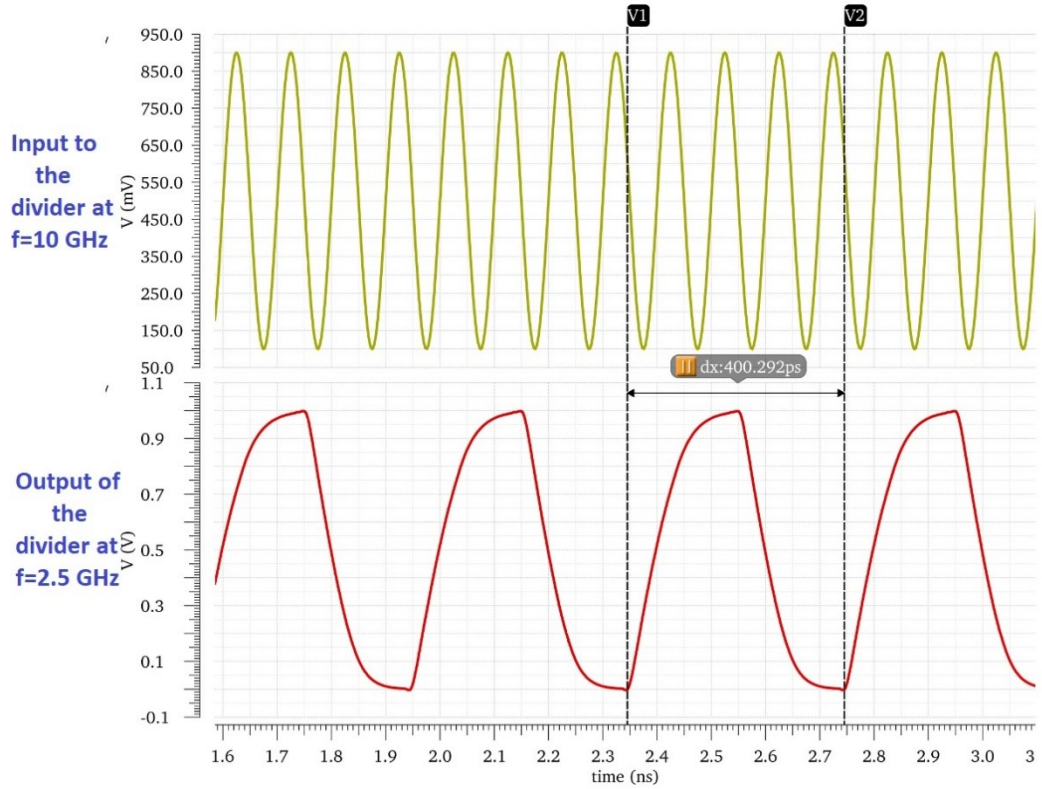


Figure 4.7 Transient simulation for the divide by four circuit.

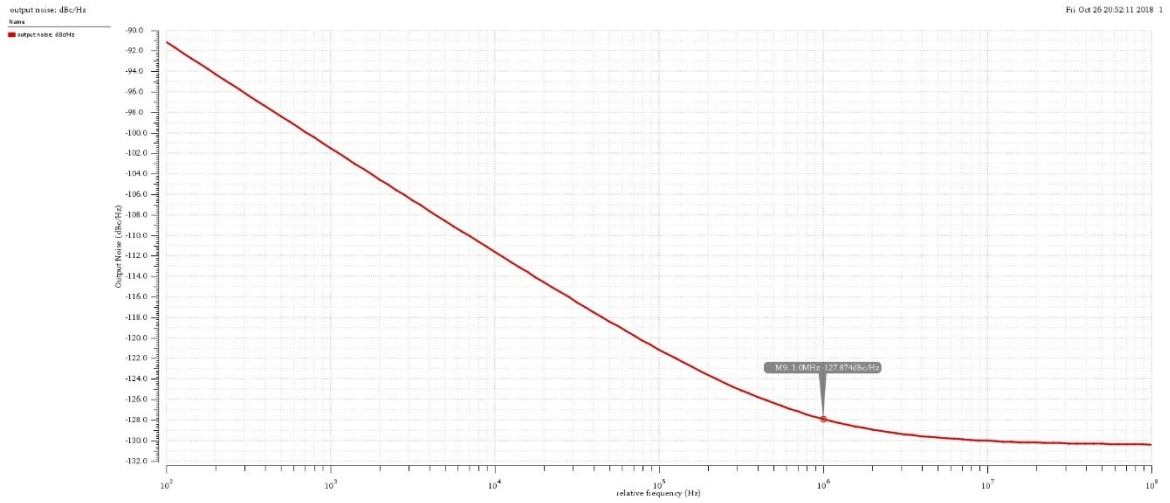


Figure 4.8 Phase noise simulation for the divider.

4.2.2 Counter:

The 6-bit counter is used to measure the frequency at the output of the DCO by counting the number of pulses at the divider output. The counter consists of cascade connection of six dynamic D-flipflops as shown in the Figure 4.9. The Dynamic D-flip flop is implemented in a master slave configuration by successive latching of data input on rising and falling edges of the clock.

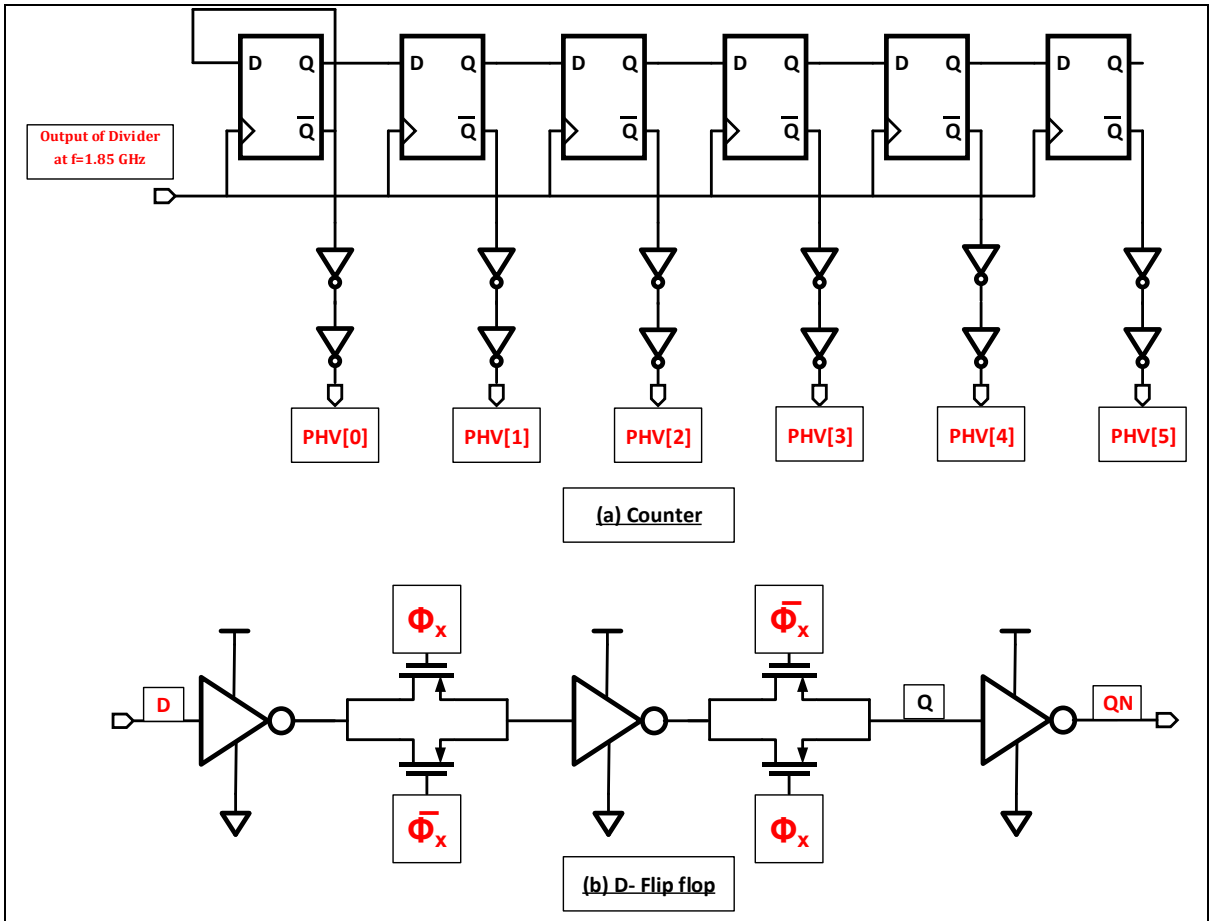
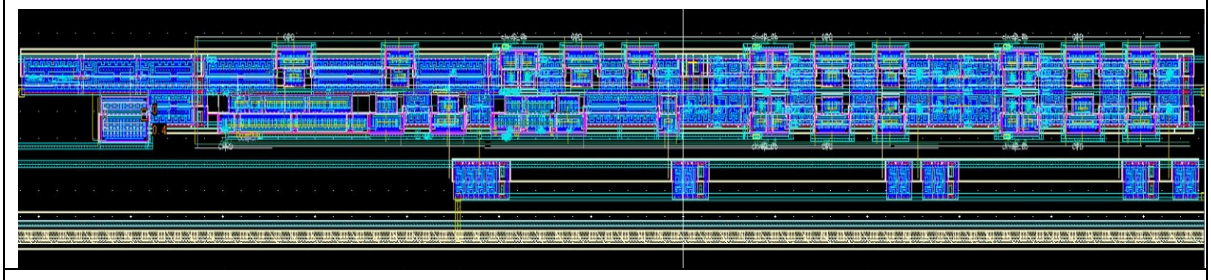


Figure 4.9 The simplified schematic of the counter(a) and flip flop(b). Standard cells are used in these implementations.



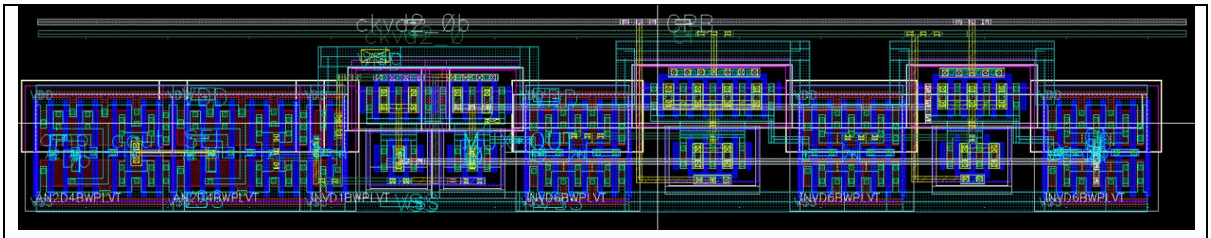


Figure 4.10 Layout of the counter and a flip flop using standard cells.

4.2.3 Digitally Controlled Oscillator:

In generic radio systems, the oscillators establish the transmitter carrier frequency and drive the mixer stages that convert signals from one frequency (RF/IF) to another (IF/RF). Two possible architectures for frequency generation at sub 10 GHz range are ring oscillator and LC oscillator. Through ring oscillator [15] is area efficient compared to LC equivalent, better phase noise performance and ease of frequency modulation with unit capacitor bank makes LC oscillator a suitable architecture choice for this application. A resonant circuit forms the fundamental building block of LC Oscillators since it acts as a bandpass filter determining the frequency of oscillations. Negative resistance generated by cross-coupled MOS transistors compensates for the energy loss due to finite Q of the tank. The frequency is determined by a variable capacitance of the tank which consists of capacitor banks namely PVT, Acquisition and chirp generation banks. PVT bank is set statically from the SPI register while acquisition and chirp generation banks are set dynamically during closed loop and open loop operation respectively. Figure 4.11 shows the architecture of the DCO with various capacitor banks. Thanks to Paul at IMEC for designing the DCO and his support for the verification of the closed loop functionality of the FLL.

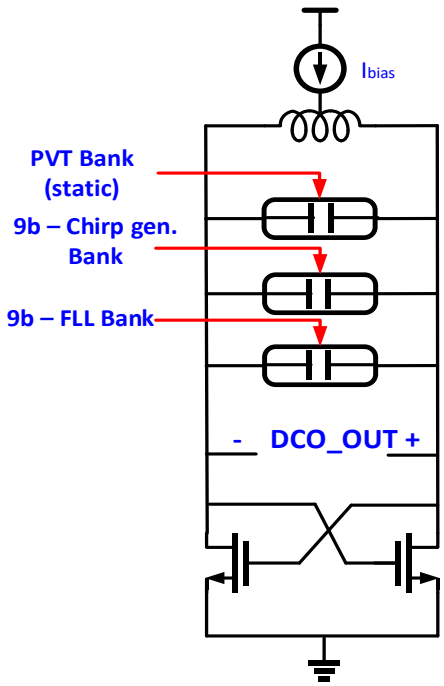


Figure 4.11 DCO with capacitor banks for chirp generation and initial frequency locking.[1]

[1] DCO is designed by a designer at IMEC-NL

4.3 Digital blocks:

The block diagram of digital implementation of the FLL is shown in the figure

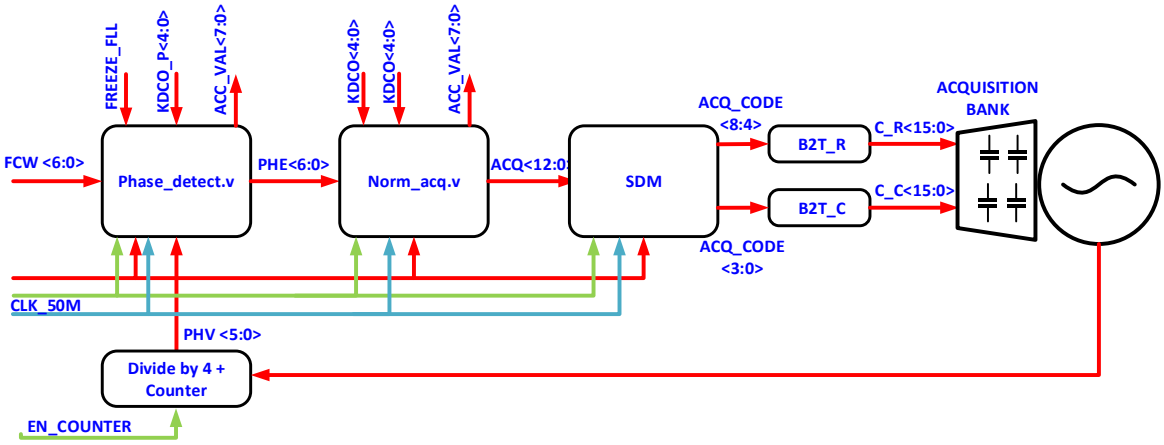


Figure 4.12 Implementation and interconnection digital blocks

The proposed FLL can be simplified to three main blocks as shown in Figure 4.12 consisting of phase detect block, normalization block and SDM with decoder.

- **Phase detect block (phase_detect.v)**

On the feedback path, the phase detector calculates the difference between the counter value at two consecutive edges of reference. This signal is then subtracted from the frequency command word(FCW) and the result is multiplied with the value of KDCO_P and generates the value of PHE<6:0> that is then applied to the digital loop filter.

- **Normalization block and SDM Block.**

Normalization block receives the accumulated value PHE<6:0> from the phase detector and scales up/down based on the value of KDCO and generates the acquisition code to control the capacitance bank. To have a lower number of bits to control the acquisition bank, only MSB's are used to generate the acquisition code and LSB's are feedback and added to the next input to form a first order SDM operating at 50 MHz. The acquisition bank code is then propagated to binary to thermometer decoder.

- **Synchronous Binary to Thermometer decoder:**

The function of this block is covert the binary code generated by FLL to thermometer code to switch the acquisition bank of capacitors to increase or decrease the DCO's output frequency to lock to desired initial frequency fo = 7.4 GHz. The decoder is clocked with reference of 50 MHz to avoid any glitches which would introduce the spurious tones at in the DCO output.

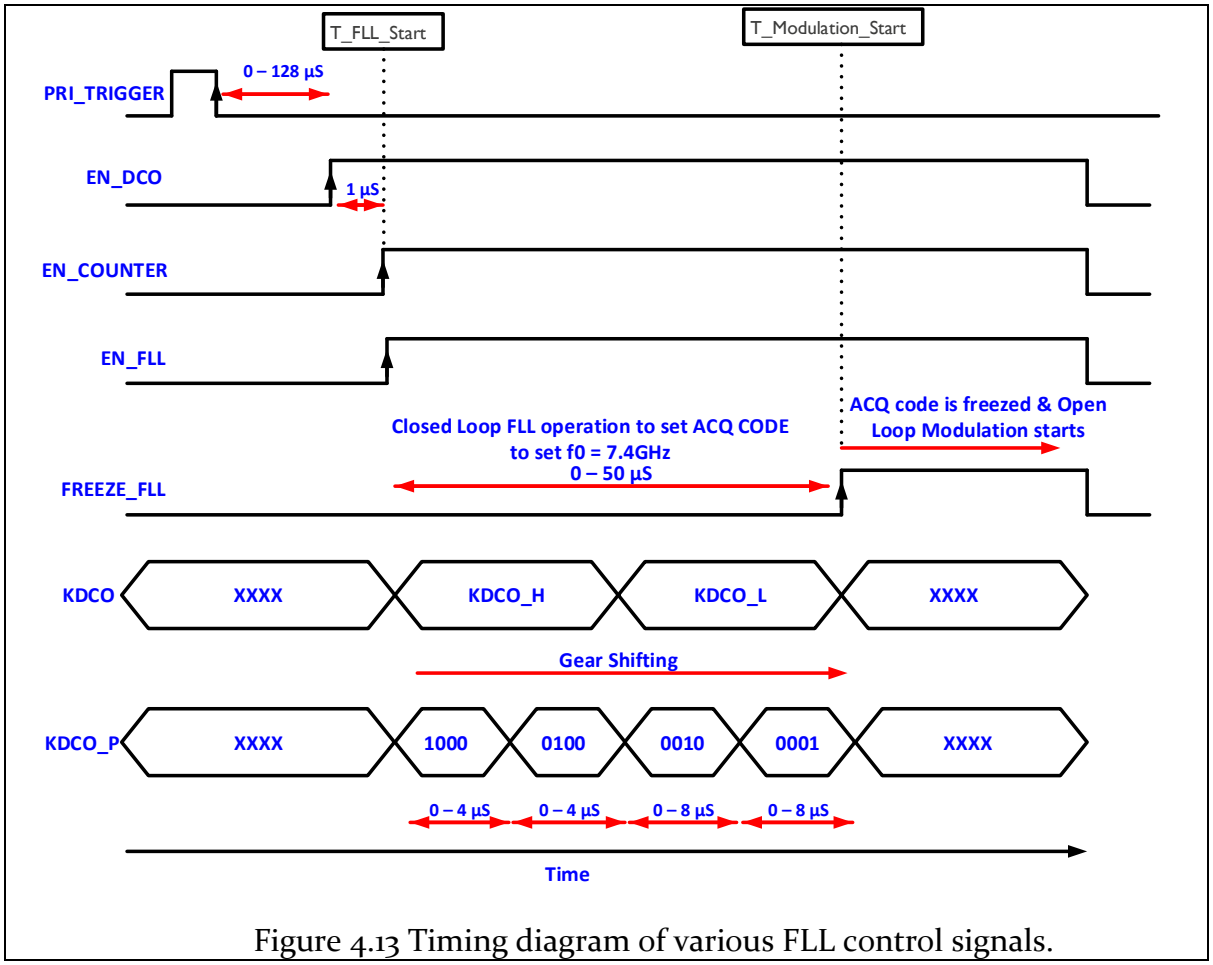


Figure 4.13 Timing diagram of various FLL control signals.

Figure 4.13 shows the various timing wave forms and key registers content during the FLL operation. PRI_TRIGGER is the main synchronization signal which acts as a starting time reference to generate all other enable signals to each of the TX and RX blocks including FLL. DCO is enabled first after a programmable delay with reference to PRI_TRIGGER signal. The time margin of 1 us is reserved for startup of the DCO. Once the DCO starts-up with a frequency not exactly as desired (7.4GHz), the divider and counter are enabled starting the closed loop operation of FLL to converge the DCO's output frequency to the desired initial frequency. KDCO value switches from KDCO_H to KDCO_L after a programmable time defined by SPI register. The KDCO_P value is switched progressively from higher value to lower value by shifting right by one-bit position enabling the gear shifting. Low to high transition on the FREEZE_FLL signal completes the closed loop operation of the FLL and DCO's acquisition bank code is locked to desired code ensuring the correct initial frequency to start the frequency modulation.

The role of different control registers and signals is discussed here.

- **T_fll_start<25:0>: Time value for Start event of FLL**
  This register value sets the turning on time with respect to the pre-trigger event. Number of clock cycles of 50 MHz clock to wait before turning on the FLL.

- **C_fll_enable<15:0>: Count value for enable event for FLL.**

This register contains the count value in-terms of number of CLK cycles for the time during which the FLL is enabled.

- **C_fll_disable<15:0>: Count value for disable event for FLL.**
  This register content is the count value to indicate the time for FLL disable event. Value of this register must be greater then C_fll_enable.

- **C_fll_enable_counter<15:0>: Count value for enable event for the 2 blocks- counter and divider.**
  Register contains the count value for enabling event of two blocks divide by 4 circuit and counter individually. The purpose of having separate enabling the counter and divide by 4 circuit to measure the frequency externally by reading out the counter value.

- **C_fll_freeze<15:0>: Count value for FREEZE event for FLL.**
  This register content is the count value to indicate the time after which the FLL freezes the acquisition code to control the acquisition bank.

- **C_kdco_h<15:0>: Count value for the time of FLL operation with kdco_h.**
  Register contains the count value to indicate the time of operation with high gain setting for kdco = kdco_h for FLL operation. The kdco value switches from kdco_h to kdco_l after the time corresponding to count value in C_kdco_h.

- **kdco_h<4:0>: Higher Gain Value for kdco.**
  Register contains the higher gain value that is multiplied with the content of the accumulator before generating the acquisition code to control the acquisition bank.
  Effective kdco value switched to lower value kdco_l after the time corresponding to C_dco_h.

- **kdco_l<4:0>: Lower Gain Value for kdco.**
  Register contains the low value that is multiplied with the content of the accumulator before generating the acquisition code to control the acquisition bank.

- **C_gain_h<15:0>: Count value for high gain setting.**
  Register contains the count value indicating the time of FLL operation with high gain setting before gear shifting for fast settling purpose. The gain before the accumulator(kdco_p) is changed to half of its initial value after time corresponding to C_gain_h.

- **C_gain_m<15:0>: Count value for medium gain setting.**
  Register contains the count value indicating the time of FLL operation with medium gain setting after 1st gear shifting event for fast settling purpose. The gain value multiplied before the accumulator is changed to half of prior value after time corresponding to C_gain_m.

- **C_gain_l<15:0>: Count value for low gain setting.**
  Register contains the count value indicating the time of FLL operation with lowest gain setting after 2nd gear shifting event for fast settling purpose.

- **kdcop<4:0>: Gain before accumulator.**
  Register contains the initial gain value to start with before shifting the gear into lower gain by shifting right by one bit which is equivalent to dividing by 2. Register value is shifted right at each of times determined by C_gain_h, C_gain_m and C_gain_l.

- **EN_sdm: Enable 1st order Sigma delta modulator.**
  This bit is used to enable the sigma delta modulator operating at 50 MHz before generating the oscillator tuning word.

- **acq_code<7:0>: Code generated by FLL to control acquisition bank**
  Acquisition code is generated by FLL during the close loop operation. For debug purpose, this value is stored on the register which can be read out of the chip on SPI.

- **dco_acq_col<15:0>: Column decoder output**
  This register holds the 16-bit output of the 4 to 16 column decoder generated from lower 4 bits of acquisition code generated from closed loop operation.

- **dco_acq_row<15:0>: Column decoder output**
  This register holds the 16-bit output of the 4 to 16 row decoder generated from higher 4 bits of acquisition code generated from closed loop operation.

- **accu_data <7:0>: Accumulator data**
  The present accumulator data can be read out from this register for the debug purpose.

- **fcw <6:0>:** Frequency control word
  Frequency control word determines the frequency of the DCO output.
  Since the desired output frequency is 7.4 GHz the value is set to 37.

- **acq_val <7:0>:** Acquisition bank value
  Fixed signed value can be added to acquisition code generated from FLL if necessary incase of overflow or underflow.

- **acc_mem_en:** Enable for accumulator memory
  This bit control is provided to select/deselect the option to retain the value of accumulator from one chirp to next chirp which can be useful in reducing the settling times for successive chirps.

- **bypass_en_fll_enable:** Bypass enable for FLL
  This is one-bit control to enable standalone testing of the FLL. By setting this bit, fll_enable is bypassed from actual timing instead manually set by a static register value.

- **bypass_en_fll_enable_counter:** Bypass enable for counter and divider
  This is one-bit control to enable standalone testing of the FLL's analog blocks divider and counter. By setting this bit, fll_enable is bypassed from actual timing instead manually set by a static register value.

- **bypass_en_fll_freeze:** Bypass FLL freeze control
  This bit is again for bypassing time based FLL freezing to manual freezing and un-freezing the acquisition code to the acquisition bank of standalone verification of FLL functionality.

- **bypass_val_fll_enable:** Actual bypass value for enabling FLL digital blocks
  This bit provides actual 1-bit control to enable/disable the FLL manually. This bit valid only if "bypass_en_fll_enable" is set to 1.

- **bypass_val_fll_enable_counter:** Actual bypass value for enabling divider and counter
  This bit provides actual 1-bit control to enable/disable the divider and counter manually. This bit is valid only if "bypass_en_fll_enable_counter" is set to 1.

- **bypass_val_fll_freeze:** Bypass value for freezing FLL.
  This bit provides actual 1-bit control to freeze/unfreeze the DCO acquisition code manually. This bit is valid only if "bypass_en_fll_freeze" is set to 1.

- **bypass_en_acq_dco_acq_col<15:0>:** Bypass enable for acquisition bank columns.
  This 16 bit word enables to bypass the FLL control to acquisition bank columns and gives the direct access control to each of the columns through SPI register.

- **bypass_val_acq_dco_acq_col<15:0>:**
  This is 16-bit word to set each of the 16 rows of the acquisition bank manually without FLL and is valid only if corresponding bits in bypass_en_acq_dco_acq_col<15:0> are set.

- **bypass_en_acq_dco_acq_row<15:0>:** Bypass enable for acquisition bank row control.
  This 16-bit word enables to bypass the FLL control to acquisition bank and gives the direct access control to set each of the rows through SPI register.

- **bypass_val_acq_dco_acq_row<15:0>:**
  This is 16-bit word to set each of the 16 columns of the acquisition bank manually without FLL and is valid only if corresponding bits in bypass_en_acq_dco_acq_row<15:0> are set.

- **fll_enable: Control signal to enable FLL**
  This control signal is intended to enable the digital blocks of the FLL that include phase_detect and normalization blocks.

- **fll_freeze: Control signal to freeze the acquisition bank code.**
  This signal is intended to freeze the acquisition code there be setting the initial frequency of the DCO exactly to desired value (7.4GHz) before staring the chirping.

- **kdcop<4:0>: Gain before accumulator.**
  This register is used for the purpose of gear shifting which is set to higher value during the closed loop operation and progressively reduced over time finally reaching the unity value.

- **kdco<4:0>: Gain before acquisition bank control.**
  This register is used to scale the code generated by FLL before controlling the acquisition bank.

4.4 Overall Mixed signal operation of the FLL

The functional block diagram of the FLL is shown in Figure 4.14. The purpose of FLL is to bring the initial frequency(fo) of the DCO to 7.4GHz by closed loop operation before starting the frequency modulation to generate the chirp by control from Chirp Generation block in open-loop.

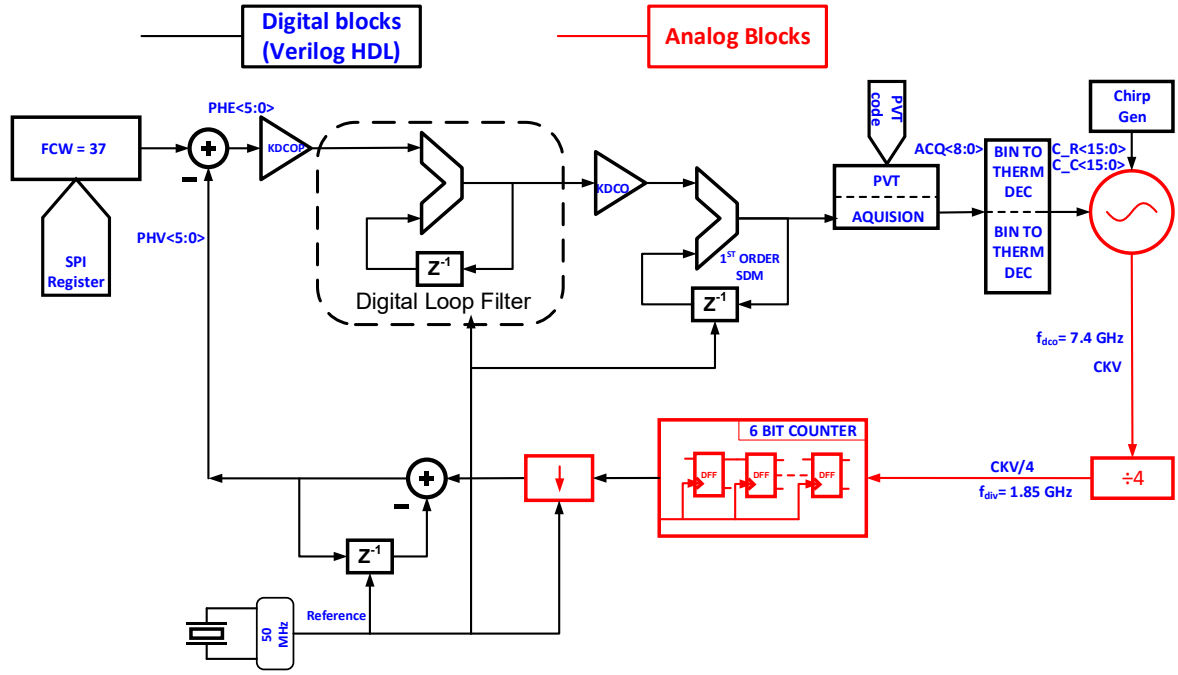


Figure 4.14 FLL architecture showing the mixed signal interconnection between analog and digital blocks.

To start with, consider the DCO output frequency is exactly at the desired fo = 7.4GHz. Hence, the output frequency of the divider is 1.85GHz. The counter calculates the number of pulses continuously and its output is down-sampled by a 50-MHz clock. Hence number of clock cycles of 1.85 GHz with in one period of the 50-MHz clock(20-ns) is 37. This value is read by the phase detector block which is compared with the FCW (37). Since the difference is zero, the accumulator value inside the phase detector block remains the same resulting in the stable oscillator tuning word with no further change.

Now consider the DCO output frequency is higher than the desired value, say 7.6 MHz results in f_div = 1.9 GHz at the divider output. The counter keeps counting the number of cycles of 1.9 GHz. The difference between two successive counter values becomes 38. The difference between 38 and FCW (37) which equals +1 increments the accumulator over the time and acquisition code value is increased to connect more capacitor units to the acquisition bank thereby reducing the output frequency of the digitally controlled oscillator.

Now, consider the DCO is running slow, and its output frequency is lower than the desired value, say 7.2 MHz. It results in the frequency f_div = 1.8 GHz at the divider

output. The counter keeps counting the number of cycles of 1.8 GHz. Now, the difference between two successive counter values becomes 36. The difference between 36 and FCW (37) which equals -1 decrements the accumulator over the time and acquisition code value is decreased to disconnect the capacitor units to the acquisition bank thereby increasing the output frequency of the digitally controlled oscillator.

After the DCO output frequency is locked to the desired initial frequency (fo=7.4 GHz), upon receiving the control signal FREEZE_FLL generated by timing generation block the acquisition code is frozen and that completes the closed loop operation. Once the acquisition code is set by setting the capacitance of acquisition bank, open loop modulation starts in which the chirp generation capacitance bank shown in Figure 4.11 is progressively triggered by a clock signal to disconnect the unit capacitors one by one hence increasing the frequency of the signal generated by the DCO.

Two gains namely KDCOP and KDCO are used in this architecture. The KDCOP is used for gear shifting which amplifies the error between the desired output frequency and actual instantaneous frequency of the DCO in the initial phase of closed loop operation hence speeding up the convergence of a DCO frequency towards desired frequency. KDCO is used to shift the bits of accumulator output to pass only most significant bits and feedback the lower significant bits with programmability on number of bits to shift, which enables the first order sigma-delta operation. The problem of metastability is generally encountered while crossing two clock domains. To address this problem, the PHV<5:0> (down-sampled counter output) is generated on every rising edge of 50 MHz clock and read into phase detector block on the falling edge of the 50 MHz clock.

4.5 Simulation results of FLL

Behavioral models are built for the all the analog blocks in the FLL to verify the closed loop operation. Extensive AMS simulations are carried out to verify all the possible scenarios for the operation of the FLL to ensure the desired functionality for various settings.

Figure 4.15 shows one of the scenarios. The DCO's frequency is set initially to 7.35 GHz in its Verilog-AMS model. FLL converges the frequency up to 7.4 GHz by closed loop operation and finally locks the acquisition bank code on the rising edge of FLL_FREEZE signal as shown. It should be noted that the decreasing the value of acquisition code results in decrease in capacitance value of the LC-tank hence increasing the output frequency of the DCO.

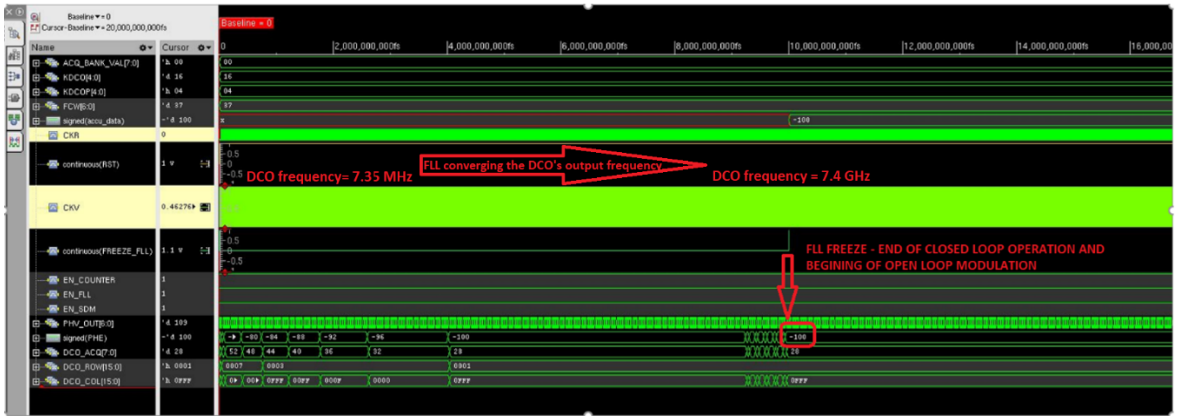


Figure 4.15 AMS Simulation result when DCO frequency is lower.

Figure 4.16 shows another case where the initial DCO frequency is set to 7.40575 GHz with an offset of +5.75 MHz. FLL converges the frequency down to 7.4 GHz by increasing the acquisition bank code.

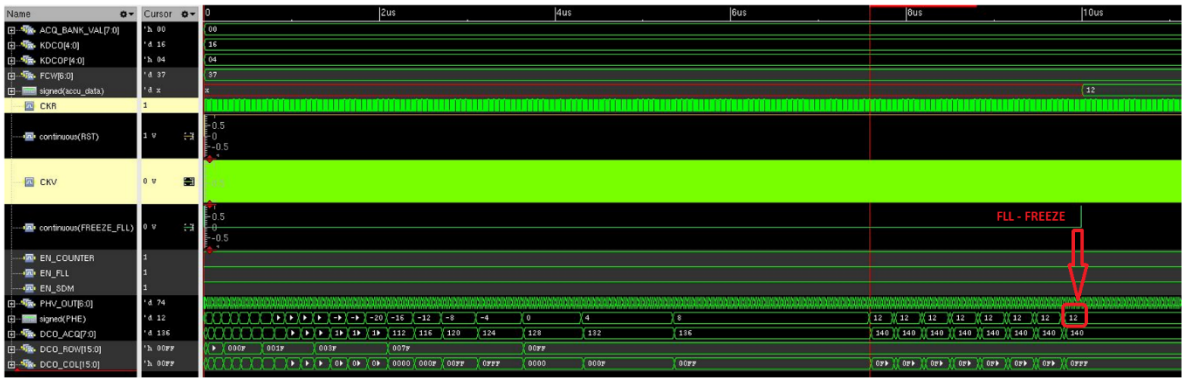


Figure 4.16 AMS Simulation result when the DCO frequency is higher.

4.6 Layout of the Transmitter:

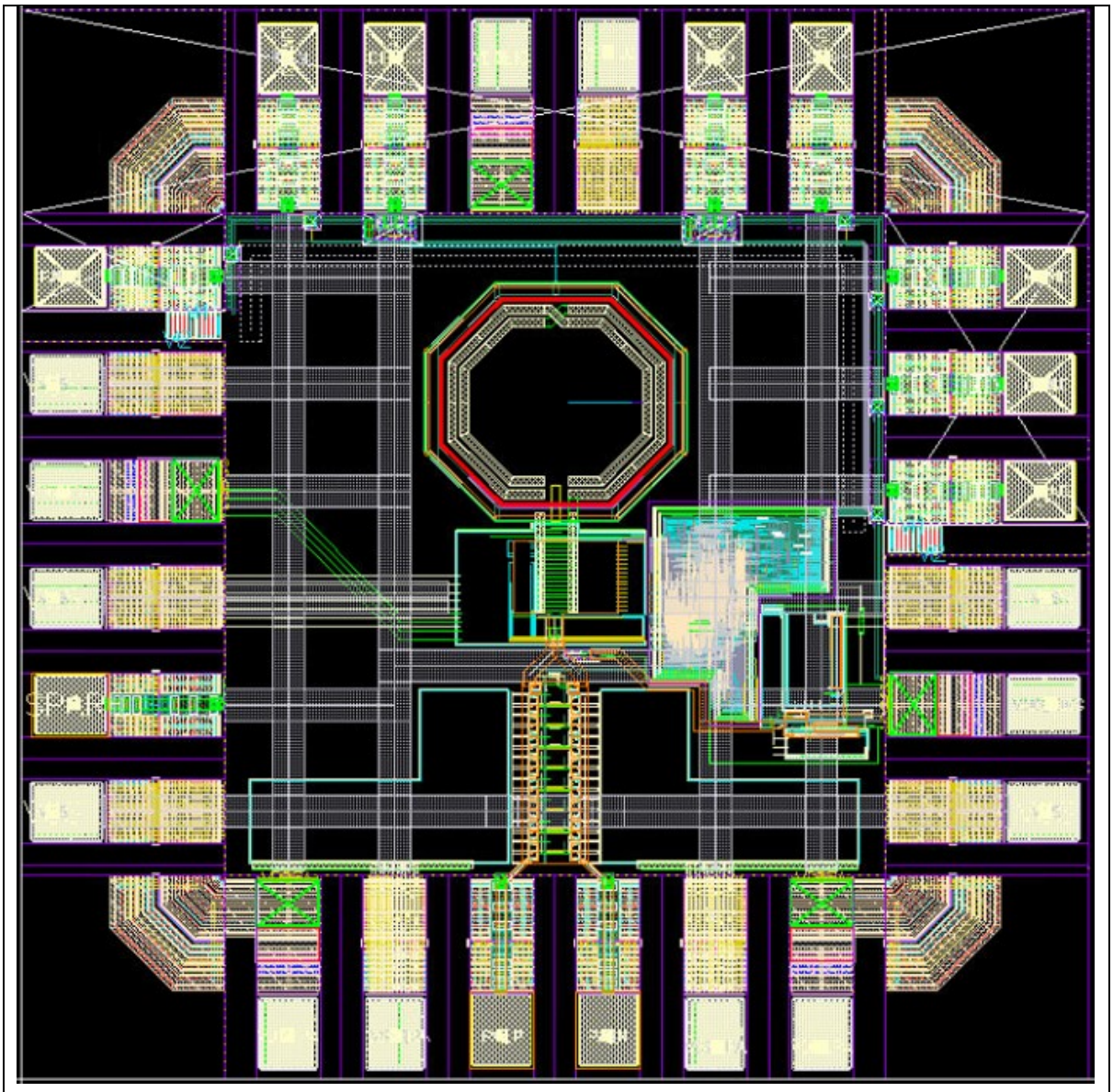


Figure 4.17 Layout of the transmitter.

Chapter 5 Design and implantation of Receiver

A receiver receives the echoed signal from the target (Human chest) followed by down conversion of RF signal to beat frequency signal which is then processed by base band signal conditioning and acquisition circuits.

The Rx chain consists of following blocks as shown in Figure 5.1

- Input matching network to match 50 Ohm impedance form antenna to LNA input to ensure S11 < -10 dB for effector power transfer with minimum reflection.
- Low Noise Transconductance Amplifier (LNTA) to amplify the input RF signal(7.4GHz-8.15GHz) of µV scale signal with minimum noise addition from the circuit.
- Mixer to down convert RF signal to beat frequency of 100's of kHz to MHz range with minimum noise addition from the circuit.
- Band-pass filter (cascading HPF and LPF) to suppress the signal at the lowest beat frequency signal generated due to a mixing of large amplitude (-35 to -30dBm) direct leakage signal from the TX antenna to the RX antenna. It also limits the band width to 2 MHz to reduce total integrated noise.
- 9b SAR ADC to sample & digitize the beat frequency signal at the sampling rate of 12.5 MHz and output 9b digital code which will be read into FPGA where signal processing is carried out offline with MATLAB to extract the vital signs.

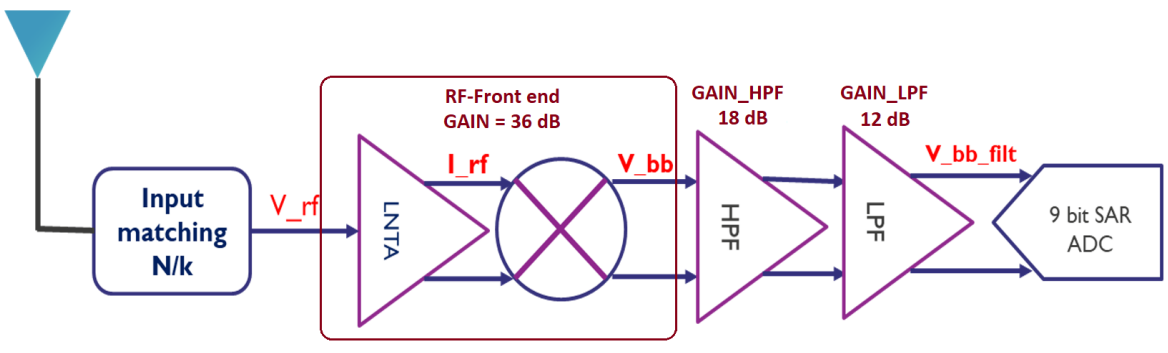


Figure 5.1 block diagram of the receiver signal chain.

5.1 Specifications:

5.1.1 Sensitivity and Noise Figure:

The well-known equation for sensitivity of the Receiver is given by

$$\text{Sensitivity} = -174\ \text{dB} + 10 * \log(BW) + NF + SNR_{min} \qquad \text{Equation 5.1}$$

Where BW is the bandwidth of base band signal (2MHz), NF is the overall noise figure of the receiver and SNR_{min} is the minimum signal to noise ratio for successful detection of target. The sensitivity may be improved by lowering the noise figure or reducing the system bandwidth. In-order to achieve very low noise-figure, low noise amplifier consumes very high power. Using the advantage of integrating multiple pulses would relax the noise figure requirement on Receiver consuming low power. Figure 5.2 depicts the concept of required SNR. It can have observed that the signal time A exceed the SNR and indicates a false target. The signal at time B is just at the threshold, and the signal time C is clearly below it. so SNR_{min} can be set to higher value to have low probability of detection of false targets. The acceptable minimum signal to noise ratio (SNR_{min}) for a receiver depends on the intended use of the receiver. For instance, a receiver that had to detect a single radar pulse would need a higher SNR_{min} that a receiver that could integrate a large number of radar pulses (increasing the total signal energy) for a detection with the same probability. For the detecting a single radar pulse with 98% probability, we need SNR of 12 dB as shown in Figure 5.3. since we integrate multiple pulses, the SNR_{min} can be reduced.

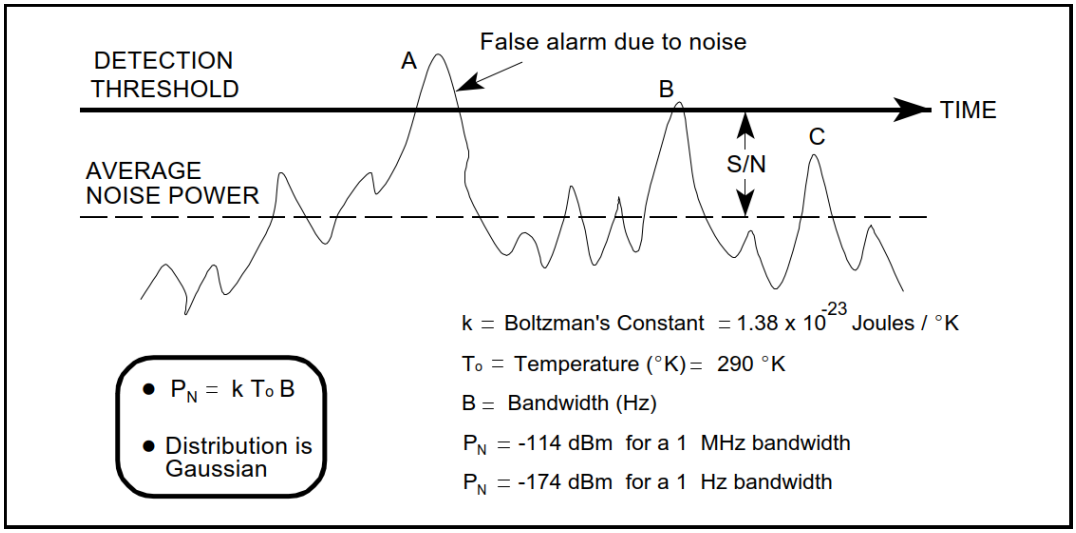


Figure 5.2 Receiver noise power at room temperature [16].

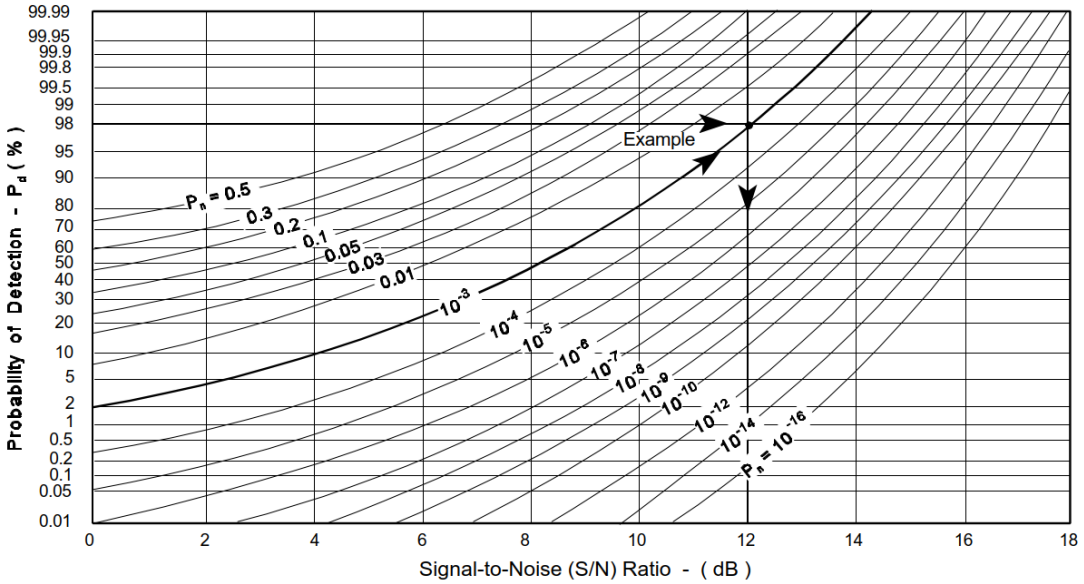


Figure 5.3 Nomograph of Signal-to-Noise Ratio as a function of Probability of Detection (Pd) and Probability of False Alarm Rate (Pn) [16].

Sensitivity from theoretical calculation is -114 dBm. Considering the processing gain due to multiple chirps and gain from directive antennas, Noise figure requirement for the complete receiver chain is relaxed to around 7 dB.

5.1.2 Gain budget and Dynamic range of Rx:

The table below summarizes the signal amplitude levels at inputs of each of the receiver blocks for various signals. The signals include,

- Signal due to direct leakage form TX antenna at 4cm distance.
- Signal reflected from a person at 1m
- Signal reflected from a person at 5m
- Offset generated in base-band circuits due to device-mismatches.

We can already see the limitation on the higher side is the blocker generating the large amplitude at the mixer output which would saturate the baseband signal processing chain. The high pass filter after the mixer should provide sufficient suppression for base-band signal generated due to direct leakage. Considering the entire range of signals, RF-Front end which includes LNA and mixer must provide the gain not larger than 36 dB. The combination of the higher pass filter and low pass filter should provide a programmable gain from 6 dB to 30 dB in the steps of 3 dB to also amplify the signal high enough to cover the dynamic range of the ADC.

	Power at the input of LNTA	Voltage (V_P) at the input of RF-Front end input (50 Ω)	Voltage at the input of HPF	Voltage at the input of LPF after 34 dB suppression	Voltage after DAC offset compensation	Voltage at the input of an ADC
4cm TX leak (5kHz)	-35 dBm	5.623 mV	360 mV	7 mV	7 mV	28 mV
Person@1 m (125kHz)	-65 dBm	177.801 µV	7.54 mV	60.32 mV	60.32 mV	241.3 mV
Chest @5m (1MHz)	-110 dBm	1 µV	64 µV	0.512 mV	0.512 mV	1.024 mV
DC offset	0	0	5mV	40 mV	5mV	20mV

Table 5.1 Signal amplitudes at the inputs of various blocks of receiver (single ended- peak voltages).

5.2 RF Front-End of the Receiver:

RF Front-End(RF-FE) consists of all the blocks in the receiver that process the signal at the original incoming radio frequency before it is down-converted to lower intermediated/baseband frequency.

RF Front End consists of low noise transconductance amplifier followed by a current mode mixer. The noise requirement is directly set by minimum SNR required to detect the target from the specified range. Linearity requirement is set by the ability receiver to sustain the direct leakage from the transmitter which deteriorates the noise figure and gain also leads to a large signal at the mixer output at the beat frequency corresponding to 4cm (the distance between transmitting and receiving antenna).

In complex-baseband implementation with I and Q channels, the received signal is mixed with the cosine and sine versions of the LO, with a duplicated IF chain and separate ADCs for I and Q channel doubling the total power consumption. The benefit of complex baseband architecture is the noise-figure improvement achievable by eliminating the image band noise foldback. Although in theory, the noise-figure improvement can be as much as 3 dB; in practice, noise-figure improvement will smaller and implementation specific, due to signal power loss associated with splitting the received signal into the I and Q paths after LNA and the resulting higher contribution of IF stages to the overall noise figure. So single channel real mixer is considered optimizing for the low power.

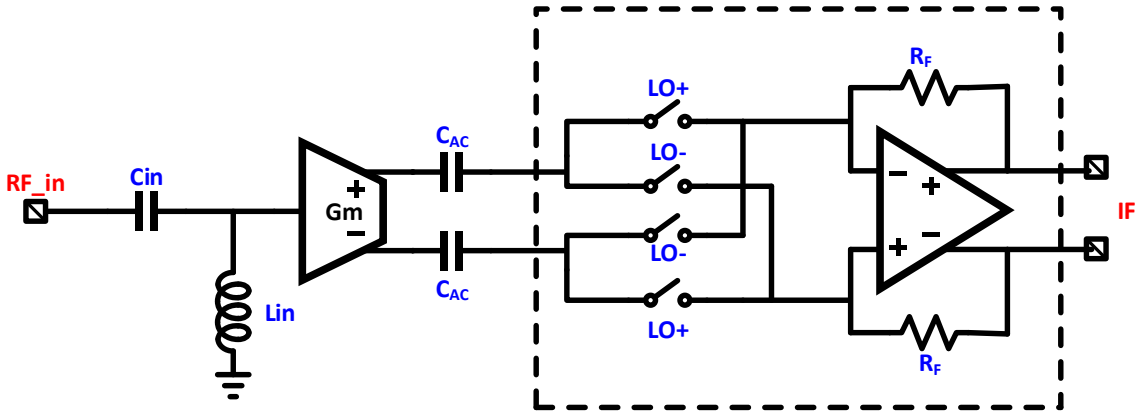


Figure 5.4 RF front-End architecture.

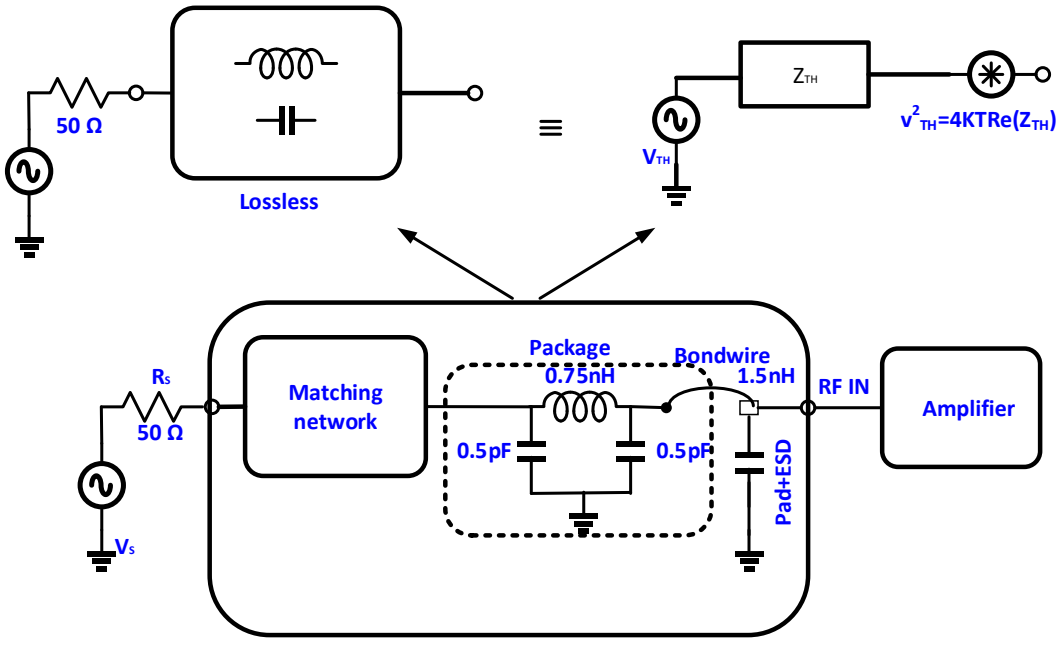


Figure 5.5 Equivalent circuit lumping the matching network, pad, package and other reactive parasitic.

5.2.1 Low Noise Transconductance Amplifier(LNTA) Topology:

The pseudo-differential active balun LNTA is designed to receive the weak signal (range <10uV) and provide sufficient gain to the signal to suppress the noise of next stages. A very high gain was found to be a problem since it would saturate the signal level at the input of next stages of the receive chain. The optimum gain of 36-40 dB was chosen to meet upper and lower constraints.

There are many possible architectures for implementing the LNTA: single ended/differential with common-source and common gate-structures. While single ended LNATs consume less power than differential architectures but suffer from no rejection common mode non-idealities like power supply variation and even order non-linearity. Fully differential topologies also require an off chip balun. The two stage LNTA [17] with first stage being single ended and second stage being differential consumes more power and provides more gain. Inductively degenerated common source LNTA is also a possible solution to push the noise figure below 3 dB but consumes more area due to inductors and has complexities to include bond-wire inductance precisely whose values are not clearly known. On the other hand, single stage pseudo-differential LNTA with single ended input and differential output can be acted as an active balun with no requirement of balun and optimum power consumption. The architecture is modified version of the second stage presented in [17]. LNTA consumes total current of 4.5 mA.

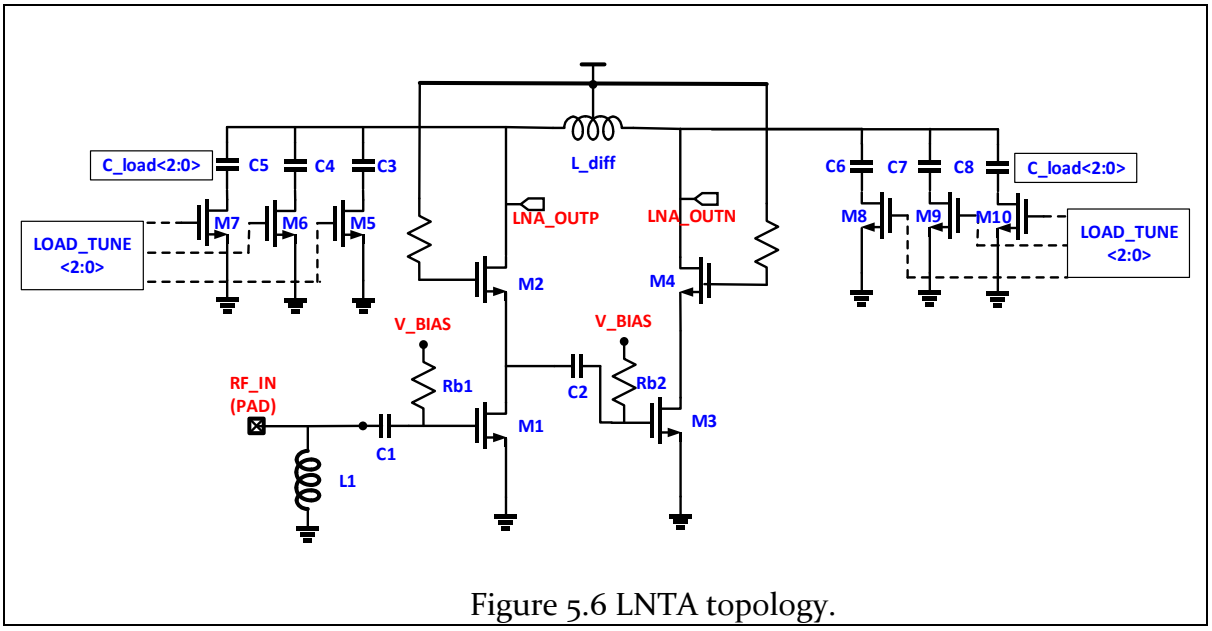


Figure 5.6 LNTA topology.

C1	320 fF	L1	4.9 nH
M1, M2	32 / 0.40 µm	Rb1, Rb2	25 kΩ
C2	300 fF	M3, M4	16 / 0.040 µm
C3, C6	200 fF	C4, C7	25 fF
C5, C8	50 fF	M5, M8	64 / 0.040 µm
M6, M9	32 / 0.040 µm	M7, M10	32 / 0.040 µm

Table 5.2 Component values of a LNTA.

The value of gm of LNTA determines the gain and thermal noise level [11]. Higher value of gm improves the noise figure and increases the gain. But very high gain is a problem since high amplitude blocker due to direct coupling from TX antenna would saturate the receiver chain. So moderate gain is chosen with optimum value for gm = 30mS.
Since the transistors of the input stage should be in the saturation in presence of the blocker, large overdrive voltage(Vov) is necessary. Hence the smaller value for transconductance efficiency(gm/Id) = 10 is chosen with higher Vov around 250 mV.

$$\left(\frac{gm}{Id}\right) = 10$$

$$Id = \left(\frac{gm}{\frac{gm}{Id}}\right) = \quad 3\ mA$$

Since the other symmetric stage receives an amplified version of signal at the gate input of input transistor, it needs only 1.5mA of current making the total current around 4.5mA to provide the required gain.

5.2.2 Input Matching:

The input matching networks serves two functions mainly, transfer the RF power transduced from antenna to the LNTA with minimum reflection. Second is to provide voltage gain to the signal from antenna to LNTA input.

Voltage Gain provided by the matching network is G_{mn}

$$G_{mn} = \sqrt{\left(\frac{R_{IN\_LNTA}}{R_S}\right) - 1} \quad = \sqrt{\left(\frac{450}{50}\right) - 1} = 3 = 9dB$$ Equation 5.2

Where R_{IN_LNTA} is the resistance seen by the matching network into input of the LNTA which is 450 Ω and Rs is source resistance which is 50 Ω. After reduction in Q by using passive components on-chip to have desired bandwidth, off-chip L-matching network is used for impedance matching from antenna to RF-input of the chip as shown in the figure.

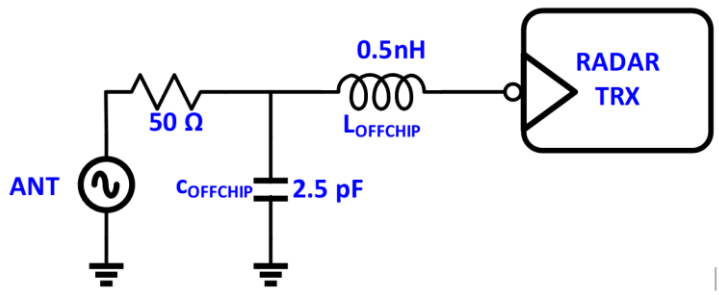


Figure 5.7 Off-chip matching network.

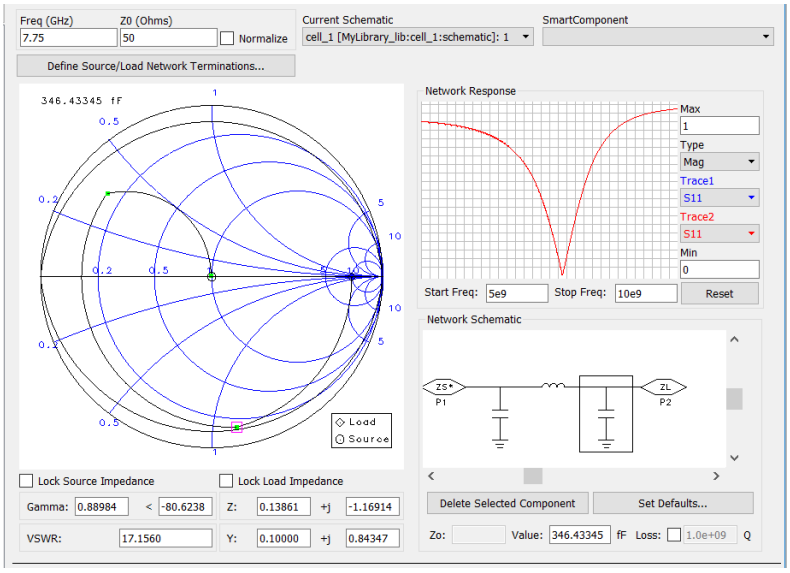


Figure 5.8 smith chart tool for impedance matching.

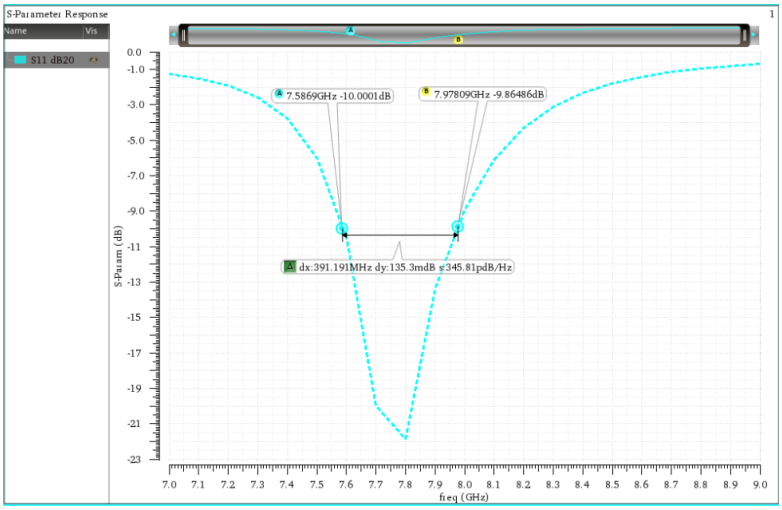


Figure 5.9 S11 after matching at the LNTA input.

Figure 5.8 shows the use of smith-chart tool in the ADS to design the matching network. Figure 5.9 show the plot of S11 in the cadence by fine tuning the values of passives components in the matching network to absorb the bond-wire parasitic.

5.2.3 Design of Loading stage of LNTA.

The LNTA load pose a parallel resonance to an active part of LNTA at a frequency,

$$f_{RF} = \frac{1}{2\,\pi\,L_{LOAD}C_{LOAD}}$$ Equation 5.3

And equivalent resistance is given by

$$R_P = \omega L_{LOAD} Q_{LOAD}$$ Equation 5.4

Since the band width is almost 10 times the center frequency, Q of 10 is selected. To maximize the R_P, it's desirable to have high inductance value for L_{LOAD} which in-turn forces to reduce the C_{LOAD}. But C_{LOAD} cannot be reduced to too lower values which would lose the control over load tunability and finally limited by the stray capacitance of the load node of the LNTA due to cascade devices and next stage connections.

Considering the above constraints, the component values were chosen, $L_{\_LOAD\_DIFF}$ = 2.32 nH, C_{LOAD} = 265 fF absorbing the parasitic capacitances of the load node. Load capacitance is kept tunable so that process variations can be considered and compensated during the measurement. Figure 5.10 shows the variation in AC response at the load of the LNTA with fine tuning the load capacitator around 265 fF.

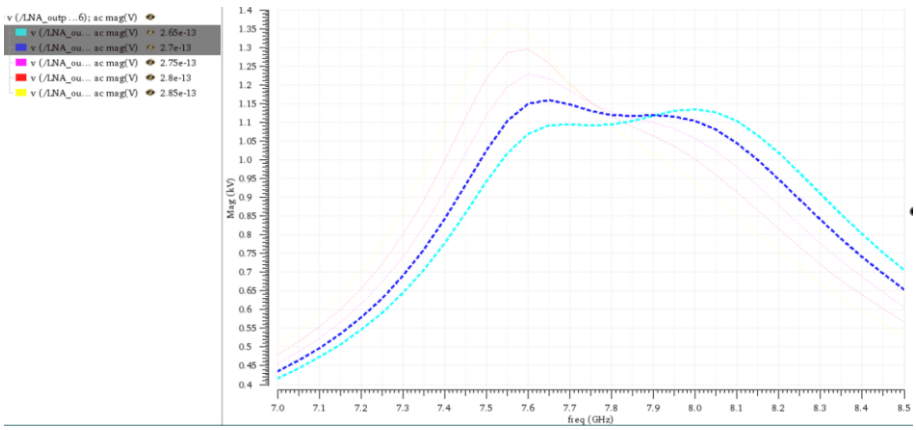


Figure 5.10 Frequency response at the load of the LNTA for various values of load capacitance resonating with load inductance.

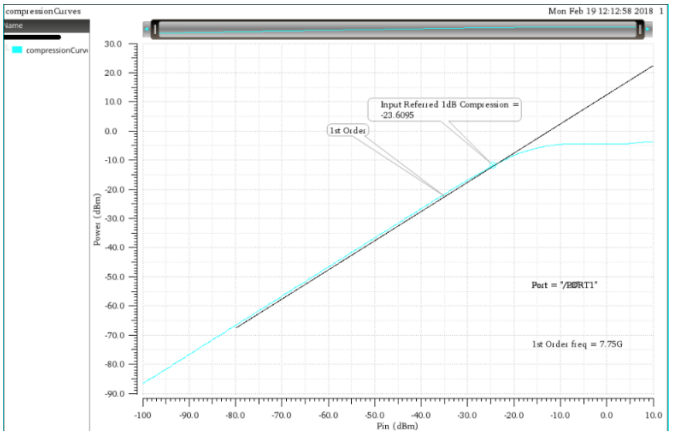


Figure 5.11 compression point for LNTA (P1dB).

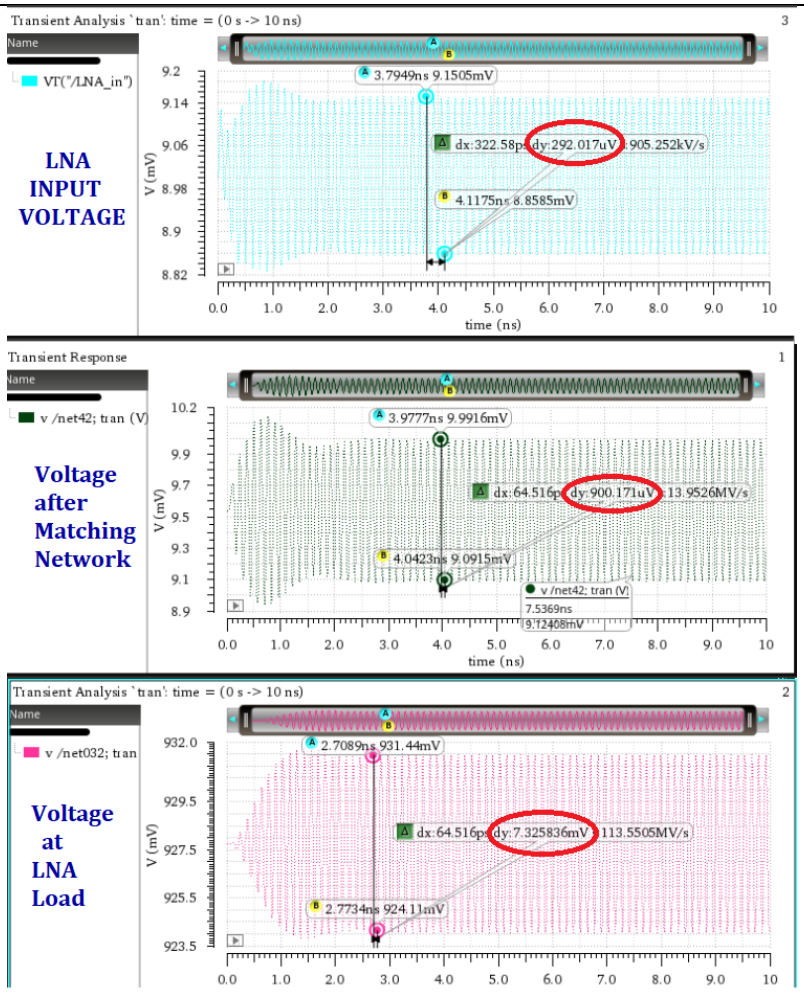


Figure 5.12 transient analysis for the LNTA.

Figure 5.11 shows the 1 dB compression point for the LNA by sweeping the input power from -100 dBm to 10 dBm. 1 dB compression point (input referred) is -23 dBm. Figure 5.12 shows the transient simulation indicating the voltage at the input of the matching network (316 µV), voltage at the output of the matching network (900 µV) and the voltage at the load of the LNA (7.325 mV) when -60 dBm is the power input from the source with source impedance of 50 Ω.

5.2.4 Layout of the LNTA

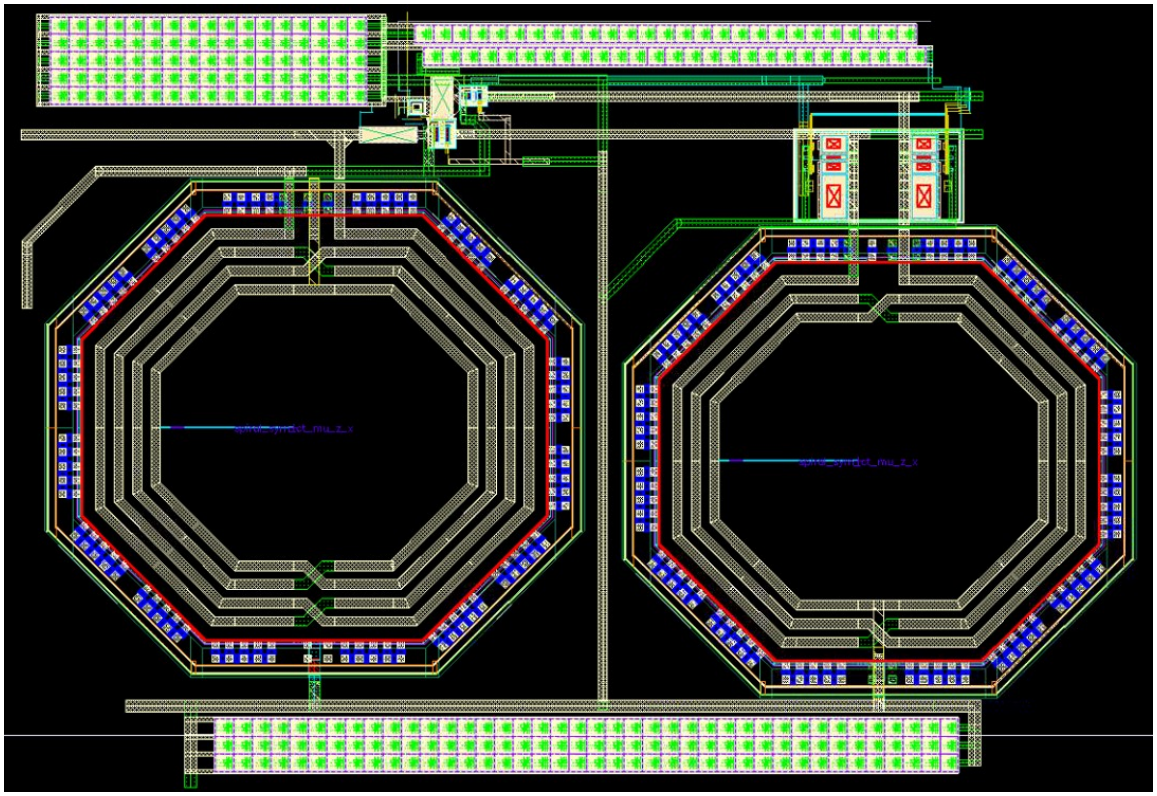


Figure 5.13 Layout of the LNTA

5.3 Mixer

A mixer is a frequency translation block which in conventional communication system terminology translates income high RF signal into low frequency Intermediate frequency signal to ease the processing and digitization process.

In this application, the transmitted signal is frequency modulated in which frequency is ramped up at the rate of 750 MHz/40uS. Reflected signal (radar echo from the target received after roundtrip propagation) is mixed with present LO signal which results in the beat frequency(f_B).

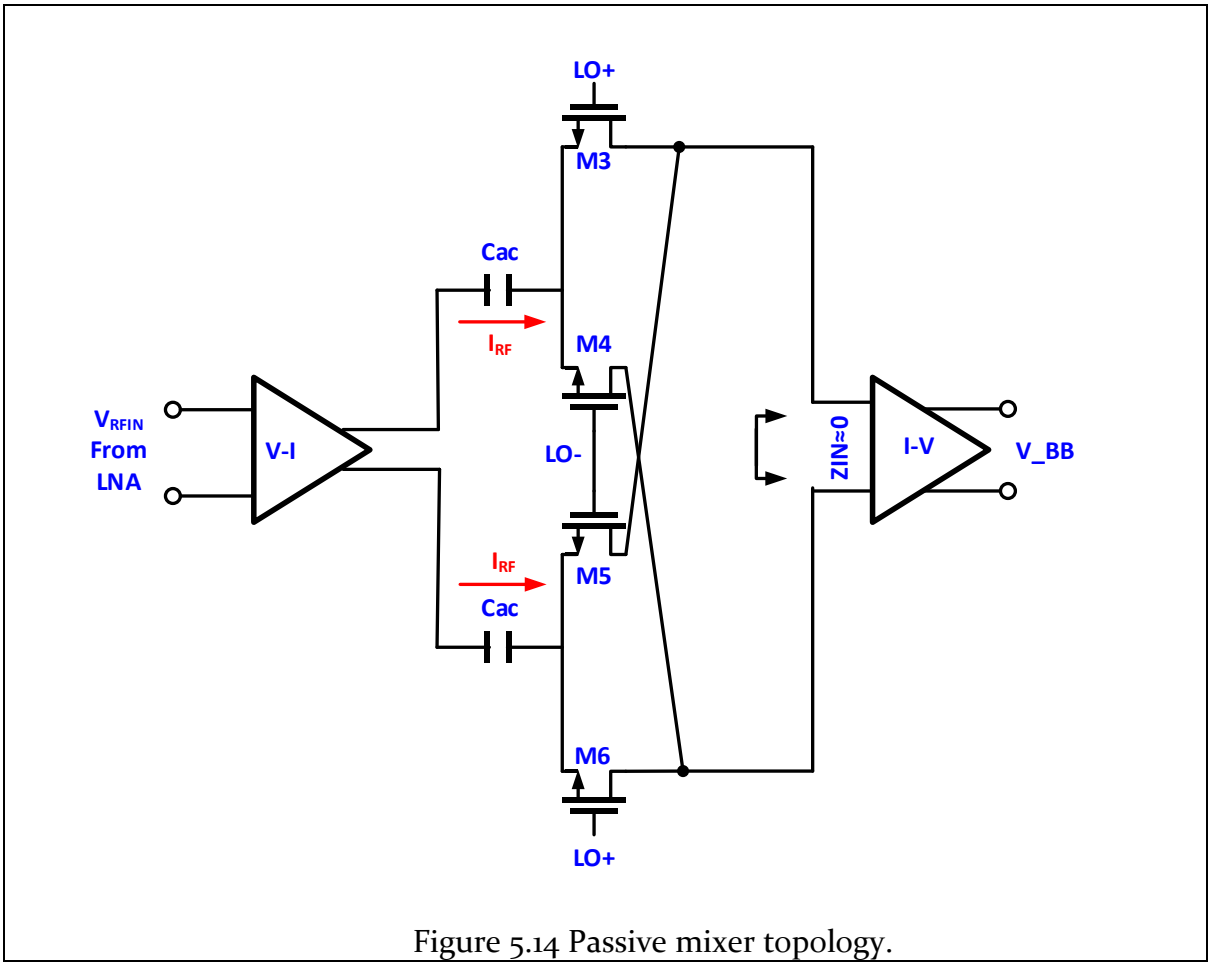


Figure 5.14 Passive mixer topology.

The operation of Passive mixers relies on switches that dissipate no power ideally. However, the notion of passive is somewhat misleading since there are typically several active circuits are associated with the passive mixer which makes non-zero power consumption. Furthermore, the switches require rail-to-rail sharp waveforms which needs power hungry LO delivery circuits like LO drive buffers compared to active mixers.

The choice of passive mixers can be justified by looking at two fundamental drawbacks with the active mixers and improved in passive mixer topology.

1. The linearity of Active mixers is modest due to several devices stacked between supply and ground.
2. Poor 1/f Noise performance since there is always DC bias current flowing through the transistors of the active mixer.

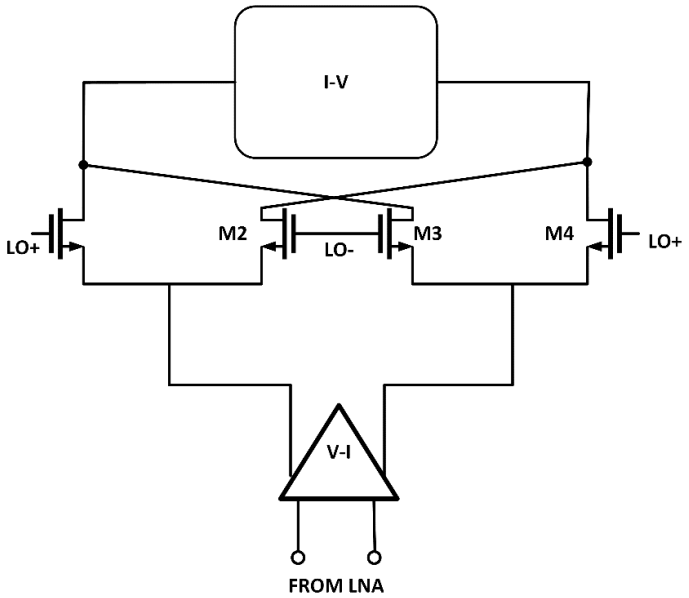


Figure 5.15 Active mixer topology.

The active mixer shown in Figure 5.15 consists of three basic stages

1. Transconductance stage which converts incoming voltage from LNA to RF voltage to RF Current
2. Switching quad that commutes the current switching at the frequency of LO
3. Load (Passive or active) which converts the IF current to IF voltage.

Stacking of all the three stages in a cascode fashion leads to poor linearity and poor 1/f noise. Instead of cascoding, if the three stages are cascaded as shown in Figure 5.14, both the problems are resolved. Placing a blocking capacitor in the signal path ensures that the switches are biased at ZERO DC current which leads to passive mixer arrangement free of flicker noise. The fundamental difference between passive and active mixers is that the former commutates the AC signal (Current or Voltage) only while the latter commutates both AC signal and DC bias which makes it ideal regarding the effect of 1/f noise which is near DC.

In this design, while it is desirable to have high gain in the front-end stage to suppress the noise of subsequent stages, large gain is also undesirable since the interference signal (direct leakage from Tx) which is near to received signal in frequency will also get amplified and would saturate the subsequent baseband signal processing circuits (LPF, HPF, ADC). So, Gm Stage (V->I conversion) of the mixer is combined with Low Noise Transconductance amplifier(LNTA) ensuring that the amplifier operates in the current mode. To ensure the current mode operation Z_{IN}(TIA) << R_L(LNTA).

Transimpedance Amplifier(TIA) is needed to receive the input current from switching and convert it to voltage in addition to presenting a very low input impedance to the mixer switches to guarantee the current domain operation of the mixer. The situation is opposite in voltage-mode operation where the mixer needs to present a high impedance to ensure voltage-mode operation.

5.3.1 Transconductance (Gm) Stage:

Gm stage is the first sub-stage of the mixer which converts the RF voltage amplified by the low noise amplifier to current followed by switching stage to commutate the current and later back to the voltage at the load of the mixer. Initially we started the self-biased inverting state as Gm stage and found that the gain of the front-end is very high and direct leakage would saturate the self-biased inverters. So LNTA itself acts as Gm stage of mixer. In this case, the impedance looking at the mixer input from LNTA output should be low enough such that, LNTA acts as a trans-conductor and small signal current flows into the input of Trans-Impedance Amplifier (TIA) and feedback resistors generating base band voltage signal at the beat frequency.

5.3.2 AC Capacitance

The Function of coupling capacitor between the LNTA and mixer is to allow only the small signal component from the low noise amplifier stage to the mixer stage. There exists an optimum value of this capacitance for maximum coupling of small signal. This capacitor has should present equivalent reactance at LO frequency along with parallel combination of load impedance.

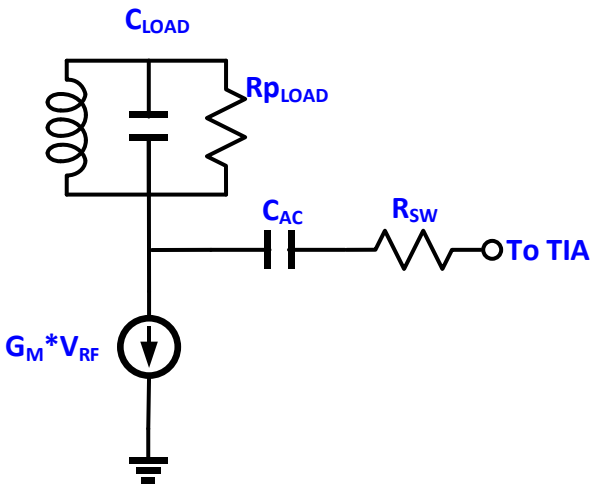


Figure 5.16 AC Coupling capacitor from LNA to mixer stage.

The combination of values of Z_{LOAD} and C_{AC} should be optimized such that $Z_L || (1/C\omega_{LO})$ should resonate at ω_{LO} as explained in detail [18] [19]. Value for C_{AC} is selected based on Rp and Rsw. The optimum value for C_{AC} based on values of Rp and Rsw simplifies to Equation 5.5.

$$\left(\frac{1}{C_{AC}.\omega_{LO}}\right) = \sqrt{(R_P R_{SW})} \qquad \text{Equation 5.5}$$

Substituting for $R_P = \omega_{LO} * L_{LOAD} * Q = 866\ \Omega$ and $R_{SW} = 10$, we get $C_{AC} = 220$ fF.

5.3.3 Design of switching stage:

The resistance of mixer switch is the main design parameter, to trade off with buffer strength required to drive the switches. The higher the size of the switches, lower is the R_{ON} (on resistance) of the switch, but gate capacitance(C_{gg}) will be higher hence resulting in the high-power consumption for buffers to drive the wide switches. While reducing the size of the switches increases the R_{ON} and hence increasing the noise with low power consumption for the buffers to drive the small sized switches. With W/L = 80µm/40nm, R_{ON} is estimated to be around 10Ω with low noise contribution.

The i_D-v_{DS} characteristics of a MOSFET in the ohmic region are given by

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left((v_{GS} - V_t)v_{DS} - \frac{v_{Ds}^2}{2}\right) \qquad \begin{array}{r} for\ v_{DS} > V_t\ \ and \\ v_{DS} < v_{GS} - V_t \end{array} \qquad \text{Equation 5.6}$$

The large signal channel resistance in the triode region is given by

$$r_{DS} = \frac{\partial v_{DS}}{\partial i_D} = \frac{1}{\left(\frac{\partial i_D}{\partial v_{DS}}\right)} \qquad \begin{array}{r} for\ v_{DS} > V_t\ \ and \\ v_{DS} < v_{GS} - V_t \end{array} \qquad \text{Equation 5.7}$$

$$r_{DS} \approx \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_t)} \qquad for\ v_{DS} \ll 2(v_{GS} - V_t) \qquad \text{Equation 5.8}$$

As we can see from the Equation 5.8, the ON resistance of switch is an inverse function of width of the MOST and gate over drive voltage. The W/L = 80µm/40nm was selected which would results in the ON resistance of around 10 Ohm.

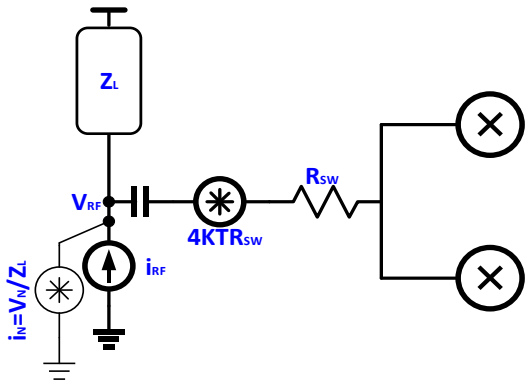


Figure 5.17 Noise contribution from switching stage.

Although mixer with multi-phase LO results in the better noise figure and conversion gain [19], Since the frequency of operation is relatively high here(7.4GHz – 8.15 GHz), only Bi-phase LO is used. The noise figure for the mixer is given by [20]

$$F = \left(\frac{\pi}{2}\right)^2 . \left(1 + \frac{rds_{(ON)}}{R_s}\right) \qquad \text{Equation 5.9}$$

Lower value of R_{ds} from the switch results in lower noise contribution from the mixer stage.

5.3.4 Trans-impedance Amplifier

The final stage of the mixer consists of the I-V Converter that converts the IF Current to IF voltage. In conventional active mixers this is implemented with passive [17]. But the disadvantage of such scheme is that it needs a voltage headroom and hence not ideal when we expect the high amplitude blocker due transmitter leakage. So, following the mixer stage, A Transimpedance amplifier (I→V Converter) is intended to convert the AC – baseband current (I_{BB}) to baseband voltage(V_{BB}). Another point as already mentioned, only AC signal current is commutated by the switches and this current(I_{BB}) is fed to trans-impedance amplifier with feedback resistance (R_F).

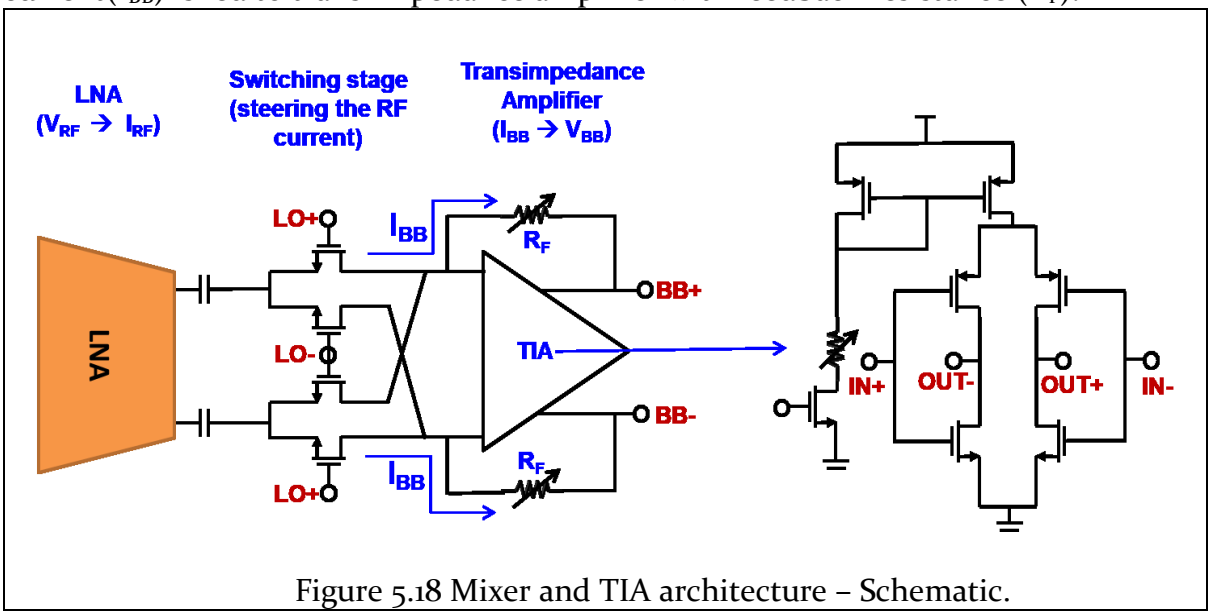


Figure 5.18 Mixer and TIA architecture – Schematic.

Figure 5.18 shows the architecture of the mixer along with the schematic of the TIA. TIA is a self-biased complementary pair of transistors(PMOS+NMOS) with tunable current source. Although the use of two stage operational amplifier for TIA is one of the solution we started with, encountered the problems in regard to driving capability of small feed-back resistors with sufficient phase margin for stability.

5.3.5 Layout of the mixer

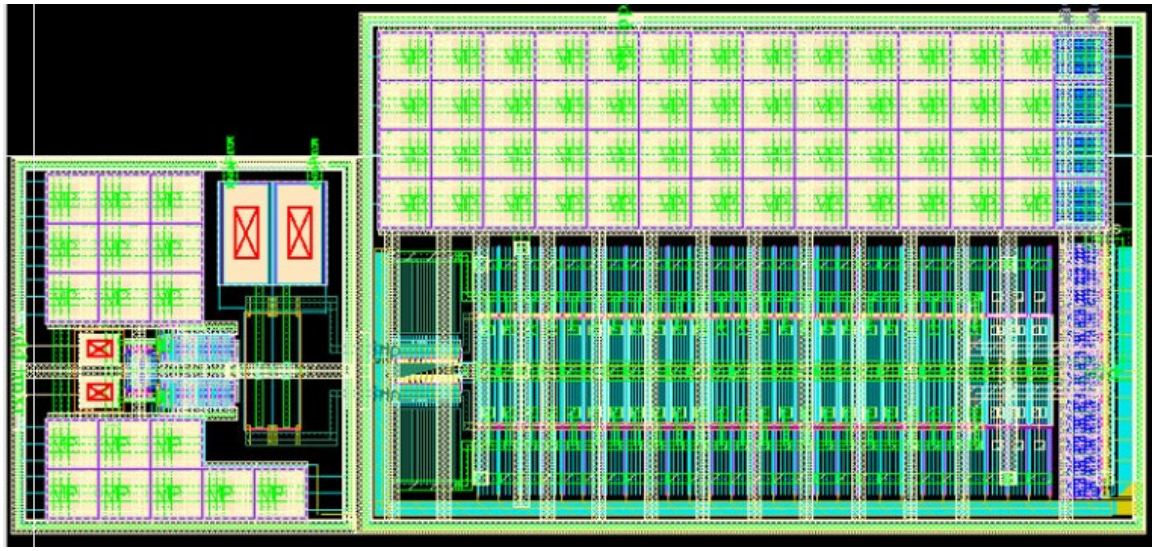


Figure 5.19 Layout of the mixer

5.3.6 Simulation results

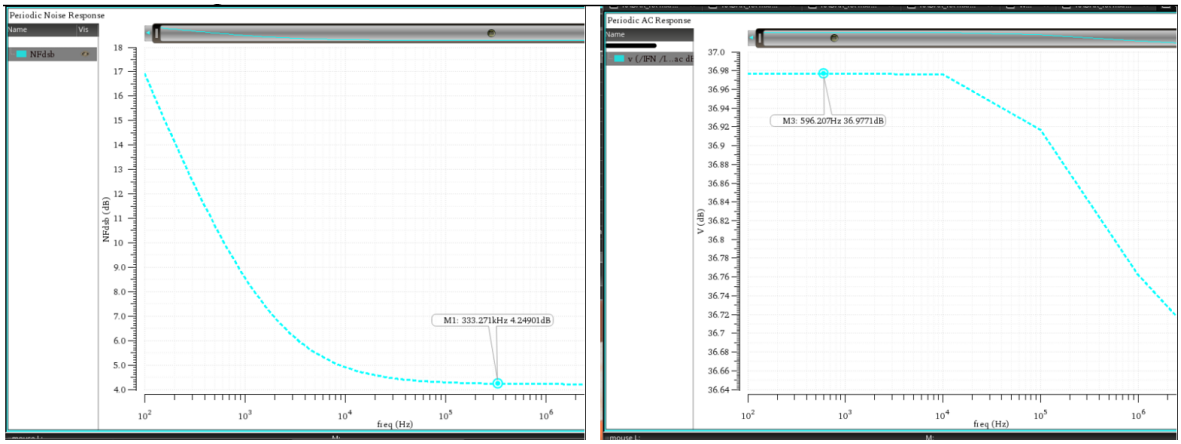


Figure 5.20 simulation result for noise figure and gain of front-end.

Figure 5.20 shows the results of simulations to estimate the noise and a gain for the front-end of the receiver by analysis using PSS+PNOISE+PAC simulations. Figure on the left indicates the noise figure about 4.2 dB. Figure on the right shows the gain of the front end about 36 dB.

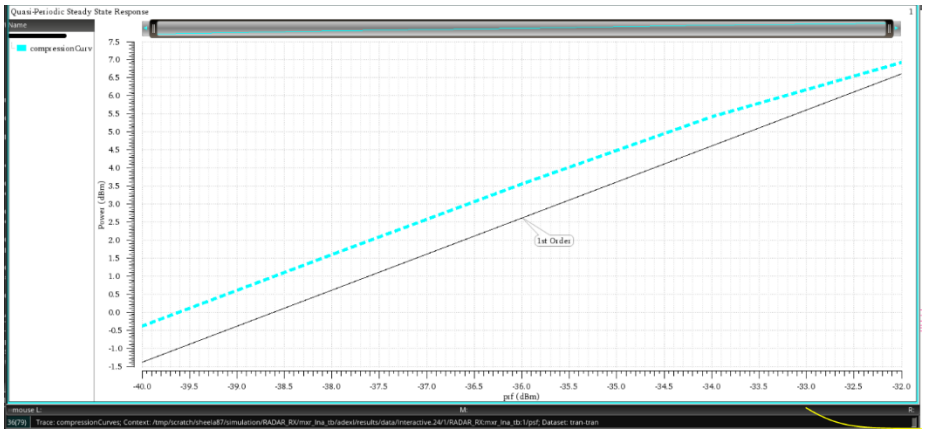


Figure 5.21 P1 dB (1 dB compression point) for the front end.

Figure 5.21 shows the simulation result of the RF front end (LNA + mixer) which indicates that the 1 dB compression point around -32 dBm.

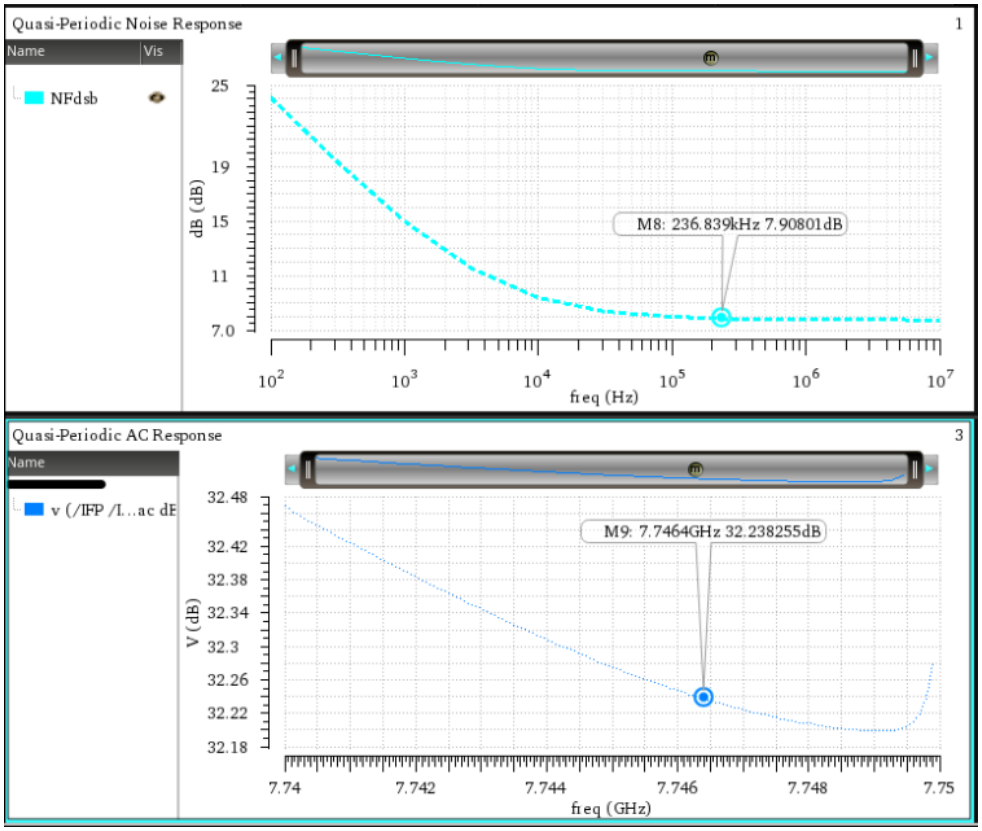


Figure 5.22 Increase in NF and drop in the gain due to presence of blocker

Figure 5.22 shows the effect of blocker on NF and gain. The figure in the top indicates the increase in noise figure due to the presence of the blocker (-27 dBm direct

leakage from TX antenna and the figure in bottom shows decrease in the gain which is obtained by qpss+qpnoise+qpac analysis.

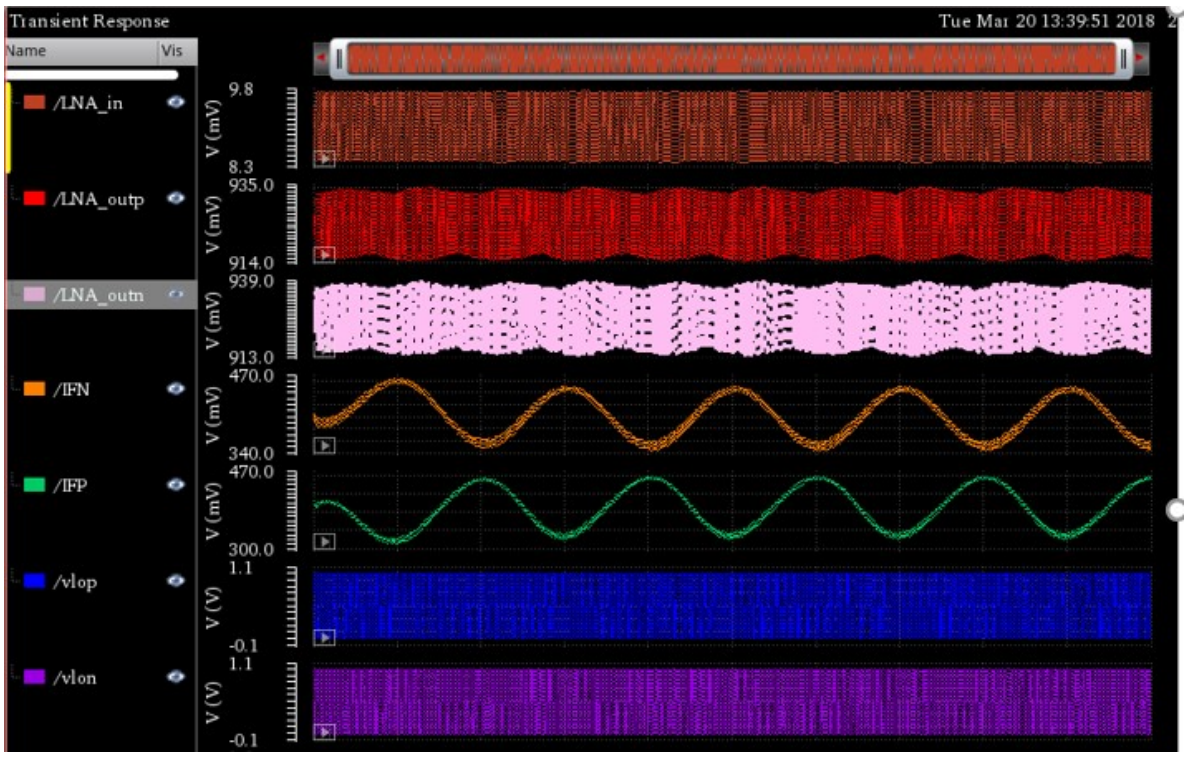


Figure 5.23 transient simulation results al the RF-Front end.

Figure 5.23 transient simulation results al the RF-Front endshows the transient simulation and time domain signals at various stages of RF-Front end. LNA_in is the RF input signal to the LNTA. LNA_outp and LNA_outn are the output signals from LNTA fed into the mixer. IFN and IFP are the base-band signals at the beat frequency. Signals vlop and vlon are the LO driving signals to mixer switches.

5.3.7 Mixer Buffer Design

The buffer is a critical and power-hungry block whose main function is to regenerate the voltage levels of the LO signal routed from the DCO to sufficient strength to be able to drive the wide mixer switches with low ON resistance. The power consumption of buffer directly trades with width of the switching transistors. Wider is the size of switching transistors, higher is the Gate capacitance (Cgg) and larger is the power required by the buffer to drive the switches with low rise and fall times.

As discussed in the case of multi-stage design of inverter chain [21], there is an optimum number of stages with which the buffers consume minimal power. A power efficient 4-stage mixer buffer is designed to regenerate the LO signal levels and drive the mixer switches which consumes 1.5 mW of power for each of the phases of LO.

Figure 5.25 shows the phase noise simulation result indicating the value of -129.5 dBc/Hz at 1 MHz offset.

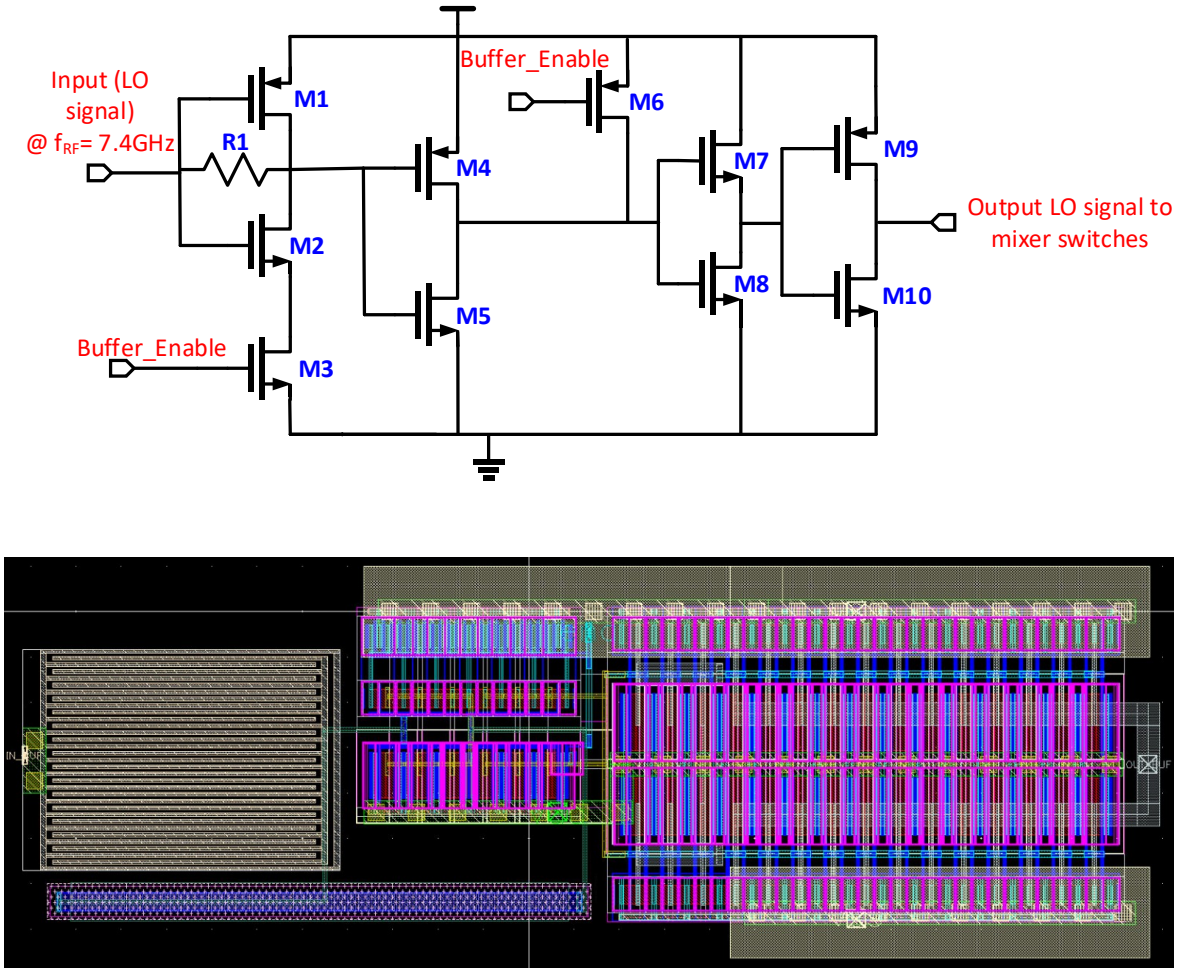


Figure 5.24 circuit schematic and layout for the mixer buffer.

Circuit reference	Size (W/ L) in µm/ µm	Circuit reference	Size (W/ L) in µm/ µm
M1	6/0.040	M6	0.26/0.040
M2	2.4/0.040	M7	15/0.040
M3	12/0.040	M8	4.8/0.040
M4	6/0.040	M9	60/0.040
M5	2.4/0.040	M10	19.2/0.040

Table 5.3 component values for mixer buffer.

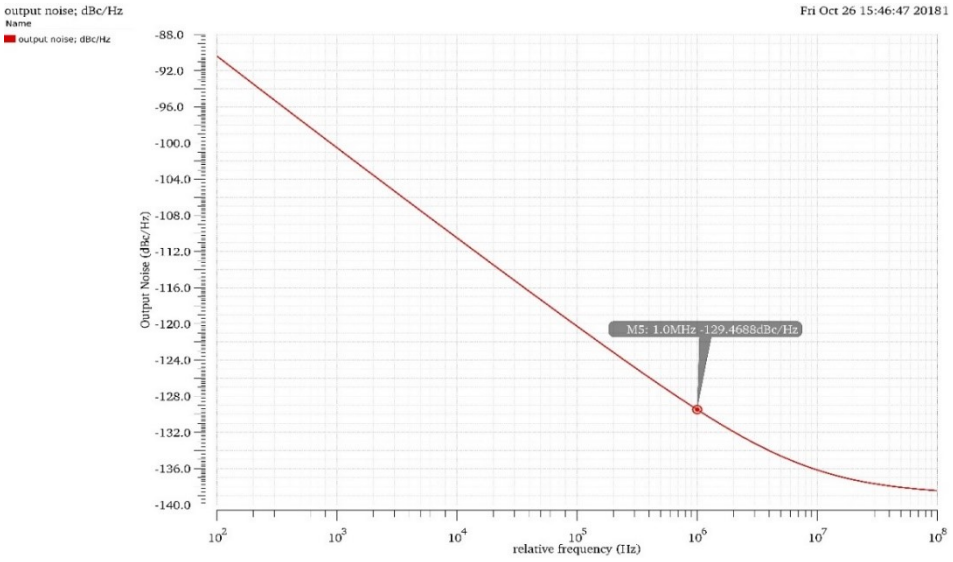


Figure 5.25 Phase noise profile at the output of the buffer.

5.4 Baseband signal processing circuits

The complete base band chain consists of a high pass filter, a low pass filter and an ADC. The main role of HPF is to suppress the signal at frequencies that is the result of leakage mixing which is analogous to self-mixing in direct conversion receivers. All the base-band signal processing blocks are re-used from previous designs of IMEC and integrated with RF-Front end.

5.4.1 Band pass filter

The first baseband block in the base band processing chain is the HPF. Since the blocker due to direct coupling from Tx antenna to Rx antenna after mixing with LO results in a near to DC (at beat frequency corresponding to distance between Tx and Rx antenna), this near DC component has to be filtered out in the early stages of baseband signal processing chain so that it does not saturate the further blocks until the ADC input. Hence the high pass filter is used to suppress the undesired near DC frequency component to a sufficiently low voltage level.

The beat frequency corresponding to the leakage is given by,

$$f_{b_{leakage}} = \frac{2 * R}{C} * \frac{df}{dt} \qquad \text{Equation 5.10}$$

Substituting R = 4 cm, C = 3e8, $\frac{\mathrm{df}}{\mathrm{dt}} = 750\frac{\mathrm{MHz}}{40\mathrm{us}}$ results in frequency component of $f_{bleakage}$= 5 kHz. Hence the corner frequency is set to suppress this signal.

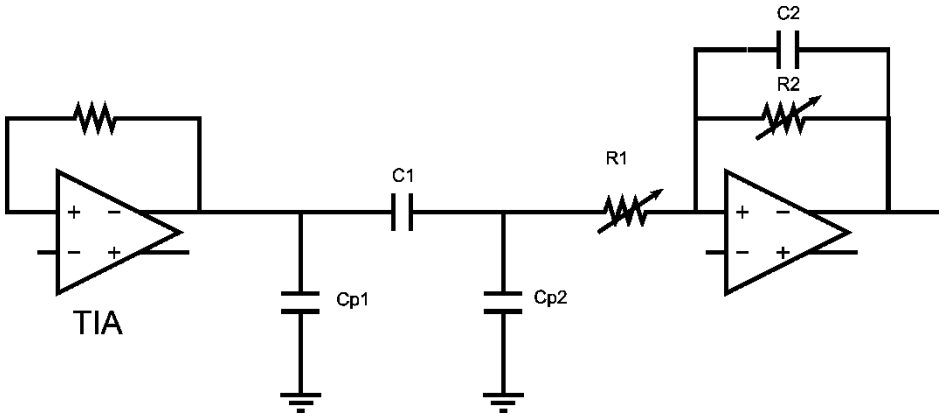


Figure 5.26 high pass filter following TIA output.

Fully differential band pass filer is implemented starting form previously designed Low-pass filter where of which the half circuit is shown in the Figure 5.26:

R1 C1 define high pass corner of around 160 KHz.

$$f_C = \frac{1}{2\pi R_1 C_1}$$ Equation 5.11

R2 C2 define low pass corner around 2MHz.

$$f_C = \frac{1}{2\pi R_2 C_2}$$ Equation 5.12

R1, R2 define the gain:

$$Gain = \frac{R_2}{R_1}$$ Equation 5.13

Circuit reference	Value	Circuit reference	Value
C1	12.5/25/50 pF	R2	20k – 160kΩ in steps of 20 kΩ
R1	20 kΩ	C2	1 pF

Figure 5.27 component values for HPF

Figure 5.28 shows the AC response of bandpass transfer with the gain of 8 (18 dB) and bandwidth of 2 MHz. Figure 5.29 shows the NF of the RF-Front end (post layout) on the left and gain of the overall receiver chain in the right. The total maximum gain of the receiver chain is 75 dB.

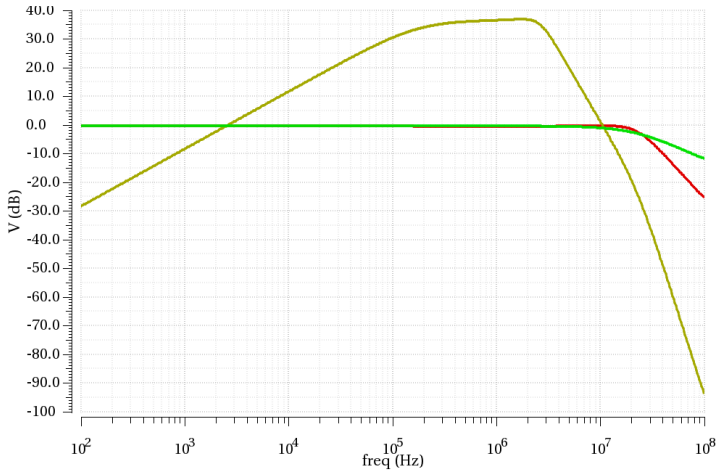


Figure 5.28 AC response simulation result of the Band Pass Filter.

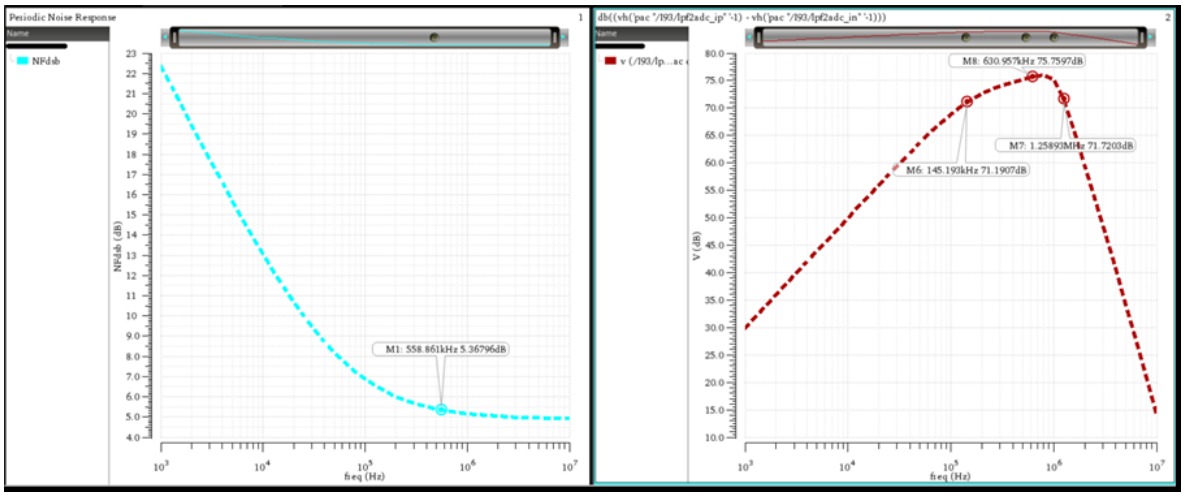
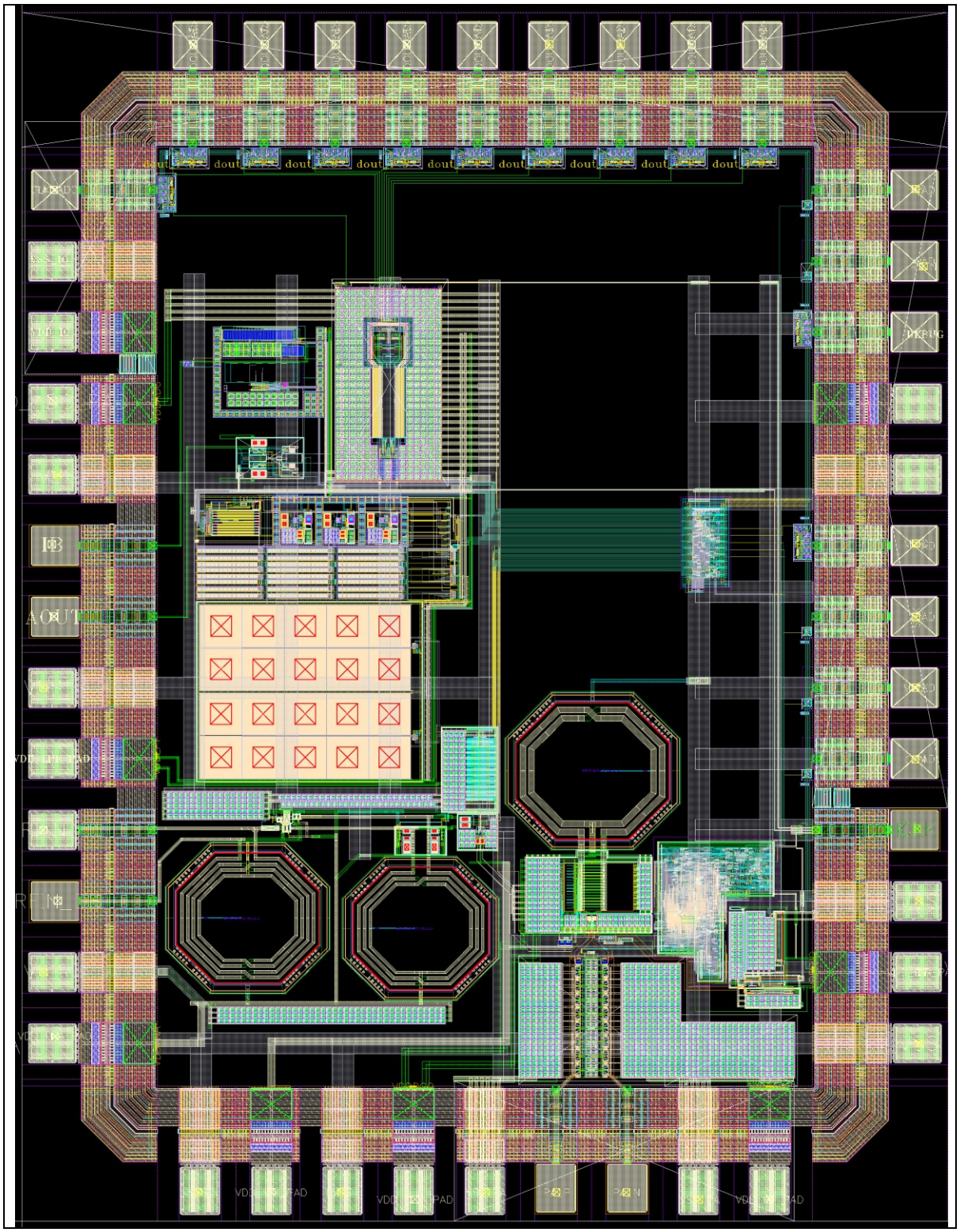


Figure 5.29 Front-End noise figure and Gain simulation results.

5.4.2 Successive-Approximation-Register Analog to Digital Converter (SAR - ADC)

After amplifying the baseband signal at beat frequency, and limiting the bandwidth, the signal is digitized using an analog to digital converter. A power efficient, 9-bit SAR ADC [22] with sampling rate of 12.5 MS/s is used while consuming the power of 50 µW. The data from the ADC is read out into a FPGA IO port synchronously with the clock and processed offline using the MATLAB.

5.5 Layout of the complete radar transceiver



Chapter 6 Measurement Results

6.1 Measurement set up

Measurement set up consists of

- PCB designed for the chip RADAR_TRX which consists of LDOs to generate the reference and supply voltages for all the blocks, Crystal oscillator to generate 50 MHz reference, level shifters to interface the digital control signals, SPI signals and IO signals on chip with 1V amplitude with FPGA which accepts signals of amplitude 1.8V and SMA connectors to connect the TX and RX antennas.
- FPGA Development board
  The function of FPGA board is to read out the data from an ADC sampling at the rate of 12.5MHz and transfer the data to a PC for the offline processing of the data. FPGA can also be used to program the chip on the SPI to automate the complete measurement. However Teensy controller is mostly used for the debug purpose to set each of the controls from the GUI and read out the registers instantaneously.
- Teensy Controller
  The function of Teensy controller is to configure the static registers in the RADAR_TRX chip by reading the data on UART interfaced with PC to which the data is written from the graphical user interface. Teensy can also be used to generate the pre-trigger pulses with reasonable timing accuracy.
- PC with MATLAB: The data from FPGA is transferred to the PC for the offline processing the data acquired by an ADC to extract the phase information to estimate the heartbeat rate and respiration rate.
- Test equipment like Spectrum analyzer and an oscilloscope for monitoring signals during the measurement and a signal generator to synthesize signals during debug.

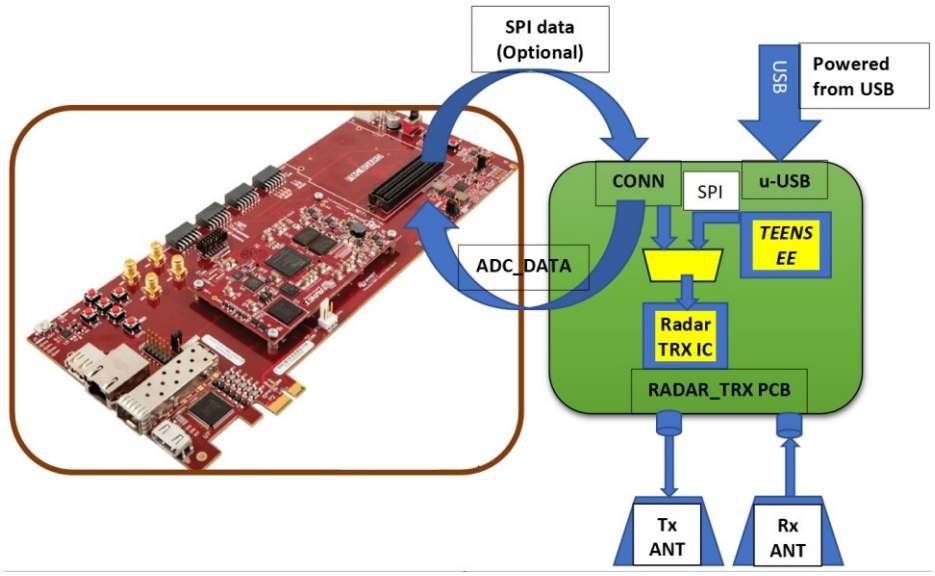


Figure 6.1 Block diagram of the measurement set-up.

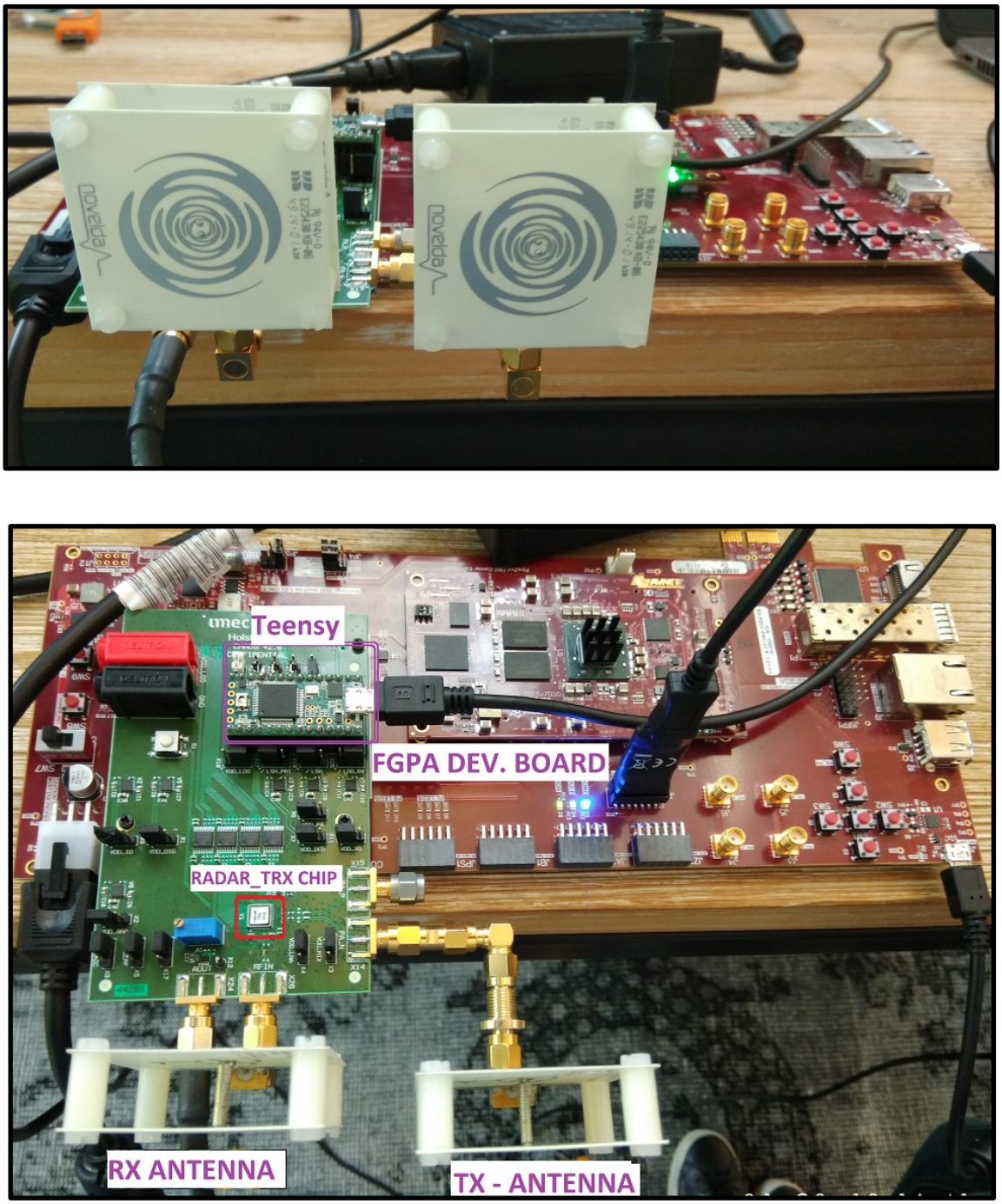


Figure 6.2 measurement set-up for system measurements.

Figure 6.2 shows the actual set up with RADAR_TRX chip mounted on the PCB, configured by teensy through SPI and connected to a FPGA for data acquisition and transfer to PC.

6.2 Measurement results of the chip

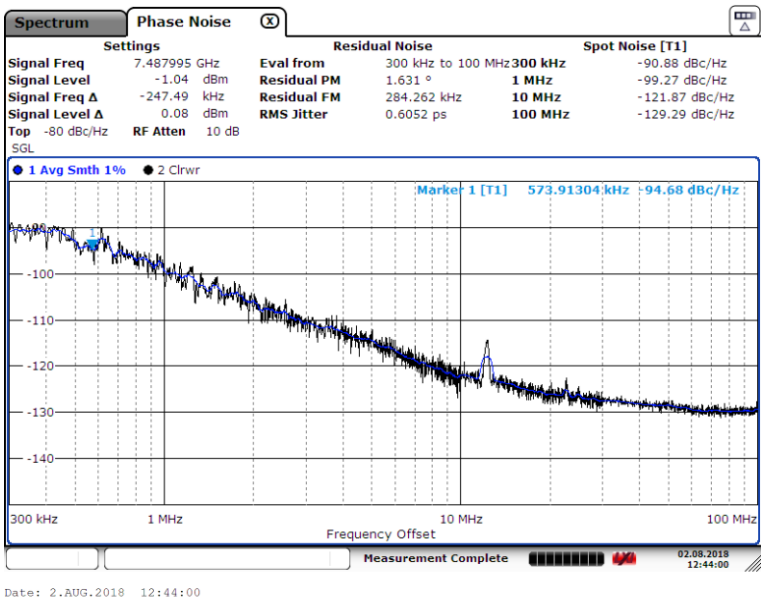


Figure 6.3 Phase noise measurement for the DCO.

Figure 6.3 shows the phase noise measurement of the DCO with phase noise of -100 dBc/Hz at 1 MHz offset.

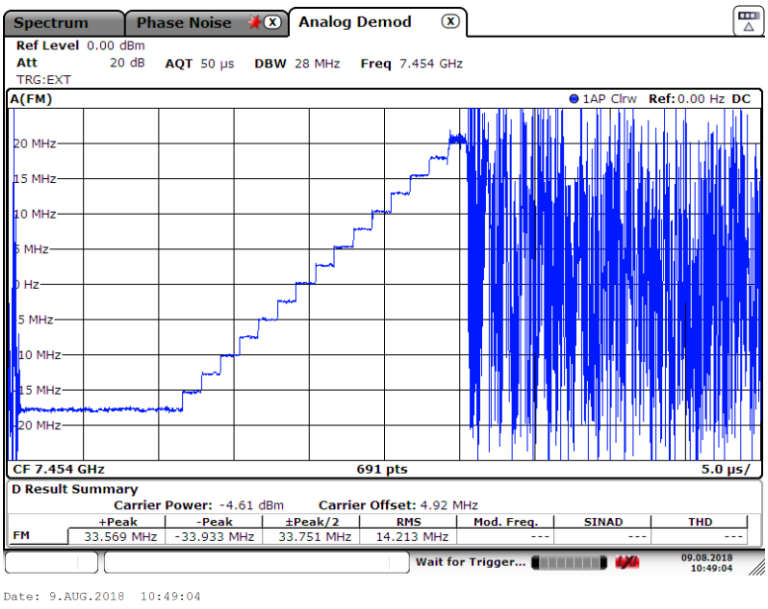


Figure 6.4 Frequency stepping during the chirp generation.

Figure 6.4 shows the frequency profile during the chirp generation by open loop modulation using unit capacitor array with frequency step of 2.5 MHz.

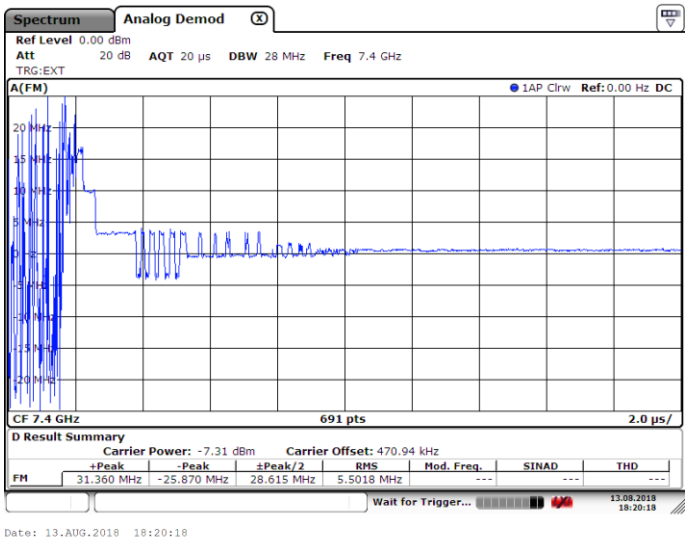


Figure 6.5 Frequency locked loop precisely locking to initial frequency with gear shifting progressively from larger frequency steps to smaller steps.

Figure 6.5 shows the closed loop operation of FLL with gear-shifting where the frequency steps are progressively lowered over time for fast settling.

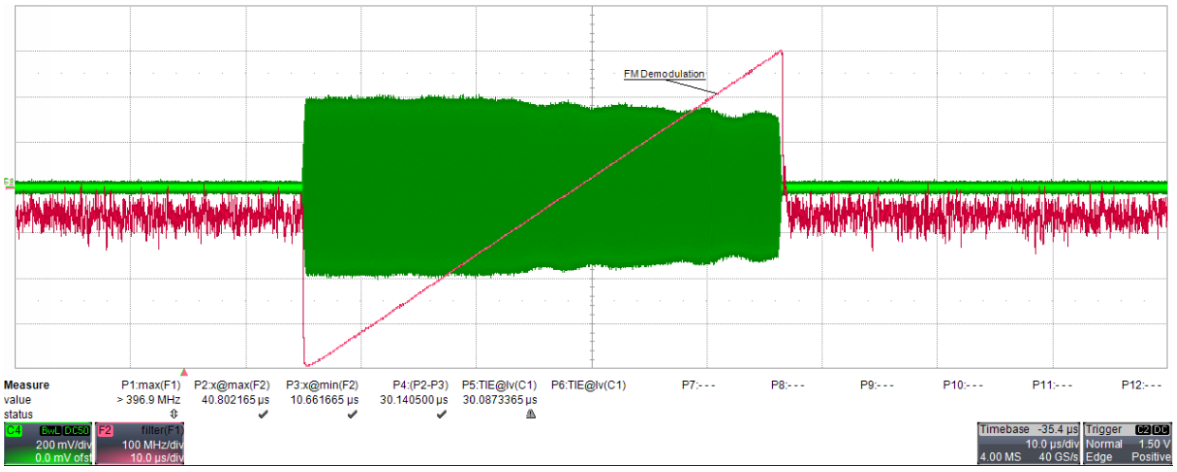


Figure 6.6 Transmit chirp in time domain showing frequency ramping.

Figure 6.6 shows the time domain wave-form (green) of single transmit chirp over the time period of 40 µs. The trace in red shows the frequency ramping up over time.

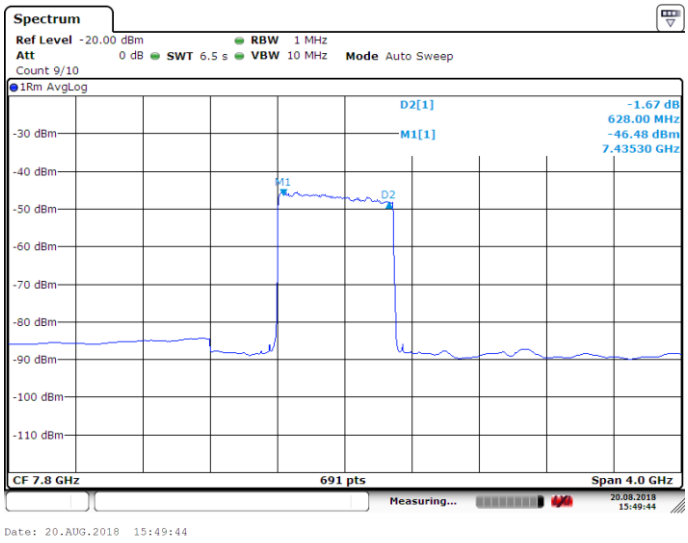


Figure 6.7 spectrum of transmit waveform consisting of series of chirps.

Figure 6.7 shows the spectrum of transmit wave form with series of chirps which is below -41.3 dBm/MHz clearing the spectral mask regulations.

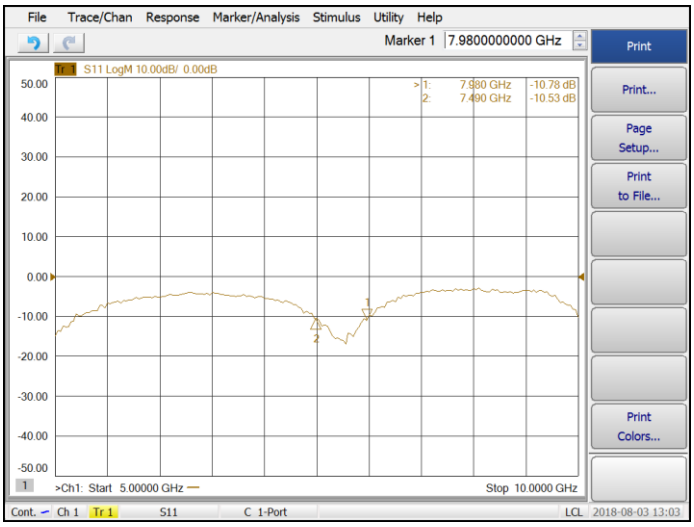


Figure 6.8 S11 at the Receiver input.

Figure 6.8 shows the measurement of S11 after tuning the matching network at the input of the receiver.

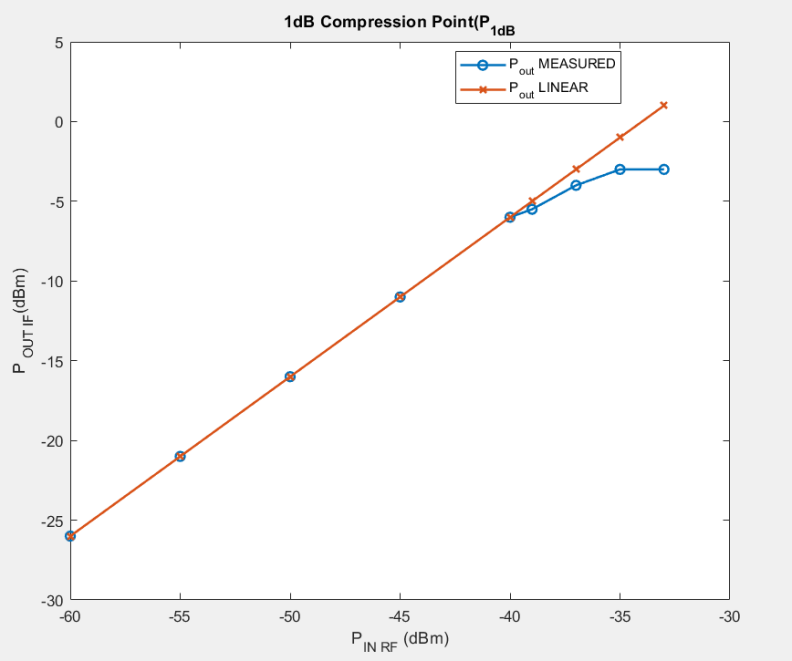


Figure 6.9 1 dB Compression Point

Figure 6.9 shows measured output power at the output of LPF with the minimum gain settings. The RX gain reduces significantly for the inputs greater then input power of -35 dBm. The overall gain of the RX chain is measured was found to be 64 dB which is combination of 30 dB gain from the baseband processing chain and 34 from the receiver front-end.

The measured over-all noise figure of the receiver was found to be 12 dB. It was found from the simulation that the optimum for NF, Gain and effective AC coupling from LNA to mixer depends on the capacitance value of load and AC coupling capacitor. In order to increase the gain, Load inductor of an LNA was chosen higher and correspondingly load capacitance was sized to resonate at the desired frequency around 7.75 GHz. Since the Load capacitance value is relatively low, will have larger variation and mismatch due to process variation for this technology. The load tuning was done differentially with similar sized capacitors. Figure 6.10 shows the effect of change in cload in the steps of 20fF deteriorating the noise figure. Tuning each side of pseudo-differential LNA individually and sizing the coupling capacitors and load capacitor with lower inductance value can reduce the effect of process variation. Another potential problem can be a large current mirror ratio used to generate the bias for the LNA. The current from the bias was 30μA that is mirrored to LNA generating the bias of 3mA which makes the ratio 100 to reduce the power consumption in biasing circuit. There will be significant contribution of noise from the supply due to this large current ration since the overdrive voltage for transistors in current mirror is very low which is proportional to mirror ratio N.

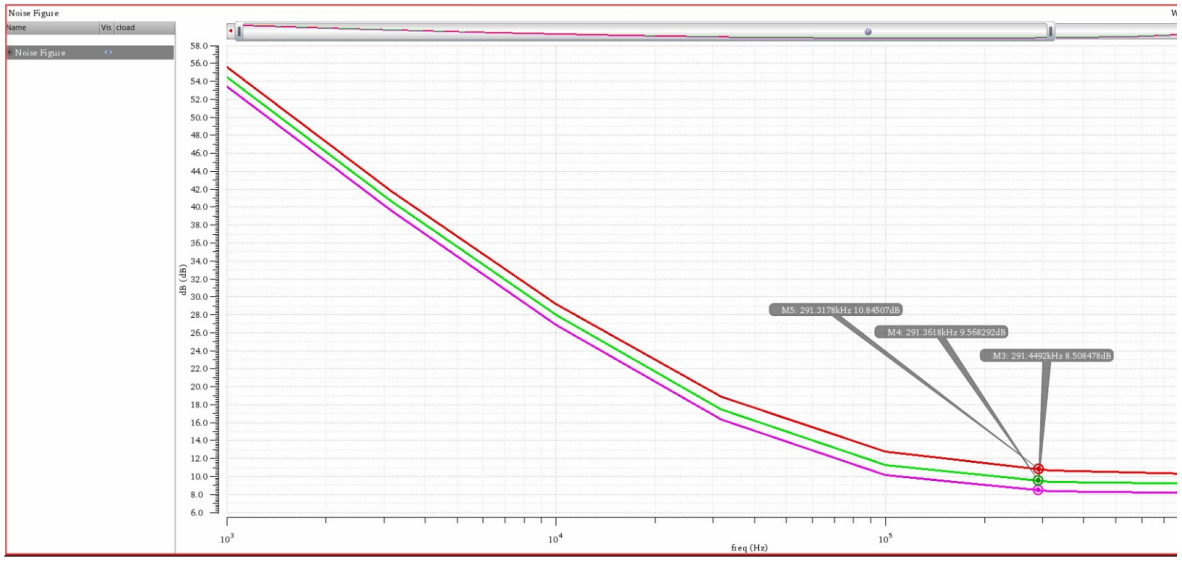


Figure 6.10 Simulation showing the increase in noise figure.

6.3 System level measurements

The Measurement setup up is shown in Figure 6.11 for multiple-people remote vital signs detection. The first person is sitting at a distance of 5 meters in front of the radar, and the second person is at 15meter distance. The respiration of both subjects can be simultaneously detected from the Doppler phase signal at each corresponding range bin. The heartbeat of the person 1 can be seen with frequency component of 1.2 Hz which corresponds heart beat rate of 83 times per minute in Figure 6.12 after digital processing with filtering. Many thanks to Marco for implementation of algorithms to extract the information of heartbeat rate and respiration rate.

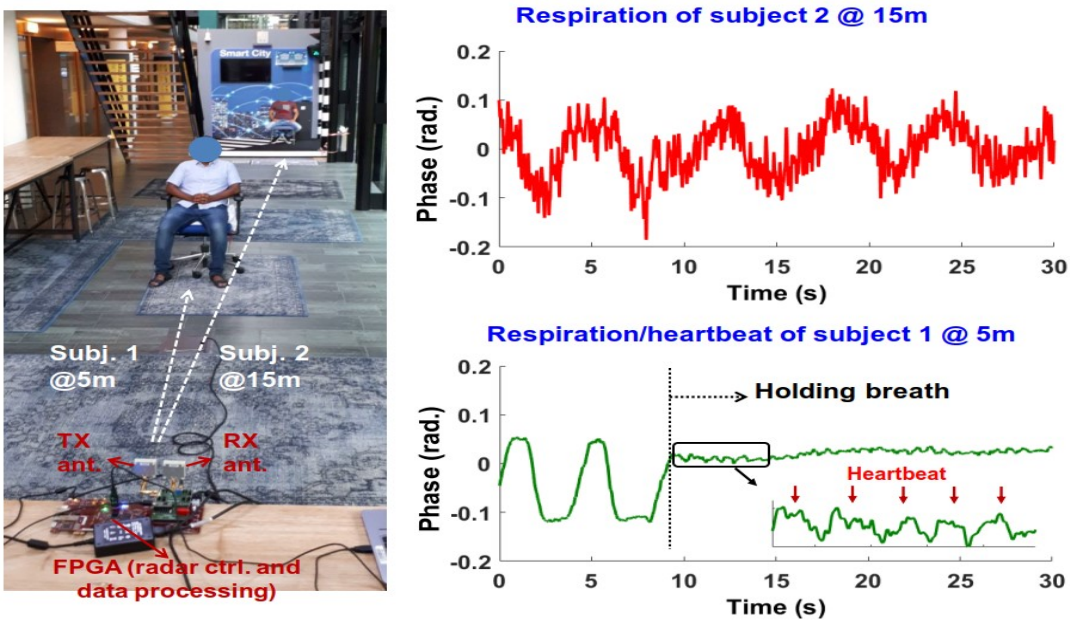


Figure 6.11 System performance measurement monitoring the heartbeat rate and respiration rate of person at 5m and a respiration rate of a person at 15m [1].

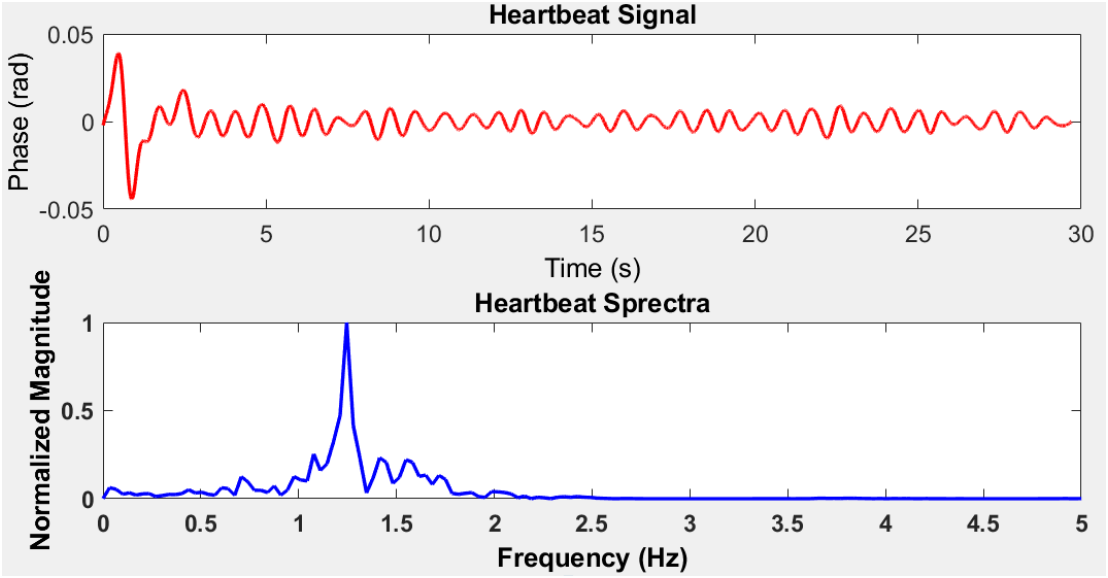


Figure 6.12 Heart beat rate measurement for the person at a distance of 5m.

6.4 Power consumption:

Figure 6.13 and Figure 6.14 shows the breakdown of power consumption and energy consumption by different blocks of the transceiver with output power of 0 dBm respectively. As in most of the cases of transceiver design, PA consumes highest energy to deliver the output power to load. Since LNA must amplify the weak signal with minimum noise addition from the circuits, it burns more power. The total energy consumption is 887 nJ which makes the average power consumption over the pulse repetition time of 1.3 ms to be 680 µW.

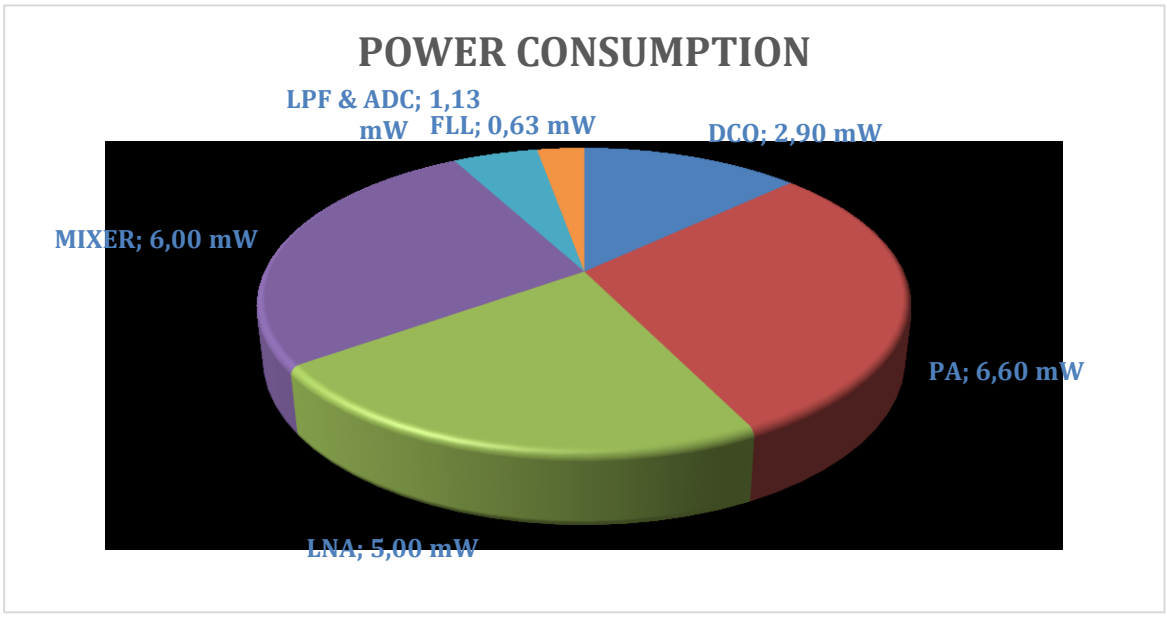


Figure 6.13 Distribution of power consumption for various blocks.

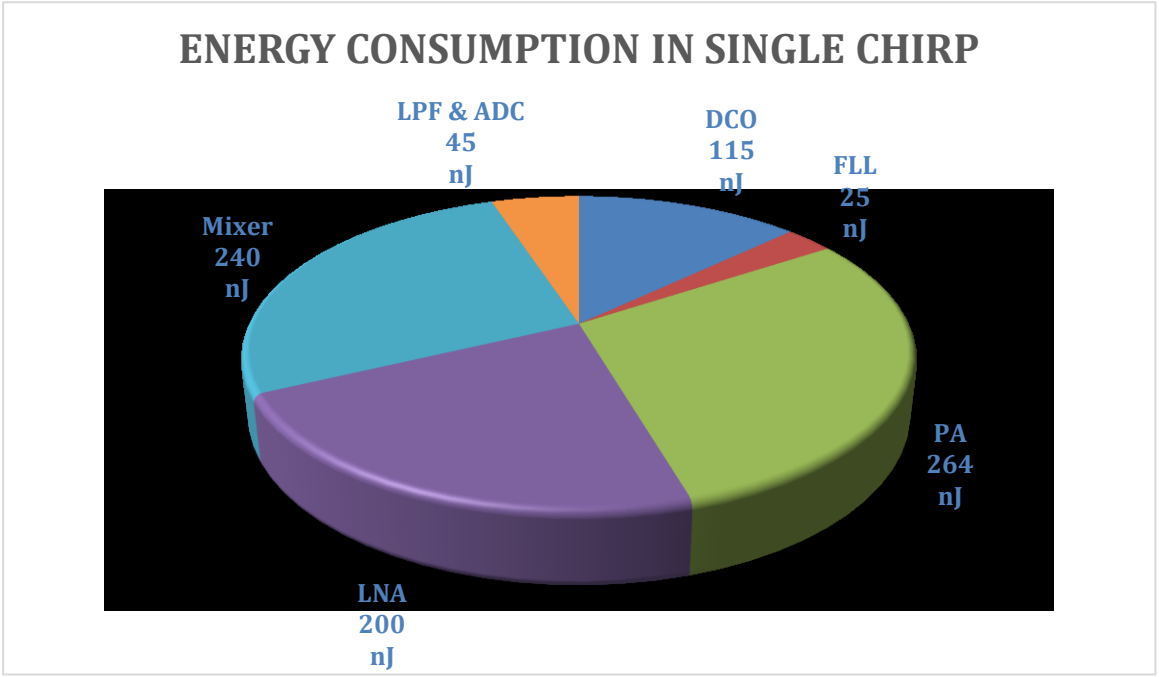


Figure 6.14 Break-down of the energy consumption over chirp period of 40µs

6.5 Comparison with state of art:

The key performance of this radar transceiver is lowest power consumption while achieving the similar or higher performance in terms of 15 meters range where the vital signs can be detected. The table below shows the comparison with previous works in for the similar applications which include indoor and outdoor.

	This work	[4] Anderson, JSSC '17	[5] Chu, ISSCC'11	[23] Lou, ISSCC'18	[17] Wang, TMTT '17	[24] Yeo ISSCC'16
Integration	TX+RX+ADC	TX+RX+ ADC	TX+RX	TX+RX+ ADC	TX+RX+ ADC	PLL only
Technology	40 nm	55 nm	130 nm	65 nm	65 nm	65 nm
Application	Vital sign	Vital sign	Vital sign	SAR Imaging	SAR Imaging	-
Frequency (GHz)	6.8 GHz –8.2 GHz	7.2 – 8.5 GHz	2- 5 GHz	10 GHz	15 GHz	8.4 – 9.4 GHz
TX Signal Type	Pulsed chirp	Impulse	Impulse	FMCW sawtooth	FMCW sawtooth	FMCW Triangular
TX Signal BW	0.75-1 GHz	1.4 GHz	0.9 GHz	1 GHz	1.48 GHz	0.95 GHz
Chirp period/PW	10-40 µs	1.8 ns	3 ns	0.2 – 1ms	1 - 10ms	28 µs
TX power (dBm)	0 dBm	0.7 dBm	N. A	10 dBm	13 dBm	-
TX output power ripple	<1 dB	-	-	<2 dB	<1.1 dB	-
TX RMS freq. error	0.3 – 0.5 MHz	-	-	0.2 – 0.1 MHz	0.16 MHz	1.7 MHz

V_{DD}	1 V	1.8 V	1.9 V	1.2 V	1.2 V	1.1 – 1.3V
Spectral regulations	FCC/ETSI/KCC/ARIB	FCC/ETSI/KCC/ARIB	N. A	Outdoor	Outdoor	-
Band width (GHz)	0.75 GHz	1.4 GHz	0.9 GHz	1 GHz	1.48 GHz	0.95 GHz
RX NF	12 dB (complete RX)	6.3 (RF-FE only)	5 (RF-FE)	6 (RF-FE)	6 (RF-FE)	-
RF – FE P1dB (P1dB)	-35 dBm	-15 dBm	N. A	-37 dBm	-33 dBm	-
RX FFT sidelobe	-12.8 dB	-	-	-12.9 dB	-12.7 dB	-
Peak DC Power consumption	19 mW	118 mW	695 mW	253 mW/ch	260 mW	
Average Power consumption	**0.68 mW**	118 mW	695 mW	141 mW/ch	260 mW	14.8 mW
Die area	**1.8 mm²**	8.6 mm²	11.9 mm²	7.8 mm²	4 mm²	0.18 mm²
Det. Range for heartbeat rate.	**5m**	5m	-	-	-	-
Det. Range for respiration rate.	**15m**	9m	0.75m	-	-	-
Resolution	**20 cm**	10 cm	11.72 cm	30 cm	20 cm	-

Table 6.1 Comparison with previous state of art systems for similar applications.

Chapter 7

Conclusion and Future Scope of the project

7.1 Conclusion

The Radar Transceiver was designed and tested for the vital sign detection with the ability to measure the respiration rate till the range of 15m and heartbeat rate up to 6-m consuming the total average power of 680 µW only.
The presented system proved the concept of vital signs detection based on FMCW chirp-based radar with aggressive duty-cycling for achieving ultra-low power consumption. However, there are also a lot of rooms for further optimization and improvement. Few of the main areas that can be focused further are explained below.

7.2 Future scope of the project

7.2.1 Dynamic offset cancellation

The direct leakage from the transmit antenna to receive antenna is a major constraint on low/zero-IF architectures and full-duplex wireless systems. It's also true for FMCW radar operation in which the base band signal with the beat frequency corresponding to distance between the Tx and Rx antenna is generated and is considerably large in amplitude. So, it is necessary to create a high pass transfer function from the mixer to ADC with sufficient suppression in the stop-band. In the traditional analog method, a such filter implementation needs a large capacitor requiring large chip area.

7.2.2 Tx to Rx Direct leakage mitigation

The direct coupling from TX antenna to RX antenna can be cancelled by adding the signal at various stages of RX to with same amplitude but opposite phase. Recent work [25] shows full duplex hybrid-coupler circulator for full duplex communication systems.

7.2.3 Single antenna system

Realization of a full-duplex wireless system with single antenna poses a greater challenge which is also research opportunity especially when TX and RX frequency bands are close to each other. Mixer first topologies can be explored as well to operate with single antenna [26].

7.2.4 Spatial resolution with multiple Tx-Rx channels

In addition to radial resolution, the multiple Tx-Rx channels can be combined and operate in time-interleaved fashion for efficient use of hardware to realize the spatial resolution.

7.2.5 Electronic Beam forming with multiple TX-RX Channels

Electronic beam forming another wide area of research which be used for precise localization in multi-target scenario.

7.2.6 Advanced signal processing and integration with a real time

In the present system, the digitized data from the ADC is transferred to FPGA followed by offline processing by reading the data from FPGA into a workstation with MATLAB. A real-time display can be developed to display the information about the targets in the multi-target scenario with range, heart beat rate and respiration rate estimates.

7.2.7 Improving the Noise Figure

The Noise figure of overall Receiver can be improved which can further increase the sensitivity of the receiver resulting in the longer range for the radar with the same transmit power.

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Acknowledgement

A considerable number of people have had an influence in the work of this thesis from multiple perspectives. I would like to acknowledge all of them.

I am extremely thankful to my supervisor from the university, Prof. Masoud Babaie, starting from introducing me to Holst center for the thesis project. Regular weekly meetings with intensive technical discussion and his key suggestions helped me along the project to progress in the right direction. His suggestions and comments sparing a lot of his time in reading my thesis helped me to improve my writing and presentation skills substantially.

I extend my thanks to Prof. Leo de Vreede and Prof. Alexander Yarovoy for reading and serving as my thesis committee. The courses I followed from Prof. Leo regarding RFIC design has equipped me with the required concepts to carry out the thesis successfully. The course on electromagnetics from Prof. Alexander had taught a good number of concepts in electromagnetic wave propagation and antennas which were not only for the course but also of worth to be carried out throughout the profession.

I am very much thankful to my supervisors at IMEC, Dr. Yao-Hong Liu and Dr. Marco Mercuri who has guided me closely throughout the execution of the project. I gained immense design experience working under the guidance of Yao-Hong in designing and optimizing at circuit and system level. His emphasis on consideration of all the boundary conditions to design and test the RF circuits resulted in working solution even through it was my first time designing a RF-IC in 40nm CMOS technology. He always had a time for me for any kind of technical discussion when I went to him with queries despite his tight schedule. Marco was very kind and happy to discuss with me about each of system level specifications, system level simulations and finally involvement for the evaluation and measurement of the chip.

I had an opportunity to work with experienced and knowledgeable designers at IMEC. The continuous interaction with the team members not only helped me gain knowledge but also learn design techniques and ways of optimization at schematic and layout level to function at high frequencies. I would like to thank Paul with whom I interacted continuously to discuss about the designs and results that helped me gain the design insights. I would like to thank Johan for providing technical know how to use tools effectively and maintain the databases. He also had key role in top level integration. I would like to thank Arjan and Stefano for digital designs, synthesizing the digital blocks and helping me to set up the AMS environment.

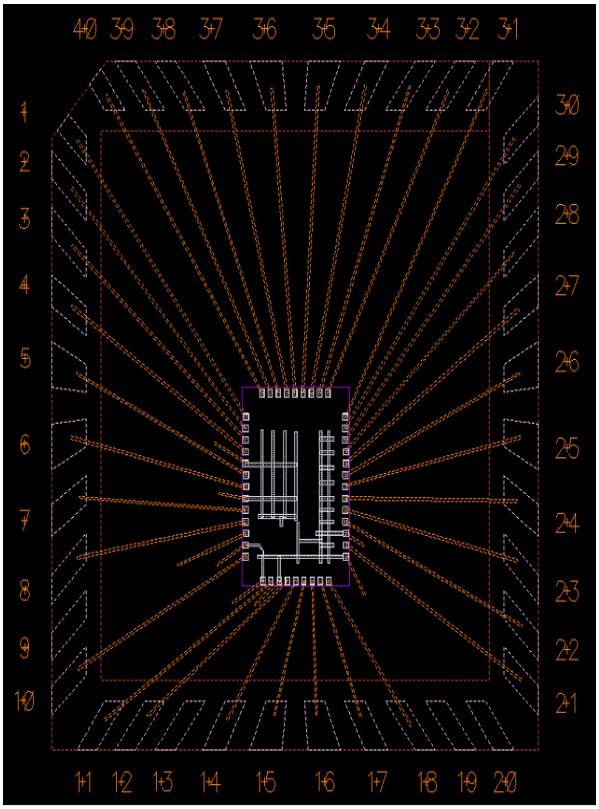
Life during the thesis project could not be of fun without friends, it was great to have a company of Sarthak, Erwin while working at IMEC. I would like to thank both for all the discussion and encouragement during my stay at Holst center.

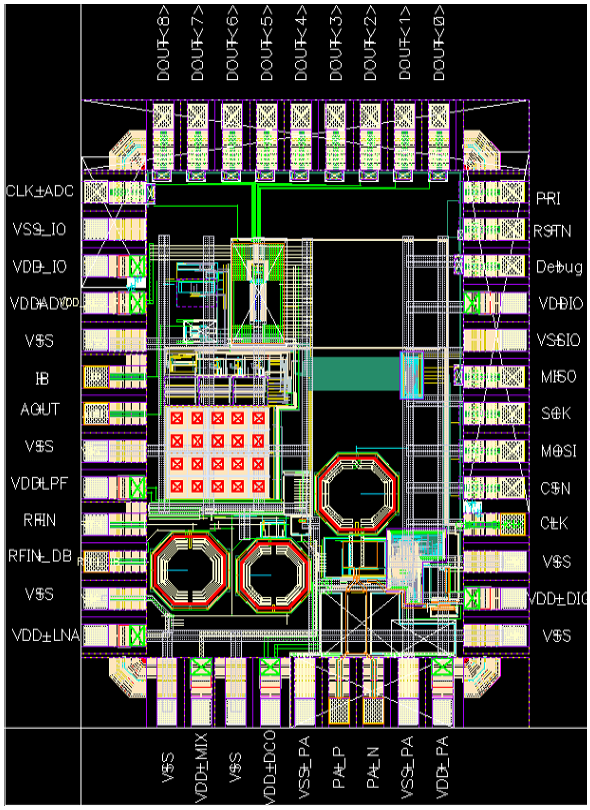
I would like to thank my sister, Ganga and Prof. Leela at my hometown in India for their motivation to keep up with the project execution, writing the thesis and helping me for it.

Finally, my deep and sincere gratitude to my family for their continuous love and encouragement thought out my stay in Netherlands.

Appendix

- **Chip IO Description:**





#PIN-Die	#PIN - Package	PIN NAME	Signal Description	TYPICAL VALUE	MAX VALUE
1	1	CLK_ADC	Clock OUT from ADC	12.5 MHz	
2	2	VSS_IO	VSS for IO signals		
3	3	VDD_IO	VDD for IO signals	1V	1.1V
4	4	VDD_ADC	VDD for ADC	1V	1.1V
5		VSS	Common GND		
6	5	IB	Reference Bias Current IN	5uA	
7	6	AOUT	Base band signal OUT	300 mV-pk @ 140KHz to 1 MHz	
8		VSS	Common GND		

9	7	VDD_LPF	VDD for Base band Circuits	1V	1.1V
10	8	RFIN	RF Input to LNA	5 uV-pk	5mV-pk
11		RFIN_DB	RF Down bond to VSS		
12		VSS	Common GND		
13	10	VDD_LNA	VDD for LNA	1V	1.1V
14		VSS	Common GND		
15	11	VDD_MIX	VDD for Mixer		
16		VSS	VDD for IO signals	1V	1.1V
17	12	VDD_DCO	VDD for DCO	1V	1.1V
18	14	VSS_PA	Common GND		
19	15	PA_P	PA OUTPUT (Differential-POS)	0 dBm (316mV-pk) @ 7.4GHz – 8.15GHz	0 dBm
20	16	PA_N	PA OUTPUT (Differential-NEG)	0 dBm (316mV-pk) @ 7.4GHz – 8.15GHz	0 dBm
21	17	VSS_PA	Separate GND for PA		
22	18	VDD_PA	VDD for PA	1V	1.1V
23		VSS	Common GND		
24	21	VDD_DIG	VDD for Digital blocks	1V	
25		VSS	Common GND		
26	22	CLK	Reference Clock IN	50 MHz	
27	23	CSN	Chip Select for SPI		
28	24	MOSI	Master Out Slave IN for SPI		
29	25	SCK	SPI Clock in		
30	26	MISO	Master In Slave Out for SPI		
31	27	VSSIO	VSS for IO Signals		
32	28	VDDIO	VDD for IO Signals	1V	1.1V
33	29	DEBUG	Debug signal OUT		
34	30	RSTN	Reset IN		

35	31	PRI	Pre-Trigger Signal IN		
36	32	DOUT<0>	ADC DATA OUT (9 BIT)		
37	33	DOUT<1>			
38	34	DOUT<2>			
39	35	DOUT<3>			
40	36	DOUT<4>			
41	37	DOUT<5>			
42	38	DOUT<6>			
43	39	DOUT<7>			
44	40	DOUT<8>			

- **Verilog-HDL code for digital blocks of the FLL**

```
//--------------------------------- Code for FLL-----------------------------------//

    //Phase Detect block to detect the frequency difference between the desired DCO
    //output frequency and instantaneous frequency.

    `timescale 1ps/1fs
    module phase_detect (i_clk, i_rst_n, i_enable, i_fcw_integer, i_phv_i, i_kdcop,
                o_phe_int, i_freeze,i_acc_mem_en ,o_accu_data);

    input                   i_clk;
    input                   i_rst_n;
    //input                   i_rst_an;
    input                   i_enable;
    input [ `FCW_INT_WIDTH-1:0] i_fcw_integer;
    input [ `PHV_INT_WIDTH-1:0] i_phv_i;
    input [4:0]               i_kdcop;

    output [ `PHE_INT_WIDTH:0] o_phe_int;
    input               i_freeze;
    input                  i_acc_mem_en;
    output [ `PHE_INT_WIDTH:0] o_accu_data;
    parameter ENABLED = 1'b1;

    wire       [ `PHV_INT_WIDTH-1:0] w_phv_iso
    reg        [ `PHV_INT_WIDTH-1:0] r_phv_i_dly;
    reg        [ `PHV_INT_WIDTH-1:0] r_phv_i;
    wire       [ `PHV_INT_WIDTH-1:0] w_phv_i;
    wire       [ `FCW_INT_WIDTH:0] w_phe_int_accu;
    wire       [              6:0] w_dphv_i;
    wire                       w_phe_int_accu_rst_n;
    wire signed [ `PHV_INT_WIDTH:0] w_dphe_i;
    wire signed [ `PHV_INT_WIDTH:0] w_dphe_limit;
    wire                       w_clk_n;
    wire       [              1:0] w_phe_int_ov;
    wire                       w_dphe_limit_overflow;
    wire                       w_dphe_limit_underflow;
```

```
wire       [              1:0] w_ov;
wire       [ `FCW_INT_WIDTH-1:0] w_dphr_i;
wire                      w_frac_ov_iso;
wire                      o_ov;
reg                       i_enable_acc;
reg                       i_enable_acc1;
//edited
reg        [ `FCW_INT_WIDTH:0] r_accu_data;



assign w_phv_iso = i_phv_i & {`FCW_INT_WIDTH{i_enable}};
assign w_phv_i = w_phv_iso;

always @ (posedge i_clk or negedge i_rst_n)
begin : p_delay_register
 if (i_rst_n == 1'b0) begin
   r_phv_i_dly <= `PHV_INT_WIDTH'd0;
 end else begin

   i_enable_acc <= i_enable_acc1;
   i_enable_acc1 <= i_enable;
   if (i_enable == 1'b1) begin
   r_phv_i_dly <= w_phv_i;
   end
 end
end

assign w_dphv_i = w_phv_i - r_phv_i_dly;
assign w_dphr_i = $unsigned(i_fcw_integer);

assign w_dphe_i    = (i_enable == 1'b1 ? ($signed({1'b0,w_dphv_i}) - $signed({1'b0,
w_dphr_i})) * $signed({1'b0,i_kdcop}) : `PHV_INT_WIDTH'd0);

signed_limit#(.DI_WIDTH(`FCW_INT_WIDTH+1),
.DO_WIDTH(`FCW_INT_WIDTH+1)) u_phe_int_limit (
                .i_di       (w_dphe_i),
                .o_do       (w_dphe_limit),  // output to accumulator
                .o_overflow  (w_dphe_limit_overflow),
                .o_underflow (w_dphe_limit_underflow)
               );
signed_accu #(.DATA_WIDTH(`FCW_INT_WIDTH+1)) u_phe_int_accu (
               .i_clk    (i_clk),
               .i_rst_n  (w_phe_int_accu_rst_n),
               .i_enable (i_enable_acc),
                                .i_freeze (i_freeze),
               .i_di     (w_dphe_limit),
               .i_acc_mem_en(i_acc_mem_en),
               .o_do     (w_phe_int_accu),
               .o_ov     (w_phe_int_ov)
              );
```

```
        assign w_ov = w_phe_int_ov | {w_dphe_limit_overflow, w_dphe_limit_underflow};
        assign o_phe_int = w_phe_int_accu;
        assign o_ov      = (i_enable == 1'b1 ? w_ov          : 2'boo          );
        assign w_phe_int_accu_rst_n = i_rst_n;
        wire ld;
        reg  freeze_del;
        assign ld = i_freeze & ~freeze_del;


        always @(posedge i_clk or negedge i_rst_n) begin : p_freezeevent
          if (i_rst_n == 1'bo) begin
            freeze_del  <= 1'bo;
            r_accu_data <= `FCW_INT_WIDTH+1'do;
          end else begin
            freeze_del  <= i_freeze;
            if (ld) begin
              r_accu_data <= w_phe_int_accu;
            end
          end
        end
        assign o_accu_data =  r_accu_data;

        endmodule

//Normalization block
`timescale 1ps/1fs
module norm_acq (i_clk, i_rst_an, i_rst_n, i_kdco, i_phe, i_bank_en, i_en_sdm, i_bank_val,
            o_dco_acq, dco_row, dco_col);// o_overflow);
`include "adpll_dig_parameters.v"

parameter W_KDCO    = 5;
parameter W_PHE     = 8;

input                   i_clk;
input                   i_rst_an;
input                   i_rst_n;
input  [       W_KDCO-1:0] i_kdco;
input  [        W_PHE-1:0] i_phe;
input                   i_bank_en;
input                   i_en_sdm;
input  [`DCO_ACQ_WIDTH-1:0] i_bank_val;
output [`DCO_ACQ_WIDTH-1:0] o_dco_acq;
output [15:0] dco_row;
output [15:0] dco_col;
wire   [`DCO_ACQ_WIDTH-1:0] w_dco_acq_gain;
wire   [`DCO_ACQ_WIDTH-1:0] w_dco_acq_ctrl;
wire   [        W_PHE-1:0] w_phe_iso;
wire [             1:0] o_overflow;   // lock detection bit
assign w_phe_iso = i_phe & {W_PHE{i_bank_en}};
gain_dco #(
```

```
        .GAIN_WIDTH     (W_KDCO),
        .DATA_WIDTH     (W_PHE),
        .TRUNK_MSB      (W_PHE-`DCO_ACQ_WIDTH),
        .TRUNCATE_WIDTH (8)
       ) u_gain_acq (
        .i_clk      (i_clk),
        .i_rst_an   (i_rst_an),
        .i_gain     (i_kdco),
        .i_data     (w_phe_iso),
        .i_en_sdm   (i_en_sdm),
        .o_result   (w_dco_acq_gain),
        .o_overflow (o_overflow)
       );
ctrl_dco #(
        .W_DCO       (`DCO_ACQ_WIDTH)
       ) u_ctrl_acq (
        .i_clk       (i_clk),
        .i_rst_an    (i_rst_an),
        .i_rst_n     (i_rst_n),
        .i_bank_en   (i_bank_en),
        .i_bank_val  (i_bank_val),
        .i_bank_sel  (i_bank_sel),
        .i_dco       (w_dco_acq_gain),
        .o_dco       (w_dco_acq_ctrl)
       );
assign o_dco_acq = w_dco_acq_ctrl;
dec4_to_therm16 row_dec(.i_dec(w_dco_acq_ctrl[7:4]),.o_therm(dco_row));
dec4_to_therm16z col_dec(.i_dec(w_dco_acq_ctrl[3:0]),.o_therm(dco_col));
endmodule
```