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18.3 An Auto-Zero Stabilized Voltage Buffer with a Quiet Chopping Scheme and Constant Input Current

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The readout of high-impedance sensors and sampled voltage references [1] requires amplifiers that can achieve both low offset and low input current. Recently, it has been shown that this unique combination can be achieved by an auto-zero (AZ) stabilized buffer [2]. However, its low-frequency noise density is $\sqrt{5}$ times higher than the buffer's own white-noise voltage spectral density e_n. Furthermore, its input current is not constant, but varies significantly with the input voltage. To overcome the first issue, a chopped AZ stabilization loop with an optimized duty-cycle is proposed to bring the low-frequency noise density close to $\sqrt{2}\cdot e_n$, the fundamental limit of an AZ stabilized amplifier. The second issue is solved by replacing the transmission-gate input switches used in [2] with NMOS switches and a constant Vgs drive. This keeps their charge injection constant over a wide input voltage range, and results in a constant input current.

As shown in Fig. 18.3.1, the AZ stabilized buffer consists of a buffer (BUF), whose offset (V_{os1}) and 1/*f* noise are periodically cancelled by a first AZ stabilization loop, which consists of an OTA (AZ1), an integrator (INT and $C_{int11\text{-}int12}$, 10pF each) and an OTA (AZ3) [2]. AZ1 is itself auto-zeroed by a second AZ loop that consists of another integrator (INT and $C_{int21\text{-}int22}$, 10pF each) and another OTA (AZ2). To prevent noise folding, the correction range of both AZ loops is quite small (~500μV). So a digitally-assisted AZ loop [2] is used to trim the mV offsets of AZ1 and BUF at startup (Fig. 18.3.2).

The minimum low-frequency noise density of the AZ stabilized buffer is $\sqrt{5}\cdot e_n$ [2], where e_n is the white-noise voltage spectral density of AZ1 and BUF (Fig. 18.3.1). This can be intuitively understood as follows. During phase ϕ_1 the first AZ loop cancels the low-frequency noise of BUF, while AZ1 contributes noise both directly and via the previously stored noise at nodes EF, leading to a total contribution of $\sqrt{2}\cdot e_n$. During phase ϕ_2 the noise of BUF, AZ1 *and* the noise of AZ1 held on nodes EF is stored on nodes GH, leading to a total contribution of $2\cdot e_n$. Assuming a 50% AZ duty cycle, the noise over the two phases would be $\sqrt{3}\cdot e_n$. However, the correlation of the sampled AZ1 noise at nodes EF in both phases leads to a low-frequency noise of $\sqrt{5}\cdot e_n$.

In order to remove this correlation, the AZ stabilization loop is chopped (Fig. 18.3.1). Choppers around AZ1 periodically invert the polarity of the noise held at nodes EF on its way to nodes GH. Over one chopping period, this should cancel its noise contribution, reducing the low-frequency noise floor to $\sqrt{3}\cdot e_n$. Since the second AZ loop is still active, however, the noise held at nodes EF will slowly change during chopping and so will not be perfectly cancelled. The amount of change depends on the duration of the chopping period, and hence on the AZ frequency f_{AZ}. Setting f_{AZ} = 15kHz, which is enough to cancel the 1/*f* noise of the buffer, only reduces the low-frequency noise floor slightly (Fig. 18.3.1). To approach the $\sqrt{3}\cdot e_n$ limit, simulations show that f_{AZ} would have to be some 3× higher, resulting in significantly more input switching, and hence, more input current.

To preserve the noise on nodes EF during a chopping period, extra integration capacitors $C_{int31\text{-}int32}$ (1pF each) are used to implement a modified ϕ_2 phase, denoted by ϕ_3 (Fig. 18.3.1). During ϕ_3, nodes EF are not connected to the output of INT. Also, resistors $R_{1\text{-}2}$ (2MΩ) limit the gain of INT, preventing it from clipping due to the residual output current of AZ1 (Fig. 18.3.1). The noise at nodes EF can then be perfectly chopped without changing f_{AZ}. The chopping transitions are arranged to occur in phase ϕ_2, when the input chopper is disconnected from the input by the AZ switches. With these two measures, the AZ stabilization loop can be chopped without introducing extra spikes or input current.

Another challenge is the offset of the integrator, which, via the chopper at its input, appears as a square-wave ripple voltage at the output of AZ1. This will be translated into a ripple voltage at the input of the buffer via the transconductance and finite output impedance of AZ1. With an expected integrator offset of about 2mV, the output impedance of AZ1 should be quite high (>150MΩ) to ensure that the resulting ripple is negligible (<100nV). This requirement is met by implementing AZ1 as a folded-cascode OTA.

The buffer noise level can be further reduced by adjusting the ϕ_1: ϕ_2 duty-cycle, noting that the noise in phase ϕ_1 ($\sqrt{2}\cdot e_n$) is less than the noise in phase ϕ_2 ($2\cdot e_n$). So the more time the buffer spends in phase ϕ_1, the closer its noise gets to $\sqrt{2}\cdot e_n$. Since some settling time is required for ϕ_2, the resulting noise level will then be somewhere between $\sqrt{3}\cdot e_n$ and $\sqrt{2}\cdot e_n$.

In [2], the input switches are implemented as transmission gates. Depending on the input voltage, this means that either the NMOS, PMOS or both devices will be turned "off" by clock transitions. Their charge injection, and thus, the input current will then be dependent on the input voltage (Fig. 18.3.3), typically changing by about 0.9pA over the input voltage range of the buffer (0 to 1.3V). In this design, the input switches are implemented as NMOS switches. Half-sized dummy transistors are used to partially cancel their charge injection. The NMOS switches are driven at constant Vgs by a circuit consisting of two latching transistors (MN1,2) and two boosting capacitors (CB1,2), which ensure that the clock waveform is superimposed on the input voltage. A simple buffer drives the capacitors, ensuring that their charging current does not load the input of the main buffer. Measurements show that the resulting input current is quite constant, varying by less than 0.2pA with input voltage (Fig. 18.3.3). As in [2], the input current is measured by observing the discharge of the hold capacitor C_H (= 36pF) of an on-chip low-leakage S&H circuit.

The buffer was realized in a 0.18μm CMOS process (Fig. 18.3.7). It draws 210μA from a 1.8V supply, and has an active area of 0.55mm², 0.12mm² of which is occupied by the S&H circuit. With a 1V input and f_{AZ} = 15kHz, measurements show that its input current is below 0.8pA (15 samples), and that its offset does not exceed 0.4μV (Fig. 18.3.4). In Fig. 18.3.5, the voltage noise density of the buffer is shown. With auto-zeroing alone, a low-frequency noise density of 31nV/√Hz is achieved, which equals the √5× noise limit. When chopped with the extra ϕ_3 phase enabled, the low-frequency noise drops to 25nV/√Hz, which equals the √3× noise limit. Finally when a 75% duty-cycle is used, a low-frequency noise of 20nV/√Hz is achieved, which is very close to the √2× noise limit. This reduction from √5× to √2× noise corresponds to a 2.5× power saving in the input stages. No tones at f_{AZ} or f_{CH} can be seen, demonstrating that the use of chopping does not add spikes, while the 75% duty-cycle does not change the offset or input current.

In Fig. 18.3.5, the input current vs input voltage of a typical sample is shown. With and without chopping, no significant difference in input current can be seen. The voltage drift across C_H is also shown (typical sample, 1V input). With AZ off, no drift can be seen, illustrating that the leakage of the S&H is indeed negligible. Furthermore, a measurement of the input current vs f_{AZ} shows a linear relationship, which indicates that charge injection is the dominant source of input current. In Fig. 18.3.6 the performance of the auto-zeroed voltage buffer is summarized and compared with the state-of-the-art. A special chopping scheme allows it to achieve a low-frequency voltage noise of 20nV/√Hz, while also achieving a constant and low input current (0.8pA), as well as state-of-the-art offset (0.4μV).

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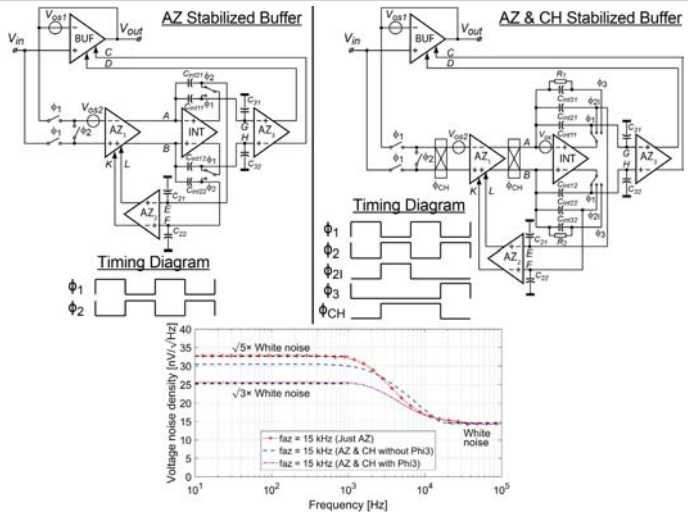

Figure 18.3.1: An auto-zero stabilized buffer without and with a chopped stabilization loop and additional Φ3 phase. Voltage noise density simulation for different configurations (AZ, AZ&CH without and with Φ3).

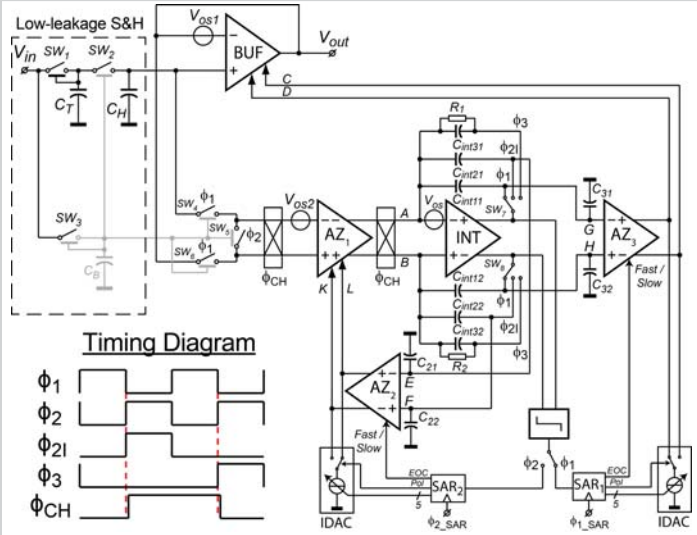

Figure 18.3.2: Block diagram of the auto-zero stabilized voltage buffer with chopped stabilization loop and digital assistance.

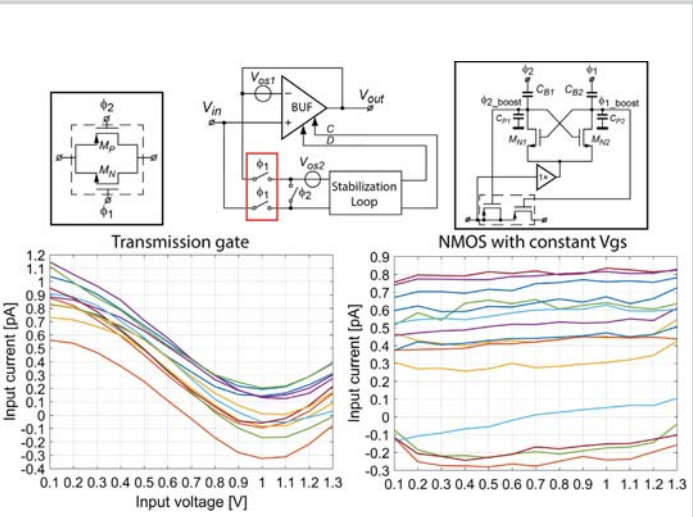

Figure 18.3.3: Measured input current vs input voltage for different type of input switches: transmission gates (Left) and NMOS with constant Vgs drive (Right).

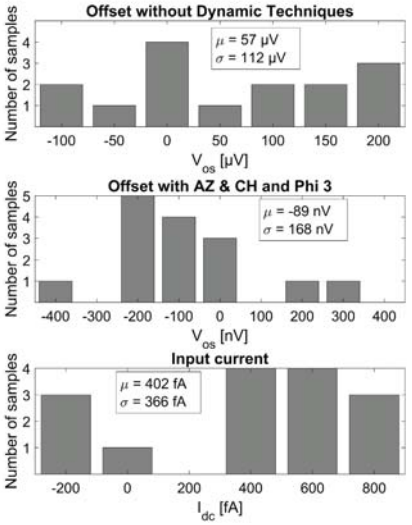

Figure 18.3.4: Histograms (15 samples) of the measured offset (without and with AZ) and input current with AZ&CH and Φ3 (fAZ = 15 kHz, Vin = 1V).

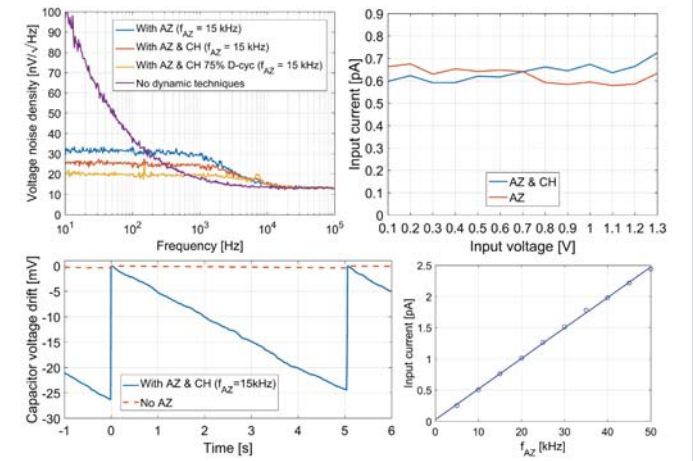

Figure 18.3.5: Measured voltage noise PSD: No AZ, with AZ and with AZ & CH (Top left). The input current vs the input voltage for a typical sample for AZ and AZ&CH (Top right). The capacitor voltage drift of a typical sample with and without AZ & CH (Bottom Left). The input current vs AZ frequency with chopped stabilization loop (Bottom Right).

	This work	[2]	[3]	[4]	[5]	[6]	[7]
Dynamic technique(s)	**Auto-zeroing and Chopped Stabilization**	Auto-zeroing	Chopping	Chopping and Auto-zeroing	Chopping and Auto-zeroing	Auto-zeroing	Chopping and Auto-zeroing
Input current (Max)	**0.8 pA**	1.2 pA*	72 pA	40 pA	-	50 pA	-
Offset (Max)	**0.4 μV**	0.6 μV	0.78 μV	3 μV	2.8 μV	5 μV	4 μV
Voltage noise (nV/√Hz)	**31 (AZ) 25 (AZ&CH) 20 (75% AZ&CH)**	29	5.9	20	38 (AZ) 27 (CH&AZ)	75	140 (AZ) 28 (CH&AZ)
NEF	**7.3**	7.4	8.7**	21.8**	43.5**	-	-
GBW (MHz)	**1.45**	1.45	4	2.5	0.8	1	-
PSRR (dB)	**125**	125	142	-	138	130	128
Frequency (kHz)	**15 (f_{AZ}) / 7.5 (f_{CH})**	15	200	15 (f_{CH}) / 7.5 (f_{AZ})	28 (f_{AZ}) / 14 (f_{CH})	4	11 (f_{CH}) / 7.33 (f_{AZ})
Supply current	**210 μA**	210 μA	1.47 mA	800 μA	1.7 mA	750 μA	480 μA
Supply voltage	**1.8 V**	1.8V	2.5 - 5.5 V	5 V	2.7 - 5.5 V	2.7 V	3.3 - 5.5 V
Technology	**0.18 μm**	0.18 μm	0.35 μm	0.6 μm	0.5 μm	-	0.5 μm
Die area (including pads)	**1.4 mm²**	1.4 mm²	1.26 mm²	0.67 mm²	2.5 mm²	-	1.48 mm²

* Input current over the full input voltage range (0 to 1.3V) ** Estimated value [8]

Figure 18.3.6: Performance summary and comparison with previous works.

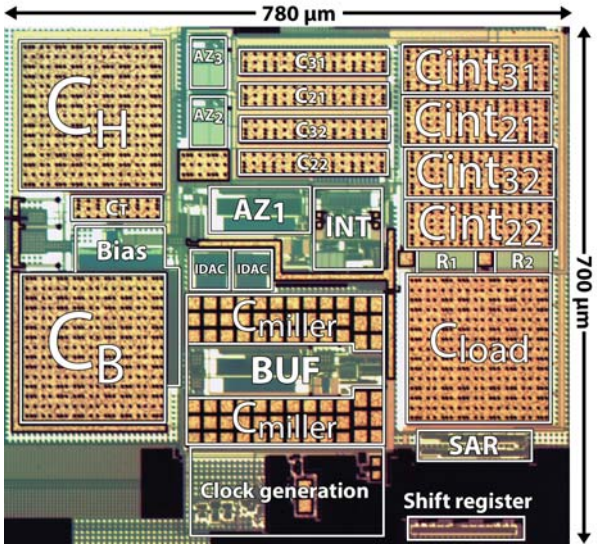

Figure 18.3.7: Die micrograph of the active area.

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