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Nanoparticles sintering technology for power electronics modules and beyond

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NANOPARTICLES SINTERING TECHNOLOGY FOR POWER ELECTRONICS MODULES AND BEYOND

NANOPARTICLES SINTERING TECHNOLOGY FOR POWER ELECTRONICS MODULES AND BEYOND

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
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chair of the Board for Doctorates
to be defended publicly on
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Keywords: Nanoparticles sintering, power electronics packaging, hermetic packaging, molecular dynamics simulation, thermo-mechanical performance, microelectronics reliability

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Summary

In advancing the 'More than Moore' paradigm, heterogeneous integration has emerged to create highly efficient, compact, and multifunctional semiconductor systems. Addressing challenges related to power efficiency, superior performance, and integration density, metallic nanoparticle (NP) sintering technology has become pivotal for integrating diverse materials and components in advanced semiconductor packaging. Traditional electronic packaging materials face limitations and process complexity, making nanoparticles sintering an attractive option. With its benefits of low processing temperatures (< 0.4 T_m), exceptional electro-thermo-mechanical performance, and high process flexibility, this technology is gaining increased attention, particularly in high-power electronics packaging applications.

Over the past decade, silver (Ag) sintering technology has shown promise in the power electronics industry, serving as an effective solution for high-power die-attach. However, due to the high cost of materials, efforts have been directed towards reducing pressure and exploring alternative sintering materials to reduce overall process costs. Recently, the concept of 'all copper (Cu) interconnect' has extended from low-power to high-power applications, with low-temperature Cu nanoparticle sintering showing substantial potential as a replacement for Ag in pressure-assisted sintering. Despite this promising avenue, the understanding of sintered Cu materials remains limited, primarily due to susceptibility to oxidation issues. Comprehensive studies comparing both sintering materials, extending beyond mere shear tests, are insufficient, leaving a significant gap in our understanding. Furthermore, methodologies for characterizing the sintered structure and providing detailed insights into its thermo-mechanical behavior are notably absent.

In this dissertation, molecular dynamics (MD) simulation was employed to study the coalescence kinetics and the mechanical and chemical performance of coalesced nanoparticles. A two-hemispherical nanoparticle model was built to simulate the impact of sintering temperature and pressure on low-temperature pressure-assisted coalescence. The sintering dynamics and microstructure evolution were analyzed, including neck growth, shrinkage variation, grain boundary development, and dislocation activities. Additionally, uniaxial tensile tests with a constant strain rate were employed to investigate the tensile performance of pressure-assisted sintered nanoparticles. Subsequently, another mechanical nanoindentation simulation was conducted on a multi-nanoparticle sintered structure, investigating the impact of indentation position and indenter size on the nanoindentation response. At the end of the first chapter, the chemical corrosion of sulphidation on multi-Ag nanoparticles' sintered structure was simulated using the reactive-force-field (ReaxFF) MD method. The sulphidation on dense Ag and porous sintered structures was compared and analyzed, revealing the sulphidation mechanism at an atomic level.

In the next chapter, the microscopic and macroscopic mechanical performance of sintered Cu was discussed through bending and high-temperature tensile tests. For microscopic mechanical performance, 4 μm-wide micro-cantilevers with different notch depths were microfabricated in a Cu nanoparticle sintered interconnect. Continuous dynamical testing on the micro-cantilevers revealed elastic-plastic fracture behavior in the porous sintered structure. The microscopic fracture toughness of different notched specimens was obtained using the J-integral according to elastic-plastic fracture mechanics. For macroscopic mechanical performance, high-temperature tensile tests were performed on dog-bone-shaped Cu nanoparticles sintered specimens at temperatures ranging from 180 °C to 360 °C with strain rates up to $1 \times 10^{-3}\ s^{-1}$. The elastic modulus and tensile strength were measured under different testing conditions. Failure analysis of the fracture surface revealed that recrystallization was the main factor for improved ductility. Additionally, a viscoplastic constitutive Anand model was parameterized based on the tensile results, achieving a great fit.

In addition to mechanical performance, offline and online thermal monitoring of the sintered nanoparticles were conducted in the following chapter. The offline transient thermal measurement was performed by attaching a silicon (Si) thermal test chip to a Cu substrate. According to the transient dual-interface method standard, the low junction-to-case thermal resistance of Ag and Cu nanoparticle sintered die-attach was successfully distinguished from the separation of thermal impedance curves and structure functions. Based on the offline transient thermal measurement, online thermal performance monitoring over 500 cycles of thermal cycling test (-55 °C to 150 °C) was characterized by fast heat pulse-enabled in-situ transient thermal measurements. The thermal degradation of Ag and Cu nanoparticles sintered quad-flat no-leads (QFN) discrete Si MOSFET devices was evaluated by thermal impedance over the first 0.1 seconds of the heat pulse. The thermal performance degradation showed remarkable consistency with the observed adhesion results. Ag sintered products demonstrated excellent robustness with a 2.5% to 3.8% thermal impedance increase over 500 cycles, while significant thermal degradation was recorded in the Cu nanoparticles sintered QFN.

Next, with the known excellent thermo-mechanical performance of the sintered joint, two prototypes of metallic nanoparticle sintering technology in heterogeneous integration applications were manufactured. First, 1200V/50A Si insulated-gate bipolar transistors (IGBTs) were packaged as discrete transistor outline (TO)247 with Ag and Cu nanoparticle sintered die-attach layers. On the top side of the power device, Al wire bonding and ribbon bonding were investigated to improve reliability. Passive thermal cycling tests were conducted with Δ T = 200 K for 500 cycles. The junction-to-case thermal resistance and IV characteristics showed relatively minor differences between the different sintered devices. To conduct more extreme aging tests, thermal shock tests with Δ T = 200 K for 1000 cycles were conducted to accelerate aging. Minor degradation was observed in adhesion, thermal, and electrical performance. Additionally, Finite Element Method (FEM) simulation was applied to calculate the Von-Mises stress distribution, verifying the experimental observations on delamination.

Furthermore, nanoparticles sintering technology was extended to a microelectromechanical systems (MEMS) hermetic package to form a vacuum in the sealed cavity. A Cu nanoparticle sintering-enabled hermetic sealing solution with a small-sized sealing ring

was developed. The technology simplifies microfabrication and requires less surface roughness using a sinterable Cu nanoparticle paste. Using a lithography-patterned photoresist as a stencil mask, a 50 μm size Cu paste sealing ring was achieved. A groove-structured chip was used to amplify localized stress. The Cu nanoparticle paste was fully sintered at 300 $^{\circ}C$ under pressure ranging from 10 MPa to 40 MPa. This resulted in robust bonding with a maximum shear strength of 280 MPa and the implementation of hermetic packaging. The deflection of the Si diaphragms estimated a vacuum level of 7 kPa. Vacuum sealing was maintained for over six months, with the lowest leak rate calculated as 8.4×10^{-13} Pa·m^3/s.

At the end of this dissertation, the main conclusions are summarized, and a few recommendations for future work are suggested.

SAMENVATTING

IN de vooruitgang van het ’Meer dan Moore’ paradigma is heterogene integratie ontstaan om zeer efficiënte, compacte en multifunctionele halfgeleidersystemen te creeren. Door de uitdagingen aan te pakken met betrekking tot energie-efficiëntie, superieure prestaties en integratiedichtheid, is metallic nanodeeltjes (NP) sintering technologie cruciaal geworden voor de integratie van diverse materialen en componenten in geavanceerde halfgeleiderverpakkingen. Traditionele elektronische verpakkingsmaterialen hebben beperkingen en procescomplexiteit, waardoor nanodeeltjes sinteren een aantrekkelijke optie wordt. Met voordelen zoals lage verwerkingstemperaturen (< 0,4 T_m), uitzonderlijke elektro-thermo-mechanische prestaties en hoge procesflexibiliteit, krijgt deze technologie steeds meer aandacht, vooral in toepassingen voor verpakkingen van hoogvermogen elektronica.

De afgelopen tien jaar heeft zilver (Ag) sintering technologie veelbelovend gebleken in de vermogenselektronica-industrie, als een effectieve oplossing voor hoogvermogen dieattach. Echter, vanwege de hoge materiaalkosten, zijn er inspanningen geleverd om de druk te verminderen en alternatieve sintermaterialen te verkennen om de totale proceskosten te verlagen. Onlangs heeft het concept van ’alles koper (Cu) interconnectie’ zich uitgebreid van laagvermogen naar hoogvermogen toepassingen, waarbij lage-temperatuur Cu nanodeeltjes sinteren aanzienlijk potentieel toont als vervanging voor Ag in drukgeassisteerde sintering. Ondanks deze veelbelovende richting blijft het begrip van gesinterde Cu-materialen beperkt, voornamelijk vanwege de gevoeligheid voor oxidatieproblemen. Uitgebreide studies die beide sintermaterialen vergelijken, die verder gaan dan alleen afschuiftests, zijn onvoldoende, waardoor een aanzienlijk kennisgat ontstaat. Bovendien ontbreken methodologieën voor het karakteriseren van de gesinterde structuur en het bieden van gedetailleerd inzicht in het thermo-mechanische gedrag.

In dit proefschrift werden moleculaire dynamica (MD) simulaties gebruikt om de coalescentiekinetiek en de mechanische en chemische prestaties van gesinterde nanodeeltjes te bestuderen. Een twee-hemisferisch nanodeeltjesmodel werd gebouwd om de impact van sintertemperatuur en druk op lage-temperatuur drukgeassisteerde coalescentie te simuleren. De sinterdynamiek en microstructuur evolutie werden geanalyseerd, inclusief nekvorming, krimpvariatie, korrelgrensontwikkeling en dislocatieactiviteiten. Bovendien werden, op basis van drukgeassisteerde gesinterde nanodeeltjes, uniaxiale trekproeven met een constante rekingssnelheid gebruikt om de trekprestaties te onderzoeken. Vervolgens werd een andere mechanische nano-indringing simulatie uitgevoerd in een multi-nanodeeltjes gesinterde structuur, waarbij de impact van de indringingspositie en de indringermaten op de nano-indringingsrespons werd onderzocht. Aan het einde van het eerste hoofdstuk werd de chemische corrosie van sulfidatie op multi-Ag nanodeeltjes gesinterde structuur gesimuleerd met de reactive-force-field (ReaxFF) MD methode. De sulfidatie op de dichte Ag en poreuze gesinterde structuren werd verge-

leken en geanalyseerd, waarbij het sulfidatiemechanisme op atomair niveau werd onthuld.

In het volgende hoofdstuk werd de microscopische en macroscopische mechanische prestatie van gesinterd Cu besproken door het uitvoeren van buig- en hoge-temperatuur trekproeven. Voor microscopische mechanische prestaties werden 4 μm brede micro-cantilevers met verschillende inkepingsdiepten gemicrofabriceerd in een Cu nanodeeltjes gesinterde interconnectie. Continue dynamische tests op de micro-cantilevers onthulden elastisch-plastisch breken in de poreuze gesinterde structuur. De microscopische breuktaaiheid van verschillende ingekeepte exemplaren werd verkregen uit de J-integral volgens elastisch-plastische breukmechanica. Voor macroscopische mechanische prestaties werden hoge-temperatuur trekproeven uitgevoerd op hondbeen-vormige Cu nanodeeltjes gesinterde exemplaren bij temperaturen variërend van 180 °C tot 360 °C met verschillende rekingssnelheden tot $1 \times 10^{-3}\ s^{-1}$. De elastische modulus en treksterkte werden verkregen onder verschillende testomstandigheden. Faalanalyse werd uitgevoerd op het breukoppervlak om te onthullen dat recrystallisatie de belangrijkste factor was voor ductiliteit verbetering. Bovendien werd een viscoplastisch constitutief Anand model geparameteriseerd op basis van de trekresultaten, en een uitstekende fit werd bereikt.

Naast de mechanische prestaties, werden offline en online thermische monitoring van de gesinterde nanodeeltjes uitgevoerd in het volgende hoofdstuk. De offline transiënte thermische meting werd uitgevoerd door een silicium (Si) thermisch testchip op een Cu substraat te bevestigen. Volgens de transiënte dual-interface methode standaard werd de lage junction-to-case thermische weerstand van Ag en Cu nanodeeltjes gesinterde die-attach succesvol onderscheiden van de scheiding van thermische impedantie curves en structuurfuncties. Gebaseerd op de offline transiënte thermische meting werd online thermische prestatie monitoring over 500 cycli van thermische cyclustests (-55 °C tot 150 °C) gekarakteriseerd door snelle warmte-puls ingeschakelde in-situ transiënte thermische metingen. De thermische degradatie van Ag en Cu nanodeeltjes gesinterde quad-flat no-leads (QFN) discrete Si MOSFET apparaten werd geëvalueerd door de thermische impedantie gedurende de eerste 0,1 seconden van de warmte-puls. De thermische prestatiedegradatie toonde opmerkelijke consistentie met de waargenomen hechtingsresultaten. Ag gesinterde producten vertoonden uitstekende robuustheid met een 2,5% tot 3,8% toename in thermische impedantie over 500 cycli, terwijl significante thermische degradatie werd geregistreerd in de Cu nanodeeltjes gesinterde QFN.

Vervolgens, met de bekende uitstekende thermo-mechanische prestaties van de gesinterde verbinding, werden twee prototypes van metallic nanodeeltjes sintertechnologie in heterogene integratietoepassingen vervaardigd. Ten eerste werden 1200V/50A Si geïsoleerde-gate bipolaire transistors (IGBT's) verpakt als discrete transistor outline (TO)247 met Ag en Cu nanodeeltjes gesinterde die-attach lagen. Aan de bovenzijde van het vermogensapparaat werden Al draad bonding en lint bonding onderzocht om de betrouwbaarheid te verbeteren. Passieve thermische cyclustests werden uitgevoerd met $\Delta T = 200K$ voor 500 cycli. De junction-to-case thermische weerstand en IV karakteristieken toonden relatief kleine verschillen tussen de verschillende gesinterde apparaten. Om meer extreme verouderingstests uit te voeren, werden thermische schoktests met $\Delta T = 200K$ voor 1000 cycli uitgevoerd om de veroudering te versnellen. Kleine degra-

datie werd waargenomen in hechting, thermische en elektrische prestaties. Daarnaast werd de Eindige Elementen Methode (FEM) simulatie toegepast om de Von-Mises spanningsverdeling te berekenen, wat de experimentele observaties op delaminatie bevestigt.

Verder werd nanodeeltjes sintering technologie uitgebreid naar een microelectromechanical systems (MEMS) hermetische verpakking om een vacuüm in de gesloten holte te vormen. Een Cu nanodeeltjes sintering-ingeschakelde hermetische afdichtingsoplossing met een klein-formaat afdichtingsring werd ontwikkeld. De technologie vereenvoudigt microfabricage en vereist minder oppervlakteruwheid met een sinterbare Cu nanodeeltjes pasta. Met behulp van een lithografie-gepatroneerde fotoresist als een sjabloonmasker werd een 50 μm grootte Cu pasta afdichtingsring bereikt. Een groefgestructureerde chip werd gebruikt om de gelokaliseerde spanning te versterken. De Cu nanodeeltjes pasta werd volledig gesinterd bij 300 $^{\circ}C$ onder druk variërend van 10 MPa tot 40 MPa. Dit resulteerde in robuuste binding met een maximale afschuifsterkte van 280 MPa en de implementatie van hermetische verpakking. De doorbuiging van de Si membranen schatte een vacuümniveau van 7 kPa. Vacuümverzegeling werd meer dan zes maanden gehandhaafd, en de laagste lekwaarde werd berekend als 8,4 × 10^{-13} Pa·m^3/s.

Aan het einde van dit proefschrift worden de belangrijkste conclusies samengevat en enkele aanbevelingen voor toekomstig werk voorgesteld.

1

INTRODUCTION

Sintering technology has been accompanying human development for thousands of years. In this era of rapid electrification and digitalization, the ancient sintering technique is experiencing a rejuvenation in novel domains. The background of this dissertation, various sintering technologies, and their significant contributions to the field of heterogeneous integration will be introduced.

1

1.1. BACKGROUND

RAPID development of microelectronics has been achieved over several decades, leading to a more efficient and intelligent society. In the' More than Moore' (MtM) concept, as shown in Fig. 1.1, the non-digital contents and heterogeneous integration are reaching incredible development to change how humans live [1]. In the MtM era, innovation is driven by integrating various technologies on a single chip or package to enable new features and functionalities. This approach combines different materials, devices, and processes to address specific challenges, such as power efficiency, sensor integration, and diverse functionalities beyond conventional scaling limits [2–4].

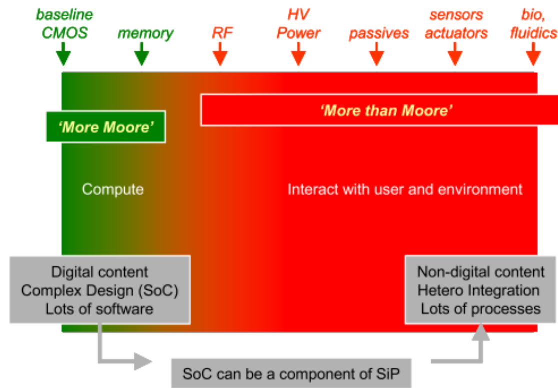

Figure 1.1.: Intelligent systems requiring both computing and interacting functionalities.

MtM emphasizes the integration of diverse technologies to address specific challenges and enable new functionalities, significantly contributed by the domain of heterogeneous integration (HI). The heterogeneous integration roadmap (HIR), proposed by IEEE EPS, provides a roadmap for achieving this integration goal, guiding the industry in terms of technologies, methodologies, and standards to be adopted [5]. The HIR works alongside the MtM concept to explore and implement innovative semiconductor design and manufacturing approaches, steering the semiconductor industry towards a more holistic and diversified approach to innovation.

The diversified technological landscape in HIR, as shown in Fig. 1.2, allows for the developing of highly efficient, compact, and multi-functional semiconductor systems [6]. Including various technologies in HIR fosters innovation across multiple domains, addressing challenges associated with power efficiency, performance, and integration density. In the domain of interconnection, alloy solder can join different materials with robust bonding performance. Solders with different melting points can be selected according to specific applications. Solders containing, e.g., In and Sn, have a low melting point, while solders formed by, e.g., Au, Ag, and Cu, are called hard solders with a tunable high melting point. The flexibility of the operation temperature makes alloy solders significant in packing high-power electronics [7], optoelectronics[8], and MEMS [8, 9] in the MtM paradigm. However, the processing temperature of solder is usually 20 °C

higher than its melting point, which may be harmful to the electronic components in the system.

Hence, as an excellent interconnect technology that decouples the processing temperature and operation temperature, incorporating nanoparticles sintering technology within the HIR adds a crucial dimension to the diverse technological landscape outlined by HIR. Specifically, none of the known solders can work in an extreme operating temperature exceeding 500 °C [10]. Thus, nanoparticles sintering technology is pivotal in integrating disparate materials and components in advanced semiconductor packaging. By enabling efficient bonding at reduced temperatures (<0.4 T_m), the sintered structure closely matches its bulk status, contributing to the HIR's goals of enhancing system-level performance and functionality, and addressing challenges related to thermal management and compatibility [11–13].

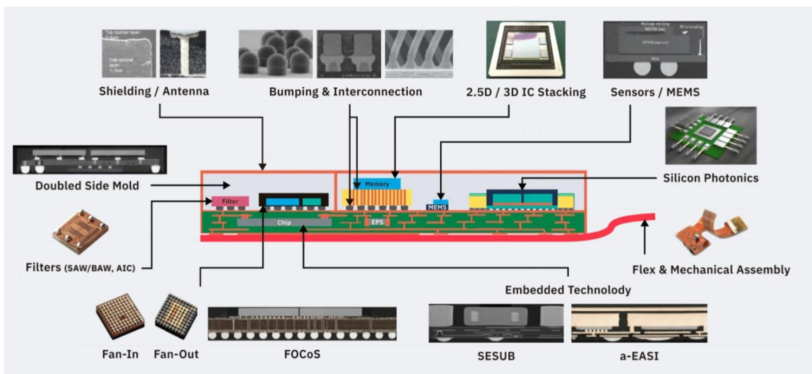

Figure 1.2.: Technology building blocks for heterogeneous integration (Source: ASE).

To understand the state-of-the-art low-temperature sintering technology, pressure-assisted and pressureless nanoparticles sintering approaches are introduced and summarized, highlighting several representative research works. Following this, a brief review of low-temperature sintering technology in various HIR domains is provided. Applications in high power/temperature packaging and multi-chip three-dimensional (3D) integration are discussed.

1.2. Overview of nanoparticles sintering approaches

Sintering is an ancient technique that has been utilized by humans for thousands of years. In modern society, sintering plays a vital role in producing a wide range of high-tech materials and products. It is a solid-state process of compacting and forming solid materials by heating a powdery material to a temperature below its melting point [14]. Figure 1.3 illustrates the sintering process in a multi-NPs material system. After densification, the NPs adhere to adjacent NPs, forming inter-particle necks. Consequently, the sintered materials achieve performance levels comparable to their bulk counterparts. The performance reduction is highly dependent on the mean porosity of the sintered materials [15].

One of the most attractive merits of nanoparticles sintering technology is its ability to achieve a low processing temperature while maintaining outstanding thermo-mechanical robustness at higher temperatures. At the microscale, the formation of the necking area, which determines macroscale densification, is governed by several mass transportation paths from the initial NPs to the necking area. As shown in the dual-NP model in Fig. 1.3, various competing mechanisms coexist in neck growth, including surface diffusion, grain boundary diffusion, lattice diffusion, surface vapor transport, and plastic flow induced by dislocation motion [16, 17].

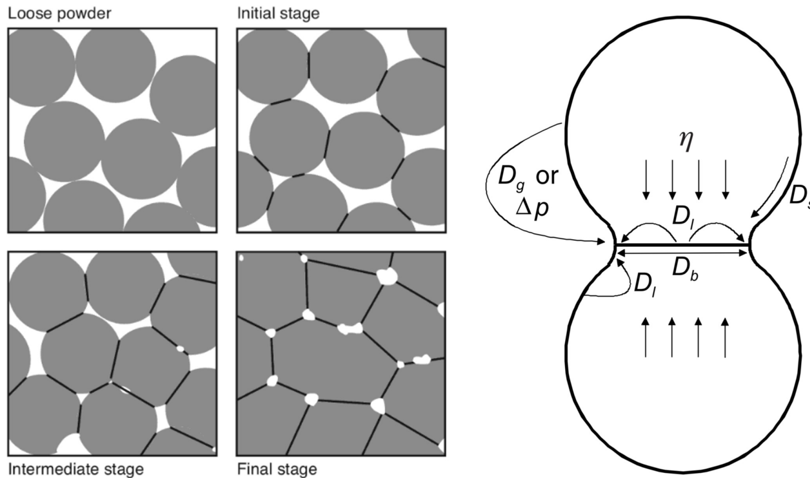

Figure 1.3.: A schematic of the multi-NP sintering process and a dual-NP model of the mass transport paths during the sintering process [17].

1.2.1. PRESSURE-ASSISTED NANOPARTICLES SINTERING

PROMOTING sintering results relies on the driving force of the abovementioned mass transportation, where external energy dominates. Beyond heating, external sintering pressure has been demonstrated as an effective method to shorten the sintering process. Low-temperature pressure-assisted sintering has recently received significant attention for its excellent electrical and thermal conductivity, which is highly valued in heterogeneous integration.

Figure 1.4 depicts a schematic of the thermal pressure-assisted Cu nanoparticles sintering process. The modulated nanoparticle paste generally contains organic additives (protective shell/passivating, binder, and solvents). The sintering process undergoes an inert/reducing sintering atmosphere to address oxidation risk and agglomeration tendency [18–20]. Besides, stencil printing is a widely adopted method to transfer paste patterns to the substrate, which ensures a flat paste surface. The surface pits are likely to cause subsequent voids and consequent delamination of the bonding interface [21].

Table 1.1 compares low-temperature pressure-assisted sintering and several lead-free bonding technologies, such as Sn-Ag-Cu (SAC) solder and AuSn solder. As alternative

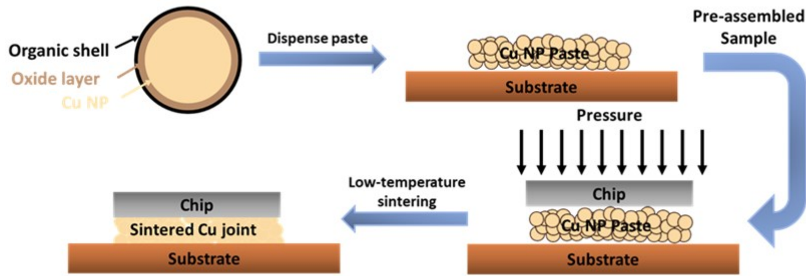

Figure 1.4.: Schematic of thermal pressure-assisted sintering process flow.

technologies, Ag sintering, Cu sintering, and hybrid Ag-Cu sintering share the merits of high thermal conductivity, high melting point and a relatively lower coefficient of thermal expansion (CTE). The CTE mismatch-induced stress accumulation is one of the challenges for high-reliability performance, and a minor CTE mismatch is desired in the microsystem [22]. Besides, it's noticeable that the elastic modulus of the sintered materials can be much lower than its bulk materials, as 83 GPa for Ag and 130 GPa for Cu, respectively. The tunability of the thermo-mechanical properties depends on the process conditions, as shown in Fig. 1.5, including temperature, pressure, time, and particle size, which, on the other hand, increases more flexibility for low-temperature sintering technology to fit different applications.

Table 1.1.: Comparison of materials properties between different lead-free bonding technologies

Bonding materials	Process temperature [°C]	Melting point [°C]	CTE [$10^{-6}K^{-1}$]	Elastic modulus [GPa]	Thermal conductivity [W/(mK)]	Cost
SAC [23–26]	~217	~217	21	30-54	~60	- -
AuSn [27–29]	280	280	16	39-76	59	+++
Ag sintering [27, 30, 31]	<280	~960	18-23	29-65	>100	++
Ag-Cu sintering [32, 33]	<280	960-1084	13	16	>100	+
Cu sintering [27, 30, 34]	<280	~1084	16-21	12-55	>100	-

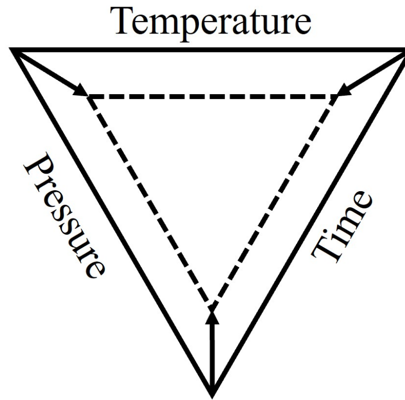

Figure 1.5.: The triangle of sintering temperature, pressure, and time to produce reliable sintered joints. The dashed triangle utilizes nanoparticles' surface curvature and surface energy to reduce these three parameters simultaneously [35].

1.2.2. PRESSURELESS NANOPARTICLES SINTERING

DESPITE the excellent performance in a pressure-assisted joint, pressureless sintering is also developed to reduce the process cost for large-scale production. Additionally, pressureless sintering is necessary in the case of fragile components in the microsystem. As indicated in Fig. 1.5, implementing pressureless sintering requires increased temperature and time simultaneously. Alternatively, the nanoparticle size reduction can soften the other two process parameters. However, to avoid self-sintering ability before the sintering process, thermosetting resin can be added to the formulation of the paste [36, 37]. However, the polymeric matrix added paste sintered thermal and electrical performance would be slightly compromised due to a relatively lower metal content [38].

Moreover, the reliability of the sintered joint highly corresponds to the die size. Compared to pressure-assisted sintering, the pressureless sintered joint is less reliable because oxygen cannot penetrate the central region to pyrolyze the organic contents in the case of a large die [39]. Hence, one mainstream of the pressureless sintering development is towards large-area sintering. Pressureless Ag sintering has been reported to bond die with an area of 100 mm^2 [40, 41]. Pressureless Cu sintering is developed slightly behind due to easy oxidation issues during the sintering process. The value for the current state-of-the-art is 25 mm^2 [42].

The reduction of parameters in Fig.1.5, ultrasonic, can also promote pressureless sintering as external energies [43]. Moreover, conventional oven heating is typically time-consuming. Other alternative energy sources, e.g., laser [44], plasma [45, 46], and electrical field [47], have been reported to implement low-temperature pressureless sintering.

The laser-assisted sintering method takes advantage of a rapid ramping rate, confined heat-affected region, and low sintering temperature, yielding higher electrical conductivity [48–50]. Despite sintering taking place around the laser focal point, low-temperature

laser sintering can fabricate continuous structures [44]. The quality of the sintered structure depends on the laser conditions, e.g., laser wavelength and specific energy, as shown in Fig. 1.6(a). Lasers with different wavelengths have different penetration capabilities in the NPs, and a larger wavelength results in a more immense depth [51]. In addition, as an alternative to Ag nanoparticles, the usage of Cu nanoparticles has been demonstrated to achieve high electrical conductivity close to the bulk Cu [52, 53].

Plasma-assisted sintering is also an alternative to implementing sintered patterns on thermal-sensitive substrates. Excited species generated from the plasma can cause chain scission and subsequently decompose the stabilizing organic agent, resulting in contact with nanoparticles and further compaction [54]. In general, the plasma sintering can be achieved below 75 °C, making it compatible with most flexible substrates, such as polyethylene terephthalate (PET) or polyethylene naphtholate (PEN) with glass transition temperatures (T_g) well below 150 °C [55, 56]. Compared to oven heating, the plasma can reach close electrical performance after one hour, as depicted in Figure 1.6(b). Besides, the plasma sintering is less determined by the plasma condition. In the bottom figure in Fig. 1.6(b), despite different plasma energies as 150 W and 300 W, the plasma sintering yields close resistivity ~ 28 $\mu\Omega$·cm.

Electrical sintering utilizes Joule heating to thermally sinter nanoparticles. Therefore, a pre-heating process is required to allow the flow of the electrical current [57]. Afterward, electrical current flows through the initial inter-particle contact, generating heat to promote neck growth. The resistance drops with the continuous sintering, and the electrical current increases accordingly. It is also a pressureless sintering technology that is friendly to thermal-sensitive substrates since the generated Joule heat is localized around the sintered pattern. The entire sintering process consists of three stages: a pre-sintering phase, a transition phase where major sintering occurs, and a large current phase, as depicted in Figure 1.6(c). Compared to the other alternative pressureless sintering technologies, electrical sintering has the merits of short sintering time (in a few milli-seconds) and better control of the final conductivity [58].

1.3. THE ROLE OF NANOPARTICLES SINTERING IN HETEROGENEOUS INTEGRATION ROADMAP

1.3.1. NANOPARTICLES SINTERING IN HIGH POWER/TEMPERATURE PACKAGING

IN the last decade, driven by the increasing demand for higher power density and power efficiency, wide-bandgap (WBG) semiconductor devices, represented by silicon carbide (SiC) and gallium nitride (GaN), have played a more critical role in high-power and high-frequency applications, as shown in Fig. 1.7(a) [63, 64]. Taking the electrical vehicle market as an example in Fig. 1.7(b), a rapid market growth contributed by multi-chip SiC modules is forecasted by the advantages of its larger bandgap, higher critical electrical field, and higher thermal conductivity [65].

Figure 1.8 depicts a transfer molded power module solution structure schematic with a Cu clip directly bonded on the source pad. It can be seen that from top to bottom, there are three bonding layers: clip-attach, die-attach, and module-attach. All these bonding

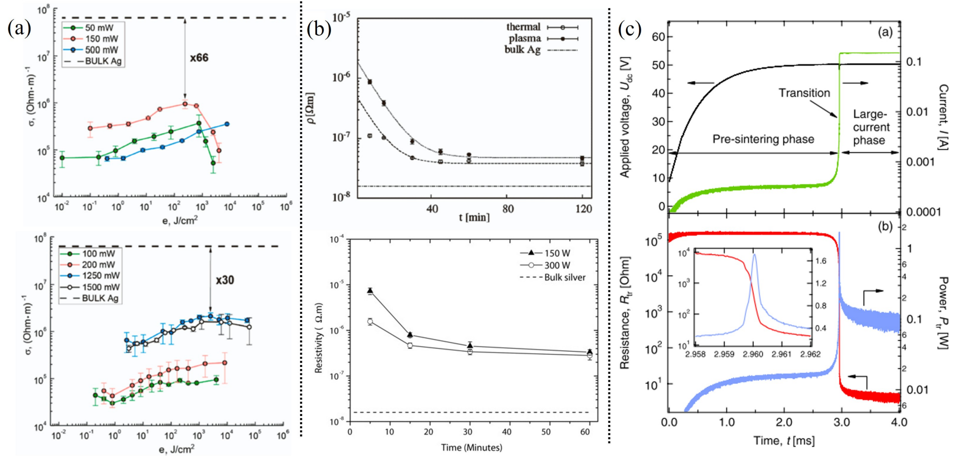

Figure 1.6.: (a) The electrical conductivity of laser-sintered Ag NPs obtained at a 527 nm laser wavelength (top) and a 1024 nm laser wavelength (bottom) with different specific energies [59]. (b) The resistivity of different sintering methods (top) and plasma sintering with different power (bottom) as a function of time [60, 61]. (c) The voltage (top) and resistance (bottom) of electrical sintering as a function of time [62].

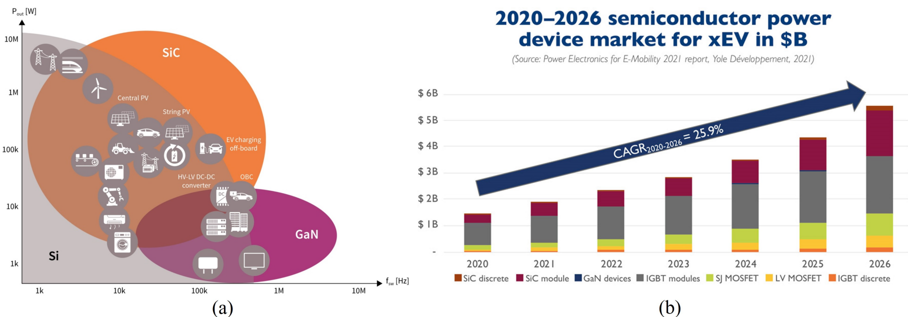

Figure 1.7.: (a) Typical applications of WBG semiconductors (Source: Infineon). (b). 2020-2026 semiconductor power device market for xEV (Source: Yole).

layers can be contributed by low-temperature nanoparticles sintering.

Die-attach is the closest layer to the power chip. Thus, a desired die-attach layer with high thermal conductivity can quickly get the heat away, resulting in a lower junction temperature. As a result, low-temperature sintering is widely applied in the die-attach application, outperforming conventional reflow soldering and transient liquid bonding [13, 27].

Recently, to handle higher current density and higher operation temperature, Cu clip bonding has been considered to replace wire bonding for lower resistance, lower in-

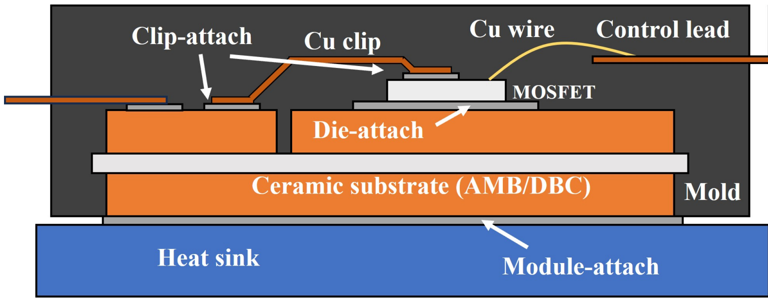

Figure 1.8.: Structure diagram of power module package with Cu clip.

ductance, and promoted reliability performance [66–68]. Currently, most clip-attach is soldered on the chip top surface by considering other factors such as cost, process complexity, etc. Some pioneer low-temperature sintering works have been reported using Ag and Cu sintered Cu clips with promoted performance [69, 70]. It is believed to have approximately 30 % die-temperature reduction compared to the conventional soldered joints [71].

Limited reports on the module attachment can be found regarding attaching the entire power module to the baseplate or directly to the heatsink. Low-temperature sintering technology is facing challenges due to the large bonding area. The organic burnout and exhaust in the paste composition and the thermal warpage at the sintering temperature significantly affect the thermal and mechanical performance of the sintered layer [72]. According to the development of large-area sintering, some attempts have been made to bond the entire power module with promoted performance [69, 73–75].

Regarding high-temperature packaging, light-emitting diodes (LEDs) are one of the market's most power-efficient solid-state lighting sources [76, 77]. Figure 1.9 presents three main LED module structures: laterally spaced electrodes, flip-chip structures, and vertically spaced electrodes with different power ranges.

The vertical structure is typically applied in high- and super-high-power applications, with the current vertically flowing through the structure. To date, the electro-optical conversion efficiency of an LED chip is no higher than 60%, and the rest of the energy is dissipated as thermal energy. Hence, the thermal challenge (junction temperature $> 150\ ^{\circ}C$) significantly threatens the maximum light output, efficiency, and lifetime [78]. Thermal management can be improved in various components, such as die-attach, wirebonding, encapsulation, and heatsinks [79–81]. Hence, as a promising high-temperature die-attach technology, low-temperature sintering shows capability in high- and super-high-power LED packages.

Ag sintering technology is the most proven in LED packaging due to its excellent thermal and electrical conductivity. Various forms of Ag sinter materials have been proven in applications with different temperature ranges, such as paste, foil, and sputtered layers [82–84]. Beyond the Ag sintering technology, more sinter materials have been investigated to reduce the cost and minimize the electromigration of silver. Cu-Ag hybrid sintered and pure Cu sintered materials have demonstrated incredible thermal performance in LED packages [30, 85, 86]. It should be noted that the selection of die-attach materi-

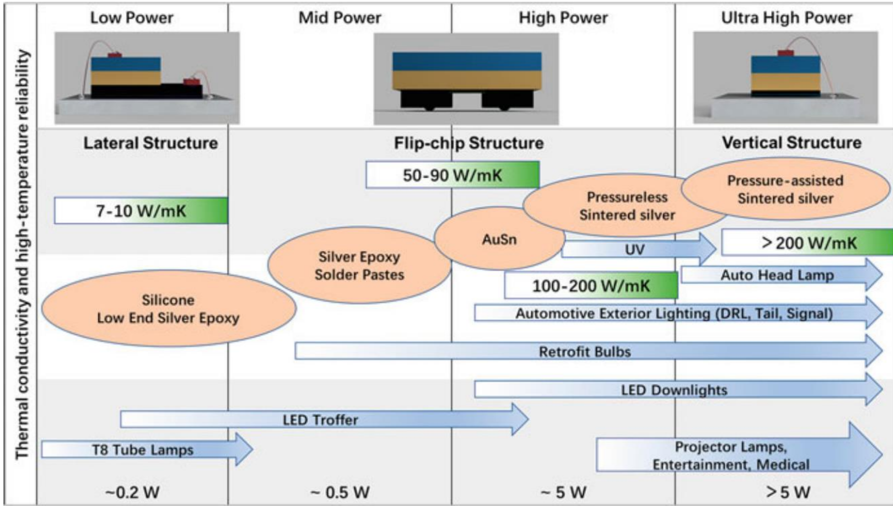

Figure 1.9.: Structure of commonly seen LED modules and suitable power range [27].

als is essential because die-attach occupies a critical part of the total cost of the LED package. Thus, low-temperature sintering is currently most suitable for high- and ultra-high-power LED packages, as indicated in Fig. 1.9.

1.3.2. NANOPARTICLES SINTERING IN MULTI-CHIP 3D INTEGRATION

BESIDES high power/temperature packaging, system-in-package (SiP), where the active integrated circuits (ICs) communicate with passive components within the package, is also a key concept to promote MtM. In emerging fields, such as mm-wave packages in communication systems, the requirement of low losses and high component densities simultaneously drives the development of 3D integration technology [87]. Figure 1.10 depicts a schematic representation of heterogeneous 5G package integration [88]. It can be seen that besides the bonding layer, other metal components, such as circuits & traces and through-silicon-via (TSV), are also potentially formed by low-temperature sintering technology as an additive manufacturing (AM) technology.

Redistribution layers (RDLs) are used to implement lateral communication that makes its I/O pads available in the desired locations of the chips [89]. Commonly, RDL fabrication is achieved by combining photolithography and the metal plating process. The involvement of lithography increases the process complexity and cost, especially in a multi-layer RDL fabrication. To allow fast prototypes, sintered Ag has been demonstrated as RDLs and contact pads with considerable thickness and width, employing ink-jet printing [90–92] and screen-printing [93]. Compared to the high power/temperature packaging application, the thermal burden in multi-chip 3D integration is less challenging. Therefore, a form of metal ink is widely applied here, where the metal content is relatively sacrificed, but a tunable low viscosity can be implemented for better printability.

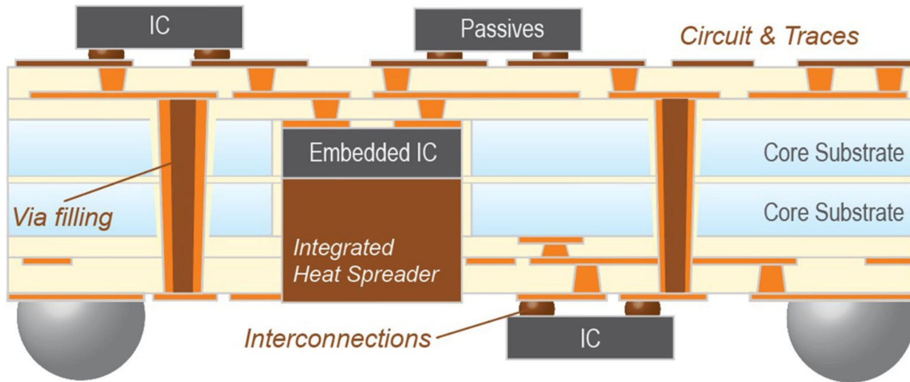

Figure 1.10.: Schematic representation of heterogeneous 5G package integration [88].

TSV filling is another crucial technology for signal transmission in a 3D integrated microsystem [94]. The current TSV filling technology consists of barrier deposition, Cu seed layer deposition, Cu via electroplating, and chemical mechanical polishing (CMP) to flatten the surface. Therefore, the low-temperature sintered structure shows competitiveness because it can skip the time-consuming electroplating and CMP processes due to no presence of metal overburden [95]. Like the application methods in RDL fabrication, ink-jet printing is mainly applied to fill the vias because of the high aspect ratio. Different sinter materials, such as Ag [93, 96, 97] and Cu [95], have been investigated to decrease the process complexity and promote performance. Moreover, the decreased process temperature enables low-temperature sintering via filling in a flexible substrate, significantly expanding its application [98].

Additionally, driven by the demand for high-density packaging and better power handling, bonding technology with a reduced interconnection pitch is urgently needed because a fine pitch challenges the applicability of conventional solder alloys [99]. As mentioned in high power/temperature packaging, low-temperature sintering has excellent performance advantages over conventional solders. Ag [100, 101] and Cu [102] sintering technologies have been demonstrated in fine-pitch bonding with profound reliability performance. Thus, the focus goes more to the application approaches because conventional screen printing cannot deal with such fine pitch size. Besides, bonding materials usually contain higher metal content for better thermal and electrical conductivity. Therefore, ink-jet printing is rarely reported in die-bonding. As alternatives, in Fig. 1.11, approaches, such as electroless plating [103], dip-transfer [104, 105], and photolithography-assisted stencil printing [106], have shown the competence to reach fine pitch (< 1 μm) bonding.

1.4. MOTIVATION AND OUTLINE OF THIS THESIS

THE previous introduction indicated that nanoparticles sintering technology holds many advantages over other heterogeneous integration technology in dedicated application fields, especially in the coming era of WBG semiconductors. However, most

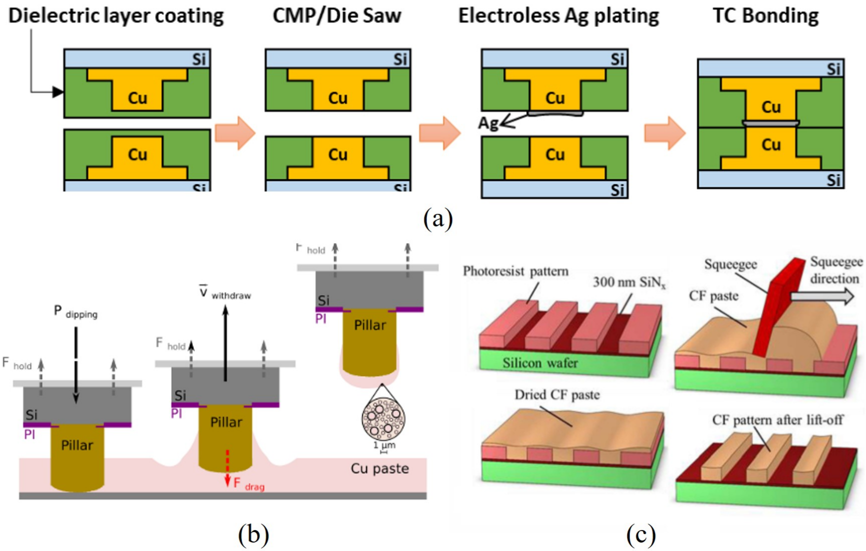

Figure 1.11.: Process flow to achieve fine-pitch bonding beyond conventional stencil printing. (a) Electroless plating [103]; (b)Dip-transfer [105]; (c) Photolithography-assisted stencil printing [106].

studies focused on either materials perspective or presented performance. A comprehensive understanding spanning from the microscopic to macroscopic levels, encompassing materials, processes, characterization, reliability, and application validation, is imperative for the seamless integration of low-temperature nanoparticle sintering technology into the power electronics modules and beyond applications. To pursuit this goal, several research questions and challenges are formulated below from scientific and technological perspectives.

1. **Question**: How does atomistic simulation contribute to understanding the coalescence process and mechanical and chemical performance of the coalesced structure?
   Challenge: Conducting atomistic simulations to study nanoparticle coalescence requires specialized computational resources and expertise. Additionally, accurately simulating the mechanical response of coalesced nanoparticles and understanding the chemical corrosion process necessitates extensive computational modeling.

2. **Question**: What insights can be gained from multi-scale mechanical tests, including micro-cantilever bending and high-temperature deformation tests, regarding the mechanical behavior of low-temperature sintered nanoparticles?
   Challenge: Performing multi-scale mechanical tests involves intricate experimental setups and multi-scale sample fabrication. Extracting and analyzing data from

these tests require sophisticated techniques and instrumentation.

3. **Question**: How can the implementation of transient thermal performance characterization and health monitoring during thermal cycling tests be effectively utilized as indicators of reliability in power device packaging applications?
Challenge: Designing and implementing offline and online thermal performance characterization methods require careful consideration of experimental setup and data interpretation. Ensuring the accuracy and reliability of these methods poses challenges in calibration, validation, and interpretation of results, crucial for assessing the long-term reliability and health condition of power device packages.

4. **Question**: What are the reliability implications of using low-temperature nanoparticles sintering technology in HIR domains such as power packaging and hermetic packages?
Challenge: Assessing the reliability of devices and packages manufactured using low-temperature nanoparticles sintering technology requires comprehensive testing, including thermal cycling tests and thermal shock tests. Analyzing reliability data and correlating it with simulation results demand expertise in both experimental techniques and computational modeling.

To answer the aforementioned research questions, the rest of this dissertation is structured as follows, as shown in Fig. 1.12. In Chapter 2 ***Atomistic simulation on nanoparticle coalescence and coalescenced structure***, atomistic simulation approaches have been applied to investigate the low-temperature nanoparticle sintering technology. At first, a two-hemispherical nanoparticle model was built to study the coalescence process at the atomic scale. Afterward, the tensile performance of the coalescence pair was simulated by adding a uniaxial force. The atomistic study expanded to a multi-nanoparticle system, where the nanoindentation simulation was conducted. The influence of indenter size and local porosity on the indentation performance was, therefore, bridged. At the end of Chapter 2, according to the corrosion issue, the sulphidation process on the sintered Ag was studied by the ReaxFF based atomistic study, where the sulphidation rate and mechanism were revealed.

In Chapter 3 ***Multi-scale mechanical behaviour of the sintered nanoparticles***, the multi-scale mechanical performance of the sintered nanoparticles was evaluated through a micro-cantilever bending test and hot deformation test. The micro-cantilevers were micro-fabricated by a focus ion beam (FIB) with designed dimensions and different notch depths. The J-integral with different notch depth was extracted based on the continuous dynamic test, and the microscopic fracture toughness was consequently calculated. In addition, the sintered nanoparticles were machined into a dog-bone tensile specimen for hot deformation tests at multiple temperatures and strain rates. Consequently, an Anand model has been parameterized to describe the constitutive behavior. The multi-scale mechanical test revealed failure mechanisms of the sintered structure and indicated robust mechanical performance enabled by low-temperature nanoparticles sintering technology.

In Chapter 4 ***Offline and online thermal monitoring of the sintered nanoparticles***, attention was paid to thermal performance. The transient thermal performance of sintered

nanoparticles was evaluated by sintering a Si thermal test chip (TTC) on a Cu substrate. The junction-to-case thermal resistance of three different nanoparticle pastes was calculated and compared following the JEDEC 51-14[107]. Regarding the online health monitoring over a thermal aging test. Si power MOSFETs were sintered in a quad-flat package (QFN) discrete package. In the −50°C to 150°C thermal cycling test (TCT) process, a heat pulse was introduced at the cold phase, and the transient thermal performance was therefore evaluated. The thermal degradation of nanoparticles in a sintered package was demonstrated as the evolution of impedance. The development of online thermal monitoring is essential to accurate lifetime estimation in low-temperature nanoparticles sintered products.

Chapter 5 ***Metallic nanoparticles sintered Si TO247 power device*** introduced the application of low-temperature nanoparticles sintering technology in the Si IGBT TO247 device. 1200V/50A Si IGBTs were sintered on an Ag-plated Cu leadframe with multiple nanoparticle paste. A commercial silver paste was set as a benchmark. In addition, thick Al wiring bonding and Al ribbon bonding were applied as the die top interconnect. Afterward, the reliability performance of the manufactured discrete package was evaluated in −50°C to 150°C TCT and thermal shock test (TST), respectively. I-V characteristics and junction-to-case thermal resistance change recorded slight electrical and thermal degradation. In addition, scanning acoustic microscopy (SAM) images were also employed to evaluate the die-attach layer adhesion. Meanwhile, FEM were applied to simulate the stress distribution by adopting the parameters from previous chapters. The simulation result was consistent with the observed void nucleation location. The results obtained in this chapter indicated outstanding thermal robustness of the nanoparticles sintered TO247 package.

Chapter 6 ***Metallic nanoparticles sintered hermetic package*** introduced the application of low-temperature nanoparticles sintering technology in a Si cavity hermetic package. A groove-structured Si test chip was fabricated with Ti/Au metallization. Afterward, the nanoparticle paste was transferred on the Ti/Au metalized Si chip with a lithographic mask, resulting in a 50 μm width sealing ring. Subsequently, a Si cavity with the same metallization was bonded on the Si test chip. The bonding parameters were optimized to implement the hermetic package in the Si cavity. FEM indirectly assessed the sealed cavity pressure. Furthermore, the evolution of diaphragm deflection over 180 days determined low leakage of the hermetic package. Thus, low-temperature nanoparticles sintering technology has been demonstrated as a flexible and robust hermetic package solution.

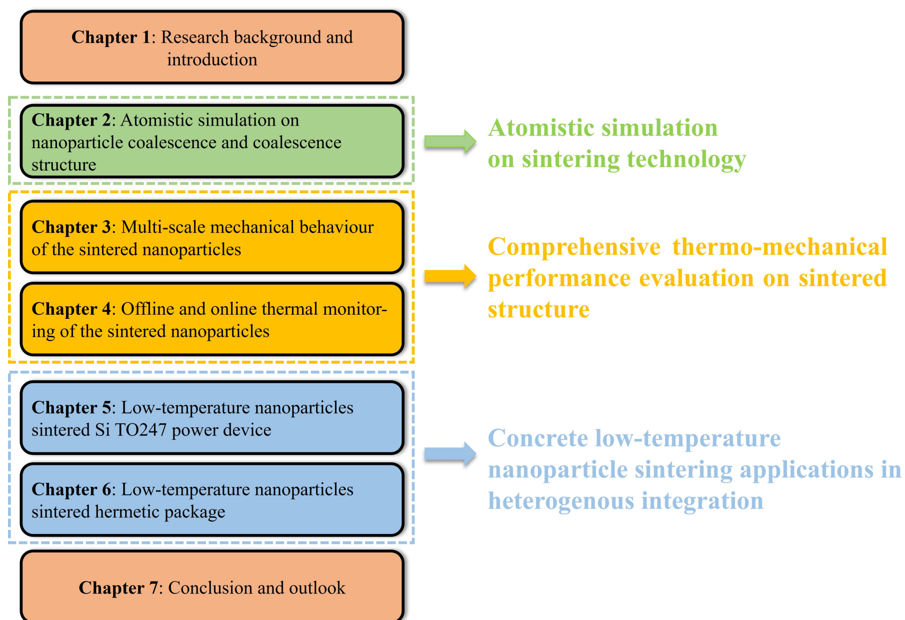

Figure 1.12.: The outline of the dissertation.

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2

ATOMISTIC SIMULATION ON NANOPARTICLE COALESCENCE AND COALESCENCED STRUCTURE

As a critical part of MtM, power electronics and its packaging technology are undergoing rapid development. Low-temperature nanoparticle sintering technology has received extensive attention for its excellent performance. Therefore, the study at an atomistic level is essential to deepen the understanding of this hot technology. MD simulations are performed on the coalescence kinetics of the pressure-assisted Cu NPs sintering. The effects of sintering pressure and sintering temperature on the coalescence of the NPs were revealed by a two-hemispherical NPs model. A transition of the dominant coalescence kinetics from slight surface diffusion to intensive grain boundary diffusion and dislocation driven plastic flows were found as pressure applied. Additionally, based on the sintered structure, uniaxial tension simulation was implemented with a constant strain rate. Furthermore, expanding from the understanding built on the two-hemispherical NPs model, multi-spherical models were constructed to explore the nanoindentation performance. The impact of indentation position and indenter size on the nanoindentation response was investigated. Besides the mechanical response, study on the chemical reaction on the sintered structure was attempted. Reactive force field (ReaxFF) MD was utilized to study the sulphidation on the sintered Ag NPs structure, revealing the formation of sulphide layer as upward migrated Ag atoms.

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2.1. Introduction

In general, the coalescence of NPs during sintering involves at least five mechanisms for mass transport, including grain boundary diffusion, surface diffusion, volume diffusion, dislocation activity, and surface evaporation-condensation [3]. The contributions of diffusion mechanisms on the evolution of particles shape were theoretically studied in the works of Coblenz *et al.* [4], Venkateshwarlu *et al.* [5] and Djohari *et al.* [6, 7]. By using Frenkels model based on continuum theory [8, 9], those work showed that the atomic concentration gradient and stress gradient contributed the driving forces for the mass transport of NPs from the center to the surface, resulting in the NPs coalescence. At the atomic scale, MD studies on NPs sintering provided an insight in understanding various NPs coalescence (Cu [10, 11], Au [12], Fe [13], Ta [14]). Goudeli *et al.* established a two-NP model to investigate the thermodynamic process of Cu NPs sintering [15]. It was found that elevated temperature can lead to a larger degree of NPs coalescence by affecting its atomic diffusion rate as well as the degree of plastic deformation. Besides, Ding *et al.* investigated the effect of the relative crystal orientation on neck growth, in which it was observed that a reorientation of particles took place to match a preferred crystalline orientation at the beginning of the sintering [16]. Additionally, the work done by Grammatikopoulos *et al.* studied the size effect on NPs sintering [17]. It was found that the smaller NPs have more dislocation nucleation, growth, and sliding of stacking faults at the junction of nanoparticles, compared to larger NPs, which efficiently promote the NPs to coalesces into the larger and uniform grains.

The pressure is another significant influential factor on NPs coalescence. From the perspective of experiments, Knoerr and Schletz reported that the density of the sintered layer of Ag NPs can be improved from 58% to 90% when the sintering pressure increased from 0 MPa to 30 MPa [18]. The increased density corresponded to the improvement of electrical and thermal conductivity of the sintered Ag layer. Zhao et al. applied pressure-assisted sintering in power electronic packaging, and better reliability performance was obtained compared to those soldered power module [19]. Therefore, the sintering pressure is preferred to ensure excellent reliability of the sintered layer in a harsh environment. Based on the continuum theory, it is believed that the external pressure applied on NPs can be amplified at the neck region, which further causes a large mechanical stress gradient from the mass central to the neck surface, accelerating the atomic immigration towards the neck region.

However, above mentioned understandings on the underlying relation between external pressure and microstructure evolution during NPs sintering are not clear. In particular, the question of how pressure affects dislocation activity and surface and bulk transport is still open. In addition, the mechanical performance of the sintered structure also need to quickly assess the sintering results. In atomisitic simulation, by assigning an elongation rate of simulation box along one direction, Yang *et al.* implemented tensile testing simulation on pressureless sintered porous Cu structure at a strain rate of $1 \times 10^{-8}\ s^{-1}$ and stress-strain curves were derived [20]. Similarly, Zhang *et al.* investigated the mechanical strength by performing MD tension simulation on a 41-Nickle NPs sintered system with a strain rate of $1 \times 10^{-9}\ s^{-1}$ [21]. But the sintering process was pressureless. To reveal the role of pressure, efforts also have been conducted in the two-NP model, where the interconnection process between NPs can be more concentrated on.

Wang *et al.* qualitatively analyzed the dislocation-stress interaction under compression condition, while the sintering pressure was not quantitatively controlled and the mechanical properties were not evaluated [21]. Besides the tensile test, nanoindentation is commonly adopted to study the mechanical properties of the sintered die-attach layer due to the thin bondline thickness [22–24]. One main drawback of nanoindentation test on the sintered structure is that the stochastic porous microstructure leads to various results in a single specimen. Thus, it is vital to understand the nanoindentation behavior on the sintered structure from an atomistic perspective.

In addition the focus on the die-attach cannot only land on the thermal-mechanical properties. In the case of Ag sintering, which is widely applied in the power electronics industries, the corrosion failure, is a severe issue for reliable performance [25]. Atmospheric corrosion of bulk silver has been widely studied [25, 26]. Silver becomes tarnished at ambient pressure when exposed to atmospheric environments due to the presence of corrosive substances, such as SO_2, SO_3, O_2, and O_3 [27, 28]. In addition, the influence factors, such as the relative humidity and concentrations of sulphur and ozone, have also been widely reported [29–31]. Furthermore, a considerate amount of literature has been published on silver tarnishing simulations. Despite the complex reactions, the adsorption site energetics for sulphur and oxygen on various silver surfaces have been calculated by density function theory [32]. MD simulations have high potential to handle large, complex simulation systems for silver tarnishing [33, 34]. ReaxFF MD, as an empirical force field method to study chemical reactions, enriches the approximations with an adequate interatomic potential utilizing the reactive bond order [35]. Utilizing ReaxFF, Saleh *et al.* revealed the formation mechanism of silver oxide and silver sulphide and developed the related Ag/S and Ag/O force fields [36]. However, the corrosion in sintered silver nanoparticles has barely been reported in atomistic simulations.

In this chapter, by using the MD calculation method, A two-hemispherical NPs model was at first built up in Section 2.2 to investigate pressure-assisted sintering of Cu NPs at a low temperature. The effect of various pressure magnitudes on Cu NPs sintering is revealed and the mechanisms behind pressure-assisted sintering are discussed. Furthermore, in Section 2.3, on the basics of pressure-assisted sintered Cu NPs, uniaxial tensile tests with a constant strain rate were employed to investigate its mechanical behaviors. In addition, in Section 2.4, atomic model containing multi-NPs was developed for nanoindentation simulation, which was not possible to be carried out on a two-hemispherical model. The impact of indentation position and indenter size on the nanoindentation response was investigated. At last in Section 2.5, a simplified Ag multi-NPs model was constructed to investigate the sulphidation behaviour in the sintered Ag NPs by utilizing ReaxFF MD, compared with a dense Ag multi-NPs model.

2.2. ATOMISTIC SIMULATION ON COALESCENCE

2.2.1. SIMULATION METHODOLOGY

In this section, Large-scale Atomic/Molecular Massively Parallel Simulator (LAMMPs) was employed to conduct all the simulations [37]. The classical embedded atom method (EAM) potential developed by Adam*et al.* [38] was applied for describing the interactions between Cu atoms. This potential has been proven to accurately calculate the cohesive

energy, lattice parameters, elastic constants, phase diagram and high-temperature properties of Cu NPs [17, 39–41]. Newton's equation of motion was integrated with the Verlet algorithm. The atomic configurations in our study were visualized by a 3D visualization software, OVITO [42].

Normally, the coalescence for Cu NPs at a low temperature (< 573 K) mostly occurs at the contacting neck. The region far away from the neck slightly affects the sintering efficiency of Cu NPs. Thus, in the present model as shown in Fig. 2.1, two hemispherical Cu NPs with an indentor at the top and a basement at the bottom were constructed. In this model, the basement is used to fix the position of the structure and the indentor is used to apply pressure. Based on previous studies, a radius of NP within 1.4 − 3 nm is feasible to reveal the sintering kinetics [17, 20, 21, 43, 44]. Thus, in the present study, the radius of a single Cu NP is selected as 2.5 nm and the length of indentor and basement is 10 nm. The simulation box has 10048 atoms for both hemispherical Cu NPs and 32000 atoms in total. In addition, in many published works, 2 − 5 Å initial distance between NPs is selected. Therefore, in the present study, a 3.6 Å initial distance is selected, that is the length of lattice constant of Cu and located in the acceptable range reported in the literature [45–47].

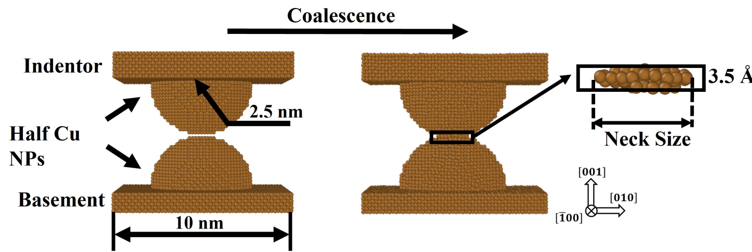


Figure 2.1.: Two-half Cu NPs model and geometric parameters for the coalescence simulation.

In all simulations, a timestep of 1 fs was chosen for calculation and the periodic boundary condition was applied in the three dimensions. The positions and velocities of each Cu atoms were recorded in every 1 ps. Fig. 2.1 exhibits the geometric parameters obtained in the simulation. To obtain the neck size, a dynamically allocated block region with 3.5 Å thickness was empirically defined in the neck region, containing less than three layers of Cu NPs. The neck size at each specific timestep was calculated from the coordinates of boundaries atoms along [010] direction. Furthermore, the MSD of the entire system was calculated to evaluate the degree of coalescence, which can be computed by using the following equation,

$$MSD = \frac{1}{N}\sum_{i=1}^{N}[r_i\ (t) - r_i\ (0)]^2 \tag{2.1}$$

where N is the number of atoms, $r_i(t)$ and $r_i(0)$ are the position of atom i at time t and 0, respectively.

The sintering simulation can be divided into three periods , as described in Fig. 2.2 with different colours. Different ensembles were applied with N in the ensemble name

standing for the constant total number of particles in the system, V for the constant system's volume, E for the constant total energy in the system, P for the constant system pressure and T for the constant system temperature:

(1) The energy of the system was first minimized and the coordinates of the atoms were iteratively adjusted (< 1000 iterations) until the change in energy between outer iteration was less than 1×10^{-8} or the length of the global force vector was less than 1×10^{-8} eV/Å. After that, we relaxed the system at 300 K in the NVE(microcanonical) ensemble for 50 ps.

(2) Then the system was heated up to various target temperatures (300 K, 400 K, 500 K) within 200 ps and relaxed for another 200 ps in the NPT(isothermal-isobaric) ensemble.

(3) After that, external pressure was assigned to the top three layers of the indentor to simulate the pressure-assisted sintering. In this step, four different pressures were selected (0, 100, 200, 300 MPa).

Afterwards, the entire model was run for 800 ps in the NVT(canonical) ensemble to reach its equilibrium state. As a note, in the present study, to distinguish the independent effects of temperature and pressure on Cu NPs sintering, the second step was conducted in NPT(isothermal-isobaric) ensemble with zero pressure to avoid the effect from pressure variation on the simulation box. Similarly, the third step was conducted in the NVT(canonical) ensemble with constant temperature to avoid the effect of temperature variation.

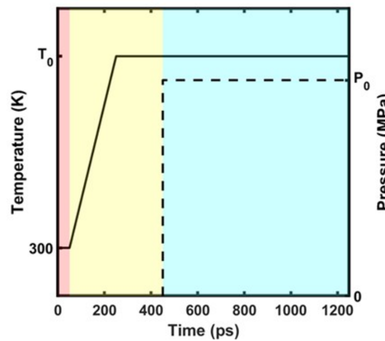


Figure 2.2.: Illustration for the temperature and pressure profile, in which four different pressures (0, 100, 200, 300 MPa) and three different temperatures (300, 400, 500 K) are selected.)

2.2.2. COALESCENCE KINETIC OF THE PRESSURE-ASSISTED CU NPS SINTERING

A whole coalescence process of the pressure-assisted Cu NPs sintering under 300 MPa and 500 K is presented. As Cu is one of the typical face-centered cubic (FCC) metals with

low stacking fault energy (SFE), the FCC and hexagonal close-packed (HCP) structures can be transformed to each other with thermal or mechanical stimuli such as heating, pressuring, or plastic deformation [48]. Thus, in Fig. 2.3, the evolution of the total dislocation length and the fraction of HCP ratio are plotted. Data points were recorded every 1 ps. Furthermore, Fig. 2.4 shows the cross-sections of Cu NPs at several time points, as noted in Fig. 2.3, where the changes of FCC and HCP structures during sintering are recorded to describe the microstructure evolution. The dislocations and different crystal structures were identified by dislocation analysis (DXA) [49] and common neighbour analysis (CNA) [50].

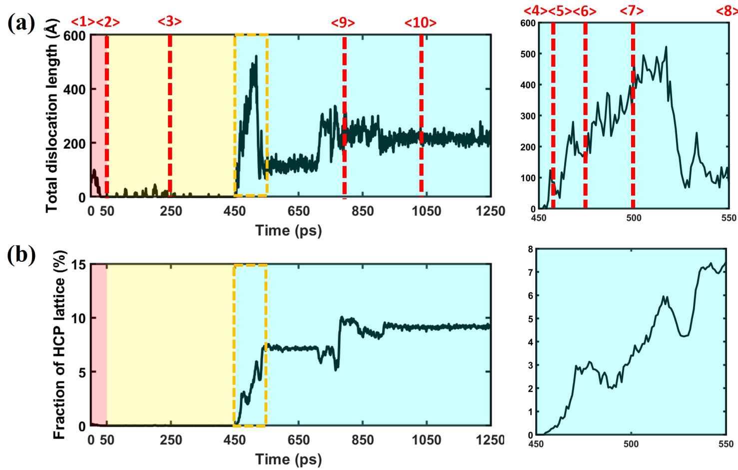


Figure 2.3.: Crystalline response during the pressure-assisted sintering (a) Evolution of total dislocation length (b) Evolution of HCP ratio. The yellow framed areas are zoom-in aside.

Based on the information shown in Fig. 2.3 and 2.4, the entire sintering dynamics can be divided into three periods according to the simulation flow. In the first period, we relax the system at 300 K with constant system energy for 50 ps. Two Cu NPs approach to each other, forming a small neck and causing the reduction of the free surface. To prevent the localized higher energy and temperature at the neck region, the velocities on the translational degrees of the atoms are rescaled every 0.01 ps. Then, atoms are further relaxed for energy minimization, forming minor dislocations and HCP crystalline structure. However, with the neck growth, the dislocation and atoms in HCP are gradually vanished, as plotted from 0 to 50 ps in Fig. 2.3. At 50 ps, a stable structure with neck size, $R = 2.54$ nm, is obtained at the end of the first period, as state <2> shown in Fig. 2.4, in which the FCC lattice is the dominating lattice structure, and no grain boundaries are found at the neck region.

In the second period, the system is heated to 500 K within 200 ps and kept at 500 K for another 200 ps. As the atomic energy increases with the temperature rising, atoms at the neck region rearrange themselves via recrystallization as state <3> at 250 ps shown in Fig. 2.4(a). However, according to Fig. 2.3, the variations of dislocation and HCP ratio are minor at this stage. Besides, atomic structure transformation from FCC to the

amorphous near surface is observed, as the cross-sections of state <3> and <4> shown in Fig. 2.4(a). These results indicate that Cu NPs sintering at low temperature mainly via surface diffusion, which results in a slow and slight coalescence.

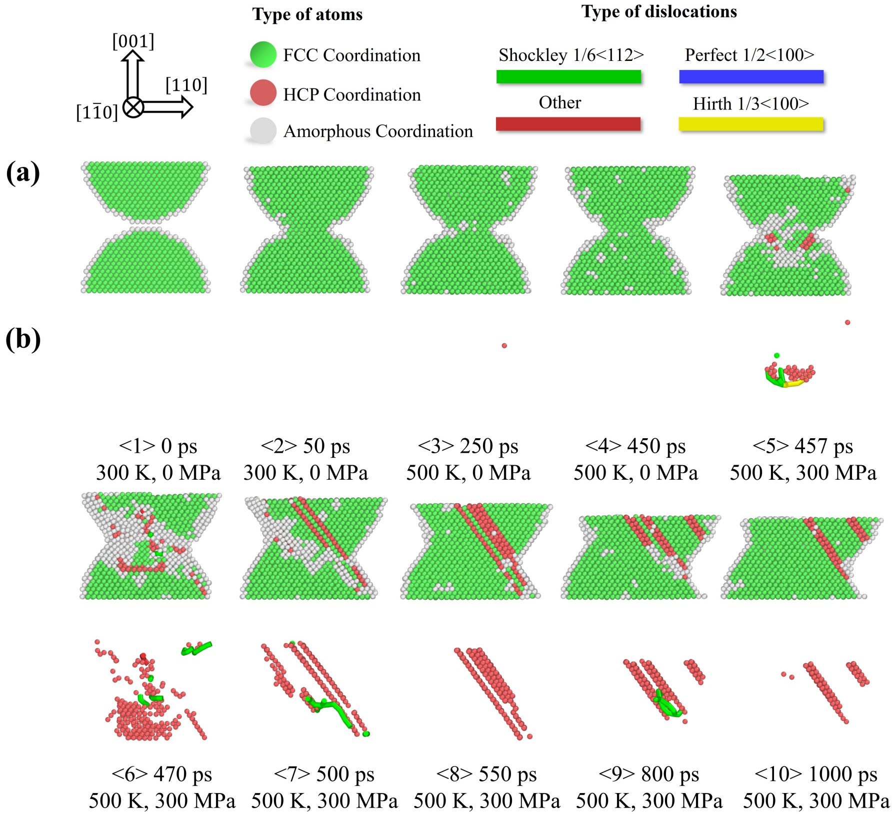


Figure 2.4.: Snapshots of the cross-section (a) Entire lattice structures (b) HCP lattice structure and dislocations. <1>-<10> are the time points marked in Fig. 2.3.

At the final period, as soon as the 300 MPa pressure is applied at 450 ps, intensive atom arrangements at the neck region start. In a short time, extensive FCC atoms transfer to HCP or amorphous atoms, accompanied by the nucleation of dislocation and formation of stacking faults, as illustrated in state <5> to <8> in Fig. 2.4. Meanwhile, the neck size dramatically increases from 2.59 nm to 4.79 nm. Corresponding to such intensive geometry changes, the dislocation length and HCP ratio also experience a rapid increase, as the curves plotted in Fig. 2.3 from 450 ps to 550 ps. These results indicate that in the post-pressure period, the surface diffusion mechanism loses its dominant role in sintering. Instead, other mechanisms, such as plastic deformation involving dislocation motion and atomic diffusion along grain boundary contribute to the coalescence of Cu NPs. At 750 ps, a slip along {111} planes occurs, which is responsible for the increases of total dislocation length and HCP lattice ratio in Fig. 2.3. State <9> shown in Fig. 2.4,

as a transition state, confirms this slip by the appearance of Shockley dislocation tangle between two twinning boundaries. During this period, the extensive activated slip systems promote the atom immigration between NPs, resulting in larger neck size. After 900 ps, the growth of neck size and evolution of microstructure gradually slow down as the increased energy induced by pressure is almost released via plastic deformation and mass migration. The slight variation of total dislocation length implies the end of plastic deformation. Finally, twinning boundaries, crossing two hemispherical NPs, are formed as exhibited in state <10>.

2.2.3. THE EFFECT OF PRESSURE ON SINTERING

To further study the effect of pressure on sintering, additional pressure-assisted sintering simulations with three different pressures (0/100/200 MPa) are conducted at 500 K. Evolutions of MSD and neck size are recorded. As plotted in Fig. 2.5(a) and (b), generally, all cases experience three stages after the pressure is applied on the indentor at 450 ps. Firstly, a dramatic increase in MSD and neck size takes place within a few picoseconds. After that, the coalescence of Cu NPs continually develops, with the steady increases of MSD and neck size of NPs. Consequently, the structures reach the steady-state, in which the structure applied higher pressure shows a better coalescence result. In the case of 300 MPa sintering pressure, it can be seen that the significant increase in Fig. 2.5 from 700 ps correspond to the dislocation behaviour and lattice transformation shown in Fig. 2.3. It implies that the dislocation-induced atom rearrangement plays a key role in the coalescence.

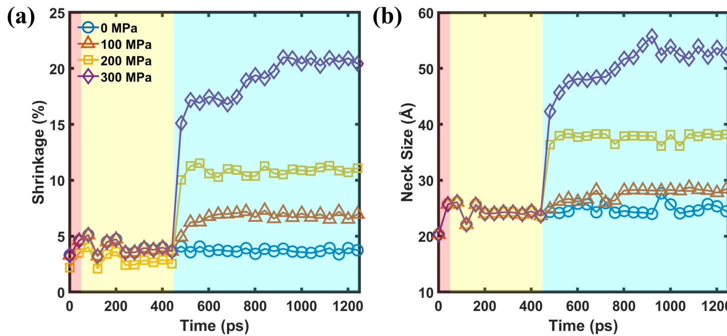


Figure 2.5.: Dimensional evolutions during press-assisted sintering at 500 K under different pressures (a) MSD (b) Neck size

To understand the mechanism behind the changing trend induced by pressure, the displacement vectors of Cu NPs sintered under 100 MPa and 300 MPa are plotted in Fig. 2.6(a) and (b), respectively. The length and direction of the arrow represent the relative distance and the direction of the atom travelled in the past 10 ps. According to Fig. 2.6(a), the motion of atoms at 462 ps shows that atoms at the upper Cu NPs move downward, and the atoms at bottom vibrate around the original sites. It confirms that the inter-diffusion between the two NPs contributes the quick neck growth. At 500 ps, the

motion of atoms becomes weak, leaving the slight atomic diffusion at surface and neck region. However, for the Cu NPs sintering under 300 MPa pressure, a much more extensive atomic motion is observed, as shown in Fig. 2.6(b). At 462 ps, atoms at upper NP intensively move downward in the neck region via surface diffusion and volume diffusion. Meanwhile, some atoms at the centre of neck flow to the surface. As a result, an abrupt increase of MSD and neck size is obtained, as the purple line plotted in Fig. 2.5. At 500 ps, although the rapid motion of atoms is significantly reduced, atoms around {111} slip planes are still migrating, continually contributing to the coalescence of Cu NPs. This atomic migration trend is corresponding to the further increasing stage of the purple line in Fig. 2.5. Finally, Cu NPs under 300 MPa pressure reach the steady-state with a more pronounced coalescence degree, compared to that under 100 MPa pressure.

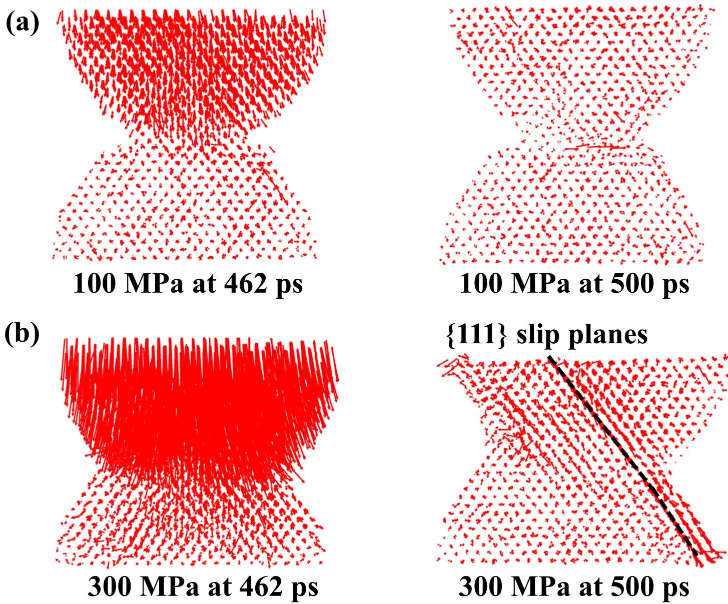


Figure 2.6.: Displacement vectors of the atoms in the pressure-assisted sintering process under different pressures of (a) 100 MPa; (b) 300 MPa

The difference of atomic motion under 100 MPa and 300 MPa shows that a larger external pressure enables a more intensive plastic flow via inter-migration between Cu NPs, resulting in a faster and stronger necking process. That is the reason why a more abrupt increase in neck size is obtained for the case with a higher pressure. Besides, pressure also affects the defects generation during Cu NPs sintering. As shown in Fig. 2.4 and Fig. 2.6(b), extensive defects are created by 300 MPa pressure. As defects play a role as a fast pathway for atomic diffusion, a profound sintering result with large MSD and neck size can be reached thanks to more defects generated during the coalescence. Above comparison shows that the effect of pressure on sintering can be found in two aspects: (1) It induces the plastic deformation during Cu NPs and enhances the atomic diffusion

at both surface and volume. (2) Once the applied pressure is large enough, it creates defects and stimulates the microstructure evolutions, increasing the dislocation density, which will, in turn, promote mass transport. As atoms easily move along the high-density dislocations and grain boundaries with low energy, a successful sintered Cu NPs can be obtained even at a low temperature (< 573 K). This is consistent with many experimental works [51–53].

2.2.4. THE EFFECT OF TEMPERATURE ON SINTERING

In pressure-assisted sintering simulation, temperature takes effect on two parts: (1) the independent effect of temperature on sintering in the 2nd step, (2) the coupled effect with pressure on sintering in the 3rd step.

In the 2nd step, with the temperature increases from 300 K to target temperatures, the dimension evolutions of Cu NPs are recorded in Figure 2.7. It can be seen that prior to the pressure is applied, the Cu NPs with different temperatures exhibit slight differences in both MSD and neck size. Also, intensive pulsations of neck size are observed at this step. Similar results were also observed in other MD work, in which no evident energy change or neck size increase was observed when the temperature rose from 300 K to 500 K [54].

However, in the 3rd step, once 300 MPa pressure is applied, the rapid changes of NPs dimensions are observed in all cases with different temperatures, as shown in Fig. 2.7. Afterwards, the coalescence process slows down, both MSD and neck size steady increase before reaching equilibrium. At around 800 ps, the saturated results show that the Cu NPs sintered with higher temperature have the larger MSD and neck size. Comparing to results in the 2nd step, the effect caused by different temperatures with pressure is dramatically amplified. For example, under the pressureless condition, the neck size at 500 K is only 1 % larger than that at 300 K. It implies that temperature plays an additional role in NPs sintering when pressure applied on the system.

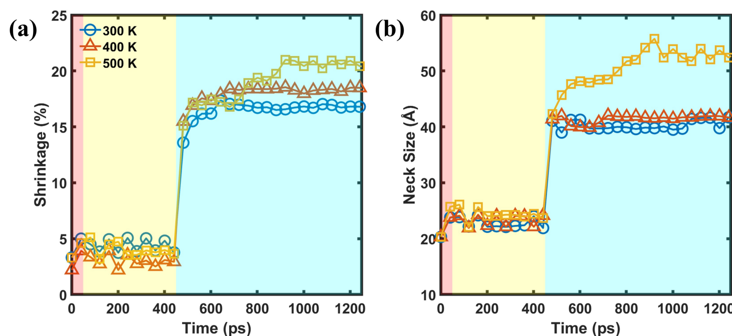


Figure 2.7.: Dimensional evolutions during 300 MPa pressure-assisted sintering at different temperatures (a) MSD (b) Neck size

To explain the temperature-induced effects, in particular, before and after pressure is applied, the atom trajectory of Cu NPs sintered at 300 K and 500 K are plotted in 2.8(a)

and (b), respectively. In general, both simulations at 300 K and 500 K show a similar magnitude of atomic migration. It can be seen that pressure creates extensive defects and atoms actively migrate around those defects. However, if we compare the trajectory of atoms in detail, the effect of temperature can be discovered. For the Cu NPs sintering under pressure-free condition, the atoms at both temperatures only show a minor surface diffusion at the local region. Therefore, the trajectory of the atoms at 300 K is close to that at 500 K. However, when the external pressure is applied at 500 ps, the different performance of atomic migration shows up. At 300 K, the atoms around {111} slip planes, intensively migrate and the atoms at surface flow into the neck area. In contrast, as shown in Fig. 2.8, at 500 K, a more intensive atomic migration on {111} slip planes occurs, around which atoms show a trend to move from upper to neck region and surface. Moreover, the surface diffusion at 500 K also shows much visible than that at 300 K. Thus, those comparisons provide us two important information:

(1) For the structure with low concentrations of defects, as the structure at 110 ps, the elevated temperature only promotes the atomic diffusion at the surface, that takes a limited effect on Cu NPs coalescence. This is the reason why the slight differences of Cu NPs dimensions are obtained in the 2nd step.

(2) However, for the structure with high concentrations of defects, as the atomic migration around defects can be strongly promoted by higher temperature, thus temperature plays a significant role in sintering. Due to more defects are generated by the applied pressure, an amplified effect of temperature in the 3rd step is observed. The higher temperature induces more intensive atomic migration to improve the Cu NPs coalescence.

2.3. ATOMISTIC SIMULATION ON TENSILE TESTS

2.3.1. SIMULATION METHODOLOGY

Based on the two-hemispherical model, to evaluate the mechanical properties of the sintered structure, the simulation of tensile testing at room temperature was conducted to derive the stress-strain curves. First, we removed the pressure applied on indentor and relaxed the entire structure for 500 ps at 300 K in the NVT ensemble, to restore its elastic deformation formed in sintering simulation and obtain an equilibrium state. After that, atoms at the top three layers of the indenter were assigned an upward velocity with a constant strain rate, $7 \times 10^8\ s^{-1}$, and the average stress for entire sintered Cu NPs was calculate by using following formulation [55]:

$$\sigma_{ab} = -\frac{1}{V}[\sum_i m v_a v b + \frac{1}{2}\sum_i \sum_{n=1}^{N_p} (r_{1a}F_{1b} + r_{2a}F_{2b})] \tag{2.2}$$

where the first term is the kinetic energy contribution to the total stress, m is the mass of atom i, a and b take on values x, y, z to generate the different components. The second term represents the virial contribution due to intra and intermolecular interactions. N_p is the neighbour of atom i, r_1 and r_2 are the positions of the 2 atoms in the pairwise

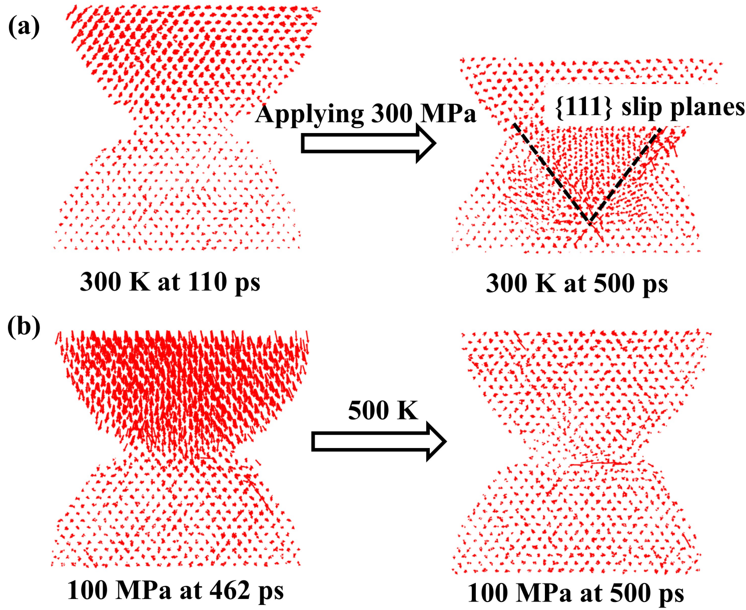


Figure 2.8.: Displacement vectors of the atoms in the pressure-assisted sintering process at different temperatures of (a) 300 K; (b) 500 K

interaction, and F_1 and F_2 are the forces on the 2 atoms resulting from the pairwise interaction. V is the volume of the system to calculate stress, which is equal to the product of atoms number and atomic volume in sintered Cu NPs in the present study. In addition, only a uniaxial tensile loading was applied on structure, thus the zz component was used to derive the stress and the stresses in xx and yy direction were neglected.

2.3.2. TENSILE RESPONSE

The stress-strain curve and evolution of total dislocation length for the Cu NPs sintered at 500 K and 300 MPa are depicted in Fig. 2.9. It can be seen that the sintered Cu NPs can endure the stress of more than 1.9 GPa at the 4.83% yield strain and fractures at 72.85% strain. To better understand the underlying tensile deformation, the cross-sections of the deformed atomic configurations are extracted in Fig. 10. It can be seen that the spikes of stress correspond to the changing trend of the total dislocation length.

Before the yield strain, the tensile stress almost linearly increases to 1.91 GPa, as the extension of sintered Cu NPs commences with the elastic deformation. The small stress releases before the yield are induced by the extinction of the existing defects, which further causes an FCC dominated structure as shown in state <2> in Fig. 2.10. After the yield strain, the stress is abruptly released, accompanied by the obvious increase of total dislocation length. It indicates the structure steps into the stage of plastic deformation. As state <3> shows, twinning boundaries are formed in both Cu NPs and a dislocation tangle is formed near the neck region. From state <3> to state <5>, the neck of Cu NPs continu-

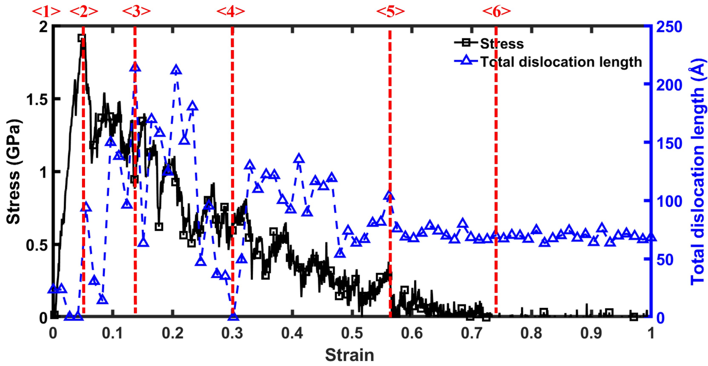


Figure 2.9.: Stress-strain response and evolution of dislocation length during the tensile deformation

ally shrinks with the increasing upper displacement. A serrated evolution of stress was observed. It is because the defects induced by tensile loading actively evolve, from nucleation to propagation to annihilation, causing the instability of microstructures of Cu NPs. Consequently, the tensile stress becomes zero with elongation of $\epsilon = 72.85\%$, and the total dislocation length almost stays unchanged, representing the end of plastic deformation induced by the tensile test. At this moment, the configuration of state <6> shows a tensile fracture with a 45° chisel-edge rupture.

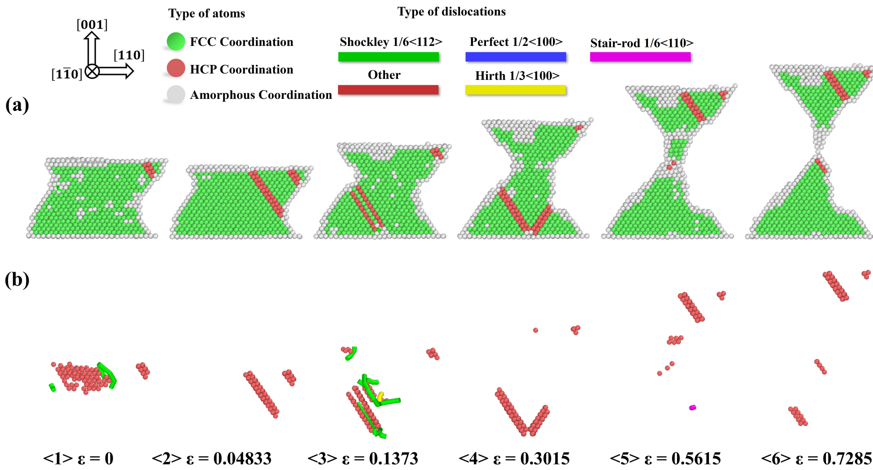


Figure 2.10.: (a) Snapshots of configurations of lattice structures (b) Snapshots of configurations of HCP lattice structure and dislocations

The stress-strain curves for Cu NPs sintered at various temperature and pressure conditions are plotted in Fig. 2.11(a) and (b). After the first yield point, during the plastic deformation, the variation in the curves become severe. It is because that the sintered

structure is complex and the area of cross-section dramatically changes accompanying intensive dislocation activities. It can be seen that under the same sintering temperature, the structure sintered with higher pressure results in higher tensile strength and elastic modulus, as well as larger fracture strain. For example, the tensile stress for the structure pressureless-sintered is 1.04 GPa that is much lower than the 1.91 GPa tensile strength for the structure sintered under 300 MPa. It can be concluded that a profound mechanical behavior of Cu NPs can be obtained by increasing its sintering pressure. For the structures sintered under the same pressure but different temperatures, Fig. 2.11(b) shows that the elevated temperature can also lead to the better mechanical behavior of Cu NPs. But, compared to the effects caused by sintering pressure, the effect of temperature is less significant than the pressure as the increase of tensile strength, from 1.55 GPa to 1.91 GPa, is less than that induced by adding pressure.

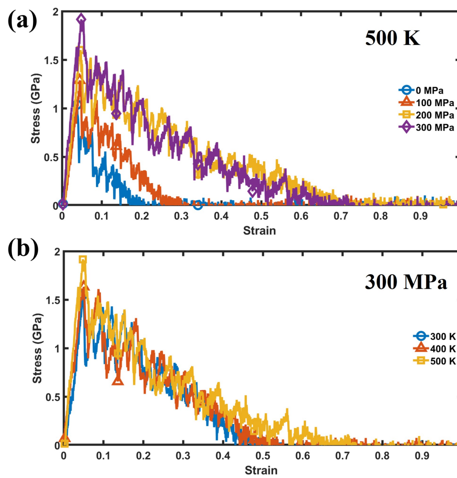


Figure 2.11.: Tensile stress-strain curve of the system sintered at (a) different pressures (b) different temperatures

Additionally, these findings on mechanical behaviours are consistent with our above-mentioned sintering results that the pressure plays a more significant role in Cu NPs coalescence than the role of temperature. As shown in Fig. 2.5, a higher sintering pressure leads to the larger MSD and neck size of Cu NPs, indicating a better degree of Cu NPs coalescence. The similar trend is also obtained for the Cu NPs sintered with different temperatures, as shown in Fig. 2.7. For the results obtained in tensile tests, Fig. 2.12 shows that in general, better elastic modulus and tensile strength are obtained on the structure with a larger neck size. It indicates that better coalesced Cu NPs enable more profound mechanical properties. In a recent experimental study, an increasing tendency of elastic modulus of the sintered Cu NPs with smaller porosity was reported, which means that there exists a positive correlation between the mechanical behavior and the coalescence degree of Cu NPs [56]. The magnitudes of elastic modulus obtained in the experiments vary in the range of $30-80$ GPa that is a qualitative agreement to our simulation results. Therefore, the results obtained in the present study may provide a fundamental explana-

tion of some experimental studies about pressure-assisted NPs sintering. A multiple NPs model, that is closer to reality, will be introduced to the following sections.

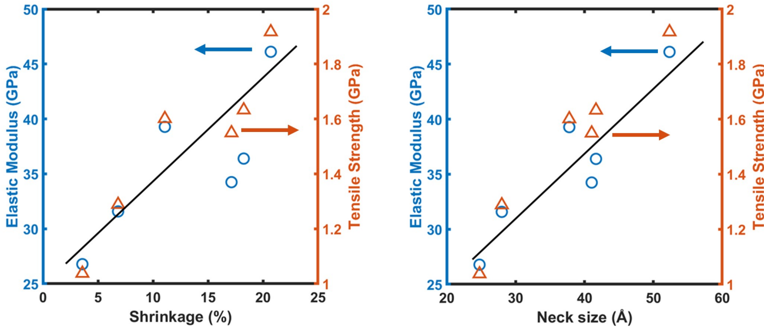


Figure 2.12.: Elastic modulus and tensile strength of the sintered structure with different shrinkage (left) and neck sizes (right)

2

2.4. ATOMISTIC SIMULATION ON NANOINDENTATION TESTS

2.4.1. SIMULATION METHODOLOGY

In this section, two Cu models with different initial packing densities were adopted for sintering and further nanoindentation study, as shown in 2.13. Model A is a sparse model containing 27 spherical Cu nanoparticles with a diameter of 79.112 Å. The inter-particle spacing is 7.192 Å to separate particles. A denser model was built up in model B by inserting a smaller Cu nanoparticle at the body-centered position with a diameter of 53.94 Å. The atom number of the models is 0.63M and 0.84M, respectively.

The nanoindentation process was also simulated by LAMMPS with Adam's classic EAM potential to describe the interaction between Cu atoms [37, 38]. The time step was fixed as 1 fs, and the periodic boundaries was set. At first, the entire system was relaxed to reach its equilibrium state. The models were then sintered in the NPT ensemble at 573 K with 30 MPa applied on the simulation box for 150 ps. Subsequently, the sintered model was kept at 300 K for another 50 ps as a relaxation step. Afterward, Fig. 2.14 shows the implementation of nanoindentation by assigning a virtual spherical indenter, initially placed 20 Å over the top surface, with a constant downward velocity of 10 m/s to the sintered model with 30 Å depth. A spherical indenter exerts a force (F) of magnitude on each atom, as shown in Equation 2.3

$$F(r) = -K(r-R)^2 \tag{2.3}$$

where $K = 10$ eV/ Å^3 is a specified force constant, r is the distance from the atom to the center of the indenter, and R is the radius of the indenter. The force is repulsive and $F(r) = 0$ for $r > R$.

The thermostatic layer was assigned as 300 K in the simulation system using the NVT ensemble. Then the indentation tests were carried out with the NVE ensemble for a 50 ps

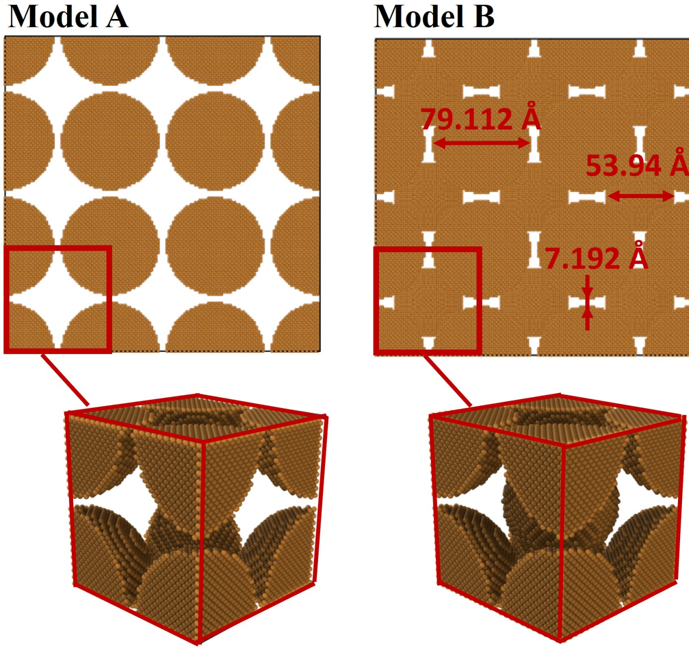


Figure 2.13.: Atomistic models with different initial packing densities

indentation process and another 50 ps withdrawal process. The bottom 10 Å atoms were frozen for fixation, and the other 10 Å atoms above them were defined as thermostatic layers for temperature control. Void-centered and particle-centered positions were selected to investigate the impact of the indentation position on the indentation response, as shown in Fig.2.14.

Additionally, several indenter sizes were chosen to investigate the indenter size's effect on the nanoindentation behavior. As shown in Fig. 2.15, a scale factor η was adopted to control the projection area when the indenter was entirely indented into the sintered Cu NPs. According to the different values of η, the corresponding radius of the indenter was from 4.73 nm to 7.50 nm.

2.4.2. P-h curves

The simulated P-h curves for a complete cycle of the nanoindentation process on void-centered and particle-centered positions are presented in Fig. 2.16. It can be seen that for the void-centered model, the load response took place later than traveling 2 nm since there was no nanoparticle beneath the indenter. The edge of the indenter would achieve the first contact with nanoparticles. In comparison, the particle-centered model responded when the displacement reached 2 nm.

The P-h curves present two stages. At beginning, the force increases steeply until the depth reaches about 0.8 nm, indicating a pure elastic response. The elastic regime al-

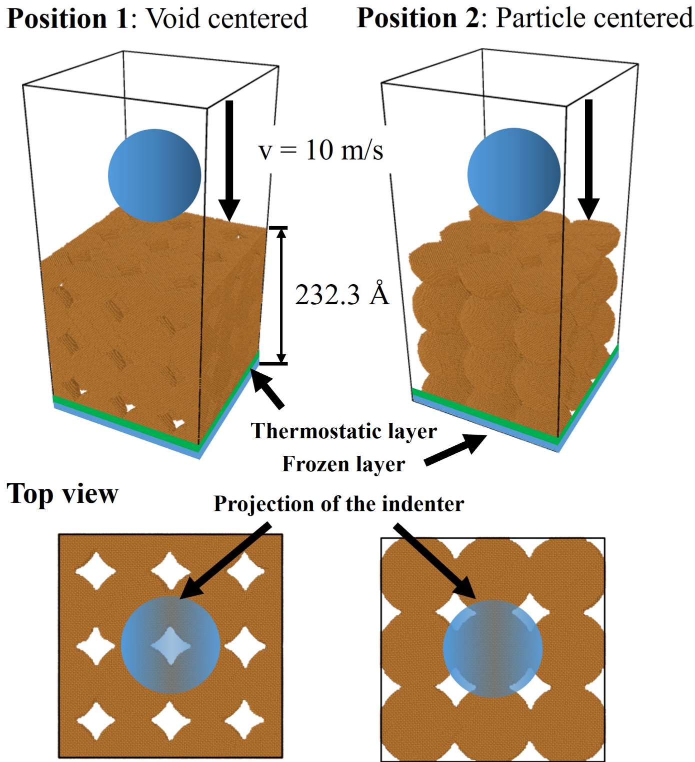
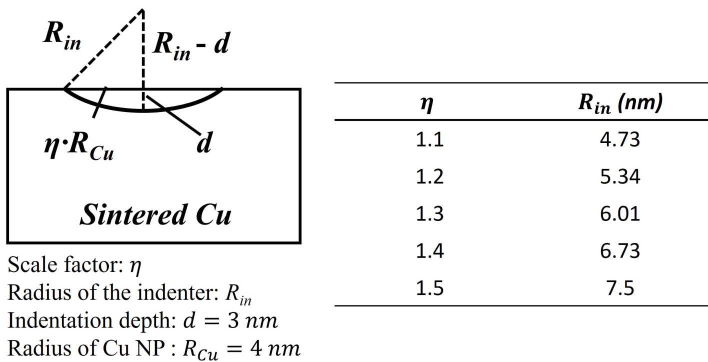


Figure 2.14.: Schematic of nanoindentation simulation with two different positions



η	R_{in} (nm)
1.1	4.73
1.2	5.34
1.3	6.01
1.4	6.73
1.5	7.5

Figure 2.15.: Definition of the different radii of the indenter

most overlaps in the particle-centered position, indicating a close elastic deformation performance. Afterward, a force drop is perceived, suggesting the onset of plastic deformation. The P-h curves fluctuate during the loading stage, which could be attrib-

uted to the plastic rearrangement and work hardening [57]. During the withdrawal process, the load significantly drops, following a decreasing power law fitted by Oliver-Pharr, which presents a similar indentation modulus as calculated by Hertz law.

By comparing the maximum loading force, a larger indenter results in a higher loading force, and the trending is more evident in the nanoindentation in the void-centered position. In the void-centered position, the maximum load increased from 98.9 nN to 157.1 nN. In contrast, the value slight goes up from 140.4 nN to 153.1 nN in the particle-centered position. The relative porosity can be the cause for this difference. In the void-centered position, the indenter projection significantly covers more nanoparticle area on the top surface with the increase of the indenter size.

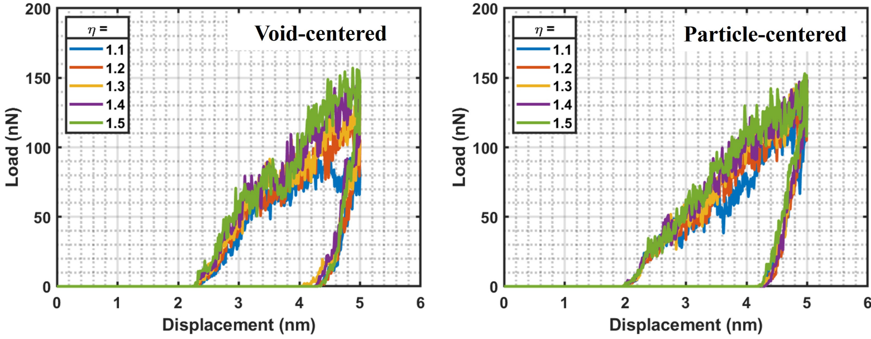


Figure 2.16.: P-h curves of the sintered Model A. (top) Void-centered position; (bottom) Particle-centered position

2.4.3. THE INDENTATION MODULUS AND HARDNESS OF THE SINTERED STRUCTURE

The indentation modulus of the sintered structure can be fitted with the Hertz law (Eq.(2)) in the initial elastic deformation stage.

$$P = \frac{4}{3} E h^{\frac{3}{2}} R^{\frac{1}{2}} \tag{2.4}$$

where P is the applied load by the indenter, R is the indenter radius, h is the indentation depth, and E is the indentation modulus.

Fig. 2.17 depicts the Hertz law fitting in P-h curves obtained from MD simulation with three different indenter sizes, indicating excellent fitting quality. The estimated indentation modulus values are summarized in Table. 2.1. It can be seen that the two models present different trends on the indentation modulus with a larger indenter. In the void-centered model, the maximum indentation module reaches 25.96 GPa with the largest indenter. However, in the particle-centered model, the maximum value happened with the smallest indenter. The relative porosity of the indenter projection on the top surface also causes this result. In the void-centered model, the relative porosity becomes smaller

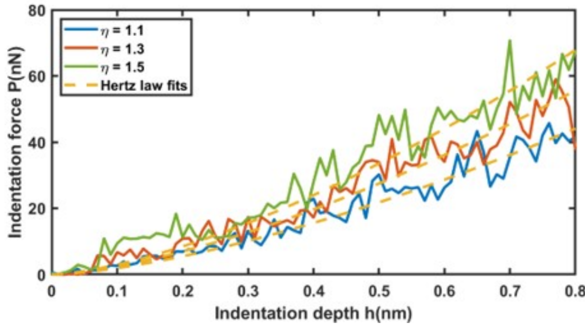


Figure 2.17.: Hertz law fitting (orange dotted lines) in the initial elastic deformation with three different indenter sizes

Table 2.1.: Indentation modulus fitted by Hertz law

η	Void-centered (GPa)	Particle-centered (GPa)
1.1	21.2515	21.6111
1.2	24.3717	20.2260
1.3	23.7687	21.1169
1.4	24.4085	20.4412
1.5	25.9645	18.0340

with a larger indenter; in the particle-centered model, more pores were affected with a larger indenter.

In terms of the nanoindentation simulation on the sintered structure with different initial packing densities, porous model A and denser model B shares density of 5.61 g/cm^3 and 7.414 g/cm^3, as 59.8% ρCu, bulk and 82.7% ρCu, bulk, respectively. The P-h curves are shown in Fig. 2.18 for the indention on the void-centered position. The indenter size is 7.5 nm, and η is 1.5. The blue line, red line and yellow line represent the Model A, void-centered indentation position, Model A, particle-centered indentation position and Model B, void-centered indentation position.

Fitted by the abovementioned Hertz law, Model B shows a larger indentation modulus of 55.01 GPa with a maximum load of around 380 nN. In contrast, the maximum load is less influenced by the different indentation positions as the void-centered curve shows a similar peak to the particle-centered curve value. Compared to the more porous model A, there is no essential difference in the penetration depth when the load reaches zero in the void-centered position, indicating a similar elastic recovery in the sintered structures with different densities. In contrast, the recovered depth is more significant in the particle-centered position.

In this case, due to the porous structure, the loading response shows up after the indenter goes beneath the surface, which makes the geometry-based quantitative analysis of the elastic recovery complicated. Therefore, the analysis employed the energy perspective to study the elastic deformation in the nanoindentation process. The plastic

flow was calculated as the area covered by the P-h hysteresis, and the elastic energy was calculated as the area covered by the P-h curve in the unloading process. Results show that 17.0%, 23.2% and 15.1% of the external work are converted to elastic energy, respectively, in different models and indentation positions. Therefore, the ratio of the external work converted elastic energy is less relevant to the global porosity than the local porosity.

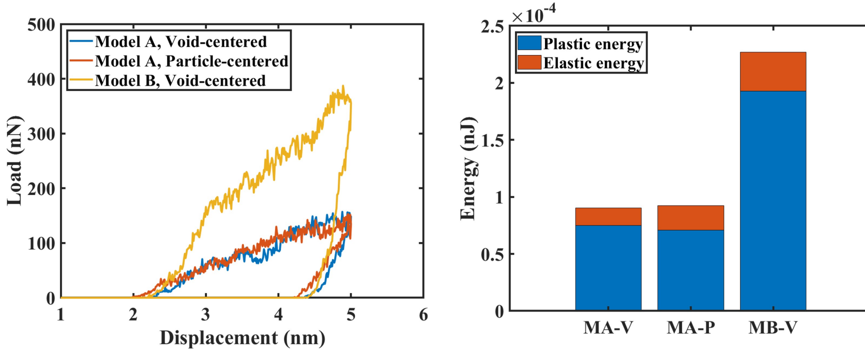


Figure 2.18.: (Left) P-h curves in Model A, void-centered (MA-V) position, Model A, particle-centered (MA-P) position and Model B, void-centered (MB-V) position.; (Right) The corresponding dissipated energy

There have been limited MD studies in the literature on the nanoindentation simulation on the porous sintered metallic materials. Compared to the existing reported nanoindentation experimental values, X. Liu *et al.* achieved an indentation modulus from 72.47 GPa to 103.02 GPa with a Berkovich indenter [58]. However, due to the size limitation in the MD simulation, the local relative porosity in the experiments is much lower than in the simulation. In contrast, X. Long *et al.* measured an indentation modulus of 15 GPa in sintered Ag while its bulk value is 83 GPa [22]. As an alternative test simulation, S. Wang *et al.* also simulated elastic modulus ranging from around 20 GPa to around 70 GPa in the compression simulation, highly depending on the porosity [20]. Thus, our simulated indentation modulus lands in a reasonable range according to other studies.

The hardness H of the sintered structure is defined as the contact pressure when a critical indentation depth has been reached, and the value stays stable with increasing loading. At a macroscopic level, the contact area can be computed according to the evolution of the diameter of the imprint. In contrast, at an atomistic level, the effective contact area is calculated based on the contact atoms with the indenter by considering the sink-in or pile-up phenomena. The atoms in contact can be calculated utilizing two spheres. Figure 2.19 presents the measurement of the contact area by using the following Equation 2.5 [59].

$$A_c = \pi\sigma^2 \sum_{i \in contact} \cos\alpha_i \tag{2.5}$$

Where σ is the atomic radius of the Cu atom at 0.128 nm, and α_i is the angle between the

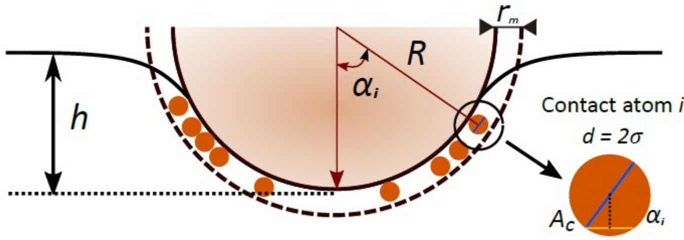


Figure 2.19.: Illustration of calculation of effective contact area in the nanoindentation simulation. R is the radius of the indenter. rm is the lattice constant of Cu as 0.36 nm, and h is the indentation depth.

vector joining the center of the indenting sphere with Cu atom *i*.

The hardness can be calculated from the effective contact area. Figure 8 gives the variation of hardness against the indentation depth. Like the P-h curves, the H values at first increase sharply until a certain depth of 1.25 nm and 0.5 nm in two positions, respectively (blue region). Furthermore, the H values become less affected by the increasing indentation depth (orange region). In the void-centered position, the simulated hardness shows slight dependence on the indenter size, while in the particle-centered position, a larger indenter reversely results in a softer value. The H values are summarized in Table 2.2.

Table 2.2.: Hardness H of the sintered model A

η	Void-centered (GPa)	PParticle-centered (GPa)
1.1	0.62	1.19
1.2	0.63	1.03
1.3	0.56	0.92
1.4	0.56	0.69
1.5	0.53	0.67

Regarding the sintered structure with different densities, Fig. 2.21 depicts the comparison of the projection area and hardness between model A and model B. The projection area in both models stays overlapped at the beginning until the indenter touches the body-positioned nanoparticle. Despite the similar projection area, the hardness rapidly increases in model B due to a more significant loading force in the P-h curves in Fig. 2.18. As a result, the average hardness H in the stable stage is 0.53 GPa and 1.19 GPa for models A and B, respectively. In the experiment, J. Fan *et al.* [23] figured out the indentation hardness of sintered Cu NPs tends to be stable with a loading rate larger than 0.25 mN/s and the reported experimental value is between 1.0 to 1.2 GPa, which is close to the simulated value in model B with a relatively high density.

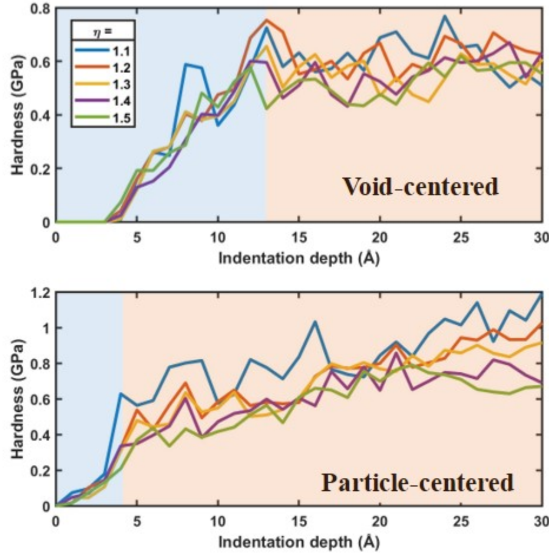


Figure 2.20.: The hardness of the sintered Model A. (top) Void-centered position; (bottom) Particle-centered position.

2.4.4. MICROSTRUCTURE EVOLUTION

Figure 2.22 visualizes the surface morphologies after the loading and unloading with a 7.5 nm-sized virtual indenter. The atoms are colored according to the Z position to visualize the relative distance to the top surface. At the final indentation depth, the indentation on the void-centered in both Model A and Model B presents a square affected zone caused by the plastic deformation enabled along $\{111\} < 110 >$ slip system. It is because the central position beneath the virtual indenter is void. The indentation causes significant shear force at the contacted NP.

On the other hand, the deformation on the particle-centered position is similar to the bulk copper as a round affected area. However, the residual deformation after nanoindentation shows dependency on different model densities, as shown in Fig. 2.23(d)-(f). The elastic recovery of the nanoindentation in Model A is larger than Model B, and the elastic recovery of the particle-centered position is larger than the void-centered position. This result is consistent with the calculated elastic energy and plastic flow in Section 2.4.3. In order to analyze the indentation mechanism in different models as well as different indentation position, the crystal structure evolution of the diagonal cross section is recorded as depicted in Fig. 2.23, in which the green represents face-centered cubic (FCC) atoms, red stands for hexagonal close-packed (HCP) atoms and the amorphous atoms are colored in grey. In the as-sintered atomic model in Model A, limited defects can be found in the necking region as the result of extensive atom rearrangement after the neck growth. However, a mass of stacking faults (SF) crossing the grains are figured out in the as-sintered model B. This is due to the higher sintering degree caused

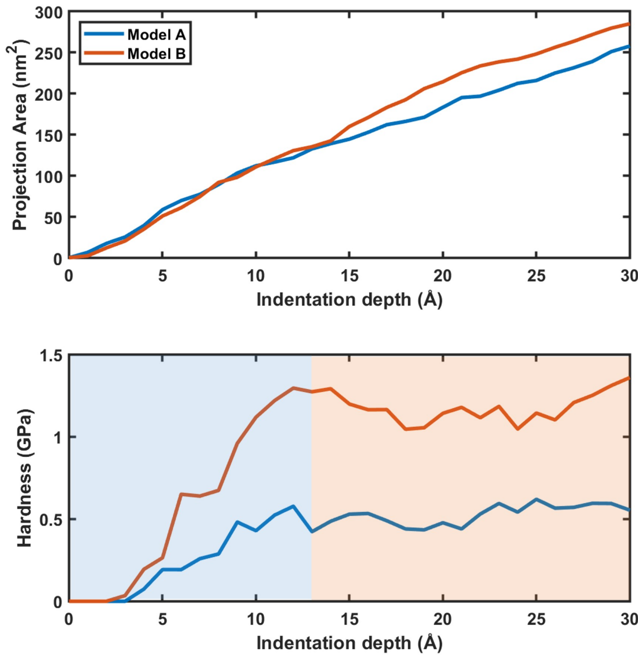


Figure 2.21.: Projection area (top) and hardness (bottom) of model A and model B in a void-centered position with a 7.5 nm sized indenter

by a higher initial packing density, where twinning boundaries (TB) crossing the grain will be formed [60].

With the indenter penetrate deeper into the sintered structure, nanoindentation on all models resemble that of a single crystalline Cu structure, which was deformed by the dislocation movement. Shockley partial dislocations are nucleated in the region beneath the indenter and around the edge of the indenter as pointed by arrows. Afterwards, the Shockley partial dislocations move forward and leave SFs behind them, which is the widely studied dislocation nucleation mechanism [61].

Meanwhile, the subsurface damage layer was increased, as denoted by the amorphous transmission from the FCC structure, which is more evident in Model A. It is attributed to a lower energy barrier that promotes neck growth due to a lower density. After unloading progress, the microstructure undergoes an elastic recovery and atom arrangement in the affected region, leading to a slight decrease in the number of dislocations.

Also, in model A on particle-centered position and model B on void-centered position, dislocation activities on the neighbor particles' necking region were observed in the circles, meaning the sintering degree is further locally promoted. The sintering pressure is generally in the range of MPa, while the contact pressure in the indentation process can reach the range of GPa. The external work done by the indentation is likely to break

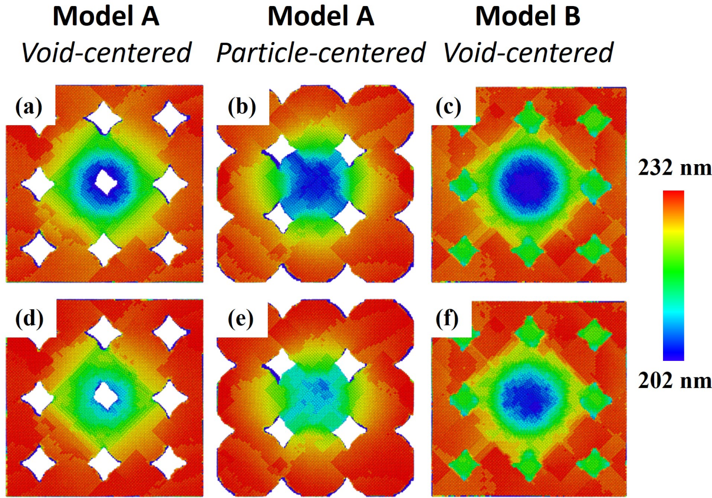


Figure 2.22.: Z-coordinate position (a)-(c) at the final indentation depth and (d)-(f) after the unloading progress

the necking region's dynamic equilibrium and promote neck growth. As observed, in this nanoindentation simulation, the plastic deformation region is not only the directly contacted nanoparticles but also includes their adjacent nanoparticles.

2.5. ReaxFF MD simulation on chemical corrosion

2.5.1. Simulation methodology

In this section, MD simulations of the pressure-assisted sintering of silver nanoparticles and further sulphidation were conducted. The LAMMPS was employed to conduct all the simulations [37]. The atomic configurations in the corrosion simulation were also visualized by OVITO [42].

To simulate the pressure-assisted sintering, the classical EAM potential developed by Foiles *et al.* [62] was applied to describe the interactions between Ag atoms. This EAM potential has been proven to be able to calculate properties, such as the cohesive energy, phase diagram, lattice constant, and elastic constant of silver atoms, accurately. The total energy E_{tot} can be expressed as follows [63]:

$$E_{tot} = \sum_i F_i(\rho_{h,i}) + \frac{1}{2}\sum_i \sum_{j\neq 1} \Phi_{ij}(R_{ij}) \tag{2.6}$$

where $\rho_{h,i}$ is the host electron density of atom i, $F_i(\rho)$ is the energy to embed atom i into the background electron density ρ, and $\Phi_{ij}(R_{ij})$ is the corecore pair repulsion between atoms i and j with a distance of R_{ij}.

However, the EAM is not capable of describing reactive chemistry, such as bond formation and breaking of bonds. The ReaxFF with the Ag/S parameters developed by Saleh

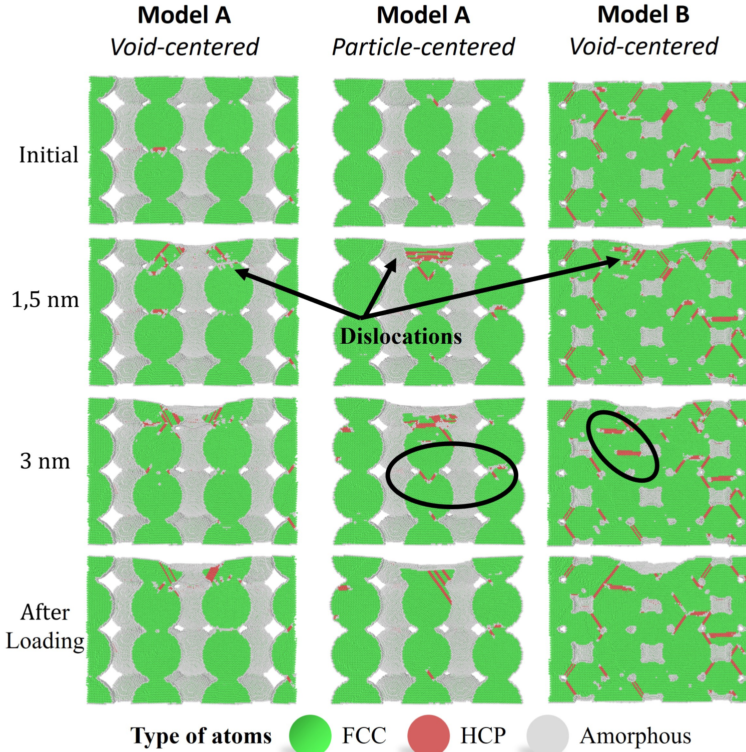


Figure 2.23.: Microstructural evolution according to the different penetration depths of Model A with void-centered indentation position (left column); Model A with particle-centered position (middle column); Model B with void-centered position (right column)

et al. [36] was adopted in this study. This force field has been confirmed to describe the sulphurisation behaviour on an Ag slab surface correctly. The total energy term in the ReaxFF force field can be expressed as follows [64]:

$$E_{system} = E_{bond} + E_{over} + E_{under} + E_{H-bond} + E_{lp} + E_{val} + E_{tors} + E_{vdWaals} + E_{Coulomb}. \tag{2.7}$$

The total energy of the system consisted of bond-order-dependent or covalent interactions and non-bonded interactions. Bond-order-dependent terms include the bond energy (E_{bond}), over coordination (E_{over}), undercoordination (E_{under}), and hydrogen bond interactions ($E_{(H-bond)}$). Energy penalty terms include the torsion angle energy (E_{tors}), valence angle energy (E_{val}), and lone pair energy (E_{lp}), whereas the non-bonded terms are the van der Waals energy ($E_{vdWaals}$) and Coulomb energy ($E_{Coulomb}$).

All the systems simulated in this study adopted periodic boundaries, and the conjugate gradient algorithm was used for energy minimization. To simulate the pressure-

assisted sintering, a symmetric multi-Ag nanoparticle system was established, containing 15,688 atoms in total. The diameter of each Ag nanoparticle was 3.6 nm, and the atomic spacing was set at 3.5 Å. The dimensions of the simulation cell were 80 Å × 80 Å × Å. The system was relaxed using the NVE (microcanonical) ensemble at 300 K for 100 ps. The system was then heated from 300 to 575 K within 500 ps using the NPT (isothermalisobaric) ensemble by controlling the pressure on the simulation box to 30 MPa. To promote the sintering, an extra 1.5 ns dwell period was included, which also used the NPT ensemble at a constant 30 MPa pressure. Eventually, the sintered structure cooled to room temperature (300 K) in another 500 ps. Meanwhile, the pressure on the box was released to atmospheric pressure.

The NVT ensemble was employed to simulate sulphurisation. Temperatures were controlled through the NoseHoover thermostat. The time step was chosen as 0.5 fs, and the damping constant was selected as 100 fs. Two temperatures, 373 and 750 K, were selected to investigate the effect of temperature. At first, atoms were assigned random velocities at the target temperature, with a Gaussian distribution. The system was then kept at the target temperature for 500 ps for further reaction and sulphur diffusion. Trajectories were analysed by the MSD defined in 2.1.

2.5.2. Multi-NP sintered atomic model construction

As the 30 MPa pressure-assisted sintering process occurred, atoms travelled to the necking area between the nanoparticles, and a dense structure was obtained. The initial configuration and the configuration of the sintered system are shown in Fig. 2.24a. The sintering degree was characterized by the evolution of the MSD, as shown in Fig. 2.24b. When pressure was applied, the NPs quickly sintered at 300 K. The MSD then increased as the temperature increased. Consequently, the MSD became stable during the 300-K relaxation process, indicating that a stable sintered microstructure was formed. The density of the sintered microstructure was 5.95 g/cm^3, which was 56.7% of the value of bulk Ag.

In the sulphurisation simulations, to reduce the computational cost, one-fourth of the sintered structure was extracted for further simulation. Meanwhile, a single crystal of Ag with the same dimensions was created. An 80 Å vacuum layer was added on the top and bottom sides, where 150 S_8 molecules were randomly placed. The S_8 molecule was selected here because, according to the experiments, most sulphur vapour molecules were in the form of S_8, and it was previously reported that the aging condition with sulphur vapour is more severe than that with hydrogen sulphide gas [65]. The S_8 molecule was pre-relaxed at 750 K for 50 ps. Every added S_8 molecule maintained a distance of not less than 3 Å with any existing atom. The assembled system shown in Fig. 2.24(c) had a size of 38.7 Å × 38.7 Å × 237.7 Å, containing 4529 and 7189 atoms, respectively, for the model with the sintered Ag and the bulk Ag. Silver and sulphur atoms are coloured silver and orange, respectively.

2.5.3. Sulphidation behaviour and mechanism

The reaction mechanism of sulphide was revealed to be the following. First, sulphur molecules physisorbed on the surface of the silver, where significant charge exchange

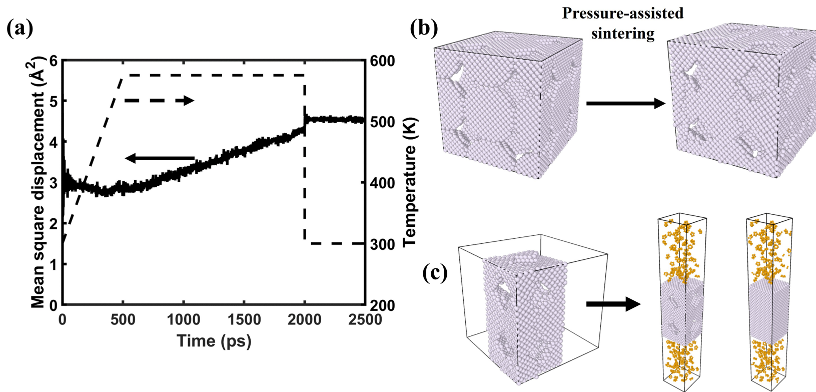


Figure 2.24.: Pressure-assisted sintering: (a) MSD and temperature evolution, (b) atomic configuration evolution, and (c) atomic configuration for sulphidation simulation

did not occur. Next, S_8 dissociation occurred on the surface and resulted in chemisorbed S atoms by reaction with Ag. Then, the thickening of the sulphide layer was not only contributed to by the S atoms diffusing into the Ag layer but surface Ag atoms were also dragged out of their original positions and continuously migrated upwards. As shown in Fig. 2.25, a selected Ag atom was lifted by one atomic layer in a short period. The reaction was confirmed by the change in the atomic charge. The atomic charge rapidly increased from 0.158e to 0.263e in 2.5 ps and then remained stable, indicating an equilibrium state. The resulting vacancy was then filled with S atoms. This result is consistent with previous reports [66, 67]. The formation of surface sulphides is the main reason for the electrical resistance degradation.

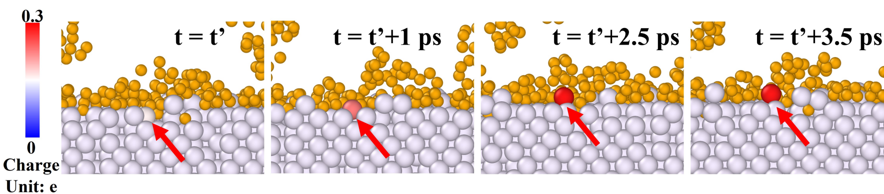


Figure 2.25.: Ag sulphidation mechanism for surface Ag atoms. Only a selected Ag atom is coloured based on its atomic charge

To investigate the influence of porous structures on sulphur corrosion, models with different microstructures were simulated at 750 K for 500 ps. The atomistic configuration after sulphurisation, as well as the evolution of the sulphide layer thickness, is shown in Fig. 2.26a. Silver sulphidation occurred at the surface, and the sulphide layer was formed by the diffusion as well as the upward migration of silver atoms. Eventually, a thicker sulphide layer was found in the model with sintered Ag after 500 ps. The thickness of the sulphide layer was defined as the distance between the lowest and topmost silver atoms

along the z-axis.

At the end of the simulation, the thicknesses of the sulphide layer in the model with sintered Ag and the model with single-crystal Ag were 25.3 and 11.2 Å, respectively, as shown in Fig. 2.26b. The steady increase rate had a minor difference between the two models. This was because the diffusivity of sulphur in silver was based on the intrinsic properties of the material, which was independent of the porous structure.

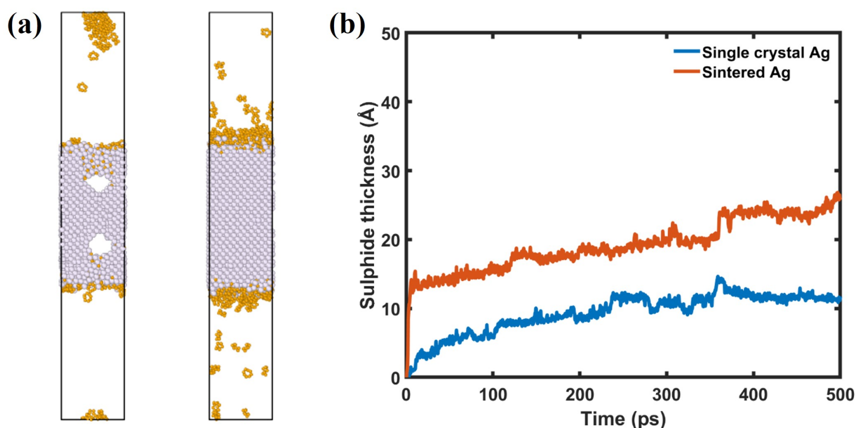


Figure 2.26.: Formation of silver sulphide layer in sintered structure and single crystal structure: (a) atomistic configuration after 500 ps (left: sintered structure, right: single crystal structure) and (b) evolution of sulphide layer thickness

The greater sulphidation corrosion in the sintered Ag was attributed to two factors. When the simulation began, a non-uniform sulphide layer abruptly formed. This was confirmed by the cross section snapshots shown in Fig. 2.27. A sulphur molecule (coloured red) quickly diffused into the pore within 3 ps. It then climbed around on the inner surface for a short time and then adsorbed on the surface. Meanwhile, the sulphidation on the surface was ongoing. Consequently, it reacted with the Ag atoms in the pore, as dissociation of the S_8 molecule was observed.

In addition, in the model with sintered Ag, sulphurisation lasted longer, while in the model with single-crystal Ag, the thickness of the sulphide layer became stable after 370 ps. This was because the porous structure had more reaction sites than the defect-free structure. The sulphidation corrosion was an electrochemical reaction with electron exchange between silver and sulphur atoms. Thus, the degree of sulphidation could be described by the evolution of the total charge of the sulphur atoms, as shown in Fig. 2.28a. According to the slope of the charge evolution, the model with sintered Ag exhibited more electrochemical activity. As a result, after the 500 ps simulation, the model with single-crystal Ag lost 135.1e worth of charge, while this number was more than double in the model with sintered Ag (295.6e). This result was consistent with the abovementioned difference in thickness. Furthermore, the distribution of silver and sulphur atoms along the x-axis after the simulation is shown in Fig. 2.28b. In the model with single-crystal Ag, the distribution of sulphur and silver atoms shared the same trend. The area with fewer

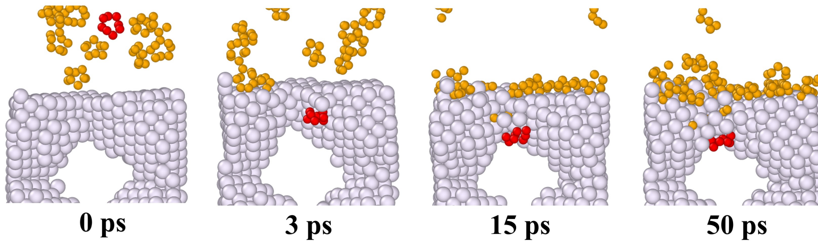


Figure 2.27.: Snapshots for the fast formation of sulphide layer at the beginning of the simulation (cross section)

atoms was contributed to by the sulphidation process, wherein the silver continuously diffused into the sulphide layer [66]. However, in the model with sintered Ag, due to the existence of pores, fewer Ag atoms were present in the middle area. In contrast, S atoms were better distributed in this area, indicating the accumulation of S atoms in the pores. Thus, the sintered Ag showed more significant sulphidation corrosion due to the greater number of reaction sites created by the pores.

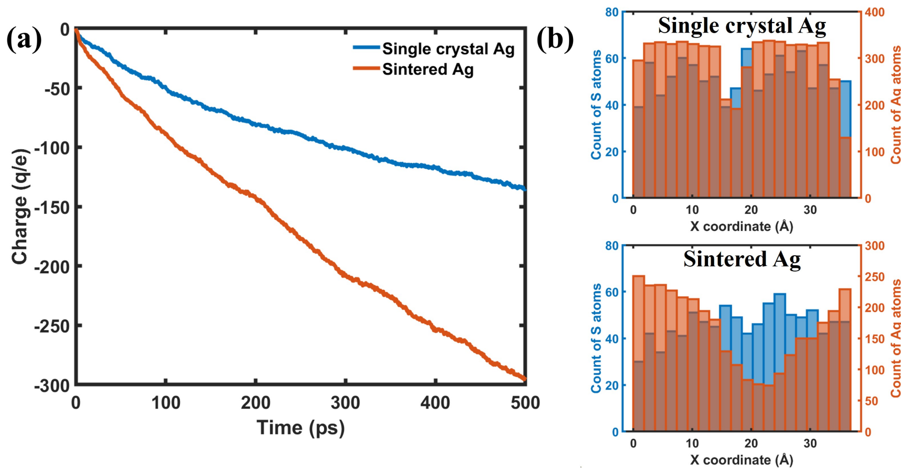


Figure 2.28.: Sulphidation process: (a) evolution of total charge of Ag atoms and (b) atom position along the X-axis

Furthermore, the effect of temperature on the sulphidation was also investigated. For the model with sintered Ag, another sulphidation simulation at 373 K (100 $^\circ C$) was conducted. The post-sulphidation atomistic configuration and the evolution of the sulphide layer thickness are shown in Fig. 2.29a.

A large number of S_8 molecules accumulated on the outer surface of the sintered silver awaiting further reaction. As a result, the final sulphide layer thickness at 373 K was 14.2,

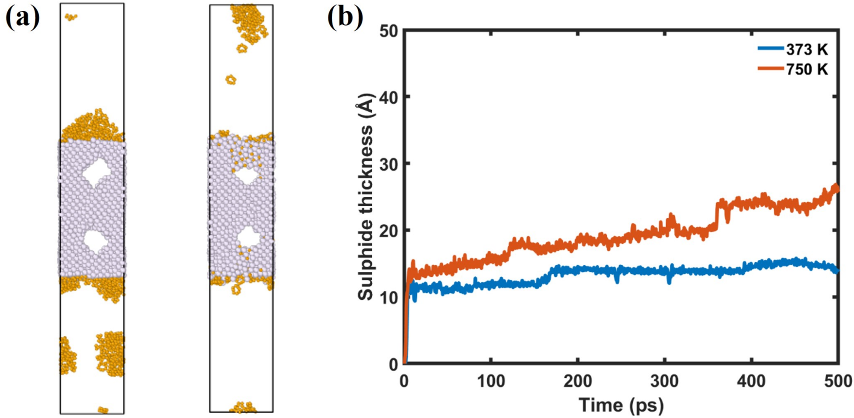


Figure 2.29.: Formation of silver sulphide layer in structure sintered at 373 K and 750 K: (a) atomistic configuration after 500 ps (left: 373 K, right: 750 K) and (b) evolution of sulphide layer thickness

while this number was 25.3 at 750 K. In Fig. 2.29b, a rapid increase at the beginning of the simulation was found at both temperatures. However, the sulphidation rate at 373 K was slower than that at 750 K. In the case of 373 K, the growth of sulphide layer formed several plateaus during the sulphidation. This explains the non-uniformity of the sulphide layer. The evolution of the charge difference showed that the total charge transfer at 373 K was 12.99e, which was 1/22 the value at 750 K, which is shown in Fig.2.30a. This indicated that less sulphidation occurred at 373 K, and the reaction rate was much slower. To directly view the distribution of S atoms, the atomic coordinates along the Z-axis are shown in Fig. 2.30b. In the histogram of the Ag atoms, the lower bars indicate the positions of the pores. At 373 K, the overlapping region between the S and Ag atoms mainly existed at the edge. Thus, it was confirmed that the S_8 molecule that diffused into the pore did not diffuse further, and at this moment, most of the sulphide formed at the outer surface. In contrast, at 750 K, there were more overlapping bars, which meant that more sulphide formed as well as diffused S atoms in Ag body. Therefore, it was concluded that higher temperature could extensively accelerate the growth of the sulphide layer, resulting in greater sulphidation corrosion.

In summary, the sulphidation corrosion on silver depended on the microstructure as well as the sulphidation temperature. The sintered Ag was prone to sulphidation corrosion due to its porous structure. Sulphur molecules can transport into the sintered Ag body through pores and react on the inner surface. Besides, high sulphidation temperature extensively promotes the sulphidation rate. The practical applications of power electronics packaging, such as in electrical vehicles and the power grid, are usually at high operating temperatures. Thus, sulphidation corrosion is an important factor that should be considered during package design.

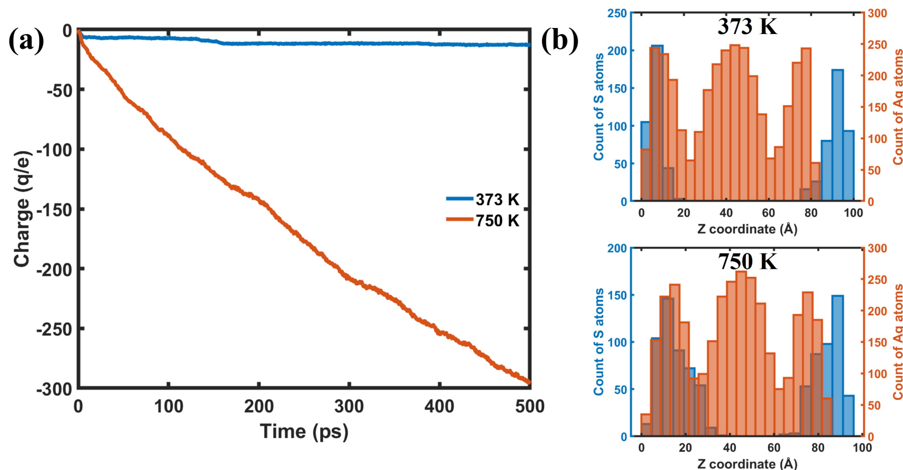


Figure 2.30.: Formation of silver sulphide layer: (a) atomistic configuration after 500 ps and (b) evolution of sulphide layer thickness

2.6. CONCLUSION

In this chapter, various atomistic simulations were demonstrated as a powerful tool to understand the sintering process and how sintered structures mechanically and chemically perform.

A two-hemispherical NP model was first constructed to reveal the influence of sintering temperature (300 − 500 K) and pressure (0 − 300 MPa) on the sintering process. The pressure was found to be a more dominant mechanism in sintering more coalesced NPs than the temperature. By applying pressure to the Cu NPs, the transition of the dominant coalescence kinetics could change from slight surface diffusion to intensive volume diffusion and plastic flow driven by the defects. The impact brought by temperature sintering is primarily on promoting atomic diffusion activities. Besides, from the further tensile simulation, the sintering pressure and temperature dependencies were also observed in the mechanical properties, such as the elastic modulus of the sintered Cu NPs.

Scaling up from a two-hemispherical NP model, multi-NP models revealed the response against mechanical loading and a corrosive environment.

The atomistic nanoindentation simulation was successfully implemented on the simulated porous structure with different initial packing densities and different loading conditions. The indentation mechanism of the plastic deformation was revealed as the dislocation nucleated in the region beneath and around the edges of the indenter. The indentation modulus in the particle-centered position decreased and reached a minimum indentation modulus of 18.03 GPa. Besides, the hardness in the void-centered position stayed relatively stable, while the value in the particle-centered position went down when the indenter size increased. The maximum hardness was obtained with a 4.73 nm indenter in a particle-centered position as 1.19 GPa.

Furthermore, the porous sintered structure with higher density resulted in better performance, as 55.01 GPa in indentation modulus and 1.19 GPa in hardness, which were

within the reasonable range as reported in other simulations and mechanical tests on porous sintered structures. It also revealed that the elastic recovery indicated that the local indentation position is more essential than the structure density.

Regarding chemical corrosion simulation on a multi-NP model, ReaxFF was employed to examine the sulphidation corrosion. The sulphidation mechanism was revealed to be the upward migration of surface silver atoms to the sulphur-rich layer and sulphur atom diffusion into the silver body. Furthermore, the porous structure suffered more severe sulphidation due to a large inner surface area. The pore slightly affected the sulphidation rate, whereas the aging temperature was a dominant factor.

By bridging pre-sinter status to the sintered structure and further linking to mechanical and chemical performance, the comprehensive MD simulation in this chapter provides a complete storyline from the materials preparation phase to the application phase. This work can shorten the time of materials and process optimization. Additionally, the estimated mechanical and chemical behavior has the potential to be further scaled up and enrich a higher level modeling, which can rapidly promote the application of nanoparticles sintering technology in heterogeneous integration.

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MULTI-SCALE MECHANICAL BEHAVIOUR OF THE SINTERED NANOPARTICLES

Cu nanoparticle sintering technology has attracted considerable attention as a promising candidate for the die-attach interconnect in power electronics packaging. The mechanical behavior characterization of the sintered layer at a macro and microscale will deepen the understanding of the mechanical behaviors and improve the modeling of materials. In this study, 4 μm*-wide micro-cantilevers with different notch depths were microfabricated in a sintered interconnect layer. Furthermore, continuous dynamical testing on the microcantilevers revealed an elastic-plastic fracture on the porous sintered structure. The microscopic fracture toughness of different notched specimens was obtained from J-integral according to elastic-plastic fracture mechanics. Specimens with deeper notches presented higher resistance to the crack extension, while a geometry factor between* 0.20 *and* 0.37 *showed a relatively stable microscopic fracture toughness. Additionally, the tensile deformation behaviors of sintered nanoCu paste were firstly characterized by high temperature tensile tests performed at various temperatures and strain rates ranging from* 180 °*C to* 360 °*C,* 1×10^{-4} s^{-1} *to* 1×10^{-3} s^{-1} *respectively. It was found that the elastic modulus and tensile strength decreased at the higher tensile temperature while the ductility increased accordingly. The highest elastic modulus and tensile strength results were* 12.15 *GPa and* 46.97 *MPa, respectively. Second, failure analysis was conducted based on the fracture surface after tensile testing. Recrystallization was revealed as the main factor for ductility improvement. Subsequently, an Anand model was fitted by stress-strain curves to describe the tensile constitutive behavior of the sintered nanoCu paste.*

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3.1. INTRODUCTION

THE intensive development of the materials composition and process optimization, understanding the mechanical properties of the sintered structure is essential for design for reliability (DfR), where an accurate material model is needed as a key input to predict the failure of the entire system. The porous die-attach layer manufactured by sintering technology presents different mechanical properties and deformation behavior from the bulk metal, depending on the post-sintering residual porosity. Typical, the mechanical performance of the sintered joint is characterized at the macroscopic scale by employing shearing and bending tests [3–5]. However, these are not rigorous measurement methods to obtain local fracture toughness and improve understanding of the fracture behavior in the sintered layer. Fracture toughness is a crucial parameter for assessing fracture failure by describing the ability of materials containing a pre-existing notch to resist crack propagation. From an experimental perspective, Wang *et al.* studied the interfacial fracture toughness of sintered hybrid silver interconnect using modified compact tension experiments, revealing that the pore size and porosity significantly influenced the fracture resistance [6]. Zhao *et al.* employed an end notch flexure (ENF) test to determine sintered Ag's mode II shearing fracture toughness considering various sintering temperatures and holding time [7]. Based on the developed ENF method, Dai *et al.* further parameterized mode II cohesive zone models in the sintered Ag joint with additive carbon nanotube [8].

In addition, it has been extensively demonstrated that the mechanical properties at a macro-scale can differ dramatically from the microscopic properties due to the size effect [9]. Considering the practical dimension of a die-attach layer of around 10 μm in thickness, plenty of features remain to be explored, and fracture toughness (K_{IC}) at the microscale is one of them. Recently, the FIB enabled micro-cantilever (MC) bending test has been reported as a helpful tool to evaluate the mode I fracture toughness at the microscale [10]. Furthermore, Wurster *et al.* [11] improved the understanding of fracture experiments using notched MC and proposed a general measurement methodology at the microscale using J-integral and crack tip opening displacement (CTOD). At present, the MC bending test has been utilized in the die-attach interconnect, including AgSn solder [10], CuSn solder [12], sintered Ag microparticles [13], and sintered Cu nanoparticles [14]. Regarding the sintering technology, a ductile fracture was revealed, accompanied by local necking at the crack tip. However, the effect of the test condition, e.g., notch depth, on the fracture toughness is underexplored, while a reliable estimation of mechanical failure at the microscale is essential.

In addition to realize the fracture behavoir, a material model at a higher scale is also needed. Typically, a general power-law model is adequate to describe the deformation and predicted load-displacement behavior of sintered joints [15, 16]. Some studies have considered the temperature dependency of mechanical and thermal properties of sintered Ag joints for cyclic thermal conditions [15, 17–19]. In theory, the mechanical properties of the die attachment are able to provide the necessary characteristics to optimize packaging design and the RUL estimation [20–22]. Constitutive models of sintered Ag have been reported according to different loading conditions, such as tensile and nanoindentation [23, 24]. Compared with the sintered nanoAg joint, there is still a lack of mechanical constitutive models related to the sintered nanoCu joint, especially under high temperat-

ures. The limited understanding of its viscoplastic behavior significantly influences the accuracy of models. At the same time, the sintered Cu joint has shown good mechanical and electrical properties and good reliability in thermal cycle tests [25–28]. Thus, a systemic study on the mechanical properties of sintered nanoCu paste at high temperatures is required to promote its application in high-power electronics packaging. Therefore, it is also essential to characterize the mechanical properties of sintered nano Cu paste at high temperatures and to further reveal its constitutive behaviors.

In the present chapter, the fracture toughness of the pressure-sintered Cu joints with a continuous porous network was investigated in MC samples at the microscale (Section 3.2). MCs were micro-fabricated by a FIB perpendicular to the loading direction with different notch depths as 0%, 20%, 37%, and 50% of the MCs thickness. The effect of the notch depths on the fracture toughness and crack propagation behavior was investigated by bending tests at the microscale. Consequently, the J-integral versus crack extension ($J - \Delta a$) curve behavior was measured to provide insights into modeling the sintered Cu joint.

Besides the micro-cantilever bending experiments at a micro-scale, we performed tensile tests of sintered nanoCu paste at different temperatures and strain rates (Section 3.3). Four temperature levels (180 °C, 240 °C, 300 °C, and 360 °C) and three strain rates (1×10^{-4} s^{-1}, 5×10^{-4} s^{-1}, and 1×10^{-3} s^{-1}) were used during the tensile tests. Failure analysis was conducted at three locations along the tensile direction to investigate the deformation mechanism. Subsequently, the tensile stress-strain curves were used to fit the parameters of the Anand model [29], describing the constitutive behavior of the sintered nanoCu paste. The results of this chapter revealed the high-temperature tensile properties of sintered nanoCu paste in a power electronics application and also proposed both constitutive and parameterized models, which is vital for virtual reliability assessment for high-power electronics packaging.

3.2. MICROSCOPIC MECHANICAL PERFORMANCE OF THE SINTERED NANOPARTICLES

3.2.1. EXPERIMENTAL METHODOLOGIES

This subsection uses a self-made nano Cu paste with the process flow reported in [1]. The paste contained quasi-spherical Cu nanoparticles with an average diameter of 100 ± 36 nm. The fabrication process of the sintered sample is illustrated in Fig. 3.1. At first, the self-made Cu paste was dispensed into a steel mold with a 5 mm × 5 mm opening using a metal squeegee. Afterward, the paste and the mold were dried in an oven at 120 °C for 15 mins. This step helped evaporate the organic solvent in the paste composition, reducing the risk of air bubble generation during the sintering process. To mimic the actual operation conditions, the dried paste was sintered at 250 °C for 10 mins with a rapid heating rate of 50 °C/min. Constant uniaxial pressure of 20 MPa was maintained to promote the sintering within a constant N_2 atmosphere to prevent oxidation. The sintered cubic specimen presented a 5 mm × 5 mm dimension and approximately 1 mm thickness.

As shown in Figure 3.2, the micro-cantilevers were microfabricated on the sintered

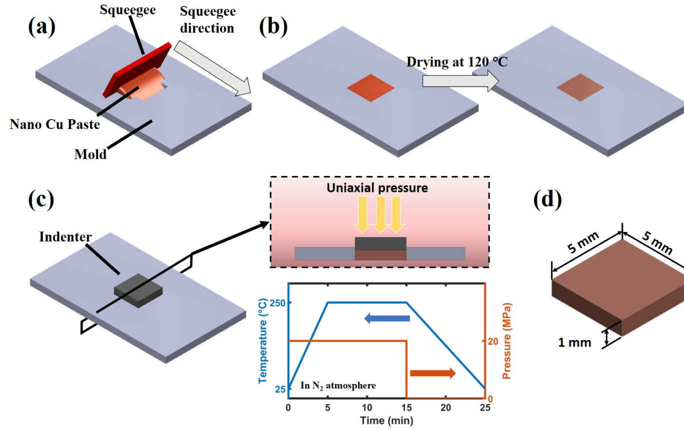

Figure 3.1.: Pressure-assisted sintering process for sample fabrication: (a) paste dispersion, (b) as-dispensed paste, (c) dried paste, (d) pressure-assisted sintering and (e) specimen dimension.

specimen using a dual-beam scanning electron microscope (SEM)/FIB microscope (FEI Helios G4Cx) with an accelerating voltage of 30 kV. The position of the MCs was chosen at the sintered specimen edge, which simplified the pre- and post-test microstructure characterization. At first, a cleaning cut was applied to remove defects on the edge. Afterward, coarse milling with an ion current ranging from 21 nA down to 2.5 nA was applied to shape the cantilevers quickly. However, due to the local heat brought by the large ion current, the near-surface was fused. In order to remove the fused surface, the cantilevers subsequently experienced fine milling with a small ion current at pAs. During the coarse milling and fine milling, the specimen has to be taken out and placed again with 90° rotation. Thus, all faces of the cantilever were well polished by FIB. The notches were cut at last with a 24 pA ion current, reducing the width of the notch. The dimensions of the MC are outlined in Table 3.1. It should be noticed that a certain amount of reliable error (approx. 0.02 μm) is included in the dimension measurement when identifying the edge of the cantilever. The geometric dimensions of the MC are indicated in Fig. 3.2, where a, L, L_{eff}, W, and B denoted notch depth, cantilever length to tip, effective crack-to-tip length, cantilever width, and cantilever height, respectively. In this study, while one specimen remained unnotched, for the others, the notch was cut on the top surface of the cantilever to result in four different a/W ratios: 0, 0.2, 0.37, and 0.5 of the cantilever height. Additionally, a high aspect ratio of 3.5 was designed for cantilever fabrication. Therefore, a linear elastic bending theory can be adopted. Three MCs were prepared per condition.

Subsequently, the fabricated MCs were loaded in a dual beam FIB/SEM workstation (Leo 1540XB, Carl Zeiss AG, Oberkochen, Germany) using a Hysitron picoindenter PI85 (Bruker Corporation, Billerica, USA) with a nanoDMA III upgrade for continuous stiffness measurement. All specimens were manually aligned and tested using a wedge-shaped conductive diamond tip indenter (Synton-MDP, Nidau, Switzerland). A constant

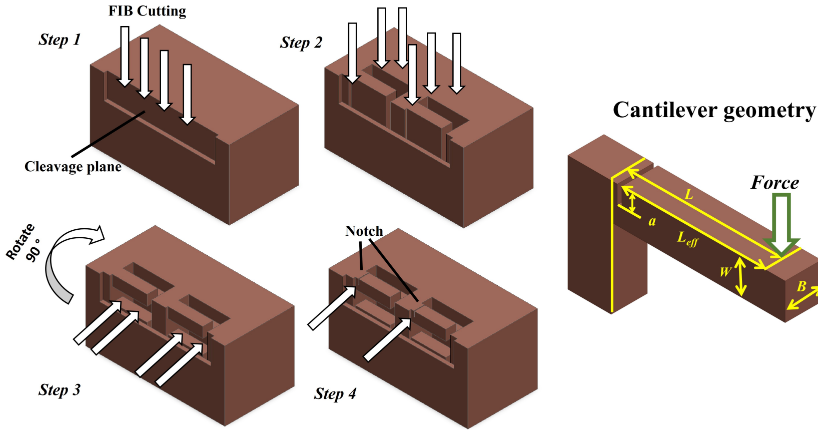

Figure 3.2.: FIB cutting process and dimensional notation. Notch depth a, cantilever length to tip L, effective crack-to-tip length L_{eff}, cantilever width W, and cantilever height B, as given in Table 3.1, are indicated. The position of the application of force is pointed.

loading rate of 10 μN/s and a constant superimposed sinusoidal 80 Hz signal with amplitude of 5 μN for continuous stiffness measurements were chosen for all specimens. The force and indenter displacement, as well as continuous in-situ SEM micrographs, were recorded for data post-processing during the bending test.

Table 3.1.: The dimensions of MC beams measured from SEM

$Specimen$	α/W	α [μm]	L [μm]	L_{eff} [μm]	W [μm]	B [μm]
aW0-01	/	/	13.39	/	3.85	4.13
aW0-02	/	/	13.95	/	4.03	4.22
aW0-03	/	/	13.66	/	3.98	4.10
aW20-01	0.21	0.87	13.00	12.01	4.17	4.31
aW20-02	0.20	0.78	14.13	13.03	3.93	4.31
aW20-03	0.19	0.77	14.13	13.07	4.06	4.39
aW37-01	0.37	1.39	14.08	13.1	3.77	4.18
aW37-02	0.36	1.40	13.97	13.07	3.86	4.22
aW37-03	0.37	1.43	14.16	12.97	3.91	4.5
aW50-01	0.50	1.75	13.40	12.2	3.5	3.94
aW50-02	0.52	1.82	12.53	11.47	3.48	4.96
aW50-03	0.50	1.86	13.49	12.41	3.70	4.33

3.2.2. FRACTURE MECHANICS METHODOLOGIES

The stress intensity factor is a function of applied stress, component geometry, and crack length. Failure or fracture is inevitable when the stress intensity factor exceeds the frac-

ture toughness regarding the Griffith and Irwin fracture criterion [30]. In terms of evaluating the J-integral according to the elastic-plastic fracture mechanics, the following iterative method described in ASTM 1820 was applied [31]. Despite ATSM 1820 is not valid in its full extent for microscopic specimens, it is generally accepted in the community as the closest analogy to valid macroscopic testing, where non-linear elastic phenomena are present.

$$J(a) = J^{el}(a) + J^{pl}(a) \tag{3.1}$$

$$J_n^{el} = \frac{K_{q,n}^2(1-v^2)}{E} \tag{3.2}$$

$$J_n^{pl} = \{J_{n-1}^{pl} + \frac{\eta_n}{W-a_n}\frac{A_n^{pl}-A_{n-1}^{pl}}{B}\}\{1-\gamma_n\frac{a_n-a_{n-1}}{W-a_n}\} \tag{3.3}$$

where $J^{el}(a)$ and $J^{pl}(a)$ are the elastic and plastic J-integral values at specific crack lengths a and n denotes the number of iteration steps. The respective crack lengths were calculated from the dynamic compliance signal based on an analytic solution as outlined in [32, 33].

$$\int_0^a \frac{a}{W} f(\frac{a}{W})^2 da = \frac{(k_0/k-1)L}{18\pi(1-v^2)r^2} \tag{3.4}$$

where a is the crack length, W and L are geometric parameters, k and k_0 are the stiffness of the cracked and unnotched beam respectively, v is Poissons ratio and $f(a/W)$ is a geometry factor that for the given cantilever geometry [34], as

$$f(\frac{a}{w}) = \sqrt{\frac{2w}{\pi a}\tan(\frac{\pi a}{2w})}\frac{0.923+0.199(1-\sin\frac{\pi a}{2w})^4}{\cos(\frac{\pi a}{2w})} \tag{3.5}$$

Subsequently, the stress intensity factor K_q was calculated as [34]

$$K_{q,n} = \frac{6F_nL_{eff}}{BW^2}\sqrt{\pi a_n}f(\frac{a_n}{w}) \tag{3.6}$$

Here B, W, a, and L_{eff} are geometric dimensions defined in Fig. 3.2 and F is the load.

The plastic part of the J-integral was calculated using recommended geometry independent prefactors $\eta = 1.9$ and $\gamma = 0.9$ in ASTM 1820 [31].It should be noticed that the value of η and γ can be slightly affected by the a/W ratio, while in this study, a constant value was assumed for simplification [35]. A^{pl} is the plastic work computed from load-displacement curves as Eq.3.7 [36].

$$A_n^{pl} = \int_0^{u_n} F du - \frac{F_n^2}{2k_n} \tag{3.7}$$

where u_n, F_n and k_n are the respective displacements, load, and stiffness. The dynamic stiffness k was calculated as the inverse of the dynamic compliance $k = c^{-1}$.

3.2.3. MICRO-CANTILEVER BENDING TEST RESULTS

Figure 3.3 depicts the microstructure after sintering. A typical nanoporous sintered structure is present, with developed inter-particle connections and occasional twin boundaries crossing entire grains. The line intercept technique was employed to evaluate the average grain size, calculated as 0.24 $\pm$ 0.04μm by randomly drawing lines and not accounting the pores. In addition, to estimate the porosity of the sintered structure while eliminating the error within single 2D images, a 3D sampling was carried out by slicing the specimens with 50 nm spacing, as depicted in Fig. 3.3(b). From this sequential data, a Gaussian filter was applied to improve the image contrast. The phase segmentation of the sintered Cu and the pores was implemented based on a thresholding method, as shown in Fig. 3.3(c). Consequently, a 3D model was reconstructed and rendered in the commercial software AVIZO [37]. The absolute porosity was then defined by the ratio of the total pore volume to that of the volume of interest (VOI). The average absolute porosity of the sintered structure is 8.25 $\pm$ 0.69 %.

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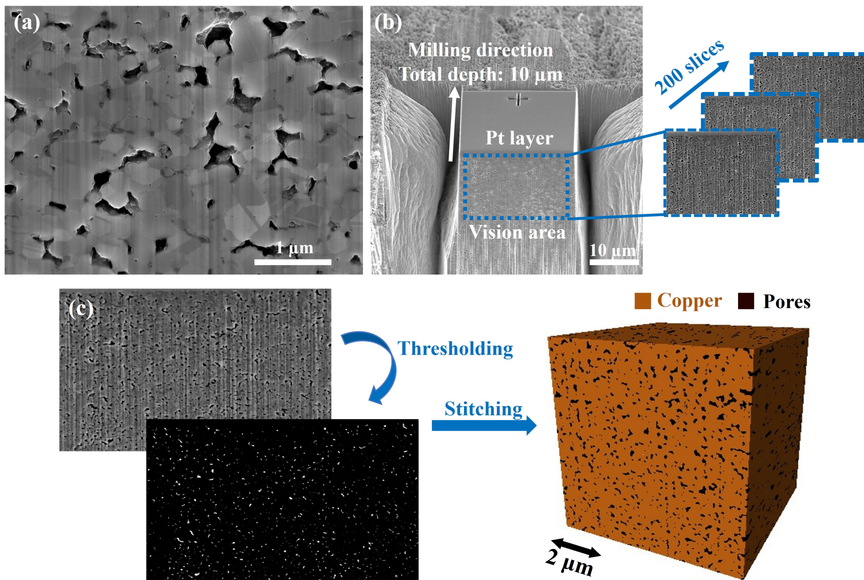

Figure 3.3.: (a) Micrograph of the sintered structure, depicting pores and individual grains. (b) FIB slicing for porosity calculation. (c) Rendered binary 3D VOI with copper and pore phase by means of a thresholding method.

Figure 3.4(a)-(d) depicts the MC beams with different a/W ratios before the bending test. It can be seen that the side view of the MC beams is rectangular, and the notches are parallel to the loading direction. The crack propagation of MC beams with a/W of 0.2 before and after the bending test is presented in Fig. 3.4(e)-(g) as an example. Before the bending (Fig. 3.4(e)), the crack is parallel to the direction of the application of force. As the bending test continued, after significant crack tip blunting (Fig. 3.4(f)), the fracture occurred at the notch position, and no bending evidence was found in the

front part of the MC beams (Fig. 3.4(g)). Furthermore, no pronounced dislocation slip deformation-induced surface steps were observed during bending, indicating a possible difference from conventional grained Cu [38]. After bending, the notch tip became more blunted than the original geometry, and the crack propagated into the cantilever body with tearing features.

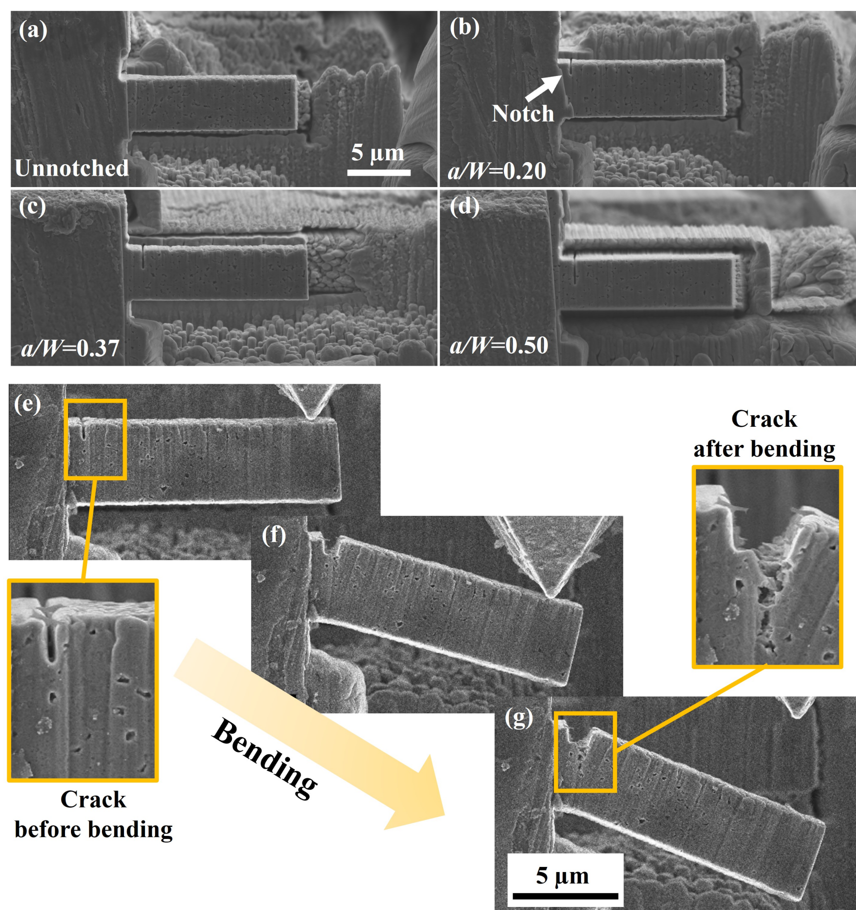

Figure 3.4.: SEM images of sintered Cu NP cantilever with different a/W ratios (a) $a/W = 0$; (b) $a/W = 0.20$; (c) $a/W = 0.37$; (d) $a/W = 0.50$; An example of crack propagation in the specimen with $a/W = 0.20$. (e) before bending; (f) notch blunting during bending; (g) after bending.

The fracture surface was analyzed in more detail to identify the fracture mechanism, as shown in Fig. 3.5(a)-(d), whereby dashed yellow frames indicate the pre-crack area. Typical continuous porous networks with highly sintered structures can be found on all fracture surfaces. Furthermore, Fig. 3.5(e)(f) magnifies the framed area in the fracture surface with *a/W* ratio of 0.37 and 0.5, respectively. The fracture surfaces present similar

fracture morphology reported in the previous tensile and shearing studies, indicating ductile fracture in the MC bending tests [1, 39].

Different fracture features are presented at the fracture surface. At first, multiple local ductile necking tips can be found on elongated Cu grains at the fracture surface, as pointed in Fig. 3.5(f). This implies that individual Cu struts deformed completely plastically until a detachment of two necked sharp tips occurred, which is consistent with previous molecular dynamics simulation results [40]. Furthermore, in Fig. 3.5(e), a tearing ridge of dimples with relatively flat edges can also be noticed at the fracture surface, which is caused by the formation of nanograins within the dimple ridge region.

Not all Cu grains showed plastic fracture features. There are also regions where grains detach without apparent plastic necking phenomenon, as pointed out in Fig. 3.5(f). This can be attributed to the grain boundary sliding in a multi-particle sintered region during deformation [41, 42]. In addition, it is also found that some regions seem not to show any evidence of plasticity, suggesting that these were regions around the previous pores.

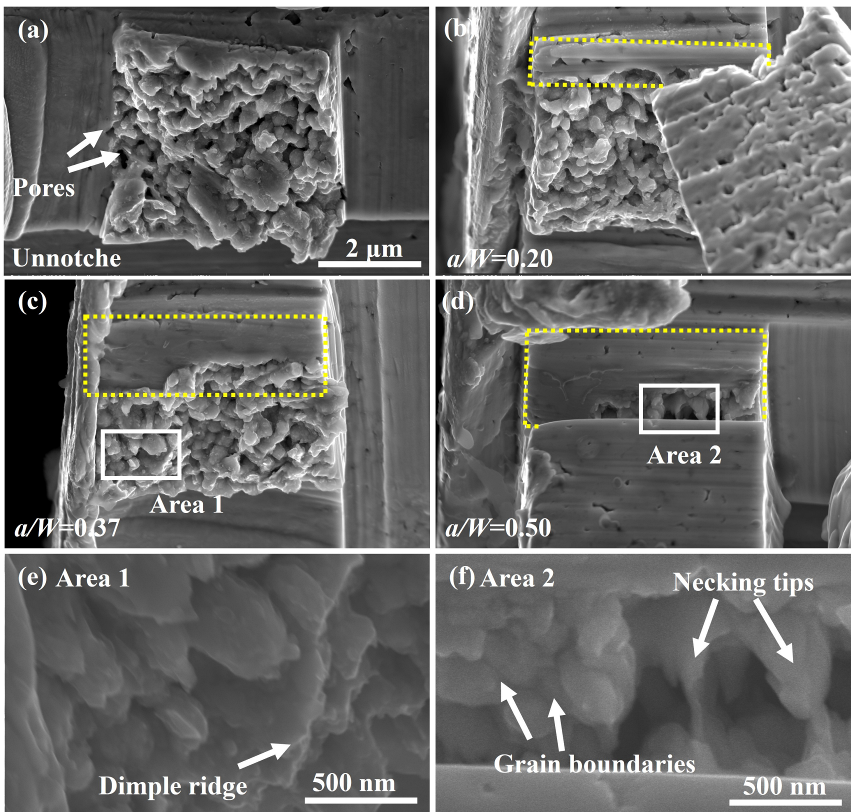

Figure 3.5.: SEM images of the initial FIB notch area (yellow box) and fracture surface of (a) Unnotched (b) $a/W = 0.20$ (c) $a/W = 0.37$ (d) $a/W = 0.50$ as well as high magnification images of (e) Area 1 and (f) Area 2 framed in (c) and (d), respectively.

The inhomogeneous sintered structure is likely to be the reason behind the hybrid evidence of local plastic deformation. Therefore, the dominant fracture mechanism in this material is best described as continuous pore coalescence upon pure plastic deformation of individual Cu struts, independent of the *a/W* ratios.

3.2.4. FRACTURE TOUGHNESS ANALYSIS

Figure 3.6(a) presents the load-displacement curves for the unnotched MCs, $aW0-01$, $aW0-02$, and $aW0-03$. An evident yield stage, followed by a decreasing load regime, was observed before failure, indicating a prominent elastic-plastic behavior. This is consistent with the microstructure observation on the fracture surface. Therefore, standard linear elastic fracture mechanics (LEFM) does not apply for the evaluation of fracture toughness K_{IC}, and the more intricate J-integral approach, as described in the experimental section, must be utilized.

The maximum bending stress [34] and strain [43] on the outermost bending fiber of MC is given by linear-elastic bending theory

$$\sigma = 6\frac{FL}{BW^2} \tag{3.8}$$

$$\varepsilon = \frac{3Wu}{2BW^2} \tag{3.9}$$

with F as the load force, L, B, and W as geometry dimensions defined in Fig. 3.1, and u as the displacement.

The maximum engineering stress-strain curves of the three unnotched MCs are plotted in Fig. 3.6(b). A highly reproducible linear elastic initial loading was observed in all specimens. The elastic modulus was calculated from the linear region as 41.42 ± 1.62 GPa. The yield strength was evaluated by plotting the linear fit line with an offset of $\varepsilon = 0.002$. In doing so, a yield strength of 970 ± 22 MPa was extracted for the sintered structure.

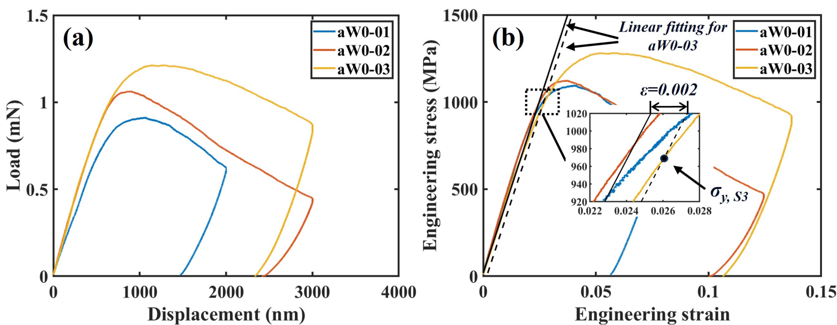

Figure 3.6.: (a) Load-displacement curves and (b) stress-strain curves of unnotched specimens.

Representative load-displacement results for four different notched MCs are shown in Fig. 3.7(a), respectively. The initial slope of each curve also depicts a linear elastic regime,

followed by evident plastic yielding and a constant flow plateau or slight decrease due to crack extension. The initial slope difference is a result of the difference in initial notch lengths and, therefore, a deviation in the bending ligament. Furthermore, the crack resistance $J-\Delta a$ curves for different a/W ratios, as calculated using Eq. 3.3-3.7, are shown in Fig. 3.7(b). Three $J-\Delta a$ curves were presented for each a/W ratio. Figure 3.7(c), taking $aW20-02$ specimen as an example, illustrates the translation from the $J-\Delta a$ curve to the K_Q.

For the conditional critical J-value evaluation, according to ASTM 1820 [31], a blunting line should be drawn with an offset of 200 μm, which is impossible in this study with micromachined MCs. A analogous 2% W construction was proposed by Pippan et al. [44] and utilized in various publications [45–47]. While it is not a perfect equivalent of the ASTM E1820, it captures the fact that geometric crack tip blunting due to plastic deformation. This criterion or similar ones in conjunction with quasi-continuous $J-\Delta a$ curve measurements have shown agreement in comparison with macroscopic data, where such data exists [36, 48]. Therefore, an offset of 2% W was chosen in this study. Segments between 50 − 200 J/m^2 were used to fit the slope of the blunting line because of excellent linearity. J_Q was therefore determined as the intersection of the $J-\Delta a$ curve and the offset blunting line. The conditional toughness K-value was subsequently calculated using the standard plane stress condition estimate as Eq. 3.10

$$K_J = \sqrt{JE} \tag{3.10}$$

where E is the elastic modulus of the sintered Cu. This study adopted $E = 41.42$ GPa as calculated from the unnotched specimens.

With the known K-value, the plastic zone at the crack tip for plane stress can be determined according to Irwins model [49, 50]

$$R_p = \frac{1}{2\pi}(\frac{K_I}{R_e})^2 \tag{3.11}$$

where R_p is the diameter of the plastic zone, which is assumed as circular, K_I is the stress intensity factor in mode I fracture, Re is the yield strength of 970 ± 22 MPa as calculated above.

The conditional fracture toughness shows a very shallow increasing trend for longer notch lengths, with values ranging from 3.6 ± 0.1 MPa·m$^{1/2}$ for $a/W = 0.2$, to 3.2 ± 0.3 $MPa \cdot m^{1/2}$ for $a/W = 0.37$ and 4.3 ± 0.1 MPa·m$^{1/2}$ for $a/W = 0.50$, respectively. In macroscopic specimens, it is generally observed that deeply cracked specimens result in lower $J-\Delta a$ curves because the plastic zone is becoming more constrained [51]. However, an increase in $J-\Delta a$ behavior has also been observed in macroscopic specimens, where it has been attributed mostly to the loss of plane strain condition [52]. Furthermore, toughness increase with increasing notch depth was also reported for similarly scaled W specimen [45], with the stress state and the plastic zone constraint as explanation. However, the good agreement between $a/W = 0.2$ and $a/W = 0.37$ suggests that the change in stress state for lower a/W ratios is not as pronounced as for higher a/W ratios.

To determine the influence of the a/W on the fracture toughness, the relationship between the plastic zone and the remaining length of the ligament must be clarified.

Irwins standard plastic zone size estimation is only a rough approximation. Depending on the local microstructure in front of the crack tip, specifically the arrangement of pores, plastic yielding might be constrained to single struts and not take over the full volume in the crack tip vicinity. While this is not a completely precise description in such heterogeneous systems, it is a useful estimation to assess which fracture mechanics framework (linear-elastic fracture mechanics, elastic plastic fracture mechanics, general yielding) would be appropriate to utilize.

According to Eq. 3.11, the size of the plastic zone when the K-value reached $K_{Q,J}$ was calculated as 2.14 ± 0.12 μm, 1.74 ± 0.29 μm and 3.1 ± 0.14 μm for $a/W = 0.2$, 0.37 and 0.5, respectively. Compared to the crack extension calculated in Fig. 3.7(b), it indicates that in the case of $a/W = 0.5$, the entire ligament experienced plastic deformation as the crack rapidly propagated, resulting in an unstable fracture. This showcases that amount of plastic deformation cannot be ignored and application of purely linear-elastic fracture mechanics, will not be able to yield valid results. For linear-elastic fracture mechanics to hold the plastic zone size should not be larger than roughly 1/25 of the smallest relevant length a, b, B (in analogy to ASTM E399, where the validity criterion would be $a, W-a, B > 2.5 \times (K_I/R_e)^2$) [53]. Hence, the validity criterion to apply liner-elastic fracture mechanics in this case is approximately 60 nm. Even if the microstructural constraint would reduce the plastic zone size by some margin, a reduction from 2 μm to below 60 nm is not likely. Thus, the plastic zone size estimation should be considered as a classification criterion that indeed elastic-plastic fracture mechanical considerations describe the actual fracture characteristics closer than simplified linear elastic fracture mechanics.

The abovementioned results conclude that the fracture initiation and crack growth in these specimens are governed mainly by the local microstructural characteristics (porosity, grain size, grain cohesion). The fracture characteristics are irrelevant to the notch depth. Besides, as the plastic zone is within the ligament length, there is a minor difference between the specimens with $a/W = 0.20$ and 0.37, giving a conditional fracture toughness $K_{Q,J}$ ranging from 3.2 to 3.6 MPa·m$^{1/2}$.

Microscopic fracture toughness has rarely been reported for pure Cu. For example, in high-pressure torsion deformed ultra-fine-grained Cu, a value of 33.4 MPa·m$^{1/2}$ was reported, and the initiation toughness decreased according to the refined grain size [54]. However, this high value is hardly applicable in the power electronics die-attachment application, where the bondline thickness is mostly a few tens of micrometers. Regarding the related specimen size effect, Hirakata *et al.* reported a fracture toughness of 7.81 ± 1.22 MPa·m$^{1/2}$ for freestanding 800 nm thickness polycrystalline Cu film [55]. However, unlike the film with a large two-dimensional scale, in the sintered MC, the size effect-induced high-yield stress restrains the plastic deformation in the localized plastic zone, resulting in much lower fracture toughness.

Besides the effect of specimen size on the fracture toughness, porosity also significantly affects the fracture toughness. Well-known classical cell models, e.g., Ashby's [56] and Yang's [57], have been widely used to correlate porosity and fracture toughness. It has been demonstrated that the model I fracture toughness better satisfied Ashby's model in the case of sintering Ag as given below [6, 8, 58].

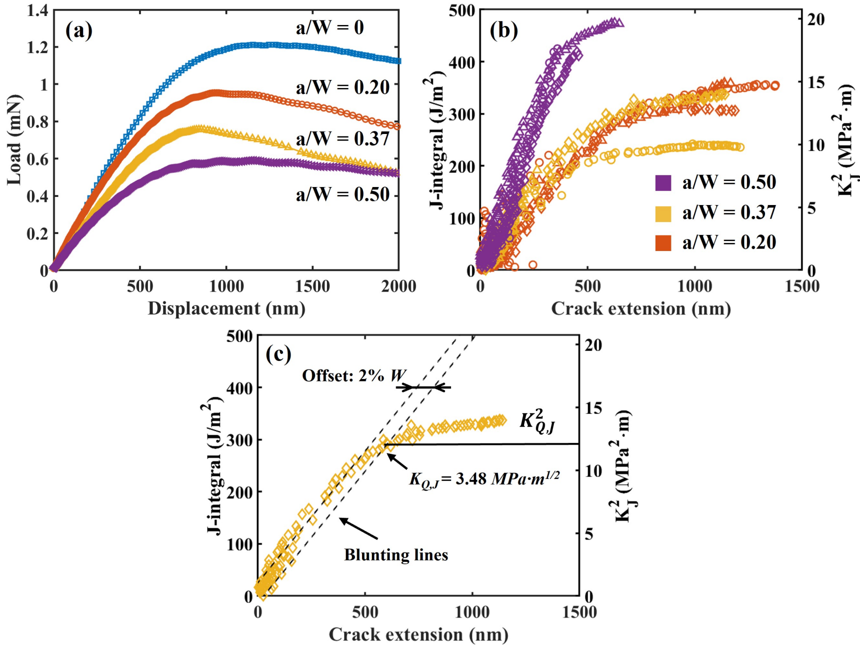

Figure 3.7.: (a) Representative load-displacement curves; (b) $J - \Delta a$ curves for the different notched microcantilevers; (c) J-integral evaluation, showing 2% W offset construction. The indices 'Q' refers to the fracture toughness calculated by a blunting line.

$$K_{IC} = \alpha_1 \sigma_f \sqrt{\pi W}(1-P)^{3/2} \tag{3.12}$$

where α_1, σ_f and P are the scaling factor, fracture strength and porosity, respectively. The fracture toughness remarkably decreases with increased porosity. To date, no mode I fracture toughness is reported in the sintered nanoporous Cu. However, due to the same technological principle, sintered porous Cu has a similar microstructure to that of the sintered porous Ag, including a single metal phase, no preferred orientation, nano-to-submicron grain sizes, randomly distributed pores, and tuneable porosity. Hence, the correlation between the fracture toughness and porosity is highly likely to be described by Eq. 3.12 because the fracture toughness is one of the reflections from the microstructure. This is further supported by the fact that solid Cu films with similar grain size of 280 nm but smaller specimen thickness of 493 nm already show an increased fracture toughness of 6.6 MPa·m$^{1/2}$ [55]. The herein determined fracture toughness values of 3 MPa·m$^{1/2}$ are closer to measured values of sub-100 nm solid Cu films at 2.3 MPa·m$^{1/2}$ [55] or severely geometrically restricted transmission electron microscopy specimens (116 nm thickness) of large grained Cu at 3.2 MPa·m$^{1/2}$ [46]. All of this suggests that the fracture in the given nanporous Cu is mainly governed by rupture of individual struts with a similar size than such geometrically limited systems.

Furthermore, the fracture toughness obtained from micro-cantilever experiments of

die-attach materials has been reported over the last decade. The comparison between different die-attach materials is scattered in Fig. 3.8, including solder materials, such as Cu_3Sn [12], Cu_6Sn_5 [59], AuSn [60] and SAC305 [10], and porous sintered Ag materials [13]. It can be seen that the sintered Cu joint is tougher than the soft Cu-Sn and Au-Sn solders, except SAC305. Additionally, it can be seen that the micron scaled specimen show a size effect regards to fracture behaviour due to the constraint of plastic zone size and the transition from a plane-strain dominated to a plane-stress dominated behavior [45, 61]. This size effect is not only the different materials but also more importantly, the different specimen sizes lead to a change in experimentally obtained fracture toughness. Although the value obtained in this work is slightly smaller than the trend of sintered Ag materials, the data in [13] was calculated from the maximum load during each experiment, neglecting any blunting line offset or R-curve type behaviour and is thus not trimmed towards a safe lower bound for fracture toughness estimations.

Moreover, Cu material has a smaller coefficient of thermal expansion (CTE) of 16.6×10^{-6}/K than the value of Ag as 18.4×10^{-6}/K. Therefore, slighter thermal stress will be accumulated at the interface during device operation. A relatively smaller fracture toughness is believed capable of withstanding high-temperature operation. Accounting for the cost-effectiveness and anti-electrochemical migration performance, sintered Cu materials can be a potential alternative to the sintered Ag as die-attach materials. Moreover, this work is helpful to the system-level modeling by digging into the fracture behavior of the sintered Cu joint.

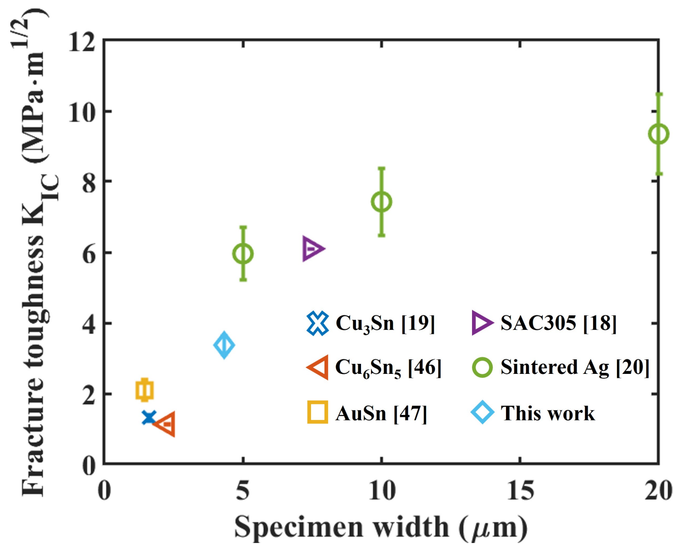

Figure 3.8.: Fracture toughness of reported die-attach materials with different specimen widths.

3.3. MACROSCOPIC MECHANICAL PERFORMANCE OF THE SINTERED NANOPARTICLES

3.3.1. EXPERIMENTAL METHODOLOGIES

In this section, a self-made nano Cu paste was prepared using the process flow shown in Fig. 3.9. The electrical explosion method produced Cu NPs [62]. The morphology and size of NPs were characterized and measured by a Hitachi 8100 SEM, where quasi-spherical Cu NPs were observed with a size of 100 ± 36 nm. Fig. 3.9(d) shows the X-ray diffraction (XRD) result of untreated Cu NPs, treated Cu NPs and treated Cu NPs after 30 days of storage. The as-produced Cu NPs were partially oxidized, confirmed by a prominent Cu_2O peak in the XRD result. Therefore, the Cu NPs must be effectively reduced first to ensure a robust inter-particle connection during the sintering process.

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First, the original Cu NPs were mixed with a solution (500 mL of 5 % formic acid and 95 % ethanol) to form a slurry magnetically stirred at room temperature for one hour. Then the slurry was centrifuged and filtered. Subsequently, the washed slurry was dried at 60 °C in the air for four hour. Thus, the oxidation could be removed by this treatment. The treatment conferred the Cu NPs excellent stability, and no severe oxidation was observed after 30 days of storage. Furthermore, the Cu NPs were formulated as a viscous paste to make it convenient for dispersion and application. Ethylene glycol and terpineol at a ratio of 1 : 1 were mixed with treated Cu NPs, with a Cu content in the paste of 80 $wt.$%. The mixture was stirred by a mechanical mixer, followed by being milled in a three-roll machine. The milled slurry was stirred by a planetary mixer at 1500 rpm for 2 mins to achieve a dispensable paste.

Figure 3.10 illustrates the process flow of sintered test sample fabrication. First, the self-made nano Cu paste was dispensed into a customized steel mould. Then, the filled mould was dried in a vacuum oven for 15 min at 120 °C. During the drying, the organic solvent evaporated so that less organic residual would be present after sintering. Following this, the dried sample was sintered in a sintering machine from Boschman B.V., with the sintering profile shown in Fig. 3.10(d). The sintering profile is the same as in Fig. 3.1. After unmolding, the dog-bone sample was finely polished to the dimensions shown in Fig. 3.10(e). The effective length was 31.25 mm, with a 6.25 mm width and approximately 1 mm thickness, which satisfied the requirement of the in situ mechanical tests.

The in situ uniaxial static tension tests were carried out to measure the mechanical properties of the sintered samples by using the micro-mechanical test system IBTC-300SL (Fig. 3.11). A 300 N sensor was equipped to ensure a high measurement accuracy of 0.1 mN. The resolution for displacement is 0.1 μm. The strain of this study is measured as the ratio of clamp displacement to specimen length. The test system allowed a maximum test temperature of 400 °C through its temperature control unit. In this study, the tensile tests were performed at four temperatures (180, 240, 300 and 360 °C) and three constant strain rates (0.0001, 0.0005, and 0.001 s^{-1}). All samples were stretched until fracture. In each group, three samples were tested to minimize the random error.

Samples that had failed the tensile testing under the test conditions of 360 °C and 0.0001 s^{-1} were characterized by Electron Backscatter Diffraction (EBSD). Prior to the EBSD characterization, the failed sample was at first line cut in the middle along the tensile direction. The cross-section was polished by ion milling (Gatan Ilion II 697). For

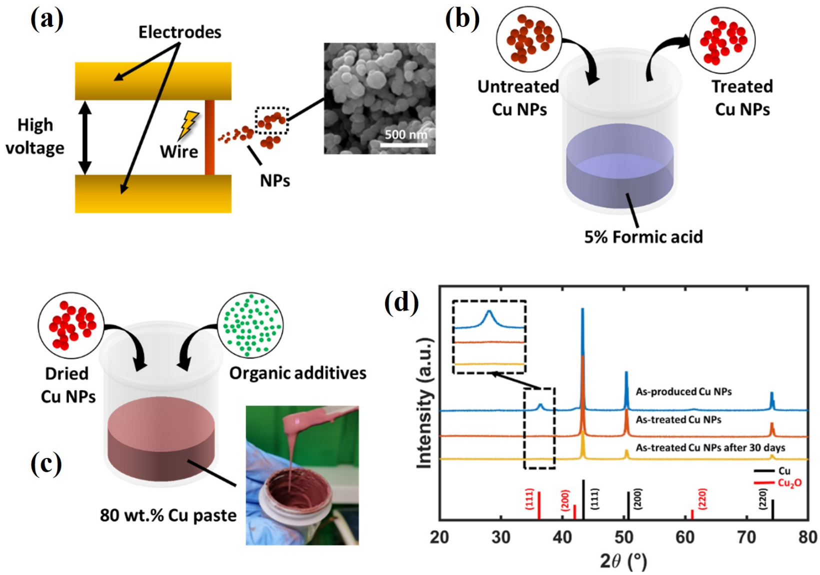

Figure 3.9.: (a) Cu NP production by the electrical explosion method; (b) acid treatment to remove oxide; (c) paste formulation; (d) XRD results on untreated Cu NPs, treated Cu NPs, and treated Cu NPs after 30 days of storage.

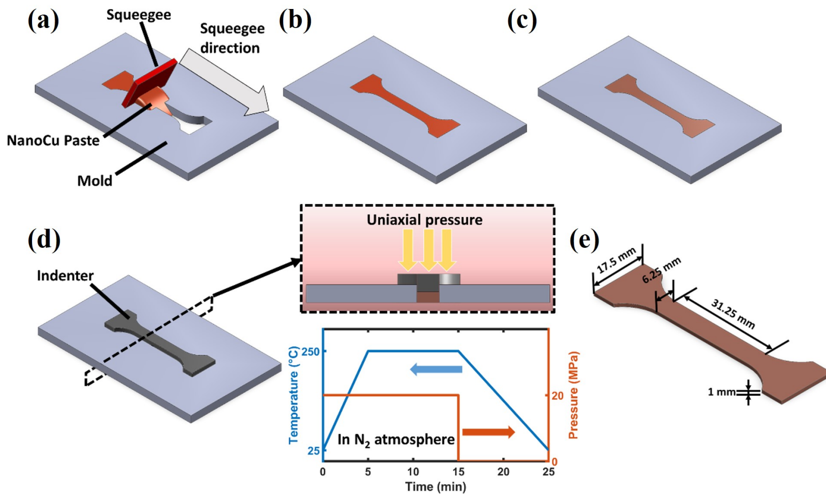

Figure 3.10.: Process flow of pressure-assisted low-temperature sintering (a) paste dispersion; (b) as-dispensed paste; (c) dried paste; (d) pressure-assisted sintering; and (e) dimensions of the sintered sample.

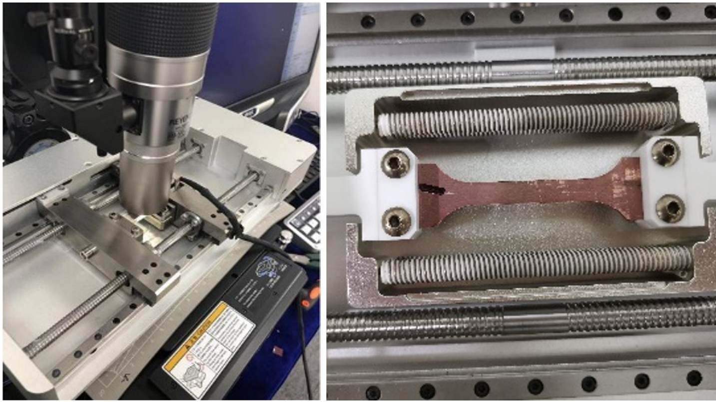

Figure 3.11.: The in situ micromechanical testing system IBTC-300SL.

each sample, three areas for EBSD analysis were selected near the fracture surface (Area A), 4 mm from the fracture surface (Area B), and 20 mm from the fracture surface (Area C), as shown in Fig. 3.12. Area C works as the reference. In this study, an Oxford C-nano EBSD system was used under 50 kV for adequate signals. The step size was chosen as one μm. The post-processing analysis was performed by CHANNEL 5 EBSD analysis software (HKL Technology) and ATEX, an open-source software for geometrically necessary dislocations (GND) analysis by means of EBSD [63].

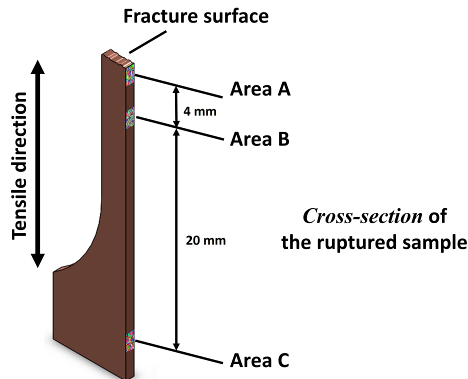

Figure 3.12.: Schematic of the locations for EBSD characterization.

3.3.2. HIGH-TEMPERATURE TENSILE RESULTS

Figure 3.13 shows the elastic modulus and tensile strength of sintered nanoCu samples measured under different temperatures and strain rates. Each data point is the average value from three specimens. It is noted that both elastic modulus and tensile strength

were affected significantly by the temperature and strain rate. The elastic modulus refers to the slope of the fitting line in the initial linear elastic stage of the stress-strain curves. During tensile testing, the tensile strength was defined as the maximum stress at the critical fracture stage.

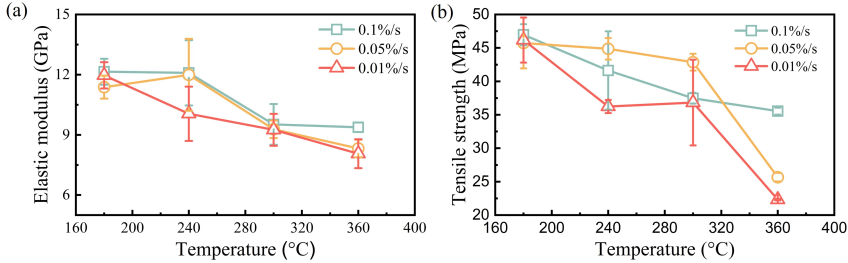

Figure 3.13.: The measured (a) elastic modulus and (b) tensile strength of sintered nanoCu samples.

With a constant strain rate, both elastic modulus and tensile strength decreased as the tensile temperature increased. This response corresponded to the behavior of bulk Cu. The strain rate from 0.1 %/s to 0.01 %/s also negatively affected the elastic modulus and tensile strength. Still, the impact was less than the effect of temperature at low temperatures. At 180 °C, the tensile strength dropped 0.79 MPa from 0.1 %/s to 0.01 %/s, and this deviation expanded to 13.23 MPa at 360 °C. As a reference for other works in this field, at 180 °C, close to the practical operating temperature of high-power electronics, the elastic modulus and tensile strength of sintered nanoCu paste were 12.15 GPa and 46.97 MPa, respectively. It is noticed in Fig.3.13 there are several data points that do not follow the abovementioned trends. It was caused by the variation in the porous tensile specimen, which can be reflected by the large error bars.

Figure 3.14 shows fracture surface morphologies and zoomed-in details of the sintered samples with the highest and the lowest elastic modulus. Dashed white lines frame the area of the fracture surface. Both samples were highly sintered with the rare presence of individual nanoparticles. However, the morphology of the fracture surface was significantly different. The sample fractured at 180 °C and 0.1%/s strain rate showed flat fracture surfaces, typical characteristics of brittle fracture. Barely any grain deformation along tensile deformation was noticeable, indicating an intergranular fracture. In addition to the lack of dimples, its low ductility was also confirmed by the flat fracture surface.

In contrast, ductile fractures occurred in the sample tested at 360 °C and 0.01%/s. Several cleavage fracture segments were observed on the fracture surface. Unlike brittle fracture-induced flat surfaces, steps are attributed to shear stress during the ductile deformation in a face-centered cubic metal. Furthermore, 360 °C is greater than the 200 °C recrystallization temperature of bulk copper, and recrystallization occurred during the high-temperature tensile test. Recrystallization was presumed to be essential in tensile strength at 360 °C. Recrystallized grains are prone to nucleate at the boundary of deformed grains and lattice defect-crowded areas. Deformation also tends to decrease the recrystallization temperature further. As a result, a recrystallized equiaxial grain with a

finer grain size can be observed in the frame of Fig. 3.14(b). The recrystallization results in a low strength but improved ductility, which corresponds to the tensile test results.

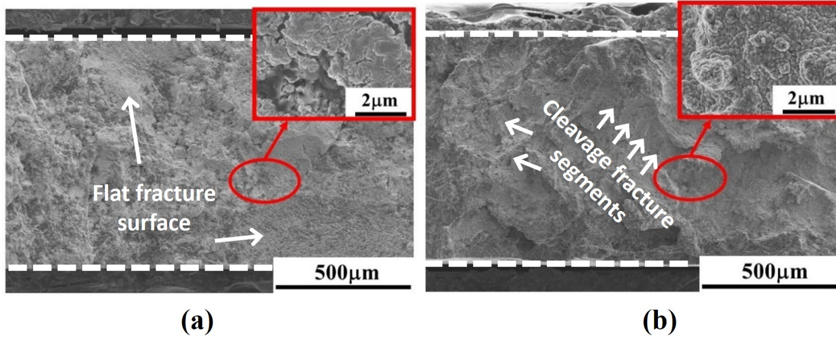

Figure 3.14.: Characteristics on the fracture surface (a) brittle fracture with 180 °C and 0.1 %/s; (b) ductile fracture with tensile temp 360 °C and 0.01 %/s.

Figures 3.15 (a)(c) present the orientation maps of the sample with the tensile test conditions of 360 °C and 0.01 %/s. The microstructure and crystallographic orientation difference is illustrated at the three locations (A, B, and C) underneath the fracture surface. The crystallographic characteristics presented a random crystal orientation distribution regardless of the relative position to the fracture surface. The pixels with a low confidence index value were the black regions close to the grain boundaries. This was attributed to the lattice distortions occurring with locally inelastic deformation.

Furthermore, the grain boundaries were identified as low-angle grain boundaries (LAGB, $\theta < 15°$), high-angle grain boundaries (HAGB, $15° < \theta < 65°$), and $\sum 3$ boundaries, as twin boundaries with a 60° misorientation. The distinguished grain boundaries and the image quality (IQ) map are visualized in Figs. 3.15(d)(f), where the red lines represent the $\sum 3$ boundary, green lines represent LAGBs, and black lines represent HAGBs. Most grain boundaries remained as HAGBs with twinning crossing within the grains after the tensile test. Compared to area C, grain refinement was extensively observed in the other two locations, around the areas of highly dense LAGBs. This resulted from the atomic rearrangement and movement of accumulated dislocations.

To quantify the differences concerning the different locations, the distribution of grain size, misorientation and GND density mapping was summarized from the EBSD measurements as shown in Fig. 3.16. Near area A and area B, the majority of grains were smaller than 50 nm, and accounted for 57% and 64% of the total grains, respectively. This refinement could be attributed to the recrystallization during the high-temperature deformation. The increase in dislocation density and further transgranular fracturing also contributed to forming the high ratio of nanograins. In contrast, the grain size distribution was more uniform in area C. It can be surmised that much less plastic deformation behavior occurred in this area, indicating that the texture and microstructure in area C could be a reference for studying the deformation mechanism. Further quantitative analysis of the distribution of grain boundaries was conducted, as shown in Figs.

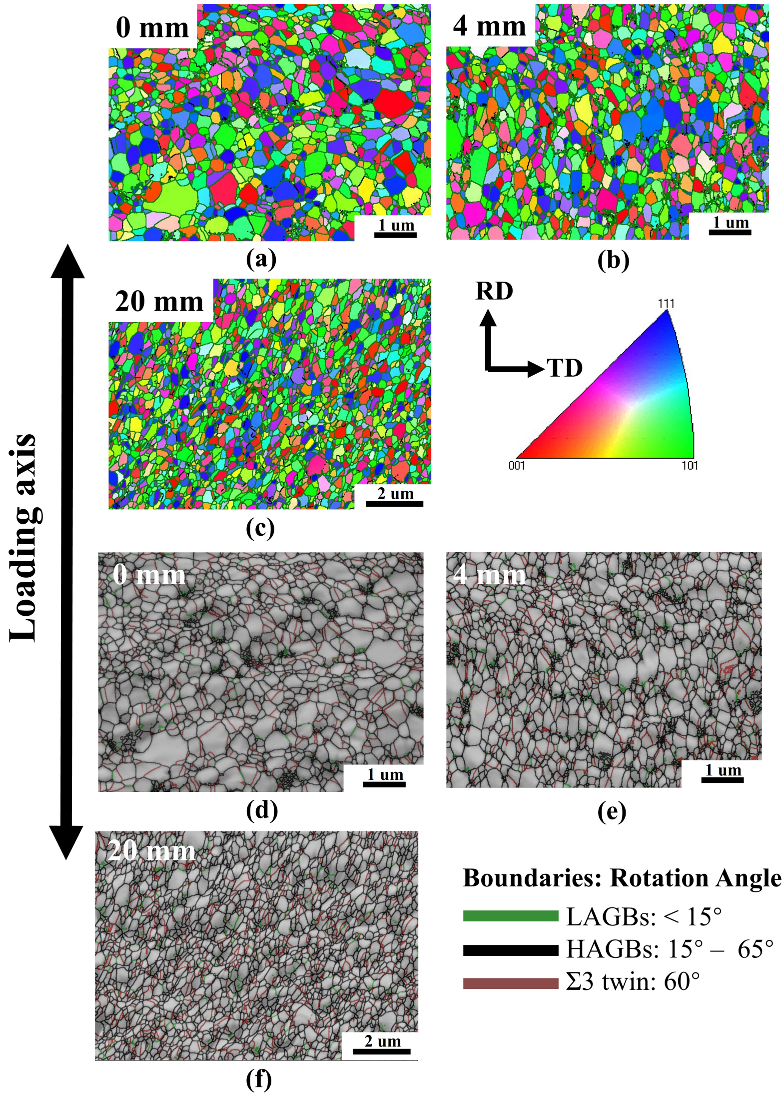

Figure 3.15.: EBSD images of sintered nanoCu sample after the 360 °C and 0.0001 s^{-1} tensile test. (a) Fracture surface; (b) 4 mm from the fracture surface; (c) 20 mm from the fracture surface, and grain boundary visualization on image quality (IQ) map (d) fracture surface; (e) 4 mm from the fracture surface; (f) 20 mm from the fracture surface.

3.16(d)(f). The average grain boundary misorientation angles of the three locations, A, B, and C, were estimated to be 37.51°, 35.29° and 39.1°, respectively. The fraction of $\sum 3$ twin boundaries was 5.76% in area A, 4.68% in area B and 5.52% in area C, which was the farthest from the fracture. The minor deviation in the fraction of the ratio of $\sum 3$

twin boundaries implies that twinning was not the dominant mechanism in the high-temperature tensile testing of sintered nanoCu samples. Additionally, Figs. 3.16(g)-(i) present the GND density mapping calculated by ATEX and the average value was given on top-right. It can be seen that the in area A and B, the GND density is much higher than the reference location, area C and the most dislocations concentrated around the grain and sub-grain boundaries.

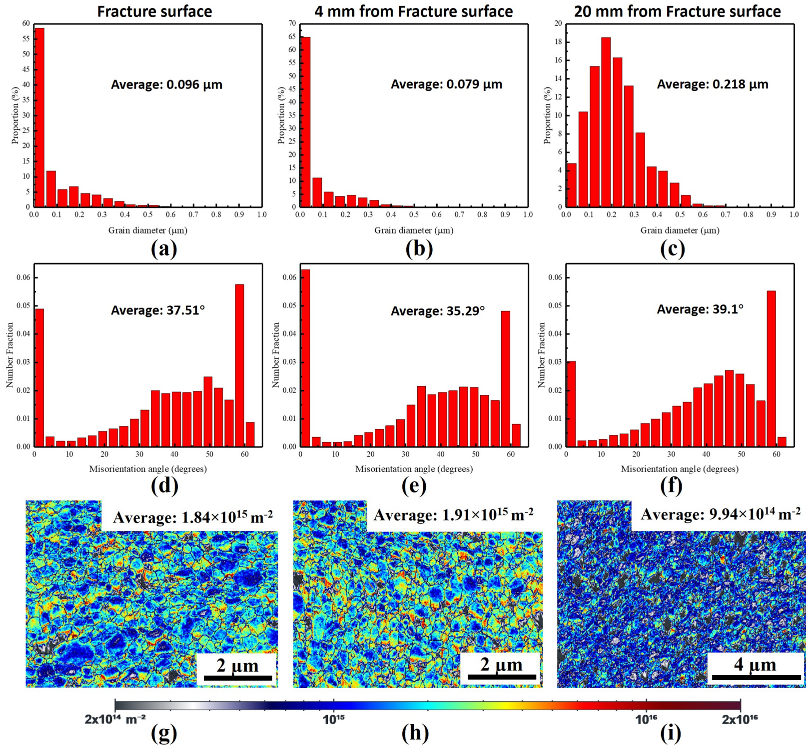

Figure 3.16.: Grain size and misorientation of the sample after tensile test at the testing conditions of 360 °C and 0.0001 s^1. (a)(c) Grain diameter; (d)(f) misorientation angle; (g)-(i) GND density mapping.

The fraction of LAGBs in the different areas revealed that area C contained the smallest ratio of LAGBs compared to areas A and B. The grain boundaries with a misorientation angle below 2.5° occupied only 3.0% of the total grain boundaries, while the values for areas A and B were 4.8% and 6.3%, respectively. This result corresponded to the results of the grain refinement shown in Fig. 3.15 and the grain size distribution shown in Figs. 3.16(a)(c). This can be regarded as the result of more plastic deformation.

Moreover, owing to the high tensile temperature, the recrystallization process promoted dislocation accumulation and grain boundary shift. The mechanical input from the tensile testing accelerated the motions of dislocations (movement, aggregation, and entanglement). Eventually, many of the substructures were formed, resulting in a high

fraction of LAGBs. At this moment, the boundaries of these substructures are the main obstacles to inhibit the dislocation movement as indicated in Figs. 3.16(g)-(i). A higher GND density means a larger plastic strain in the area. Thus, the conclusion can be drawn that along the tensile direction, areas A and B had a vital contribution to the plasticity of the sintered nanoCu paste. Compared to area A, where the fracture occurred, a higher fraction of LAGBs, higher average GND density and refined grains were found in area B, indicating more plastic deformation. This implies that the failure at the end of the tensile test was caused by weak inter-particle connections that induced rupture rather than by exceeding the plasticity limit of the sintered structure.

3.3.3. PARAMETERIZATION OF THE ANAND MODEL

A unfied viscoplastic constitutive model was proposed by Anand and further improved by Brown [64]. This study used the Anand model to characterize the viscoplasticity, strain rate and temperature-related deformation behavior of the sintered nanoCu paste. The Anand model is shown in Eq. 3.13:

$$\dot{\varepsilon}_p = A\exp(-\frac{Q}{RT})[\sinh(\xi\frac{\sigma}{s})]^{1/m} \tag{3.13}$$

The Anand model assumes that the internal variable s is proportional to the stress σ, and the relationship is:

$$\sigma = cs \tag{3.14}$$

where c is a function of temperature and strain rate:

$$c = \frac{1}{\xi}\sinh^{-1}((\frac{\dot{\varepsilon}_p}{A}e^{\frac{Q}{RT}})^m),\ c<1 \tag{3.15}$$

where $\dot{\varepsilon}_p$ is the inelastic strain rate, A is a constant, Q is the activation energy, m is the strain rate sensitivity index, ξ is the stress multiplier, R is the gas constant, and T is the absolute temperature. The internal variable can be expressed by

$$\dot{s} = [h_0|1-\frac{s}{s^*}|^a\mathrm{sign}(1-\frac{s}{s^*})]\dot{\varepsilon}_p \tag{3.16}$$

where

$$s^* = \hat{s}[\frac{\dot{\varepsilon}_p}{A}\exp(\frac{Q}{RT})]^n \tag{3.17}$$

In Eq. 3.16, s^* represents the saturation value of the internal variables at a given temperature and strain rate, h_0 is the hardening/softening coefficient and a is the strain rate sensitivity index. In Eq. 3.17, $\hat{s}$ and n denote a coefficient and the strain rate sensitivity for the saturation value for deformation resistance, respectively.

From Eqs. 3.14, 3.15 and 3.17 together with $\sigma^* = cs^*$, the equations are as below:

$$\sigma^* = (\frac{\hat{s}}{\xi})(\frac{B}{A})^n\sinh^{-1}[(\frac{B}{A})^m] \tag{3.18}$$

where σ^* is the saturation stresses and B is the temperature-compensated strain rate expressed as:

$$B = \dot{\varepsilon}_p \exp(\frac{Q}{RT}) \tag{3.19}$$

In Eq. 3.18, the saturation stresses of material is relevant to the temperature and the strain rate. At a certain temperature with the condition of $s^* > s$, from Eq. 3.14 and 3.16, we obtain:

$$\frac{d\sigma}{d\varepsilon_p} = ch_0(1-\frac{\sigma}{\sigma^*})^a \mathrm{sign}(1-\frac{\sigma}{\sigma^*}),\ a \geq 1 \tag{3.20}$$

Therefore, the following stress-strain relationship can be obtained by the integral with respect to Eq. 3.20:

$$\sigma = \sigma^* - [(\sigma^* - \sigma_0)^{(1-a)} + (a-1)(ch_0)(\sigma^*)^{-a}\varepsilon_p]^{1/(1-a)} \tag{3.21}$$

where $\sigma_0 = cs_0$ and s_0 is the initial value of s.

Subsequently, the stress-strain data of the sintered nanoCu samples were used to fit the Anand model, where nine parameters need to be fitted respectively. The parameter analysis was achieved using the commercial software 1*stOpt* (7D-Soft High Technology Inc.). The standard process of determining materials constants, s_0, Q/R, A, ξ, M, N, h_0, $\hat{s}$,a is shown below [65, 66],

(1) The saturation stresses regarding constant rates and temperatures were obtained from the stress-strain curves.

(2) The value of a, ch_0 and σ_0 in Eq. 3.21 were determined from the saturation stresses obtained in step 1 by using least-squares nonlinear regression fitting. Levenberg-Marquardt (LM) algorithm and universal global optimization (UGO) were adopted in this study. The iteration step and the criteria of convergence is 1000 and 1×10^{-10}, respectively.

(3) The value of A, Q, M, N and in Eq. 3.18 were determined by using simulated annealing (SA) algorithm to find the global optimal solution. The maximum iteration number was set as 1000. The acceptance probability function, known as Metropolis criterion, is $P = \min\{1, e^{\Delta E/T}\}$, where ΔE is the difference between two steps [67].

(4) The value of ξ was selected with the constant c in term ch_0 was less than unity. $\hat{s}$ is therefore determined from the combined term $\hat{s}/\xi$. Moreover, the value of h_0 was determined from the combined constant ch_0 and the value s_0 was calculated with σ_0 acquired in step (2) by using Eq. 3.14.

Consequently, the obtained materials parameters of Anand viscoplastic model for the sintered nano Cu materials are listed in Table 3.2. The experimental stress-strain curves and the fitting results are shown in Fig. 3.17. The Anand model has been demonstrated to adequately describe the high-temperature tensile deformation behavior of sintered

nano Cu materials. It can be seen that the experimental data and prediction has good agreement in the inelastic deformation behavior at temperatures higher than 240 °C. While the extracted Anand model describes the linear elastic deformation well at all temperatures with no observed strain rate dependency.

Table 3.2.: The Anand viscoplastic model parameters of sintered nano Cu materials

Parameters	s_0 [MPa]	Q/R [K^{-1}]	A [s^{-1}]	ξ	M	N	h_0 [MPa]	$\hat{s}$ [MPa]	a
Values	0.446	7146.478	2.677	12	0.884	2.917×10^{-8}	210.351	53.874	1

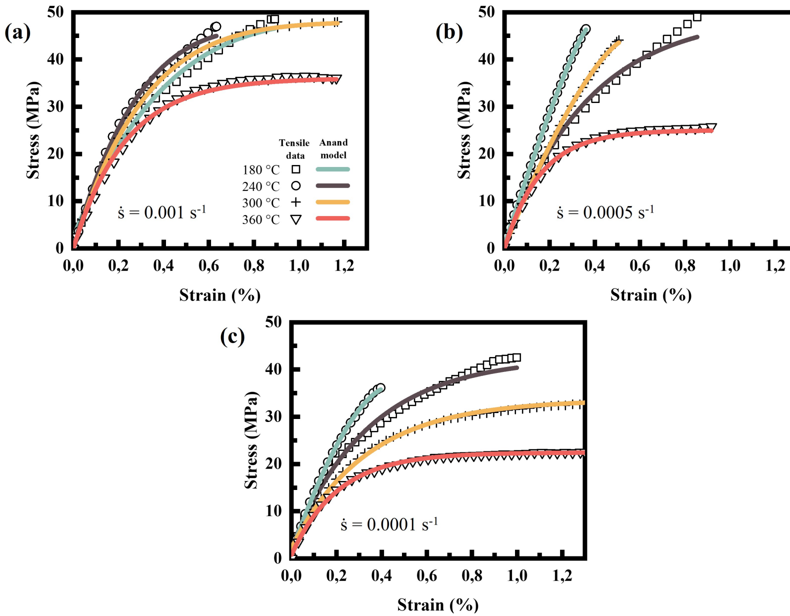

Figure 3.17.: The fitted in-situ tensile response, using the Anand model at (a) 0.001 s^{-1}; (b) 0.0005 s^{-1}; (c) 0.0001 s^{-1}.

According to the root mean square error (RMSE) calculations shown in Table 3.3, the RMSEs between the test value and the predicted value of the Anand model were slightly larger at the temperature of 180 °C and 240 °C. The low RMSE at 240 °C with 5×10^{-3} and 1×10^{-4} s^{-1} strain rate was due to the lack of inelastic behavior in the stress-strain curves. While at the temperatures of 300 °C, and 360 °C, corresponding to the curve with evident creep behavior, the RSME between the predicted value of the Anand model and the actual test value was less than 1. Thus, the two values were in good agreement, and the fitting accuracy of the Anand model was high. In summary, the test values agreed with

the predicted values at viscoplastic behavior at higher temperatures and elastic behavior at lower temperatures.

Table 3.3.: The root mean square error of the suggested Anand model

Temperature (°C)	strain rate (s^{-1})	RMSE
	1×10^{-3}	1.3024
180	5×10^{-3}	1.5649
	1×10^{-4}	1.1025
	1×10^{-3}	1.1735
240	5×10^{-3}	0.1236
	1×10^{-4}	0.2643
	1×10^{-3}	0.2634
300	5×10^{-3}	0.2364
	1×10^{-4}	0.3802
	1×10^{-3}	0.8001
360	5×10^{-3}	0.5036
	1×10^{-4}	0.2125

3.4. CONCLUSION

In this chapter, microscopic fracture toughness and macroscopic viscoplastic model of Cu nanoparticles sintered structure were evaluated. They are the fundamental focuses to evaluate the remaining useful lifetime of a die-attach layer in the power electronics packaging.

In the first part, an experimental method for evaluating crack propagation behavior at a micro-scale in a sintered nanoporous Cu joint by micro-fabricating micro-cantilevers with different notch depths. A 3D sintered Cu model was reconstructed by a FIB milling method. The sintered Cu nanoparticle structure yielded a low porosity of 8.25 ± 0.69 %. Necking tips and dimple ridges were observed on the fracture surface, confirming elastic-plastic fracture in the bending test. MCs elastic modulus and yield strength were extracted as 41 ± 2 GPa and 970 ± 21 MPa, respectively. Subsequently, in-situ microscale measurements of $J - \Delta a$ curves were carried out on different notched (*a*/*W* 0.20, 0.37, and 0.50) specimens. Specimens with an *a*/*W* ratio of 0.20 and 0.37 presented a close bending behavior. A tougher fracture was noticed with a higher *a*/*W* value of 0.5. Instead of the LEFM theory, the microscopic conditional fracture toughness K_Q was translated from elastic-plastic J-integral evaluation, ranging from 3.2 ± 0.3 MPa·m$^{1/2}$ to 4.3 ± 0.1 MPa·m$^{1/2}$. The microscopic fracture toughness presents a limited relationship with notch depth. A relative initial notch depth *a*/*W* between 0.20 and 0.37 shows a near-constant fracture toughness. This provides insights into the testing conditions for future testing on the thermally aged specimens and the study on the size effect.

In the second part of macroscopic evaluation, dog-bone tensile specimens were fabricated in an N_2 environment by pressure-assisted sintering at 250 °C. The dispensable paste was self-formulated by Cu NPs with a 100 ± 36 nm size. The high-temperature

tensile experiments were implemented at four temperatures and three strain rates. By increasing the temperature from 180 °C to 360 °C, both the elastic modulus and tensile strength of the sintered nanoCu dropped significantly to 8.06 GPa and 22.32 MPa. At the same time, the response to varying the strain rate between 1×10^{-4} s^{-1} and 1×10^{-3} s^{-1} was found to be minor. Next, different failure modes were determined from the failure analysis. From the fracture surface morphology, the sample tested at 180 °C and 0.001 s^{-1} showed brittle fracture features, while more ductile fracture features were present in the sample tested at 360 °C and 0.0001 s^{-1}. Evidence of grain refinement and LAGB formation at different locations through the EBSD results confirms that ductility was significantly promoted by recrystallization at high temperatures. Additionally, an Anand model was fitted and parameterized according to the stress-strain curves of the sintered Cu paste. The established numerical model was then used to describe the constitutive behavior of sintered Cu paste. The proposed numerical model presented high consistency at high-temperature conditions.

In summary, the results of this chapter revealed the failure mechanism of the microscopic bending test and high-temperature tensile of Cu nanoparticles sintered structure and provided insights into package-level modelling by exploring the fracture behavior and elastic-plastic constitutive models. These results suggested solid comprehensive approaches to accelerate the assessment process of the mechanical properties of porous sintered structures.

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OFFLINE AND ONLINE THERMAL MONITORING OF THE SINTERED NANOPARTICLES

The rapid development of power electronics has challenged the thermal management of high power semiconductor packaging. Further developments in this domain can be supported essentially by developing fast and reliable thermal characteristic evaluation. This chapter employs the transient thermal measurement to characterize the thermal resistance of Ag- and Cu-sintered die attach joint utilizing a Si thermal test chip. Low junction-to-case thermal resistance of the sintered joints were extracted as 0.144 K/W and 0.158 K/W for Ag and Cu paste, respectively. Moreover, by adopting the offline thermal measurement on the sintered joint, online thermal performance monitoring over 500 cycles of thermal cycling test ($-55\,^{\circ}C$ to $150\,^{\circ}C$, $\Delta T = 205\,^{\circ}C$) was characterized by a fast heat pulse-enabled in-situ transient thermal measurement. The thermal degradation of Ag- and Cu-sintered quad-flat no-leads (QFN) discrete Si MOSFET device was evaluated by the thermal impedance over the first 0.1 seconds of the heat pulse. The thermal performance degradation showed remarkable consistency with the observed adhesion results. Ag-sintered products presented excellent robustness with a 2.5% to 3.8% thermal impedance increase over 500 cycles, while significant thermal degradation was recorded in the Cu-sintered QFN.

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4.1. INTRODUCTION

RECENTLY, nano-metallic sintering, such as that of Ag and Cu, has received extensive attention in die-attach technology [2–5]. Nanometallic materials are tuned to have process temperatures comparable to those of conventional solders. However, in contrast to soldering, nanometallic sintering is an irreversible process, yielding a material with a higher melting point and excellent electrical and thermal conductivity [6–8]. The evaluation of the thermal performance of nano-metallic materials as a die-attach layer is crucial for developing and applying these materials in corresponding processes and packages.

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Conventionally, to determine the junction-to-case thermal resistance θ_{jc}, the junction temperature T_j, case temperature T_c, and power dissipation of the device under test (DUT) must be measured. This widely used method applies a thermocouple to a case to measure the case temperature. However, the thermocouple can only estimate the temperature of a single contact point under the DUT, whereas the temperature distribution over the heatsink may not be uniform. Consequently, the accuracy and reproducibility of the conventional thermocouple method are low [9]. In 2010, the JEDEC51-14 standard specified the transient dual interface method (TDIM) without thermocouples to improve the reproducibility of θ_{th-jc} measurement with a 1D dominant heat flow path [9, 10].

For a systematic approach to apply the TDIM method and measure the junction-to-case thermal resistance, it is preferable to use a chip that provides power delivery and temperature measurements in the test package [11]. Transient thermal measurements of sintered metallic materials have been reported by utilizing device characteristics, such as the gate-emitter voltage [2, 12, 13] and forward voltage [14, 15]. Further developments in the domain of thermal evaluation in a sintered structure can significantly support fast and flexible thermal characteristic evaluation for power electronic packaging. Therefore, a universal solution for transient thermal evaluation is urgently required to enable fast material selection in different user cases.

To continuous monitoring the health condition of the devices during operation, the online health monitoring of power devices is usually implemented by electrical methods since temperature estimation can be carried out by measuring electrical properties. Furthermore, methods using thermo-sensitive electrical parameters (TSEPs) can better correlate the electrical properties to the junction temperature [16]. It has been reported that TSEPs such as on-state voltage [17, 18], Turn-on-off delay time [19–21], and peak gate current [22, 23] can work for online measurements with excellent linearity. However, implementing the aforementioned online measurements requires high sensing costs for large currents, high bandwidth, complex trigger circuits, etc.

Therefore, further developments in this domain can be supported significantly through fast and flexible thermal characteristic evaluations for power electronic packaging. Flexible offline and online thermal performance evaluations are both required for fast design and material selection in different user cases.

This chapter first presents a fast, flexible offline thermal evaluation approach for nano-metallic die-attach joints (Section 4.2). An in-house developed TTC [24] is applied as a tool in TDIM to compare the thermal conductivity of different nano-metallic sinter pastes. The thermal performance of different die-attach sinter pastes was evaluated and

compared using the TDIM method following the JEDEC51-14 standard. Moreover, to implement the online thermal evaluation of nanoparticles sintered die-attach over the thermal cycling tests (-55 °C to 150 °C), an in-house developed online health monitoring system is applied to trace the thermal degradation over the cycles [25](Section 4.3).

4.2. OFFLINE THERMAL PERFORMANCE CHARACTERIZATION

4.2.1. EXPERIMENTAL METHODOLOGIES

The conventional junction-to-case thermal resistance measurement method directly measures the temperature difference using thermocouples in combination with on-chip temperature sensors [9]. However, this method is susceptible to errors; First, the temperature distribution over the package case may not be uniform, while the thermocouple measures the temperature only at its contact point. Secondly, the thermocouple is not entirely embedded in the cooling plate and therefore does not provide an accurate temperature reading. Thirdly, a trench or a hole is needed at the backside of the heatsink plate to place the thermocouple, which adversely affects the measurements accuracy and influences the thermal resistivity of the heat removal path. Moreover, the clamping pressure applied in this method might close any potential delamination at the interfaces that must be detected in reliability experiments.

TDIM mitigates the errors of thermocouple measurements, allowing for higher reproducibility and consistency without a case temperature measurement [26]. To evaluate the thermal impedance $Z_{\theta JC}(t)$, the following equation is defined:

$$Z_{\theta JC}(t) = \frac{T_J(t) - T_J(t=0)}{P_H} \tag{4.1}$$

Where P_H is the constant power dissipated by the DUT at $t = 0$, and $T_J(t)$ is time-dependent junction temperature measured by a dedicated resistance temperature detector (RTD) when the case surface is sufficiently heat sunk by a cooling setup.

This method requires two measurements with different cooling conditions at the case surface. In such a way, the thermal impedance will not change until the heat reaches the heatsink contact, where the temperature starts to rise. At this point, the impedance curves begin to separate, where the external thermal resistance contributes to heat removal. The cumulative thermal resistance at the separation point of these two measurements indicates θ_{JC}.

A constant current was applied to the on-chip micro-heaters to generate a certain P_H to heat the DUT. To measure $T_J(t)$, on-chip high precision RTDs with a sensitivity of 12 Ω/K are used. After the heating power was switched off, the data acquisition system recorded the transient resistance of the RTD. The online RTD data provides the cooling curve, which is not disturbed by the heating power. Using the RTD calibration data of the thermal test chip, its resistance can therefore be converted to the DUT junction temperature.

This study applied four metal nanoparticle pastes (Ag paste, Cu paste A, B, and C) from different vendors. At first, the metallic sinter paste was dispensed by stencil printing on the top surface of pure Cu plates, which was pretreated by isopropyl alcohol(IPA). The thickness of the printed layer is 100 μm. Subsequently, a drying step was performed in

the air at 110 °C for 20 minutes. Afterward, the TTC was mounted on the dried paste, and the pressure-assisted sintering was conducted in a vacuum bonder (AWB-04, Applied Microengineering Ltd, UK). The sample was then heated to 280 °C with a 20 °C/min ramp. Next, 10 MPa uniaxial force was applied for 10 minutes. Finally, the pressure was released, and the sample was cooled down in the bonder until 80 °C to prevent oxidation.

The entire measurement setup is shown in Fig. 4.1. The sintered sample was wire-bonded to a PCB for electrical connection using 25 μm thick Au wires, and the whole assembly is connected to a close-loop water cooling element. According to the TDIM method, the heatsink-cooling plate is in contact with the copper case with or without thermal grease. For the thermal grease, MX-4 from Arctic GmbH with thermal conductivity of 8.5 W/m·K was used in this study.

The test sequence is illustrated in Fig. 4.2. The RTD sensing current used to determine the chip temperature was set to 0.4 mA to exclude self-heating errors. Meanwhile, the heaters were driven by a current of 2.2 A from a BK Precision 1550 DC Power Supply (36 V, 3 A). The driving current was chosen to maximize the output power within the limitations of the power supply. To record sufficient data points and guarantee synchronization, two data acquisition systems (sampling rate: 250 kS/s) from National Instruments were used to read out the voltage of the heater and temperature sensor, respectively.

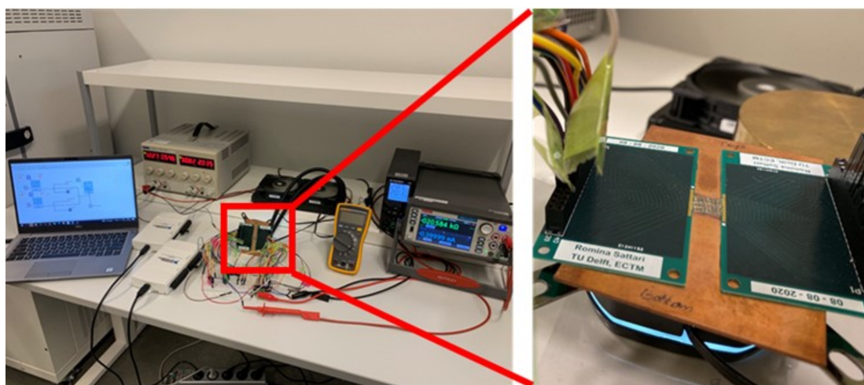

Figure 4.1.: The TDIM measurement setup and the wire-bonded sample.

4.2.2. JUNCTION-TO-CASE THERMAL RESISTANCE CHARACTERIZATION

Prior to the measurement, the setup with an 8 × 8 mm^2 chip on the Cu substrate was set to equilibrium with a driving current of 2.2 A. The corresponding chip temperature and power consumption at equilibrium are shown in Figure 4.3. All samples consumed approximately 68 W of power. The minor difference in the power consumption, that is, less than 0.2 W, can be attributed to the variations in the temperature-dependent heater resistance. As for the chip temperature, the Ag paste sample had the lowest value at 75.6 °C, while that of the samples of Cu pastes A and B were 77.8 °C, and Cu paste C performed slightly worse, at 78.7 °C.

Subsequently, the driving current was switched off and the signal on the temperature

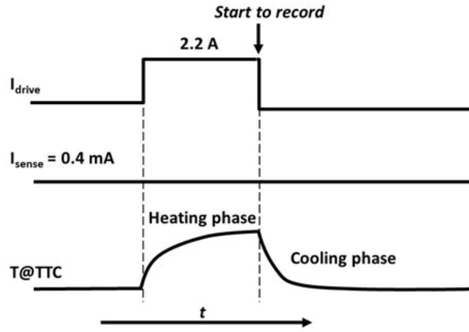

Figure 4.2.: The TDIM measurement setup and the wire-bonded sample.

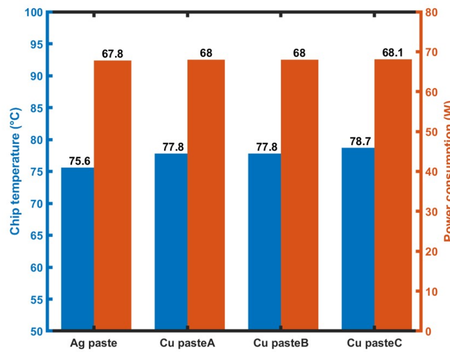

Figure 4.3.: Chip temperature and power consumption at equilibrium.

sensor was recorded simultaneously for 120 s. A digital low-pass filter was first applied to denoise the oversampled signals during the signal process. The sparse signals were then smoothed using a Gaussian-weighted moving average filter. Figure 17 show the curves of the temperature change and thermal impedance of the sample. Figure 17(a) shows the smoothed results of the temperature change of the Cu paste A sample with and without thermal interface materials (TIM). In addition, owing to the inevitable electrical disturbance, an offset time of 1000 μs was subtracted according to the standard [9]. After the offset correction, the temperature change for the sample with and without TIM was 48.38 °C and 28.12 °C, respectively.

It can be seen in Figure 4.4(a) that the sample reaches steady-state at 100 s and the difference in thermal impedance $\Delta\theta$ is 0.2848 K/W. It can be noticed that the two curves present a separation point when the heat flux reaches the top surface of the cooling block. Therefore, the thermal impedance of the separation points indicates θ_{JC}, as marked in Figure 4.4(b).

To precisely determine the point of separation, the variable transformation t to $z = \ln(t)$ was applied, where $a(z)$ was derived to obtain the θ_{JC} value as a function of z, as shown

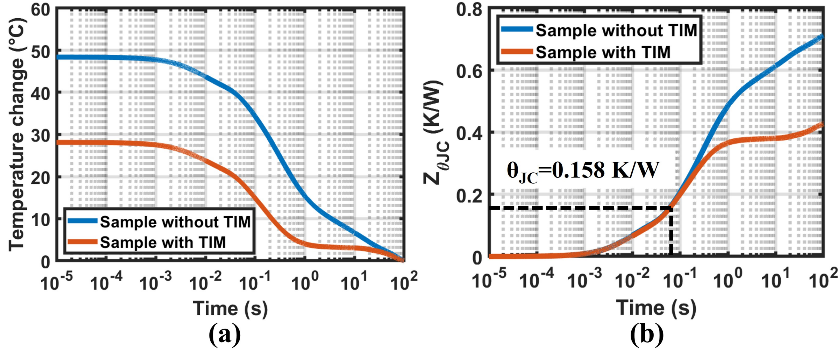

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Figure 4.4.: (a) Junction temperature change and (b) Z_{th} curve during the thermal transient for the sample with and without TIM.

in Eq. 4.2:

$$a(z) = Z_{\theta JC}(t = \exp(z)) \quad \text{for} z = \ln(t) \tag{4.2}$$

Therefore, piecewise linear interpolation can be performed at the measurement points $(z_i, Z_{\theta JC})$ to compute the derivatives of da/dz. The number of interpolations chosen was 200, which meets the requirements of the standard [9]. Subsequently, to minimize the impact of the steady-state difference, the derivative of a was normalized by $\Delta\theta$, as shown in Eq. 4.3:

$$\delta Z_{\theta JC}(t) = \frac{\Delta(da/dz)(dt)}{\Delta\theta} \tag{4.3}$$

To prevent the result from being influenced by random fluctuations of the $\delta(Z_{\theta JC})$ curve, the difference between the two $Z_{\theta JC}$ curves was fitted with the RC network response. Then, a trend line $\epsilon = 0.0045$ W/K $\times\ \theta_{JC} + 0.003$ was applied, and the abscissa of the intersection point of the and curves, as shown in Figure 4.5, is the θ_{JC} of the sample. Thus, the junction-to-case thermal resistance θ_{JC} of Cu paste A sample is found to be 0.158 K/W.

The evaluation of θ_{JC} was also performed by utilizing the separation of the cumulative structure functions $C_{\theta\Sigma}$ $(R_{\theta\Sigma})$ calculated from the sample with or without TIM. The cumulative structure function (SF) of a heat flow path is defined as the cumulative thermal capacitance $C_{\theta\Sigma}$ as a function of the cumulative thermal resistance $R_{\theta\Sigma}$ along the heat flow path. In the case of a 1-D heat-flow path, the cumulative SF can separate the thermal properties of the individual layers in the package. Similar to the Z_{th} curves, the cumulative SFs of the two Z_{th} curves were expected to separate because the heat flux flowed into an interface with different thermal conductivities. Thus, the separation point of the cumulative structural functions indicates the value of θ_{JC}.

In this study, $Z_{\theta JC}$ curves were transformed into cumulative structure functions using the TDIM-Master software [27]. First, as recommended by the JEDEC51-14 standard

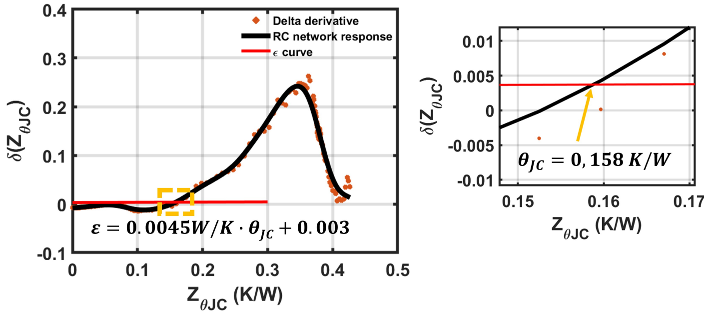

Figure 4.5.: θ_{JC} is the abscissa of the intersection of the RC response network and ϵ curve. The yellow framed area is zoomed in aside.

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[9], the time-constant spectrum is computed by numerical deconvolution with bandwidth Φ and edge steepness σ of 0.45 and 0.05, respectively. The time-constant spectrum was related to the FOSTER RC model for the distributed thermal networks. The lumped-element FOSTER model can then be generated from the discredited time-constant spectrum function. However, the FOSTER model cannot be utilized to characterize the thermal structure because it contains only the node-to-node capacitance. Thus, the FOSTER RC network was transformed into the CAUER RC network to obtain an accurate physical description of the heat flow path [28]. The cumulative structure extends the CAUER ladder description to the continuous case. In other words, the discretization of the cumulative SF results in a CAUER RC network.

Figure 4.6(a), presents an example of the cumulative SF for Cu paste A sample after numerical transformation. The red and blue lines represent the samples with and without TIM, respectively. The horizontal axis denotes the sum of the thermal resistance along the thermal path. The different portions of the curve are identified as the Si TTC chip, die-attach layer, Cu case, TIM, and closed-loop water cooling element. It can be seen that the SFs initially match well until the cumulative Rth reaches a value where the TIM is included. As shown in Figure 4.6(b), the separation point of the SFs can be extracted by plotting the deviation between the two curves. The figures below show the data analysis of Cu paste sample A, yielding a junction-to-case thermal resistance value of 0.191 K/W.

Thus, the θ_{JC} of all the samples was extracted based on the point of separation of $Z_{\theta JC}$ curves, as well as the cumulative structure functions. The results are presented in Table 4.1. The θ_{JC} value obtained from the SF separation is slightly larger than that obtained from $Z_{\theta JC}$ curve separation, which was reported in another study as well [10]. Table 4.1 shows that the Ag paste sample has the lowest θ_{JC} for both methods, followed by Cu pastes A, B, and C. This trend is consistent with the abovementioned difference in the chip temperatures in Fig. 4.3.

To elaborate on the θ_{JC} difference between different materials, Figure 4.7 displays scanning acoustic microscopy (SAM) images of the sintered samples after measurement. The scanning process resulted in horizontal shadows. It can be seen that a homogeneous sintered layer was observed in the sintered Ag paste and Cu paste A samples. However, sintered Cu paste B showed several black spots, which can be attributed to the drying

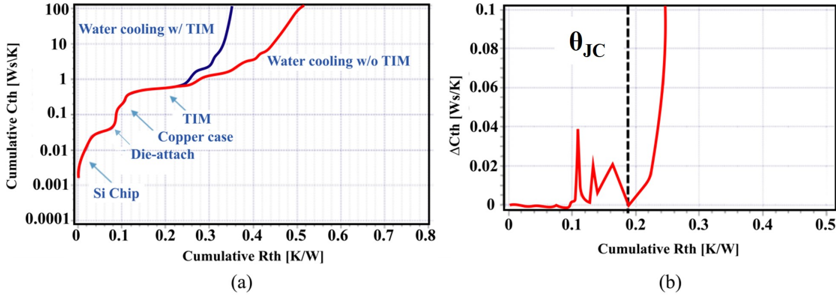

Figure 4.6.: Cumulative structure function for Cu paste A sample.

Table 4.1.: θ_{JC} of die-attach sintered using different metal nanoparticle pastes

Die-attach materials	θ_{JC} (K/W) from $Z_{\theta JC}$ curves separation	θ_{JC} (K/W) from SF separation
Ag paste	0.144	0.149
Cu paste A	0.158	0.191
Cu paste B	0.162	0.205
Cu paste C	0.168	0.214

channels of the organic compound. The sintered Cu paste C sample exhibited dense spots, indicating that worse drying channels occurred during the sintering process. In addition, the evident cracks in Figure 4.7(c) and (d) may have been caused by external forces during transportation and operation. Therefore, it was found that the adhesion in the different sintered samples corresponded to their thermal performance. The seamless adhesion of Ag resulted in it outperforming the others. Similarly, Cu paste A outperformed the other two Cu paste samples owing to its better adhesion.

4.3. ONLINE THERMAL PERFORMANCE CHARACTERIZATION

4.3.1. EXPERIMENTAL METHODOLOGIES

In the implementation of online health monitoring on the sintered power device, this study used 40V/190A Si power MOSFET (BUK7Y1R4-40H) from Nexperia and silver-metalized QFN leadframes as product carriers. A self-made Ag and Cu paste were applied as the die-attach material for thermal evaluation [29]. In addition, 20 MPa and 10 MPa were applied accordingly to investigate the influence of sintering pressure on thermal degradation. The samples were divided into three groups, QFN-A1, QFN-A2 and QFN-C, referring to 20 MPa Ag sintered, 10 MPa Ag sintered and 20 MPa Cu sintered QFN products.

In the process, the die-mount was implemented by a die-bonder (Tresky 3000-Pro) and an AML wafer bonder was used to implement pressure-assisted sintering on the entire leadframe. The detailed process parameters are listed below in Table ??. It needs

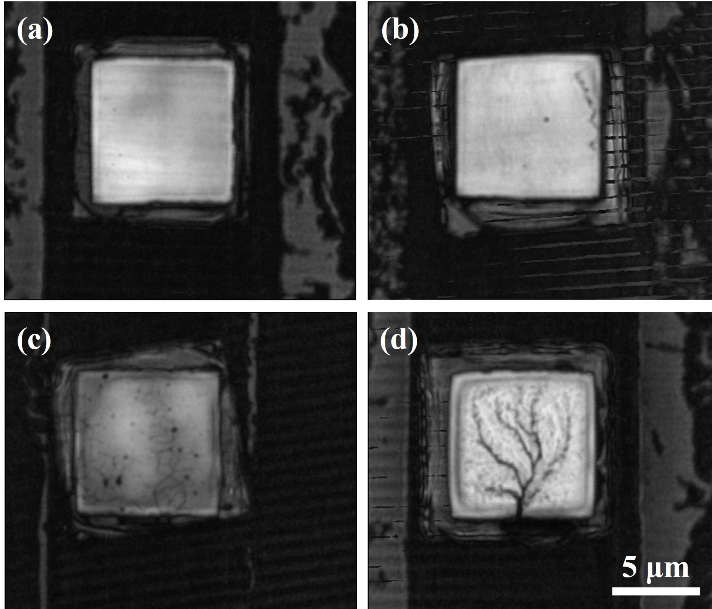

Figure 4.7.: SAM images of sintered (a) Ag paste, (b) Cu paste A, (c) Cu paste B, and (d) Cu paste C

to be noted that hot-mounting was applied to Ag sintered QFN-A1 and QFN-A2, while hot-mounting cannot form preliminary sintering for Cu sintering. Therefore, a tacking agent (TAC-001, Mitsui, JP) containing alcohol(80-99%) and decane(1-20%) was used for the die-mounting process of QFN-C.

Table 4.2.: Die-attach process parameters

		QFN-A1	QFN-A2	QFN-C
Die-attach materials		Ag paste		Cu paste
Paste printing		Manual stencil printing		
Drying		130 °C, 5 mins		
Die-mount	Temperature	130 °C		20 °C
	Pressure	3 MPa		0.1 MPa
	Time	3s		
Sintering	Temperature	250 °C		
	Pressure	20 MPa	10 MPa	20 MPa
	Time	10 mins		
	Atmosphere	1 mbar 5% H_2/N_2		
Cooling		Natural cooling		

The microstructure of dried paste is depicted in Fig. 4.8(a)(b). It can be seen that the Ag paste contained finer nanoparticles (76 ± 28 nm) than the Cu paste (216 ± 72

nm). Figure 4.8(c) shows the samples after die-attach. After die-attach, 50 μm aluminum wires were bonded on the topside for electrical connections. The wire-bonded products subsequently experienced transfer molding and singulation. Consequently, the molded QFN devices were soldered on the test board developed in [25].

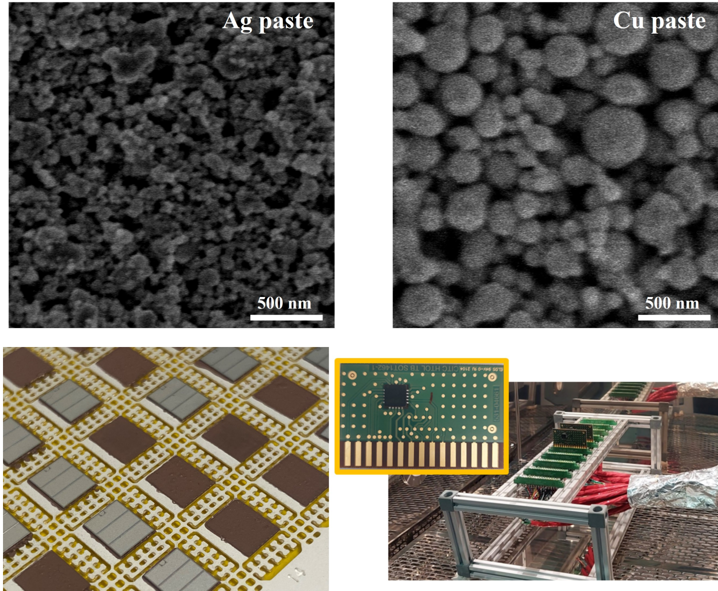

Figure 4.8.: Microstructure of dried (a) Ag and (b) Cu. Samples after (c) die-attach and (d) fully assembled in the online monitoring system.

The test boards were securely placed in the sockets of the online monitoring system in a thermal cycling oven, which can hold a maximum of 10 boards, as depicted in Fig. 4.8(d). Figure 4.9(a) presents the temperature cycling profile (-55 to 150 °C) according to JESD22-A104F standard [30]. One cycle took approximately 45 minutes with a ramping rate of 20 °C per minute. The upper soak time and the lower soak time were defined as the total time that the sample temperature is within -5 °C to +10 °C for the upper soak temperature and +5 °C to -10 °C for the lower soak temperature, respectively. A longer lower soak time was observed around 14 minutes while the upper soak time was around 11.5 minutes.

A schematic of the entire online monitoring system is shown in Fig. 4.9(b). The system can be divided into three primary parts. A user-defined Matlab program synchronized the communications between all instruments. In the temperature trigger part, the oven temperature was perodically feedbacked. Besides, in the transient measurement part, a source-meter unit (SMU) and a digital multimeter (DMM) were employed for pulse generation and fast sampling at 1 kS/s. At last, a multiplexer was employed to allow for sequential measurement.

Figure 4.10 presents a detailed flow chart adopted for the test sequence in this study. At first, when the oven temperature is detected as 25 °C during the ramp up in the cycling,

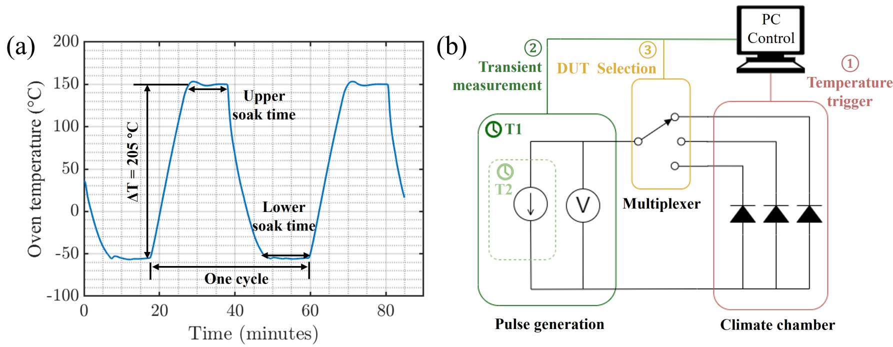

Figure 4.9.: (a) The temperature cycling profile in this study. (b) Schematic of online monitoring circuit system.

data acquisition starts to record the voltage and time. After stabilization of 0.2 seconds, a 0.2-second transient heat pulse was generated by supplying a 1 A current to the body diode. Using a temperature coefficient, the junction temperature of the DUT was therefore estimated according to the change in the forward voltage. Afterward, the data recording continued until the timer T1 reached 5 seconds. Then, the multiplexer switched to the next device, and the exact transient thermal measurement was repeated until all DUTs went through the measurement. Hence, the transient thermal performance of all DUTs was recorded every cycle. The online monitoring stopped when the cycle number reached 500.

4.3.2. IN-SITU THERMAL IMPEDANCE MEASUREMENT

At first, the temperature coefficient of the body diode was calibrated to correlate the forward voltage and junction temperature. As shown in Fig. 4.11(a), four devices were calibrated at various temperatures ranging from -55 °C to 150 °C by a current of 1 A, consistent with the applied current in the heat pulse. An excellent linearity in the voltage change was observed. The temperature coefficient of all devices linearly fit as 2.26 mV/°C.

Figure 4.11(b) shows the voltage measurement at the first cycle for sample QFN-A1. The rapid increase in the voltage is caused by pulse generation. A slight decrease was observed during the pulse period, which would be used to evaluate the thermal performance. At first, abnormal measurement data was detected at the starting phase of the pulse. The electrical turbulence caused this due to rapid change in current. Therefore, a 3 ms offset was applied to avoid the abnormal data caused by the electrical turbulence.

As indicated by the dashed box in Fig. 4.11(b), the voltage drop in the first 0.1 seconds was recorded. 0.1 seconds was chosen based on the result of the structure function in Fig. 4.6. As the heat was ideally assumed to flow vertically, a 0.1-second heat window can reflect the thermal contribution from the Si chip, die-attach layer, and Cu substrate. Hence, the influence of the solder layer beneath the QFN device on the transient thermal measurement can be neglected because the heat flux cannot reach the solder layer within 0.1 seconds.

Subsequently, the voltage drop was translated to temperature difference by applying

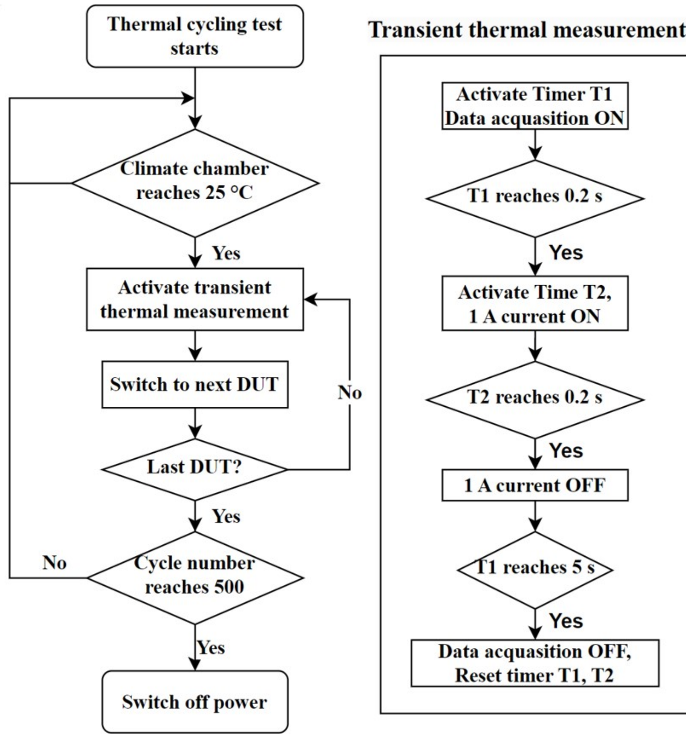

Figure 4.10.: Flow chart of online health monitoring test sequence.

the temperature coefficient of 2.26 mV/ °C. This example calculated the temperature difference ΔT after 0.1 seconds as 0.525°C. Here, the thermal impedance Z_{th} can be expressed as Eq.4.4.

$$Z_{th} = \frac{T_{t+0.1} - T_t}{P_t} \tag{4.4}$$

Where T_t is the temperature after the 3 ms offset, $T_{t+0.1}$ is the temperature after 0.1 seconds and P_t is the power recorded on time t. It should be noted that Eq 4.4 has a similar form as Eq 4.1 but Eq 4.1 describes the cooling phase while Eq 4.4 presents the thermal impedance in the heating phase.

Based on the abovementioned results, the thermal impedance Z_{th} at every cycle is plotted in Fig.4.12 (a-c) for QFN-A1, QFN-A2, and QFN-C, respectively. The fluctuated data can be caused by the measurement errors from the instruments and the oven temperature fluctuations. Therefore, a simple moving average method was applied to facilitate visual interpretation. The 50-cycle moving average was able to smooth most of the data fluctuation and indicate the degradation trends.

Figure 4.12(d) summarizes all samples' 50-cycle moving average results, where a linear fitting was added. After 500 cycles, the thermal impedance increased by 0.02 K/W, 0.03 K/W, and 1.05 K/W for QFN-A1, QFN-A2, and QFN-C, respectively. In the ideal situation,

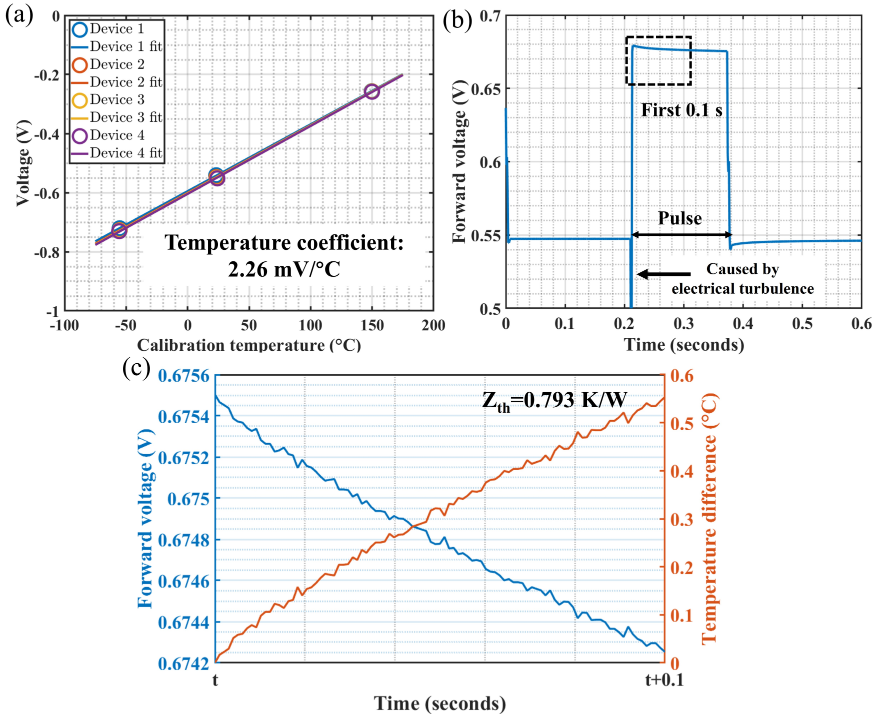

Figure 4.11.: (a) Voltage-temperature calibration of MOSFET. (b) Voltage measurement for QFN-A1 at the first cycle. (c) Voltage and temperature translation as framed in (b).

the thermal impedance has no change according to the ongoing thermal cycling because of a robust die-attach thermal interface. The results stayed relatively stable in the Ag-sintered QFN, QFN-A1, and QFN-A2, while in the case of QFN-C, the measured thermal impedance gradually increased regarding thermal cycling. The abrupt change around 100 and 300 cycles in QFN-A2 can be attributed to system errors because the measured data became stable afterward. The degradation of thermal impedance can be described according to the number of thermal cycles N as the fitting equation below,

$$\begin{aligned} \text{QFN-A1:} \quad & Z_{th} = 3.95 \times 10^{-5} N + 0.79 \\ \text{QFN-A2:} \quad & Z_{th} = 6.80 \times 10^{-5} N + 0.78 \\ \text{QFN-C:} \quad & Z_{th} = 0.0021 N + 1.07 \end{aligned}$$

The slope of the 50-cycle moving average suggested a robust die-attach formed by Ag sintering with a sintering pressure of 20 MPa and 10 MPa. However, a gradual degradation from the first cycle was found in the case of the Cu-sintered QFN-C device. No rapid jump in thermal impedance was recorded in the case of QFN-C. Moreover, regarding zero-hour performance, Ag-sintered QFN-A1 and QFN-A2 held a similar thermal impedance at zero hours, smaller than the value of QFN-C.

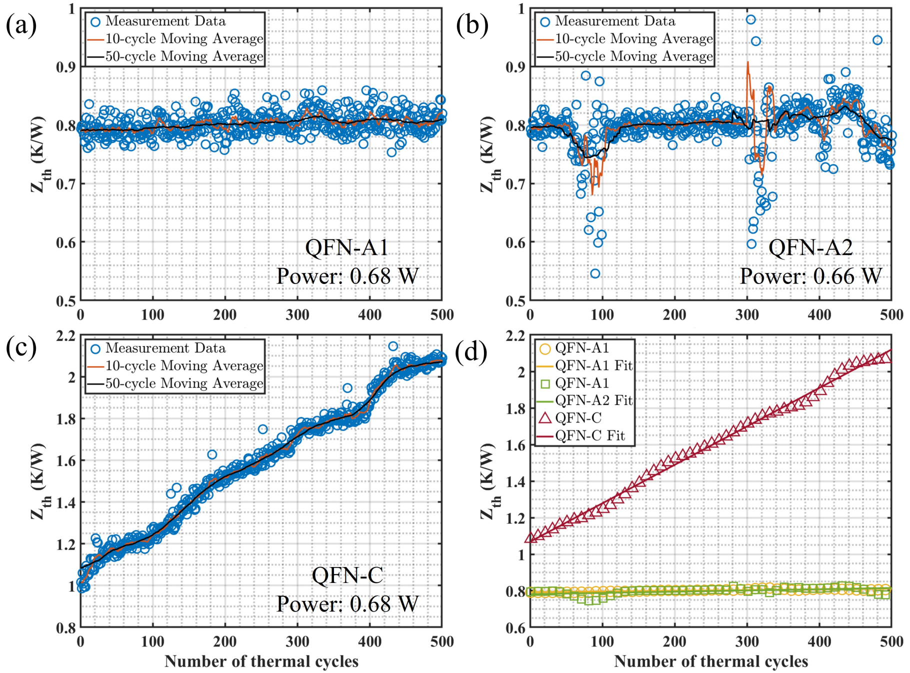

Figure 4.12.: Online thermal impedance monitoring of (a) QFN-A1 (b) QFN-A2(c) QFN-C and (d) fitting of 50-cycle moving average results.

To identify the delaminations before and after 500 cycles of thermal cycling, confocal scanning acoustic microscopy (CSAM) was employed to support the online monitoring results. In this study, no intermediate CSAM images were captured because loading and unloading samples were likely to break the continuousness of measurement. For example, the position of the test board placement and the adsorbed water in CSAM capture can influence QFNs' thermal performance.

The CSAM images before and after thermal cycling are depicted in Fig. 4.13. Dashed rectangles frame the chip positions. At zero hour, good adhesion in all QFN samples is demonstrated by limited indications of delamination. Some degree of delamination can be found on corners, as pointed by arrows, caused by the thermal mechanical stress concentration.

The different thermal conductivity in die-attach materials can explain the difference in zero-hour thermal impedance. The organic tacking agent can be incompletely decomposed and leave a negative influence on the thermal performance. In theory, there is chip variation to make a difference in thermal performance. But in this study, QFN-A1 and QFN-A2 presented similar zero-hour performances. Hence, better thermal conductivity in the Ag sintered die-attach is believed to be the primary reason for a better thermal performance.

Furthermore, the CSAM images after 500 cycles are consistent with the thermal degradation results obtained from the online monitoring. Limited delamination took place

from the corners in QFN-A1 and QFN-A2. Despite slight delamination expansion compared to zero hours, the reflection of the thermal impedance can be limited as there is a negligible increase in 50-cycle moving average curves. This result also indicates a sintering pressure of 10 MPa is sufficient to construct a robust die-attach layer. However, significant large-area delamination was found in QFN-C, which primarily contributed to the gradual increase in the thermal impedance. There were a few potential results for worse performance in Cu-sintered QFNs.

On the one hand, the Cu paste used in this study contained a larger nanoparticle size, nearly triple the Ag nanoparticle size. Therefore, lower sintering quality can be expected since the sintering profile is the same. On the other hand, the treatment of Cu paste involved an organic tacking agent. Due to the close dimension of the Si chip and die-attach area, precise die placement is a must. Therefore, the tacking agent had to be used to prevent die shift during transportation. However, the residual organic can form a poor interface between the paste and the backside metallization layer. The released gas from the organic decomposition during thermal cycling can further deteriorate the interface quality.

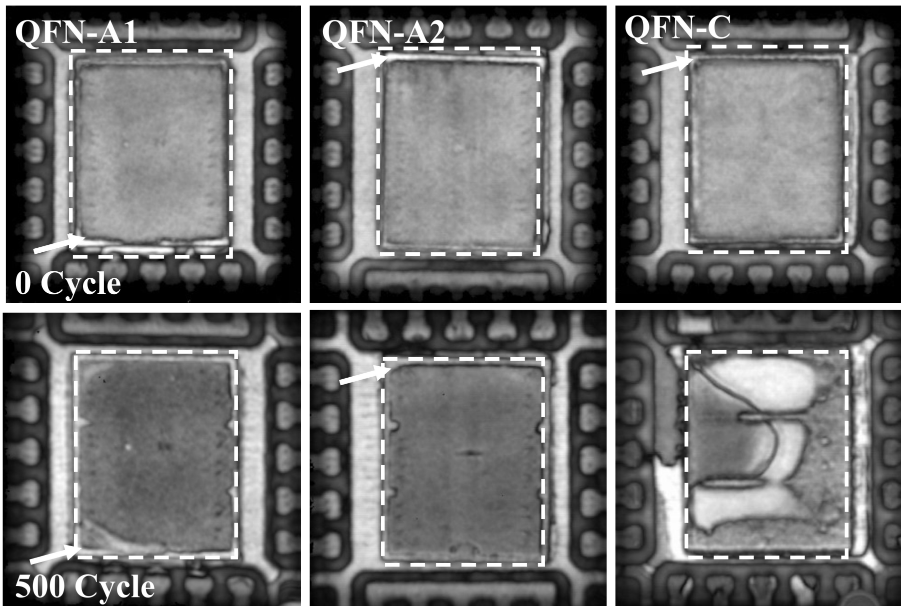

Figure 4.13.: CSAM images before and after the 500 cycles of thermal cycling (The broken line in SAM images shows the outline of Si chips).

In conclusion, in this section, a newly developed online health monitoring technology successfully recorded the thermal performance shift in sintered power devices over 500 cycles of thermal cycling. The thermal impedance calculated from the first 0.1 seconds of a heat pulse was proposed. The health evaluated by the abovementioned methodology is consistent with the delamination results assessed from CSAM images. Thermal robust

die-attach layers formed by Ag sintering has been demonstrated in this study.

4.4. CONCLUSION

In the first part of this chapter, a configurable TTC was applied as a flexible and cost-effective solution for fast thermal evaluation of nano-metallic die-attach joints. The junction-to-case thermal resistance of four different nano-metallic sintered packages were extracted from the separation point of $Z_{\theta JC}$ curves, as well as the SFs. The device sintered using the Ag paste outperformed the devices sintered using Cu pastes A, B, and C. The Ag sinter paste exhibited the lowest θ_{JC} values of 0.144 K/W, and Cu sinter paste A exhibited θ_{JC} value of 0.158 K/W, as determined by $Z_{\theta JC}$ curves. The SAM images were carried out to confirm the consistency of the analysis.

The second part of this chapter discussed the thermal performance degradation over a thermal cycling test. A newly developed online thermal evaluation methodology was employed for online health monitoring of QFNs sintered at 250 °C with nanoparticles (Ag and Cu) and sintering pressure (20 MPa and 10 MPa). The transient thermal performance within the first 0.1 seconds of a heat pulse has been successfully demonstrated to reflect the thermal impedance evolution. The thermal degradation has a high consistency of adhesion results obtained from SAM images. Ag-sintered products presented superior robustness with a 2.5% to 3.8% thermal impedance increase over 500 cycles, while Cu-sintered QFN suffered visible degradation from the first cycle. Besides, the promotion from sintering pressure increase from 10 MPa to 20 MPa could not be distinguished as limited degradation was observed in both cases.

The transient approaches in this chapter allow thermal evaluation of nanoparticles sintered devices in different scenarios. The TTC-assisted offline evaluation enables a flexible design of experiments to screen the optimal thermal resistance of die-attach materials and subject them to further reliability tests. The follow-up online monitoring technology further shortens the evaluation time and removes the requirement for dual interfaces. The self-defined thermal impedance can quickly evaluate the thermal degradation of sintered die-attach layers during device operation.

However, it should be noted that, unlike TDIM, which directly gives junction-to-case thermal resistance, the proposed online thermal monitoring technology needs further promotion to extract more physics properties and standards. Therefore, offline and online thermal monitoring technologies must be flexibly selected for different purposes. Fast thermal evaluations are believed to accelerate the introduction of novel and cost-effective die-attach materials.

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5

Metallic nanoparticles sintered Si TO247 power device

Driven by the strong demand for power electronics, metallic nanoparticle (NP) sintering has been widely investigated for power electronics packaging. Ag sintering technology has been proven as one of promising die attachments. Recently, Cu NP sintering has attracted attention because of its excellent performance and cost-effectiveness. However, reliability is the main challenge inhibiting its application. The present work packaged Si IGBT with Ag and Cu nanoparticles sintered die-attach layers. In addition, on the topside of the power device, both Al wire bonding and ribbon bonding were investigated to improve the reliability. Passive thermal cycling tests were conducted with ΔT = 200 K for 500 cycles. The junction-to-case thermal resistance and IV characteristics show relatively minor differences between the different sintered devices. Furthermore, thermal shock tests with ΔT = 200 K for 1000 cycles were conducted to speed up the aging. Consequently, minor degradation was observed in adhesion, thermal, and electrical performance. Additionally, Finite element method (FEM) simulation was applied to verify the experimental observations. The presented robust reliability performance indicates metallic sintering is a promising solution for TO247 type discrete power device packaging.

Parts of this chapter have been submitted to IEEE transactions of component of packaging materials and technology.

5.1. INTRODUCTION

AG sintering technology has been matured and applied in the power module industry [1]. However, the concern with the migration in the Ag sintered joint leads to the risk in the reliability performance. Besides, considering the high cost of Ag materials, Cu sintering technology shows potential as an alternative with excellent electrical and thermal performance [2]. It has been widely reported that Cu-sintered joints formed at considerable temperatures and pressures exhibit high strength and excellent thermal/electrical conductivity performance [3–6]. But most focus concentrates on the material composition and the process optimization, while the reliability performance of the pressure-sintered power semiconductor has been little investigated [7–10].

Additionally, despite less contribution to the thermal management of the power packages, the topside interconnect in the power electronics package is also essential to the electrical connection. The aluminum bonding techniques, i.e., wire-bonding (WB) and ribbon bonding (RB), have demonstrated excellent reliability performance on an Al-Ni bond system [11]. Furthermore, according to the die topside metallization development, the weldability of Al bonding techniques on the Cu surface has been achieved, while the impact on the reliability performance needs further investigation [12, 13].

In this chapter, we investigated the influence of the backside and topside interconnect on the electrical and thermal performance. Cu and Ag nanoparticles sintering technology was applied for backside die attachment, and thick Al wire and ribbon were bonded on the die topside with a Cu finish. The TO247 package was chosen as a carrier to reduce the system complexity [14, 15]. Two thermal mechanical aging tests were conducted following JESD22-A104 [16] and the temperature difference was extended to accelerate the aging process. Passive thermal cycling tests (TCT) (−50 °C to 150 °C, $\Delta T = 200$ °C) were at first conducted for 500 cycles. Subsequently, thermal shock tests (TST) (−50 °C to 150 °C, $\Delta T = 200$ °C) were executed to speed up the thermo-mechanical aging to determine whether the sintered TO247 packages are capable of withstanding sudden temperature changes. The preliminary reliability results indicate that heavy Al wire and ribbon are viable options for the Cu metalized Si IGBT. Additionally, Cu sintering technology is proven to be a potential alternative to Ag sintering technology in power electronics packaging by exhibiting limited performance degradation. The reliability results were consistent with the FEM results, as the observed delamination initiated at the simulated stress concentration region. This work suggests great thermal-mechanical reliability performance of sintered die-attach and thick Al interconnect in TO247 packages.

5.2. EXPERIMENTAL METHODOLOGIES

5.2.1. MATERIALS AND PROCEDURE

Figure 5.1 shows Si power IGBT dies (TRENCHSTOP^{TM} IGBT7, 1200V/50A) from Infineon and Cu TO247 leadframe with Ag coating. The die size of the Si IGBT was 6.15 × 6.70 mm^2. The backside of the die is metalized with NiAg system while the topside metallization is plated by 4.4 μm Cu. One commercially available Ag sinter paste was chosen as a reference. Two Cu sinter pastes that are under development from different vendors were used in this study for comparison. In this study, the materials are named *Ag paste*, *Cu paste A*, and *Cu paste B*.

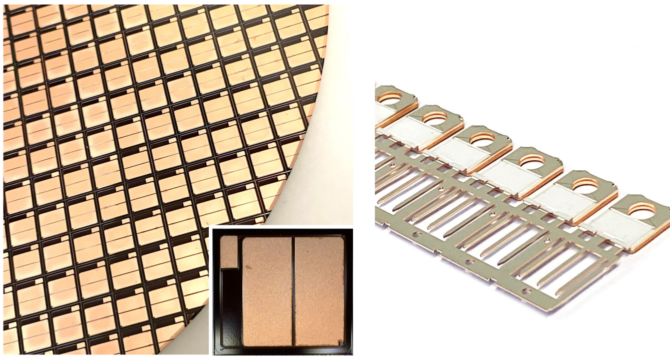

Figure 5.1.: Si IGBT (left) and TO247 leadframe (right) used in this chapter

Figure 5.2 presents the entire assembly process. To reduce the complexity of the study, all sinter pastes went through the same process flow and shared the same sintering profile.

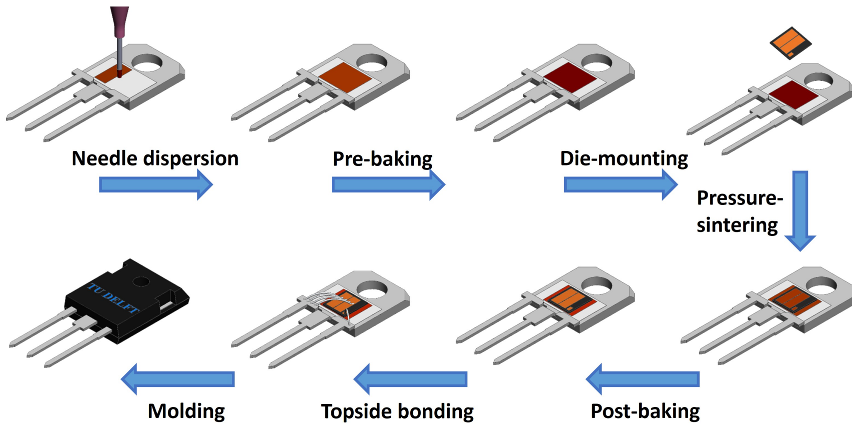

Figure 5.2.: Fabrication process flow for a TO247 discrete device

The sintering paste was first dispensed by a modular micro-assembly station (Häcker Automation GmbH, Germany), which was able to control the amount of material in a single dispersion. Then, the samples were baked in the air for 10 minutes at 110 °C to evaporate the organic solvents. Afterward, the chip was mounted on the top surface of the dried paste, and pressure-assisted sintering was implemented by a FinePlacer Lambda die-bonder (FineTech GmbH, Germany). A 100 μm Teflon foil was put between the sample and the sintering tool to avoid tool contamination.

The adopted sintering profile is described below. The whole sintering process was conducted with a formic acid flow. The sintering temperature ramped to 280 °C and dwelled for 10 minutes. A 9 MPa sintering pressure was set for 5 minutes, applied when the temperature entered the dwelling stage. Afterward, the sintering tool was lifted to

expose the Cu top surface for 5 minutes. Ultimately, all sintered samples were placed in a reflow oven for 1 hour post-annealing at 280 °C. The formic acid was introduced in the first 12 minutes, and the remaining time was in a vacuum environment. This additional post-annealing process was intended to reduce the chip top surface for further topside bonding. Samples that were sintered with different pastes are shown in Fig. 5.3(a).

Regarding the topside bonding, two kinds of topside interconnects were chosen on the Cu paste A sintered samples (Fig. 5.3(b)). Heavy Al wires with a diameter of 200 μm were bonded with an ultrasonic power of 12 W. The bonding time was 0.5 seconds, and the applied force was 3.5 N. To reduce the power density on the individual wire, 4 Al wires were bonded on one sample. In addition, heavy Al ribbons with a width of 500 μm and a thickness of 100 μm were bonded with 8 W ultrasonic power and 3 N for 0.5 seconds. Due to the limited area on the lead, only 2 ribbons were bonded on one sample. The other samples sintered with *Ag paste* and *Cu paste B* all received the Al wires as topside interconnect.

Finally, all samples were molded and singluated in Boschman Advanced Packaging Technology B.V. with a standard process for TO247 packages. Fig.5.3(c) shows the molded sample for the further reliability test. A corresponding 3D geometry was constructed for FEM simulation. The cross-section and thickness of each layer in the constructed 3D geometry model is shown in 5.3(d).

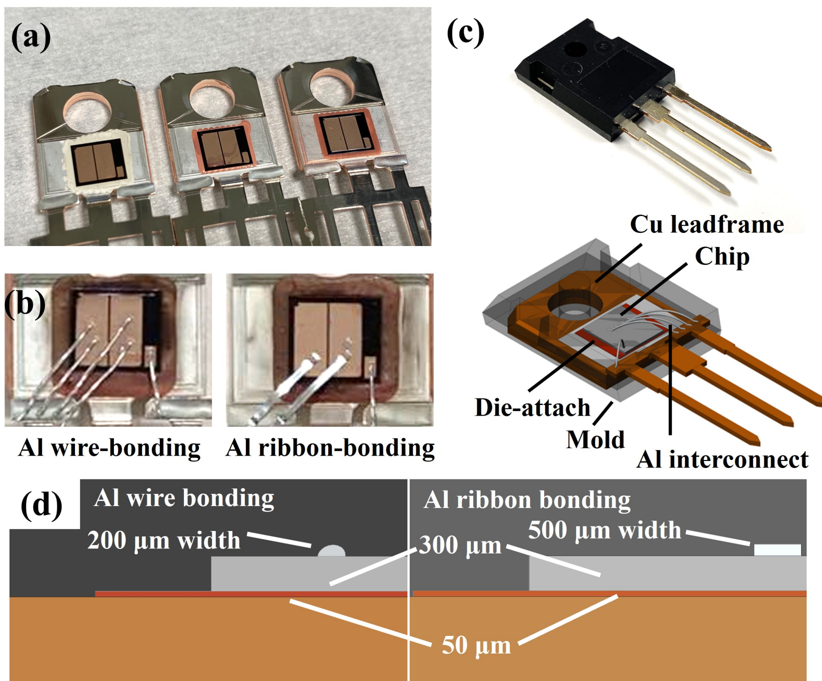

Figure 5.3.: Image of samples with (a) Various backside interconnects, (b) Various topside interconnects, (c) Schematic of molded TO247 sample and the constructed geometry model for FEM simulation, (d) Thickness of each layer in the constructed geometry model.

5.2.2. THERMAL AGING TEST CONDITIONS

The molded sample was exposed to a TCT and, subsequently, TST. Fig. 5.4 presents the temperature evolution in the TCT and TST.

The TCT was conducted in a Tenney Junior temperature test chamber (Thermal Product Solution, US). 500 cycles of passive thermal cycling were carried out with ΔT = 200 °C (−50 °C to 150 °C). The ramping rate was 5 °C/min, and the soak time was 10 minutes. Therefore, the total time of one cycle is 100 minutes. There was no intermediate status observation during the TC test.

The TS test was conducted in a temperature aging system (Weisstechnik, ShockEvent T/60/V2) for 1000 cycles of passive thermal cycling with ΔT = 200 °C (−50 °C to 150 °C). The switching time between the hot and cold chambers was approximately 1 minute. The soak time in both chambers is 15 minutes. Therefore, one TS test cycle takes around 30 minutes. Samples were taken out for measurement every 200 cycles.

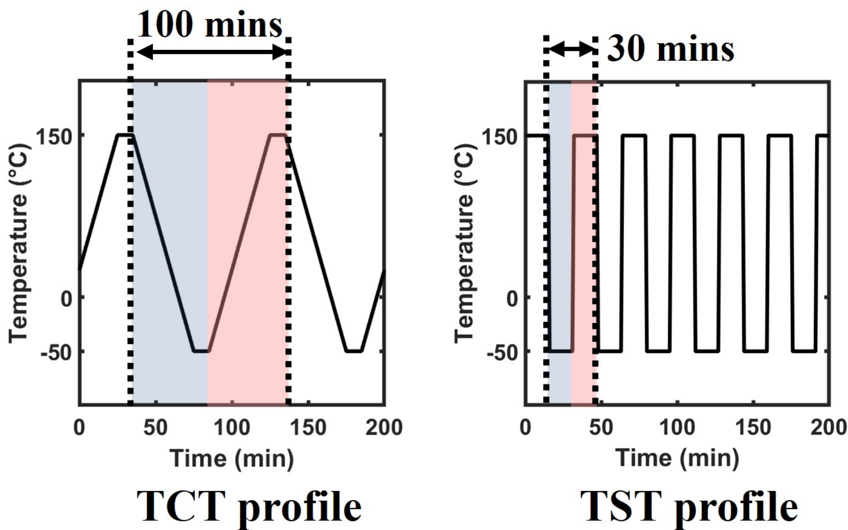

Figure 5.4.: Temperature profile for TCT (left) and TST (right). The red and blue areas represent the heating and cooling duration.

5.2.3. DEVICE CHARACTERIZATION METHODOLOGIES

The quality of the die-attach layer was observed by scanning acoustic microscopy (SAM, SAM 400, PVA TePla) to inspect the void propagation. The microstructure pre- and post-thermal aging were checked by an SEM (XL30 SFEG, Thermo Fisher Scientific).

Regarding thermal performance, temperature sensitivity parameter (TSP) calibration was first carried out to estimate the junction temperature, T_j. The calibration was done in a temperature chamber from 25 °C to 105 °C with gate-emitter voltage (V_{ge}) = 15 V and collector-emitter current (I_{ce}) = 50 mA and 100 mA. A linear relationship was fit-

ted between collector-emitter voltage (V_{ce}) and temperature, as shown in Fig. 5.5. The slopes of the fitting lines are considered as TSP, which were 0.002 V/K.

Besides, the TDIM was conducted according to the JEDEC 51-14 standard [17]. Two interface materials with different thermal conductivity (thermal grease and ceramic foil) were applied at the interface between the DUT and the cooling element. The test sequence is presented in Fig. 5.5. The device was entirely switched on with 15 V V_{GE}. Then, the device was heated up with 40 A I_{CE}. The junction temperature was considered in equilibrium after 10 seconds of heating up. Afterward, the power was cut off, and data acquisition was activated after a 400 μs delay, which was applied to skip the electrical turbulence that occurred when the power was switched off. The junction-to-case thermal impedance $Z_{\theta JC}$ is expressed as Eq. 5.1.

$$Z_{\theta JC}(t) = \frac{T_J(t) - T_J(t=0)}{P_H} \tag{5.1}$$

Where P_H is the constant power dissipated by the DUT at $t = 0$ before switching off the load current. $T_J(t)$ is the time-dependent junction temperature estimated by TSP.

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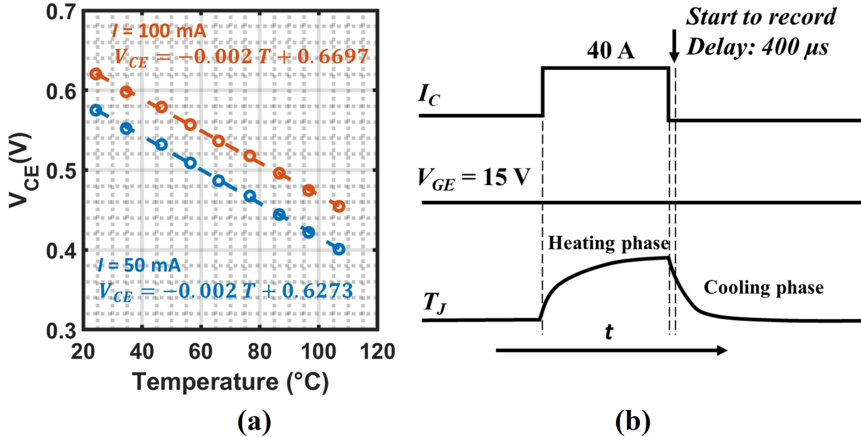

Figure 5.5.: (a) Temperature sensitivity parameter calibration with V_{ge} = 15 V; (b) The sequence of heating and measuring the cool-down curve.

To quantitatively analyze the thermal performance, junction-to-case thermal resistance θ_{th-jc} is extracted for a quantitative description of their thermal performance. In this case, the thermal dissipation was considered completely vertical from the powered device to the Cu leadframe. Therefore, the thermal conductivity difference in the thermal interface caused the separation of the thermal impedance curves. The separation point is then regarded as the θ_{th-jc}, representing the sum of the thermal resistance from the junction to the case surface. A schematic is shown in Fig. 5.6. Z_{th} is the measured thermal impedance.

In addition, the IV characteristics was measured after certain thermal cycles to record the performance degradation. A 15 V V_{ge} was applied to switch entirely on the devices.

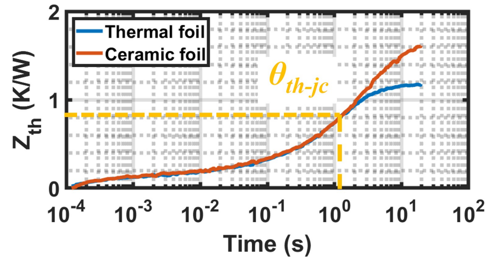

Figure 5.6.: Determination of the junction-to-case thermal resistance, following the TDIM method.

The IV characteristics were measured until I_C reached 50 A. The resistance at I_C = 50 A was identified as the effective electrical resistance, and the corresponding voltage was determined as the saturation voltage V_{cesat}.

5.3. THERMAL CYCLING TEST PERFORMANCE

Figure 5.7 shows the SAM results on the initial and aged die-attach layer. Dashed rectangles frame the chip positions. Evident traces can be observed in all samples caused by the needle dispersion method. This is because the rectangle pattern was formed by line scanning. Every scanning of the needle slightly overlapped the previous printed line, leaving more materials at the boundaries. Unlike conventional solder, the surface non-uniformity in the dried sinter paste can hardly be eliminated in the sintering process. Therefore, the contrast difference was made by the locally uneven materials. However, we found that in all samples, no observable voids were generated during the TCT.

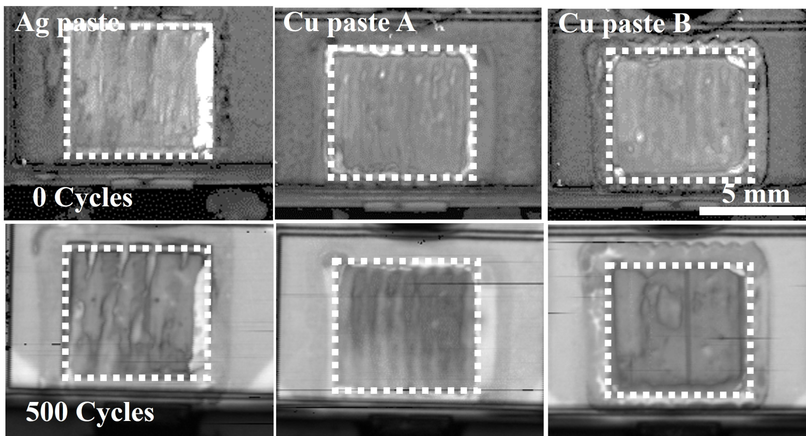

Figure 5.7.: SAM images before and after the TCT. The dashed line in SAM images shows the outline of Si chips.

Moreover, the cross-section of samples was inspected. The bondline thickness is 23.3 μm, 26.9 μm, and 30.2 μm for the sample sintered by *Ag paste*, *Cu paste A*, and *Cu paste B*, respectively. To observe the difference between Ag and Cu sintered die-attach layer, *Ag paste* and *Cu paste B* sintered samples, both unaged and aged, are presented in Fig. 5.8. A dense Ag sintered layer was observed with sufficient inter-diffusion to the Ag metallization layer, resulting in a seamless interface between the substrate and the die-attach layer. Furthermore, the *Cu paste B* sintered sample exhibits a highly sintered cross-section. No evident delamination at the interface and big cracks were found before and after the thermal aging test.

Thus, no evident degradation in the microstructure was made during the 500 TCT cycles. The contrast change in the Cu sintered product can be correlated to the preparation artifact as evident dispersion lines. The void region at the edges shows no evident expansion. The Ag and Cu sintering technology is demonstrated to form a reliable interface to the Ag metalized substrate.

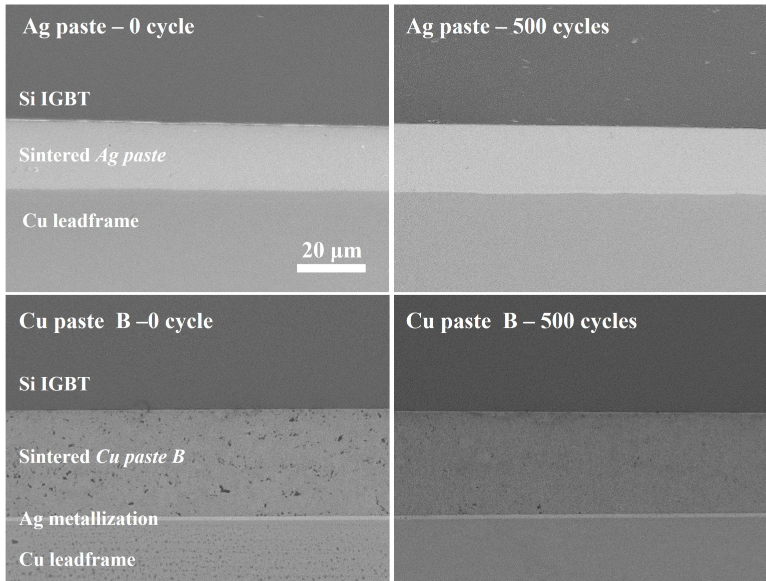

Figure 5.8.: Cross-section image of unaged and aged samples that were sintered by *Ag paste* and *Cu paste B*.

Fig. 5.9 presents the thermal impedance curves before and after the TCT with thermal grease as the thermal interface material. The separation point of each group is relatively close. Therefore, the data with one thermal interface was plotted to compare the crossing of different groups. In the plots for ribbon-bonded and wire-bonded samples, it can be seen that the two curves overlap in unaged and aged samples. While the influence of the topside interconnects on thermal management is less critical than that of the backside die-attach layer, the heavy Al interconnect on the Cu surface demonstrates limited degradation after 500 cycles of the TCT. The suitable interconnect's robustness can be partially attributed to its large cross-sectional area and high thermal conductivity.

In terms of the backside interconnect, the thermal impedance curve of samples sintered with *Ag paste*, and *Cu paste A* slightly differ, while the difference does not get larger after 500 cycles. However, the *Cu paste B* sintered sample shows a significantly higher thermal impedance than the other samples, indicating worse thermal performance.

The θ_{th-jc} of all samples is summarized in Table ??. It can be seen that no degradation in the thermal performance was observed. In contrast, the θ_{th-jc} of all groups was promoted after 500 aging cycles. Further sintering in passive thermal cycling can explain this. In addition, θ_{th-jc} measurements could be slightly affected by other factors, such as the mounting force and the position of the thermal element for the case temperature measurement.

However, the measured θ_{th-jc} shows a minor difference between Al wire and Al ribbon before and after thermal cycling. All samples show excellent thermal performance in terms of the backside sintered die-attach layer. The Ag sintered sample performed slightly better than the Cu sintered samples.

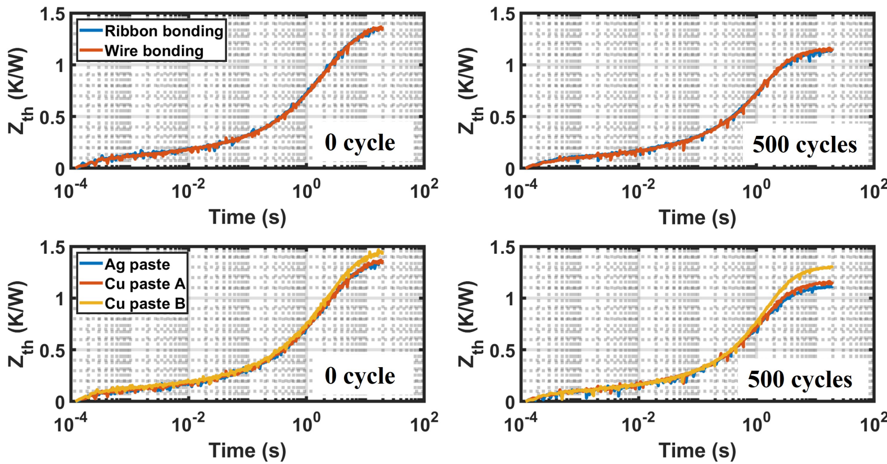

Figure 5.9.: Thermal impedance curves before and after the thermal cycling test with thermal grease as thermal interface material.

Table 5.1.: Junction-to-case thermal resistance before and after thermal cycling test (unit: K/W)

Position	Materials	Junction-to-case thermal resistance		
		0 Cycle	500 Cycles	Deviation (%)
Topside	Al wire	0.868	0.807	-7.02
	Al ribbon	0.882	0.811	-8.05
Backside	Ag paste	0.863	0.779	-9.73
	Cu paste A	0.868	0.807	-7.02
	Cu paste B	0.901	0.828	-8.10

The shift in IV characteristics is shown in Fig. 5.10, and the deviation near the region

of I_C = 50 A is zoomed in the inserted frame. Consistent with the transient thermal performance, no significant degradation was found in all samples. However, the curve of most samples shifted towards better electrical conductivity instead.

The effective resistance of the samples was therefore recorded in Table ??. It can be seen that the deviation between the performance before and after the TCT is minor, around 1%. This minor promotion is negligible because of the measurement error.

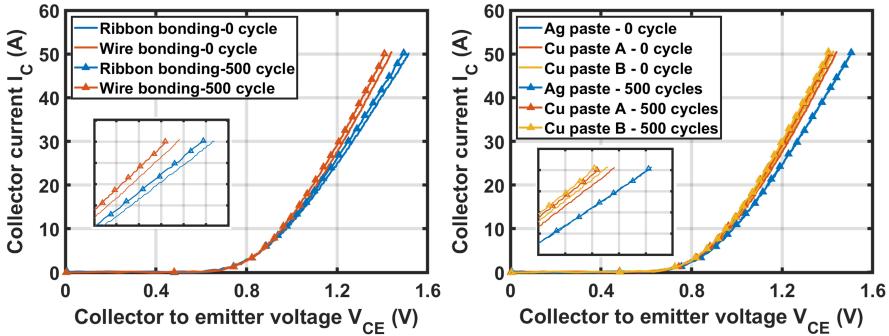

Figure 5.10.: IV characteristics before and after the thermal cycling test at room temperature.

Table 5.2.: Effective resistance before and after thermal cycling tests (unit: mΩ)

Position	Materials	Effective resistance		
		0 Cycle	500 Cycles	Deviation (%)
Topside	Al wire	28.5	28.1	-1.4
	Al ribbon	30.2	29.8	-1.7
Backside	Ag paste	29.7	29.9	-0.7
	Cu paste A	28.5	28.1	-1.4
	Cu paste B	28.2	27.8	-1.4

In terms of topside interconnect, the Al wire outperforms the Al ribbon in this study in terms of electrical performance. It can be attributed to the difference in equivalent cross-sectional area, with the wired sample having an equivalent cross-sectional area of 0.13 mm^2, compared to a slightly smaller area of 0.1 mm^2 for the ribbon bonded sample. The equivalent resistance of the wire-bonded sample is 28.1 mΩ, while the value for a ribbon-bonded sample is 29.8 mΩ. As for the backside interconnect, two aged Cu paste sintered samples present close performance as 28.1 mΩ and 27.8 mΩ, respectively, slightly better than the Ag sintered sample.

Therefore, it is found in this study that the Ag sintered sample shows better thermal performance while slightly lower electrical performance. Besides the process-related thickness variation, it could also be attributed to the interface between the die-attach layer and the chip backside Ag metallization, as well as the interface between the die-attach layer and the substrate Ag finishing. Thus, the Ag-sintered samples eventually

formed an all-Ag joint, while a heterogeneous Cu-Ag interface existed in the Cu-sintered samples. The interface impedance is reported to play an essential role in transient thermal impedance [18]. However, in the case of electrical performance, the existence of a hetero-interface is less significant for thermal performance.

5.4. THERMAL SHOCK TEST PERFORMANCE

The abovementioned TCT results showed limited thermal and electrical degradation. TST with the same temperature difference was carried out for another 1000 cycles to accelerate the failure. Figure 5.11 depicts the SAM image evolution of different sintered joints during the 1000 cycles. Each column represents one kind of sinter paste. The SAM images of 0, 400, 800, and 1000 cycles were recorded. The dispersion needle imprints were that much for *Cu paste B*, which was attributed to the viscosity difference.

The SAM results show *Cu paste A* and *B* resulted in good adhesion. No drying channels or evident delamination were observed. However, partial delamination was observed in the *Ag paste* and *Cu paste A* sintered sample, starting from the die-attachment's edge. Unlike the results in TCT, in a more extreme aging environment, the defects caused by the needle dispersion became the weak point to nucleate the cracks, as indicated by the arrows.

Figure 5.12 plots the thermal impedance change during the TST to investigate the thermal degradation. The data was obtained with an isolation foil as a thermal interface material. It shows no significant degradation over 1000 cycles despite void propagation in the Ag paste sintered sample. The environment and sample re-mounting could cause a slight difference in the thermal impedance curves. Therefore, both backside and top-side interconnects show good resistance to the TST.

To confirm the thermal impedance results, The evolution of θ_{th-jc} of all samples is summarized in Fig. 5.13. Although the same measurement methodology was applied, the absolute number of the θ_{th-jc} is smaller than the values in Table **??**, which the estimation error on the T_j could cause after deducting the electrical disturbance region. Focusing on the value evolution over thermal aging, the results are consistent with the thermal impedance curves. The value at 600 cycles is little higher, which is also observed in the thermal impedance. In general, the value of θ_{th-jc} presents no degradation in the thermal performance.

Figure 5.14 plots the IV characteristics evolution during the TST for different backside and topside interconnects. The effective resistance at each 200 cycles was calculated as marked in triangles in the figure. The IV characteristic curves only slightly vary during the TST, indicating a low level of electrical degradation. The value of the effective resistance fell in a range between 28 and 30 mΩ. The chips natural process variation in forward voltage drop is visible in the different samples. The electrical conductivity experienced a slight improvement during the TST in all groups, which fell into the measurement error range. Thus, the thermal stress generated in the TST may not cause destructive damage to the Al-Cu hetero-interface on the chip topside. It can be found that even the *Ag paste* sintered product exhibited non-noticeable electrical degradation, although void propagation was found in SAM images. It implies that the large bonding area makes electrical performance less sensitive to the backside sintered interconnect.

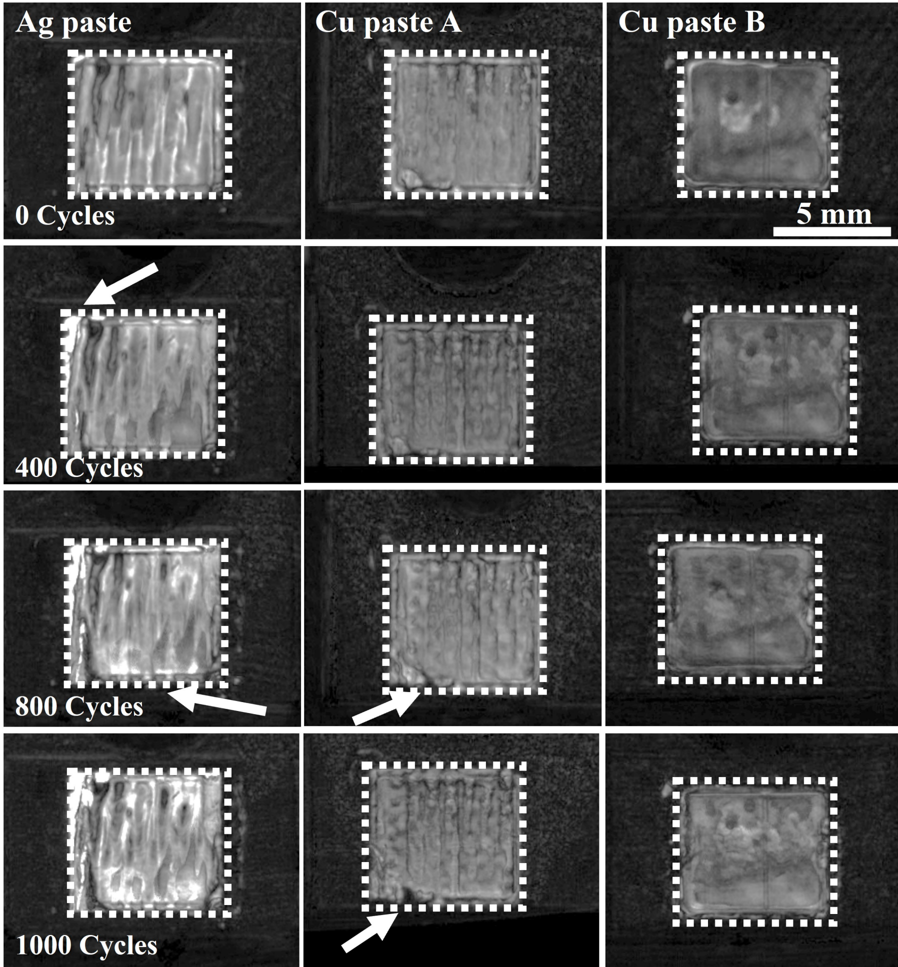

Figure 5.11.: SAM images at 0, 400, 800, and 1000 cycles of the TST. The dashed line in SAM images shows the outline of Si chips.

5.5. VON MISES STRESS DISTRIBUTION SIMULATION

The TST experiments were simulated by using ANSYS Mechanical 23.1. The geometry model is shown in 5.3(c)-(d). Transient FEM simulations of one cycle of the TST (Fig. 5.4) were performed and the stress in the backside interconnects and topside interconnects were estimated at the end of the low temperature phase after one cycle. Different materials were assigned to the different bodies as indicated in the Fig. 5.3(c). The long terminals and the leadframe are copper, the die is silicon, the wires and ribbon are aluminum, and the external mold is epoxy. In the simulations, the thermal load of the experiments was applied simultaneously to all the bodies, and the geometry was constrained at three points to prevent rotations of the whole system but to allow deformations in all

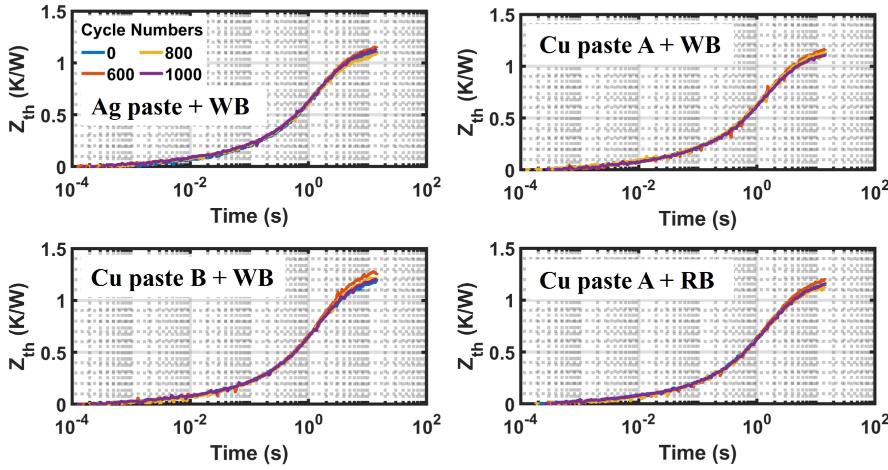

Figure 5.12.: Thermal impedance curves over the TST for different backside and topside interconnects with thermal grease as thermal interface material.

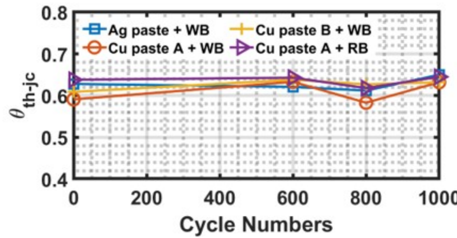

Figure 5.13.: The summary of the θ_{th-jc} evolution over 1000 cycles of TST.

directions.

The mechanical properties of these materials were depicted in the Table 5.3 below. Materials except die-attach materials are all considered purely elastic. Materials except the die-attach materials are all considered purely elastic. A viscoplastic constitutive Anand model is adopted for the sintered Ag and sintered Cu die-attach layer from previous studies [19, 20].

A fully conformal mesh was generated for the whole geometry with approximately 0.4 million nodes as shown in Fig. 5.15. In this study, the von Mises stress was simulated to analyze the stress distribution at the end of the cold phase after the first cycle. Mesh convergence was checked by comparing the equivalent von Mises stress in the die-attach layer obtained with different mesh refinements and the coarsest mesh providing convergent results was chosen for further simulations.

Figure 5.16 visualizes the von Mises Stress distribution of the package at the end of the low-temperature phase after one thermal aging cycle. Stress concentrations were found at the corners of the Si chip, as indicated by the arrows. The leading cause is the CTE mismatch because the thermal transient time was relatively short compared to the

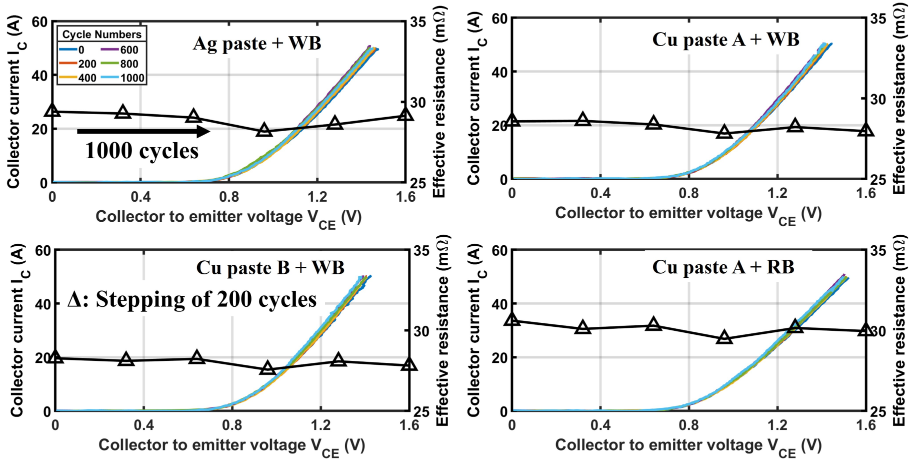

Figure 5.14.: The IV characteristics and effective resistance of different backside and topside interconnects at 0, 200, 400, 600, 800, and 1000 TST cycles. Triangle marks present effective electrical resistance at $I_c = 50\ A$ evolution over 1000 TST cycles.

Table 5.3.: Thermo-mechanical properties of the materials used in the simulation [11, 19, 21, 22].

Materials	Elastic modulus [GPa]	Poisson's ratio	CTE [10^{-6}·K^{-1}]	Thermal conductivity [W·mK^{-1}]	Specific heat [J·$kg^{-1}K^{-1}$]	Density [kg/m^3]
Cu lead-frame	120	0.34	16.8	33.	385	8900
Al inter-connect	64	0.3	25	238	920	2680
Si IGBT	130	0.28	2.6	156	703	2330
Epoxy resin	16.5	0.3	19	0.75	800	1820
Sintered Cu	/	0.34	17	180	/	5100
Sintered Ag	/	0.31	21.1	430	/	6924

dwelling stage (15 mins). Therefore, there is a negligible temperature gradient along the vertical structure. The maximum stress in the case of a Cu-sintered joint is 1016.1 MPa, while the value in an Ag-sintered joint is slightly larger, as 1047.6 MPa. This difference is expected because sintered Cu joints have a lower CTE mismatch than sintered Ag joints. Therefore, the corner areas will likely have cracks initiated due to thermal fatigue, which is consistent with the SAM observation in Fig. 5.11.

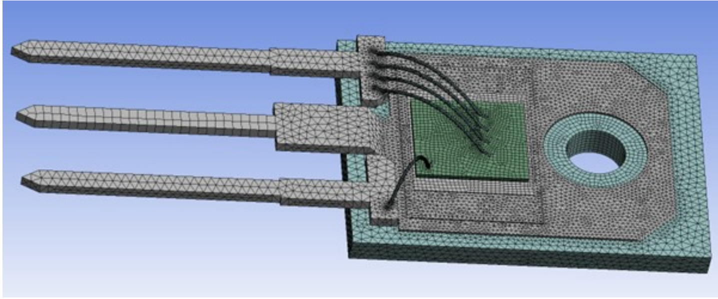

Figure 5.15.: Mesh used for transient simulations. The mold top cover is taken into account but hidden for the sake of representation.

Regarding the topside interconnect, some stress concentration in the heels was observed in both Al wire bonding and ribbon bonding, as shown in Fig. 5.16. The topside bonding tolerated a higher von Mises stress with a more central position. Compared to the stress concentration at the corners of the silicon, the stress concentration at the topside bonding is much smaller. It is because of the passive thermal swing rather than active heating from the Si chip. Reflecting on stress distribution on the Si chip, the ribbon-bonded sample resulted in slightly larger von Mises stress at the corners of the Si chip, indicating a slight influence on the die-attach layer.

As the CTE mismatch between the Al interconnect and Si die is fixed, the difference in stress amplitude highly depends on the total adhesion area and cross-section area. As calculated before, the total cross-section area of the wire-bonded device is larger than the ribbon-bonded device despite it having a larger total adhesion area (0.66 mm^2) than the wire-bonded device (0.48 mm^2). This stress relaxation in the different topside interconnected samples is consistent with the abovementioned electrical measurement results in Fig. 5.10, where a lower effective resistance was measured in the wire-bonded sample. Thus, a conclusion can be drawn that a larger cross-section of the topside interconnects could enable a more stress-relaxation structure by conducting more heat away.

5.6. CONCLUSION

In this study, we fabricated TO247 Si IGBT devices with three different sintered backside die attachment and two types of thick Al topside interconnects on Cu metalized pads. 500 cycles of passive thermal cycling (−50 °C to 150 °C, $\Delta T = 200$ °C) and 1000 cycles of thermal shock (−50 °C to 150 °C, $\Delta T = 200$ °C) were further conducted to investigate the reliability degradation. All samples presented excellent electrical and thermal performance. Ag and Cu paste sintered backside interconnect demonstrated great reliability with respect to the thermal stress accumulated during the passive thermal mechanical aging. The thick Al wire and ribbon bonded topside interconnect in the passive thermal cycling also demonstrated good reliability performance. The following conclusions were obtained:

(1)) Sintered TO247 packages were fabricated with bondline thickness ranging from

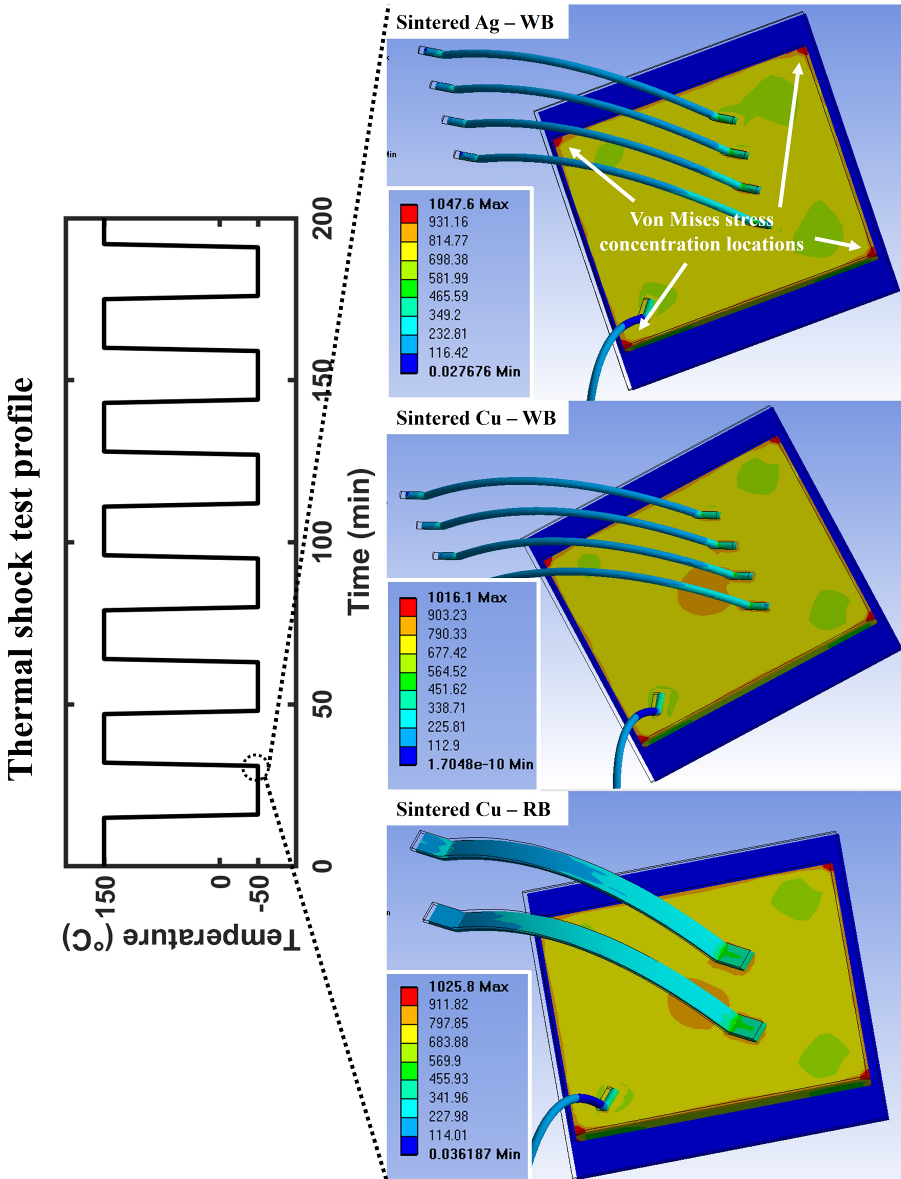

Figure 5.16.: Von Mises Stress (in MPa) distribution of different sintered packages after one cycle of the thermal shock test. From top to bottom is the combination of Ag sintered device with wire-bonding, Cu sintered device with wire-bonding, and sintered Cu device with ribbon bonding.

23.3 μm to 30.2 μm. Uneven material distribution was found due to the dispersion method. However, no evident voids and cracks were found in the *Cu paste A*& *B*

sintered product. Evident void generation and propagation were observed in the Ag sintered product in TST aging developed from the defects caused by dispersion.

(2) The transient thermal impedance of samples bonded by heavy Al wires is close to that of heavy Al ribbons. The difference between the *Ag paste* sintered sample and the *Cu paste A* sintered sample is also minor. In addition, θ_{th-jc} was extracted over both thermal aging tests. The variation of θ_{th-jc} is not apparent thanks to the high thermal conductivity of Ag and Cu paste. Despite weak delamination at the edge regions, TCT and TST aging posed a negligible influence.

(3) Despite similar thermal performance, the effective electrical resistance of samples bonded by heavy Al wires is smaller than that of heavy Al ribbons. Regarding different sinter pastes, both *Cu paste A& B* sintered samples performed better than the *Ag paste* sintered sample. The reliability test neither enlarged nor eliminated the gap in the effective resistance.

(4) Transient FEM simulations revealed the stress concentration at the corners of the Si chip as well as at the heterogeneous interface of the topside interconnect. The simulation results are consistent with the experimental characterization. The corners of the Si chip concentrated much higher thermo-mechanical stress, which may induce failure initiation. Additionally, heavy Al wires resulted in a more stress-relaxation structure because of a larger total cross-section area.

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6

METALLIC NANOPARTICLES SINTERED HERMETIC PACKAGE

Driving by the increased demand for hermetic packaging in the More than Moore roadmap, a Cu nanoparticle sintering-enabled hermetic sealing solution was developed with a small-size sealing ring. The developed technology simplifies microfabrication and requires less surface roughness using a sinterable Cu nanoparticle paste. A 50 *µm size Cu paste sealing ring was achieved using a lithography patterned photoresist as a stencil mask. A groove-structured chip was used to amplify localized stress. The Cu nanoparticle paste was fully sintered at* 300 *°C under pressure ranging from* $10 MPa$ *to* 40 *MPa resulting in a robust bonding with a maximum shear strength of* 280 *MPa and implementing hermetic packaging. The deflection of the Si diaphragms estimated a vacuum level of* 7 *kPa. Vacuum sealing was maintained for over six months, and the lowest leak rate was calculated as* 8.4×10^{-13} *Pa·m*^{3}*/s. The developed technology that comprises small-size patterning and pressure-assisted sintering offers the potential for a simple, cost-effective, but robust solution for hermetic packaging.*

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6.1. INTRODUCTION

IN the concept of More than Moore (MtM), the non-digital functions, including radio frequency (RF), power and sensors, will be the focal point of future commercial prospects [2]. Notably, microelectromechanical systems (MEMS) often require a hermetic environment to realize the appropriate sensitivity and performance. In addition, capping the sensitive components in a vacuum environment guarantees their reliability. On the path to a high integration density on a single chip, a cost-effective and precise hermetic packaging solution for MEMS sensors is a significant challenge.

As a critical part of hermetic packaging, the bonding technology can be categorized by the presence or absence of an intermediate layer bonding [3]. The bonding technology without an intermediate layer comprises anodic bonding and direct bonding. The process involves high voltage and high temperature (>1000 °C), respectively, which pose challenges to the stability of components [4, 5]. The bonding technology with an intermediate layer can also be divided into a non-conductive intermediate layer, such as glass frit bonding [6], and a conductive metal-based intermediate layer.

Metallic bonding techniques, as widely used in hermetic seal methods, include solder bonding, eutectic bonding, solid-liquid inter-diffusion bonding (SLID), surface-activated bonding and thermo-compression bonding. However, solder and eutectic bonding have disadvantages because the melting of solder alloys can cause reflow concerns. The sealing ring widths frequently exceed 100 μm in meeting the required hermeticity and bond strength [7, 8]. SLID bonding technique can result in the formation of voids in the intermetallic compound layer and therefore requires extra considerations, e.g. the sealing layer thickness and temperature profile [9]. Surface-activated bonding permits sealing at room temperature. However, substrates' surface planarity and roughness requirements are very stringent [10]. Thermo-compression bonding utilizes high temperature and pressure and has been demonstrated with metals like Al [11] and Cu [12].

Over the last decade, metallic nanomaterial sintering technology, represented by Ag and Cu, has been reported in the heterogeneous integration application of 3D-IC integration, e.g. chip-to-chip, wafer-to-wafer and wafer bonding, achieved by dip-transfer and direct printing methods [13–15]. Recently, few attempts have been made to apply nanomaterial sintering in a hermetic package. It has been reported that sinterable Ag film can implement hermetic sealing through thermo-compression and electric-assisted sintering [16, 17]. However, the hermeticity degradation over time has been reported, and the application of sinterable metal film increases the cost unless used as a fine sealing ring.

This chapter proposes a hermetic sealing solution using Cu nanoparticle sintering with a 50 μm size sealing ring. The sealing ring was patterned through lithographically defined stencil printing [18]. Hermeticity was achieved in a Si cavity on an Au-finished Si substrate. Multiple sintering profiles were studied to investigate the feasibility of hermeticity and bonding strength. Analysis of the fracture surface subsequently revealed the mechanism of hermeticity. Finally, the deflection of the Si diaphragm was recorded over six months, and a relatively low leak rate was demonstrated.

6.2. DESIGN AND MICROFABRICATION

6.2.1. GEOMETRY DESIGN

A simple two-chip test hermetic package was built for proof of concept (Fig. 6.1). A thin diaphragm with a dimension of 4 × 4 mm and thickness of 50 μm was created in the top component. Thus, the interior cavity pressure could be measured by its deflection. Furthermore, a groove structure was designed in the bottom component to create nonuniform stress over the sealing ring area. Locally amplified stress was therefore designed to promote nanoparticle sintering and eliminate the pores. Three parallel 5 μm width groove structures followed the geometry of a 5 × 5 mm^2 square with rounded corners. The radius of the rounded corners was 250 μm, and the inter-groove spacing was 4 μm.

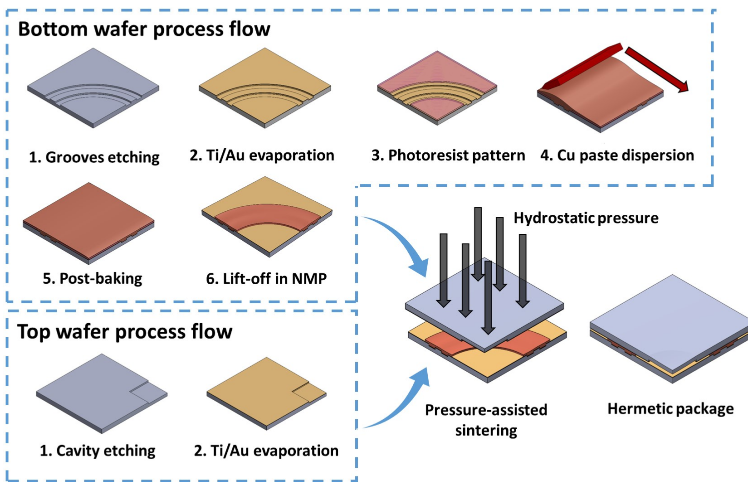

Figure 6.1.: Microfabrication process flow (one quadrant of the die is presented for better illustration).

6.2.2. PROCESS FLOW

Figure 6.1 presents the process flow for microfabrication. According to the symmetric geometry, one quadrant of the die is presented for better illustration.

For the Si bottom wafer, a 2.5 μm deep designed groove structure was etched away by reactive ion etching. Following this was the growth of a 100 nm thermal oxide layer, which provides good adhesion for the metal layer. Afterwards, a 20 nm Ti/ 200 nm Au layer was e-beam evaporated to strengthen the sealing ringcomponent interface. A 3.5 μm thick negative photoresist was coated with varying openings, followed by Cu nanoparticle paste (CP-005, Mitsui Mining and Smelting Company, Ltd., Japan) dispersion with a silicone squeegee. Subsequently, the sample was baked in the air at 80 °C for 5 minutes. This baking step evaporated organic solvent to promote the adhesion between the dried paste and the substrate. Eventually, the small-size paste pattern was formed by a lift-off process. The baked sample was bathed in 80 °C NMP (N-Methyl-2-pyrrolidone) solvent for 1 minute to strip the photoresist.

The process of the top wafer contains mainly two steps. Deep reactive ion etching (DRIE) was employed to create a 450 μm deep cavity, where a 5 μm plasma-enhanced chemical vapor deposition (PECVD) SiO_2 worked as the hard mask. Afterwards, the same 20 nm Ti/ 200 nm Au layer was evaporated on the surface of the top wafer. More process details can be found in Supporting information E.

This study employed pressure-assisted sintering for the die-level metal-metal bonding in a vacuum wafer bonder (Applied Microengineering Ltd, UK). The dies were manually aligned with each other. The sintering temperature from 275 °C to 350 °C was performed, whereas the pressure ranged from 1.5 MPa to 40 MPa. A constant sintering time was controlled at 10 minutes. A low-pressure (0.1 kPa) 5% H_2/N_2 forming gas was inserted during the first 5 minutes of sintering to reduce the oxide. A high vacuum < 0.01 Pa was kept for the rest of the process, including the cooling phase.

6.2.3. HERMETICITY EVALUATION

The evaluation of the hermeticity of the sample was achieved by monitoring the pressure-driven deflection of the diaphragm using an optical profilometer. If the sample is successfully sealed, the diaphragm deflects due to the pressure difference between the interior and exterior of the cavity. Diaphragm deflection (δ) determines the pressure difference (ΔP) between the inside and outside of the package. Equation 6.1 illustrates the relationship between the diaphragm deflection and the pressure difference [19].

6

$$\Delta P = \frac{\delta E d^3}{a x^4} \tag{6.1}$$

where E is Youngs modulus of silicon, d is the diaphragm thickness; a is the shape constant equal to 0.0138 when the diaphragm is square-shaped, and x is the diaphragm length.

By measuring the change in diaphragm deflection over time, the stability of the hermetic package can be determined using this method. If the package has a slight leak, the deflection will progressively decrease until the internal and external pressures of the cavity are equalized. The deflection at the center of the diaphragm is proportional to the differential pressure, and the leak rate L can be calculated using Equation 6.2 [20]. The calculated leak rate includes the influence caused by nanoparticles outgassing during storage.

$$L = ln(\frac{W_{t1}}{W_{t2}})(\frac{VP_0}{t_2 - t_1}) \tag{6.2}$$

where W_{t1} and W_{t2} are the maximum deflections at the center of the diaphragm at times t_1 and t_2, respectively; P_0 is the ambient pressure outside the cavity, and V is the volume of the cavity.

6.3. RESULTS ON SIMULATION

To efficiently assess the vacuum level in the cavity, a finite element analysis (FEA) model was constructed in *COMSOL Multiphysics*. The Solid Mechanics module with Multiphysics coupling to the heat transfer in solids was applied. A quarter of the entire model was

simulated due to its symmetry to save computational resources, as shown in Figure 6.2. The simulation parameters adopted for each layer are listed in Table 6.1. The properties of the bulk Cu were adopted for the sintered Cu paste structure.

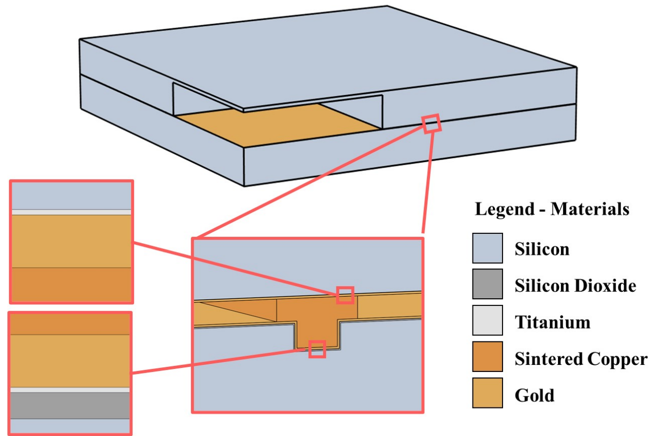

Figure 6.2.: Schematic of the FEA model

The exterior boundary of the geometry was kept at a pressure of 1×10^5 Pa to emulate the atmospheric pressure. The thickness of the diaphragm was determined as 50 μm. A parametric study was conducted with applied interior pressure ranging from 0 Pa to 1×10^5 Pa. Furthermore, the temperature change during the sintering process was also considered in the simulation. The model was simulated from 300 °C down to 20 °C to incorporate the warpage effect caused by the CTE mismatch and geometry asymmetry, something which is not part of the analytical model.

Table 6.1.: Summary of material properties in the simulation

Material	Elastic modulus [GPa]	Poisson ratio	CTE [10^{-6}/K]	Thermal conductivity [W/mK]
Silicon	170	0.28	2.6	130
Gold	70	0.44	14.2	317
Titanium	115.7	0.32	8.6	21.9
Silicon dioxide	70	0.17	0.5	1.4
Sintered Cu paste	120	0.34	16.5	401

The deflection in the diaphragm was successfully simulated with a low cavity interior pressure. The relationship between maximum deflection and interior cavity pressure from the FEM simulation and analytical model were plotted in Figure 6.3, respectively. The inserted frame presents an example of surface displacement mapping when the interior cavity pressure was set as 1.6×10^{-3} Pa. The slope shows a slight deviation, which was caused by the selection of the shape constant. The FEA model simulated shape con-

stant was 0.0156, while the analytical model adopted was 0.0138. It is because the deflected structure was not a perfect square. Therefore, the FEM model was verified with the analytical model. Additionally, the thermo-mechanical deformation causes residual deflection as the cavity is sealed at a high temperature.

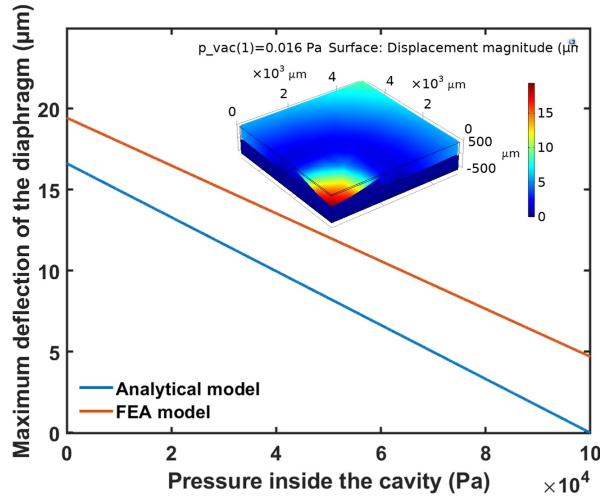

Figure 6.3.: Relationship between maximum deflection and interior cavity pressure with a 50 μm thickness diaphragm)

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6.4. RESULTS EXPERIMENTS

6.4.1. EVALUATION OF BONDING PERFORMANCE

Figure 6.4 shows the Cu paste ring with a clean surrounding surface after the lift-off process. The width was kept around 50 μm as designed in the lithographic mask. Furthermore, the Cu paste ring's profile in two directions was measured. The highest point of the two cross sections is 2.2 μm and 2.09 μm, respectively. The direction of stencil printing can influence the deviation of the ring height. It is noticed that the value is smaller than the photoresist height of 3.5 μm, which is caused by the shrinkage during the baking process. Besides, a non-flat surface is revealed. This can be attributed to more volumetric loss when covering a groove.

The result demonstrates that the lithographic lift-off method applies to the viscous paste to form a small-size sinterable structure for further heterogeneous integration.

In general, low-temperature sintering of nanomaterials results in a porous structure, and the inter-particle bonding highly relies on the sintering condition, temperature, pressure and dwell time.

In this study, a design of experiments (DoEs) comprising sintering temperatures ranging from 275 °C to 340 °C and sintering pressure ranging from 1.5 MPa to 40 MPa were conducted to explore the feasibility of realizing hermetic packaging. The results are

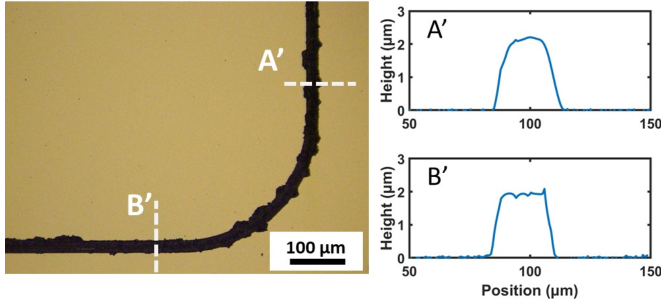

Figure 6.4.: Profile of Cu paste ring after lift-off

scattered in Fig. 6.5. In all groups, the top die was successfully bonded with the bottom die through pressure-assisted sintering technology.

As a result, we found that the sample fabricated with a sintering temperature higher than 300 °C and pressure larger than 10 MPa could result in a deflected diaphragm, indicating a sealed vacuum chamber at 0 hours. In contrast, the red region in Fig. 6.5 represents the non-vacuum sealable region. This region comprises the combination of temperatures <300 °C and applied pressure values of <10 MPa. Sufficient sintering temperature enables the surface diffusion between nanoparticles to promote the neck area. Sintering pressure, on the other hand, plays a crucial role in eliminating the pores and therefore reducing the porosity. Therefore, the softest sintering parameter to realize hermetic sealing was determined as 300 °C and 10 MPa.

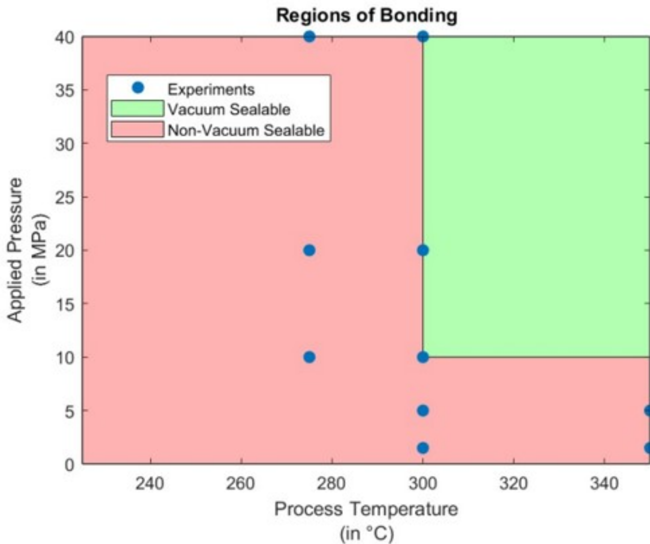

Figure 6.5.: Parameter study for the hermetic packaging

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Moreover, the bonding strength of the sample sintered at 300 °C was evaluated by the shearing test on a Royce 650 Universal Bond Tester, as shown in Figure 6.6. To comprehensively assess the shear strength, each sample was diced into four quadrants using a standard dicing saw. The quadrants were glued on a leadframe for the shear test, as shown in the inserted frame in Figure 6.6. Therefore, each data points represent the average value of four tests.

Except for the sample sintered at 1.5 MPa, the samples survived the mechanical dicing process. The shearing results are plotted in Figure 6.6. The bonding area was theoretically calculated as 0.127 mm^2. The bonding strength increases according to a higher sintering pressure. The promotion of the bonding strength is significant when the sintering pressure increases from 5 MPa to 20 MPa. The bonding strength at 5 MPa sintering pressure is 76 MPa, which jumps to 250 MPa as the sintering pressure increases to 20 MPa. However, the improvement between the sintering pressure of 20 MPa and 40 MPa is slight, as the bonding strength is 250 MPa and 280 MPa, respectively.

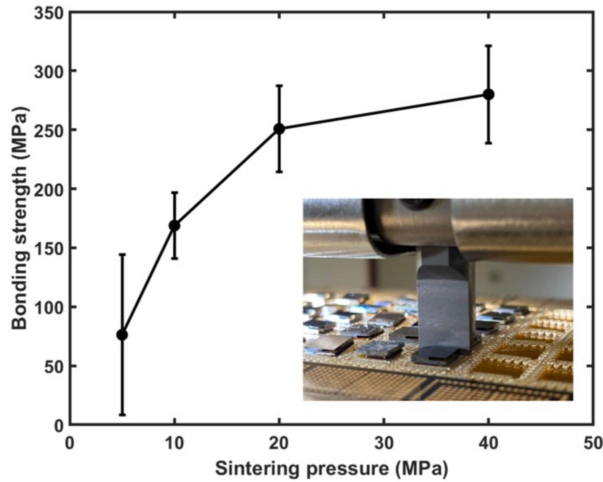

Figure 6.6.: Bonding strength with different sintering pressure

Afterward, the fracture surface of a sample sintered at 300 °C and 10 MPa was analyzed, as shown in Figure 6.7, to investigate the mechanism of hermeticity. Three typical morphologies can be found around the groove structure region. It can be seen that the microstructure in the grooves is porous, indicating insufficient sintering. In contrast, as shown in the insert, the surrounding microstructure is seamless and presents different contrast compared to the Au coating. The width of this light area is relatively 50 μm, which implies limited shrinkage along the horizontal direction. In addition, high structures were noticed remaining on the sealing ring area.

Energy dispersive X-ray (EDX) spectroscopy was used to identify the elements in the different structures, and the results of scanning on lines L1 and L2 are plotted in Figure 6.7(c). The EDX results demonstrate that the non-flat high structure is purely Cu. Besides, the materials remaining in the grooves are also pure Cu. The surrounding struc-

ture contains a thin Cu layer.

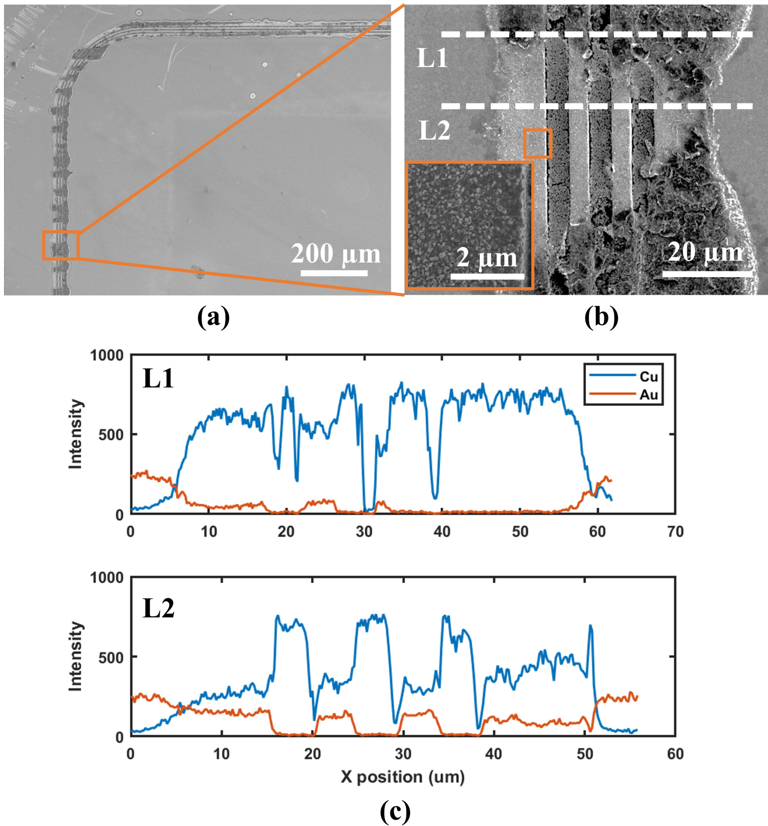

Figure 6.7.: Fracture surface of a sample sintered at 300 °C and 10 MPa (a) A quadrant of the sealing ring; (b) The groove structures; (c) EDX line scan on the position marked in (b)

To further investigate the porosity of the microstructure, the cross-section of the failed groove structure was prepared by a focus ion beam (FIB), as shown in Figure 6.8(a). Same as seen from the top surface, the internal microstructure of the thin Cu layer between grooves is also seamless. The Cu layer in the grooves, however, presents cracks and pores. This result is consistent with the observed sealing ring morphology. The Cu paste layer was wave-shaped after lift-off (Fig. 6.4). The contact area between the top die and the Cu paste in the grooves was thus inadequate. Moreover, it had edges at these positions, leading to stress concentration.

The failure mode of the shear test can be identified as a cohesive failure (Figure 6.8(b)) as negligible Au finish is exposed in the sealing ring area. The developed technology achieves hermeticity through the solid, seamless sintered Cu structure around the grooves, created using the amplified pressure at the edge of the patterned Cu structure.

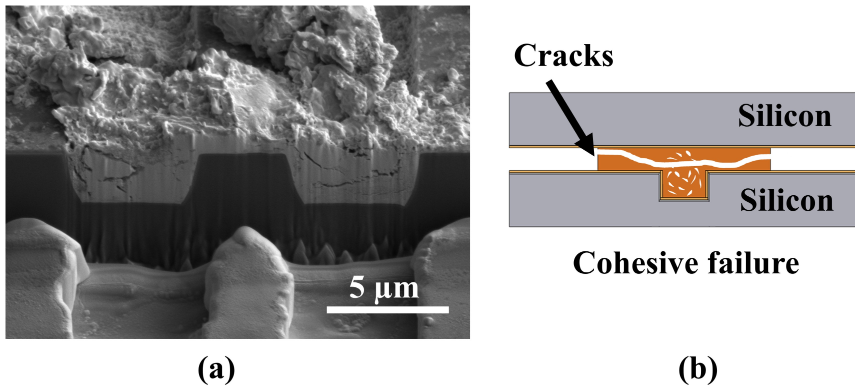

Figure 6.8.: (a) Cross-section on the fracture surface; (b) Schematic of the failure

6.4.2. EVALUATION OF HERMETICITY

At first, the actual depth of the cavity was measured to calculate the pressure difference. Figure 6.9 presents the profile of the Si cavity. The edge of the cavity is sharp, and the bottom surface is relatively flat. A 3D visualization was inserted to show the high quality of DRIE. The thickness of the diaphragm before sintering activities was 78 μm, 59 μm and 46 μm for the samples sintered under 10 MPa, 20 MPa and 40 MPa, respectively.

Consistent with the simulation results, a deflected diaphragm was successfully formed after pressure sintering, as shown in Figure 6.10. In contrast, the non-vacuum-sealed sample shows a flat top surface as a reference. The symmetric deflection of the diaphragm is visualized with the top surface as the zero planes. The maximum displacement of the deflection is therefore determined as 12.3 μm.

With the known diaphragm thickness and the maximum deflection of the diaphragm, the sealed vacuum level can be calculated. The vacuum level for the sample sintered at 300 °C under 10 MPa, 20 MPa, and 40 MPa is 61.8 kPa, 60.0 kPa and 7.2 kPa, respectively. There is no evidence to support the dependence of the cavity pressure on the sintering pressure. At the same temperature and sintering time, other influence factor could be the decomposed organic content in the paste composition, which is difficult to quantify.

It can be noticed that the sealed value is one to two orders higher compared to the forming gas pressure level (0.1 kPa) during the sintering. This increase could be attributed to the Cu paste materials composition. The organic solvent and binder decomposed during the bonding process, and the decomposition products were therefore sealed in the cavity, resulting in a low-medium vacuum level.

The samples were stored at constant humidity and room temperature for around six months to assess the hermeticity. Figure 6.11 presents the deflection evolution of the sample sintered under 10 MPa. The results reveal excellent vacuum stability of the sealed sample over 169 days. It can be seen that the diaphragm has limited recovery over storage. The maximum deflection of the diaphragm changed from 12.3 μm on 0 days to 12.0 μm after 169 days.

Due to the diaphragm thickness variation, the deflection values of each sample varied.

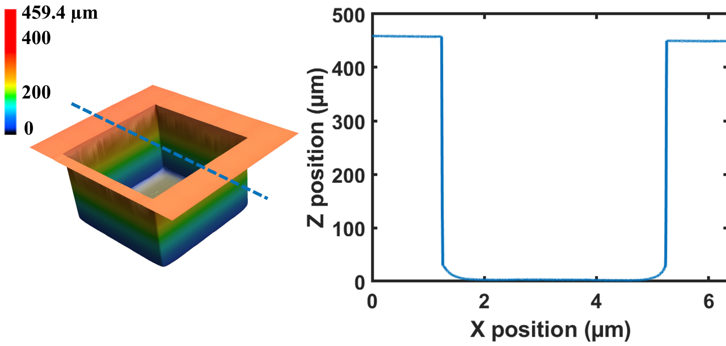

Figure 6.9.: 3D profile of the etched cavity

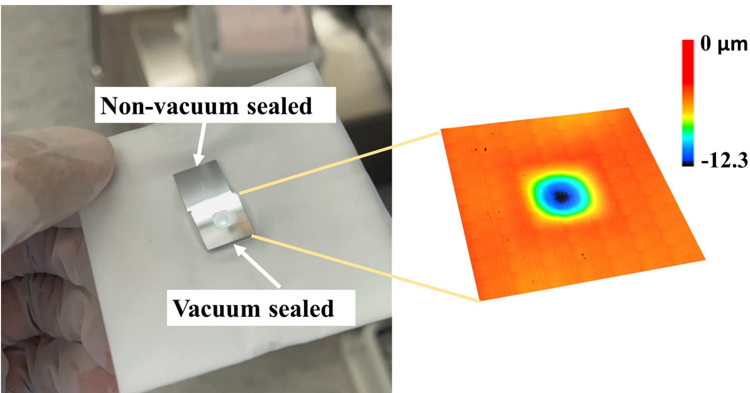

Figure 6.10.: Sample sintered at 300 °C under 10 MPa and top surface 3D visualization

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To calculate the leak rate of the package, the item $ln(W_{t2}/W_{t1})$ of the samples sintered under 10 MPa and 40 MPa was plotted in Figure 6.12 as a function of the storage time. The data points fluctuate because of measurement inaccuracy. Furthermore, the linear fitting was calculated to evaluate the leak rate by using Eq. 6.2.

In this study, the cavity is assumed as a perfect cuboid, and the volume is accordingly calculated as 7.2×10^{-6} L. Subsequently, the leak rate is calculated as 1.2×10^{-12} Pa·m^3/s and 8.4×10^{-13} Pa·m^3/s. Thus, 10 MPa and 40 MPa sintering pressure resulted in a reliable hermetic package. A lower leak rate was observed in the sample sintered under high sintering pressure. It can be caused by the fewer pores in the sintered structure and a more solid connection between the metallization layer and the sintered sealing ring. The leak rate achieved in this study is considerably lower compared to the reported values of 10^{-11} to 10^{-9} Pa·m^3/s achieved by the Ni/Sn solder bonding [21] and Au-Sn eutectic bonding [22] but still below the Cu thermos-compression enabled hermetic package as 10^{-17} Pa·m^3/s [20]. However, this work achieved the comparable value as the reported sintered hermetic package of 10^{-14} Pa·m^3/s [23] while implementing a longer storage and a smaller Cu sealing ring. Therefore excellent hermeticity stability is demonstrated

for the Cu nanoparticle sintering-enabled hermetic packages.

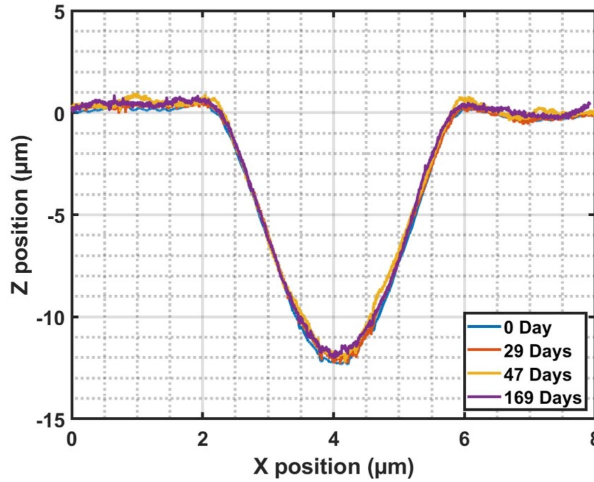

Figure 6.11.: Evolution of the diaphragm deflection in the sample sintered under 10 MPa over 169 days

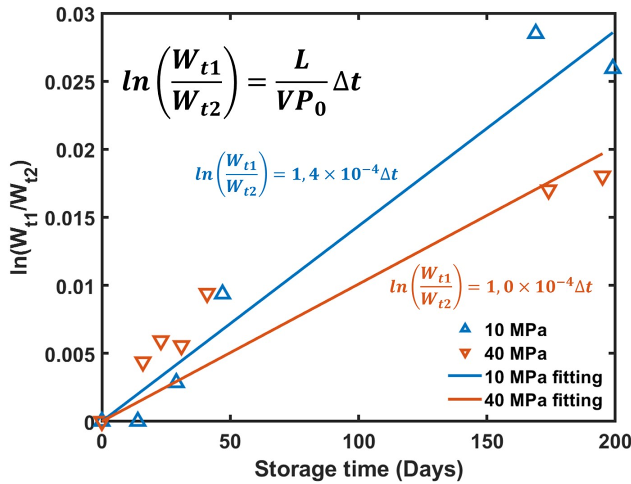

Figure 6.12.: Evolution of item $ln(W_{t2}/W_{t1})$ with the storage time

6.5. CONCLUSION

This study demonstrates the successful hermetic sealing of a Si cavity using Cu nanoparticle sintering with a 50 μm sealing ring dimension. We demonstrate excellent bond-

ing strength and hermetic stability. The following conclusions were obtained:

- Hermetic sealing was achieved using thermos-compression bonding, with the boundary of the process parameter determined from 300 °C and 10 MPa. Strong shear strength of 280 MPa was obtained. According to the fracture surface analysis, stress concentration on the edge promoted the sintering. The fully sintered Cu in the surrounding area near the grooves contributed to the hermeticity.

- A verified FEA model was established to evaluate the interior cavity pressure. The lowest value of 7 kPa was calculated. Additionally, robust hermetic stability was demonstrated over six months of storage. A low leak rate of 8.4×10^{-13} Pa·m^3/s was extracted.

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CONCLUSIONS AND RECOMMENDATIONS

7.1. CONCLUSIONS

THIS dissertation conducted a comprehensive study on metallic nanoparticle sintering, covering the sintering mechanism, thermo-mechanical performance characterizations, and implementations in two applications. These studies span a wide range of physical scales, from atomic-level behavior to component-level reliability, and involve multiple physics domains, including thermal, mechanical, and electrical characterization. This research can provide promising support for advancing low-temperature nanoparticle sintering in power electronics packaging and beyond applications.

Atomistic insights on nanoparticles sintering and sintered structure - Dual-NP model: A 2.5 nm two-hemispherical NP model was constructed to reveal the influence of sintering temperature (300-500 K) and pressure (0-300 MPa) on the sintering process. he study found that pressure is a more dominant factor than temperature in promoting the coalescence of NPs. Applying pressure to Cu NPs can shift the dominant coalescence mechanism from slight surface diffusion to intensive volume diffusion and plastic flow driven by defects. While temperature primarily enhances atomic diffusion activities, tensile simulations on the two-hemispherical NP model revealed that higher pressure and temperature improve mechanical properties, such as the elastic modulus and tensile strength.

Atomistic insights on nanoparticles sintering and sintered structure - Multi-NP model: A scaled-up multi-NP atomistic model was constructed to simulate nanoindentation on the sintered structure. The simulation revealed that plastic deformation during indentation is driven by dislocation nucleation beneath and around the indenter's edges. Limited pressure-induced further sintering was observed. The local indentation position proved more critical than the structure's density, with the porous sintered structure showing an indentation modulus of 55 GPa and hardness of 1.19 GPa. Beyond mechanical performance, chemical corrosion was examined using ReaxFF MD simulation, revealing that the sulphidation mechanism involves the upward migration of surface Ag atoms to a sulphur-rich layer and sulfur atom diffusion into the Ag body. Porous structures suffered more severe sulphidation due to a larger inner surface area, indicating more reaction sites, with aging temperature being a dominant factor.

Multi-scale mechanical behaviour of the sintered nanoparticles - Microscopic fracture toughness: An experimental method for evaluating crack propagation behavior at a micro-scale in a sintered nanoporous Cu joint was developed by micro-fabricating 14 μm × 4 μm × 4 μm micro-cantilevers with different notch depths. A 3D sintered Cu model was reconstructed by a FIB milling method. The sintered Cu nanoparticles yielded a low porosity of 8.25 ± 0.69%. Necking tips and dimple ridges were observed on the fracture surface, confirming elastic-plastic fracture in the bending test. The elastic modulus and yield strength were extracted as 41 ± 2 GPa and 970 ± 21 MPa, respectively. In addition, specimens with an a/W ratio of 0.20 and 0.37 presented a close bending behavior. A tougher fracture was noticed, and a higher a/W value of 0.5. Instead of the LEFM theory, the microscopic conditional fracture toughness K_Q was translated from elastic-plastic J-integral evaluation, ranging from 3.2 ± 0.3 MPa·m$^{1/2}$ to 4.3 ± 0.1MPa·m$^{1/2}$. The microscopic fracture toughness showed limited dependence on notch depth, with a relative initial notch depth a/W between 0.20 and 0.37 maintaining near-constant fracture toughness, providing insights for future testing on the size effect.

Multi-scale mechanical behaviour of the sintered nanoparticles - Macroscopic high-temperature tensile performance: Cu dog-bone tensile specimens were fabricated in an N_2 environment by pressure-assisted sintering at 250 °C with 100 ± 36 nm self formulated Cu NPs. The high-temperature tensile tests were implemented at temperatures ranging from 180 °C to 360 °C with different strain rates ranging from 1 × 10^{-4} s^{-1} to 1 × 10^{-3} s^{-1}. By increasing the temperature to 360 °C, the sintered structure's elastic modulus and tensile strength dropped significantly to 8.06 GPa and 22.32 MPa. At the same time, the response to varying the strain rate was found to be minor. Next, different failure modes were determined from the failure analysis. From the fracture surface morphology, the sample tested at 180 °C and 1 × 10^{-3} s^{-1} showed brittle fracture features, while more ductile fracture features were present in the sample tested at 360 °C and 1 × 10^{-4} s^{-1}. Evidence of grain refinement and LAGB formation at different locations through the EBSD results confirms that ductility was significantly promoted by recrystallization at high temperatures. Additionally, a viscoplastic Anand model was fitted and parameterized according to the stress-strain curves of the sintered structure, demonstrating high consistency under high-temperature conditions.

Dynamic transient thermal behaviour of the sintered nanoparticles - Offline transient thermal measurements: A configurable TTC was applied as a flexible and cost-effective solution for fast thermal evaluation of different nanoparticles sintered die-attach joints. The TTCs first reached equilibrium status with a 2.2 A current. The external power was subsequently switched off. RTDs recorded the transient thermal performance accordingly within 100 seconds in the cooling phase. The transient measurement was measured on a water-cooled case with/without TIM, following the TDIM standard JEDEC 51-14. The junction-to-case thermal resistances were extracted from the separation point of thermal impedance curves and structure functions, respectively. The Ag sintered die-attach exhibited the lowest junction-to-case thermal resistance of 0.144 K/W, while the Cu sintered die-attach exhibited a relatively higher thermal resistance of 0.158 K/W. The SAM images confirmed the difference.

Dynamic transient thermal behaviour of the sintered nanoparticles - Online transient thermal measurements: Si MOSFETs were used to record thermal performance

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degradation during thermal cycling tests (-55 °C to 150 °C). The Si chips were sintered in QFN discrete devices at 250 °C with different pressures and sinter materials (self-formulated Ag and Cu). Unlike the offline transient thermal measurement strategy, a short heat pulse (0.2 seconds) was introduced at room temperature. The transient thermal performance within 0.1 seconds was employed to calculate the thermal impedance, which was successfully demonstrated to reflect the thermal impedance evolution. The thermal impedance degradation exhibited a high consistency of adhesion results obtained from SAM images. Ag sintered products presented superior robustness with a 2.5% to 3.8% thermal impedance increase. The promotion from sintering pressure increase from 10 MPa to 20 MPa didn't diverse the degradation trend much. In contrast, Cu-sintered QFN suffered visible degradation from the first cycle.

Prototype I - Nanoparticles sintered Si TO247 power device: TO247 Si IGBT (1200V/50A) devices with three different sintered backside die-attach and two types of thick Al topside interconnects on Cu metalized pads were manufactured. The reliability degradation was examined by 500 cycles of passive TCT (-50 °C to 150 °C) and further 1000 cycles of TST (-50 °C to 150 °C). The bondline thickness ranges from 23.3 μm to 30.2 μm. Uneven material distribution was found in all specimens due to the needle dispersion method. Before the reliability test, no evident voids and cracks were found, while Ag sintered product exhibited void generation and propagation in TST aging tests. Regarding the transient thermal impedance, the specimens bonded by heavy Al wires were close to that of heavy Al ribbons. The difference between the Ag-sintered specimens and Cu-sintered specimens was slight. The variation of junction-to-case thermal resistance was not apparent, thanks to the high thermal conductivity of sintered die-attach. TCT and TST posed a negligible influence despite a bit of delamination. Similar results were concluded regarding effective electrical resistance. Cu-sintered specimens performed better than the Ag-sintered specimens, and the thermal aging tests neither enlarged nor eliminated the gap in the effective resistance. According to the TST conditions, a transient FEM simulation was carried out and revealed the stress concentration took place at the corners of the Si chip as well as the heterogeneous interface of the topside interconnect. The simulation results were consistent with the SAM images that void propagated from the Si chip corners due to CTE mismatch-induced thermo-mechanical stress. FEM simulations also indicated that a larger total cross-sectional area in the topside interconnect could lead to a more stress-relaxed structure, though the improvement was slight.

Prototype II - Nanoparticles sintered hermetic package: A hermetic package demonstrator was fabricated with a top Si dummy die featuring a 50 μm diaphragm and a bottom Si dummy die with groove structures. A 50 μm thin ring containing Cu nanoparticles paste was transferred by using a 3.5 μm lithographic stencil masker. An effective lift-off was optimized as a 1-minute bath in 80 °C NMP solvent. The hermetic sealing was therefore achieved using thermo-compression bonding, with the boundary of the process parameter determined from 300 °C and 10 MPa. A strong shear strength of 280 MPa was achieved. Fracture surface analysis indicated stress concentration on the edge promoted sintering, and fully sintered Cu near the grooves contributed to hermeticity. Hermeticity was estimated by simulating the relationship between interior cavity pressure and diaphragm deflection, calculating the lowest cavity pressure at 7 kPa. Furthermore, robust hermetic stability was demonstrated over six months of storage. A low leak rate

of 8.4×10^{-13} Pa·m^3/s was extracted.

7.2. RECOMMENDATIONS FOR FUTURE WORKS

THIS dissertation discusses the sintering mechanism and multi-scale, multi-physics evaluation of sintered nanoparticles, demonstrating the implementation of metallic nanoparticles sintering technology in power electronics and beyond. The ultimate goal in this field is to establish robust reliability performance and develop a reliable lifetime estimation model. Therefore, further research is necessary in this area.

Atomistic simulation has proven to be an effective tool for understanding the mechanisms of sintering and the mechanical/chemical responses of sintered structures. However, Cu nanoparticle sintering faces oxidation issues. Future work should focus on evaluating the effect of the oxide shell on the sintering degree and subsequent electro-thermo-mechanical performance. Additionally, multi-scale experiments are needed to verify and utilize properties extracted from MD simulations, potentially enhancing higher-level FEM simulations or data-driven methods.

Preliminary results regarding thermo-mechanical performance have been obtained in this work. To develop a more accurate material model, future research should explore the microscopic mechanical performance at various temperatures and the size effect to establish a precise fracture criterion. Furthermore, the numerical model's verification requires reliability testing with sufficient specimens.

During reliability testing, the sintered structure is expected to experience degradation accompanied by microstructural changes (e.g., grain size, porosity, grain boundary). These changes affect the thermo-mechanical performance descriptions. An analytical model would consume excessive computational resources, making real-time descriptions of the sintered layer impractical for RUL estimation. Thus, a data-driven model can be developed by monitoring various electrical signals. As demonstrated in this dissertation, online thermal monitoring is a promising starting point. However, further development is necessary to reduce noise and improve data accuracy.

This research has shown that sintered Cu nanoparticles can perform similarly to sintered Ag nanoparticles. Therefore, future work should focus more on Cu nanoparticle sintering. Developing Cu nanoparticle paste to reduce the required temperature, pressure, and time is essential. Moreover, creating a new Cu paste that allows pre-sintering during the die-mounting process would be highly beneficial in an industrial setting.

Finally, more concrete applications of nanoparticles sintering in heterogeneous integration should be explored. Building on the work presented in this dissertation, Ag and Cu nanoparticles sintering could be applied to multi-die modules operating under more extreme conditions. The MEMS hermetic packaging solution could be further developed into a SiP with functional MEMS. The superior performance of sintered nanoparticles could extend beyond this application, potentially playing a vital role in WBG MEMS devices. Additionally, Cu sintering technology has the potential to advance the 'all-copper interconnect' concept in 3D-IC, especially for systems operating in extreme environments.

A

SUPPORTING INFORMATION - CHAPTER 2

AG/S REAXFF FORCE FIELD

```
39 ! Number of general parameters
    50.1077      !p(boc1)
    9.5380      !p(boc2)
    127.8302      !p(coa2)
    3.0000      !p(trip4)
    6.5000      !p(trip3)
    0.0000      !kc2
    1.3997      !p(ovun6)- this param is replicated twi
    9.0000      !p(trip2)
    12.4607      !p(ovun6)- this param is replicated twi
    13.6017      !p(ovun8)
    0.0000      !p(trip1)
    0.0000      !Lower Taper-radius (swa)
    10.0000      !Upper Taper-radius (swb)
    2.8793      !Not used
    33.8667      !p(val7)
    7.1219      !p(lp1)
    1.0563      !p(val9)
    2.0384      !p(val10)
    6.1431      !Not used
    6.9290      !p(pen2)
    0.3989      !p(pen3)
    3.9954      !p(pen4)
    -2.4837      !Not used
    5.7796      !p(tor2)
    10.0000      !p(tor3)
    1.9487      !p(tor4)
```

A

```
     -1.2327      !not used
     2.1571      !p(cot2)
     1.4647      !p(vdW1)
     0.1000      !Cutoff for bond order*100 (cutoff)
     2.0038      !p(coa4)
     0.6093      !p(ovun4)
     1.2120      !p(ovun3)
     1.8512      !p(val8)
     0.5000      !Not used
     20.0000      !Not used
     5.0000      !not used
     0.0000      !not used)
     3.6942      !p(coa3)

2 ! Nr of atoms; atomID; ro(sigma); Val; atom mass; Rvdw; Dij; gamma
     alfa; gamma(w); Val(angle); p(ovun5); n.u.; chiEEM; etaEEM; n.u.
     ro(pipi); p(lp2); Heat increment; p(boc4); p(boc3); p(boc5),n.u.; n.u.
     p(ovun2); p(val3); n.u.; Val(boc); p(val5); n.u.; n.u.; n.u.
Ag 2.4066 1.0000 107.8680 1.9021 1.3275 1.3032 -1.0000 1.0000
     9.6526 6.9178 1.0000 0.0000 0.0000 1.0455 7.9233 0.0000
     -1.0000 0.0000 0.0000 65.6028 4.1849 4.1329 0.0000 0.0000
     -9.8989 0.0000 0.0000 1.0000 0.0000 0.0000 0.0000 0.0000
S 2.1928 2.0000 32.0660 1.8716 0.8217 1.4180 2.1606 6.0000
     9.4898 9.7325 2.0000 14.9077 0.0000 4.7986 5.2118 0.0000
     -1.0000 0.0000 0.0000 21.2401 4.5184 0.6594 0.0000 0.0000
     -6.5772 0.7164 0.0000 2.0000 16.5911 0.0000 0.0000 0.0000

3 ! Nr of bonds; at1; at2; De(sigma); De(pi); De(pipi); p(be1); p(b)
     p(be2); p(bo3); p(bo4); n.u.; p(bo1); p(bo2); p(ovun1); n.u.
1 1 81.6619 0.0000 0.0000 -0.3737 0.0000 1.0000 0.0000 0.3953
     1.0227 -60.0000 1.0000 0.0000 -0.0893 5.5093 0.0000 0.0000
1 2 104.8710 0.0000 0.0000 3.6442 -0.2000 0.0000 16.0000 0.2700
     -0.2285 -0.2000 15.0000 1.0000 -0.2986 4.8391 0.0000 0.0000
2 2 115.9740 54.7129 0.0000 0.2390 0.0000 1.0000 0.0000 0.3365
     15.0313 -1.3461 15.4752 1.0000 -0.9944 4.4430 1.0000 0.0000

1 ! Nr of off-diagonal terms. at1; at2; Dij; RvdW; alfa; ro(sigma); r
1 2 6.0463 1.4418 9.6198 1.9016 -1.0000 -1.0000

2 ! Nr of angles. at1; at2; at3; Thetao,o; p(val1); p(val2); p(coa1);
1 2 1 34.4834 24.4547 17.8095 0.0000 -4.2021 0.0000 1.5800
2 2 2 91.0591 47.8305 4.7429 0.0000 2.9635 0.0000 1.5520

1 ! Nr of torsions. at1; at2; at3; at4; V1; V2; V3; p(tor1); p(cot1); n
0 2 2 0 5.1332 0.0107 -1.0684 -2.3333 -4.2259 0.0000 0.0000
```

```
0 ! Nr of hydrogen bonds. at1; at2; at3; r(hb); p(hb1); p(hb2); p(hb3
```

Ag/S ReaxFF MD LAMMPS script

```
log log.reaction
units real

atom_ style charge
boundary p p p
read_data data.SinteredAg150S

pair_style reax/c NULL
pair_coeff * * Reaxffr.AgS S Ag

neighbor 2 bin
neigh_modify every 10 delay 0 check yes

group S type 1
group Ag type 2

compute 1 all property/atom q
compute SQ S reduce sum c_1
compute 2 S msd
compute myRDF all rdf 1000 1 2

velocity all create 750.0 4928459 dist gaussian

variable qS equal c_SQ

thermo 1000
thermo_style custom step temp etotal pe ke v_qS c_2[4]
thermo_modify lost ignore flush yes
timestep 0.5

fix 1 all qeq/reax 1 0.0 10.0 1e-6 reax/c

min_style cg
minimize 1.0e-10 1.0e-10 50000 50000

reset_timestep 0

dump 1 all custom 1000 dump.reax.deposit id type x y z vx vy vz c_1
```

A

```
fix 2 all nvt temp 750.0 750.0 100.0
fix 4 all reax/c/species 1 10 1000 species.out element S Ag
fix rdf all ave/time 1 10 10000 c_myRDF[*] file tmp.rdf mode vector

run 1000000

write_restart restart.750K
unfix 2

fix 3 all nvt 750 300 100.0

run 1000000
write_restart restart.750K_RT
```

B
SUPPORTING INFORMATION - CHAPTER 3

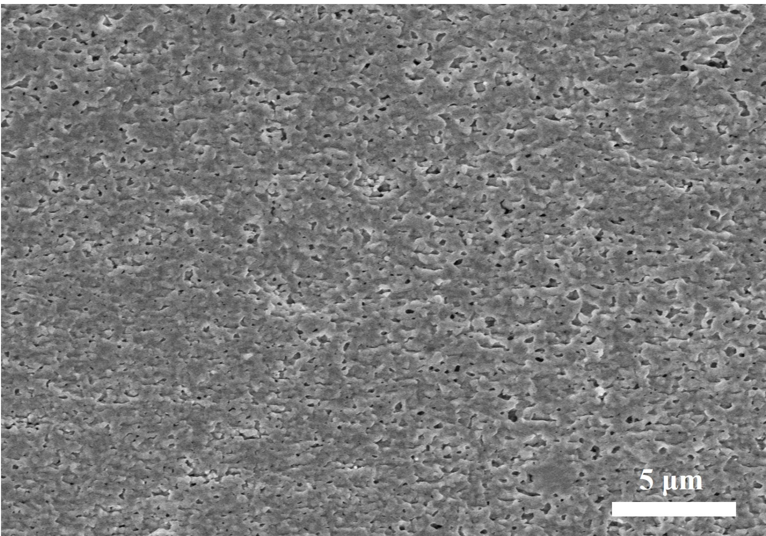

Figure B.1.: Nano-Cu sintered porous structure for high-temperature tensile tests.

B

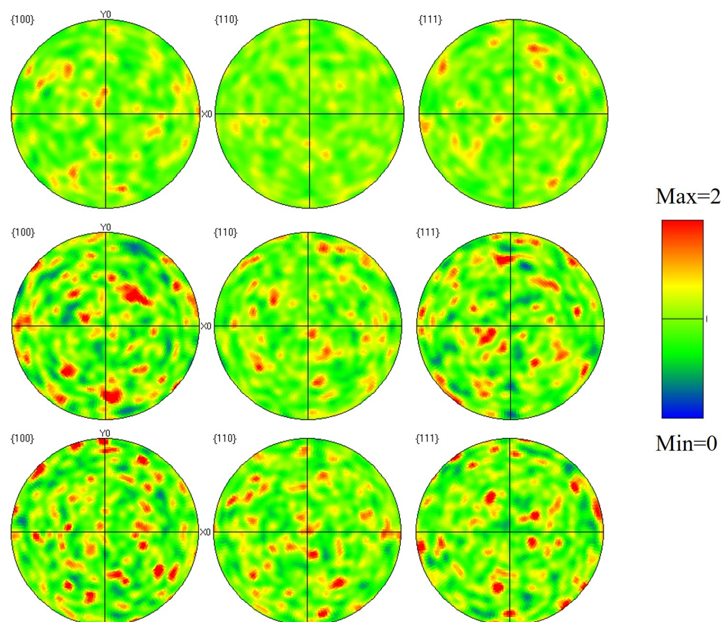

Figure B.2.: EBSD pole figure of the rapture sample in the position of 20 mm to the fracture surface (top row), 4 mm to the fracture surface (middle row) and 20 mm to the fracture position (bottom row).

C

Supporting information - Chapter 3

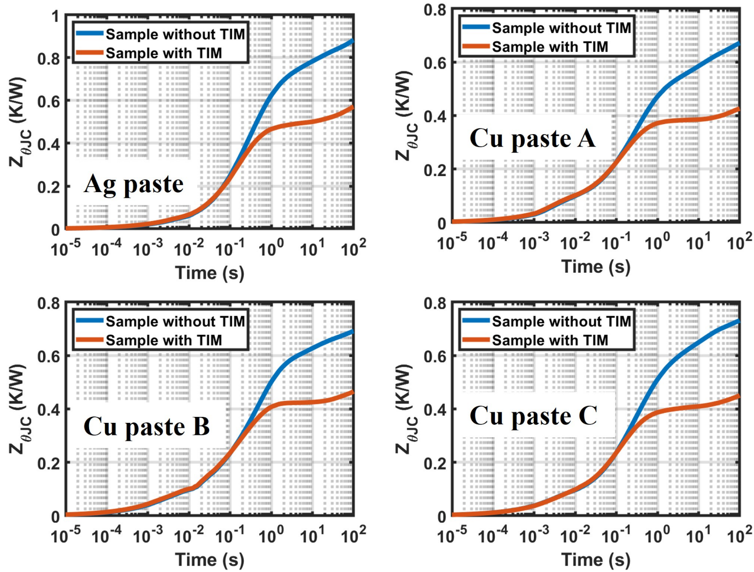

Figure C.1.: Thermal impedance curves during the thermal transient for the samples with and without TIM.

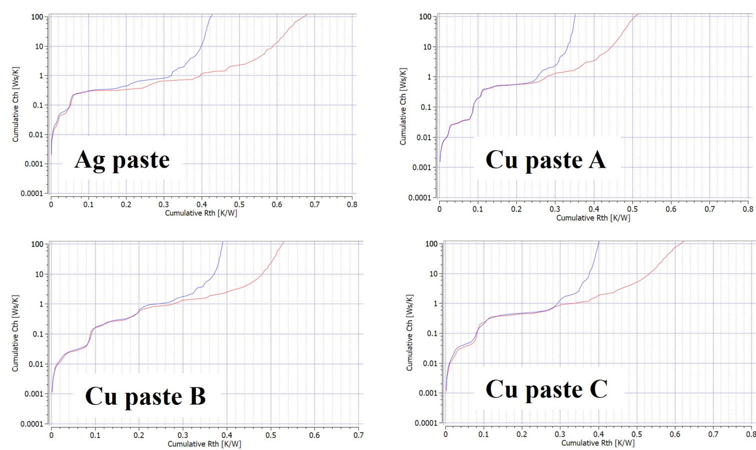

Figure C.2.: Cumulative structure function for sample sintered by different sinter materials. The images were generated by TDIM-Master software.

D

SUPPORTING INFORMATION - CHAPTER 5

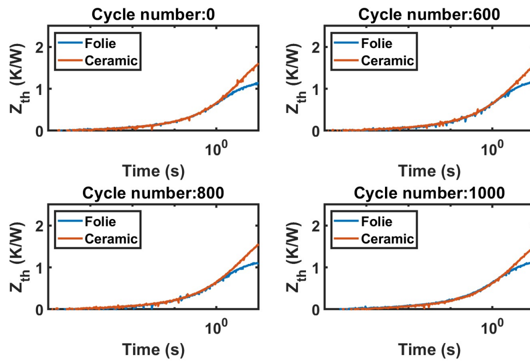

Figure D.1.: Thermal impedance curves with dual interfaces during 1000 cycles of *Ag paste*-sintered and wire-bonded sample.

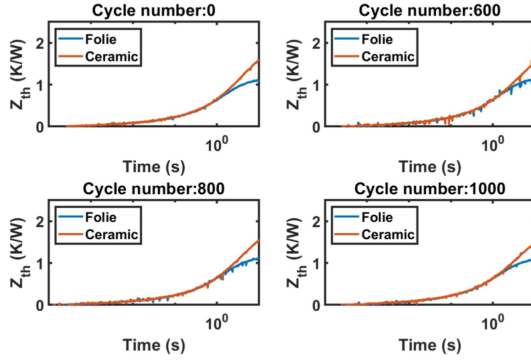

Figure D.2.: Thermal impedance curves with dual interfaces during 1000 cycles of *Cu paste A*-sintered and wire-bonded sample.

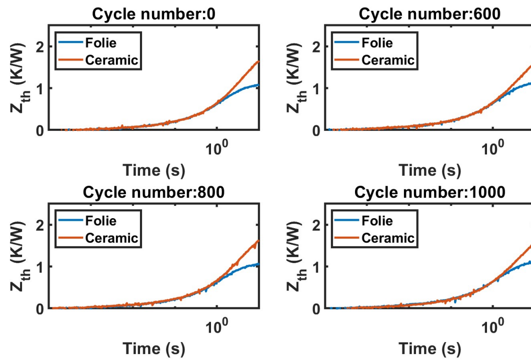

Figure D.3.: Thermal impedance curves with dual interfaces during 1000 cycles of *Cu paste A*-sintered and ribbon-bonded sample.

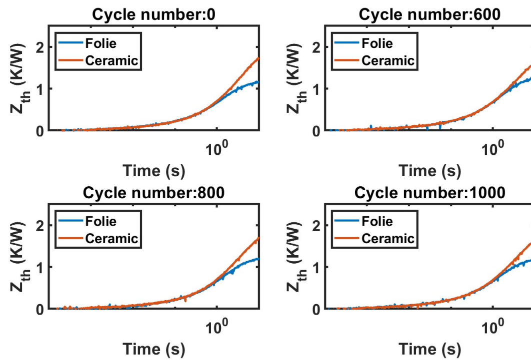

Figure D.4.: Thermal impedance curves with dual interfaces during 1000 cycles of *Cu paste B*-sintered and wire-bonded sample.

E

SUPPORTING INFORMATION - CHAPTER 6

PROCESS FLOW CHART - TOP WAFER

PART1: CLEANING STEP

1. **CLEANING PROCEDURE: HNO_3** 100% **and** 65%

   Cleaning:

   - 10 minutes in fuming nitric acid (Merck: HNO_3 100%) at ambient temperature.
   - Use wet bench "HNO_3 100%" and the carrier with the red dot.

   QDR:

   - Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

   Cleaning:

   - 10 minutes in fuming nitric acid (Merck: HNO_3 65%) at 110 $^\circ C$.
   - Use wet bench "HNO_3 65%" and the carrier with the red dot.

   QDR:

   - Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

   Drying:

   - Use the Semitool ïinser/dryerẅith the standard program, and the white carrier with a red dot.

PART2: CREATION OF ZERO LAYER

2. **COATING AND BAKING**
   Use the EVG 120 wafertrack to coat the wafers with resist, and follow the instructions specified for this equipment.

The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95 degC for 90 seconds.

Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating Co SPR3012-1.4μm no-EBR (resist thickness: 1.400 μm).

3. **ALIGNMENT AND EXPOSURE**
   Processing will be performed on the ASM PAS 5500/80 automatic waferstepper.

   Follow the operating instructions from the manual when using this machine.

   Use COMURK mask, die-size 20×20 mm, job: litho/Zefwam, energy (120 mJ/cm^2).

   Add AML bottom/top wafer alignment markers. Use COMURK mask, job zeaml-up and an exposure energy of 150mJ/cm^2.(Bonder Alignment markers should be deeper.)

4. **DEVELOPMENT**
   Use the EVG 120 wafertrack to develop the wafers, and follow the instructions specified for this equipment. The process consists of a post-exposure bake at 115 degC for 90 seconds, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100 degC for 90 seconds. Always check the temperature of the hotplates first.

   Use development program Dev - SP

5. **INSPECTION: LINEWIDTH**
   Visually inspect the wafers through a microscope and check the linewidth. No resist residues are allowed.

6. **PLASMA ETCHING OF ALIGNMENT MARKS**
   Use the Trikon Ωmega 201 plasma etcher and follow the operating instructions from the manual when using this machine.

   Use sequence URK_NPD and set the platen temperature to 20 °C to etch 120 nm deep ASM URK's into the silicon. (Sequence LEON 1 for 3 minutes for wafer bonder alignment markers)

7. **CLEANING PROCEDURE: TEPLA + HNO_3 100% and 65%**
   Plasma strip:

   - Use the Tepla plasma system to remove the photoresist in an oxygen plasma.
   - Follow the instructions specified for the Tepla stripper and use the quartz carrier.

   Cleaning:

   - 10 minutes in fuming nitric acid (Merck: HNO_3 100%) at ambient temperature.
   - Use wet bench "HNO_3 100%" and the carrier with the red dot.

   QDR:

- Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Cleaning:

- 10 minutes in fuming nitric acid (Merck: HNO_3 65%) at 110 °C.
- Use wet bench "HNO_3 65%" and the carrier with the red dot.

QDR:

- Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying:

- Use the Semitool rinser/dryer with the standard program, and the white carrier with a red dot.

PART3: METALLIZATION

8. **COATING AND BAKING**
   Use the EVG 120 wafertrack to coat the wafers with resist, and follow the instructions specified for this equipment.

   The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with AZ NLOF2020 negative photoresist, and a soft bake at 95degC for 90 seconds.

   Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

   Use coating Conlof2020-3.5μm no-EBR (resist thickness: 3.500 μm).

9. **ALIGNMENT AND EXPOSURE**
   Processing will be performed on the Suss MA8 and follow the operating instructions from the manual when using this machine.

   Mask: metal contacts (glass mask)

   Exposure time: check logbook (55 mJ equivalent)

10. **DEVELOPMENT**
    Use the EVG 120 wafertrack to develop the wafers, and follow the instructions specified for this equipment.

    The process consists of a post-exposure bake at 115 degC for 90 seconds, followed by a development step using Shipley MF322 developer (double puddle process), and a hard bake at 100 degC for 90 seconds.

    Always check the temperature of the hotplates first.

    Use development program Dev Only X-link Bake.

    Use development program xDens-Dev-Lift-Off.

11. **INSPECTION**
    Visually inspect the wafers through a microscope and check openings.

12. **Ti/Au EVAPORATION**
    Use the CHA evaporator in CR10000 to deposit 20200 nm of Ti/Au. Contaminated after this step.

13. **LIFE-OFF**
    Perform lift-off in SAL using NMP heated bain-marie to 70°C in an ultrasonic bath. Apply ultrasonic till all Au is removed from the areas it should be lifted off. Rinse in DI water for 5 min and dry the wafers using the contaminated chuck.

    Use dedicated beakers for lift-off

PART4: CAVITY FORMATION

14. **MANUAL COATING AND BAKING**
    The process starts with a manual pre-treatment with HMDS vapor with Nitrogen as the carrier gas. This will ensure the adhesion of the resist with the wafer surface.

    This will be followed using Brewer Science Spinner in the Polymer Lab to manually coat the wafers with resist, and following the instructions specified for this equipment.

    The coating is done with AZ 10XT/12XT thick photoresist with a thickness of 10 μm, spin speed of 1500rpm, and a spin time of 30-60 sec, and a soft bake at 95 °C for 90 seconds.

    Use the chuck for Cu contaminated samples and the hotplate for contaminated wafers

15. **ALIGNMENT AND EXPOSURE**
    Processing will be performed on the Suss MA8 and follow the operating instructions from the manual when using this machine. **Use the contaminated chuck.**

    Mask: passivation (glass mask)

    Exposure time: 300mJ/cm2 (exposure time: check calibration log of Suss s)

16. **MANUAL DEVELOPMENT**
    Use a hotplate to manually develop the wafers.

    Post-exposure bake: 115 °C for 60 seconds on hotplate for **contaminated wafers**.

    Development: Shipley MF322 developer for 60 sec

    Hard bake: 100 °C for 90 seconds on hotplate for **contaminated wafers**.

17. **INSPECTION**
    Visually inspect the wafers through a microscope, and check openings. Put a tissue underneath the wafer.

18. **DEEP REACTIVE ION ETCHING OF SILICON**
    Use the AMS 110/AMS100(in Kavli) DRIE etcher to etch away 500 ţm of Silicon.

19. **LAYER STRIPPING**
    Use the acetone to dissolve the photoresist. (Plasma Etcher in SAL can also be used)

E

20. **MANUAL CLEANING**
Manually clean the wafers in Class 10000. Use the plasma etcher in Class 10000 or prepare a 100% HNO_3 bath for the clean following by the drying on the contaminated chuck.

Process flow chart - Bottom wafer

PART1: CLEANING STEP

1. **CLEANING PROCEDURE: HNO_3** 100% **and** 65%

   Cleaning:

   - 10 minutes in fuming nitric acid (Merck: HNO_3 100%) at ambient temperature.
   - Use wet bench "HNO_3 100%" and the carrier with the red dot.

   QDR:

   - Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

   Cleaning:

   - 10 minutes in fuming nitric acid (Merck: HNO_3 65%) at 110 $^\circ C$.
   - Use wet bench "HNO_3 65%" and the carrier with the red dot.

   QDR:

   - Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

   Drying:

   - Use the Semitool ïinser/dryerẅith the standard program, and the white carrier with a red dot.

PART2: CREATION OF ZERO LAYER

2. **COATING AND BAKING**
   Use the EVG 120 wafertrack to coat the wafers with resist, and follow the instructions specified for this equipment.

   The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95 degC for 90 seconds.

   Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

   Use coating Co SPR3012-1.4μm no-EBR (resist thickness: 1.400 μm).

3. **ALIGNMENT AND EXPOSURE**
   Processing will be performed on the ASM PAS 5500/80 automatic waferstepper.

   Follow the operating instructions from the manual when using this machine.

E

Use COMURK mask, litho job epi0.0, energy (150 mJ/cm^2).

Add AML bottom wafer alignment markers. Use COMURK mask, job zeaml-up and an exposure energy of 150mJ/cm^2.

4. **DEVELOPMENT**
   Use the EVG 120 wafertrack to develop the wafers, and follow the instructions specified for this equipment. The process consists of a post-exposure bake at 115 degC for 90 seconds, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100 degC for 90 seconds. Always check the temperature of the hotplates first.

   Use development program Dev - SP

5. **INSPECTION: LINEWIDTH**
   Visually inspect the wafers through a microscope and check the linewidth. No resist residues are allowed.

E

6. **PLASMA ETCHING OF ALIGNMENT MARKS**
   Use the Trikon Ωmega 201 plasma etcher and follow the operating instructions from the manual when using this machine.

   Use sequence URK_NPD and set the platen temperature to 20 °C to etch 120 nm deep ASM URK's into the silicon. (Sequence LEON 1 for 3 minutes for wafer bonder alignment markers)

7. **CLEANING PROCEDURE: TEPLA + HNO_3 100% and 65%**
   Plasma strip:

   - Use the Tepla plasma system to remove the photoresist in an oxygen plasma.
   - Follow the instructions specified for the Tepla stripper and use the quartz carrier.

   Cleaning:

   - 10 minutes in fuming nitric acid (Merck: HNO_3 100%) at ambient temperature.
   - Use wet bench "HNO_3 100%" and the carrier with the red dot.

   QDR:

   - Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

   Cleaning:

   - 10 minutes in fuming nitric acid (Merck: HNO_3 65%) at 110 °C.
   - Use wet bench "HNO_3 65%" and the carrier with the red dot.

   QDR:

   - Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

   Drying:

- Use the Semitool ȑinser/dryerẅith the standard program, and the white carrier with a red dot.

PART3: FORMATION OF GROOVES

8. **COATING AND BAKING**
Use the EVG 120 wafertrack to coat the wafers with resist, and follow the instructions specified for this equipment.

The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95 degC for 90 seconds.

Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating Co SPR3027-3.1 no EBR (resist thickness: 3.1 μm).

9. **ALIGNMENT AND EXPOSURE**
Processing will be performed on the Suss MA8 and follow the operating instructions from the manual when using this machine. Mask: grooves (glass mask) Exposure time: check logbook (mJ equivalent) (check the exposure value here)

10. **DEVELOPMENT**
Use the EVG 120 wafertrack to develop the wafers, and follow the instructions specified for this equipment. The process consists of a post-exposure bake at 115 degC for 90 seconds, followed by a development step using Shipley MF322 developer (double puddle process), and a hard bake at 100 degC for 90 seconds. Always check the temperature of the hotplates first. Use development program Dev SP

11. **INSPECTION**
Visually inspect the wafers through a microscope, and check openings.

12. **PLASMA ETCHING OF SILICON**
Use the Trikon Omega 201 plasma etcher and follow the operating instructions from the manual when using this machine. The process conditions of the etch program may not be changed. Use sequence LEON-1 and set the platen temperature to 20 $^\circ C$ to etch 400 nm deep grooves into the silicon.

13. **CLEANING PROCEDURE: TEPLA + HNO_3 100% and 65%**
Plasma strip:

    - Use the Tepla plasma system to remove the photoresist in an oxygen plasma.
    - Follow the instructions specified for the Tepla stripper and use the quartz carrier.

    Cleaning:

    - 10 minutes in fuming nitric acid (Merck: HNO_3 100%) at ambient temperature.
    - Use wet bench "HNO_3 100%" and the carrier with the red dot.

    QDR:

E

- Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Cleaning:

- 10 minutes in fuming nitric acid (Merck: HNO_3 65%) at 110 °C.
- Use wet bench "HNO_3 65%" and the carrier with the red dot.

QDR:

- Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying:

- Use the Semitool ïinser/dryerẅith the standard program, and the white carrier with a red dot.

PART4: OXIDATION

14. **OXIDATION**

Furnace no: C1 or D1; Program name: WET10000

Process	Temperature [$^\circ C$]	Gasses & Flows [Liter/min]	Time [Mins]	Remarks
Boat in	600	Nitrogen: 6.0	5	
Satbilize	600	Nitrogen: 6.0	10	
Anneal	600	Nitrogen: 6.0	15	
Heat up	+10$^\circ C$/min	Nitrogen: 3.0 Oxygen: 0.3	40	
Stabilize	1000	Nitrogen: 3.0 Oxygen: 0.3	3.0	
Oxidation	1000	Oxygen: 2.25 Hydrogen: 3.85	11	Target 100 nm oxide thickness
Cool down	-7$^\circ C$/min	Oxygen: 2.25 Hydrogen: 3.85	60	
Boat out	600	Nitrogen: 3.0	5	

15. **MEASUREMENT OXIDE THICKNESS**
Use the Leitz MPV-SP measurement system to measure the oxide thickness:

Progam:	Th. SiO2 on Si, >50nm auto5pts
Oxide thickness	100 nm on the process wafers

PART5: METALLIZATION

16. **Ti/Au EVAPORATION**
    Use the CHA evaporator in CR10000 to deposit 20200 nm of Ti/Au. Contaminated after this step.

PART6: NANOPARTICLE PASTE STENCIL PRINTING

17. **MANUAL COATING AND BAKING**
    The process starts with a manual pre-treatment with HMDS vapor with Nitrogen as the carrier gas. This will ensure the adhesion of the resist with the wafer surface. This will be followed using Brewer Science Spinner in the Polymer Lab to manually coat the wafers with resist, and following the instructions specified for this equipment.

    The coating is done with AZ NLOFT negative photoresist with a thickness of 2.1 μm, spin speed of 1500 rpm, and a spin time of 30-60 sec, and a soft bake at 95 $°C$ for 60 seconds.

    Use the chuck for Cu contaminated samples and the hotplate for contaminated wafers

18. **ALIGNMENT AND EXPOSURE**
    Processing will be performed on the Suss MA8 and follow the operating instructions from the manual when using this machine. Use the contaminated chuck. Mask: Cu_ Ring (glass mask) Exposure time: 55mJ cm^2 (exposure time: check calibration log of Suss s)

19. **MANUAL DEVELOPMENT**
    Use a hotplate to manually develop the wafers. Post-exposure bake: 115 $°C$ for 90 seconds on hotplate for contaminated wafers. Development: Shipley MF322 developer for 2 mins (Check in the logbook) Hard bake: 100 $°C$ for 90 seconds on hotplate for contaminated wafers.

20. **INSPECTION**
    Visually inspect the wafers through a microscope, and check openings. Put a tissue underneath the wafer.

21. **COPPER NANOPASTE STENCIL PRINTING**
    Screen printing of a copper nanoparticle paste on the bottom wafer using a manual a squeegee fill blade from KOENEN Technologies with a 65° hardness or a normal blade. A drop of copper nanoparticle paste is deposited on the photoresist, and it is wiped on the front side of wafer in all directions.

22. **DRYING**
    Use a hot plate to dry the wafer for 5 minutes at 50 degC.

23. **LIFT-OFF**
    Hot bath in N-Methy1-2-pyrrolidone (NMP) for 1 minute at 70 degC.

24. **RINSING AND DRYING**
    Rinsing in DEMI Water and spin-drying using copper chuck.

PART7: OXIDATION

Wafer bonding is performed in the AML bonder between the top and bottom wafer. Bonding parameters are depicted in Chapter 6.

Acronyms and abbreviations

3D	Three-dimensional
5G	The fifth generation mobile network
CMP	Chemical mechanical polishing
CNA	Common neighbour analysis
CSAM	Confocal scanning acoustic microscopy
CTE	Coefficient of thermal expansion
CTOD	Crack tip opening displacement
DfR	Design for Reliability
DMM	Digital multimeter
DoEs	Design of experiments
DRIE	Deep reactive ion etching
DUT	Device under test
DXA	Dislocation analysis
EAM	Embeded atom method
EBSD	Electron backscatter diffraction
EDX	Energy dispersive X-ray
EV	Electric vehicles
FCC	Face-centered cubic
FEA	Finite element analysis
FEM	Finite element methods
FIB	Focus ion beam
GND	Geometrically necessary dislocations
HAGB	High-angle grain boudries
HCP	Hexagonal close-packed
HI	Heterogeneous integration
HIR	Heterogeneous integration roadmap
I/O	Input/Output
IC	Integrated circuits
IGBT	Insulated-gate bipolar transistor
IQ	Image quality
LAGB	Low-angle grain boundaries
LAMMPS	Large-scale Atomic/Molecular Massively Parallel Simulator

LEAM	Linear elastic fracture mechanics
LED	light-emitting diode
LM	Levenberg-Marquardt
MC	Micro-cantilever
MD	Molecular dynamic
MEMS	Microelectromechanical systems
MOSFET	Metal-oxide-semiconductor field-effect transistor
MtM	More-than-Moore
NP	Nanoparticle
NPT	Isothermal-isobaric
NVE	Microcanonical
NVT	Canonical
PECVD	Plasma-enhanced chemical vapor deposition
QFN	Quad-flat package
RB	Ribbon bonding
RDL	Redistribution layers
ReaxFF	Reactive force-field
RF	Radio frequency
RTD	Resistance temperature detector
SA	Simulated annealing
SAM	Scanning acoustic microscopy
SEM	Scanning electron microscope
SF	Stacking faults (Chapter 2); Structure function (Chapter 4)
SFE	Stacking fault energy
SiP	System-in-package
SLID	Solid-liquid inter-diffusion
SMU	Source-Measure unit
TIM	Thermal interface materials
TB	Twinning boundary
TCT	Thermal cycling test
TDIM	Transent dual interface method
TO-247	Transistor outline 247
TSEPs	Thermo-sensitive electrical parameters
TSP	Temperature sensitivity parameter
TST	Thermal shock test
TSV	Through-silicon-via
TTC	thermal test chip
UGO	Universal global optimization
VOI	Volume of interest
WB	Wire bonding
WBG	Wide bandgap
XRD	X-ray diffraction

PERIODIC TABLE OF THE ELEMENTS AND MATERIALS

1 IA 1A	2 IIA 2A	3 IIIB 3B	4 IVB 4B	5 VB 5B	6 VIB 6B	7 VIIB 7B	8	9 VIII 8	10	11 IB 1B	12 IIB 2B	13 IIIA 3A	14 IVA 4A	15 VA 5A	16 VIA 6A	17 VIIA 7A	18 VIIIA 8A
1 **H** Hydrogen 1.008																	2 **He** Helium 4.003
3 **Li** Lithium 6.941	4 **Be** Beryllium 9.012											5 **B** Boron 10.811	6 **C** Carbon 12.011	7 **N** Nitrogen 14.007	8 **O** Oxygen 15.999	9 **F** Fluorine 18.998	10 **Ne** Neon 20.180
11 **Na** Sodium 22.990	12 **Mg** Magnesium 24.305											13 **Al** Aluminum 26.982	14 **Si** Silicon 28.086	15 **P** Phosphorus 30.974	16 **S** Sulfur 32.066	17 **Cl** Chlorine 35.453	18 **Ar** Argon 39.948
19 **K** Potassium 39.098	20 **Ca** Calcium 40.078	21 **Sc** Scandium 44.956	22 **Ti** Titanium 47.867	23 **V** Vanadium 50.942	24 **Cr** Chromium 51.996	25 **Mn** Manganese 54.938	26 **Fe** Iron 55.845	27 **Co** Cobalt 58.933	28 **Ni** Nickel 58.693	29 **Cu** Copper 63.546	30 **Zn** Zinc 65.38	31 **Ga** Gallium 69.723	32 **Ge** Germanium 72.631	33 **As** Arsenic 74.922	34 **Se** Selenium 78.971	35 **Br** Bromine 79.904	36 **Kr** Krypton 83.798
37 **Rb** Rubidium 85.468	38 **Sr** Strontium 87.62	39 **Y** Yttrium 88.906	40 **Zr** Zirconium 91.224	41 **Nb** Niobium 92.906	42 **Mo** Molybdenum 95.95	43 **Tc** Technetium 98.907	44 **Ru** Ruthenium 101.07	45 **Rh** Rhodium 102.906	46 **Pd** Palladium 106.42	47 **Ag** Silver 107.868	48 **Cd** Cadmium 112.414	49 **In** Indium 114.818	50 **Sn** Tin 118.711	51 **Sb** Antimony 121.760	52 **Te** Tellurium 127.6	53 **I** Iodine 126.904	54 **Xe** Xenon 131.294
55 **Cs** Cesium 132.905	56 **Ba** Barium 137.328	57-71	72 **Hf** Hafnium 178.49	73 **Ta** Tantalum 180.948	74 **W** Tungsten 183.84	75 **Re** Rhenium 186.207	76 **Os** Osmium 190.23	77 **Ir** Iridium 192.217	78 **Pt** Platinum 195.085	79 **Au** Gold 196.967	80 **Hg** Mercury 200.592	81 **Tl** Thallium 204.383	82 **Pb** Lead 207.2	83 **Bi** Bismuth 208.980	84 **Po** Polonium [208.982]	85 **At** Astatine 209.987	86 **Rn** Radon 222.018
87 **Fr** Francium 223.020	88 **Ra** Radium 226.025	89-103	104 **Rf** Rutherfordium [261]	105 **Db** Dubnium [262]	106 **Sg** Seaborgium [266]	107 **Bh** Bohrium [264]	108 **Hs** Hassium [269]	109 **Mt** Meitnerium [278]	110 **Ds** Darmstadtium [281]	111 **Rg** Roentgenium [280]	112 **Cn** Copernicium [285]	113 **Nh** Nihonium [286]	114 **Fl** Flerovium [289]	115 **Mc** Moscovium [289]	116 **Lv** Livermorium [293]	117 **Ts** Tennessine [294]	118 **Og** Oganesson [294]

Lanthanide Series	57 **La** Lanthanum 138.905	58 **Ce** Cerium 140.116	59 **Pr** Praseodymium 140.908	60 **Nd** Neodymium 144.243	61 **Pm** Promethium 144.913	62 **Sm** Samarium 150.36	63 **Eu** Europium 151.964	64 **Gd** Gadolinium 157.25	65 **Tb** Terbium 158.925	66 **Dy** Dysprosium 162.500	67 **Ho** Holmium 164.930	68 **Er** Erbium 167.259	69 **Tm** Thulium 168.934	70 **Yb** Ytterbium 173.055	71 **Lu** Lutetium 174.967
Actinide Series	89 **Ac** Actinium 227.028	90 **Th** Thorium 232.038	91 **Pa** Protactinium 231.036	92 **U** Uranium 238.029	93 **Np** Neptunium 237.048	94 **Pu** Plutonium 244.064	95 **Am** Americium 243.061	96 **Cm** Curium 247.070	97 **Bk** Berkelium 247.070	98 **Cf** Californium 251.080	99 **Es** Einsteinium [254]	100 **Fm** Fermium 257.095	101 **Md** Mendelevium 258.1	102 **No** Nobelium 259.101	103 **Lr** Lawrencium [262]

NMP	N-Methyl-2-pyrrolidone
Cu_2O	Copper(I) oxide
GaN	Gallium nitride
IPA	Isopropyl alcohol
PEN	Polyethylene naphtholate
PET	Polyethylene terephthalate
SAC	Sn-Ag-Cu
SiC	Silicon carbide
SiO_2	Silicon dioxide

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List of Publications

Journal Papers

1. **D. Hu**, A. Roshanghias, X. Liu, E. de Bruin, S. Vollebregt, J. Fan, T. Basler & G. Zhang. *Thermal-mechanical reliability evaluation on silver and copper nanoparticles sintered TO247 power devices*, IEEE Trans. Components, Packag. Manuf. Technol. (2024), Under Review.

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