A High-Precision Particle Detection ROIC With an Active Shaper in 40 nm CMOS with Sub 200 aC Sensitivity

Zaki, Alireza Mohammad; Nihtianov, Stoyan

DOI
10.1109/ISIE54533.2024.10595727

Publication date
2024

Document Version
Final published version

Published in
2024 33rd International Symposium on Industrial Electronics, ISIE 2024 - Proceedings

2024 IEEE 33rd International Symposium on Industrial Electronics (ISIE) | 979-8-3503-9408-5/24/$31.00 ©2024 IEEE | DOI: 10.1109/ISIE54533.2024.10595727

A High-Precision Particle Detection ROIC With an Active Shaper in 40 nm CMOS with Sub 200 aC Sensitivity

Alireza Mohammad Zaki
Department of Microelectronics
Delft University of Technology
Delft, The Netherlands
A.R.Mohammadzaki@tudelft.nl

Stoyan Nihtianov
Department of Microelectronics
Delft University of Technology
Delft, The Netherlands
S.Nihtianov@tudelft.nl

***Abstract*— Accurate registration of weak charge signals with a high event rate is the most challenging requirement of state-of-the-art detector readout frontends. This has given rise to the development of a wide variety of low-noise power-efficient readout frontends with a trend in achieving an ultra-small detection error and small silicon area occupation. This paper presents the methodology and experimental characterization of a state-of-the-art particle detection ROIC (readout integrated circuit) employing an active shaper after the frontend charge-sensitive amplifier (CSA), with: high time resolution (2.5 ns), low-noise, and very good power-efficiency, for registering charge signals between 140 aC and 200 aC, resulting from particles impinging in a silicon PIN detector. The small silicon area occupation of the readout electronic circuit allows a small detector area, which, in backside illumination/exposure mode, provides the opportunity for the pixelization of the total detector area with close to a 100 % fill factor. Experimental verification tests indicate that the proposed ROIC, designed in TSMC 40 nm MS/RF CMOS technology, operates with 3-sigma error rates between 1.8 ppm and 1.3 ppm (parts per million), with the above-mentioned charge signal range, provided that no more than one particle hits the detector surface in a 2.5 ns period of time. The power consumption is 0.37 mW.**

Keywords*— *readout integrated circuit ROIC, analog frontend, charge-sensitive amplifier, signal shaper block, low-offset, low-noise, power-efficient, high time resolution

I. Introduction

In the ever-evolving landscape of industrial technology, highly sophisticated instrumentation and imaging devices have transformed into influential tools for inspection and metrology. Progress in electronics, paired with the widespread integration of high-resolution pixelated detectors, has not only facilitated but also propelled the development of intricate investigation techniques, widely employed across diverse scientific disciplines and practical applications [1]. A notable example of this advancement is found in scanning electron microscopes (SEMs), where nanometer-resolution images of specimen surfaces are achieved using highly pixelated semiconductor p-n junction-based detectors. Within SEMs, the detector is complemented by a readout integrated circuit (ROIC) designed to process the charges generated by particles interacting with the detector.

A significant challenge confronting cutting-edge charge readout frontends is the precise registration of weak, high-event-rate charges generated by detectors. This challenge arises from the need to detect a series of subtle events with an unprecedentedly low error rate – less than 1 ppm (parts per million) – and with a high time resolution manifested in the nanosecond range. Addressing this challenge mandates the implementation of a high-bandwidth, low-noise readout frontend with modest power consumption, ensuring the mitigation of thermal heating and bias drift across the entire frontend [2].

The key performance indicator in detecting charge signals is the error rate, which can be compromised by either noise or inter-symbol interference (ISI). ISI refers to the signal pileup at the output of a low-bandwidth stage [3]. The delicate interplay between noise and ISI necessitates an optimal bandwidth that strikes a balance in error rates between the two factors [4], [5]. The ultimate goal is to detect charge signals smaller than 200 aC (equivalent to 1250 electrons) with a resolution of 2.5 ns at the moment of occurrence. This level of precision permits an event rate of up to 400 MEvents/s. Another challenge is to keep the power consumption as low as possible. In the targeted applications it has to be less than 500 µW [4] - [6].

Current readout frontends, designed to handle fast and low-energy particles with exceptional time resolution and accuracy, exceed the specified power requirements [7] – [9]. Conversely, the low-power readout frontends reported in the literature fall short in delivering the required detection accuracy for a high rate of charged particles [10] – [12]. Consequently, the need for a novel readout frontend is evident – one that not only offers a high time resolution and accuracy for detecting low-energy particles but does so with reasonable power consumption.

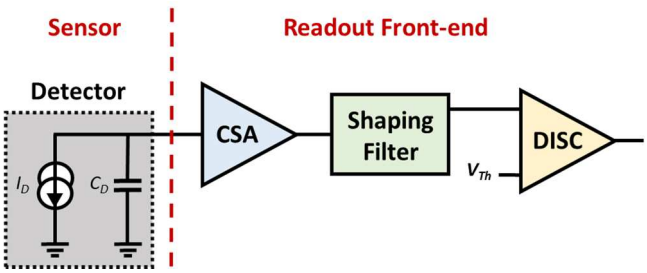

Fig. 1. Simplified block diagram of the analog readout frontend.

In prior publications, we already presented the design and the experimental validation of each functional block of the ROIC with the architecture depicted in Fig. 1 [6, 13, 14]. In

[15] we reported a solution based on the same architecture (Fig. 1) utilizing a passive high-pass filter. While this readout frontend exhibits the ability to detect charge signals with commendably low power consumption, its detection accuracy falls short of specifications due to periodic deadtime imposed by the discriminator for offset reduction through autozeroing.

To address this limitation, we propose a solution by substituting the passive shaping filter with an active shaping filter, as demonstrated in [13]. By amplifying the signal by the active shaping filter, the significance of the discriminator offset is diminished, allowing for the elimination of the autozeroing process and the associated deadtime.

Section II details the setup and the main functional blocks of the readout frontend. In Section III, we discuss the experimental test setup and address the measurement challenges. Section IV shares the measured performance results, demonstrating how accurately the ROIC captures charge signals triggered by various particle arrival patterns. Finally, the paper concludes with a summary.

II. Readout Frontend Architecture

The readout frontend generates a digital logic pulse for every particle that hits the detector. To achieve this, an analog frontend that connects the detector to the digital backend is essential. To meet the specifications for noise level and power consumption, the analog frontend compromises on bandwidth. However, this trade-off results in a higher error rate, primarily influenced by Inter-Symbol Interference (ISI) [16]. Given that ISI is a deterministically sourced error, it can be mitigated with a certain level of architectural complexity. To address this, the signal in the analog frontend can be shaped using a band-pass filter stage, which compensates for ISI-induced errors during the detection and digitization of charge signals. This helps in reducing the overall error rate.

Illustrated in its simplest form in Fig. 1, the ROIC consists of a charge-sensitive amplifier (CSA) responsible for converting charge to voltage, characterized by a specific input noise and signal bandwidth. Additionally, a signal shaping filter is incorporated to generate an output signal with a well-defined shape, and a threshold discriminator (DISC) is utilized to distinguish the signal from the noise floor, ultimately providing a digital output.

The charge-sensitive amplifier (CSA) plays a pivotal role in converting each charge signal into an output voltage signal. As depicted in Fig. 2, it comprises a core amplifier followed by a current conveyor stage known as an ICON Cell in the feedback network, intended to implement a large feedback resistance. As an example, for an input charge of 160 aC, (1000 electrons) the resulting output voltage signal is $V_{CSA} = 29.45\ \text{mV}$ with a signal-to-noise ratio of $\text{SNR} = 20.59$. Despite the rapid rise time of the voltage signal $t_r = 2.56\ \text{ns}$, it exhibits a relatively prolonged tail, leading to a signal width of $t_{width} = 286.91\ \text{ns}$. Additionally, the drift of the DC level (offset) at the CSA output requires enhanced control to preserve detection accuracy, as discussed in [4], [14]. The extended tail of the voltage signal, a consequence of the CSA's limited bandwidth ensuring a robust SNR, can, however, impact detection accuracy. This lingering tail, coupled with the offset drift at the CSA output, poses potential challenges to accurate signal detection [4], [14]. The experimentally validated power consumption of the CSA is 140 µw [6].

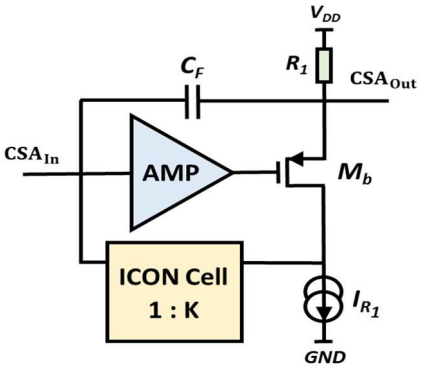

Fig. 2. Simplified schematic of the CSA with the ICON Cell.

The active shaping filter (Fig. 3) plays a crucial role in refining the output voltage signal from the CSA. Its primary function is to eliminate the lingering tail and associated offset by implementing a band-pass transfer function, thereby generating output signals within 2.5 ns time frames. The shaper achieves this by attenuating the offset at the CSA output by a factor of 17 and amplifying the CSA signal over 7 times. Consequently, the shaper produces an output voltage of $V_{shaper} = 220.4\ \text{mV}$, accompanied by an $\text{SNR} = 13.7$ and a time-width of $t_{shaper} = 2.91\ \text{ns}$ for each voltage signal provided by the CSA. This operation is achieved with a power consumption of 170 µw [14].

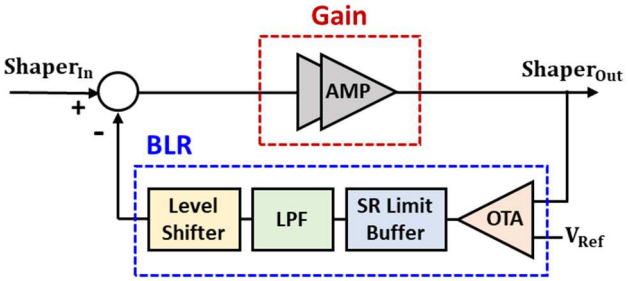

Fig. 3. Block diagram of the active shaping filter.

The performance of the active shaping filter reduces the influence of the input offset and noise on the discriminator, contributing to its power-efficient design. The discriminator generates a digital logic pulse when the output signal of the shaper surpasses a predefined threshold level V_{Th}. As shown in Fig. 4, it comprises a differential OTA serving as a preamplifier to compare the input signal with the threshold voltage V_{Th}, followed by two inverters designed to enhance the logic levels at the output while minimizing the delay time [15]. The threshold level V_{Th} is typically set within the range of 6 to 8 times the total noise $\sigma_{noise} = 16.08\ \text{mV}_{rms}$ to achieve high detection accuracy. For instance, with a threshold level set at 8 times the noise voltage ($8 \times \sigma_{noise}$), the discriminator generates digital pulses with a time width of $t_{disc} = 1.71\ \text{ns}$, which is within the target time frame of 2.5 ns. The power consumption of the discriminator is 60 µw.

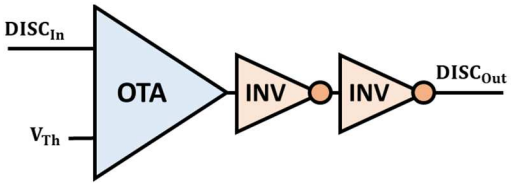

Fig. 4. Block diagram of the discriminator.

III. Test Setup for Experimental Qualification

Accurate characterization and evaluation of the particle detection ROIC demand precise laboratory equipment and a dedicated test setup. A FPGA-based Data Acquisition Board (DAB) DE10-Standard is used for programming the chip and testing the performance of the ROIC. The communication between the FPGA and the ROIC is done via high-speed low-voltage differential signal (LVDS) interface. To safeguard the test setup and the chip from noise interference, isolation buffers are employed to channel all FPGA signals. Figure 5 provides a photograph of the test setup PCB.

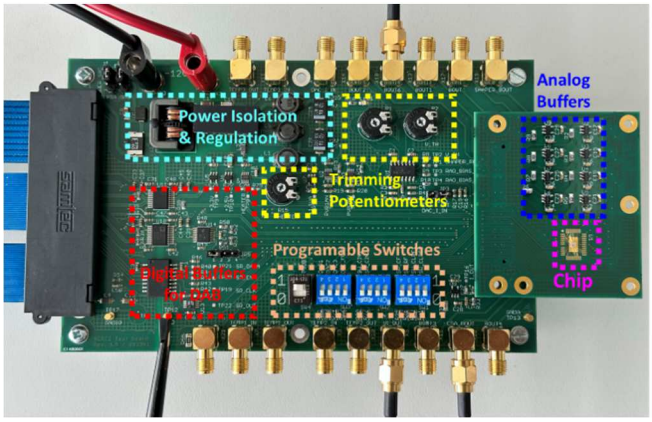

Fig. 5. PCB designed for experimental qualification of the chip.

To enhance the testability of the analog readout frontend, supplementary auxiliary and peripheral blocks are integrated into the same chip, as depicted in Fig. 6. These auxiliary and peripheral blocks encompass a detector emulator for generating input charge pulses, wide-bandwidth voltage buffers to mitigate loading effects during signal monitoring, a power regulator stage for proper biasing, and a programmable shift register followed by a set of configuration switches to modify the operating modes of the building blocks. During the chip programming phase, various parameters for the readout frontend can be configured, including the equivalent detector capacitance C_D (Fig. 1), the feedback components of the CSA C_F and R_1 (Fig. 2) determining its gain and time constant, and the low-pass filter capacitor C_{LPF} (Fig. 3) influencing the bandwidth of the active shaping filter.

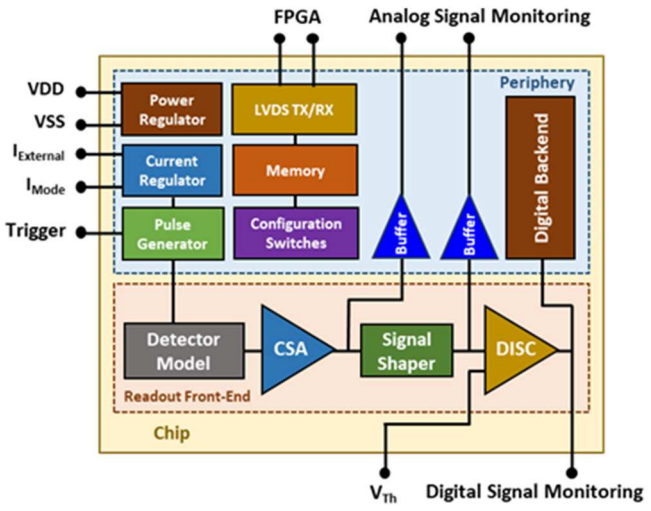

Fig. 6. Additional auxiliary and peripheral blocks to facilitate the testability of the performance.

In this study, with a focus on the operational accuracy and performance of the ROIC, the detector is substituted by an equivalent network designed to model its characteristics. As demonstrated in [16], the shape of the voltage signal post-CSA becomes less dependent on the shape of the input charge pulse, owing to the significantly larger time constant of the CSA compared to the time width of the charge pulse. As highlighted in [6], this network comprises an array of capacitors in parallel with a digitally controlled current source (DCCS), representing the equivalent capacitance of the detector $C_D = 50$ fF and equivalent charge pulse, respectively. The DCCS is responsible for generating a charge pulse with the desired equivalent charge and duration for every trigger signal provided by the DAB.

IV. Experimental Results

The prototype of the readout frontend, comprising the CSA, the active shaping filter, and the discriminator, is produced using the TSMC 40 nm CMOS process. Figure 7 depicts the micrograph of the chip, directly bonded to the PCB, featuring a matrix of 3×4 readout channels. Experimental tests are conducted to assess the operating principles and characterize the performance of the readout frontend across various detector charge signals (Q_{in}) spanning from 140 aC to 200 aC. The proposed readout frontend has a power consumption of 0.37 mW.

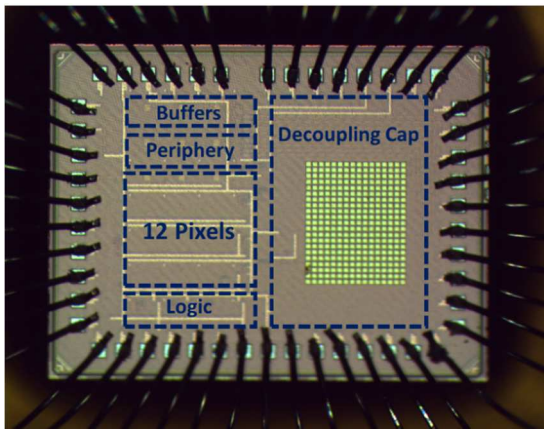

Fig. 7. Chip micrograph.

In the experimental assessment of the readout frontend performance, the DAB generates a series of trigger signals based on digital codes stored in a register labeled ‘trigger register’. Each trigger signal precisely delineates the status of the detector within 2.5 ns timeframes, where the logic state ‘1’ signifies the occurrence of a particle landing on the detector surface. For this test series, the assumption is made that particles consistently land on the detector surface at the outset of each timeframe.

To validate the precise moment of signal detection with a resolution of 2.5 ns, a reference clock generator operating at 400 MHz frequency is implemented on the DAB. Simultaneously, the DAB collects the digital data generated by the readout frontend, allocating them to a register labeled ‘data register’. The performance algorithm of the DAB as depicted in Fig. 8.

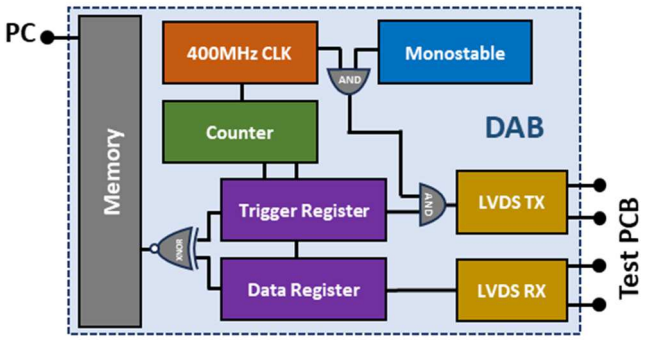

Fig. 8. Simplified block diagram of the DAB code.

Comparing the logical state patterns in both the trigger and data registers, the DAB performs a comparative analysis to evaluate the detection error rate and operational accuracy of the designed readout frontend. The *"true"* counts represent the number of bits where the logical state of the trigger and data registers align. However, in certain instances, due to the inherent noise of the readout frontend, the discriminator may generate additional digital pulses and assign them to subsequent time frames in the data register, resulting in *"erroneous"* counts. Furthermore, any triggers missed by the discriminator are categorized as *"missed"* counts. The combined total of *erroneous* and *missed* counts is denoted as *"incorrect"* counts. The error rate is subsequently computed as the ratio of *incorrect* counts to the total number of logical states of '1' in the trigger register. This comprehensive evaluation methodology enables a thorough assessment of the readout frontend performance and detection accuracy under various conditions.

In all conducted tests, each charge signal generated by the DCCS consistently maintains a time width of 1.8 ns (concerning the detector time constant) while the signal amplitude is tunable to generate the input charge of interest. As mentioned earlier, the goal is to detect charge signals Q_{in} spanning from 140 aC to 200 aC. This translates to a current signal featuring an amplitude spanning from 78 nA to 112 nA with a fixed time width of 1.8 ns. Notably, these values remain comfortably below the targeted charge of 200 aC. It is reasonable to anticipate even further improved performance with a larger input charge, as this adjustment would likely result in a better SNR. Table I summarizes the measured characteristics of the signal after the CSA and the active shaping filter for different values of detector charge signals.

TABLE I. MEASURED CHARACTERISTICS OF THE SIGNAL AFTER THE CSA AND THE ACTIVE SHAPING FILTER FOR DIFFERENT VALUES OF DETECTOR CHARGE SIGNALS

Q_{in} [aC]	CSA		Shaping Filter	
	V_{Amp} [mV]	SNR	V_{Amp} [mV]	SNR
140	25.81	18.13	192.9	12
160	29.45	20.59	220.4	13.7
180	23.26	23.26	248.1	15.4
200	36.64	25.62	247.8	17.1

To ensure precise and consistent data across all experimental test scenarios, the readout frontend undergoes 100 firing cycles via the trigger code, and the outcomes are subsequently averaged. For detector charge signal $Q_{in} =$ 160 aC, Fig. 9 illustrates the average count of *erroneous* and *missed* counts relative to the threshold level in the discriminator. This evaluation is conducted under the condition where the readout frontend is triggered by 10^8 well-separated charge pulses in each firing cycle, with a trigger period of 250 ns (equivalent to an event rate of 4 MHz).

Analyzing the presented data, the optimal threshold level is identified as $V_{th} = 105$ mV. At this threshold level, the average count of *erroneous* and *missed* counts is nearly equivalent. This equilibrium signifies a balanced performance where the readout frontend effectively mitigates both types of errors (in applications where this is acceptable) highlighting the efficacy of this particular threshold setting. Such an experiment can be performed for other values of detector charge signal to evaluate the optimum threshold level.

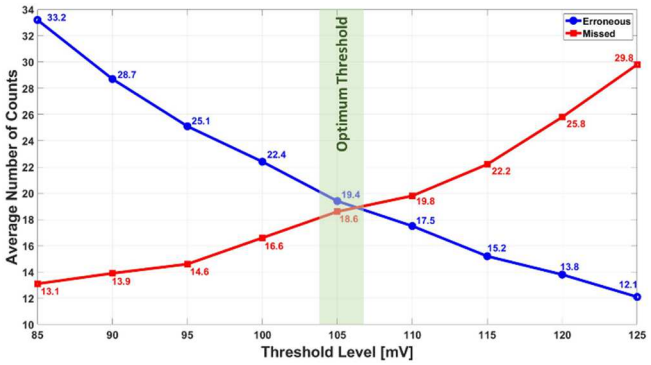

Fig. 9. Average number of *erroneous* (blue) and *missed* (red) counts as a function of the discriminator threshold level for $Q_{in} = 160$ aC.

To probe the operation accuracy of the readout frontend when 2 or 3 consecutive events occur in consecutive time frames, using the optimum threshold level, a trigger code is used in every trigger period of 250 ns, which can be illustrated by logic states '110000….' and '111000….', respectively. Figure 10 illustrates the digital pulses generated by the frontend for the aforementioned trigger codes in blue and red, respectively. This analysis provides insights into the ability of the frontend to accurately respond to and register consecutive events within rapid timeframes. The measured propagation delay of the readout frontend is 1.83 ns, attesting to its swift and accurate response in capturing consecutive events occurring in quick succession.

Furthermore, it is imperative that the readout frontend refrains from generating any digital pulses at its output in the absence of charge generated by the detector, indicated by an all-zero trigger code. Digital pulses generated in this scenario are termed *"dark"* counts, attributed to the inherent noise within the readout frontend building blocks. To evaluate this aspect, the digital output of the readout frontend is systematically recorded for a specified duration while the entire trigger register maintains a logic state of '0'. Conducting this test 100 cycles, Fig. 11 illustrates the average *dark* counts as a function of the threshold level, spanning a measurement time equivalent to 10^{10} time frames in each cycle. The average number of *dark* counts diminishes with a larger threshold; however, these counts remain negligible in comparison to the number of *incorrect* occurrences across all threshold levels. This is attributed to the conservative setting of the threshold, maintained at levels greater than 6 times the noise power.

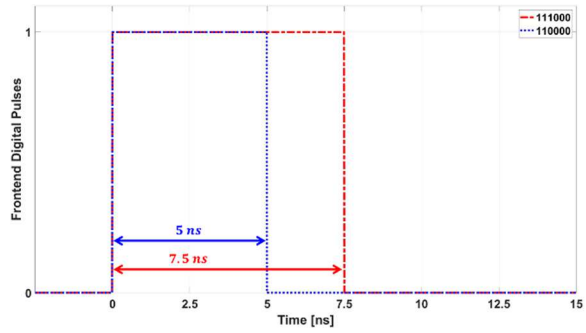

Fig. 10. Digital pulses generated by the frontend for '110000….' and '111000….' trigger codes in blue and red, respectively.

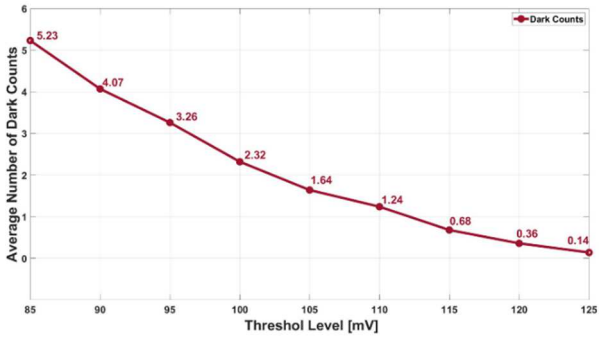

Fig. 11. Average number of *dark* counts as a function of the threshold level.

To evaluate the effectiveness of the proposed architecture and estimate the detection error rate, the readout frontend is activated by a trigger code consisting of 10^8 Poissonian-distributed logic states of '1'. In a series of 100 iterations of the experimental test for $Q_{in} = 160$ aC, Fig. 12 illustrates the average error rate μ_{error} (in blue) along with the corresponding standard deviation σ_{error} (in black) as a function of the threshold level. Additionally, the 3-sigma error rate, calculated through $Error_{3\sigma} = \mu_{error} + 3 \times \sigma_{error}$ error, is highlighted in red. This visualization provides a comprehensive overview of the system performance and the impact of threshold levels on error rates. For instance, at the optimum threshold level $V_{Th} = 105$ mV, the average error rate of the proposed architecture is calculated as $\mu_{error} = 0.63$ ppm with a standard deviation of $\sigma_{error} = 0.28$. This corresponds to a 3-sigma error rate of $Error_{3\sigma} = 1.47$ ppm. Figure 13 denotes the 3-sigma error rate as a function of threshold level for various detector charge signals (Q_{in}) spanning from 140 aC to 200 aC. As anticipated, larger input charge provides further improved performance as this adjustment would likely result in a better SNR.

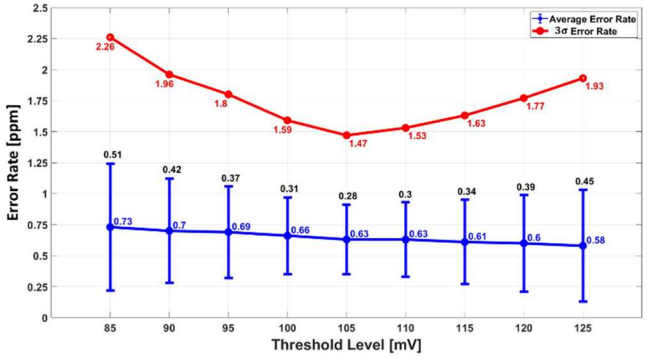

Fig. 12. Average error rate along with the corresponding standard deviation, as well as the 3-sigma error rate, as a function of the threshold level for $Q_{in} = 160$ aC.

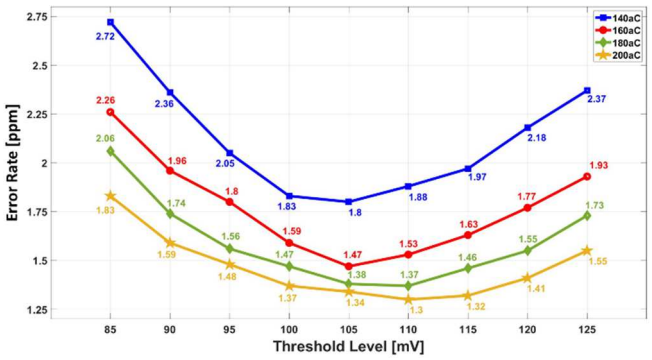

Fig. 13. The maximum error rate as a function of the threshold level for various detector charge signals (Q_{in}) spanning from 140 aC to 200 aC.

V. Conclusions

The reported readout frontend is proposed as a solution to the conflicting requirements of a small input signal, high time resolution, and low power consumption in readout integrated circuits. We report the experimental qualification of a previously presented architecture of a state-of-the art particle detection ROIC implemented in 40 nm CMOS technology. The ROIC demonstrates the capability to register charge signals smaller than 200 aC generated by charged particles landing on a PIN detector surface, achieving a very low error rate with a very good power efficiency and excellent time resolution.

Through comprehensive experimental qualification tests, the proposed ROIC exhibits compelling performance. The detection error rate is assessed across various threshold levels, assuming no more than one electron hits the detector surface within a 2.5 ns period. For an input charge ranging from 140 aC to 200 aC, optimal threshold levels yield 3-sigma error rates from 1.8 ppm to 1.3 ppm, respectively. With an input charge of 160 aC and an optimal threshold level of $V_{Th} = 105$ mV, the frontend achieves an average error rate of only 0.63 ppm. The ROIC operates with a total power consumption of 0.37 mW. These results underscore the effectiveness of the designed readout frontend in meeting stringent requirements for precision and energy efficiency.

Acknowledgment

This work started as a master's research project [16] and has been extended into a Ph.D. project at TU Delft, the Netherlands, supported by the Dutch Top Consortium for Knowledge and Innovation (TKI) HTSM.

References

[1] I. Fleck, M. Titov, C. Grupen, and I. Buvat, Handbook of Particle Detection and Imaging, 2nd ed., Cham: Springer, 2021.

[2] M. Nakhostin, "Pulses from Ionization Detectors," in Signal Processing for Radiation Detectors, New York: John Wiley & Sons, 2017.

[3] E. Säckinger, "Analysis and Design of Transimpedance Amplifiers for Optical Receivers," John Wiley & Sons, 2017.

[4] M. A. Disi, A. Mohammad Zaki, Q. Fan and S. Nihtianov, "High-count rate, low power and low noise single electron readout ASIC in 65nm CMOS technology," 2021 XXX International Scientific Conference Electronics (ET), pp. 1-5, 2021.

[5] A. Mohammad Zaki and S. Nihtianov, "High Time Resolution, Low-Noise, Power-Efficient, Charge-Sensitive Amplifier in 40 nm Technology," 2022 XXXI International Scientific Conference Electronics (ET), pp. 1-6, 2022.

[6] A. Mohammad Zaki and S. Nihtianov, "Experimental Qualification of a Low-Noise Charge-Sensitive ROIC with Very High Time

Resolution," 2023 IEEE 32st International Symposium on Industrial Electronics (ISIE), Helsinki-Espoo, Finland, 2023.

[7] M. Ciobanu, N. Herrmann, K. D. Hildenbrand, M. Kis, A. Schuttauf, H. Flemming, H. Deppe, S. Lochner, J. Fruhauf, I. Deppner, P. A. Loizeau, and M. Trager, "PADI, an Ultrafast Preamplifier - Discriminator ASIC for Time-of-Flight Measurements," IEEE Transactions on Nuclear Science, vol. 61, no. 2, pp. 1015–1023, 2004.

[8] F. Anghinolfi, P. Jarron, F. Krummenacher, E. Usenko, and M. Williams, "NINO, an Ultra-Fast, Low-Power, Front-End Amplifier Discriminator for the Time-Of-Flight Detector in ALICE Experiment," IEEE Nuclear Science Symposium. Conference Record (IEEE Cat. No. 03CH37515), vol. 1, pp. 375-379, 2003.

[9] R. Kleczek, P. Grybos, R. Szczygiel and P. Maj, "Single Photon-Counting Pixel Readout Chip Operating Up to 1.2 Gcps/mm2 for Digital X-Ray Imaging Systems," in IEEE Journal of Solid-State Circuits, vol. 53, no. 9, pp. 2651-2662, Sept. 2018.

[10] R. Ballabriga et al., "The medipix3RX: A High Resolution Zero Dead-Time Pixel Detector Readout Chip Allowing Spectroscopic Imaging", J. Instrum., vol. 8, no. 2, 2013.

[11] H.-S. Kim, S.-W. Han, J.-H. Yang, S. Kim, Y. Kim, S. Kim, et al., "A Sampling-Based 128x128 Direct Photon-Counting X-Ray Image Sensor with 3 Energy Bins and Spatial Resolution of 60 um/pixel", IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp. 110-111, Feb. 2012.

[12] A. Peizerat, J. Rostaing, P. Ouvrier-Buffet, S. Stanchina, P. Radisson and E. Marché, "A 256 Energy Bin Spectrum X-Ray Photon-Counting Image Sensor Providing 8Mcounts/s/pixel and On-Chip Charge Sharing Charge Induction and Pile-Up Corrections", Proc. Symp. VLSI Circuits, pp. C246-C247, 2017.

[13] A. Mohammad Zaki and S. Nihtianov, "Low-Offset Band-Pass Signal Shaper with High Time Resolution in 40nm CMOS Technology," the 49th Annual Conference of the IEEE Industrial Electronics Society, Singapore, 16–19 October 2023.

[14] A. Mohammad Zaki, Yutong Du, S. Nihtianov, "Design and Qualification of a High-Speed Low-Power Comparator in 40nm CMOS Technology," submitted to the IEEE International Scientific Conference "Electronics'23", Sozopol, 13-15 September, 2023.

[15] A. Mohammad Zaki, Yutong Du, S. Nihtianov, "Low-Power High Time Resolution Charge Detection ROIC in 40nm CMOS Technology," submitted to the International Instrumentation and Measurement Technology Conference (I2MTC), Glasgow, Scotland, 2024.

[16] A. Mohammad Zaki and S. Nihtianov, "Characterization Challenges of a Low Noise Charge Detection ROIC," in IEEE Transactions on Instrumentation and Measurement, vol. 71, pp. 1-8, 2022.

[17] M. A. Disi, "Single Electron Readout Circuit: SERCuit," M.S. thesis, Dept. Microelectronics, TU Delft, Delft, the Netherlands, 2020.