A Capacitive Pressure Sensor Interface

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Introduction

This thesis describes the theory, design and realization of capacitive sensor interface for low pressure measurements, which is based on a generically used pressure readout architecture. The goal of this work is to realize a capacitive pressure sensor electronic interface, starting from an existing piezo-resistive pressure readout solution. So that a state-of-the-art general interface for capacitive and piezo-resistive low-pressure sensors can be realized. Also, this capacitive pressure sensor interface is aiming for interfacing various capacitive pressure sensors with sufficient measuring range.

The thesis is organized in 4 chapters, as follows:

Chapter 1: High Resolution Capacitive Pressure Sensor Interfaces: An Overview.
Chapter 2: Circuit-level Design and Simulation Results.
Chapter 3: Measurement results.
Chapter 4: Conclusion and Future Work.

Chapter 1 introduces the capacitive pressure sensors with piezo-resistive and capacitive technique, firstly. Then, capacitance measurement approaches, including direct and indirect conversion, are shown. System-level techniques based on the existing problems are discussed. Last, conclusions are made and the aim of the thesis is defined.

Chapter 2 is mainly focused on circuit-level analysis, starting from the explanation of the existing design. The block diagram and the circuit-level design of the proposed design are analyzed, including operating modes, transfer function, noise analysis and the selection of the feedback capacitor C_f. The simulation results are shown at the end of this chapter.

The measurement results are presented in Chapter 3, which includes the sensitivity, resolution, thermal drift and power consumption.

At the end, conclusions are made in Chapter 4 and possible future work is suggested.

Chapter 1

Capacitive Pressure Sensor Interfaces: An Overview

This chapter will provide an overview and detailed discussion of the state-of-the-art capacitive pressure sensor interface systems.

1.1 Capacitive Pressure Sensors

Since a long time, pressure sensors have been widely used in fields like automotive industry, manufacturing, aviation, bio-medical measurements, air-conditioning, hydraulic measurements etc. Pressure sensors generally use a force collector, based on the deflection induced by pressure acting on a spring or diaphragm, which is related to the magnitude of the force deployed. Besides force-collector pressure sensors, other pressure transducers exist which rely on material properties rather than the force, such as the density of a gas or fluid, the resonant frequency set up by pressure changes and the changes to a material's thermal conductivity in response to pressure fluctuations [1]. However, most of the very low pressure measurement applications are based on force-collector pressure sensors. The topic of this thesis: Capacitive Pressure Sensors based on the force-collector sensing principle.

Force-collector pressure sensors are now widely used to measure absolute pressure, differential pressure, gauge pressure and vacuum pressure, based mainly on piezo-resistive and capacitive techniques. The piezo-resistive pressure sensing technique is based on the change of the resistance of piezo-resistive material induced by stress as a result of a deflection of a diaphragm, whereas the capacitive pressure sensing method is based on detecting the displacement of a membrane due to pressure variation [2]. When compared to piezo-resistive pressure sensors, silicon-based micro-machined capacitive pressure sensors need a silicon diaphragm with extremely high aspect ratio area/thickness, in order to achieve high pressure sensitivity. As ultra-thin

silicon diaphragm is difficult to fabricate, capacitive pressure sensors often have large sensor size. Although capacitive pressure sensors are ideally noiseless, due to their relatively low sensitivity, the requirements of the electronic readout circuit for capacitive pressure sensors are more challenging. However, capacitive pressure sensors have low thermal drift and no power dissipation (unlike piezo-resistors) [3], which makes them attractive to develop.

A comparison between piezo-resistive and capacitive pressure sensing techniques is presented in the table 1-1 below [4] [5] [6] [7] [8] [9].

TABLE 1-1. COMPARISON BETWEEN PIEZO-RESISTIVE AND CAPACITIVE PRESSURE SENSORS.

Parameter	Piezo-resistive	Capacitive
Pressure Sensitivity	**Higher**	Lower
Size	**Compact**	Large
Range	0 to 200 psi	0 to 5000 psi
Thermal Drift	Higher	**Lower**
Stability	Good	**Excellent**
Noise	High	**NO**
Power Consumption	High	**NO**

Pressure measurement with sub-mPa resolution requires a capacitive readout circuit with attoFarad resolution. Our aim is to develop a capacitive pressure sensing interface based on an existing piezo-resistive interface. By achieving this, a state-of-the-art general interface for both: capacitive and piezo-resistive low-pressure sensors, will be realized.

In the following section, we shall present an overview of the working principle, structure, applications and main challenges of existing capacitive pressure sensors.

1.1.1 Structures of Capacitive Pressure Sensors

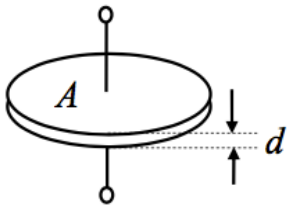


FIG. 1-1. A SIMPLIFIED CAPACITOR WITH FLAT PARALLEL PLATES.

As shown in Fig.1-1, the simplest structure of a capacitive sensor consists of two flat parallel plates with area *A* and distance between them *d*.

The capacitance between two parallel plates can be approximated as (when *d* is much smaller than the plate dimensions):

$$C_0 = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{1-1}$$

where ε_0 is the permittivity of the vacuum (ε_0 = 8.85×10^{-12} F/m), and ε_r is the relative permittivity of the dielectric between the two electrodes.

In the case of small displacement $\pm\Delta d$ ($\Delta d \ll d$), the capacitance value can be presented as:

$$C_x = \frac{\varepsilon_0 \varepsilon_r A}{d + \Delta d} = C_0 + \Delta C \approx C_0 - \frac{\varepsilon_0 \varepsilon_r A}{d^2} \cdot \Delta d \tag{1-2}$$

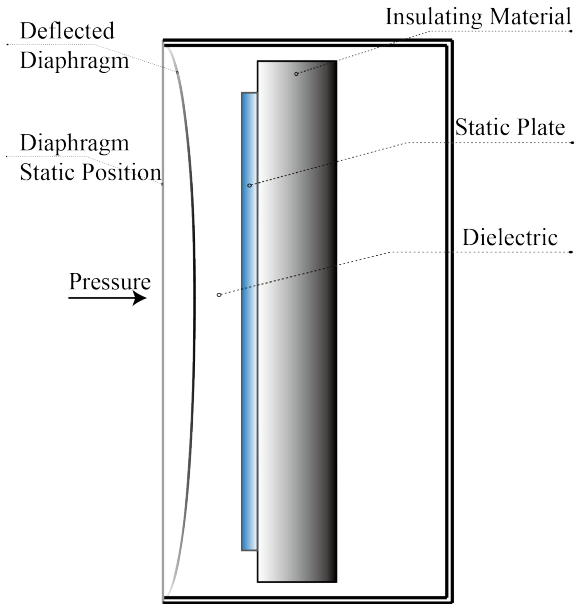


FIG. 1-2. CAPACITIVE PRESSURE SENSORS.

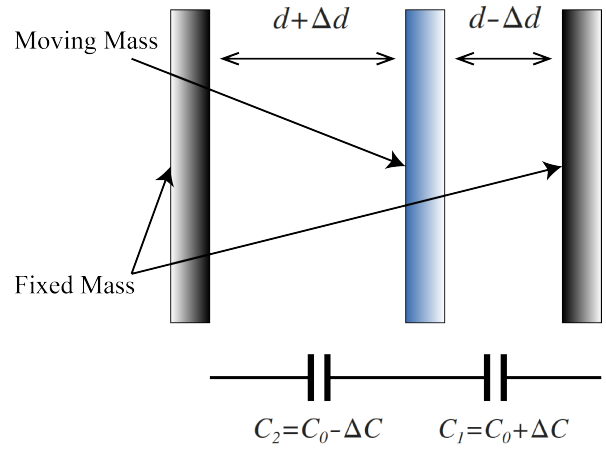
From expression 1-2, it is clear that the sensitivity of the sensor $\frac{\varepsilon_0 \varepsilon_r A}{d^2}$ is inversely proportional to the square of the standoff distance *d* and proportional to the electrode area *A*.

Capacitive pressure sensors use mainly *d* as a measurand (D-type), as this is very effective for short-range displacement measurements. Figure 1-2 shows how the distance between a diaphragm and a fixed place is changing with the pressure variation [10] [11].

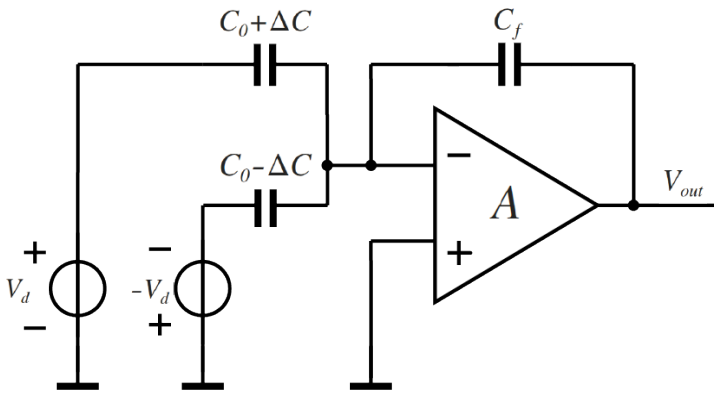
The topologies of the D-type capacitive pressure sensors can be classified into three main categories in terms of sensitivity.

1. Single Capacitive Pressure Sensors

Single capacitive pressure sensors have one sensing element whose capacitance C_x changes with pressure (Fig. 1-2) [12].



(A)



(B)

FIG. 1-3. (A) A SIMPLIFIED FULLY DIFFERENTIAL SENSOR STRUCTURE (B) READOUT CIRCUIT.

2. Differential Capacitive Pressure Sensors

The sensitivity to mechanical displacements can be improved by using a diaphragm between two fixed plates (see Figure 1-3). The three-plate sensor offers the well-known advantages of a differential system, such as rejection of common-mode interference and cancellation of the baseline value of the capacitance [13]. The detection circuit measures the difference between two capacitances rather than an absolute value of one capacitance [14]. The measured pressure value can be a function of the difference $(C_1 - C_2)$ or the ration $(\frac{C_1}{C_2})$ of the two capacitors.

The commercial off-the-shelf capacitive pressure sensors are based on the Silicon-capacitive (SCAP) technology, applicable mainly for: air handing systems, variable air volume (VAV), filter monitoring and duct air flow management. An example of capacitive pressure sensor is *P994*, supplied by *Kavlico.* This is a low range differential capacitive pressure sensor.

3. Bridge-type Capacitive Pressure Sensors

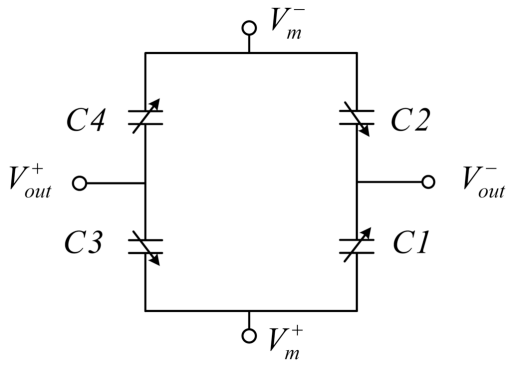


FIG. 1-4. A SIMPLIFIED STRUCTURE OF FULLY DIFFERENTIAL CAPACITIVE SENSORS.

Capacitive sensors in a bridge topology (Fig. 1-4) are frequently applied to measure pressure and linear or angular position. The sensitivity of fully differential capacitive bridge sensor is 4 times higher than the single capacitive pressure sensors. This is essential for special applications, which require high sensitivity to detect a small difference of capacitance. However, compared with single (two-terminal) and differential (three-terminal) capacitive pressure sensors, the capacitive-bridge sensors have a two-port configuration, which requires a fully differential readout circuit.

Generally, for obtaining higher sensitivity, more complex topology is needed. Furthermore, when the number of capacitors increases, the mismatch between them will introduce errors in the system.

In this part we explained the working principle and described different types of capacitive pressure sensors with examples. Next, a general analysis about the existing challenges will be introduced.

1.1.2 Existing Challenges

Table 1-1 indicates that the sensitivity of capacitive pressure sensors is lower than piezo-resistive pressure sensors, while no noise generated in capacitive pressure sensors. So, the requirements of the electronic readout circuits for capacitive pressure sensors are more challenging. This is relevant with the status of the existing capacitive pressure sensor measurements.

Next we shall discuss two major challenges with capacitive pressure sensor measurements.

1. Large Baseline Capacitance

When measuring very small movement (in the nanometer and sub-nanometer ranges) of the plate, the change of the capacitance is much lower than its baseline value, so that the response of the capacitive sensing is difficult to measure. Due to the baseline capacitance, the readout circuit will require higher dynamic range, higher resolution, higher power consumption and longer conversion time.

2. Low-frequency Interferences

Pressure can change very slowly. That is the reason that the signal bandwidth of the readout electronics has to include DC (start from 0 Hz). However, many interfering signals, such as offset, flicker noise and main supply interferences, are also located in the low-frequency domain, which may corrupt the sensor signal. In order to be able to sense the slowly changing input signals, we have to reduce the effect of the low-frequency interferences.

In the following section we shall address the possible solutions for the above-mentioned challenges.

1.2 Capacitance Measurement Methods

In the previous section, the operating principle and the existing problems of capacitive pressure sensors is presented. In this section, interface circuits which convert capacitance to electrical signal, especially for pressure sensing, are discussed.

The electronic interfaces of pressure sensors need to have very good performance at low cost. Different techniques to measure pressure by detecting capacitance variation have been reported. Based on the signal conversion, two types of interface approaches can be distinguished:

1. Direct Conversion: the unknown capacitance C_x is digitized directly into digital code by a capacitance-to-digital converter (CDC).

2. Indirect Conversion: the unknown capacitance C_x is first converted into an electrical signal, such as voltage, frequency, time, etc, and then digitized by an analog-to-digital converter (ADC).

1.2.1 Direct Conversion

When the capacitance value is converted into a digital signal by incorporating the unknown capacitor C_x and a reference capacitor C_{ref} in an ADC block, it is referred to as a direct capacitance-to-digital conversion (CDC), most often using the charge-balancing technique.

Delta-sigma-based CDCs and successive-approximation-based CDCs are typical examples of the direct capacitance-to-digital conversion. We take Delta-sigma based

CDC (DS-CDC) as an example. As Fig. 1-5 shows, the unknown capacitor C_x is part of the integrator of the ΔΣ Modulator. By applying the same reference voltage to the unknown capacitor C_x and the reference capacitor C_{ref}, the comparison is done in the charge domain and the exact value of V_{ref} does not affect the comparison result. The output digital bitstream is a representation of the ratio between C_x and C_{ref}.

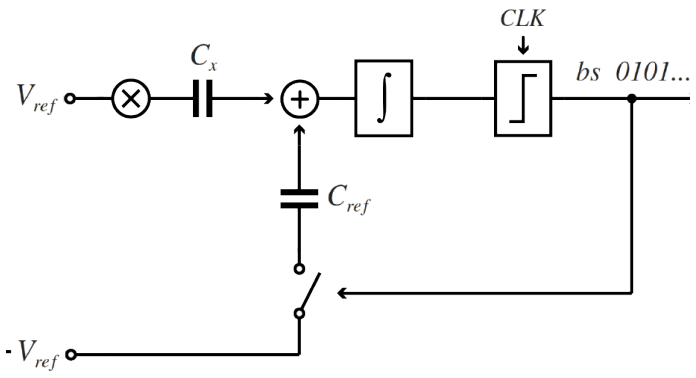


FIG. 1-5. EXAMPLE: DELTA-SIGMA MODULATOR BASED CDC WITH DIRECT COMPARISON WITH REFERENCE CAPACITOR.

During each clock period, the unknown amount of charge from C_x is supplied to the first integrator. A comparator compares the output voltage of the integrator with a reference voltage, resulting in the change of its output level (0 or 1) by additional charge with opposite signs being supplied to the input of the integrator via a controlled switch and a reference capacitor C_{ref}. So the output voltage of the integrator is kept close to the reference voltage.

The charge of the two capacitors is supplied from the same voltage source V_{ref} with opposite signs. So, after considerable number N of clock cycles, the charge supplied by the reference capacitor C_{ref} will balance the charge from the unknown capacitor C_x. A digital bitstream will be generated from the output levels of the comparator. The charge balancing can be expressed as:

$$N \cdot V_{ref} \cdot C_x = N_1 \cdot V_{ref} \cdot C_{ref} \quad (1\text{-}3)$$

where N_1 is the number of code '1' of the output bitstream. From expression 1-3, we obtain:

$$\frac{C_x}{C_{ref}} = \frac{N_1}{N} \tag{1-4}$$

In this way, the unknown capacitor C_x is directly digitized into a digital bitstream and its value can be obtained by knowing the value of the reference capacitor C_{ref}.

1.2.2 Indirect Conversion

Another possibility of conversion is to convert the unknown capacitance value C_x into an electrical signal (e.g. voltage, frequency, time, etc) in a first step, and then to digitize the electrical signal by a conventional analog-to-digital converter (ADC). This kind of conversion is called "indirect". It has two independent functional blocks, which can be optimized according to the practical requirements, resulting in high performance.

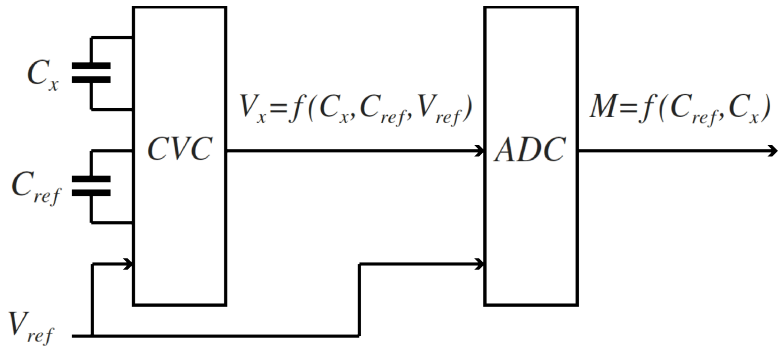


FIG. 1-6. EXAMPLE: CAPACITANCE-TO-VOLTAGE CONVERTER FOLLOWED BY ADC.

Converting capacitance into voltage and frequency are two most commonly used structures. Here, we take "capacitance-to-voltage conversion" as an example. Capacitance-to-voltage converter (CVC) followed by a conventional analog-to-digital converter (ADC) is shown in Fig. 1-6. First, the capacitance value is converted to a

voltage signal by a CVC. Then, the voltage, which is a function of C_x, C_{ref} and V_{ref}, is digitized by an analog-to-digital converter (ADC). The unknown capacitor C_x is represented digitally as a function of the reference capacitor C_{ref}.

CVCs can be divided into two categories based on the operating principle: switched-capacitor (SC) CVCs and continuous-time (CT) CVCs. The complexity and the power dissipation of SC circuits are quite low, but they suffer from *kT/C* noise and noise folding, while the noise performance of the CT circuits is much better.

1.2.3 System-level Techniques

The previous section discussed the most important aspects of capacitance measurement. In this part we focus on analyzing the problems and possible solutions.

1. Stability of Capacitive Sensors

In most of the applications the environmental conditions are not perfectly controlled, which will limit the minimum detectable variation of the measurand. The environmental effects can be minimized either by using a differential structure or by using a reference capacitor with similar behavior as the sensing capacitors, and build a balanced bridge detector.

Fortunately, when measuring very low pressure (in mPa range), the environmental conditions are generally very well-controlled. This relaxes the stability requirements of the sensor.

2. Baseline Compensation and Zoom-in

The presence of an offset capacitance is a common issue for capacitive sensors. The standard way to cancel its effect is by means of capacitance subtraction. By

implementing a compensation (zoom-in) capacitor C_z driven by a voltage with opposite polarity, the baseline capacitance can be cancelled.

Another approach to solve this problem can be found in the use of differential capacitive pressure sensors. In addition to enhancing the resolution, the applied half-bridge structure can reject common mode interfering effects. With differential measurement an accurate capacitance difference/ratio can be obtained enhancing accurate differential pressure measurement.

3. System-level Chopping Technique

Significant part of the sensor signal bandwidth is in the low-frequency range, where many interfering signals such as: offset and flicker noise of the readout circuit, as well as interferences from the supply, are located. Chopping is a technique which can separate the sensor signal in the low-frequency domain from the interfering signals. Firstly, the desired signal is modulated to a higher frequency and then, after certain processing, it is demodulated back to the baseband frequency.

1.2.4 State-of-the-Art Solutions

Table 1-2 shows the performance of state-of-the-art capacitance-to-digital converters, as discussed in the previous section.

TABLE 1-2. SURVEYS OF STATE-OF-THE-ART OVER DIRECT AND INDIRECT CONVERSION.

	Type	Tech. (µm)	Input Range (pF)	Meas. Time (µs)	Resolution (aFrms)	Power (µW)
	Direct Conversion					
[15]	DS	0.35	8.4-11.6	20000	65	14900
[16]	SAR	0.18	12.66	16	1100	7.25
[17]	DS+SAR	0.18	2.5-75.3	4000	6000	0.16

	Type	Tech. (µm)	Input Range (pF)	Meas. Time (µs)	Resolution (aFrms)	Power (µW)
	Indirect Conversion					
[18]	PM	0.16	8	210	1400	14
[19]	ID	0.04	11.3	19	12300	1.84
[20]	CVC+ADC	0.5	10.3	100000	11620	7

1.3 Discussion and Conclusion

In this chapter, an investigation of high-performance capacitive pressure sensor systems has been presented.

To interface a capacitive sensor, many possible circuit architectures have been developed in the past decades. Regarding the conversion approaches, there are two types of interface structures: direct conversion and indirect conversion. In terms of their performance, state-of-the-art designs are investigated. Both delta-sigma based CDCs and CVC followed by ADC architectures can achieve high resolution. However, the CVC followed by ADC configuration can be optimized according to specific requirements, resulting in higher performance under special conditions.

To design an accurate capacitive sensor interface, some techniques at system level have been addressed to solve the existing problems. Differential readout circuit structure is required for rejection of the common-mode interference. To measure a 2-port capacitive sensor, a fully differential readout circuit should be implemented.

The goal of this project is to realize a high-performance interface for measuring low pressure with capacitive pressure sensor. A starting point of the design is an existing high-performance interface for piezo-resistive pressure sensors, in which techniques like zoom-in and chopping can be simply implemented [19]. The intension is, with minimum modifications, to apply the same design technique for interfacing capacitive pressure sensors achieving similar high performance. In this way, a more generic

interface will be created, which can equally well be used for interfacing both capacitive and piezo-resistive pressure sensors.

1.4 Aim and Scope

The goal of this project is to develop a capacitive pressure sensor readout interface based on an existing design of piezo-resistive pressure sensor interface. The design is intended for low pressure measurements, which requires resolution in aF level. Table 1-3 lists the targeted interface performance parameters.

TABLE 1-3. THE TARGET SPECIFICATIONS IN THIS PROJECT.

Parameter	Value
Technology	0.18 μm CMOS
Supply voltage	1.8 V
Input range	0-10 pF
Resolution	20 bits (8 aF_{rms})
Conversion time	0.5ms
Thermal Drift	30 ppm/°C
Power Consumption	2.16 mW

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Chapter 2

Circuit-level Design and Simulation Results

In this chapter, first the existing design is briefly introduced. Then, the block diagram of the proposed interface is given and the detailed core circuit design, which combines three operating modes and transfer function, is discussed. Next, the noise performance is analyzed. Finally, the layout of the design and the simulation results evaluating the circuit are shown.

2.1 Existing Design

The low-noise energy-efficient interface based on piezo-resistive technology reported in [1] archives high performance with 3.7nV/√Hz input-referred noise with bandwidth 2 kHz. This design is applied for Wheatstone bridge sensors. The operating principle of this design will be introduced.

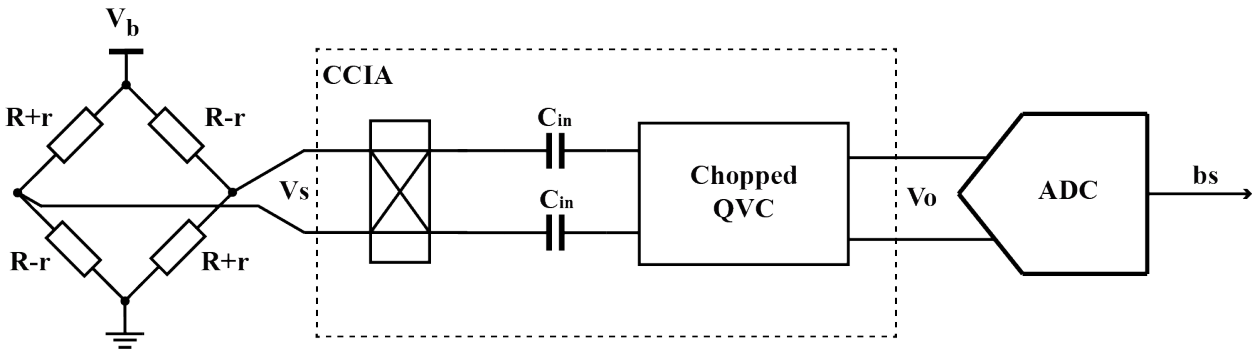


FIG. 2-1. BLOCK DIAGRAM OF THE EXISTING DESIGN.

A functional block diagram is shown in Fig. 2-1. The output of the Wheatstone bridge is small differential voltage superimposed on a large common-mode (CM) voltage. A capacitively coupled instrumentation amplifier (CCIA) followed by a continuous-time ΔΣ Modulator is implemented to transfer the differential signals into digital bitstream. The voltage V_s is first chopped into AC signals and then converted into charge by capacitors C_{in}.

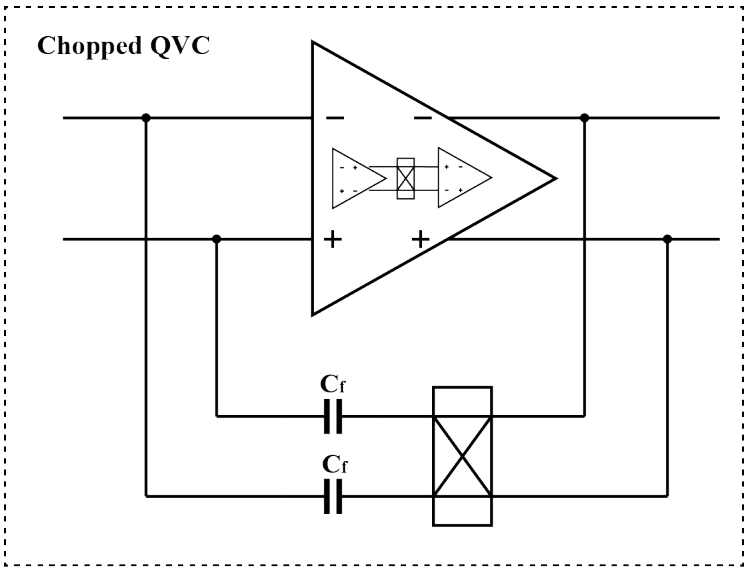
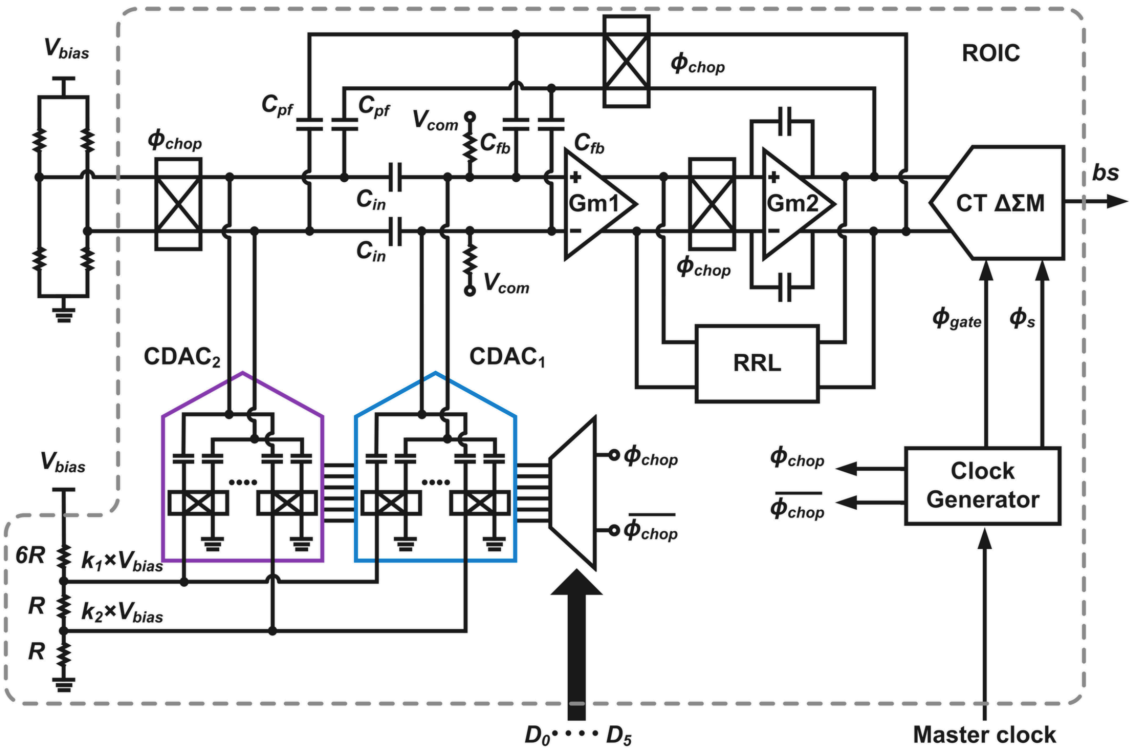


FIG. 2-2. SIMPLIFIED CIRCUIT DIAGRAM OF CHOPPED CHARGE-TO-VOLTAGE CONVERTER



(QVC).

FIG. 2-3. SIMPLIFIED CIRCUIT DIAGRAM OF THE EXISTING DESIGN [1].

A simplified chopped charge-to-voltage convertor (QVC) is shown in Fig. 2-2. The output voltage of CCIA V_o is proportional to $\frac{C_f}{C_{in}}$.

The core blocks and simplified circuit diagram are shown in Fig. 2-3. Ripple-reduction-loop (RRL) is used to suppressed the up-modulated offset. Considering the output signal of the bridge is much smaller than the offset of the bridge, an offset-compensation scheme (resistive voltage divider and $CDAC_1$) is used to reduce the offset before it is amplified.

Based on this structure, we need to explore whether it can also be used for capacitive sensor interface and capacitive bridge sensor interface. In the next section, a functional block diagram is shown, followed by an introduction of a simplified circuit.

2.2 Functional Block Diagram

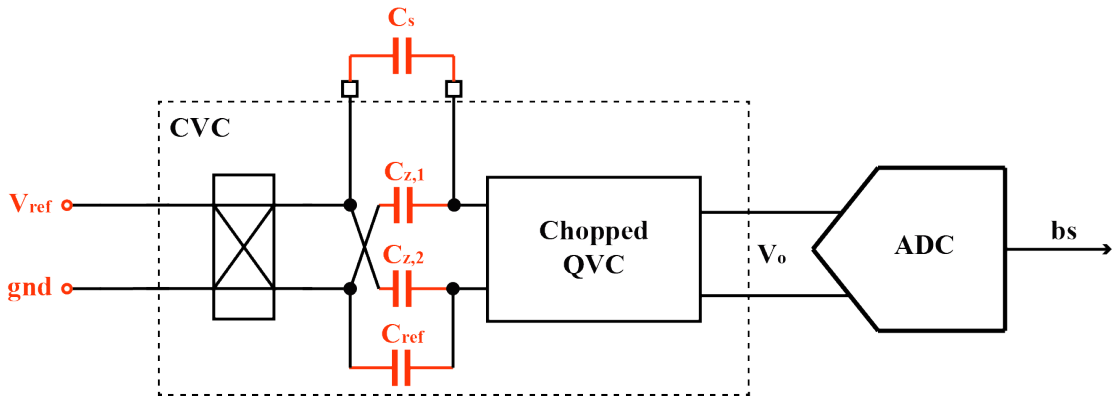


FIG. 2-4. BLOCK DIAGRAM OF PROPOSED DESIGN.

Fig. 2-4 illustrates the functional block diagram of the capacitive-pressure-sensor interface.

After switching voltage levels between V_{ref} and ground (*gnd*), the unknown capacitor C_s and the zoom-in capacitor $C_{z,1}$ are charged with opposite sign, and the charge difference is stored on the feedback capacitor C_f of the chopped QVC (shown in Fig.

2-2) and a DC output voltage is produced. Next, a ΔΣ Modulator is used to digitize the output voltage of the QVC into a digital bitstream. Different operating modes are realized by replacing the reference capacitors with capacitive sensors, so that different sensor configurations can be interfaced with this topology. The operating modes and transfer function will be introduced in the next section.

2.3 Circuit-level Design

The circuit-level diagram is shown in Fig. 2-5.

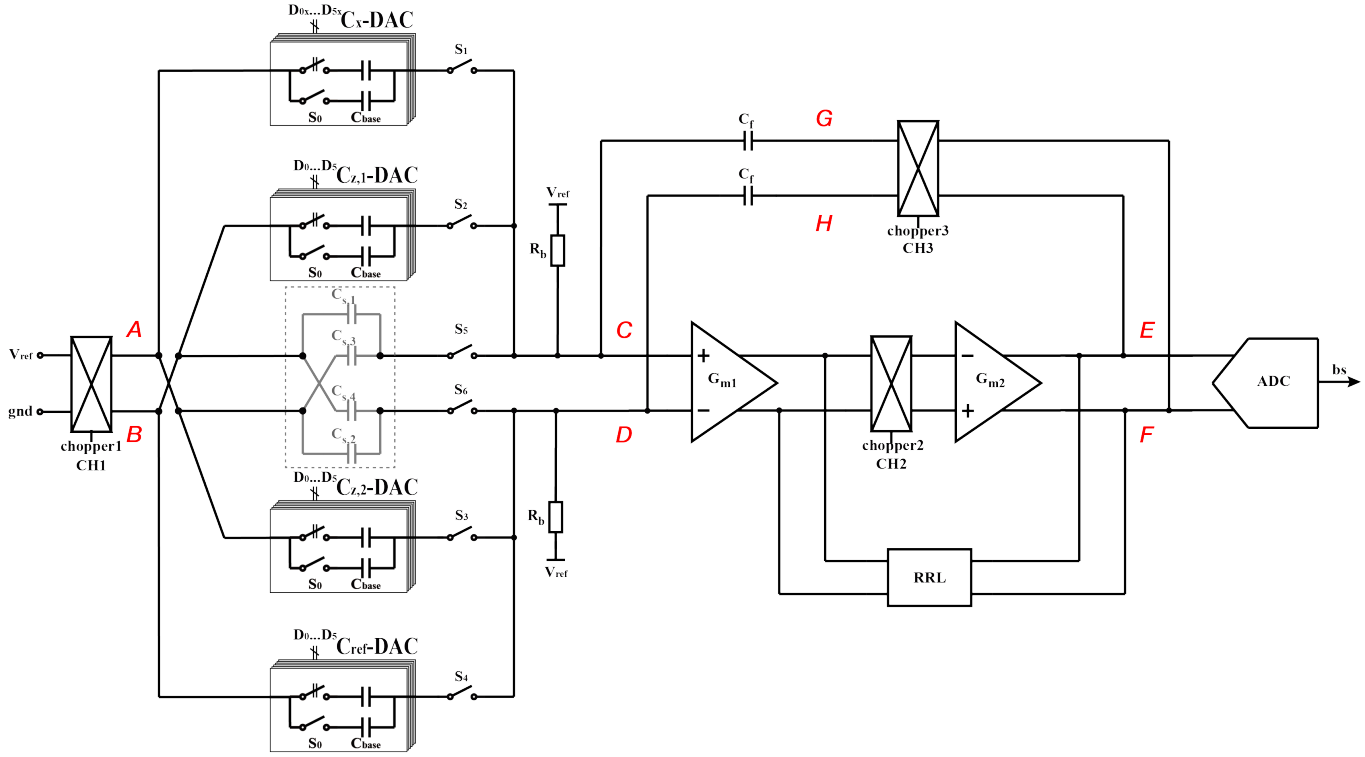


FIG. 2-5. SIMPLIFIED CIRCUIT DIAGRAM.

The on-chip testing capacitor C_x and the other three reference capacitors for zooming-in are implemented as four C-DACs. The C-DACs will be introduced later in this section. Five switches S_2, S_3, S_5, S_6 and S_0 are controlled by enable signals and are used for switching among 3 different operating modes, which can satisfy different sensors measuring requirements.

After the reference voltage V_{ref} is chopped by the input chopper CH1, two C-DACs will be charged with opposite signs at each input of the QVC. The charge will be subtracted at points *C* and *D* and the charge difference will be transferred to the feedback capacitors C_f. Due to the synchronized chopping function between choppers CH1, 2 and 3, the QVC will deliver a demodulated voltage at the input of the ADC, which is proportional to the difference between the unknown capacitor C_x and the zoom-in capacitor C_z. The ADC will digitize this voltage in the form of a digital bitstream.

2.3.1 Capacitive Digital-to-analog Convertor (C-DAC)

To realize an on-chip testing mode, two capacitors are needed for each input of the system. The C_x-DAC is programmable by a 6-bit digital code D_{0x}-D_{5x}, while the other three capacitors $C_{z,1}$, $C_{z,2}$ and C_{ref} by another 6-bit code D_0-D_5. Also, there is a switch S_0 controlled by the same signal in each DAC to decide whether a baseline capacitor with the value of 5.12 pF is connected or not.

Considering maximum variation of the capacitance of the capacitive pressure sensor of ±80 fF, the LSB of the C-DAC is set to 80 fF. So the full range of the C-DACs is 10.16 pF. In this way, we can realize the three operating modes for basic measurement requirements with simple implementation. The operating modes will be introduced in the following section.

2.3.2 Operating Modes

Three different operating modes can be realized with the help of enabling signals, as mentioned above. The different codes for these three modes and the corresponding functions are listed in the Table 2-1 below. The diagrams are shown in Fig. 2-6, 7, 8. The enable signals for Mode 2 and Mode 3 use the same code. The difference is that the baseline capacitor is disconnected in Mode 3. One C-DAC remaining at each input in Mode 3 gives the possibility for offset cancellation.

TABLE 2-1. MODE SIGNALS FOR THREE MEASUREMENT MODES.

	Enable Signal	Functions
Mode 1	’1’	Testing: All on-chip capacitors
Mode 2	’0’	Two off-chip capacitive sensors with two on-chip zoom-in C-DACs
Mode 3	’0’	Capacitance Bridge: All off-chip capacitive sensors

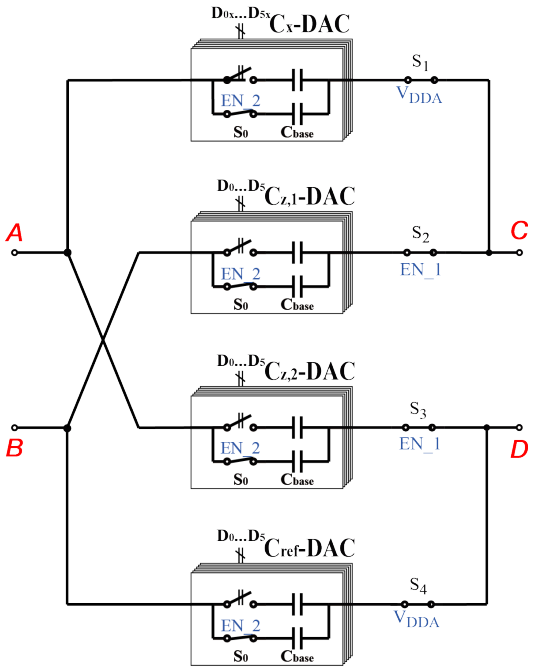


FIG. 2-6. OPERATING MODE 1: TESTING MODE.

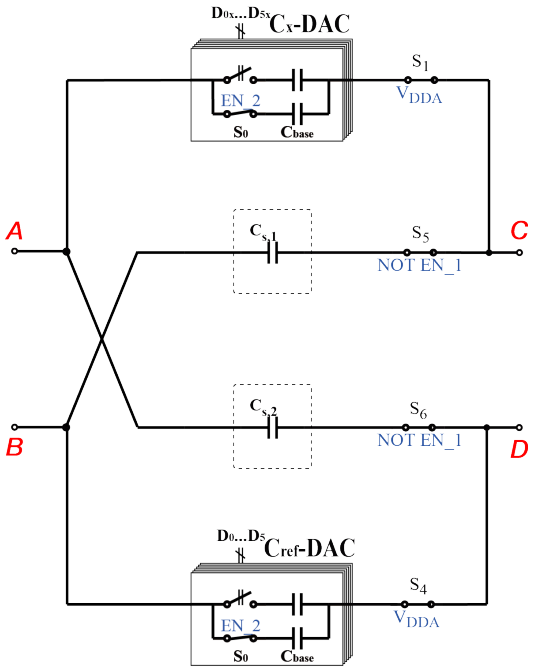


FIG. 2-7. OPERATING MODE 2: TWO OFF-CHIP CAPACITIVE SENSORS.

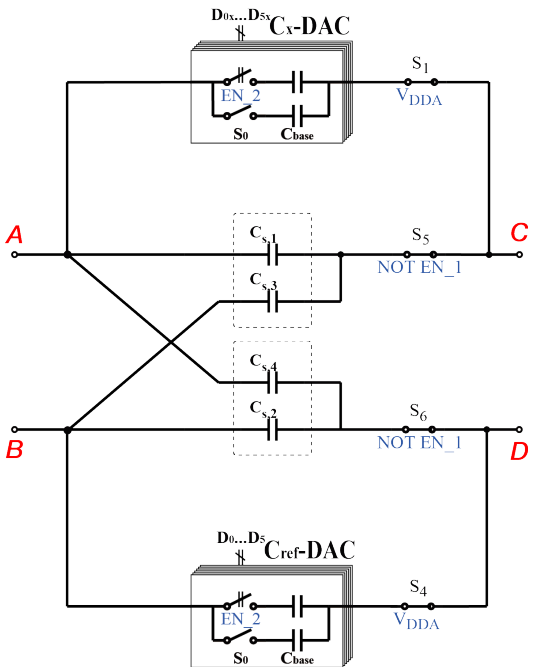


FIG. 2-8. OPERATING MODE 3: ALL OFF-CHIP CAPACITIVE SENSORS.

2.3.3 Transfer Function

1. Output voltage V_o of the CVC

If we keep (C_x-$C_{z,1}$) equal to 1 LSB of the C-DAC and $C_{z,1} = C_{z,2} = C_{ref}$ (Mode 1), the effective input capacitance at the non-inverting input of the gm stage (see Fig. 2-5) will be 80 fF, while the effective input capacitance at the inverting input will be zero. In this case the voltage at point *G* (in the feedback network, before the chopper CH3) is derived as follow:

$$V_G = \frac{V_{ref} \cdot \left(C_x - C_{z,1}\right)}{C_f} \tag{2-1}$$

The voltage V_G is chopped by chopper CH3, which reduces twice its amplitude at the output of the CVC. So, the output swing is:

$$\left(V_F - V_E\right)_{Mode1} = \frac{1}{2} \cdot \frac{V_{ref}\left(C_x - C_{z,1}\right)}{C_f} \tag{2-2}$$

Let's now consider Modes 2 and 3. In Mode 2, we set the two capacitive sensor values as $C_{s,1}$ and $C_{s,2}$. The values of the two on-chip capacitors are C_x and C_{ref}. In Mode 3, we set the capacitive sensor values as $C_{s,1}$, $C_{s,2}$, $C_{s,3}$ and $C_{s,4}$. The output voltage of the QVC between points *E* and *F* in this two modes will be:

$$\left(V_F - V_E\right)_{Mode2} = \frac{1}{2} \cdot V_{ref} \cdot \frac{(C_x - C_{s,1}) - (C_{ref} - C_{s,2})}{C_f} \tag{2-3}$$

$$\left(V_F - V_E\right)_{Mode3} = \frac{1}{2} \cdot V_{ref} \cdot \frac{(C_{s,3} - C_{s,1}) - (C_{s,4} - C_{s,2})}{C_f} \tag{2-4}$$

2. Transfer Function

Based on the analysis and calculations above, the ΔΣ Modulator will produce a bitstream based on the DC voltage V_o from the output of the CVC.

$$\frac{N_1}{N} = \frac{V_o}{V_{ADC}} \tag{2-5}$$

$$\frac{N_1}{N}_{Mode1} = \frac{1}{2} \cdot \frac{V_{ref}}{V_{ADC}} \cdot \frac{C_x - C_{z,1}}{C_f} = \frac{1}{2} \cdot \frac{C_x - C_{z,1}}{C_f} \tag{2-6}$$

$$\frac{N_1}{N}_{Mode2} = \frac{1}{2} \cdot \frac{(C_x - C_{s,1}) - (C_{ref} - C_{s,2})}{C_f} \tag{2-7}$$

$$\frac{N_1}{N}_{Mode3} = \frac{1}{2} \cdot \frac{(C_{s,3} - C_{s,1}) - (C_{s,4} - C_{s,2})}{C_f} \tag{2-8}$$

Where N_1 is the number of '1' in the output bitstream, while N is the total number in the output bitstream or the clock cycles. V_{ADC} is the reference voltage used by the ADC and V_{ref} is the reference voltage used to re-charge the capacitors. If $V_{ref} = V_{ADC}$, in operating mode 1, the number of '1' in the output bitstream will be equal to $\frac{N}{2} \cdot \frac{C_x - C_{z,1}}{C_f}$.

2.3.4 Noise Analysis

According to the simplified circuit diagram Fig. 2-5, there are two main noise source: noise of Gm1 and Rb, which need to be taken into consideration, firstly. The input referred noise V_{n1} of G_{m1} noise $V_{n,gm}$ can be calculated as follows:

$$V_{n1} = \frac{C_x + C_z + C_f}{C_x} \cdot V_{n,gm} \tag{2-9}$$

Apart from G_{m1}, each biasing resistor R_b also generates thermal noise $V_{n,Rb}$, whose value can be expressed as:

$$V_{n,R_b} = \sqrt{\frac{4kT}{R_b}} \tag{2-10}$$

Considering the power efficiency, the noise source $V_{n,Rb}$ should be much smaller than the noise contribution by G_{m1}. Thus, the resistance of biasing resistors R_b is normally very high (tens of Mega ohm). The biasing resistor can be implemented in several ways, like on-chip resistor, MOS transistors biasing in the sub-threshold region and switched-capacitor biasing circuit. On-chip resistor is the simplest approach with no residual error, high linearity and acceptable accuracy. However, to ensure that the noise of G_{m1} is dominated source, the noise generated by the biasing resistors R_b should be optimized by increasing the resistor value, which means large chip area would be taken up with on-chip resistors. From the area perspective, MOS in sub-threshold and swished-cap approach hold the major benefit. However, the linearity and accuracy of MOS in sub-threshold approach are lower, while the ripple-offset exists in switched-cap way. In the previous design, the resistors are implemented in switched-cap approach with 90-degree phase shifted between the switching frequency f_s and chopping frequency f_{chop} to avoid offset from the common-mode biasing block.

Based on the discussion above, the dominant noise source is the noise of G_{m1}, $V_{n,gm}$, while the noise of common-mode biasing block can be ignored. Also, the noise of A-D converter $V_{n,ADC}$ is shown in the simplified noise model Fig. 2-9. The input-referred noise $V_{n,eq}$ related to $V_{n.gm}$ and $V_{n,ADC}$ is:

$$V_{n,eq} = \sqrt{\left(\frac{C_x + C_z + C_f}{C_x} \cdot V_{n,gm}\right)^2 + \left(\frac{C_f}{C_x} \cdot V_{n,ADC}\right)^2} \tag{2-11}$$

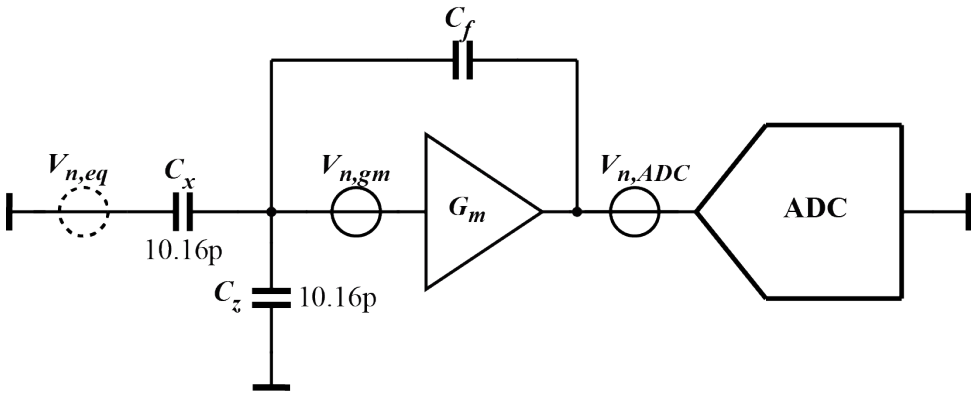


FIG. 2-9. SIMPLIFIED NOISE MODEL.

From measurement results of previous design, $V_{n,gm}$ = 2.94 nV/√Hz and $V_{n,ADC}$ = 180 nV/√Hz with bandwidth 2 kHz. The full-scale range of C_x-DAC and C_z-DAC is 10.16 pF.

Having in mind that the targeted resolution C_{rms} for this design is 8 aF_{rms}, the maximum input-referred noise can be calculated as 25.29 nV/√Hz with bandwidth 2 kHz and V_{ref} = 1.8 V, according to the equation 2-12.

$$V_{n,eq} \cdot \sqrt{ENBW} \cdot C_x \leq V_{ref} \cdot C_{rms} \tag{2-12}$$

The interferences from the reference voltage V_{ref} can also have the impact on the noise performance. However, as shown in equation 2-6, the influence can be cancelled by offering the same supply signal for V_{ADC} and $V_{ref.}$

As can be seen from expression 2-9, the feedback capacitor C_f has an impact on the input-referred noise. This capacitor is also part of the transfer function of the CVC. To settle the value of C_f, we need to consider these two factors.

2.3.5 Selection of the Feedback Capacitor C_f

The input range of the ΔΣ Modulator is 1.2 V. This means that the output differential voltage of the CVC should not be exceed 1.2 V. The aim of the design is for ±80 fF maximum input cap difference. However, from safety perspective and creating margin for other applications, the max input cap difference range is set to ±3LSB of the DAC. According to equation 2-2, the feedback capacitor should be 0.75 times greater than the input cap difference (C_x - C_z), which is 180 fF. Also, the full-scale input of ADC is supposed to respond to the full-scale range of input capacitance difference: ±3LSB. So the value of C_f is set as 200 fF.

Based on the equation 2-2 with the selected value of the feedback cap C_f, the output of the CVC in Mode 1 with different input is summarized in Table 2-2.

TABLE 2-2. OUTPUT SWING OF CVC - MODE 1.

Input cap difference (fF)	V_E	V_F	Output of CVC $V_o = V_E - V_F$
80	1.08V	0.72V	0.36V
160	1.26V	0.54V	0.72V
240	1.44V	0.36V	1.08V

Take the Mode 1 as example, with 80fF input cap difference, the sensitivity can be obtained from equation 2-6:

$$Decimation = \frac{N_1}{N_{Mode1}} = \frac{1}{2} \cdot \frac{C_x - C_{z,1}}{C_f} = 0.2$$

$$Sensitivity = \frac{Decimation}{C_x - C_{z,1}}_{Mode1} = 2.5/pF$$

2.3 Layout

The layout of the design is shown in Fig. 2-10. The whole chip including the bond-pad and the seal-ring occupies an area of 1.45×1.45 mm^2.

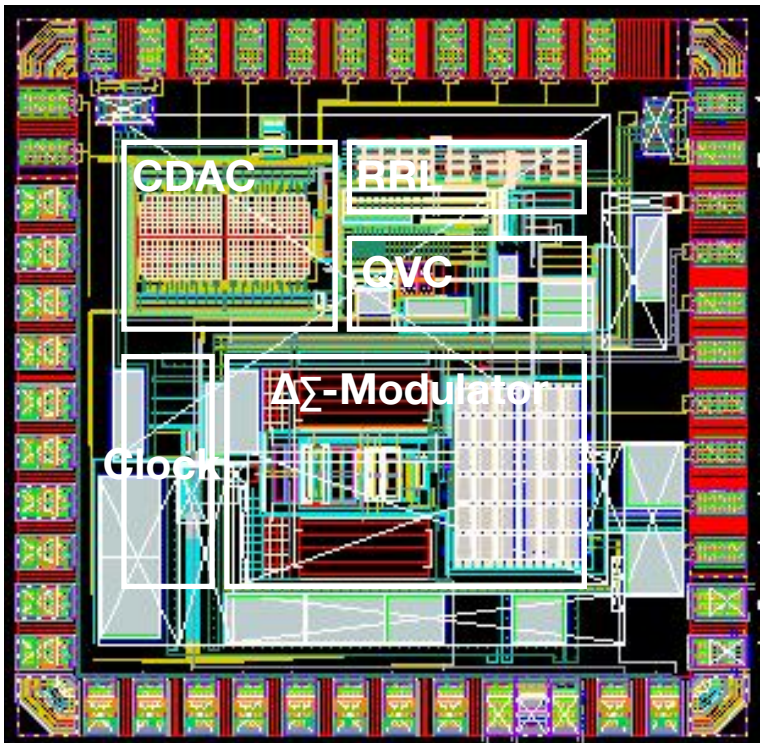


FIG. 2-10. LAYOUT.

The chip has been taped out in TSMC 180nm technology and the measurement results will be shown in the next chapter.

2.4 Circuit-level Simulation Results

In this section, the simulation results are given.

As the work is mainly focused on modifying the CCIA in previous design into a CVC, the CVC is simulated firstly with transfer characteristic (Fig. 2-11). V_o represents the output voltage of the CVC. The result follows the transfer function (Eq. 2-2 & Table 2-2), which proves the function of CVC stage.

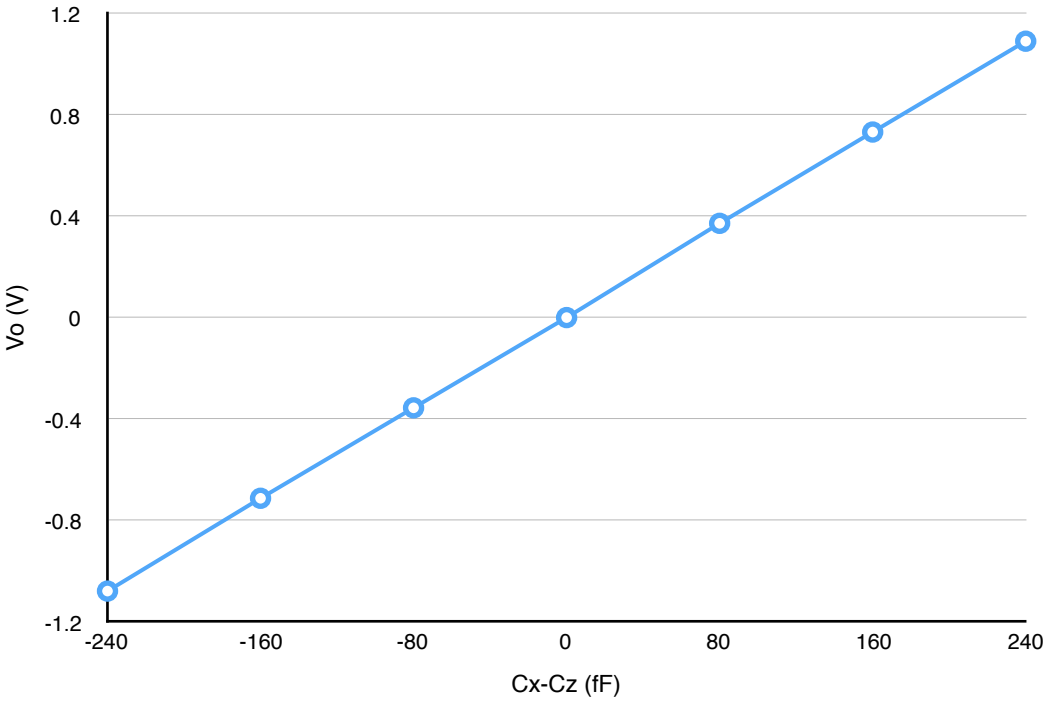


FIG. 2-11. TRANSFER CHARACTERISTIC.

Then, considering the targeted resolution in aF_{rms} is $8aF_{rms}$, the pnoise simulation is done with output noise density shown in Fig. 2-12. The input referred noise can be calculated as 6.056 nV/√Hz with bandwidth 2 kHz. According to the equation below, the resolution in aF_{rms} can be obtained.

$$V_{n,eq} \cdot C_x = V_{ref} \cdot C_{rms} \tag{2-13}$$

$$C_{rms} = 1.92aF_{rms}$$

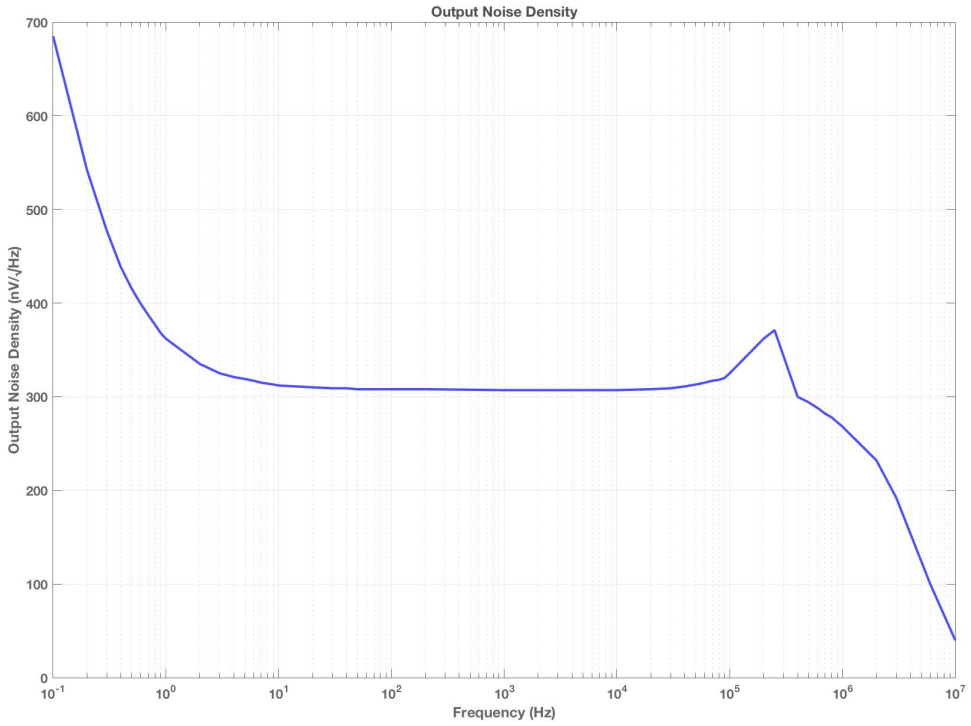


FIG. 2-12. PNOISE SIMULATION RESULTS.

Reference

[1] Jiang, Hui, Kofi AA Makinwa, and Stoyan Nihtianov. "9.8 An energy-efficient 3.7 nV/√Hz bridge-readout IC with a stable bridge offset compensation scheme." *Solid-State Circuits Conference (ISSCC), 2017 IEEE International*. IEEE, 2017.

Chapter 3

Measurement Results

In this chapter, the measurement results of the designed CVC plus the ΔΣ Modulator are presented. First, the fabricated chip and the measurement setup, including the circuit layout, test board design and measurement equipment, are introduced. Next, the performance regarding the sensitivity, resolution, temperature stability and power consumption is presented. Finally, conclusions of this chapter are given.

3.1 Fabricated Chip

The chip is realized in TSMC 180nm technology. It occupies an active area of 0.5mm^2 and is packaged in a QFN48 package. The micrograph is shown in Fig. 3-1.

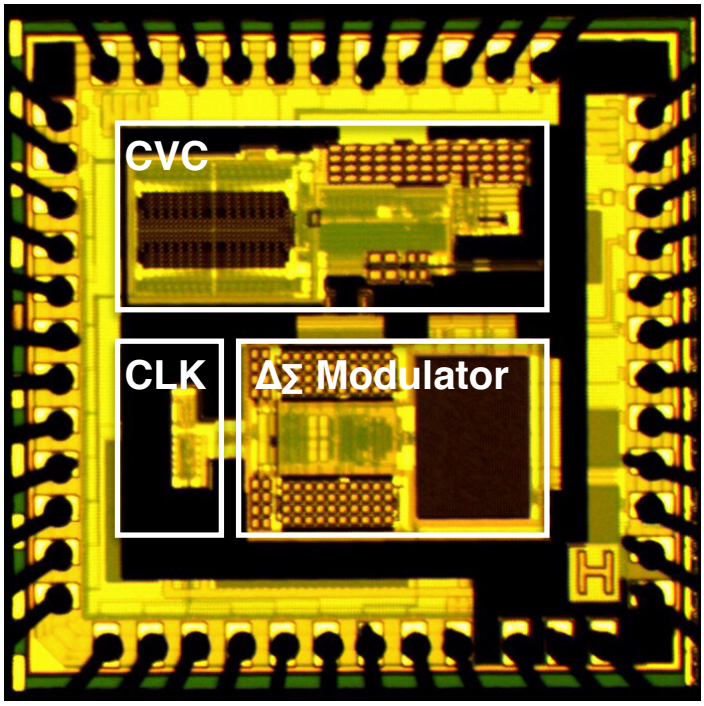


FIG. 3-1. CHIP MICROGRAPH.

3.2 Measurement Setup

The block diagram for the whole measurement setup is shown in Fig. 3-2. The photo of the measurement setup is attached in the Appendix A.

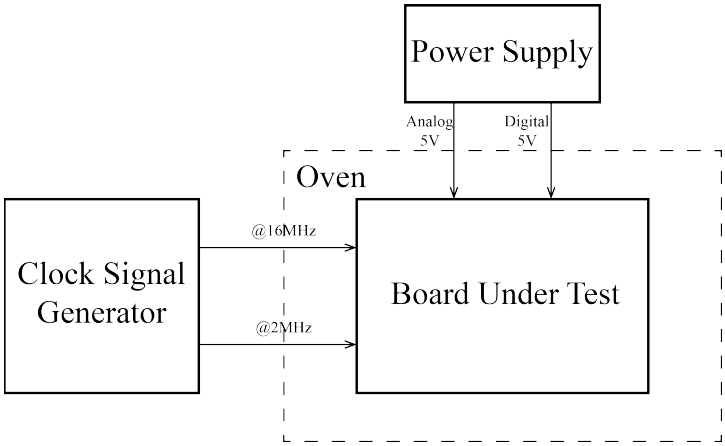


FIG. 3-2. MEASUREMENT SETUP BLOCK DIAGRAM.

1. Printed Circuit Board (PCB)

In order to perform the measurements, a PCB is designed and fabricated as a test board for the measurement. The complete schematics and the photo of the board are demonstrated in Appendix A.

2. Power Supply

The power supply provides positive supply +5V (Analog), +5V (Digital) and ground for the test board.

3. Oven and Digital Multi-meter

The oven is used for temperature stability measurement. The temperature is monitored and controlled by a computer, while the temperature of the chip is measured by a resistive temperature sensor PT100 and processed by a digital multi-meter. In this measurement, the temperature range is 20°C-70°C with tolerance 0.5°C, 5°C per step.

3.3 Experimental Results

In this chapter, the performances regarding: sensitivity, resolution, temperature stability and power consumption are listed.

All presented measurement results are obtained with Mode 1 and Mode 2. The system is designed for measuring the capacitance of capacitive sensor whose variation is within ±80 fF. This target is set with the survey based on *Kavlico P994*, as we mentioned in Chapter 1. The sensitivity and resolution are obtained with ±80 fF input cap difference. However, to create more margin for other applications, the input range is extended to ±240 fF, as will be seen below.

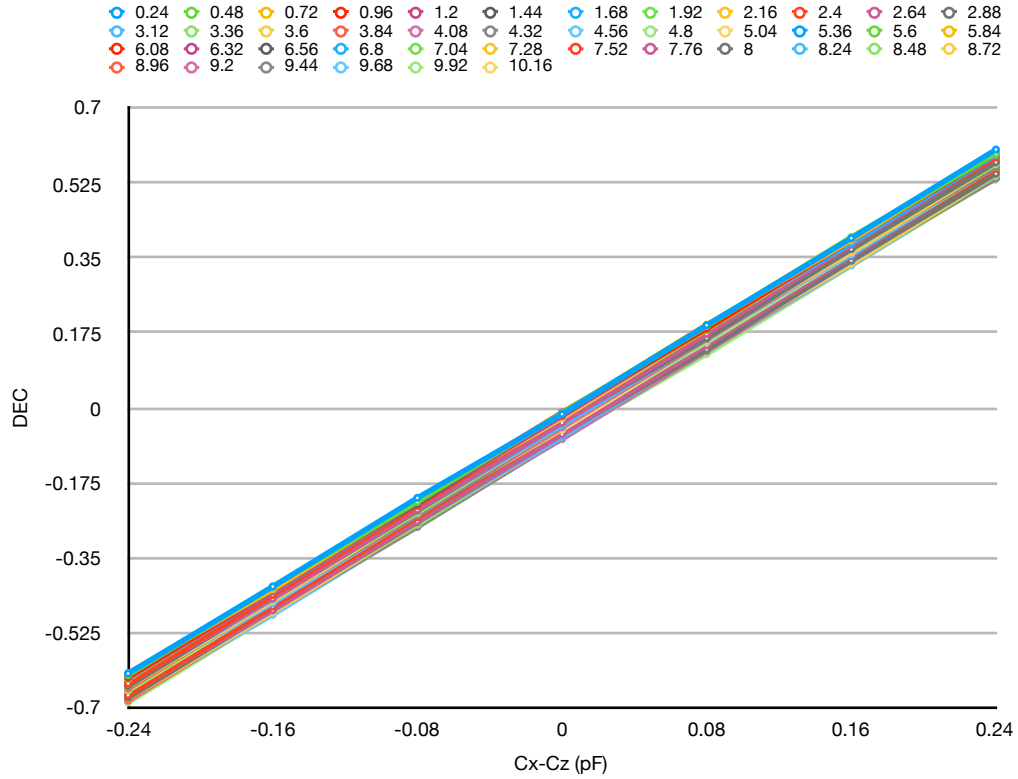
3.3.1 Sensitivity

The sensitivity of capacitive sensor interfaces presents the relation between the output value of the system and the input capacitance difference: (C_x - C_z).

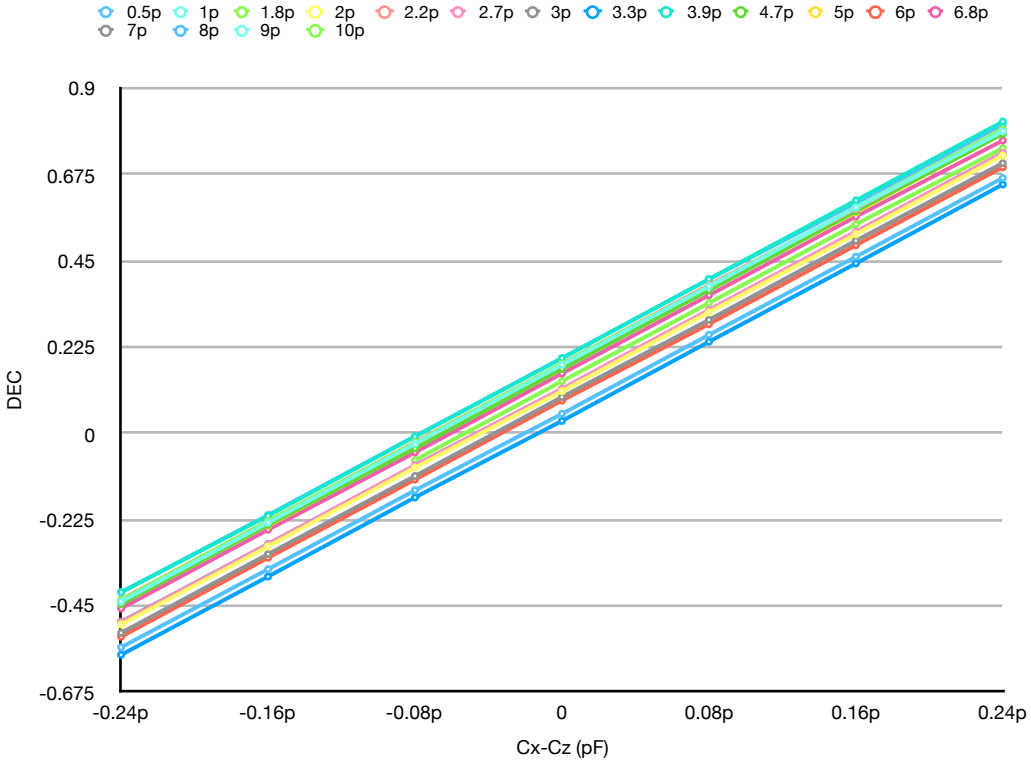
The transfer characteristic (Decimation vs input capacitance difference (C_x-C_z)) is shown in Fig. 3-3, firstly.

The results with operating Mode 1 are shown in Fig. 3-4, and the results with Mode 2 are shown in Fig. 3-5. With input cap difference (C_x - C_z) = ±80 fF, the averaged sensitivity is 2.546 /pF for Mode 1, while it is 2.551 /pF for Mode 2.

At the mean time, sensitivity versus C_x is also demonstrated. When keep the input cap difference (C_x - C_z) as a fixed value, like +80 fF, the sensitivity is supposed to be stable as C_x varies from 0 to 10.16 pF in the ideal case. However, because the capacitance on chip might have some uncertainty, which can cause the value slightly differ from the expectation. The the sensitivity is shown a periodical variation. For the Mode 2, the external cap is subtracted by the on chip zoom-in cap firstly. So the result of sensitivity versus external cap C_x can also show the trend as Mode 1.

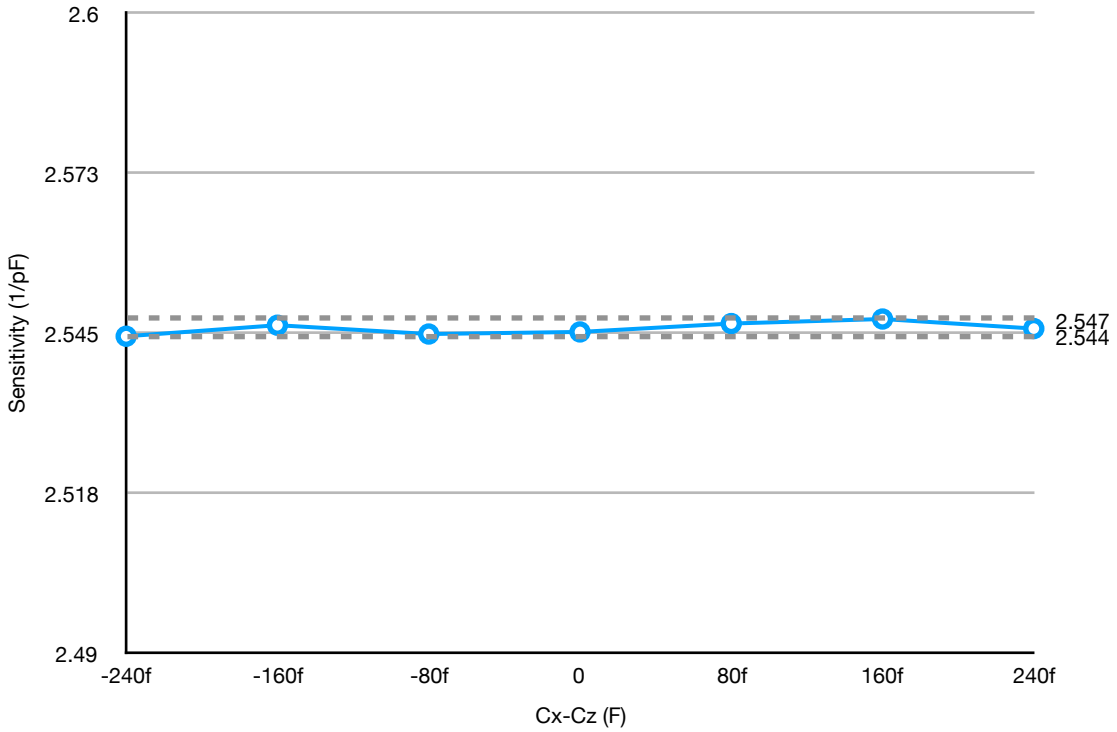


(A)

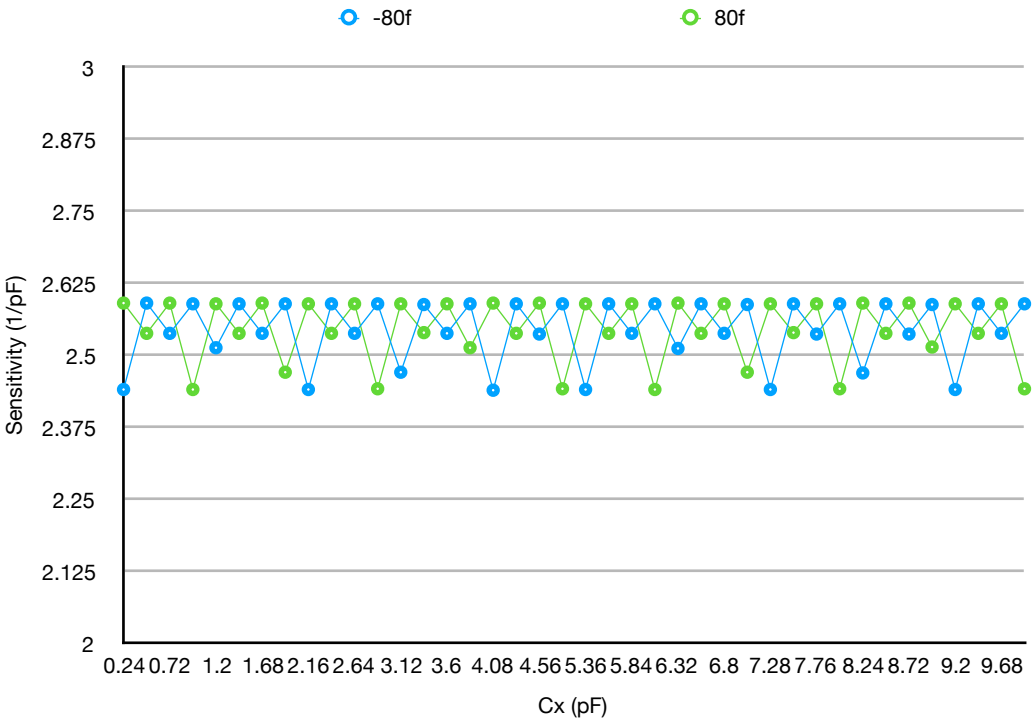


(B)

FIG. 3-3. TRANSFER CHARACTERISTIC.
(A) MODE 1, (B) MODE 2.

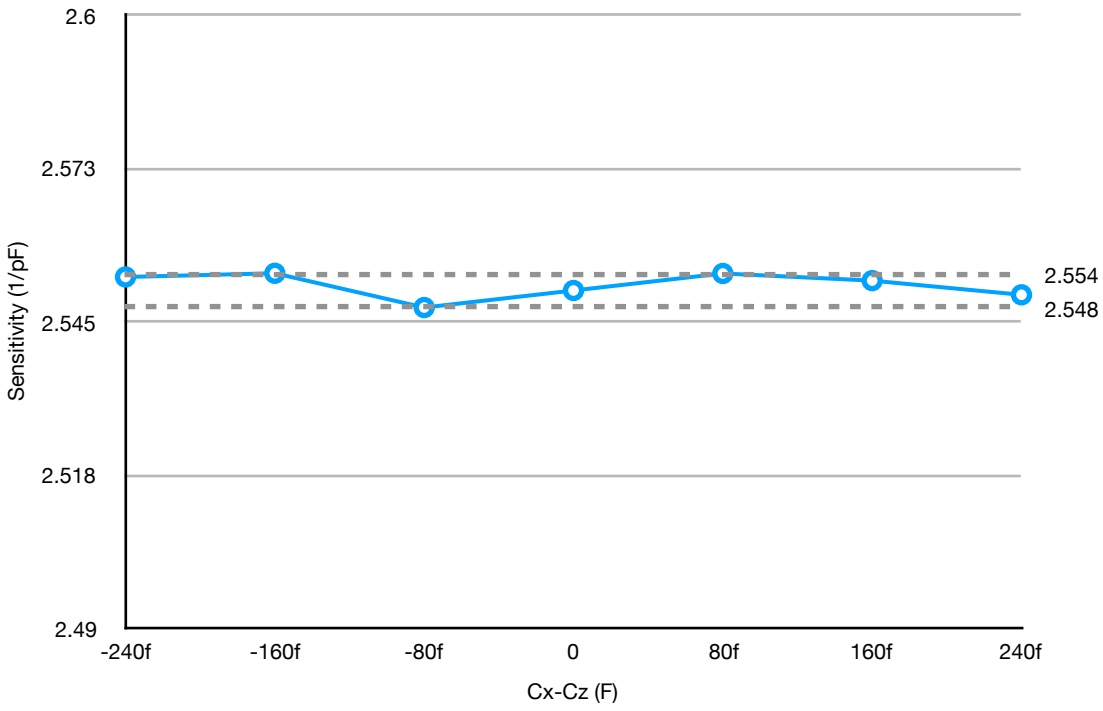


(A)

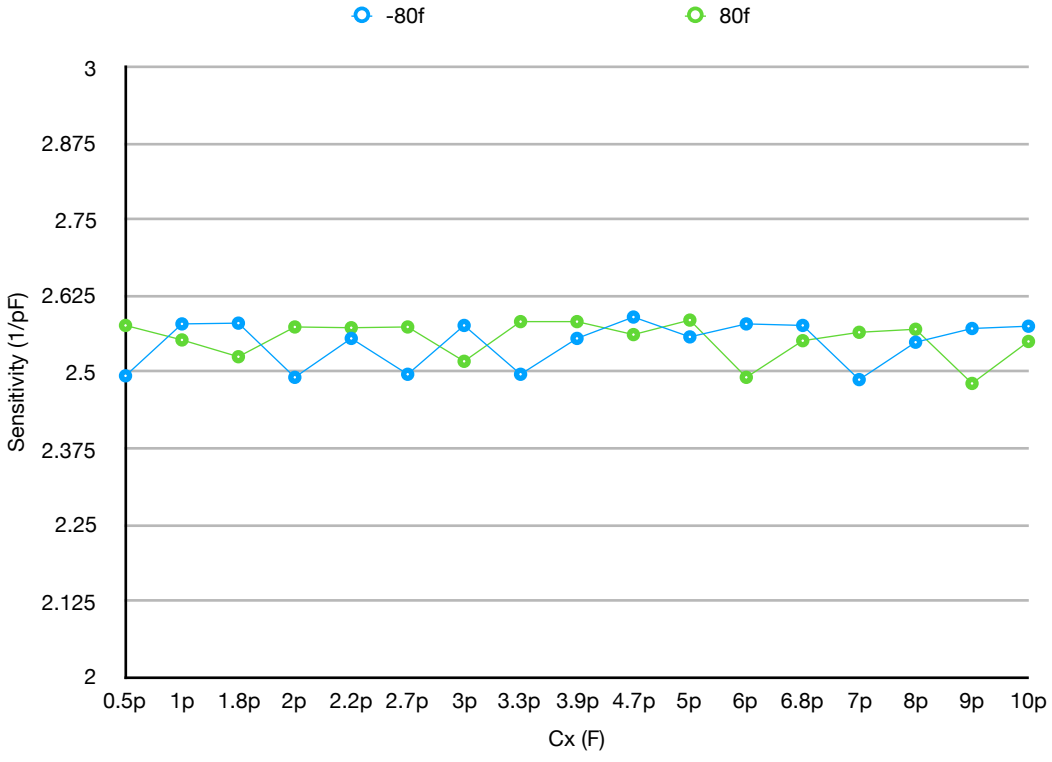


(B)

FIG. 3-4. SENSITIVITY - MODE 1.
(A) SENSITIVITY VS *(C_X-C_Z)*, (B) SENSITIVITY VS *C_X*.



(A)



(B)

FIG. 3-5. SENSITIVITY - MODE 2.
(A) SENSITIVITY VS *(C_X-C_Z)*, (B) SENSITIVITY VS *C_X*.

3.3.2 Resolution

After the sensitivity is obtained, the resolution can be calculated and the results are shown in Fig. 3-6 (Mode 1) and Fig. 3-7 (Mode 2).

With the design target, $|C_x - C_z| \leq 80$ fF, the averaged value of resolution (in aF_{rms}) is 5.1 aF_{rms} with 4.8-5.5 aF_{rms} variation for $C_x > C_z$, while 5.2 aF_{rms} with 4.9-5.7 aF_{rms} variation for $C_x < C_z$. Both of these two conditions meet the target resolution 8 aF_{rms}.

From safety and application perspective, other measurement results ($|C_x - C_z| \leq 160$ fF, 240fF) are also shown in the figure. For the input with ±160fF and ±240 fF, the resolution is 6.3 aF_{rms} and 7.5 aF_{rms}, respectively. So, the acceptable input range is within ±240 fF, while the designed range is ±80 fF.

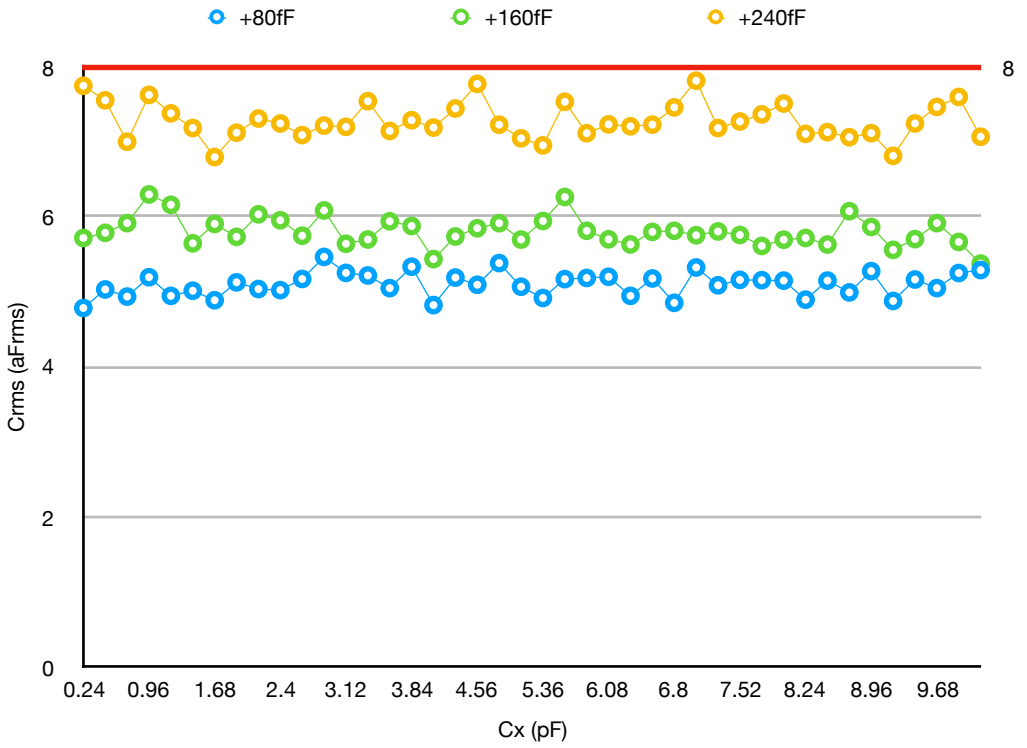
It is interesting to find that the average value of the resolution is decreasing as the input cap difference increases from ±80 fF to ±240 fF. Considering the sensitivity cannot result in a change in 1.5 aF_{rms} level of resolution, the noise of the system might increase as the input cap difference increases.

3.3.3 Temperature Stability

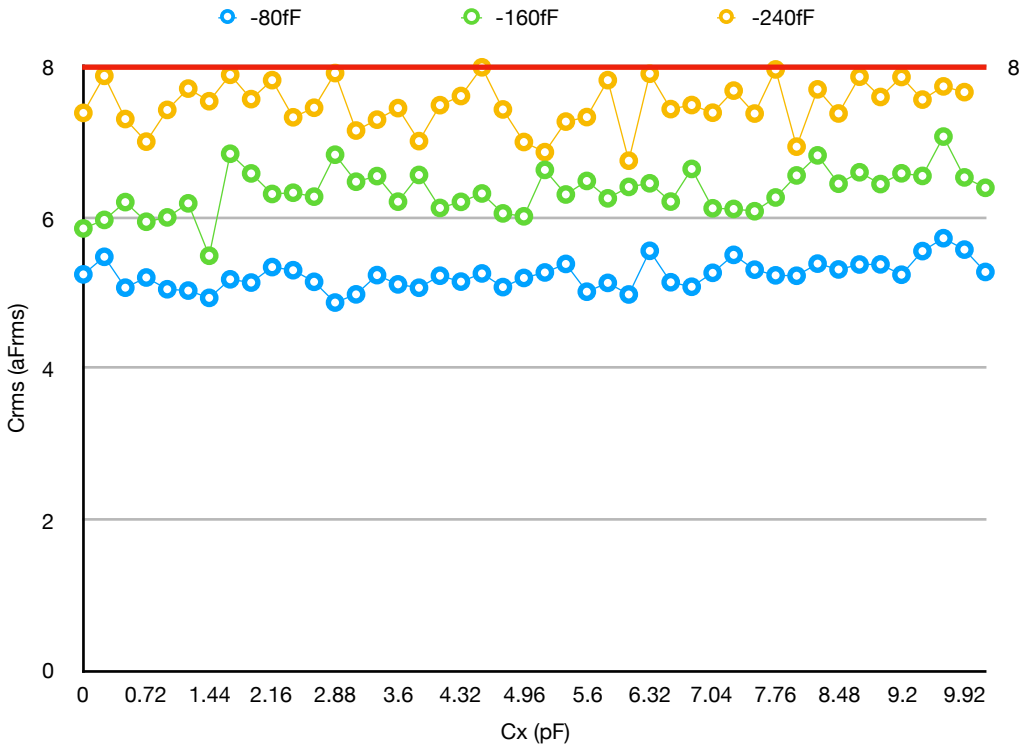
This part is focused on the temperature stability. The temperature measurement is done with Mode 1. The temperature range is 20 °C - 70 °C with steps of 5 °C.

For the worst case, the thermal drift is 17.54 ppm/°C.

The average results (based on 2 times measurements with 3 points for the same temperature each time, all the results are shown in Appendix B) shown in the Fig. 3-8 illustrates that there is a 2nd order effect. The capacitance used on chip is MIM cap, which has a thermal drift 30 ppm/°C. However, according to the transfer function, the drift is supposed to be cancelled. So the results mainly show the drift of the readout circuit and the PCB testing board.

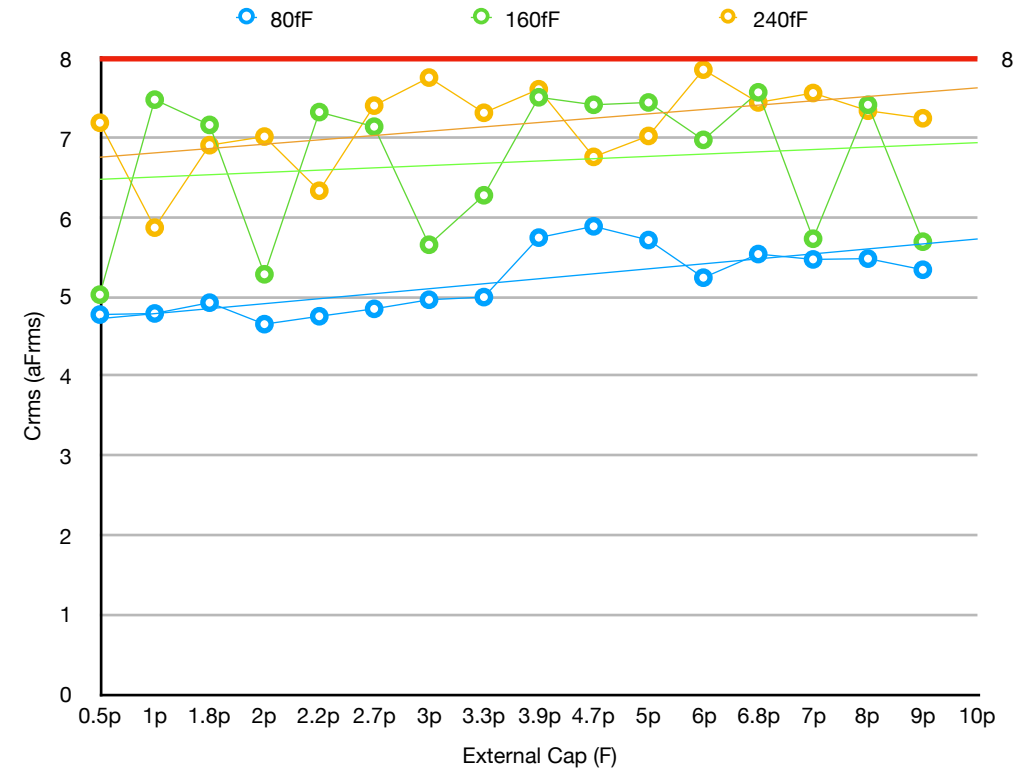


(A)

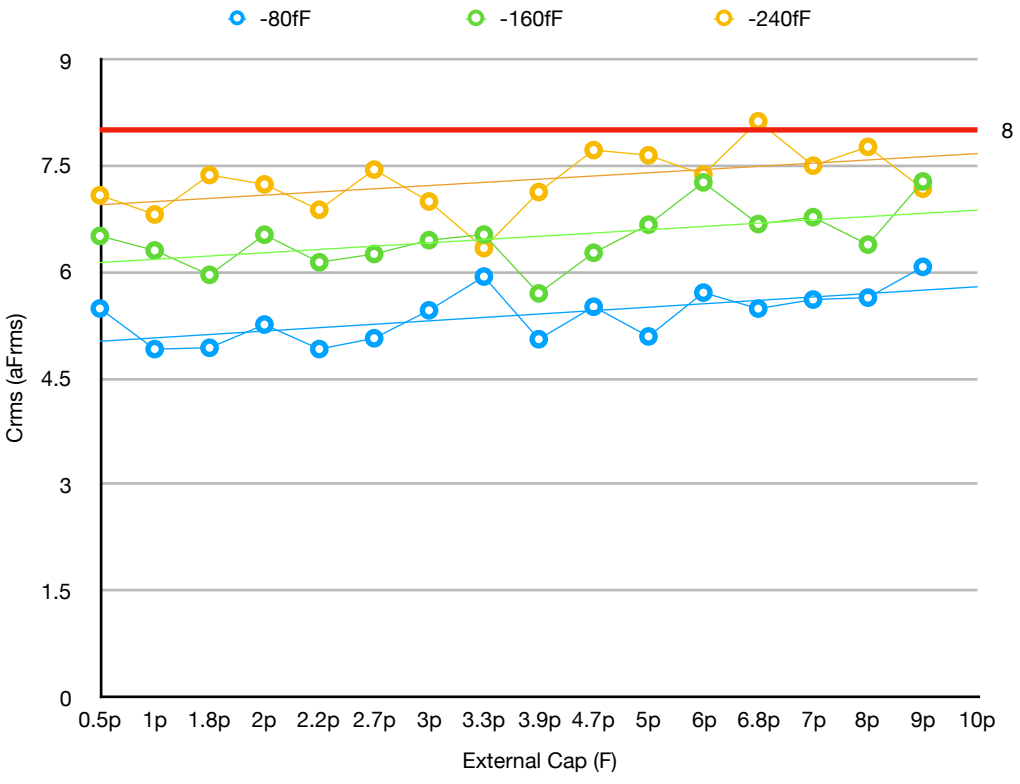


(B)

FIG. 3-6. RESOLUTION VS C_X - MODE 1.
INPUT CAPACITANCE DIFFERENCE: (A) +80, +160, +240fF (B) -80, -160, -240fF.

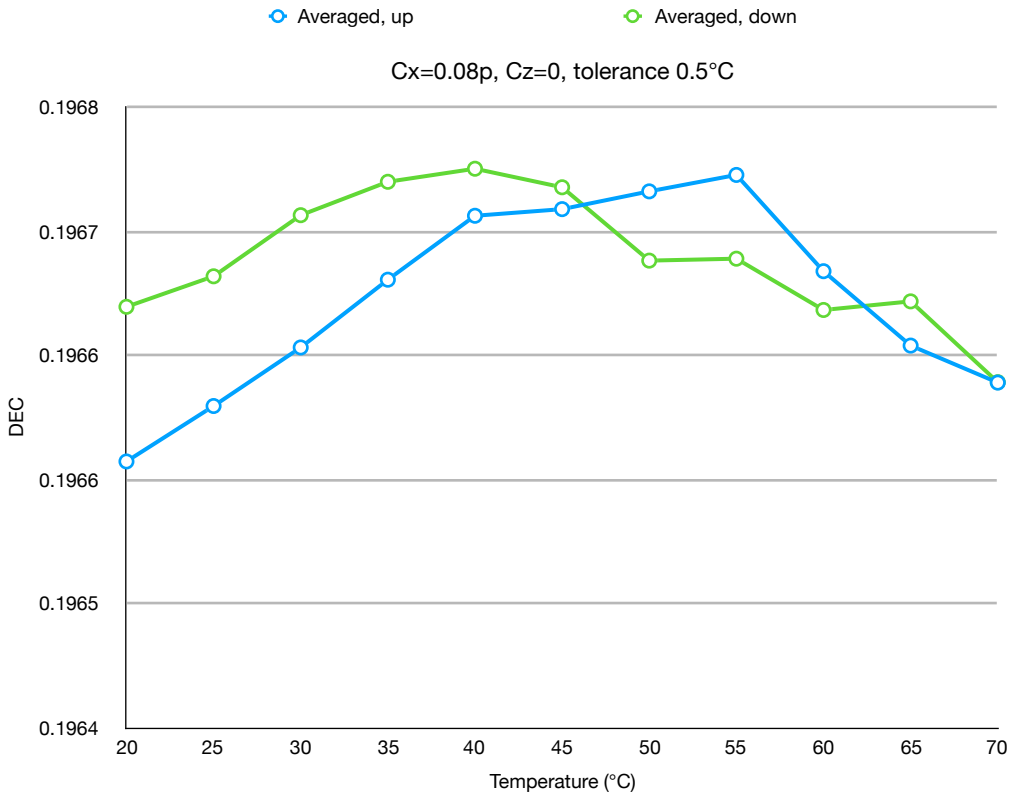


(A)

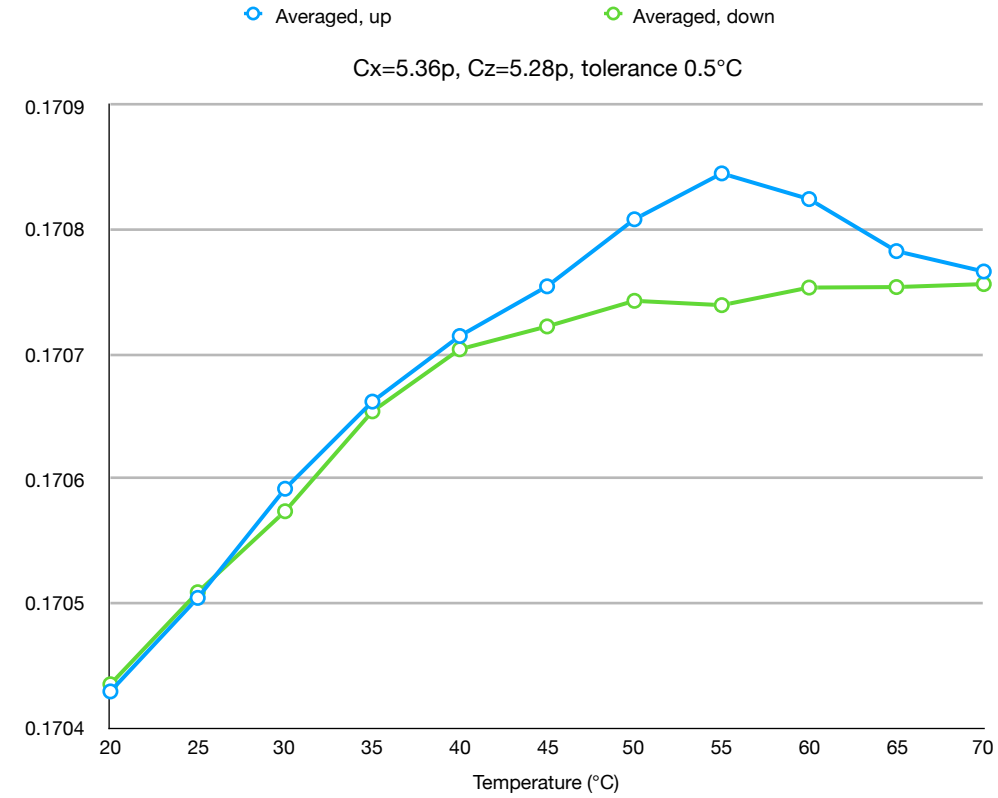


(B)

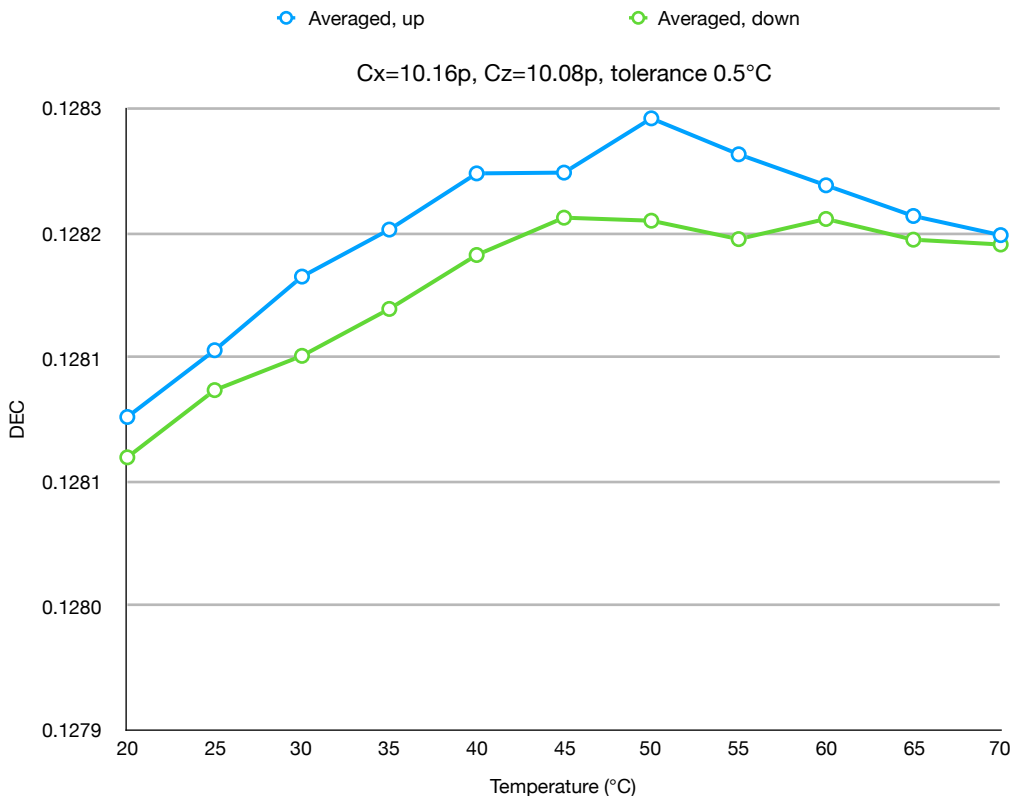
FIG. 3-7. RESOLUTION VS C_X - MODE 2.
INPUT CAPACITANCE DIFFERENCE: (A) +80, +160, +240fF (B) -80, -160, -240fF.


Averaged, up
Averaged, down
Cx=0.08p, Cz=0, tolerance 0.5°C
DEC
0.1968
0.1967
0.1966
0.1966
0.1965
0.1964
20
25
30
35
40
45
50
55
60
65
70
Temperature (°C)

(A)


Averaged, up
Averaged, down
Cx=5.36p, Cz=5.28p, tolerance 0.5°C
0.1709
0.1708
0.1707
0.1706
0.1705
0.1704
20
25
30
35
40
45
50
55
60
65
70
Temperature (°C)

(B)



(C)

FIG. 3-8. DECIMATION VS TEMPERATURE.
(A) C_x = 0.08pF, (B) C_x = 5.36pF, (C) C_x = 10.16pF.

3.3.4 Power Consumption

The power consumption of the chip is 1.8 mW with supply voltage 1.8 V.

3.4 Conclusions

In this chapter, the measurement results of the PCB are present. The resolution for ±80 fF input cap difference is 5.7 aF_{rms} which comes to 20.5 in bits. Measurements in oven to test the temperature stability of the whole system (PCB included) is done with range 20-70°C. And the thermal drift is 17.54 ppm/°C for the worst case. Based on the existing design, this structure can be used in capacitive pressure sensor measurement and piezo-resistive application. The power consumption of the piezo-resistive sensors is about 12 mW or higher, which relaxes the power consumption requirement.

Before the measurement results, the micrograph of the fabricated chip and the measurement setup are shown.

The measurement results and comparison to the expectations are demonstrated in Table 3-1.

TABLE 3-1. PERFORMANCE SUMMARY AND COMPARISON.

	Target	This work
Resolution in bits	20 (8 aF_{rms})	20.5 (5.7 aF_{rms})
Capacitance Range (pF)	0-10	0-10.16
Thermal Drift (ppm/°C)	30	17.54
Power (mW)	2.16	1.8
Conversion Time (ms)	0.5	0.5
FoM (pJ/step)*	-	0.607

$$^{*}\, FoM = \frac{Power_{total} \times T_{Measurement}}{2^{Resolution}}$$

Reference

[1] Guo, Xiaodong, and Stoyan N. Nihtianov. "A capacitive sensing technique for measuring displacement with one floating target electrode." *Industrial Technology (ICIT), 2010 IEEE International Conference on*. IEEE, 2010.

Chapter 4

Conclusions and Future Work

4.1 Conclusions

The thesis objective was to develop a capacitive pressure sensing interface based on an existing structure with piezo-resistive technique.

We converted the CCIA in the existing design into a capacitance-to-digital converter (CVC) to measure the unknown capacitor and transfer the capacitance into digital bitstream with an indirect approach.

The proposed structure was verified by simulation and then fabricated into a chip. The measurement results: the resolution, thermal drift and power consumption all meet the requirement for the design.

In the end, a capacitive pressure interface is developed by updating the existing state-of-the-art piezo-resistive structure with minimum modifications.

4.2 Future Work

Due to time constraints of a master thesis period, there is always room for improvements and various things can be addressed in the future. The expected future work can be categorized into the following parts:

- To verify and certain the reasons for the measurement results of temperature stability, the PCB should be separated from the chip out of oven. Also, to test the variation of the supply and reference signals for the chip could be a more realistic way.

- More interesting measurements can be done with Mode 3, like capacitive bridge structure.

- In this design, we are aiming for looking a generous structure for piezo-resistive pressure sensing readout as well as capacitive one. So we tried to find a way to realize it without changing the existing structure. However, better target can be reached with more optimization.

Acknowledgements

Two and a half years ago, I came to Netherlands with my passion and love for learning. I know that without the support from others, it would not be possible for me to reach this stage.

I would like to thank my supervisor dr. Stoyan Nihtianov for his guidance on the project and this thesis. I respect the way of teaching students very much. He gave me guidance on all the aspects of this design and technical suggestions during this project. I really appreciate his encouragement and patience because there has been hard times in this project, and he is always encouraging me and also teaching me with his way of working.

I wish to thank my daily supervisor Hui Jiang for his invaluable supports contributed much to the completion and improvement of this project. I cannot be more grateful for his valuable suggestions on this design. I am truly lucky to learn from him, especially his way of doing analog design.

I give my sincere thanks to Zu-yao and Lukasz for their patience and strong support.

I would like to thank all my friends both in the Netherlands and in China. These go to Xianwei, Guanchu, Yang Qiao, Xuyang, Chuhan, Jiayi, Zhichao, Huili, etc, for happy times we spend together.

Words cannot express my deepest gratitude to my beloved parents and family members for their unconditional support. Without their boundless love, I would never have had the strength to chase my dream.

Last but not least, I would like to express my sincere gratitude to my boyfriend, Hongming. Thank you for the year you accompanied me. You were not only my best friend but also my best supporter who encouraged me to be a brave and remorseless girl. I also wish to thank your lovely family and wish you a brilliant future.

Yang Liu
21/11/2017

Appendix A

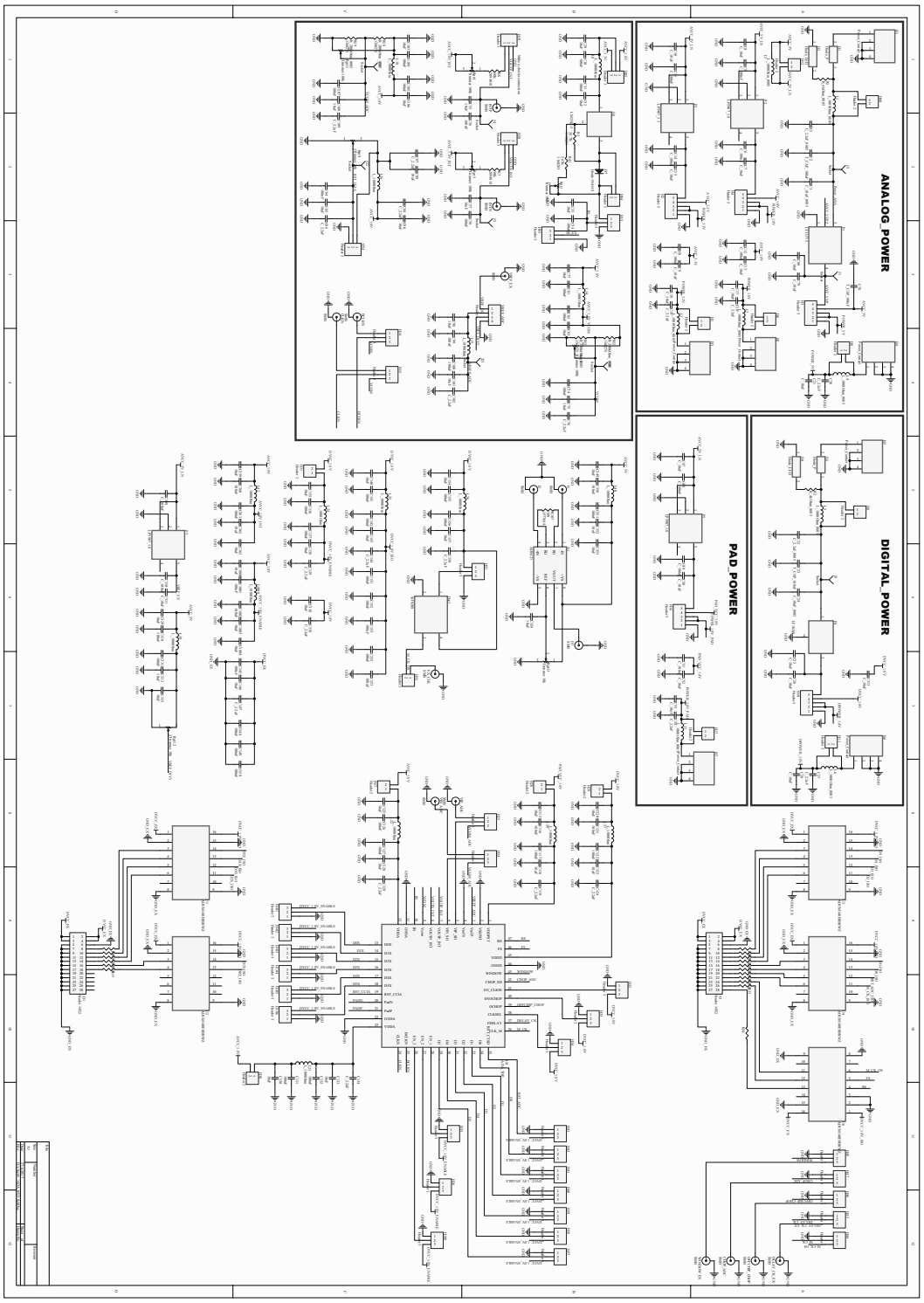


FIG. A-1. PCB SCHEMATICS-1.

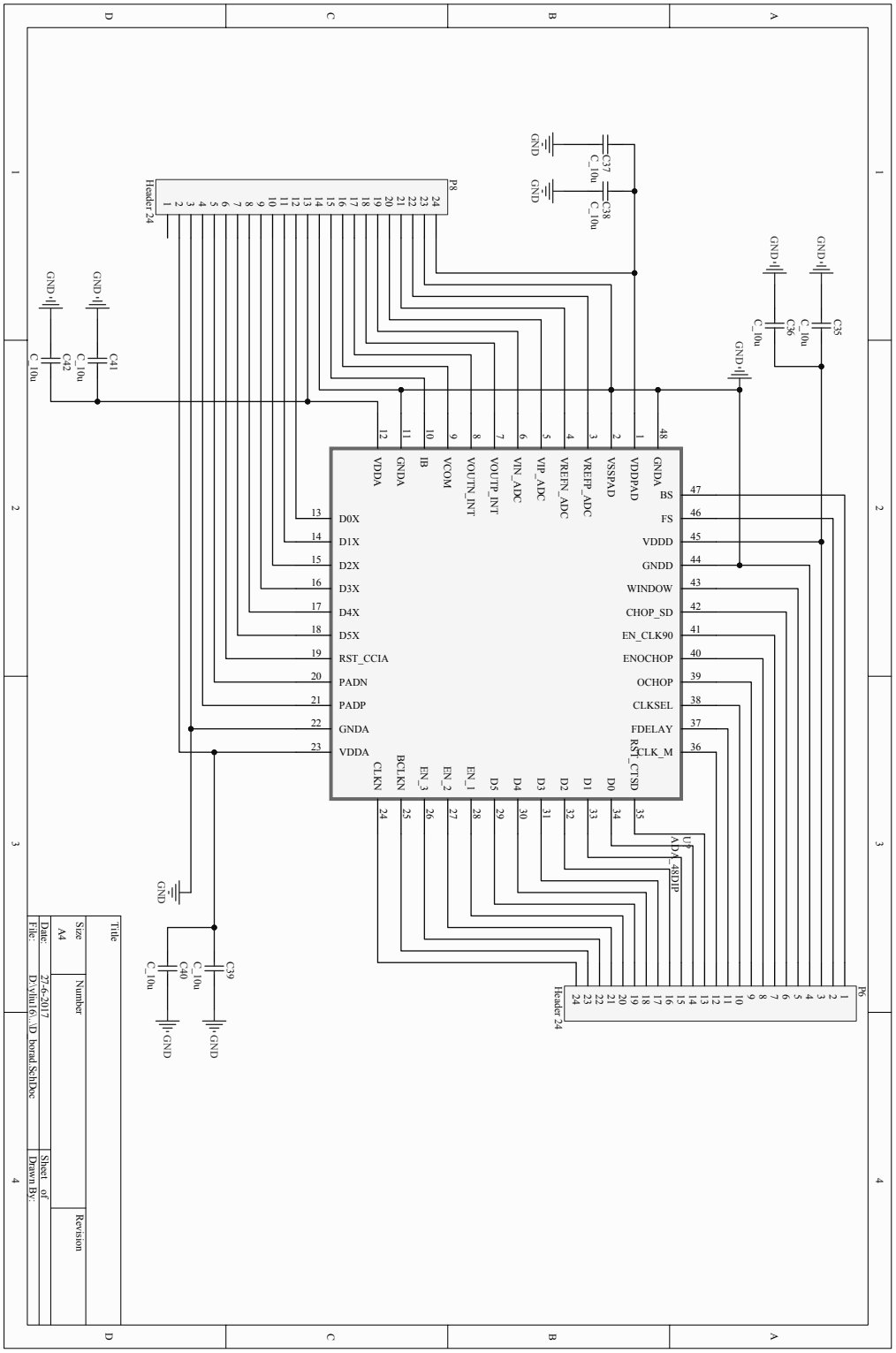


FIG. A-2. PCB SCHEMATICS-2.

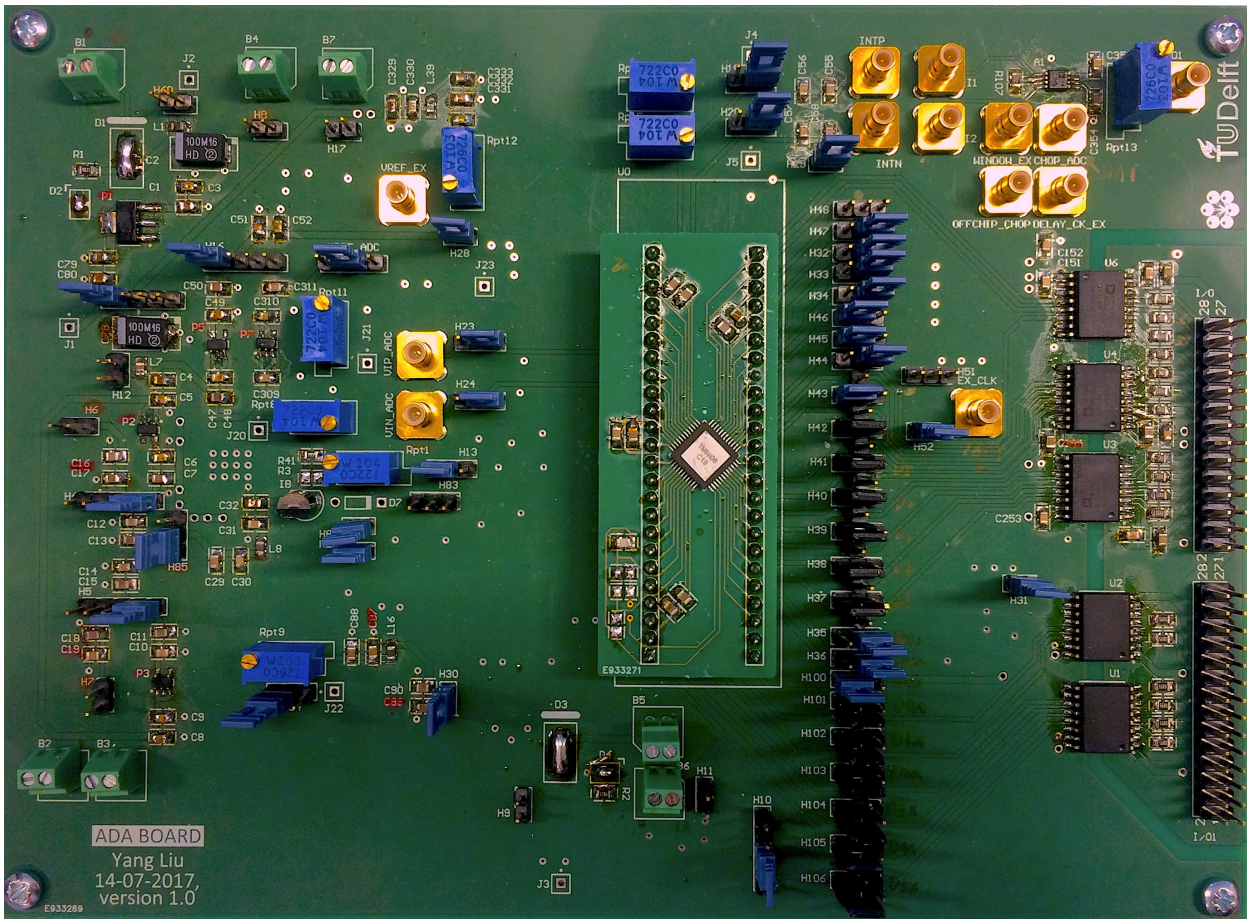
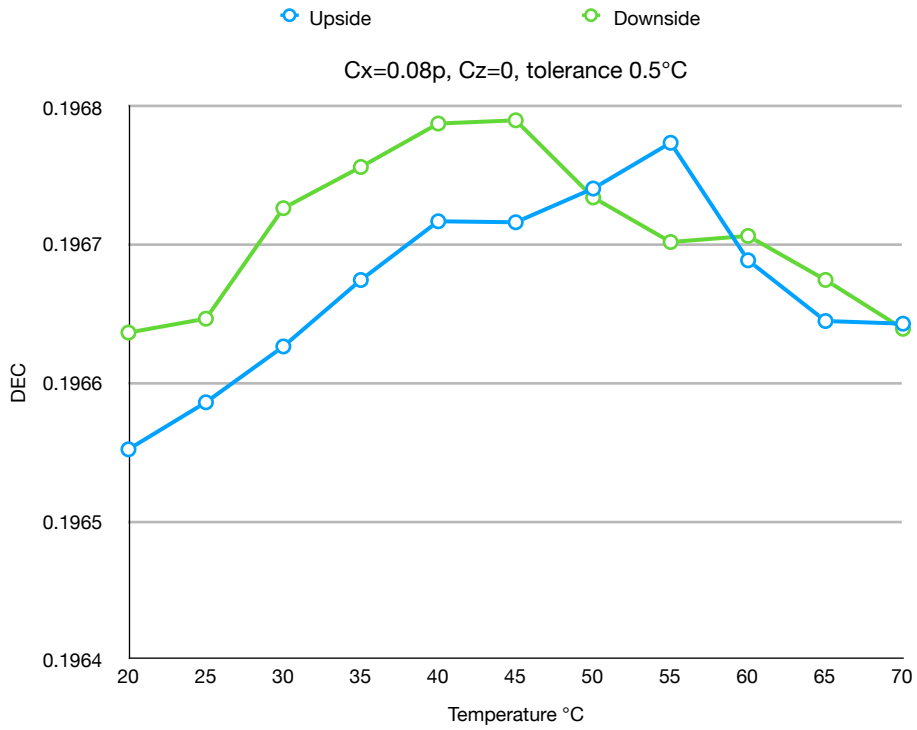
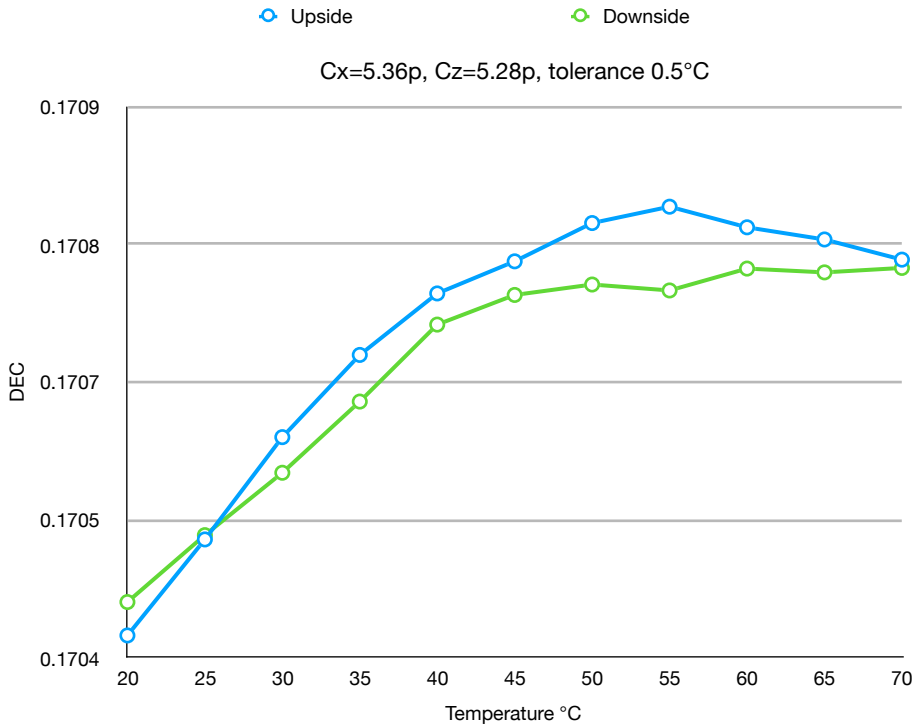


FIG. A-3. THE PHOTO OF PCB.

FIG. A-4. THE PHOTO OF THE MEASUREMENT SETUP.

Appendix B


Upside
Downside
Cx=0.08p, Cz=0, tolerance 0.5°C
0.1968
0.1967
0.1966
0.1965
0.1964
DEC
20
25
30
35
40
45
50
55
60
65
70
Temperature °C


Upside
Downside
Cx=5.36p, Cz=5.28p, tolerance 0.5°C
0.1709
0.1708
0.1707
0.1705
0.1704
DEC
20
25
30
35
40
45
50
55
60
65
70
Temperature °C

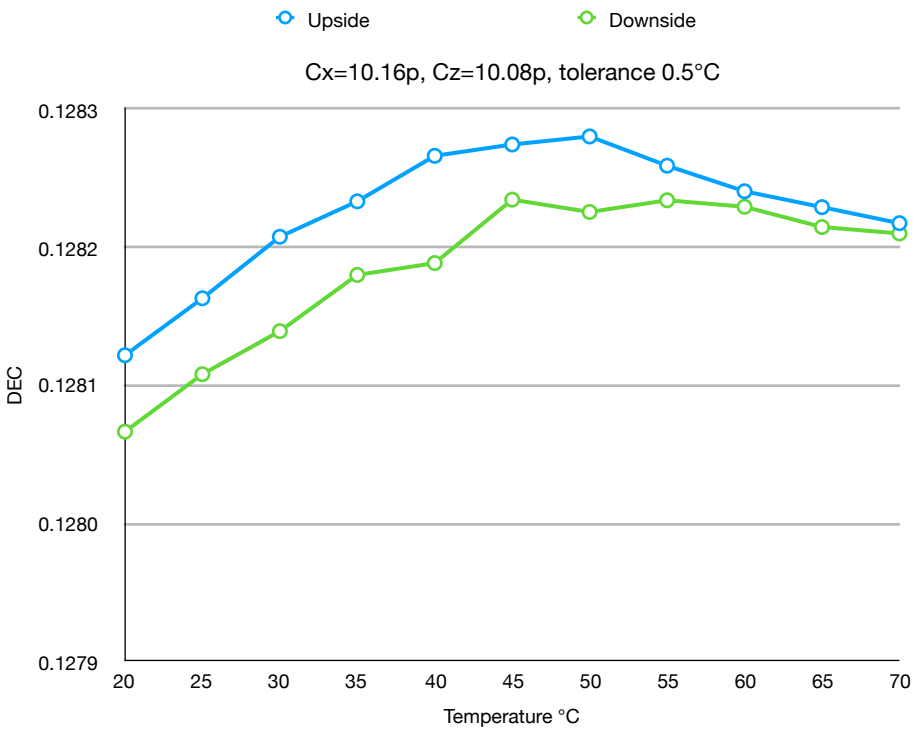
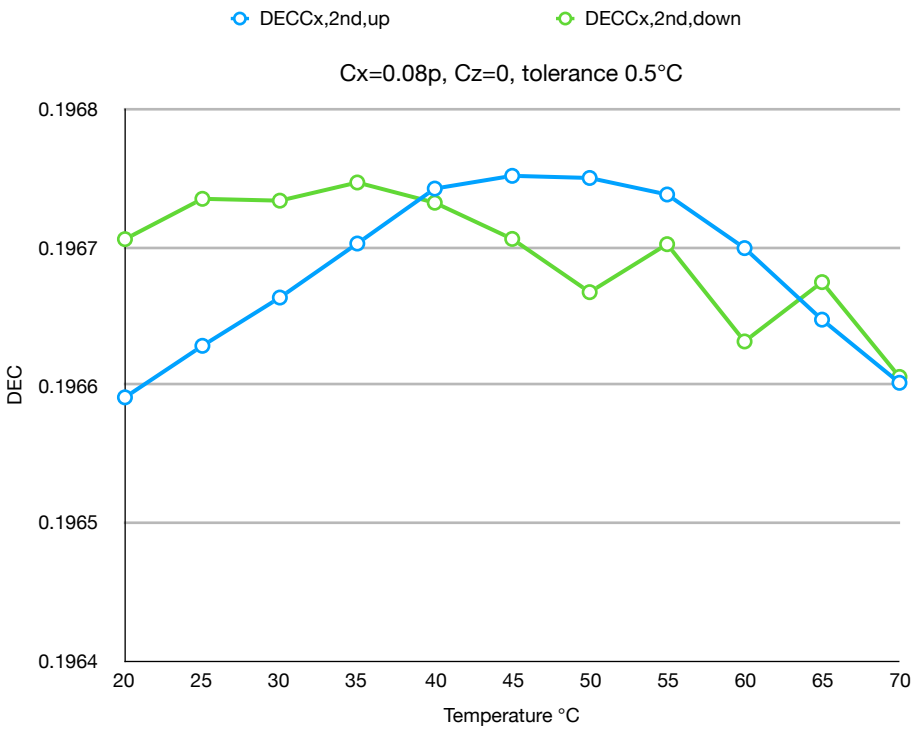


FIG. B-1. DECIMATION VS TEMPERATURE - 1ST MEASUREMENT.



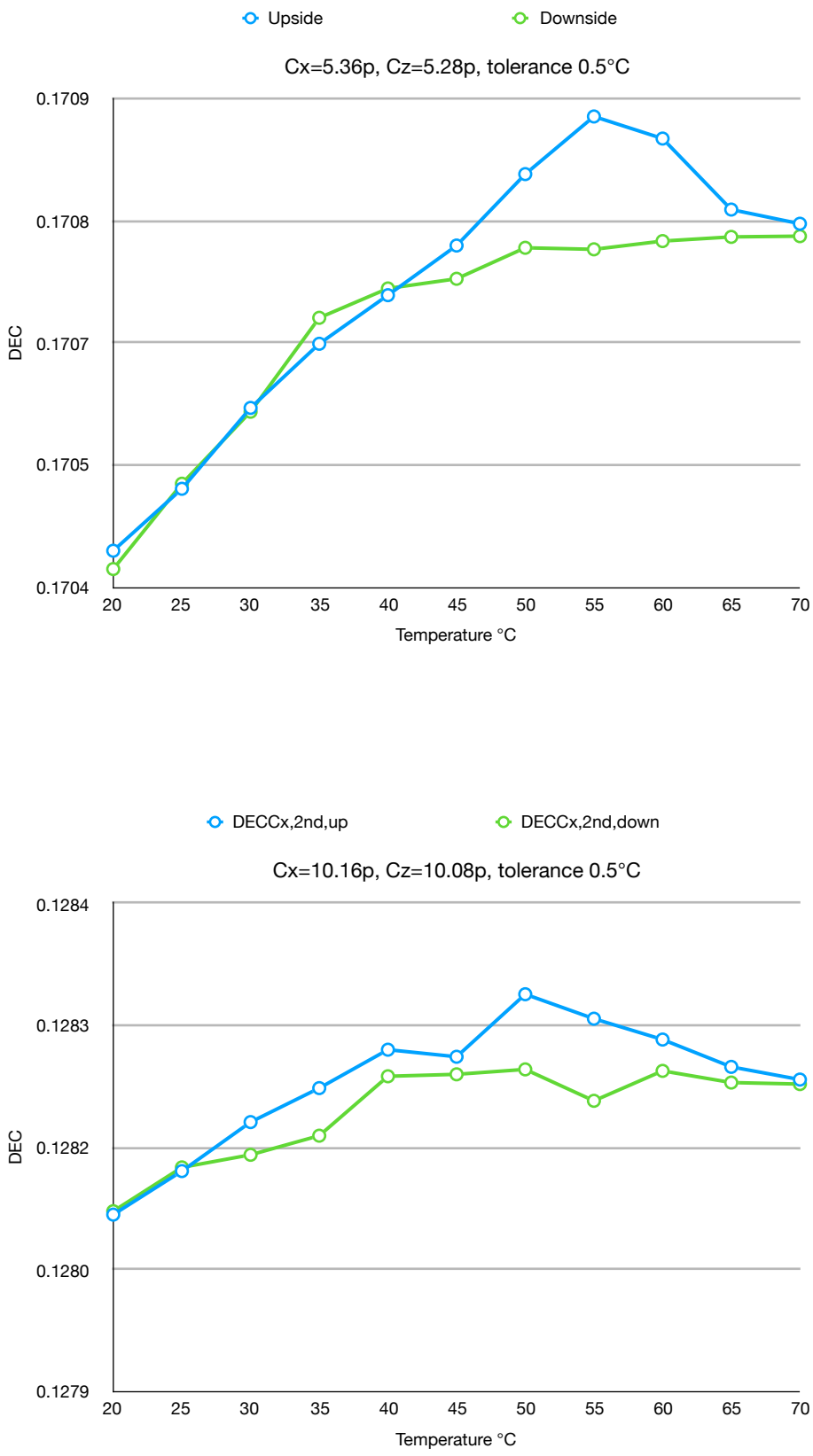


FIG. B-2. DECIMATION VS TEMPERATURE - 2ND MEASUREMENT.

Appendix C

Matlab code for bitstream readout.

```
clear all;
close all;
format long
clc
%%
Fs   = 2e6;
load  temp_x_chipx_BSb.txt;
bs   = temp_x_chipx_BSb;
%%

N = length(bs);

rbw    =  10*Fs/N;
fstep  =  rbw/2;
[fft_bs_dB , f] = fun_calc_psd(bs, Fs, rbw, fstep);

figure(3);
semilogx(f , fft_bs_dB, 'b')
xlabel('Frequency (Hz)');
ylabel('Magnitude (dB)');
grid on; hold on;
%%

for i=1:floor(length(bs)/1000)
   bs_M = bs((i-1)*1000+1:1000*i);
%    DEC_bs(i) = sum(bs_M.*hann(length(bs_M))) / sum(hann(length(bs_M)));
    DEC_bs(i) = sum(bs_M.*triang(length(bs_M))) / sum(triang(length(bs_M)));
end

resolution_in_bit = log2(1 / std(DEC_bs));

DEC = sum(bs.*hann(length(bs)))/sum(hann(length(bs)));
DEC_av = mean(DEC_bs);
rms = std(DEC_bs);

disp('rms = ');

disp( rms );
```