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Investigation on Transient Failure Mode of Asymmetric Trench Gate SiC MOSFET Under Single-Pulse Avalanche Stress

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***Abstract*—In this article, the avalanche withstand capability and transient failure model of commercial 1200 V asymmetric trench gate SiC MOSFETs are investigated by experiment and simulation under single-pulse unclamped inductive switching (UIS) conditions. The limiting avalanche current and limiting avalanche energy of the device are determined by evaluating the voltage and current waveforms, the power dissipation, and the avalanche energy curves before and during avalanche failure. Then, by using the calibrated simulation model, the sequence between the critical electric field stress and critical thermal stress suffered by the device is revealed, and the transient failure mode of the device is proved to be the thermal runaway. Moreover, after decapping the failed device, the failure mode of the device is further confirmed by analyzing the failure point. Finally, by using the focused ion beam (FIB) technology, the failure mechanism of the device is confirmed as a structural rupture caused by avalanche thermal stress.**

Keywords*—*unclamped inductive switching* (*UIS*), *silicon carbide* (*SiC*), *avalanche breakdown, asymmetric trench gate.

I. Introduction

Given the outstanding electrical and thermal properties of silicon carbide (SiC), there is a consensus among researchers and engineers that SiC will progressively supplant silicon (Si) and emerge as the primary material for next-generation power semiconductor devices [1]. In terms of device performance, SiC MOSFETs offer several advantages over traditional Si-MOSFETs and Si-IGBTs. They not only exhibit higher breakdown voltage [2], increased switching frequency [3], and enhanced power density [4] but also demonstrate suitability for high-temperature [5], high-radiation [6], and high power applications [7].

With advancements in SiC epitaxy technology [8], device structure innovation [9, 10], and manufacturing techniques [11, 12], SiC MOSFETs have experienced rapid commercialization by numerous manufacturers [2, 13-15]. Transitioning from planar gate to trench gate, SiC MOSFETs strive consistently to increase power density and reduce specific on-resistance[16, 17]. Moreover, progressing from double trench gate to asymmetric trench gate, SiC MOSFETs undergo continuous optimization to enhance reliability and robustness [1, 13]. Consequently, through these improvements in fabrication processes and innovative structural designs [18], the electrical characteristics of SiC MOSFETs have been significantly enhanced [19-22]. Nevertheless, challenges persist in the reliability of SiC MOSFETs due to limitations in etching process capabilities [23] and gate oxide reliability [24, 25].

In terms of applications, SiC MOSFETs are widely used in high-frequency switching and inductive load circuits, including solenoid actuators, anti-lock braking systems (ABS), and engine control units (ECU) in the automotive field [26]. In these application scenarios, when the MOSFET is turned off, the inductor generates a back electromagnetic force (EMF) that applies a high voltage to the MOSFET due to the abrupt interruption of the inductive current. This eventually leads to an avalanche impact on the MOSFET [26, 27]. Simultaneously, the corresponding energy stored in the unclamped inductive load needs to be dissipated through the switching device, with the energy primarily characterized by the integral of the product of high voltage and high current during the turn-off period. Consequently, the resulting thermoelectric stress from this demanding switching process is self-evident and serves as the primary cause of device failure. Therefore, whether it is the inherent load inductance of electric motors and solenoids or the stray inductance caused by wire harnesses and circuit boards, greater attention needs to be paid to the switching process of MOSFETs in inductive load circuits [28, 29].

This study investigates the avalanche withstand capability and transient failure model of the 1200 V asymmetric trench gate SiC MOSFET (IMW120R140M1H) through single-pulse avalanche stress experiments and simulations. The aim is to determine the failure characteristics and modes of the device by analyzing recorded current and voltage waveforms, power dissipation, avalanche energy curves, and static characteristic curves. Additionally, a calibrated finite-element simulation model is employed to uncover the internal electrothermal stress and transient failure mode of the device during avalanche failure. Furthermore, the failure point and mechanism of the device are confirmed through decapsulation and focused ion beam (FIB) technologies.

II. Setup and Mechanism

A. UIS Experiment and Simulation Setup

For the decoupled single-pulse UIS test, the ITC5514 testers were utilized as the test platform. All tests were conducted at a room temperature of 25 ℃. Regarding the experimental parameter settings, the test circuit's bus voltage (V_{DC}) was set to 100 V, and the peak avalanche current (I_{AV}) was treated as the dependent variable to adjust the different avalanche stresses for the Device Under Test (DUT). Consequently, the peak avalanche current (I_{AV}) was modified by adjusting the two independent variables of the gate pulse

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width (t_{ON}) and the inductive load (L). For subsequent discussions and analyses, t_{ON} is defined as $t_{ON\text{-}exp}$ used in the experiment, while $t_{ON\text{-}sim}$ is used in the simulation. To investigate the transient failure model and failure mechanism of the asymmetric trench gate 4H-SiC MOSFET under avalanche impact, we employed Sentaurus Technology Computer-Aided Design (TCAD) software to evaluate the thermoelectric stress experienced by the device

B. UIS Experiment Mechanism

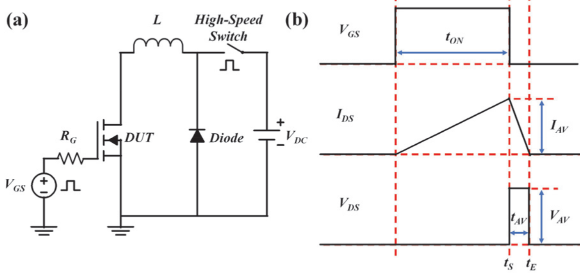

Fig. 1. (a) Schematic of the equivalent test circuit for the UIS test. (b) Ideal UIS test input and output waveforms.

Fig. 1(a) depicts the schematic of the equivalent test circuit and the ideal input and output waveforms for the UIS test. During the UIS test, the DUT is turned on by applying the gate pulse width (t_{ON}) to the gate, and the high-speed switch is simultaneously activated. Subsequently, the drain-source voltage (V_{DS}) of the DUT remains constant, while the drain-source current (I_{DS}) starts to increase gradually in response to the inductive load (L) and the bus voltage (V_{DC}). The relationship between I_{DS} and these parameters is expressed as follows:

$$L\frac{dI_{DS}}{dt} = V_{DC} \tag{1}$$

At the end of the gate pulse, the inductance current reaches its peak avalanche current (I_{AV}), which can be calculated using the following equation:

$$I_{AV} = \frac{V_{DC}}{L} \times t_{on} \tag{2}$$

When the DUT is turned off, the DC power supply is disconnected from the test circuit by deactivating the high-speed switch. Simultaneously, the current in the inductor flows through the antiparallel diode, resulting in a rapid change in the inductive current within a short period of time (dI_{DS}/dt). Additionally, this varying inductive current induces the peak avalanche voltage (V_{AV}) across the inductive load, subjecting the DUT to avalanche stress. Therefore, V_{AV} can be mathematically expressed as:

$$V_{AV} = L \times \frac{dI_{DS}}{dt} \tag{3}$$

Subsequently, all the energy stored in the inductive load is transferred to the DUT, driving it into an avalanche state. During this process, the drain-source current (I_{DS}) decreases linearly, while the peak avalanche voltage (V_{AV}) of the device abruptly drops to zero after a short period of time. Eventually, the device undergoes a complete avalanche impact and reaches a steady state. The avalanche time ($t_{AV} = t_E - t_S$) and avalanche energy (E_{AV}) can be calculated using the following equations:

$$t_{AV} = \frac{L}{V_{AV}} \times I_{AV} = t_E - t_S \tag{4}$$

$$E_{AV} = \frac{1}{2} \times L \times {I_{AV}}^2 = \int_{t_S}^{t_E} V_{DS}(t) \cdot I_{DS}(t)\, dt \tag{5}$$

III. Result and Discussion

A. Single-Pulse UIS Tests

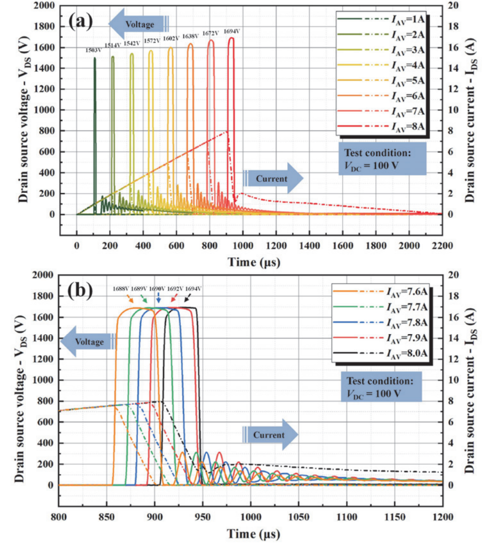

Fig. 2. The voltage and current waveforms of asymmetric trench gate SiC MOSFET before and during avalanche failure (a) with 1.0 A as the current increase step (b) with 0.1 A as the current increase step.

To verify the withstand capability of DUT at different avalanche energy (E_{AV}) levels, the peak avalanche current (I_{AV}) of the DUT is incrementally increased from 1.0 A to 7.0 A in 1.0 A steps. Once the I_{AV} reaches 7.0 A, in order to accurately monitor the performance and parameter changes of DUT during the early stages of failure, the I_{AV} is further adjusted in increments of 0.1 A, gradually increasing from 7.6 A to 8.0 A until the DUT reaches the failure state.

The voltage and current waveforms of the DUT before and during avalanche failure are illustrated in Fig. 2(a) and Fig. 2(b), respectively. It is clear that as the $t_{ON\text{-}exp}$ and L values increase, both the I_{AV} and V_{AV} of the DUT also increase. Eventually, when the I_{AV} reaches 8.0 A, the DUT undergoes avalanche failure. Additionally, it is worth mentioning that all voltage waveforms display slight amplitude oscillations following the avalanche, except for the waveform observed during DUT failure in an avalanche. Specifically, the oscillation in the waveform is predominantly caused by LC resonance, which arises due to parasitic parameters within the test circuit.

Fig. 3(a) shows the comparison of the voltage and current waveforms of the DUT both before and during avalanche failure. The I_{AV} values during these instances are 7.9 A and 8.0 A, respectively. In the last test prior to avalanche failure, where L is set to 11.34 mH, and $t_{ON\text{-}exp}$ is set to 893.7 μs, the I_{AV} reaches 7.9 A. Following the gate being turned off, the energy stored in the inductor discharges through the DUT, causing V_{DS} to be clamped at 1692 V, and subsequently, I_{DS} decreases in a linear fashion. As I_{DS} approaches zero, V_{DS} experiences a sudden drop until the DUT reaches a stable state, with the entire avalanche duration lasting 54 μs. The waveform effectively illustrates the complete switching process of the DUT under the impact of an avalanche due to

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the decoupled UIS circuit.

In the test during avalanche failure, with L set to 11.37 mH and $t_{ON\text{-}exp}$ set to 907.2 μs, the I_{AV} reaches 8.0 A. As the gate is turned off, the V_{DS} of the DUT sharply rises to 1694 V while I_{DS} continues to decrease linearly. Eventually, the DUT experiences avalanche failure as V_{DS} suddenly collapses from 1682 V to 2.5 V, and the entire avalanche event lasts 40.5 μs. During this period, the I_{AV} of the DUT undergoes a sudden rise from a linear decline state until the device completely fails. The waveform directly illustrates that the failure characteristics of the DUT involve the loss of voltage-blocking capability and the formation of a conductive path between the drain and the source.

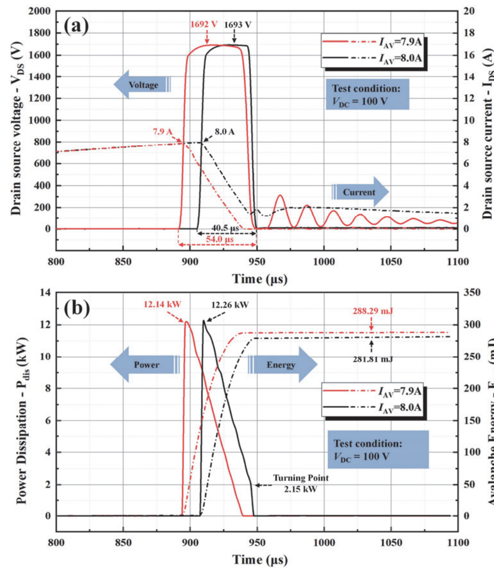

Fig. 3. (a) The comparison of the voltage and current waveforms, (b) the power dissipation and avalanche energy curves of the asymmetric trench gate SiC MOSFET before and during avalanche failure.

The corresponding comparison of the power dissipation and avalanche energy curves of the DUT before and during avalanche failure is depicted in Fig. 3 (b).

In the last test before avalanche failure (I_{AV} = 7.9 A), the DUT exhibits a relatively low power dissipation before the gate is turned off. However, upon turning off the gate, the dissipated power of the DUT experiences a rapid and substantial increase, reaching a maximum value of 12.14 kW. Simultaneously, as the power dissipation decreases approximately linearly, the avalanche energy of the DUT reaches its peak at 288.29 mJ. This curve visually illustrates the two most critical transient states for the DUT: the maximum power dissipation and the maximum avalanche energy. These states correspond to critical electric field stress and thermal stress, respectively.

In the test during avalanche failure (I_{AV} = 8.0 A), the DUT also maintains a relatively low power dissipation prior to gate turn-off. However, when the gate is turned off, the power dissipation of the DUT suddenly and rapidly rises to the maximum value of 12.26 kW. The power dissipation curve is divided into two stages due to the turning point at 2.15 kW. Ultimately, the maximum avalanche energy during avalanche failure is only 281.81 mJ, which is significantly lower than the maximum avalanche energy before avalanche failure (288.29 mJ). This curve clearly demonstrates that the rate of decline in the power dissipation curve after DUT failure is significantly higher than before DUT failure. This indicates that when avalanche failure occurs, the remaining energy in the inductive load is released in a more efficient manner rather than through the unclamped inductive switching circuit.

Based on the above discussion and analysis, it can be concluded that the DUT exhibits a limiting avalanche current of 7.9 A and a limiting avalanche energy of 288.29 mJ. Furthermore, one of the avalanche failure characteristics of the DUT is the occurrence of a drain-source short circuit. Since the DUT has already experienced critical electric field stress prior to avalanche failure, and the decline rate of the power dissipation curve significantly increases after avalanche failure, it can be tentatively concluded that the failure model of the DUT is associated with thermal failure.

B. Transient Finite Element Simulation

To conduct a more precise investigation into the transient failure mechanism and mode of the asymmetric 4H-SiC MOSFET under avalanche stress, a mixed-mode TCAD simulation is employed to analyze the final test where the DUT failed under the same conditions (I_{AV} = 8.0 A). Typically, when the device is in the avalanche state, the internal structure is subjected to thermoelectric stress [30]. In fact, there exists a time sequence between electric field stress and thermal stress during avalanche impact.

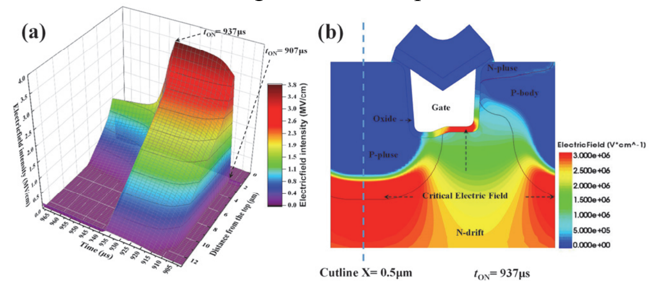

Fig. 4. (a) The 3D electric field distribution along the channel direction from the bottom to the top of the device at different times. (b) The 2D electric field distribution of the device at the critical state of the electric field.

Fig. 4 (a) shows the three-dimensional (3D) distribution of the electric field along the channel direction, from the bottom to the top of the device, at various time points. During the time interval of 901 μs to 907 μs, when $t_{ON\text{-}sim}$ is in this range, the electric field distribution inside the device appears mostly flat, with a slight bulge observed at the PN junction of the P-plus and N-drift regions (at around 2 μm). This distribution is primarily influenced by the on-state voltage of the device.

Once $t_{ON\text{-}sim}$ reaches 907 μs, the gate channel of the device is turned off, and the device experiences avalanche impact due to the high voltage across the drain and source. Concurrently, the internal electric field distribution of the device undergoes an abrupt transition from a flat distribution to a triangular shape. This intense state persists for a duration of 30 μs. When $t_{ON\text{-}sim}$ reaches 937 μs, the electric field inside the device reaches its peak value of 3.78 MV/cm. Subsequently, the electric field rapidly decreases, forming an equally proportioned triangle shape.

Fig. 4 (b) shows the two-dimensional (2D) electric field distribution of the device during the critical state of the electric field ($t_{ON\text{-}sim}$ = 937 μs). It is evident that the critical

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electric field is primarily concentrated at the edge of the P-plus region and a portion of the gate oxide region without being surrounded by the P-plus region. This observation directly indicates that the asymmetric structure with the P-plus region effectively mitigates electric field crowding at the bottom of the gate oxide layer, particularly at the corners below the channel. As a result, it helps prevent the breakdown of the gate oxide layer.

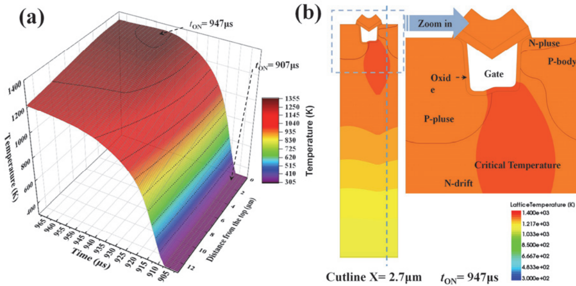

Fig. 5. (a) The 3D temperature distribution along the channel direction from the bottom to the top of the device at different times. (b) The 2D temperature distribution of the device at the critical state of temperature

Fig. 5(a) shows the 3D temperature distribution along the channel direction, from the bottom to the top of the device, at different time intervals. When $t_{ON\text{-}sim}$ falls within the range of 901 μs to 907 μs, the temperature distribution within the device remains relatively flat. Correspondingly, the peak temperature recorded in the device is 308.70 K. However, once $t_{ON\text{-}sim}$ reaches 907 μs and the gate channel of the device is turned off, the avalanche current starts to flow linearly through the P-plus region toward the source. Simultaneously, the overall temperature inside the device experiences a significant rise. This elevated temperature state persists for 40 μs until the device reaches its peak temperature of 1351.20 K at $t_{ON\text{-}sim}$ 947 μs. Analyzing the temperature contour during the first 20 μs (907 μs to 927 μs) reveals a uniform temperature distribution throughout the device, from top to bottom. Conversely, during the last 20 μs (927 μs to 947 μs), the internal temperature of the device exhibits a gradient distribution due to heat accumulation at the top of the device.

Fig. 5(b) presents the two-dimensional (2D) temperature distribution of the device during the critical temperature state ($t_{ON\text{-}sim}$ = 947 μs). It is apparent that the critical temperature within the device primarily concentrates in the region below the trench gate, which is not encompassed by the P-plus region. Notably, the critical temperature region beneath the trench gate overlaps with the gate oxide layer and contacts the edge of the P-plus region. At this stage, the peak temperature inside the device reaches 1352.74 K, which is lower than the intrinsic temperature limit of 4H-SiC (1543.15 K) but significantly impacts the reliability of the device. This observation directly indicates that when the device reaches a critical temperature state, the primary heat accumulation occurs in the region beneath the trench gate.

Consequently, this finding directly confirms that the failure mechanism of the asymmetric trench gate SiC MOSFET in the single-pulse UIS test is primarily attributed to thermal runaway, resulting from the rapid elevation of the junction temperature to the critical state.

C. Device Failure Region Confirmation

Fig. 6 shows the surface optical microscope image of the DUT after failure and decapsulation. It is apparent that the device exhibits a circular failure point in the source pad area near the gate pad area, occupying an area of approximately 0.05 mm^2. Notably, the bonding wires connecting the source pad and gate pad remain intact [31]. Furthermore, it can be observed that the failure point results in the burning of the metal layer on the surface of the gate pad near the failure point. However, the isolation region between the gate pad and the source pad does not suffer significant damage. Taking into consideration that the melting point of the aluminum-copper alloy (0.25% ~ 2.5% Cu) used as the surface metal layer of the power device is around 930 K, the extent of the metal layer burning at the failure point directly indicates that the transient failure model of the DUT is attributable to thermal runaway [32, 33].

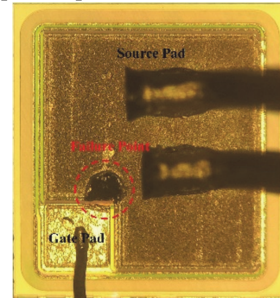

Fig. 6. The surface optical microscope image of asymmetric 4H-SiC MOSFET after failure and decapsulation.

To further characterize the failure mechanism of the DUT, the scanning electron microscope (SEM) images of the DUT are presented in Fig. 7 (a). The images clearly reveal the catastrophic burning at the failure point of the DUT. Upon closer inspection, significant morphological changes are evident in the metal layer located at the edge region (R1) surrounding the failure point. Additionally, the metal oxide layer in the middle region (R2) of the failure point exhibits delamination and curling, which can be attributed to the high temperatures experienced. Furthermore, the metal layer at the center region (R3), which is the most severely burned area, has completely melted.

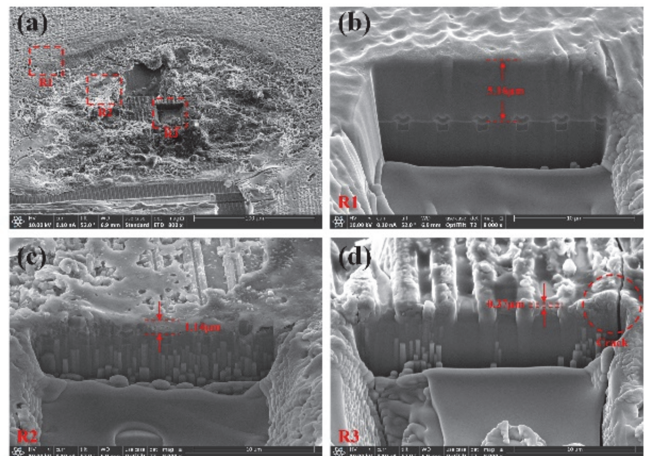

Fig. 7. (a) Scanning electron microscope (SEM) images of failure point of asymmetric 4H-SiC MOSFET. (b), (c), and (d) Focused ion beam (FIB) cross-sectional images of asymmetric trench SiC MOSFET.

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Subsequently, three regions spanning from the edge to the center of the failure point are etched using focused ion beam (FIB) technology, as illustrated in Fig. 7(b), (c), and (d). It is clearly observable that the thickness of the metal layer progressively decreases from the edge region to the center region of the failure point, measuring 5.16 μm, 1.14 μm, and 0.37 μm, respectively. This further substantiates the damage inflicted upon the DUT due to the transient high temperatures generated by thermal runaway. Additionally, a visible crack running along the gate sidewall can be discerned in the center region of the failure point, as displayed in Fig. 7(d). Based on the crack's position on the DUT, it can be inferred that the failure mechanism involves the rupture of the silicon carbide material on the conductive channel side, triggered by the transient high temperature. By integrating this finding with the earlier discussion on the gate oxide layer reliability, further support is provided for the accuracy of the equivalent circuit following device failure.

IV. Conclusion

In this article, the avalanche withstand capability and transient failure model of commercial 1200 V asymmetric trench gate SiC MOSFET is investigated by single-pulse UIS experiment and finite-element simulation methods. In the experiment, a decoupled UIS circuit is used to test the avalanche current and avalanche energy withstand capacity of the device. The limiting avalanche current and limiting avalanche energy of the device at a bus voltage of 100 V are 7.9 A and 288.29 mJ, respectively. Through the comparative analysis of the current and voltage waveforms, the power dissipation, and avalanche energy curves before and during device failure, it is preliminarily determined that the failure mode of the device is thermal failure. In the simulation, the comparative analysis of 3D and 2D electric field and temperature distribution reveals that the device is first subjected to the critical electric field stress and then thermal stress during avalanche impact, with a 10 μs time gap. Meanwhile, the failure mode of the device is determined as thermal runaway. In addition, after decapping the failed device, the failure mode of the device is further confirmed as thermal runaway through the analysis of the failure point. Finally, it is proved by FIB technology that the failure mechanism of the device is the structural rupture caused by avalanche thermal stress.

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