A Low Distortion Sine-Wave Generator based on Resistive DACs

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Xiaoran Li
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ABSTRACT

This thesis proposes a novel low distortion, on-chip sine-wave generator. A low distortion input is required in many test and measurement setups for analog and mixed-signal systems, where the input signal should have less distortion than that contributed by the device under test (DUT). For conventional oscillators, there is a compromise between output quality and circuit complexity, as high-order filter is required to achieve high selectivity.

In recent years, harmonic cancellation (HC) based sine-wave generators become more attractive as it can generate low distortion signal at low hardware cost. Unfortunately, most HC based sine-wave generators suffer from mismatch and process variations, which limit the achieved spectral purity.

This work aims to develop a generator which is insensitive to these limiting factors. A two-stage HC based approach is proposed. It can achieve low distortion signal generation while keeping the simplicity of the whole system. The project involves the design and test of a prototype chip. The measurement results are provided to verify the feasibility of the proposed generator.

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INTRODUCTION

1

A sine-wave generator often serves as the input signal source in test and measurement setups for analog and mixed-signal systems such as amplifiers and ADCs. In such applications, it is important that the distortion of the input signal is much less than that contributed by the device under test (DUT). However, most precision sine-wave generators are off-chip components or instruments, and thus are significant parts of the total cost of test and measurement systems. The purpose of this work is to realize a low-cost on-chip sine-wave generator, which provides sufficient linearity for precise measurements.

1.1. CLOSED-LOOP VERSUS OPEN-LOOP SINE-WAVE GENERATORS

There are generally two types of topologies used to realize on-chip sine-wave generators: closed-loop topologies and open-loop topologies. Both will be discussed in the following, together with their pros and cons.

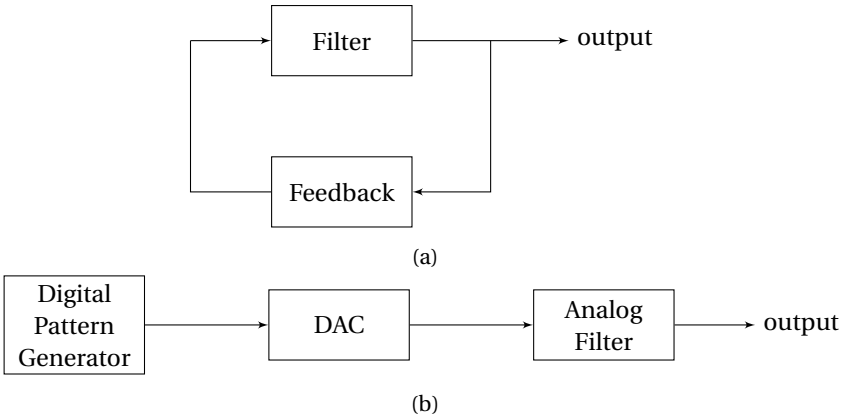


Figure 1.1: (a) Closed-loop and (b) open-loop signal generator

A closed-loop signal generator, which is essentially an oscillator, consists of a bandpass filter (BPF) and a feedback network as illustrated in Figure 1.1a. The oscillation frequency must be around the center frequency of the bandpass filter f_c, since the circuit's loop gain decreases rapidly as the oscillation frequency deviates from f_c. With a bandpass filter with an infinite Q factor, the loop gain is infinite at the center frequency and zero at other frequencies, thus the output signal will be a pure sine-wave located at the center frequency. However, ideal bandpass filters do not exist and so the total harmonic distortion (THD) of the output signal will increase as Q decreases. For instance, to achieve a THD lower than -62dBc, a Q factor larger than 70 is required [1]. Figure 1.2 illustrates a popular multiple feedback BPF [2]. Its central frequency and Q factor are given in Equations 1.1 and 1.2 respectively, revealing that achieving both high Q and low center frequency require large capacitors and resistors. In addition, the open-loop gain of the opamp should be 40dB above the peak gain of a filter section to achieve a maximum gain error of 1% [3]. Thus, an amplifier with a high GBW is also a necessity, resulting in a sizable area and a complicated design. Furthermore, these active components are

process-sensitive and need to be redesigned when switching from an old technology to a new technology.

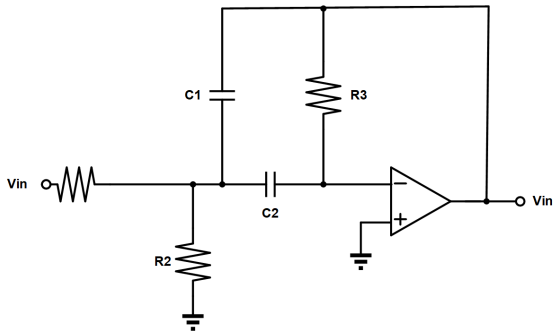


Figure 1.2: A multiple feedback BPF

$$f_c = \frac{1}{2\pi}\sqrt{\frac{1}{R_3 C_1 C_2}\left(\frac{1}{R_1}+\frac{1}{R_2}\right)} \tag{1.1}$$

$$Q = 2\pi f_0 \frac{C_1 C_2}{C_1 + C_2} R_3 \tag{1.2}$$

An open-loop sine-wave generator consists of a digital pattern generator, a digital to analog convertor (DAC) and an analog filter as shown in Figure 1.1b. This is the topology on which conventional memory-based, direct digital frequency synthesizers are based. Compared to closed-loop generator, open-loop generator is more digital-friendly. It typically employ a multibit DAC, which requires large areas [4]. Moreover, a multibit DAC is sensitive to component mismatch and process variations. To solve this problem, a ΣΔ modulation based approach was proposed in [5]. It employs a 1-bit DAC, instead of a multibit one, to generate the bitstream. However, a ΣΔ based generator suffers from quantization noise, and thus requires a high-order analog filter to attenuate the noise.

1.2. STATE-OF-THE-ART OF SINE-WAVE GENERATORS

Several state-of-the-art on-chip sine-wave generators will be described in this section, followed by a discussion of the pros and cons of each design.

The ΣΔ modulation seems to be a very attractive solution. As a simple 1-bit DAC can be used [9], as illustrated in Figure 1.3, the generated signal has a clean frequency band adjacent to the fundamental. Unfortunately, it suffers from quantization noise. Although the generated signal has almost no harmonic at low frequencies, there are large harmonics at high frequencies due to quantization noise [4]. [10] proposed a ΣΔ oscillator achieving good SFDR and THD behavior, but at the cost of a sixth-order low pass filter. [5] based on similar ΣΔ modulation realized a ΣΔ oscillator on-chip, but with a third-order LPF, it only achieve 60dBc THD .

To relax the filter's requirements, the harmonic cancellation (HC) technique was proposed. HC is a linearization technique, which has been used extensively in recent works

1

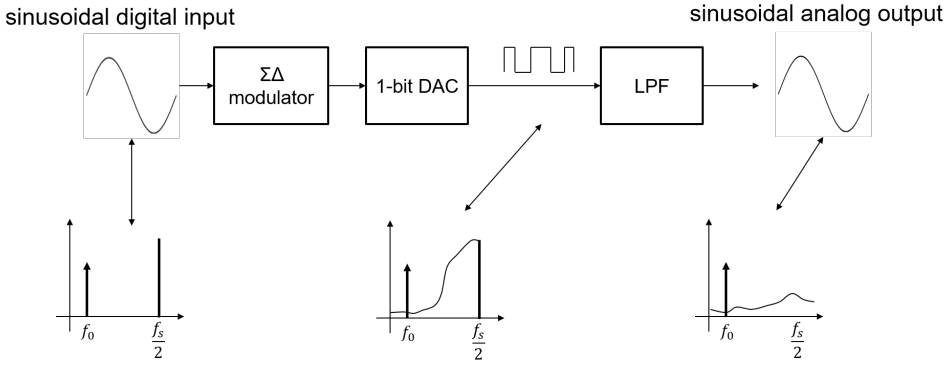


Figure 1.3: Block diagram of the signal generator using ΣΔ modulation

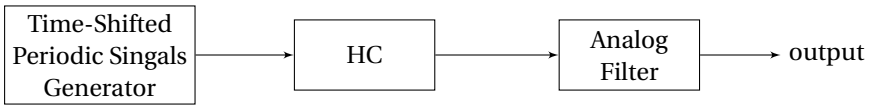


Figure 1.4: Block diagram of HC based sine-wave generator

[1, 6–8]. It uses a group of time-shifted signals to cancel certain harmonics. Its block diagram is shown in Figure 1.4, including a time-shifted periodic signals generator, HC block and an analog filter. This work also employs HC, and its theory will be presented in the next chapter in detail. The use of differential signaling naturally suppresses even-order harmonics, while HC can be used to handle odd harmonics. Unfortunately, only a limited number of odd harmonics can be cancelled at a time, with the exact number depending on the complexity of the cancellation circuitry. Furthermore, HC is highly dependent on mismatch and process variations, which limits the cancellation performance and results in a poor THD. Since the input of the HC block can be any periodic signal, square waves are often used, thus turning the task of periodic signal generation into digital pattern generation. In that case, HC block works just like a DAC, converting digital square waves into analog signals, and so the whole system fits into the topology demonstrated in Figure 1.1b. In the frequency domain, HC cancels the harmonics close to the fundamental, and an analog filter is still needed to remove higher-order harmonics.

In [1] a generator based on HC was proposed. It includes a built-in ring oscillator to generate a master clock. Then, a counter and a digital time shifter are used to generate time-shifted square waves, which are fed to a resistor summing network, and then smoothed by an analog filter . The main limitations are the phase mismatch between the time-shifted square waves and the resistor mismatch in the summing network, which contribute phase errors and amplitude errors, respectively. It achieves a state-of-the-art performance of -72dBc THD at 10MHz. However, the use of a third-order LPF greatly increased its complexity.

Based on this topology, an optimization method to reduce phase error is proposed in [7]. Such post-fabrication calibration improves the THD by approximately 20dBc at high

Table 1.1: State-Of-The-Art Sinewave Synthesizer

	[1]	[7]	[11]	[10]	[5]
Circuit type	HC	HC	SC+HC	ΣΔ modulation	ΣΔ modulation
SFDR*/THD (dBc)	72	70*/62.6	77	86*/84	60
Frequency	10MHz	750 MHz	62.5 kHz	5 kHz	0.8333 kHz
Power (mW)	3.34	9.1 – 57.2	3.24	NA	NA
Process (nm)	130	180	180	FPGA	180
Supply (V)	1.2	1.0 1.8	1.8	NA	1.8
Area (mm^2)	0.186	0.08	0.04	NA	0.068
Filter type	Third-order LPF	First-order LPF	Second-order SC LPF	Sixth-order LPF	Third-order LPF
Summing network	Resistor network	Resistor network	SC	NA	NA
Clock type	Multiphase	Multiphase	Conditional clock	NA	NA

frequencies and approximately 10dBc at low frequencies. It achieved a 62.6dBc THD at 750MHz. [8] also includes a post-fabrication calibration designed to reduce amplitude error. It works better for low-frequency applications as the amplitude error dominates in such situations.

In summary, all the works described above cannot achieve a decent THD without the use of calibration or a high-order filter, thus increasing the complexity of the system. This work proposes a sine-wave generator based on two-stage HC, which is implemented with resistors and switches, achieving an excellent THD performance while maintaining simplicity.

1.3. TARGET SINEWAVE GENERATOR

The main goal of this work is to design a low cost on-chip sine-wave generator with state-of-the-art THD (-80dBc) and low complexity. It should not require any additional post-fabrication calibration or a high-order LPF. To do this, low-order harmonics need to be attenuated enough to relax the required filtering, so a second-stage of HC was introduced. This only requires a few resistors and switches and is insensitive to mismatch and process variations. It thus does not require any post-fabrication calibration, keeping the whole system simple but with high performance.

1.4. ORGANIZATION OF THE THESISS

This thesis starts by discussing the principle of HC and its use state-of-the-art implementations in Chapter 2. The system-level design of the proposed sine-wave generator is presented in Chapter 3, and its circuit-level implementation is described in Chapter 4. Simulation and measurement results are described in Chapter 5 and last, but not least, a summary and a proposal for future work are presented in Chapter 6.

2

THEORY AND BACKGOUND

This chapter presents the theory of harmonic cancellation (HC), a popular linearization technique extensively used by recently proposed signal generators. Those works employ either switched-capacitor (SC) circuitry [11, 12] or a resistor network [1, 7, 8] to achieve low THD signal generation. Typical generators based on these two structures and their pros and cons are also discussed.

2.1. PRINCIPLE OF HARMONIC CANCELLATION

HC is a commonly used signal processing technique to improve the linearity of the signal. For instance, employing a differential input stage can greatly help to reduce the even harmonics [11]. The same principle can also be applied to cancel odd harmonics such as the third and fifth harmonics. The basic working principle of HC will be presented in this chapter.

Equation 2.1 presents a generic periodic signal.

$$x_0(t) = \sum_{k=1}^{\infty} A_k cos(k\omega_0 t + \varphi_k) \tag{2.1}$$

Where A_k and φ_k are the amplitude and phase of the k-th harmonic respectively, and where ω_0 is the fundamental frequency.

If two time-shifted signals are added together, the resulting signal has the same harmonic components but is modulated by coefficients determined by the delay time, as demonstrated in Equation 2.2. To keep the symmetry of the produced signal, two signals with the same time shift, but opposite directions, are added.

$$x(t+\Delta t) + x(t-\Delta t) = \sum_{k=1}^{\infty} 2A_k cos(k\omega_0 \Delta t) cos(k\omega_0 t + \varphi_k) \tag{2.2}$$

It reveals that the result is the original signal modulated by the coefficient $2cos(k\omega_0\Delta t)$. If $2cos(k\omega_0\Delta t) = 0$ is valid for a given k, the k-th harmonic will disappear, thus realizing the so-called HC. To cancel more harmonics, further time-shifted signals are added and each harmonic is multiplied by a coefficient calculated via the following equation:

$$\sum_{i=1}^{N} 2cos(k\omega_0 \Delta t_i) \tag{2.3}$$

Where N is the number of time-shifted signals. To cancel the third harmonic for instance, the following equation, which is derived from Equation 2.3 as N equals to 1 and k equals to 3, needs to be solved:

$$\begin{aligned} 2cos(3\omega_0\Delta t) &= 0 \\ \Delta t &= \frac{2n+1}{12} T \end{aligned} \tag{2.4}$$

Where T is the period of the signal. As shown in Figure 2.1, two square waves are added with $\frac{T}{6}$ time shift. The resulted signal, which is a step-wise sine-wave, is free of third harmonic. The number of time-shifted signals is determined by how many harmonics the user wants to cancel. Addressing two harmonics simultaneously – for example, the

third and fifth harmonics – requires N equals to 2 and solving simultaneous equations.

$$\begin{cases} 2cos(3\omega_0\Delta t_1) + 2cos(3\omega_0\Delta t_2) = 0 \\ 2cos(5\omega_0\Delta t_1) + 2cos(5\omega_0\Delta t_2) = 0 \end{cases} \tag{2.5}$$

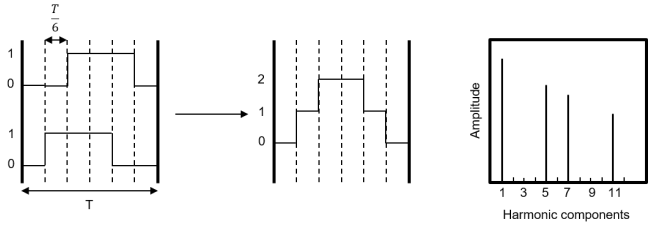


Figure 2.1: Added square waves with $\frac{T}{6}$ time shift results in third harmonic cancellation

However, different time delays are difficult to implement in the circuit. A delay circuit either requires a high frequency clock [13], or has limited accuracy and working range [14]. Thus instead of customizing delay times, extra amplitude coefficients are introduced. In that case, all the signals have the same time shift but are modulated by different gain coefficients, which transforms the selection of delay time into selection of gain coefficients. When each signal is multiplied by a_i and the delay between signals is fixed to Δt, the coefficient becomes:

$$\sum_{i=1}^{N} 2a_i cos(k\omega_0 i\Delta t) \tag{2.6}$$

Adding a group of fixed time-shifted signals, which are multiplied by accurately calcu-

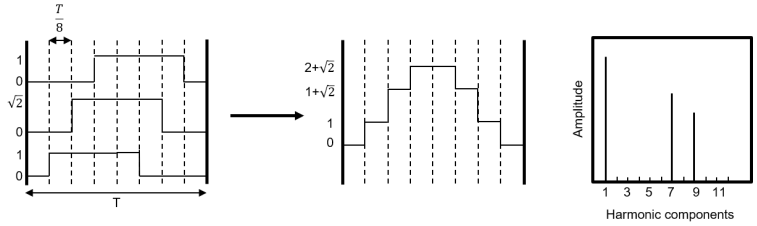


Figure 2.2: Added square waves with $\frac{T}{8}$ time shift and amplitude modification results in third and fifth harmonic cancellation

lated coefficients $a_1, a_2 \ldots\ldots a_i$, cancels the desired harmonics. If only one harmonic is required to be cancelled ,as the case shown in Figure 2.1, there is no need to introduce amplitude coefficients, since only one delay time is needed. However, when more than one harmonic is required to be cancelled and delay time is fixed, amplitude coefficients are introduced. As shown in Figure 2.2, Three square waves are added with $\frac{T}{8}$ time shift and the second square wave is amplified by $\sqrt{2}$, making the third and fifth harmonic equal to 0.

2.2. SC-BASED IMPLEMENTATION

The foundation of a SC circuit is its ability to store and transfer charges. For low THD sine-wave generation, two approaches are possible. In one case, a SC circuit works as a filter to attenuate the harmonics. A SC filter is implemented by replacing an analog filter's resistors with SCs. Another method employs SCs to achieve HC.

2.2.1. SC FILTER

Theoretically, a SC filter is the same as an active analog filter, except switches and capacitors take the place of resistors. It has the same requirements as its analog counterpart. To filter out harmonics close to the fundamental, a high-order filter is needed to achieve high selectivity. For a square wave input, the third harmonic is approximately 9.5dB below the fundamental. A seventh-order Butterworth LPF has about 67dB attenuation at 3 times the cutoff frequency and is able to achieve a THD below -70dBc. For such a high-order active filter, many amplifiers and large resistors and capacitors are needed, resulting in a complicated circuit design and a large silicon area.

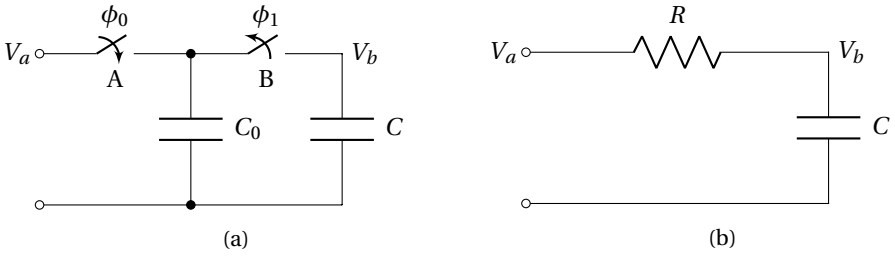


Figure 2.3: (a) An SC filter and (b) an RC filter

SC filters solve the problem caused by large resistors and capacitors. Figure 2.3a demonstrates an SC filter, whose analog counterpart is a simple RC filter (Figure 2.3b). Equation 2.7 illustrates the cutoff frequency of the SC filter [15].

$$f_{cut-off} = \frac{f_{clk} C_0}{2\pi C} \tag{2.7}$$

It reveals that only the capacitor ratio matters. In that case, SC filter has better accuracy and its cutoff frequency can be changed by tuning the clock frequency, making it versatile and much more attractive than the active filter.

Unfortunately, SC filters still have weak points compared to active filters. Its output is a filtered and sampled version of its input, so it is discontinuous. In the frequency domain, such discontinuity results in harmonics at clock frequency, so that an analog filter is needed to smooth the output.

In addition, SC filters suffer from the charge injection and clock feedthrough when a single MOSFET is used as the switch. When transistor B in Figure 2.3a is turned off, a portion of the charges in its channel flow to C and change the stored charges. Conventional solutions for these problems include CMOS switches and a dummy transistor. However, none of these methods solve the problems completely [16].

Moreover, SC filters still suffer from problems because of the need of opamps. The opmap's headroom and linearity limit the swing and distortion of the final output. A high-order filter needs multiple opamps, which consume significant silicon area and raise the hurdle of design, making the whole system quite complicated. An SC filter is better than traditional analog filters, but is not particularly outstanding.

2.2.2. SC-BASED HARMONIC CANCELLATION

As mentioned above, based on the property of charge transfer, a SC circuit can also be configured for HC. All HC needs are delays, weighted coefficients and an adder. The topology of the SC FIR filter can be used, since a FIR filter likewise consists of these three parts. The difference is that the coefficients are calculated by the equations 2.6, instead of calculating via a FIR filter design method.

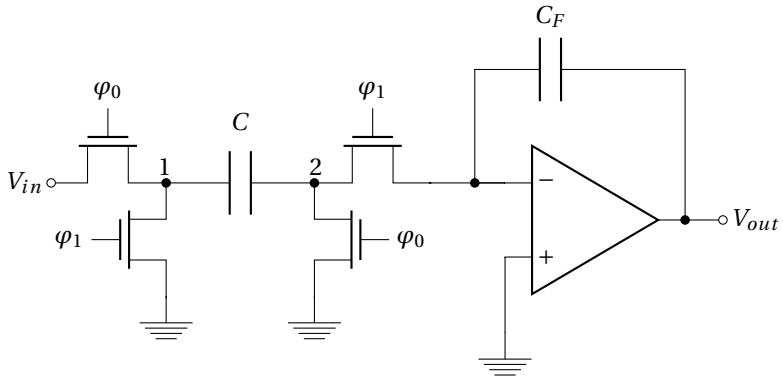


Figure 2.4: A SC delay cell

The most important and challenging part is the delay cell. in [13, 17], multiple SC-based delay cells were employed. They are all based on the structure elaborated in Figure 2.4. During ϕ_0, the input signal is sampled on the capacitor C. During ϕ_1, charges on C are transfered to C_F. In this case, the output is delayed for $\frac{T_{clk}}{2}$. To generate a group of time-shifted signals, a number of such structures are connected in series, requiring lots of amplifiers, thus increasing the power consumption and chip area.

A more power and area efficient approach is to employ a multi-phase clock, as proposed in [18]. The sum of (N-1) time-shifted signals with delay time $\frac{T_{clk}}{N}$ can be realized with one amplifier employing an N-phase clock. Multiplication of the charge can also be merged into the same stage as demonstrated in Figure 2.5.

During phase 1, the input signal is sampled on C_0. The charges on C_1, C_{21} and C_{31} are transferred to C_{11}, generating the output voltage. At that point, C_1, C_{21} and C_{31} are discharged and ready for the signal in next clock phase. In phase 2, C_2 transfers its charges to C_1. In phase 3, the charges on C_3 are transferred to C_2 and copied on C_{21}. Finally, in phase 4, the charges on C_0 are transferred to C_3 and replicated on C_{31}. At this stage, C_0 is fully discharged and ready for a new signal in the next clock period. Assuming an ideal

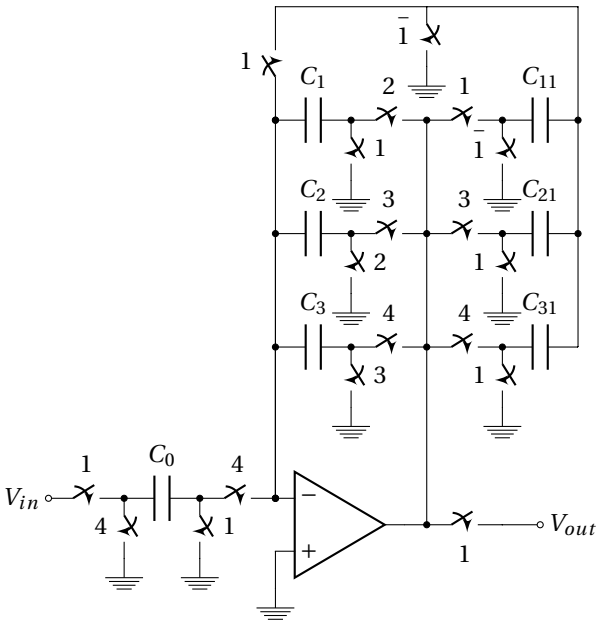


Figure 2.5: Harmonic cancellation based on a SC based 3-stage delay line

opamp, the transfer function is:

$$H(z) = \frac{C_0}{C_{11}}\left(\frac{C_{31}}{C_3}z^{-1} + \frac{C_{21}}{C_2}z^{-2} + z^{-3}\right) \tag{2.8}$$

The coefficient of each delayed component is determined by different capacitors, making it simple to independently set the coefficients by scaling capacitors C_{11}, C_{21} and C_{31}. All the other capacitors are scaled to the same value to achieve the maximum signal swing [19]. Compared to a conventional SC filter, such SC-based HC needs significantly fewer amplifiers. The circuits depicted in Figure 2.5 can be readily modified to a higher order circuit by adding more feedback paths and employing a clock with the corresponding number of phases.

However, as the number of phases increases, other problems emerge. The capacitor spread becomes larger as more capacitors with different values are added. In addition, the amplifier settling requirement also becomes stricter as the clock pulse width decreases. Furthermore, SC-based HC does not solve all the problems of an SC filter. It still suffers from the charge injection and clock feed-through and is still limited by the amplifiers' linearity.

Apart from the linearity and settling time of the amplifier, its finite gain also affects the accuracy of the SC circuitry. We assume an ideal opamp in Equation 2.8, where all the charges are transferred completely in every step with the help of an ideal virtual ground. However, such an ideal opamp does not exist and a real opamp has a finite gain. To minimize the influence due to finite gain, an amplifier with a gain more than 10000 [18] is needed to reduce the charge inaccuracy, which complicates the design.

2.2.3. SC FILTER WITH BUILT-IN HC

As discussed above, both SC filters and SC-based HC have their own merits and demerits. [11] proposed an architecture combining both of them. The author added a summing stage at the input of the SC filter, as demonstrated in Figure 2.6, to integrate HC into a regular SC filter.

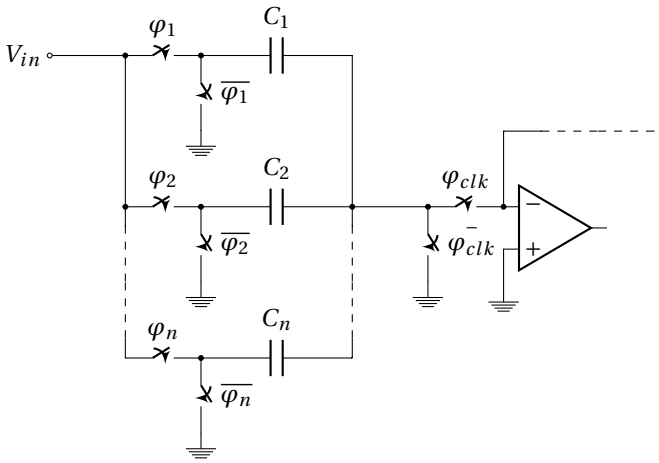


Figure 2.6: SC filter merged with harmonic cancellation

Integrating a summer into the SC filter's input stage means that no additional amplifier is needed, since the amplifier forming the SC filter's input stage is shared with the HC. An added HC summer releases the requirement for the SC filter, as low-frequency harmonics are attenuated by the summer, and the SC filter only needs to focus on the higher-order components. As a result, the added HC stage reduces the order of the SC filter and thus lowers the number of amplifiers needed. However, the summer needs complex control signals. Generating these signals (φ_1, φ_2, $\cdots$, φ_n) may require additional logic circuits. In addition, the summer also suffers from transistor non-ideality (e.g., charge injection and clock feed-through) and capacitor mismatches, which causes incomplete harmonic cancellation. Furthermore, the linearity and headroom of the amplifier limit the distortion and swing range of the final output as always.

2.3. RESISTOR NETWORK BASED IMPLEMENTATION

Another approach that more recent reports have commonly used for low THD signal generation is a HC-based resistor summing network. The basic idea is to transform a group of time-shifted signals into current form so that they can be easily scaled and added.

Figure 2.7 contains a conceptual block diagram of the resistor summing network based HC. The whole system consists of a phase-shifted signal generator, buffers and a resistor summing network. As mentioned above, any periodic signal can serve as the HC's input. As the most digital-friendly option, a square wave is easy to generate and digitally tune, which explains why it is typically chosen as the HC's input in most works

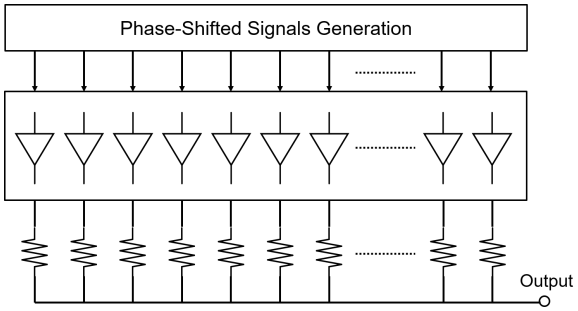


Figure 2.7: Block diagram of HC based on resistor summing network

[1, 7, 8, 11]. A buffer is usually needed to isolate the signal generation stage from the resistor network. That is because the commonly used periodic signal generators, such as a ring oscillator and a shift register, cannot connect directly to the resistor network.

2.3.1. PHASE-SHIFTED SIGNAL GENERATION

The ring oscillator [1, 7] and the shift register [8] are two popular square wave generators. A ring oscillator does not need an external clock, making the whole system independent and entirely on-chip, while a shift register needs a high-frequency input clock but can be digitally controlled.

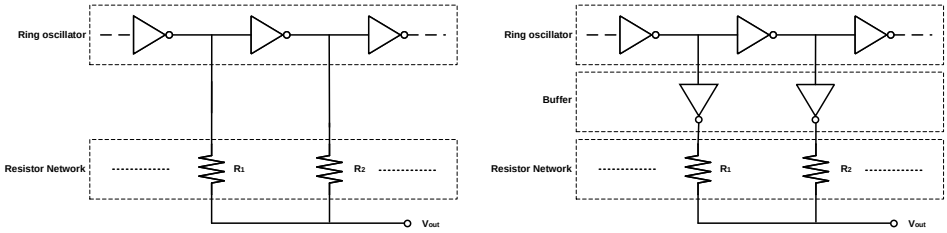
The ring oscillator is highly suitable for HC, thanks to its time delay characteristic providing multiple parallel outputs. The frequency of the generated signals can be tuned by changing either the supply voltage and current or the load capacitors. Due to process voltage temperature (PVT) variation, the generated square waves suffer from phase and duty-cycle mismatches.

A simple circular shift-register can also generate a group of time-shifted square waves. An equal number of consecutive logic 1s and 0s produces a 50% duty-cycle square wave, and the duty-cycle can be modified by changing the number of logic 1s and 0s. The time shift between each square wave is determined by the clock period, and the total number of flip-flops is calculated according to the desired output frequency and clock frequency. Assuming the clock frequency is f_{clk} and the number of flip-flops is N, the output square wave frequency is Nf_{clk}, which is also the frequency of the final sine-wave.

2.3.2. BUFFER

A buffer is needed to isolated the time-shifted generator from the resistor network. As the time-shifted signal generator, a ring oscillator relies on the charging time at every node to determine the output frequency. If each node is connected directly to the resistor network, as demonstrated in Figure 2.8a, the charging time varies. This is because the network's resistors are added to the load resistance of the ring oscillator, and the network's resistors are different, thereby causing the load difference at each node of the ring oscillator. To avoid such situation, each node must be isolated from the resistor network to guarantee the accuracy of the output frequency. Simple inverters, as depicted in Figure 2.8b, separate the ring oscillator from the resistor network and provide identical load

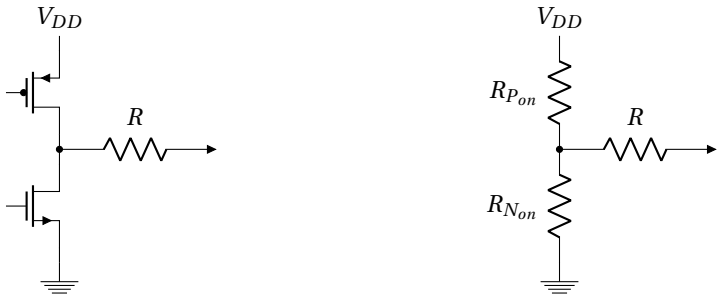
conditions for each node of the ring oscillator.



(a) (b)

Figure 2.8: Ring Oscillator (a) connecting directly to resistor network and (b) buffered by an inverter

Unfortunately, such an inverter buffer is not harmless. It introduces both phase and amplitude errors to the system. The NMOS and PMOS used in inverters have different threshold voltages, resulting in different rising and falling times and causing duty-cycle errors. Furthermore, NMOS and PMOS also have different on-resistances. As Figure 2.9 indicates, when the PMOS is conducting, its on-resistance is added to the resistor network, while the NMOS adds its on-resistance to the resistor network when it is conducting. Since the PMOS and NMOS have different on-resistances, they also introduce amplitude errors into the resistor network.



(a) (b)

Figure 2.9: (a) inverter followed by resistor (b) equivalent PMOS and NMOS on resistance introduced resistance error

[7] proposed to drive the PMOS and NMOS separately with a pair of phase-shifted signals. In that approach, the duty-cycle issue due to the uncontrollable threshold voltage is addressed, as it can be controlled by tuning the phase shift of the control signal pair. Besides, the author also added a cross-coupled inverter pair to reduce the impact of the on-resistance difference.

2.3.3. RESISTOR NETWORK

To reduce the resistor mismatch in the network, the size of all the resistors should be relatively large. Several strategies can further reduce the mismatch. As components with

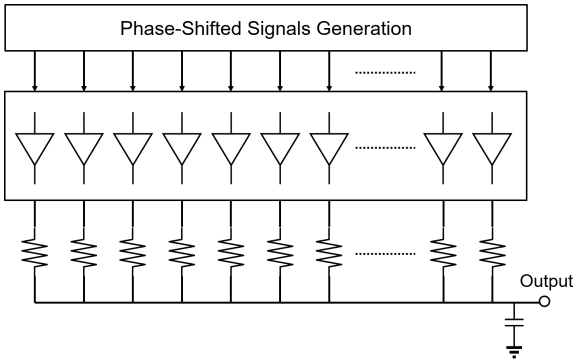


Figure 2.10: HC based on resistor summing network loaded by capacitor

same value match more closely, [7] used two 2R resistors in parallel to replace a R resistor, thereby reducing the number of different resistors. However, this approach only works for a network with a small number of resistors, limiting the number of cancelled harmonic. In addition, a well-organized and symmetric resistor matrix, as provided in [1], can also assist with the matching issue from layout perspective.

A small modification is integrated into the resistor network to form a simple and elegant filter, as demonstrated in in Figure 2.10. With a load capacitor, a simple RC filter is implemented.

2.3.4. OPTIMIZATION TECHNIQUES

As discussed in Chapter 2.1, HC is highly dependent on the input signals matching each other. A signal mismatch can take the form of either a phase error or an amplitude error, and their primary contributors are the phase-shifted signal generator and the resistor network respectively. Both of these two parts are sensitive to process variation. Consequently, post-fabrication calibration techniques are integrated into these two blocks to address the issue.

[7] proposed using a digitally-controlled phase shifter to individually tune the edges of each square wave (Figure 2.11). The phase shifter consists of binary-weighted MOS varactors triggered by external control signals. By changing the load capacitance at each node, the phase is modulated to a certain extent. Such a phase shifter provides a 20ps tuning range and requires external control signals and an optimization algorithm. This approach works well for high-frequency signal generation due to the limited phase tuning range. Additional and larger varactors are needed for lower frequency applications. Fixed varactors don't have sufficient tuning range for different output frequencies.

A similar calibration method can also be employed in the resistor network. [8] added several calibration resistor segments to the main resistors, as elaborated in Figure 2.12. Switches serve to connect or disconnect these calibration resistors and the main resistors. First, switch S_{cal} is turned on, and the output voltage V_{cal} is measured. Then, the measured voltage drop across R_{main} is compared to the ideal value and the difference is identified. Finally, proper digital control words are applied to choose the needed calibration resistors, achieving a better resistor match.

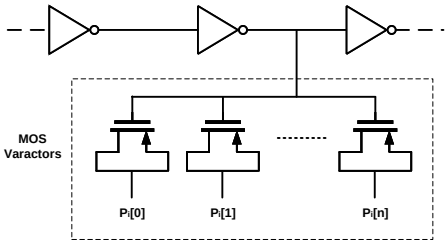


Figure 2.11: A phase shifter consists of MOS varactors

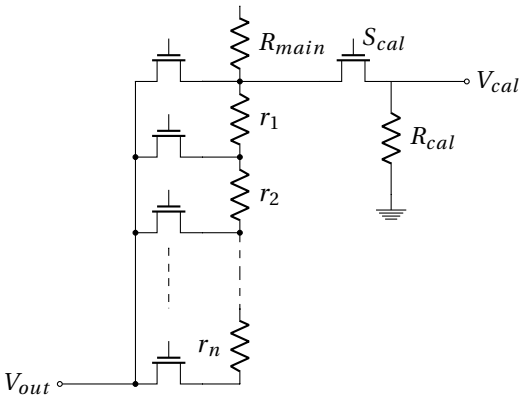


Figure 2.12: Post-fabrication resistor calibration

In summary, the resistor summing network based HC keeps the circuit simple and releases analog filter's requirement. However, to achieve a decent THD, post-calibration is required, complicate the design and test process. Based on the resistor structure, this work will propose a 2-stage HC to make the signal distortion insensitive to mismatches and process variations, so that achieve an excellent THD while keeping the whole system and design process simple.

3

Proposed Sinewave Generator based on Resistor Ladder with Comb Filter

The previous chapter discussed state-of-the-art, low THD sine-wave generation approaches, most of which are based on harmonic cancellation (HC). The main limitations of the effectiveness of HC are component mismatch and process variation. Thus, a two-stage HC approach, which is much less sensitive to these effects, is proposed and discussed in this chapter.

3.1. CONCEPT OVERVIEW

The HC implementation discussed in the previous chapter is highly dependent on resistor or capacitor ratios. To deal with more harmonics, more components with different values are required, with larger resistance or capacitance spread as a result. On the other hand, if only one harmonic is targeted, two time-shifted signals with identical amplitudes are sufficient. In this case, the signals are scaled by components with the same value. That method should yield an excellent cancellation, since identical components should be better matched.

Based on this observation, a two-stage HC is proposed. Figure 3.1, in which blocks HC1 and HC2 are combinations of a buffer and a summing network, illustrate this principle. HC1 and HC2 implement a first-stage HC, they are the same structures shown in Figure 2.7 except for a shared, phase-shifted signal generation block. By feeding phased-shifted signals to HC1 and HC2, the resulting outputs V_1 and V_2 will have identical amplitude but different phases. Then, V_1 and V_2 are added in the next stage, forming the second-stage HC, to further attenuate the specific harmonics.

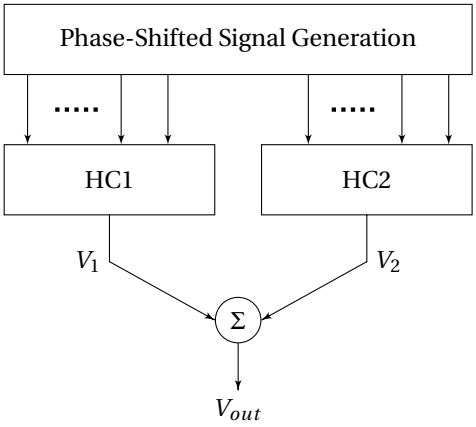


Figure 3.1: Block diagram of 2-stage harmonic cancellation

The amplitude of certain harmonics in the output signals V_1 and V_2 generated by the first-stage HC has been attenuated. Unfortunately, due to the non-ideality of the first-stage HC, these attenuation may not be sufficient. In particular, the most significant harmonic residue is in the frequency range adjacent to the fundamental frequency, where the subsequent analog filter has the least attenuation. Therefore, the second-stage HC serves to further reduce the closest harmonic components (e.g., the 3rd one). The coefficients of the summing network are the same for HC1 and HC2, which should result in

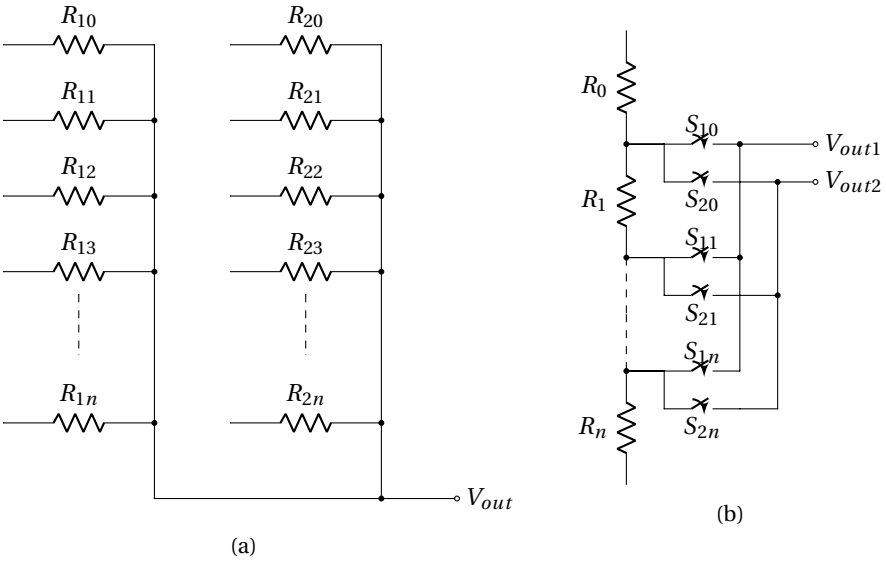


Figure 3.2: 2-stage HC implemented with (a) parallel resistor network and (b) resistor ladder and switch arrays

a closer matching.

To further increase the matching of V_1 and V_2, it is preferred to use a single group of resistors to generate two time-shifted signals. For that purpose, the parallel resistor network (Figure 3.2a) is converted to a series resistor network (Figure 3.2b), thus forming a resistor ladder. The values of the resistors are calculated by calculating the amplitude of an ideal sine-wave at the appropriate time instant, while the output amplitude is determined by the biasing voltages at the two ends of the ladder. By adding a group of switches that can connect a single output node, e.g. V_{out1} to any node of the ladder, stepwise sine-waves can be generated at the output. The main advantage of such a ladder structure is that by adding a second group of switches, another stepwise sine-wave (V_{out2} in Figure 3.2b) can be generated. These two signals come from the same ladder, so they should be completely identical. When the two groups of switches are driven by two shifted control sequences, V_{out1} and V_{out2} will also be time-shifted.The time shift between V_{out1} and V_{out2} is determined by the control sequences driving these switches and so is a multiple of the clock period.

3.2. STEPS CALCULATION FOR DESIGNED HARMONICS CANCELLATION

To realize the second-stage HC, the clock period and number of steps need to be carefully chosen. According to Equation 2.3, if one signal is to be canceled, only two time-shifted signals are required. This particular case is the same as a one-tap FIR filter, also known as a comb filter, since its frequency response has a comb shape.

Figure 3.3 depicts a feedforward comb filter; its frequency response is given by the

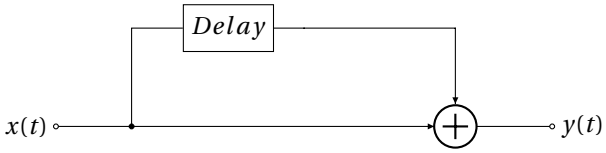


Figure 3.3: Block diagram of comb filter

following equation:

$$H(e^{j\omega}) = 1 + cos\omega\Delta t - jsin\omega\Delta t \tag{3.1}$$

Where Δt is the fixed delay. This calculation is compatible to Equation 2.3 when N=1. As shown in Figure 3.4, at $\omega = \frac{(2n+1)\pi}{\Delta t}$, the gain is equal to 0, which cancels the signal at those frequencies. To cancel the third harmonic, the delay time can be calculated as follows:

$$\Delta t = \frac{(2n+1)\pi}{3\omega_0} = \frac{(2n+1)\pi}{3\times 2\pi f_0} = \frac{(2n+1)}{6} T_0 \tag{3.2}$$

Note that the time shift here is two times the time shift in Equation 2.2, and so the results from Equation 2.4 and Equation 3.2 are the same. Since the time shift needed for cancelling the third harmonic is $\Delta t_3 = \frac{T_0}{6}$, a stepwise sine wave with 6n (n=1,2,3...) steps is required.

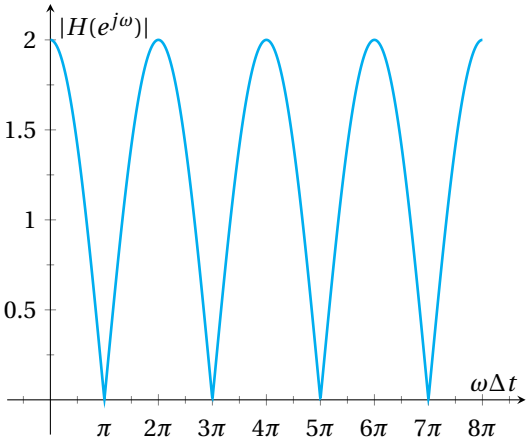


Figure 3.4: Comb filter frequency response

3.3. CASCADE COMB FILTER REALIZATION

A similar calculation can be made to determine the requirements of fifth harmonic cancellation, which requires a delay $\Delta t_5 = \frac{T_0}{10}$. To cancel both the third and fifth harmonics, the cancellation needs to be executed twice, resulting in a cascade two-stage comb filter,

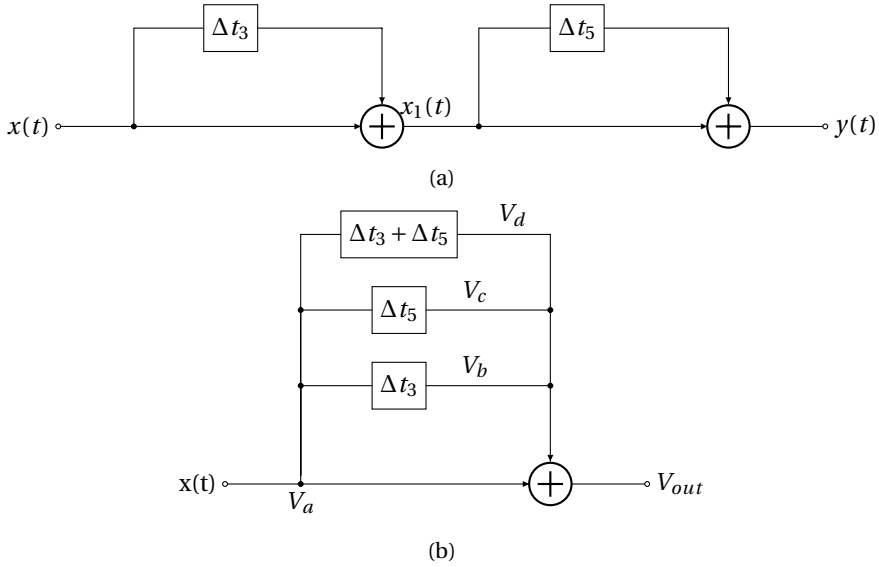


Figure 3.5: The second-order comb filter in (a) cascade and (b) parallel

as shown in Figure 3.5a. However, such a structure needs an extra delay stage to provide Δt_5 delay. As shown in Figure 3.6, $x_2(t)$, a delay version of $x_1(t)$, is required. To avoid the use of extra delay cell and realize the delay with only ladder and switches, the two-stage cascade configuration is converted into a one-stage parallel architecture as shown in Figure 3.5b. As demonstrated in Figure 3.7, V_a and V_b have a Δt_3 time shift and their sum will be $x_1(t)$. V_c and V_d have a Δt_3 time shift and their sum will be $x_2(t)$. Since the delay of V_a and V_c and the delay of V_b and V_d are both Δt_5, $x_1(t)$ and $x_2(t)$ will have a Δt_5 time shift. As a result, the sum of these four signals, V_{out}, is free of the third and fifth harmonics. This delay arrangement is also one solution for Equation 2.5.

To implement both Δt_3 and Δt_5 with switches, the step duration (t in Fig. 3.8) should be a common divisor of them. When that is the case, Δt_3 and Δt_5 can be represented as n steps (n=1,2,3...). According to Equation 3.2, $\Delta t_3 = \frac{T_0}{6}$ and $\Delta t_5 = \frac{T_0}{10}$. As $t = \frac{T_0}{N}$, N must be a common multiple of 6 and 10, and the minimum value for N is 30. When $N = 30$, Δt_3 equals 5t and Δt_5 equals 3t. In this case, there are four signals generated from one ladder, and the time shifted between them is either three steps or five steps. By combining them, the third and fifth harmonics are cancelled.

3.4. PARASITIC CAPACITORS

The proposed HC approach, like all the others, is highly dependent on the signals matching. Since these four signals are from the same resistor ladder, their step voltages should be completely identical. However, at every switching point, the output jumps from one voltage level to another. During this transition phase, every output affects each other, resulting in mismatch.

Figure 3.9 highlights the simulation result for two signals from one ladder. Every

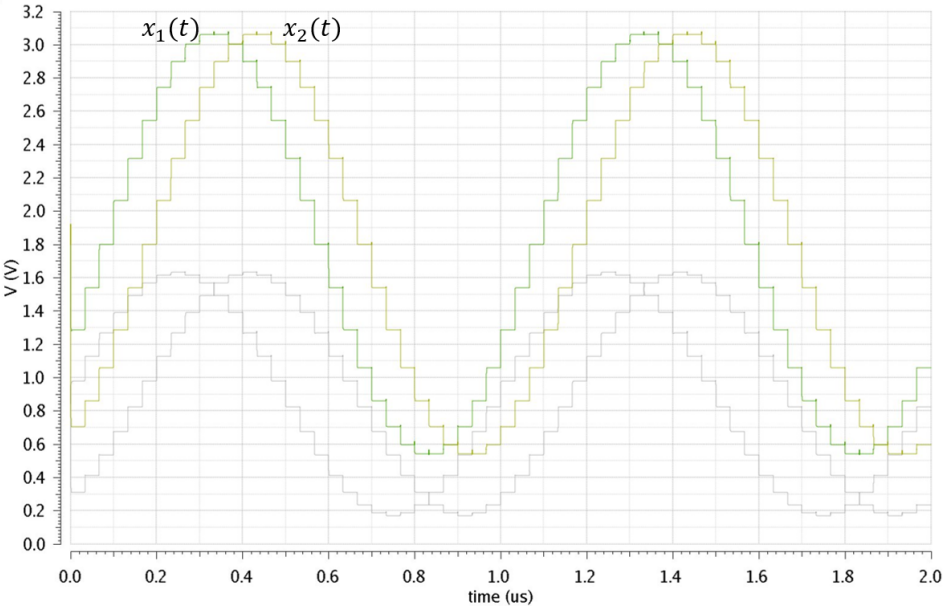


Figure 3.6: Time domain signals of the second-order com filter in cascade

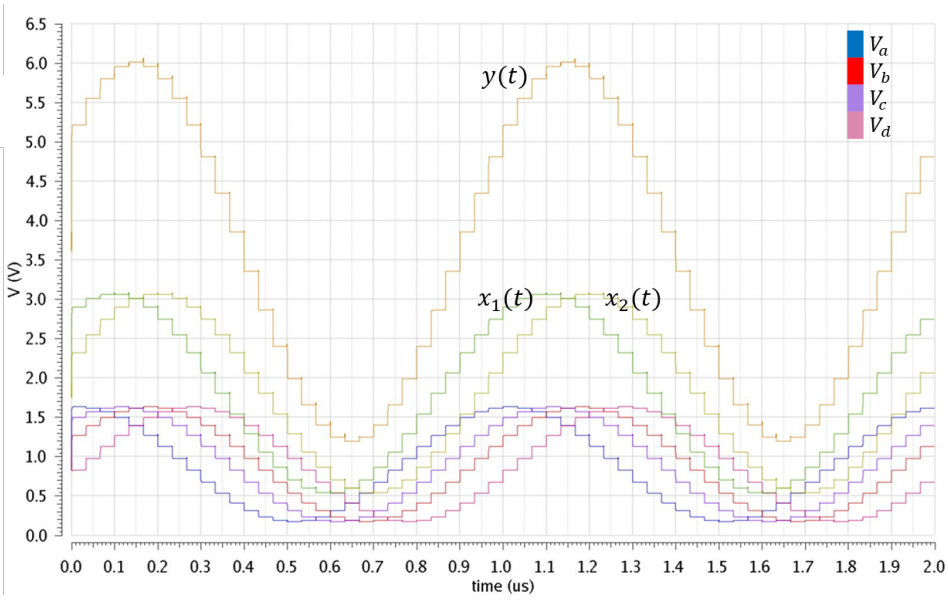


Figure 3.7: Time domain signals of the second-order com filter in parallel

settled voltage is perfectly matched. Unfortunately, the transition regions (where the signal jumps from one voltage level to another) are not, as shown in the circled part in

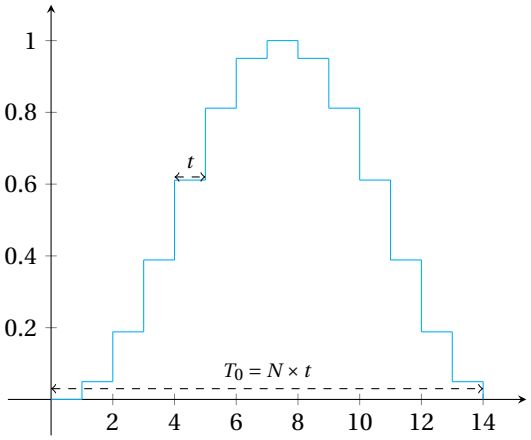


Figure 3.8: Stepwise sinewave

Figure 3.9, causing incomplete harmonic cancellation.

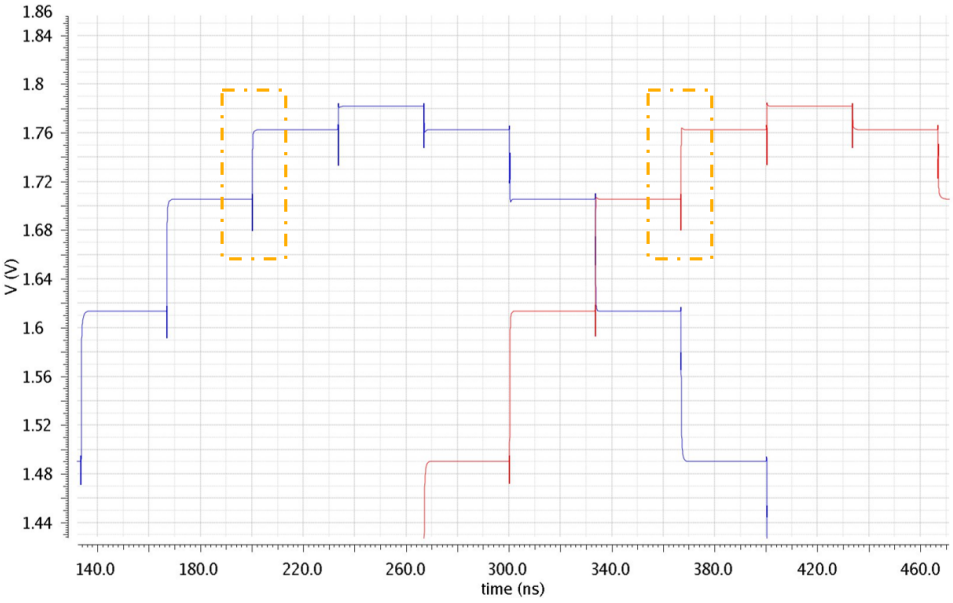


Figure 3.9: Transition region mismatch

This 'transition region mismatch' is due to the load capacitors. As outputs are loaded by capacitors, the output voltage cannot change instantly. At each switching moment, a current is needed to charge or discharge the load capacitor. Figure 3.10a shows a part of the ladder at the switching moment. At the moment that switch S_C opens and switch S_B closes, output disconnects from node C and connects to node B. However, the output

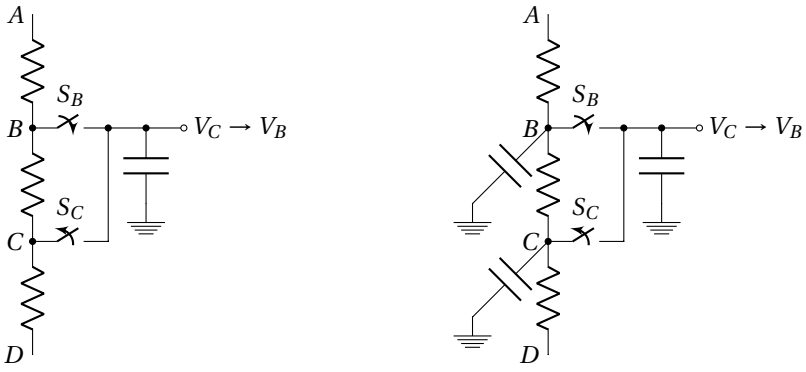


Figure 3.10: (a) Resistor ladder loaded by capacitor and (b) parasitics of resistors

voltage remains unchanged at this moment due to the load capacitor. As a result, the voltage at node B is pulled down by the output. Since the current moving through the resistor ladder does not change at this moment, the voltage at node A is also pulled down. As a result, all the voltages of the ladder will change at the switching moment. In the end, the voltage variation draws an extra current from the supply to charge the load capacitor until all the node voltages recover to their stable value.

Ideally, at the switching moment, the voltage at node B is pulled down to V_C, resulting in a large voltage variation, so that it can draw a large current from the supply to quickly charge the load capacitor. Unfortunately, the resistor ladder also suffers from parasitic capacitors. As Figure 3.10b reveals, the voltage at node B does not decline to V_C at the switching moment because of the parasitic capacitor at node B. Instead, the voltage at node B only varies slightly and can only draw a small current from the supply. Thus, more time is needed to charge the load capacitor to V_B. In other words, the transition time is determined by the ladder's parasitic capacitors and the output load capacitors. That is not a problem for low-frequency output, since the transition time is fixed and only comprises a small portion of each step. However, at high frequencies, the mismatch of the transition regions destroy the effectiveness of HC as the step duration declines.

One solution is to reduce the parasitic capacitors of the resistor ladder so that the transition time also decreases. This method requires resistors with smaller size to minimize parasitic capacitance. However, small resistors do not match as well, resulting in a trade-off between the output frequency and harmonic distortion.

3.5. BALANCING OF LADDER'S OUTPUTS

In addition to reducing the resistor size to minimize the transition time, there is a more effective way, which will be referred to as 'output balancing'. It does not matter what the transition region looks like or how long the transition takes as long as these two signals have the same transition regions. Mismatch is caused by multiple outputs affecting each other at the switching moment. As highlighted in the circled region in Figure 3.11, when

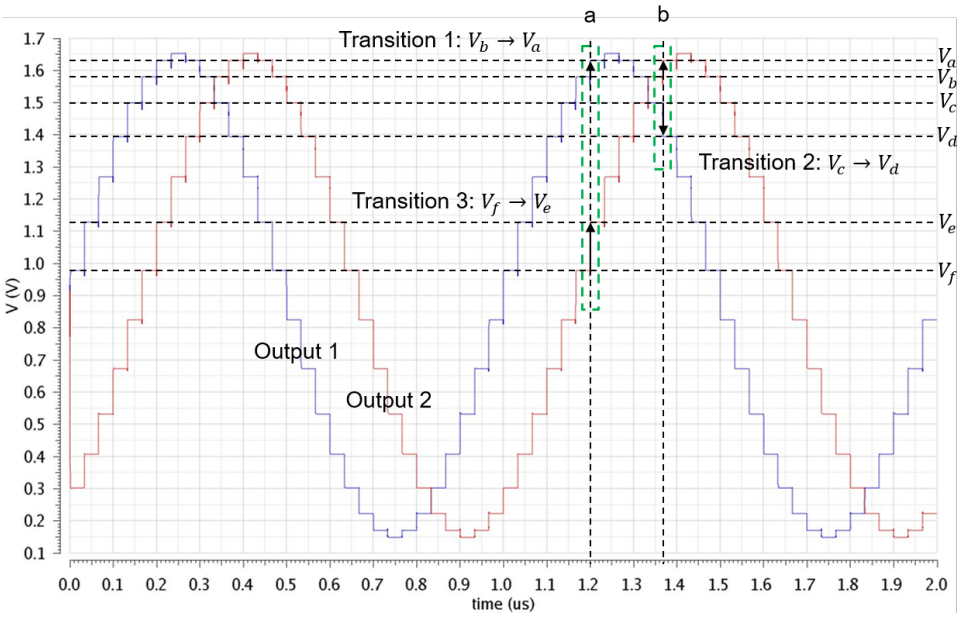


Figure 3.11: Different switching action causes transition region mismatch

output 1 transferring from V_b to V_a, output 2 jumps from V_f to V_e. When output 2 moves from V_b to V_a, output 1 jumps from V_c to V_d. Let's mark the three transition region as denoted in the Figure 3.11. Since transition 2 and transition 3 are different, their influences on the ladder's node voltage differ, making output 1 and output 2 have different transition 1.

To solve this problem, the ladder's experience has to be identical at time a and time b. Adding a transition 3 at time a and a transition 2 at time b can balance the output and ensure that they match. If these actions are performed for every step, the results are two extra outputs as demonstrated in Figure 3.12. Unfortunately, these two additional outputs also introduce another two unbalanced transition regions. Thus, more outputs are added until all of them are evenly spread across one signal period (Figure 3.13). Figure 3.14 shows the zoomed in signals and demonstrates noticeable improvement as compared to Figure 3.9.

The four extra outputs may at first seem to be useless. However, two of them are complementary versions of the original two outputs and so can be used to implement differential signals, and thus cancel even-order harmonics. So only two of the extra outputs are not used. Each extra output only requires a group of switches and a identical load, which consumes neither substantial power nor silicon area. The number of outputs is determined by the time-shift to signal-period ratio, which is essentially determined by which harmonic is to be cancelled. Figure 3.15 contains the simulated third harmonic distortion (HD3) versus the output frequency with and without output balancing. At low frequencies, their values are comparable, since the transition regions only comprise a

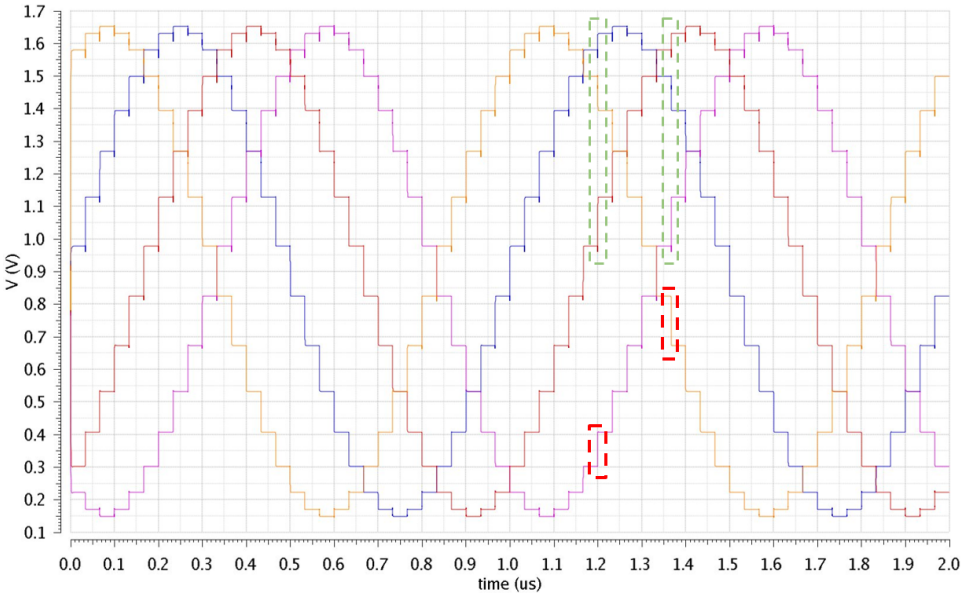


Figure 3.12: Half balanced by 2 additional outputs

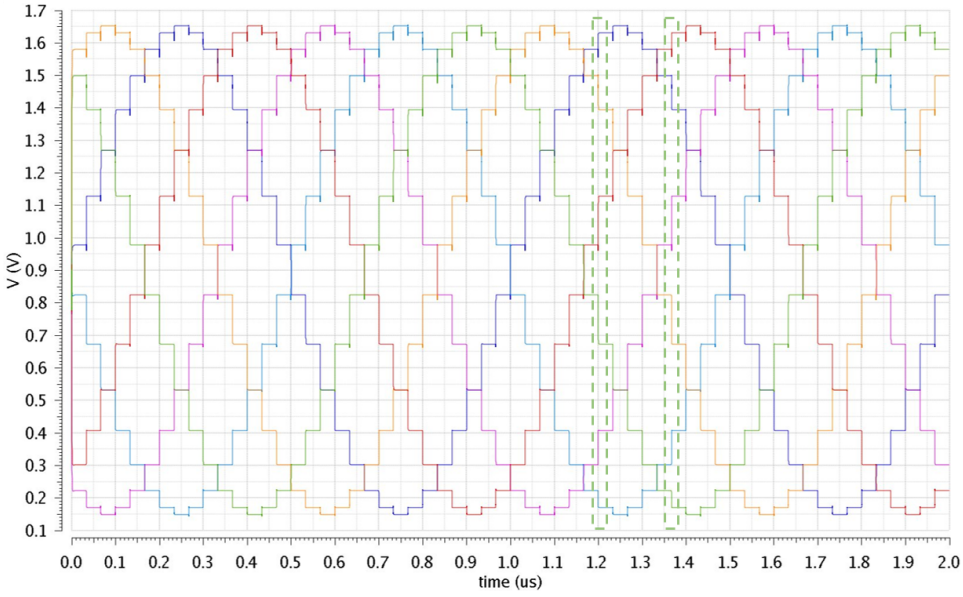


Figure 3.13: Fully balanced by 4 additional outputs

minimal portion of each step. However, at higher frequencies, transition region starts to pollute the signal matching and ruins the effectiveness of HC.

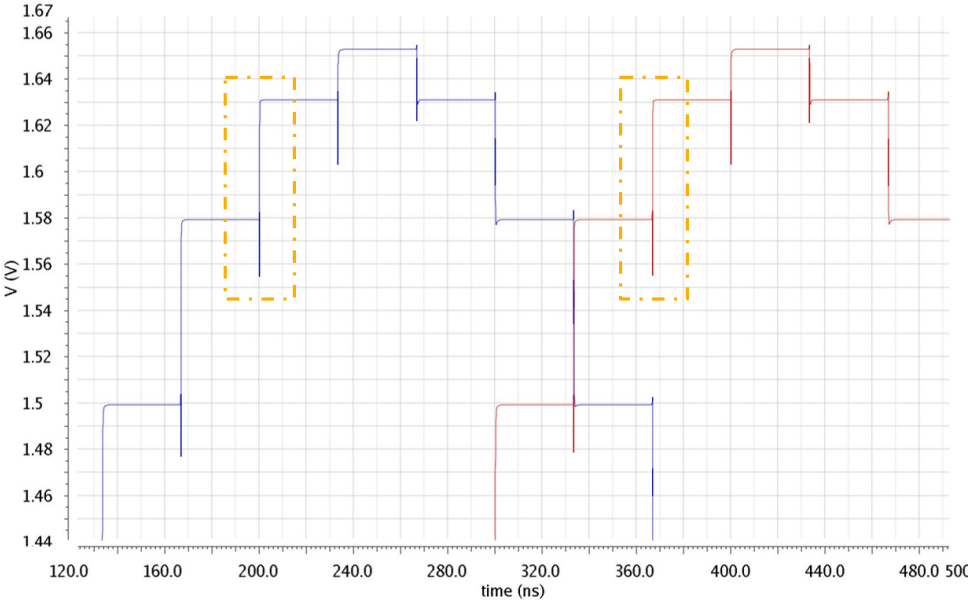


Figure 3.14: Zoom-in part of two outputs after balancing

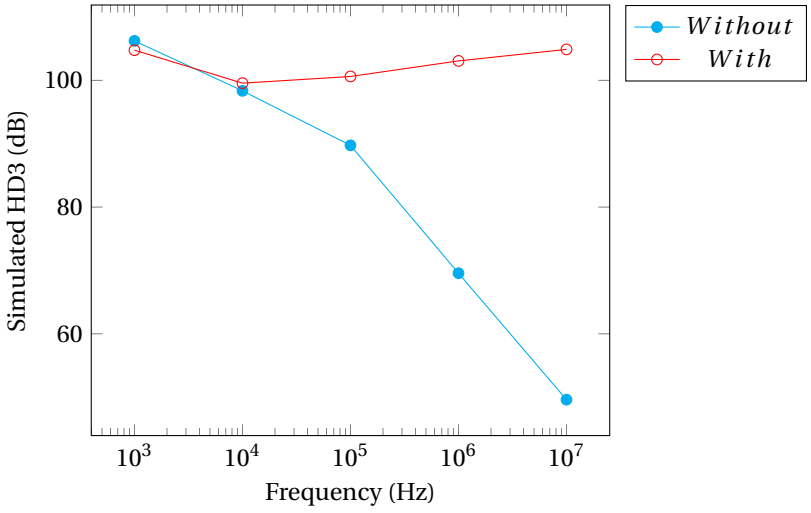


Figure 3.15: Simulated HD3 with and without output balancing

To cancel both the third and fifth harmonics, four time-shifted signals are needed. Unfortunately, the time shifts between these four signals will be different. They can only be balanced by signals with a one-step shift, which means that 30 outputs will have to be generated for our 30-step sine-wave – an excessively high number. Numerous out-

puts will be useless, and thus area and power are wasted. Another approach must be proposed to solve this problem.

As mentioned above, to cancel the 3rd harmonic, only 6 outputs are needed. If there are two signals, which are free of the third harmonic, come from different ladders, and have a 3-step time shift with each other, adding them should remove the fifth harmonic. As demonstrated in the Figure 3.16, the four signals are divided into two groups, and each group is balanced with other four signals. Thus, twelve outputs are needed in total, which is much less than 30 outputs. Of course, as the two signals now come from two ladders, they do not match as well as the signal from one ladder. However, the objective is to cancel the fifth harmonic, which is smaller than the third harmonic and more effectively attenuated by a subsequent LPF. Thus such mismatch is less important.

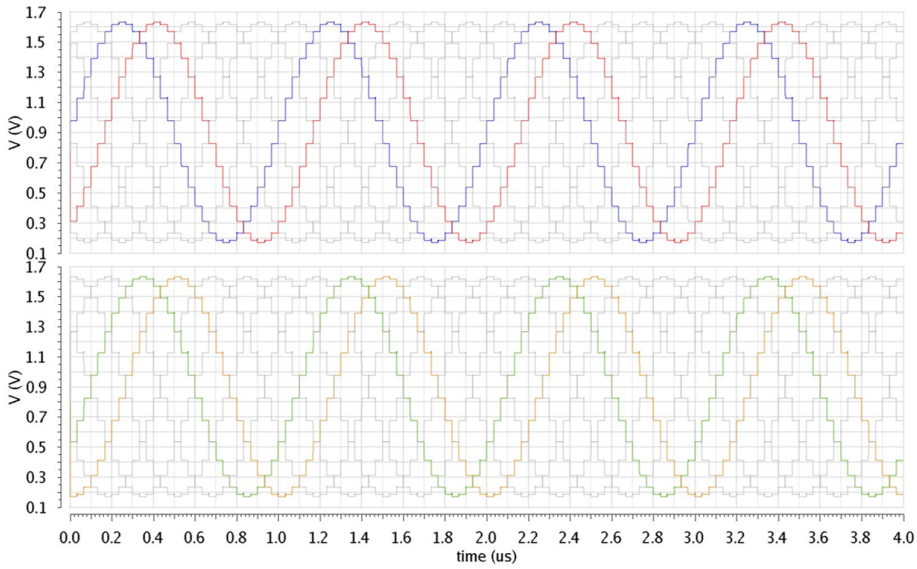


Figure 3.16: Four fully balanced outputs generated from two ladder with time shifted to cancel both 3^{rd} and 5^{th} harmonics

Using two ladders do double the power consumed, but with a 1.8v supply the current drawn by the ladder is only $50\mu A$. Moreover, all the switch control signals are produced by the same signal generator, which does not require additional power and facilitates phase matching.

This chapter presented a low THD sine-wave generator based on a two-stage HC approach. A single resistor ladder is used to generate multiple identical outputs, which are then perfectly matched with each other. To deal with both third and fifth harmonics, the required number of segments in the ladder has been calculated, ans was found to be 15, resulting in 16 levels and forming a 4-bit ladder. In addition, the signal mismatch caused by parasitic capacitors is mitigated by the proposed output balancing technique, resulting in perfectly matched outputs, which are required by HC. The schematic and layout will be presented in next the chapter.

4

CIRCUIT DESIGN

As discussed in the previous chapter, the proposed sine-wave generator is based on the concept demonstrated in Figure 4.1. Each ladder generates two time-shifted signals, the combination of which is free of the third harmonic. The sum of the four signals is free of both the third and fifth harmonics. In this chapter, the circuit and layout design will be presented.

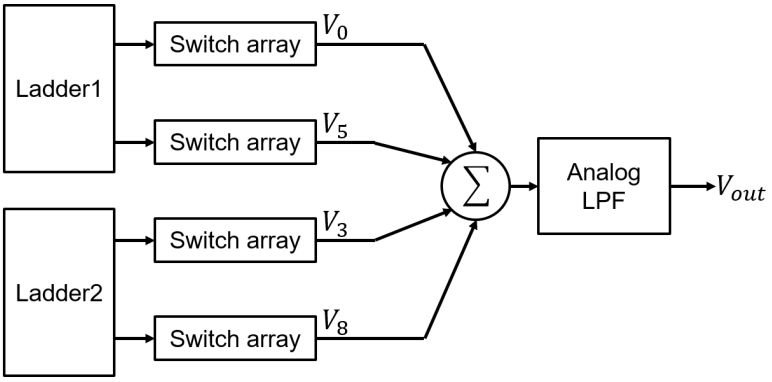


Figure 4.1: Conceptual block diagram

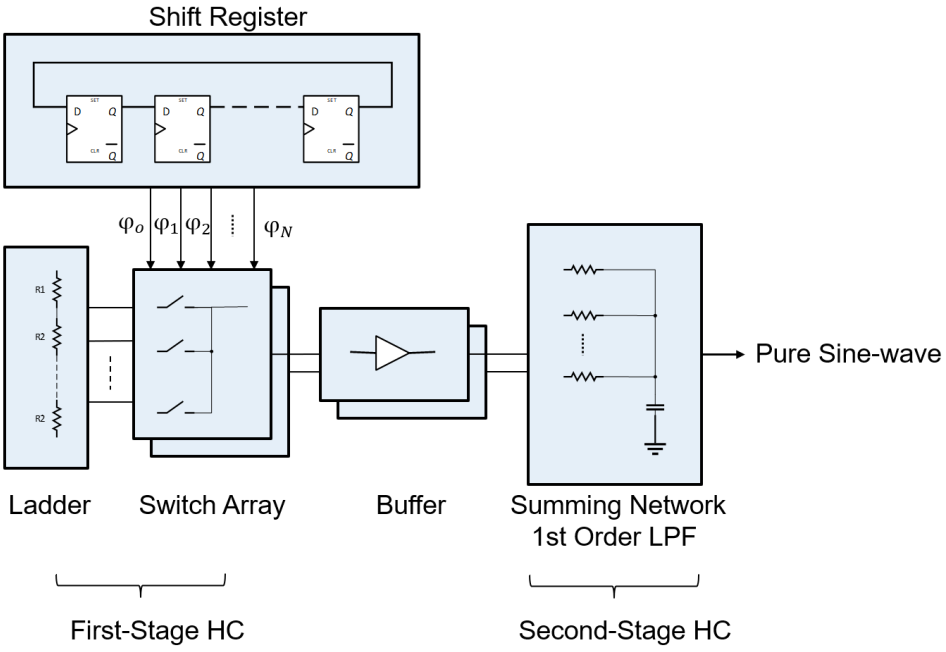


Figure 4.2: System block diagram (for simplicity, only Ladder1 and its switch arrays are presented)

4.1. SYSTEM ARCHITECTURE

The whole system consists of five parts, as presented in Figure 4.2. They are the shift register, resistor ladder, switch array, buffer and the summing network. The shift register generates control sequences for the switch arrays. The ladder is a 4-bit ladder consists of p-type diffusion resistors. A CMOS transmission gate works as the switch, providing a full signal swing. For simplicity, Figure 4.2 only presents Ladder1 and its switch arrays, which generate V_0 and V_5. Ladder2 and its switch arrays are implemented with the same structure. A resistor network sums all the time-shifted signals, executing the second-stage HC. In addition, it is loaded by a capacitor, forming a RC LPF. There is one additional block not presented in Figure 4.2. which are the logic gates between the shift register and the switch arrays to customize the control signal for every single switch.

4.2. SCHEMATIC DESIGN

In this section, the consideration and schematic design of each block is going to be presented. The resistor ladder was designed based on a previous project. In the previous project, ladders made of different material and with different sizes are measured. According to those measured data, the new ladder used in this project is determined.

4.2.1. SWITCHING SEQUENCE GENERATION

A serial-in parallel-out (SIPO) shift register generates the switching driving sequences. Its parallel outputs customize the control signals for every switch. Figure 4.3 illustrates a three-stage shift register connected in a ring configuration. The unit is a D flip-flop with the reset and setup functions, which are capable to generate a starting signal.

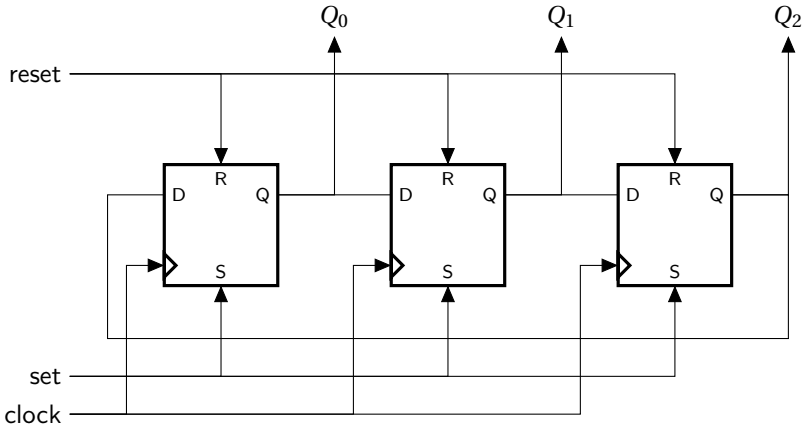


Figure 4.3: 3-stage ring shift register with parallel outputs

The starting signal can be generated by making a small modification in the structure elaborated in Figure 4.3. For a D flip-flop, When its R is enabled, Q equals 0; while its S is enabled, Q equals 1. One flip-flop's S is connected to the external reset signal as demonstrated in Figure 4.4a. When the reset signal is high, that flip-flop generates a

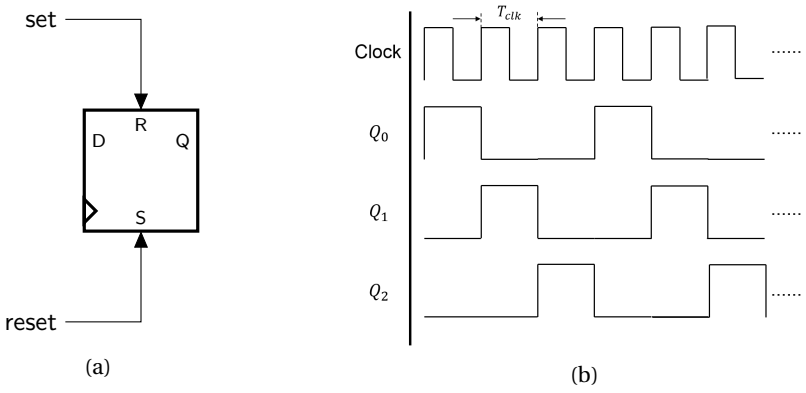


Figure 4.4: (a) Flip-flop configured as start cell (b) outputs of 3-stage shift register

logic 1 in the ring, and this logic 1 is shifted to the next flip-flop stage by stage. The R of this particular flip-flop and the S of all the other flip-flops are not enabled at any point. In this case, a three-stage shift register such as the one in Figure 4.3 has three outputs as denoted in Figure 4.4b. Connecting them to three switches permits them to turn on these switches one by one. For our ladder, which must generate a 30-step output, a 30-stage shift register is employed.

In one signal period, all the switches, except for those connected at the ladder's two ends, are turned on twice as the signal goes from the bottom to the top then back to the bottom (Figure 4.6). A simple OR gate (Figure 4.5a) combines two control signals to generate the control signal for one switch as demonstrated in Figure 4.5b.

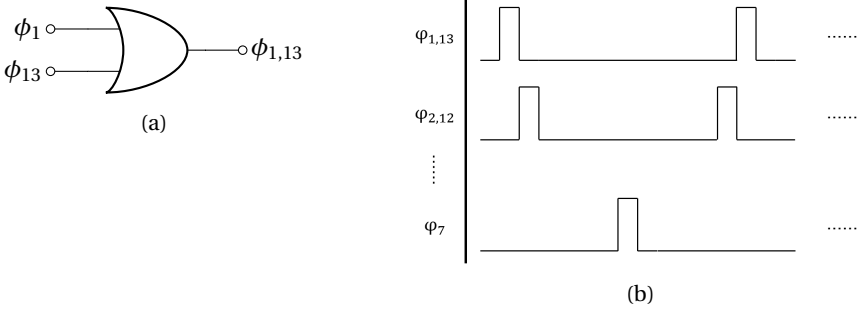


Figure 4.5: switch control logic generation (a) circuit (b) control logic

Table 4.1: Measured THD of different resistor ladders

Ladder	1	2	3	4	5	6
THD (dBc)	68.66	68.43	74.08	73.59	75.41	62.66

Ladder 1: 3-bit, poly-resistor, $1mm \times 3\mu m$
Ladder 2: 4-bit, poly-resistor, $1mm \times 3\mu m$
Ladder 3: 4-bit, active-resistor, $1mm \times 3\mu m$
Ladder 4: 5-bit, active-resistor, $1mm \times 4.18\mu m$
Ladder 5: 5-bit, active-resistor, $350\mu m \times 1.464\mu m$
Ladder 6: 5-bit, active-resistor, $194mm \times 0.816\mu m$

4.2.2. RESISTOR LADDER

In this work, the resistor ladder was designed based on the measured data of previous project. The measured data is illustrated in Table 4.1. The measurement was done at DC, by recording every node voltage of each ladder. The THDs were calculated in Matlab. Comparing the ladder 2 and ladder 3 in Table 4.1 shows that the ladder consists of p type active (diffusion) resistors has better matching and results in lower distortion than the poly-resistor ladder. The size of the resistor ladder also depends on these data. From ladder 4 to ladder 6, the ladder was scaled down while keeping the whole resistance the same. The ladder 5 is much smaller than the ladder 4, but the resulted THD is comparable. If the ladder was scaled down to ladder 6, the resulted THD became worse. Thus, the ladder 5 represents the best balance between silicon area and performance. The ladder in this project is based on the ladder 5 and has a width of $0.84\mu m$ and a length of $200\mu m$. These values were determined by scaling the ladder 5 from a 5-bit to a 4-bit ladder, which is required by the third and fifth harmonics cancellation, keeping the total resistance approximately $36k\Omega$, including the isolation resistor at two ends.

As discussed in the previous chapter, time-shifted signals are easy to generate with such a resistor ladder. For simplicity's sake, Figure 4.6 presents a 3-bit ladder with two time-shifted outputs. The driving sequences of the two switch arrays are shifted one step, resulting in two one-step time-shifted signals, V_{out1} and V_{out2}.

4.2.3. SWITCH ARRAY

To handle signals over the full supply range, CMOS transmission gates are used in the switch array unit. Since there is no current flowing through the switch at the settled state, the on-resistance variation does not cause any inaccuracy. As a result, it is not particularly necessary to scale the PMOS and NMOS to make their on-resistance equal. Moreover, the input signal for every switch is always the same for a fixed output amplitude, negating the need to worry about the on-resistance's dependence on the input signal. For this reason, each switch consists of equally sized NMOS and PMOS transistors. Small transistors have a minimal parasitic capacitance, which can reduce the charging time. In addition, there is always one switch conducting in every phase, so that the output does not suffer from charge injection or clock feedthrough. In this case, a simple transmission gate is sufficient, keeping the circuit simple.

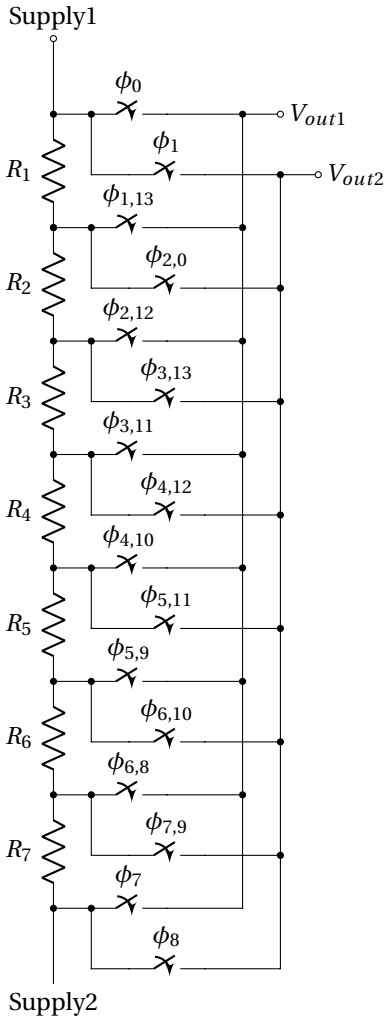


Figure 4.6: 3-bit resistor ladder with two outputs

4.2.4. BUFFER AMPLIFIER

The outputs from the ladders needed to be feed into the resistor network to execute the second-stage HC. These two blocks form a RC filter as shown in Figure 4.7. R_{ladder} and R form a voltage divider. The maximum value of R_{ladder} is approximately $36k\Omega$, requiring R to be approximately $4M\Omega$ to achieve 99% accuracy. Such a large resistor consumes a sizable area and generates large thermal noise. Thus, buffers are needed to isolate these two stages. The buffers also drive the RC filter with a low source impedance, so that R can be smaller while keeping a high signal accuracy.

The buffer used is a unity-gain amplifier. It should have a low distortion and a low output impedance. As shown in Figure 4.8, to achieve high linearity, a class-A output

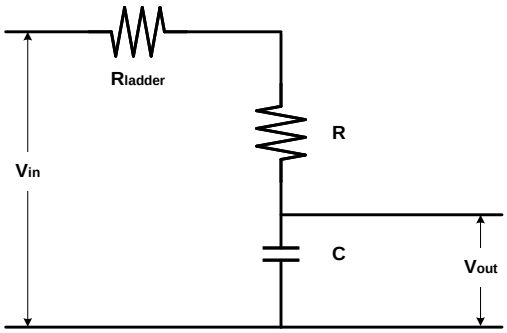


Figure 4.7: RC filter impedance matching

stage is selected. The r_{out} of output transistor should be small. A small r_{out} can be realized by increasing the $\frac{W}{L}$ of the transistor, which also means large gm, increasing the gain and reducing the effective output impedance. Since both low distortion and small output impedance are required, folded-cascode topology is used to provide a high gain. And a PMOS+NMOS differential pair is used as input stage to handle the wide signal range.

The output impedance is approximately $5k\Omega$ and the gain is $76dB$, resulting in an effective output impedance $\frac{R_{out}}{G} \approx 1\Omega$. In that case, the following RC filter can have a smaller resistance.

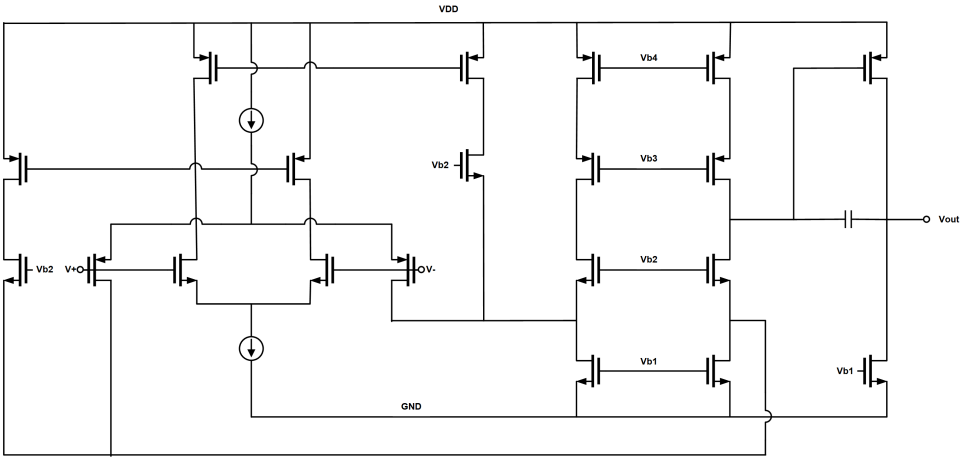
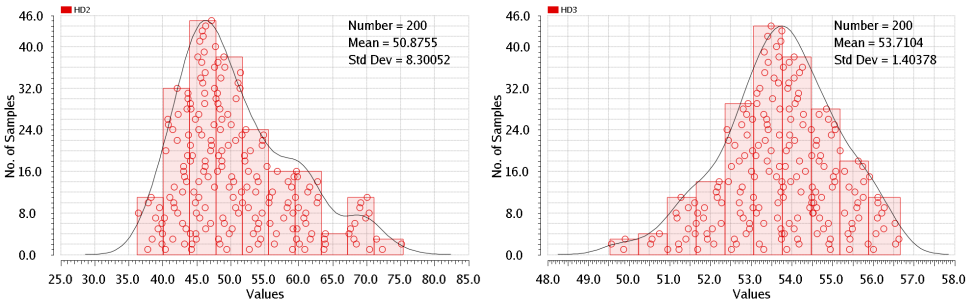


Figure 4.8: The buffer amplifier

Ideally, the amplifier's distortion is not important since the buffer-introduced third and fifth harmonics will be cancelled by the subsequent second-stage HC. Unfortunately, as discussed in the previous chapter, HC is highly dependent on the signal matching. A

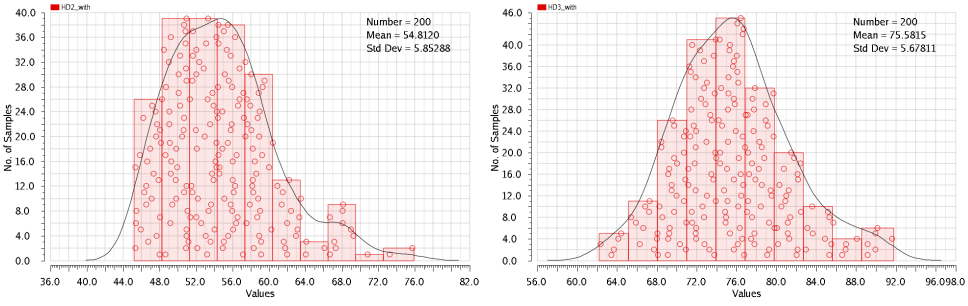
mismatch among buffers means that the buffer-introduced harmonics cannot be completely cancelled. There is a matching difference between buffer-introduced even and odd harmonics. Figure 4.9 shows the buffer-introduced HD2 and HD3 with a $1.4V_{pp}$ output. Both HD2 and HD3 are rather poor, but HD3 has much smaller standard deviation than HD2, meaning that a substantial portion of the buffer-introduced HD3 can be cancelled by the second-stage HC, while the HD2, which suffers from large deviation, can not be cancelled. The difference in standard deviations between the even and odd harmonics is due to the offset spread. Even harmonics are more sensitive to offset, which is highly dependent on components mismatch and process variations, so they suffered from a much more significant deviation than the odd harmonics.

Figure 4.10 shows the HD2 and HD3 of the final output, whose HD2 and HD3 are polluted. Figure 4.10a contains an HD2 almost identical to the one shown in Figure 4.9a, proving that the buffer-introduced second harmonic is not cancelled. That said, the HD3 in Figure 4.10b is much better than the HD3 in Figure 4.9b, confirming that the third harmonic is partially cancelled. Unfortunately, even the aimed third and fifth harmonic can be reduced by the second-stage HC, the THD is still limited by the even-order harmonics.



(a) (b)

Figure 4.9: Buffer-introduced (a) HD2 and (b) HD3 with a $1.4V_{pp}$ output swing



(a) (b)

Figure 4.10: (a) HD2 and (b) HD3 of the final differential output with a $1.4V_{pp}$ swing

For that reason, the buffer should also equip with low distortion. In this project, the

most important specification is distortion. Thus, class-A output stage is implemented to achieve high linearity while sacrificing a bit power consumption. Besides, the output swing is also limited to 400mV to further reduce the buffer-introduced distortion. As a result, the buffer achieve more than 80dB THD.

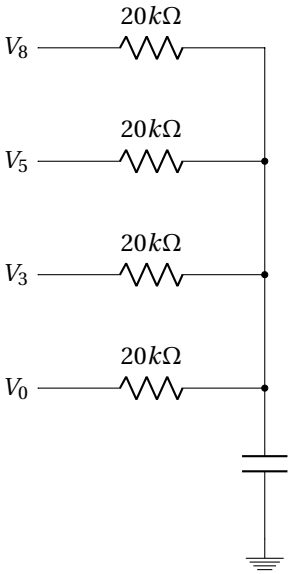


Figure 4.11: Summing network and RC LPF

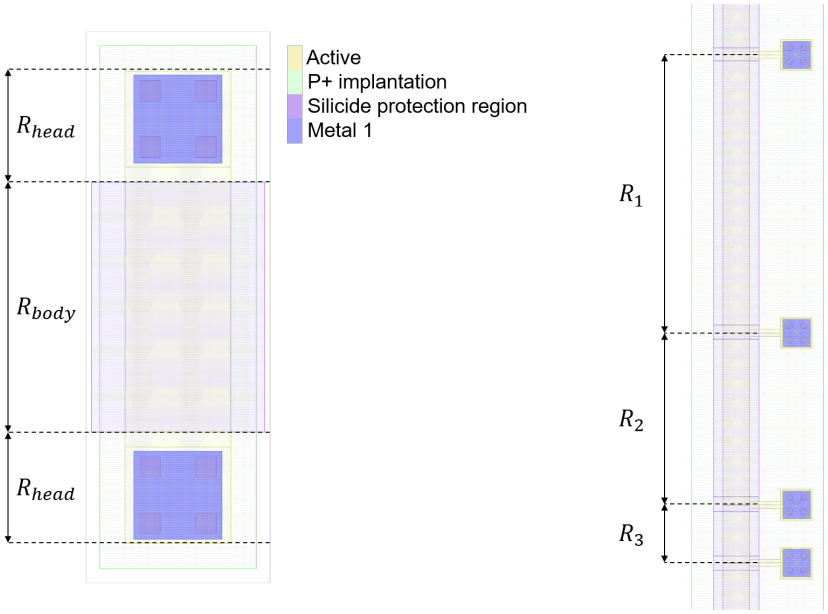
4.2.5. SUMMING NETWORK AND LOW PASS FILTER

The resistor summing network is combined with the RC filter, as shown in Figure 4.11. Since the input is buffered by the unity gain amplifier, which has an approximately 1Ω output impedance, the RC resistor can be relatively small. Here, $20k\Omega$ resistors are employed, which is smaller than the ladder's resistance. The resistor size is approximately $20\mu m \times 17.5\mu m$. The capacitor is off-chip, which can be tuned to adapt to different cut-off frequencies.

4.3. LAYOUT DESIGN

4.3.1. MATCHING OF RESISTOR LADDER

As discussed in Chapter 4.2.2, the resistors used are p type active resistors. Its resistance has two elements, the body resistance over the body silicide protection region (the light purple region as shown in Figure 4.12a) and the head resistance at the two ends of the resistor. The head has contacts with the metal, introducing a fixed resistance into every resistor. As a result, the resistance value is not proportional to the resistor's length. For our ladders, the only item of relevance is the resistance ratio. The head resistance becomes a contributor to mismatch. Thus, the head section of each resistor was removed. Their body sections were directly connected, forming a single, continuous active region.



(a) (b)

Figure 4.12: (a) Standard resistor layout and (b) modified resistor ladder layout

Metal pads were attached at the side of the resistor, as demonstrated in Figure 4.12b. At a settled state, there is no current going through these metal pads, so avoiding introducing any additional mismatch to the resistors. The voltage at each node is only determined by the body resistance. As a result, the resistance ratio is consistent with the resistor-length ratio.

Although the head sections of most resistors are removed, there are still two head sections at the ladder's two ends. Based on the measured data (from the same project mentioned in Chapter 4.2.2), the deviations of measured resistor from ideal value were calculated. Figure 4.13 contains the measured errors of every step. The potential drop across each resistor (e.g. aka $V_1 - V_2$ in Figure 4.14a) was measured and its deviation from the ideal value was calculated. The error discussed here is the relative error: $error = \frac{measured - ideal}{ideal}$. There are two huge errors, which are approximately 10%, at the two ends of the ladder. As discussed above, they are caused by the head resistance and metal pads at two ends. To solve this problem, two extra resistors were added at the ladder's two ends as illustrated in Figure 4.14. These two resistors do not belong to the ladder and act to isolate the ladder from the supply metal contacts at its two ends. Also in this case, all the ladder's resistors don not have a head resistance. Ideally, the length of the isolation resistor should be the longer the better. However, a long isolation resistor consumes a large area and reduces the output swing. In this project, the length of isolation resistor was chosen as 5% of the total length of the ladder. As a result, the measured result can be compared with that of the previous project to verify the effectiveness of the isolation

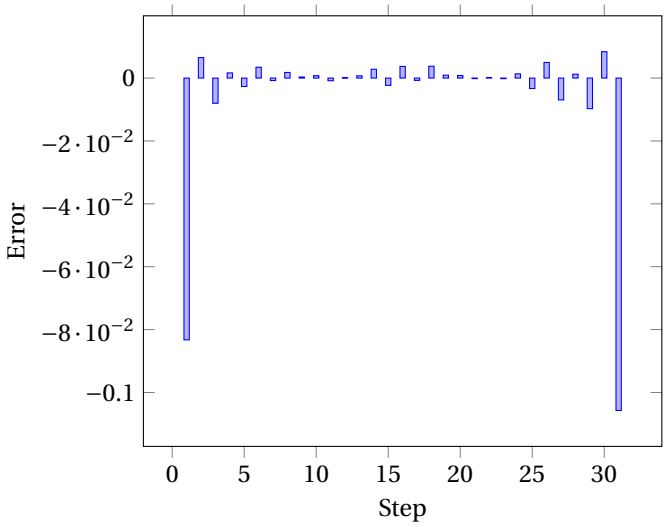


Figure 4.13: Measured relative error in previous project

resistor. The optimum value can be determined by taping-out a number of ladders with different isolation resistors in the future work.

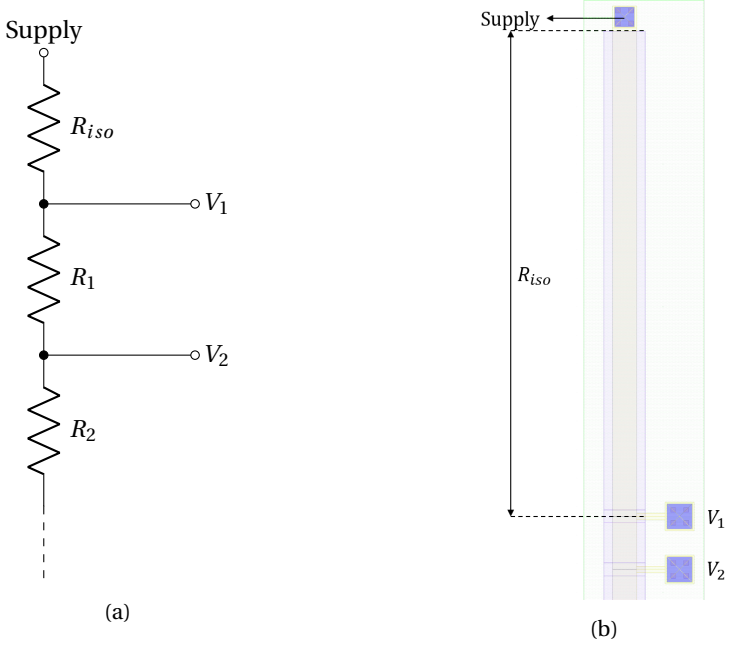


Figure 4.14: Ladder with isolation resistor (a) schematic (b) layout

4.3.2. FLOOR PLAN

The floor plan for the system is demonstrated in Figure 4.15. As discussed in the previous chapter, two ladders are implemented to cancel the third and fifth harmonics. These two ladders should be placed as close as possible to each other to improve matching. However, the matching between the two ladders only affects the effectiveness of fifth harmonic cancellation, while the phase matching is related to the cancellation of all harmonics(third, fifth and even order harmonics). Thus, to reduce phase mismatch, the switch arrays and the shift register were placed between the two ladders. In such an arrangement, the control signals' paths from the shift register to the switches have less variation, thereby resulting in better phase matching.

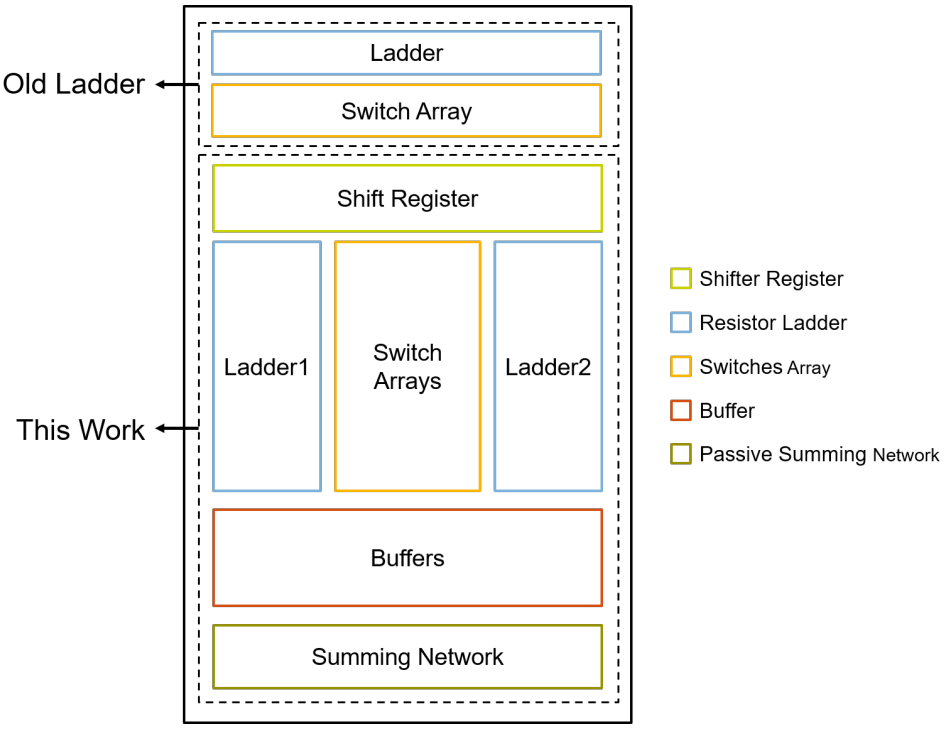


Figure 4.15: Floor plan for system layout

Each ladder has 6 groups of switches and thus 6 outputs, but only four of them are used. To provide the same load environment for every output to guarantee a good output balancing, two extra buffers are connected to the additional outputs. These two extra buffers also function as two dummy buffers at two sides of the group of buffers to ensure better matching for the buffers in use. The summing network is comprised of 8 folded, large resistors. Again, there are two dummy resistors at their two sides to achieve better matching.

The old ladder, which was the ladder 5 in Table 4.1, was integrated on the same chip for comparing purpose. The old ladder was copied from the previous project. All the

parameters were kept the same except two isolation resistors were attached at its two ends. The measured data of this ladder will be compared with the previous data to verify the effect on resistors matching of the isolation resistors.

4.3.3. PAD-RING AND PACKAGING

The bonding pads are customized for the layout design (Figure 4.16). The supplys and grounds of the pad ring, the digital part and the analog part are separated to protect analog performance from digital noise.

Finally, the chip is packaged within a 20-pin CDIL package as shown in Fig. 4.17.

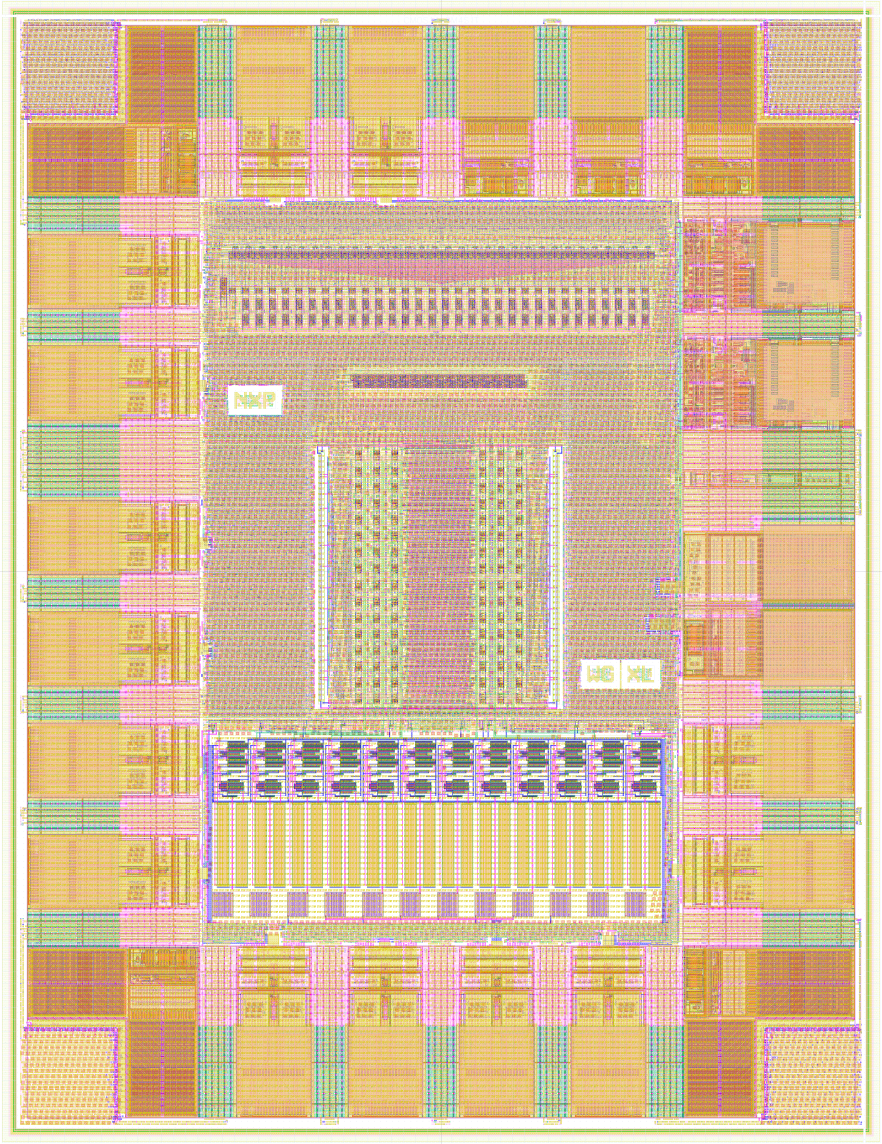


Figure 4.16: Complete System Layout

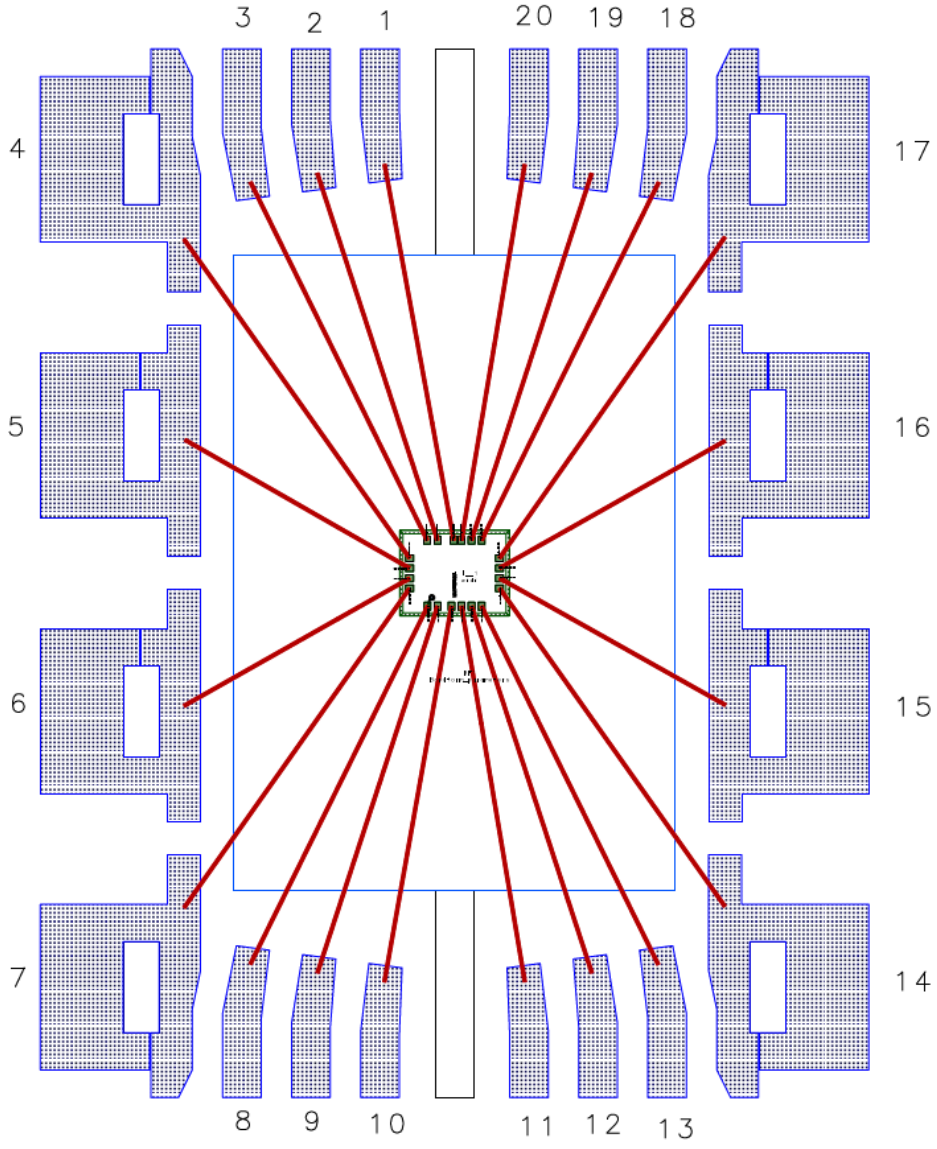


Figure 4.17: Wiring Diagram

5

Simulation and Measurement Results

A low-THD sine-wave generator based on a resistive DAC has been implemented in 140nm CMOS technology. In this chapter, the Monte-Carlo simulation of the resistor ladder and buffer, which are the main limiting factors of signal distortion, are presented and discussed. In the following measurement section, DC measurement shows the accuracy of ladder's resistors. Finally, the measurement results of THD versus output swing and frequency are presented.

5.1. SIMULATION RESULTS

5.1.1. MONTE-CARLO SIMULATION OF THE RESISTOR LADDER

To verify the influence of component mismatch and process variations on the resistor ladder, the Monte-Carlo simulation of 200 samples were made for a 1MHz output frequency. Both process variation and mismatch of the resistor ladder were considered in the simulation. Figure 5.1 shows the simulated third harmonic distortion (HD3) before and after the second-stage HC. The second-stage HC introduced an approximately 20dB HD3 improvement, as the figure clarifies. In addition, the standard deviation of HD3 was much smaller after second-stage HC, thus proving that the HD3 became less sensitive to mismatch and process variations.

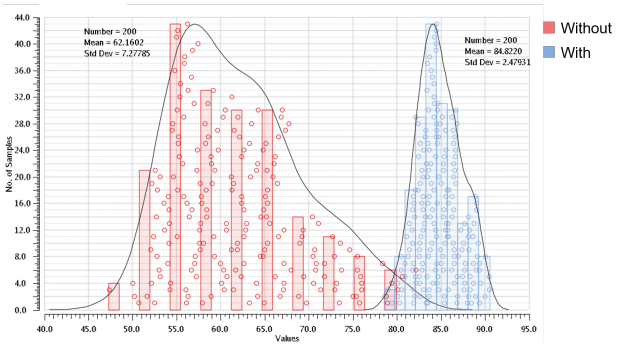


Figure 5.1: Simulated output: HD3 histogram with and without the second-stage HC

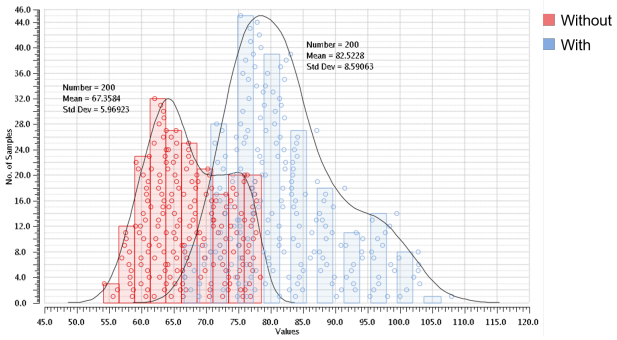
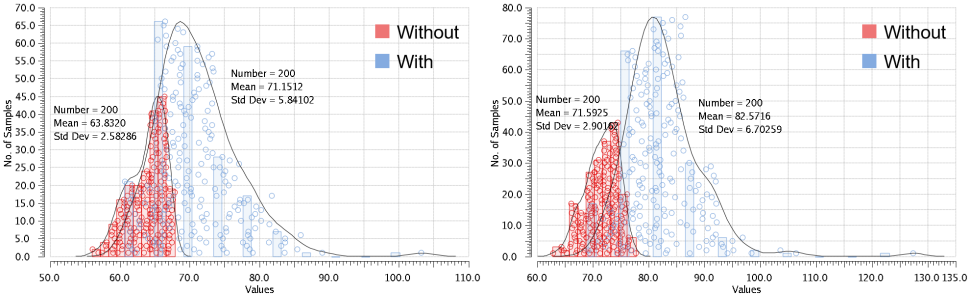


Figure 5.2: Simulated output: HD5 histogram with and without the second-stage HC

Figure 5.2 shows the simulated HD5 results. HD5 is improved by 15dB approximately. The improvement is a bit less compared to that for HD3, this is because HD5 depends on the matching of two ladders, which involves more components.

Apart from the attenuation of HD3 and HD5, the second-stage HC also reduces even harmonic distortion, as shown in Figure 5.3. As even harmonics are caused by asymmetric signals, HC, which is also an averaging stage, potentially reduces the even harmonics. However, the reduction is quite limited as it strongly depends on mismatch and process variations.



(a) (b)

Figure 5.3: Simulated output: (a) HD2 and (b) HD4 histogram with and without the second-stage HC

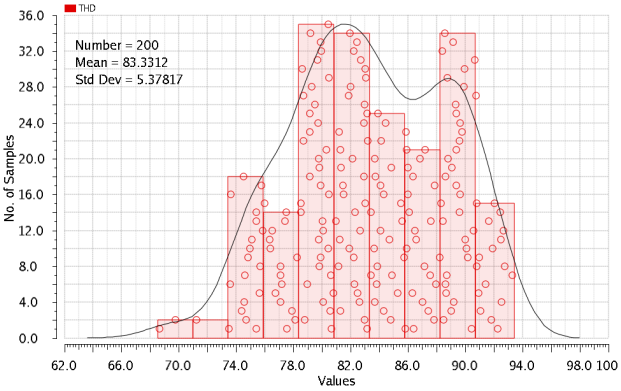


Figure 5.4: Simulated buffer amplifier THD

5.1.2. BUFFER AMPLIFIER SIMULATION

The buffer should not introduce more distortion to the ladder's output, Thus, the signal swing is limited to 400mV as a larger signal swing would cause excessive distortion. Figure 5.4 shows the Monte-Carlo THD simulation of 200 samples, proving that the amplifier can achieve more than 80dB THD.

5.2. TEST SETUP

The proposed low THD sine-wave synthesizer was fabricated using CMOS14 technology and packaged in a 20-pin CDIL package. The pin configuration and functions are shown in Figure 5.5 and Table 5.1 respectively.

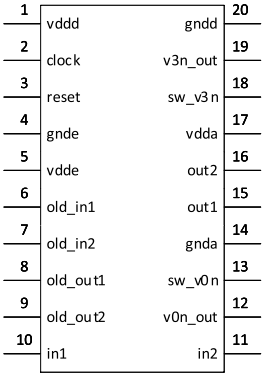
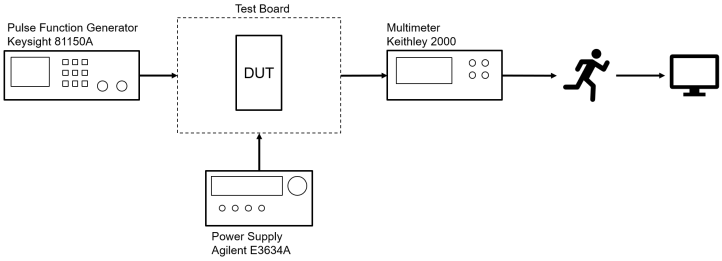
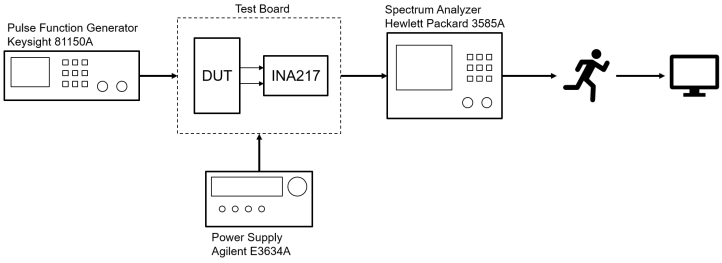


Figure 5.5: Pin configuration



(a)



(b)

Figure 5.6: The test setup for (a) DC measurement and (b) spectrum measurement

Table 5.1: Pin functions

PIN		I/O	DESCRIPTION
Name	NO.		
vddd	1	I	Digital supply (1.8v)
clock	2	I	Digital supply (1.8v)
reset	3	I	Reset signal, low enable
gnde	4	I	Padring ground
vdde	5	I	Padring supply (1.8v)
old_in1	6	I	Top supply of old ladder (maximum 1v)
old_in2	7	I	Bottom supply of old ladder
old_out1	8	O	Output1 of old ladder
old_out2	9	O	Output2 of old ladder
in1	10	I	Top supply of ladder
in2	11	I	Bottom supply of ladder
v0n_out	12	O	Direct output from ladder
sw_v0n	13	I	Switch connecting v0n-out to the board, high enable
gnda	14	I	Analog ground
out1	15	O	One differential output
out2	16	O	One differential output
vdda	17	I	Analog supply (1.8v)
sw_v3n	18	I	Switch connecting v3n_out to the board, high enable
v3n_out	19	O	Direct output from ladder
gndd	20	I	Digial ground

There are three groups of outputs. Pins 8 and 9 are the differential outputs of the old ladder. Pins 12 and 19 are the two direct outputs of the new resistor ladder, which are the input signals of the internal buffers. Pins 15 and 16 are the differential signals after the second-stage HC.

The test setup is shown in Figure 5.6. The external clock and power supply needed to be clean enough and to not introduce any extra harmonics. For DC measurement, the ladder's nodes voltages were measured by a Keithley 2000 multimeter. The measured data was imported into Matlab and distortion and deviation were calculated. For spectrum measurement, an instrumentation amplifier INA217 was added at the output of the sine-wave generator to combine differential signals into single-ended one and to drive spectrum analyzer. INA217 has a roughly 0.0003% THD+N and 1MHz bandwidth [20]. As a result, the GBW of INA217 became the main limiting factor for high-frequency measurements. The input capacitor of INA217 adds extra capacitance to the RC filter, causing inaccuracy of cutoff frequency. This is not a problem since the capacitor of the RC filter is off chip and can be tuned freely.

5.3. MEASUREMENT RESULTS

Based on the above test setup, DC and AC measurements were done. The data was processed and analyzed in Matlab.

5.3.1. DC MEASUREMENT

DC measurement was aimed to specifically measure the voltages at the various nodes of the resistor ladder. All the node voltages were measured and recorded. First, the relative errors (as discussed in Chapter 4.3.1) of the old ladder were measured. The result is shown in Figure 5.7. Compared to the result shown in Figure 4.13, the relative errors at two ends of the ladder were reduced from 10% to approximately 2%. It proves that the isolation resistors improve the bottom and top resistors matching. However, the resulted THD is 75.95dBc, which is almost the same as the previous result 75.41dBc. This is because the isolation resistors only increase the accuracy of the resistors at the two ends while the other resistors are not affected. The bottom and top resistors have limited influence on the resulted THD. Although the errors of these two resistors decrease, the resulted THD is still limited by the mismatch of other resistors.

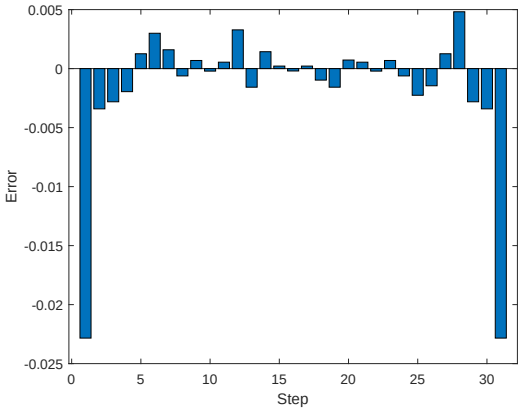


Figure 5.7: Measured relative error of the old ladder

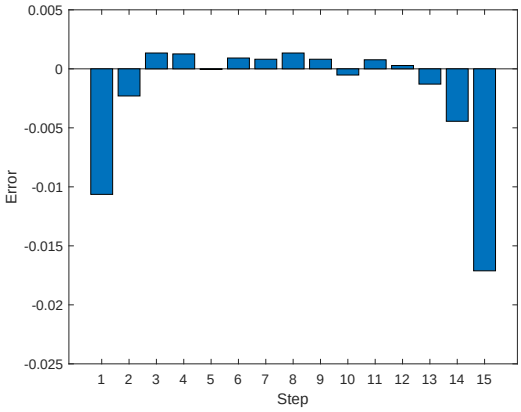


Figure 5.8: Measured relative error of the new ladder

The same measurement and calculation were done for the new ladder. Its relative error is shown in Figure 5.8, and is very comparable to the old ladder. In addition, the resulted THDs of the old and the new ladders are 75.95dB and 74.98dB respectively. Both the relative error and THD of the two ladder are very close, proving that the scaling from a 5-bit ladder to a 4-bit ladder succeeded.

5.3.2. SPECTRUM MEASUREMENT

First, the relationship between the THD and the output swing was investigated. The output swing was mainly limited by the buffer amplifier. Due to the mismatch between the buffer amplifiers, their introduced harmonics could not be cancelled, distorting the outputs with large swing. As discussed above, even- and odd-order harmonics have different sensitivities to mismatch and process variations, and so a portion of the buffer-introduced odd-order harmonics were cancelled while the even-order harmonics were not. Figure 5.9 gives the spectrum for a 50kHz output with a $1.4V_{pp}$ output swing. HD3 was lower than HD2 and even lower than HD4. The HD2 was very close to the buffer amplifier's simulated HD2 (Figure 4.9a), while the measured HD3 was much better than the simulated buffer-introduced HD3 (Figure 4.9b). This proves that a portion of HD3 was cancelled since it had a lower standard deviation, as the simulation revealed. Figure 5.10 shows the output's HD2 and HD3, along with the output swing. As the figure clarifies, HD2 rapidly declined and was finally consistent with the buffer-introduced HD2. It meant that the buffer-introduced HD2 was not cancelled due to the large deviation. On the other hand, for HD3, it was always much better than the buffer's HD3 thanks to the small deviation that resulted in efficient HC.

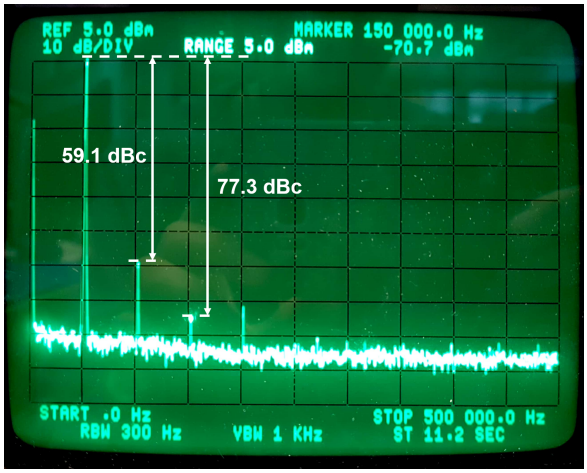


Figure 5.9: Measured spectrum of 50kHz output with a 1.2 output swing

Figure 5.11 presents the results for a 10kHz, 400mVpp output. Figure 5.11a shows the signal before second-stage HC (signal V8 shown in Figure 4.11). It had very poor SFDR due to resistor mismatch and phase errors. with the help of the second-stage HC, as the final output in Figure 5.11b presents, all harmonics were attenuated to a very low level.

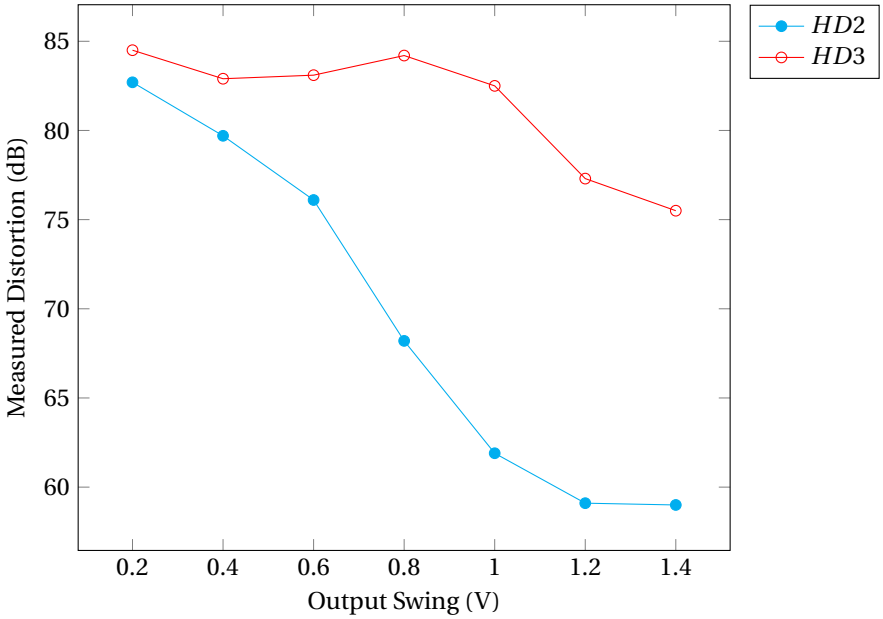
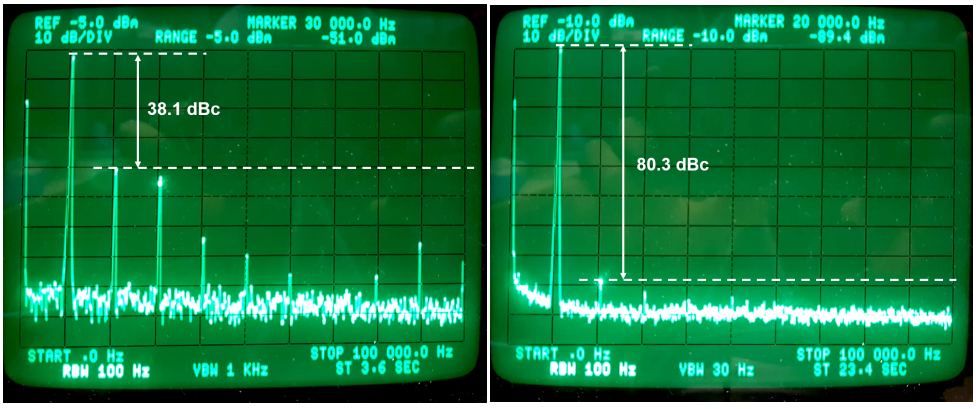


Figure 5.10: Measured distortion versus output swing at 50 kHz

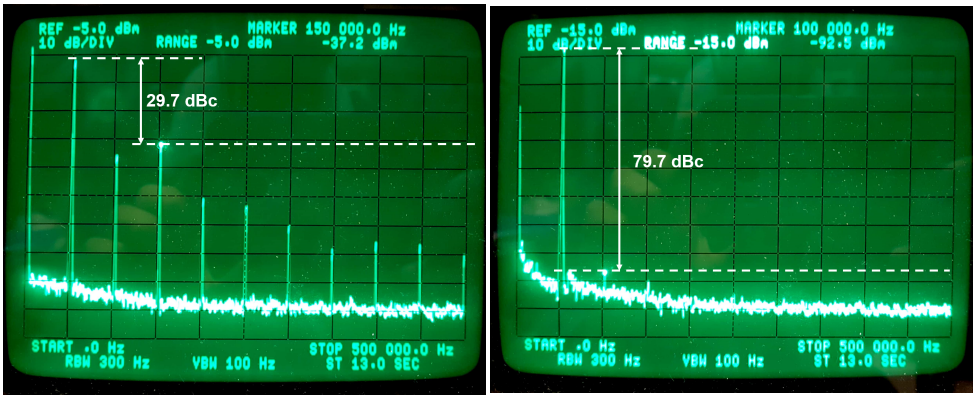
The undesired third and fifth harmonics were more than 80dB lower than the fundamental. While a small second-harmonic residue remained, the value was still approximately 80.3dB lower than that of the fundamental. The residual harmonics were mainly limited by the buffer distortion, as discussed in the previous simulation results. Higher-order odd harmonics were filtered out by the LPF.



(a) (b)

Figure 5.11: Measured spectrum of a 10kHz, 400mV_{pp} sine-wave: (a) ladder's direct, single-ended output (b) final differential output

At higher frequencies, the THD without the second-stage HC worsened, as shown in Figure 5.12a. This result occurred because at high frequencies, the influence of the transition region became stronger. Thanks to the second-stage HC, the SFDR and THD also declined to approximately 79.7dBc and 77dBc respectively at higher frequencies, as presented in Figure 5.12b. Notably, the noise floor increased at low-frequencies due to the flicker noise of the buffer amplifier. The noise floor at 55kHz was roughly $150nV/\sqrt{Hz}$, resulting in an 80dB SNR in a 20kHz bandwidth. At higher frequencies, the noise floor further declined to $45nV/\sqrt{Hz}$ at 550kHz, resulting a better SNR.



(a) (b)

Figure 5.12: Measured spectrum of a 50kHz, $400mV_{pp}$ sine-wave: (a) ladder's direct, single-ended output (b) final differential output

Figure 5.13 makes it even clearer that the THD without second-stage HC became poorer as the frequency increased, while the THD after second-stage HC barely changed. As the proposed method deals with both amplitude and phase errors, it yielded more significant improvements at higher frequencies. No additional calibration or high-order LPF was needed; instead, with only simple resistors and switches, a decent THD and SFDR were achieved. The THD before second-stage HC became constant at high frequencies, because the transition region expanded to encompass the whole step duration. That factor meant that the signal had not settled yet when the next switching point arrived. This was mainly due to the large capacitor of the spectrum analyzer (30pF for Hewlett Packard 3585A used). Such a large load capacitor needs a long charging period, which means large transition region. Although adding a off-chip buffer can reduce the ladder's load capacitance so that reduce the transition region, the signal distortion caused by the transition region still exists. A smaller load capacitor can reduce the slope, but the signal THD and SFDR still decrease as frequency increases,

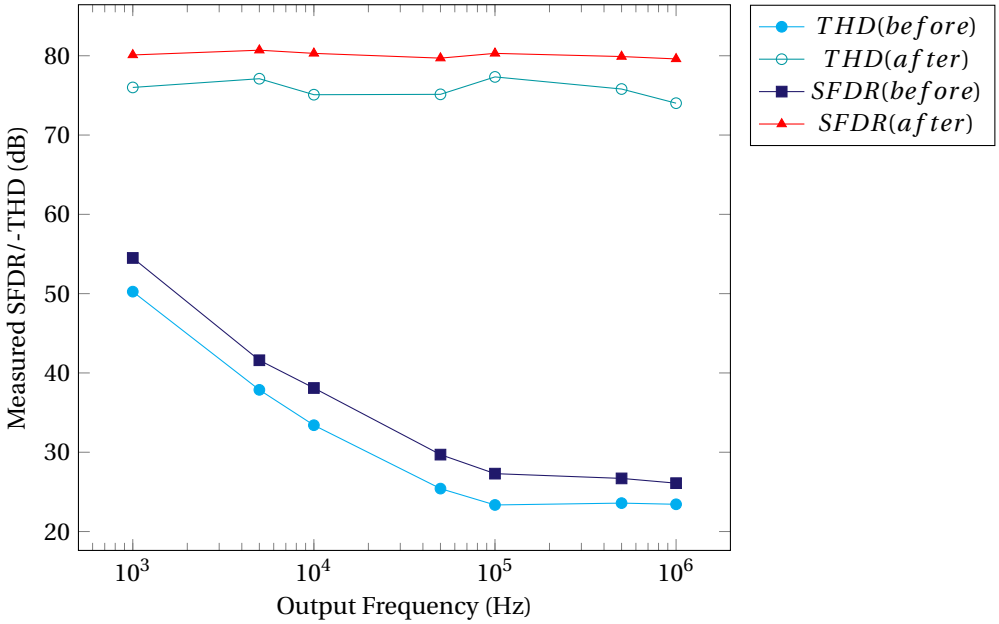


Figure 5.13: Measured SFDR/THD versus output frequency

In summary, this chapter presented the simulation and measurement results of the proposed sine-wave generator. The resistor ladder design are based on a previous project. Isolation resistors are added to improve the resistor matching and its effect is proved by the DC measurement. The proposed two-stage HC are also verified in spectrum measurement. It achieves approximately 80dB SFDR and 77dB THD from 1kHz to 1MHz.

6

CONCLUSION

6.1. SUMMARY AND DISCUSSION

A low-distortion sine-wave generator employing scaled resistive ladders has been proposed, implemented and measured. A two-stage harmonic cancellation (HC) scheme is proposed to achieve low THD. Besides the first-stage HC realized by the ladders, the second-stage HC is introduced to further attenuate the third and fifth harmonics. As the proposed second-stage harmonic cancellation is less sensitive to components mismatch and process variations, it can achieve a good HD3 and HD5 without any post-fabrication optimization or calibration, keeping the whole system simple, versatile and cost-effective. The final summing stage is integrated with a LPF by combining the resistor network with a load capacitor. It realizes the summing function required to implement the second-stage HC, and also works as a LPF to smooth the output signal. With the help of the proposed two-stage HC, which relaxes the matching requirement for the resistor ladder, the ladder can be scaled down and be more area efficient.

6.2. FUTURE WORK

As discussed in Chapter 4.2.4, the main limitation of the system is the buffer used to isolate the resistor ladder and resistor network. As shown in Figure 5.10, the buffers introduce significant harmonic distortion in the presence of signals with amplitudes more than $400mV_{p-p}$. As a result, the buffer should be designed for a larger signal swing in future work. An alternative is to verify the structure proposed in Figure 3.2a, which has a more mismatch, but does not require any buffer.

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