

## A 10-bit, 771 nW Time-Mode ADC with a 2-Step TDC for Bio-Signal Acquisition

Kandilakis, Emmanouil; Serdijn, Wouter A.; Akgun, Omer Can

**DOI**

[10.1109/BioCAS49922.2021.9644997](https://doi.org/10.1109/BioCAS49922.2021.9644997)

**Publication date**

2021

**Document Version**

Accepted author manuscript

**Published in**

BioCAS 2021 - IEEE Biomedical Circuits and Systems Conference, Proceedings

**Citation (APA)**

Kandilakis, E., Serdijn, W. A., & Akgun, O. C. (2021). A 10-bit, 771 nW Time-Mode ADC with a 2-Step TDC for Bio-Signal Acquisition. In *BioCAS 2021 - IEEE Biomedical Circuits and Systems Conference, Proceedings: Proceedings* (pp. 1-6). Article 9644997 (BioCAS 2021 - IEEE Biomedical Circuits and Systems Conference, Proceedings). IEEE. <https://doi.org/10.1109/BioCAS49922.2021.9644997>

**Important note**

To cite this publication, please use the final published version (if applicable).  
Please check the document version above.

**Copyright**

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

**Takedown policy**

Please contact us and provide details if you believe this document breaches copyrights.  
We will remove access to the work immediately and investigate your claim.

# A 10-bit, 771 nW Time-Mode ADC with a 2-Step TDC for Bio-Signal Acquisition

Emmanouil Kandilakis\*, Wouter A. Serdijn\*, and Omer Can Akgun\*

\*Section Bioelectronics, Delft University of Technology, the Netherlands

Email: e.kandilakis@tudelft.nl, w.a.serdijn@tudelft.nl, o.c.akgun@tudelft.nl

**Abstract**—In this paper, we present the design of a low-voltage, low-power, and small-area time-mode ADC (TM-ADC) for bio-signal sensing applications. The proposed time-mode ADC (TM-ADC) consists of a programmable oversampling ratio (OSR), voltage-controlled ring oscillator (VCRO) based analog-to-time converter (ATC), followed by an asynchronous unfolded SAR coarse TDC and an asynchronous, enhanced-range fine flash TDC. The integrated circuit has been implemented in a standard CMOS 65 nm process and its performance has been evaluated through extracted transient noise simulations. The ADC consumes 771 nW at a sampling rate of 2.2 kHz from a 0.5V supply voltage and achieves 10-bit resolution in a total area of 0.014 mm<sup>2</sup>. The simulation results indicate DNL and INL values of +0.86/-0.83 and +0.88/-1.79, respectively, an SNDR of 60.7 dB and an ENOB of 9.8 bits for a 10mV peak-to-peak signal 1 kHz input signal.

**Index Terms**—Bio-signal sensing, time-mode operation, analog-to-time conversion, two-step, time-to-digital conversion.

## I. INTRODUCTION

While the technology scaling is beneficial for improving the performance of digital systems, it imposes the lowering of the supply voltages for reliability concerns, while the reduction in the threshold voltages is minimal. This effectively reduces the headroom available for analog signal processing and enforces strict constraints on the analog signal processing chain and the front-end of ADCs, in turn limiting the achievable noise performance and processing speed. This limitation can be addressed by two main approaches. The first approach is moving the accuracy and precision burden from the analog to the digital domain. This is achieved by minimizing the analog part of modern signal processing systems and the creation of more and more digitally heavy signal processing chains. The second approach is using time-mode signal processing (TMSP) techniques and focuses on the representation and quantization of the signals in the time domain [1]–[4]. The main advantage of TMSP is the improved timing resolution that comes with technology scaling as the gate delays are reduced, resulting in a higher signal-to-noise ratio (SNR) for operating on a fixed time pulse. In order to take advantage of TMSP techniques in analog-to-digital conversion, two main blocks are required, namely, the analog-to-time converter (ATC), and the time-to-digital converter (TDC).

In a time-mode ADC, the ATC initially converts a voltage value to a time difference. This time difference can either be the difference between the rising and falling edges of a signal, or two separate signals, a start and a stop signal. Subsequently, the time difference is resolved by a TDC into a digital value. The result of the conversion is a digital word representing the time difference and, hence, the sampled analog value, similar to the digital output word in analog-to-digital (AD) conversion.

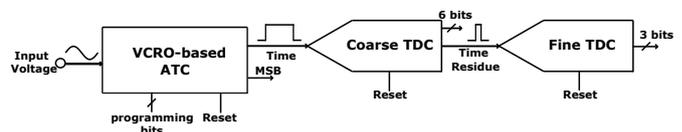


Figure 1. Block level diagram of the proposed ADC. The analog-to-time converter (ATC), and coarse and fine time-to-digital converters (TDCs) are shown.

Time-mode systems find more and more applications in the biomedical field, such as biomedical imaging applications [5], diffuse optical tomography measurements [6], and measuring the electrocardiogram R-R interval [7].

The main goal of the research presented here is to develop a low-voltage, low-power, small-area and medium-resolution time-mode ADC for biomedical applications. The proposed time-mode ADC is presented in Figure 1 and it consists of a voltage-controlled ring oscillator (VCRO) based ATC, followed by an asynchronous unfolded SAR coarse TDC and an asynchronous, enhanced-range fine flash TDC. As the analog voltage is sensed, the ATC converts it into a time pulse, embedding the analog information to a time period between a rising and a falling edge. Moreover, it produces the most significant bit (MSB) of the conversion depending on the polarity of the input signal. The output of the ATC is then fed to the unfolded SAR TDC that operates as a coarse-quantizer. The coarse TDC outputs not only the 6-bit digital conversion of the original time pulse, but also a time residue, that is later converted by the fine TDC to obtain the remaining 3 digital bits. Then, a simple digital block combines the three digital outputs to the final 10-bit equivalent of the analog input value.

The contributions and organization of this paper are as follows: First, the three main blocks of the ADC, the VCRO-based ATC, the asynchronous unfolded SAR coarse TDC and the enhanced-range fine flash TDC, are described in Section II. In this section, detailed analysis of the system-level design choices, operation of each sub-system as well as implementation details are presented. In Section III, the simulation results are given and a comparison with state-of-the-art biomedical ADCs is made. Finally, conclusions are drawn in Section IV.

## II. SYSTEM DESIGN AND IMPLEMENTATION

This section presents the key components and the system-level design choices of the proposed asynchronous time-mode ADC. The first block in the signal chain is a VCRO-based ATC. It has been selected due to its low power consumption, small area, and suitability for having a programmable

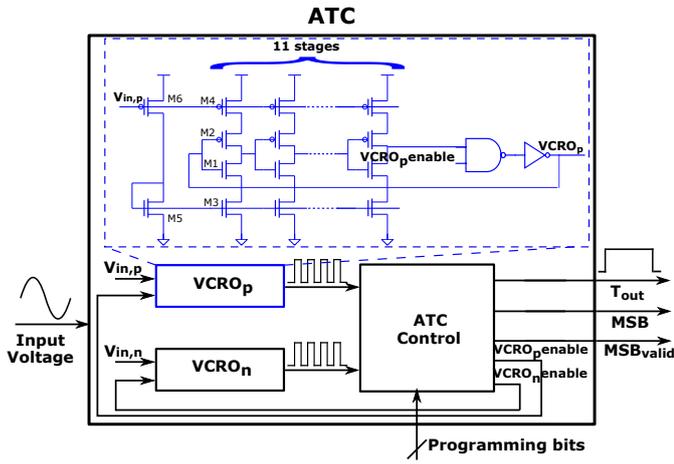


Figure 2. Block level diagram of the designed ATC with the schematic of the VCRO highlighted.

oversampling ratio. The second block is the TDC that has been implemented in a two step fashion, consisting of an unfolded SAR coarse TDC with time-mode subtraction and a fine enhanced range flash TDC. The coarse TDC aims in converting a wide time range difference and it is chosen for both low power consumption and small area properties while having moderate conversion speed. The second TDC has been selected for its low power consumption, small area, monotonicity and high conversion speed. The whole implementation is asynchronous due to the event based nature of time-domain signals and achieves lower power operation due to lack of a clocking signal while providing a better interface to TMSP systems [8].

### A. Analog-to-Time Converter

The front-end of the ADC is the analog-to-time converter (ATC). It consists of two VCROs working in a differential fashion and a logic control block as shown in Figure 2. A VCRO-based ATC has been selected as its gain, noise performance and sensing capabilities fit the demands of biomedical sensing applications and through its digital control, it offers a high level of programmability for oversampling. VCROs, compared to relaxation oscillators, are able to achieve relatively higher spectral purity, while maintaining a smaller size due to the lack of big passive elements. The monostable multivibrator circuit described in [9] had also been taken into consideration as an ATC, however its performance in terms of spectral purity and programmability was considered inferior to a VCRO based implementation.

As there is no need for high oscillation frequencies, current starving is applied to achieve a reduced power consumption, an important benefit in biosensing applications [10]. In Figure 2 the schematic of the VCRO is shown in blue. Each delay stage is composed of the inverter core (transistors M1 and M2) and the current starving transistors (M3 and M4). The top (M4) and bottom (M3) transistors modulate the source and sink currents depending on the analog input voltage. In order to increase the gain of the VCRO, the current of the input transistor (M6) is copied through M5, and is used to modulate the resistance of both the header and footer transistors. To control the oscillation

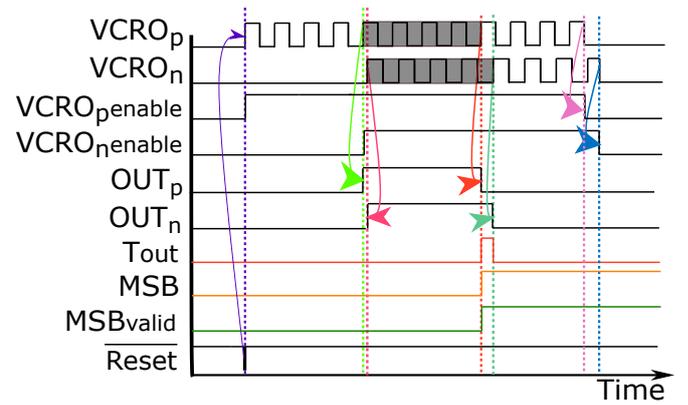


Figure 3. Timing diagram showing the internal signals and operation of the ATC.

and to be able to power down the ATC when not needed, a reset mechanism was implemented by the addition of an AND logic gate. The implemented VCRO achieves a constant gain over the input signal range, with a reset signal to control its operation. The ATC control block controls the operation of the two VCROs, creates the final time pulse as the output of the converter and also generates the MSB of the conversion. Furthermore, this control block adds oversampling ratio (OSR) programmability to the design.

In order to explain the operation principle, a timing diagram is given in Figure 3. As soon as the active-low reset signal goes high, the  $VCRO_{p\_enable}$  goes high and  $VCRO_p$  begins oscillating. Then, the next 10 cycles are discarded in order to have a stable oscillation frequency (for simplicity and lack of space, the example shows only 4 cycles discarded). As soon as the cycle count reaches 10, the ATC control block asserts its internal  $OUT_p$  signal and the  $VCRO_n\_enable$  signal, in order to start the  $VCRO_n$ . The  $VCRO_n$  starts oscillating as well, causing the internal  $OUT_n$  signal to be asserted. Onward, the number of periods of oscillation for both VCROs are counted and their outputs are deasserted as soon as the desired OSR is achieved, OSR being the number of oscillation cycles. In the timing diagram, the OSR is set as four for simplicity.  $VCRO_p$  reaches the OSR limit first and thus  $OUT_p$  is the first signal to be deasserted. At this moment, the ATC control block generates the rising edge of the output time signal ( $T_{out}$ ) and the MSB is being decided. When the  $VCRO_n$  reaches the OSR limit, the  $OUT_n$  signal and thus the output of the ATC ( $T_{out}$ ) are deasserted, finalizing the generation of the output time pulse. The two VCROs keep oscillating for 4 more periods in order to eliminate any effects from the power-down of the circuit to the converted time pulse.

In bio-signal acquisition applications, the input signals have extremely low amplitude, and amplification and/or oversampling is necessary to get a meaningful SNR. Oversampling in ADCs is a commonly used technique to suppress the sources of noise or error with a Gaussian distribution on top of the signal. The power of these sources is reduced by a factor of 3 dB per doubling of the OSR, while keeping the signal power constant [11]. Oversampling in this implementation is achieved by summing the oscillator cycles modulated by the same input signal in the time domain through the ATC control

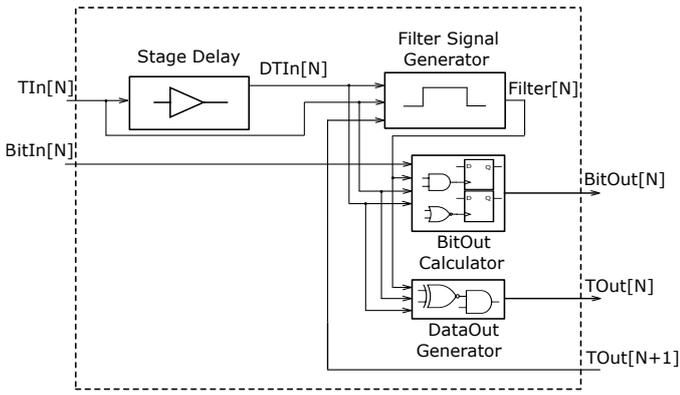


Figure 4. Block diagram of a stage of the asynchronous unfolded SAR coarse TDC, based on [12] with a modified Filter Signal Generator.

block, resulting in a significantly reduced noise as a result of noise averaging.

### B. Time-to-Digital Converter

The time-to-digital conversion in the system is implemented in two stages. First, the time pulse is fed to an asynchronous, unfolded SAR algorithm based coarse TDC employing time-mode subtraction. This TDC outputs 6 digital bits and a residue time pulse. Subsequently, the enhanced-range fine flash TDC quantizes the time residue to an 8-bit thermometer code, which is later converted into 3 digital bits. Due to the event-based nature of time-mode signals, both TDCs operate asynchronously. The choice of a two-stage architecture was made in order to relax the resolution requirements of the coarse TDC and to be able to acquire extended range measurements needed for the calibration of the TDC, which is work still in progress.

1) *Coarse Time-to-Digital Converter*: The coarse TDC is implemented as an asynchronous 6-stage unfolded SAR TDC employing time subtraction similar to [12]. The selection of such an architecture was due to its reduced power and area consumption, while achieving sufficient resolution and conversion speed for biomedical sensing applications. Moreover, the lack of time amplification between the cascaded stages, as typically is done in the analog domain, is an extra benefit that reduces the power consumption.

The block diagram of a stage of the coarse TDC is illustrated in Figure 4. Time-mode subtraction as well as the operation principle of the implemented TDC are described in detail in [12]. [N] in the figure denotes the values for the Nth stage,  $TIn[N]$  is the input pulse to be resolved,  $BitIn[N]$  is the resolved bit from the previous stage,  $DTIn[N]$  is the delayed input signal,  $Filter[N]$  is the signal marking the operating time window of interest,  $BitOut[N]$  is the resolved bit by the stage,  $TOut[N]$  is the output time residue, and  $TOut[N+1]$  is the time residue output from the following stage. As a two-step time to digital conversion approach has been implemented and a fine TDC follows the coarse one, we made two main changes to the implementation in [12]. First, the time window of the time subtraction (the Filter Signal Generator block) has been modified and the window is defined by the rising edge of the input signal and the falling edge of the time-mode output

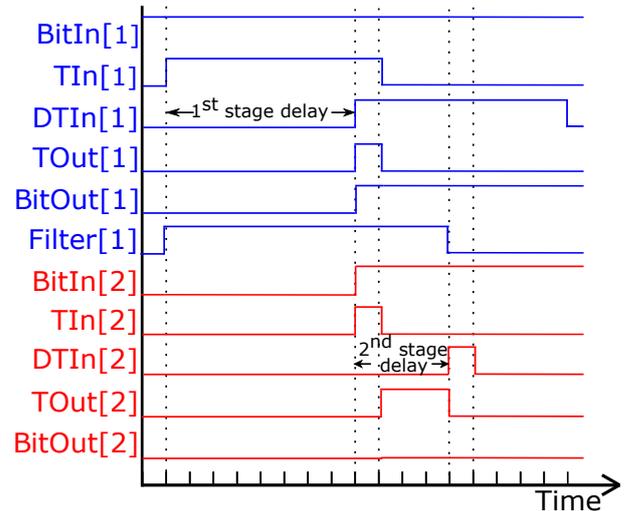


Figure 5. Operation timing diagram of the coarse TDC showing its operation principle for 2 consecutive stages.

pulse of the next stage. Moreover, the completion detection described in [12] has not been implemented as it would result in wrong time residues fed to the fine TDC.

The timing diagram showing the operation of the first two stages is presented in Figure 5. Let us assume that a time pulse larger than the first stage delay and smaller than the sum of the first two stage delays is generated by the ATC and is fed to the TDC. It should be noted that the delay in the stages is the amount to be subtracted from the input value. In the first stage, the input signal and its delayed version overlap and according to the conversion logic previously presented in [12], and given that the  $BitIn[1]$  is 1, the decision of conversion is  $BitOut[1]=1$  and the resulting time pulse is  $TOut[1]$ . In the following stage, the input signal ( $TIn[2]=TOut[1]$ ) and its delayed version do not overlap, resulting in a “negative”  $TOut$  pulse, and given that the  $BitIn[2]=1$ ,  $BitOut[2]$  is resolved to be 0.

The implementation details of the delay elements are of interest, as they need to create delays in the order of microseconds with minimal amount of power consumption. In order to satisfy the above criteria, Dynamic Leakage Suppression (DLS) delay cells have been investigated. In [13] and [14], DLS logic cells have been used as a way to reduce the standby power consumption by up to three orders of magnitude, at the cost of substantially degrading the operating speed of the circuit. The low standby power consumption and the lack of need for high speed operation in many bio-signal sensing applications led to the selection of such an implementation for the delay cells. The DLS cells described in [13] and [14] achieved delays of a few microseconds for an energy consumption of a few fJs in our simulations. However, the process variation resilience and the jitter performance of those designs are not sufficient for our targeted performance metrics. The standard DLS inverters operate using only the leakage currents, and, thus, they are very sensitive to the shifts in the threshold voltage due to process variations. Furthermore, the jitter performance of the same DLS inverters is bad due to the fact that the  $\mu s$  delays achieved from the cells are due to the slow rising and falling edges, translating to a large  $dt/dV$ . In

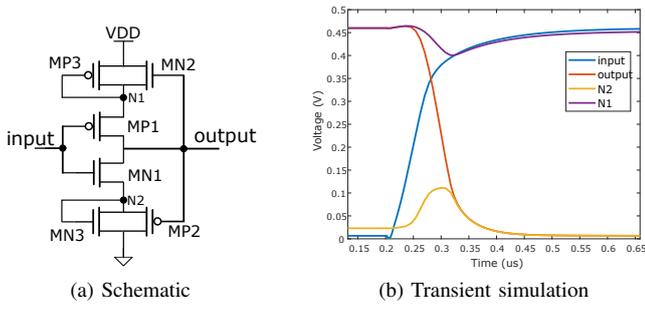


Figure 6. a) Schematic and b) Transient simulation results of the modified DLS inverter.

such a case, a small voltage noise is translated into a large-time uncertainty and, thus, jitter.

In order to circumvent these drawbacks, modifications have been made to the standard DLS inverter. The schematic and the transient simulation results of the modified DLS inverter are presented in Figure 6(a) and Figure 6(b), respectively. Two diode-connected transistors (MN3 and MP3) have been added in parallel with the feedback transistors (MN2 and MP2). By the addition of the diode-connected transistors, the operation of the standard DLS inverter has been improved in two ways: 1) the internal nodes N1 and N2 do not settle around  $VDD/2$  as in the standard version, but around  $VDD$  and  $VSS$ , respectively, as the parallel connected devices (MN3 and MP3) are not in the cut-off region but they are in weak inversion, pulling the internal nodes close to the rails, and 2) the charging and discharging of the output node does not depend only on the leakage currents of the big feedback devices, but also on the current of the small diode-connected transistors, resulting in faster rising and falling edges, hence less noise-to-jitter conversion. However, the drawback of this approach is that the delay elements consume more power and have higher leakage currents. Moreover, because they are much faster, more elements are needed to achieve the desired delay for each stage.

2) *Fine Time-to-Digital Converter*: An enhanced-range, asynchronous flash TDC is used as the fine TDC, and its block diagram is shown in Figure 7. This implementation has multiple advantages over that of standard synchronous flash TDCs. First, the asynchronous implementation of the flash TDC offers reduced power consumption, as active energy is only used during the conversion period and a clocking network is not required. Second, it has an enhanced input range, meaning an increased input pulse-width range that can be accommodated, and is realized by looping the output of the TDC back to its input and counting the number of looping cycles through a counter, as shown in Figure 7. The

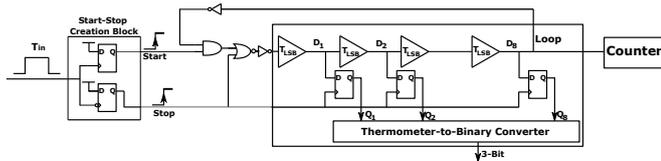


Figure 7. Block diagram of the asynchronous, enhanced-range flash fine TDC.

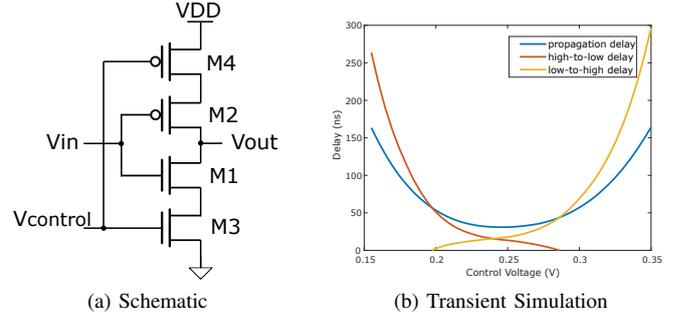


Figure 8. a) Schematic and b) Transient simulation results of the current starved inverter used in the fine TDC.

implemented loop counter is a 5-bit one and is also used in the calibration mechanism that is currently under development.

The input of the fine TDC is the time delay between the rising and falling edges of the residue pulse created by the last stage of the coarse TDC. However, the flash TDC implementation requires the time information to be encoded as the difference between two rising edges of two pulses. For this reason, a start-stop creation block has been implemented, to create the required start and stop control signals. In order to achieve the delay values needed and to deal with the mismatches created by the different rise and fall times of the propagated signals in the fine TDC, the delay cells consist of four current-starved inverters instead of just one inverter, as is commonly done in high resolution TDCs. Current-starved inverters, shown in Figure 8(a), have been used as they achieve higher delay values with low power consumption. A single control voltage has been used to control the delay in order to reduce the effects of control voltage fluctuations on the stage delay around  $0.25\text{ V}$  ( $VDD/2$ ), as shown in the simulation results in Figure 8(b). This reduction in sensitivity to the control voltage happens due to the fact that with a higher control voltage the NMOS limiting device (M3) sinks more current, leading to a smaller high-to-low propagation delay, while the PMOS limiting device sources less current, leading to a higher low-to-high propagation delay, averaging out the change in the stage delay. Furthermore, as a delay cell is composed of four inverters, the four propagation delays are averaged, leading to a reduced delay value change due to process variation.

### C. ADC Layout

Figure 9 shows the layout of the ADC. In the yellow box, the two VCROs of the ATC together with two decoupling capacitors are placed. In the red boxes, the stage delays of the coarse TDC are highlighted. The green box marks the fine TDC, and the purple box marks the control logic of the ATC, the coarse TDC, and the counter of the fine TDC.

## III. SIMULATION RESULTS

The ATC and the TDCs have been characterized extensively through extracted transient-noise simulations. As the required computing power and the simulation time for the complete characterization of the chain were beyond our means, both blocks were characterized separately. Even in such a situation, due to the simulation time and computing power constraints,

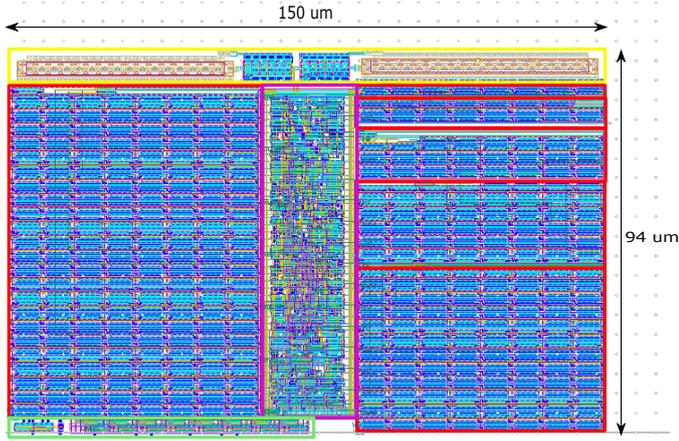


Figure 9. ADC layout with the implementation dimensions.

the transient-noise simulation based FFT of the ATC could not be run for the desired OSR of 600, which is expected to yield a signal-to-noise and distortion ratio (SNDR) of more than 60 dB for the ADC. However, the implemented ATC has been simulated for a variety of OSRs, and we verified that with each doubling of the OSR, a 3 dB improvement in the SNR is achieved. By the extrapolation of our simulation results, we calculated an achievable SNDR of 58.18 dB for the pulse generated, for a total expected SNDR of 64.18 dB (with an extra 6 dB coming from the MSB) for the whole ADC. Figure 10 shows the FFT of the ATC for an OSR of 128. As it can be observed, the implemented differential ATC has a linear behavior with a third order component at -66.42dB and for this reason we do not expect a reduced linearity or lower than expected SNDR for the ATC for an OSR of 600.

In our transient-noise simulations, the jitter contributions from the time-to-digital converter stages were always better than the design requirements, i.e., 11-bits of accuracy for the first stage, 10-bits of accuracy for the second stage, etc. Therefore, we concluded that the quantization noise of the TDC and DNL errors are the main factors affecting the

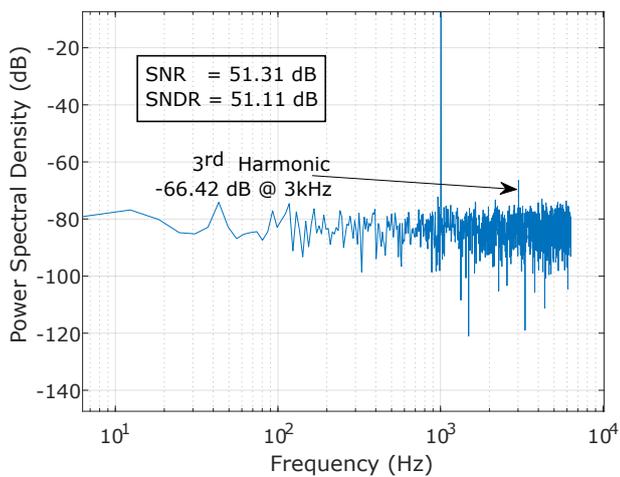


Figure 10. FFT of the pulse generated by the ATC for an OSR of 128 and a 10 mVpp input signal at 1 kHz.

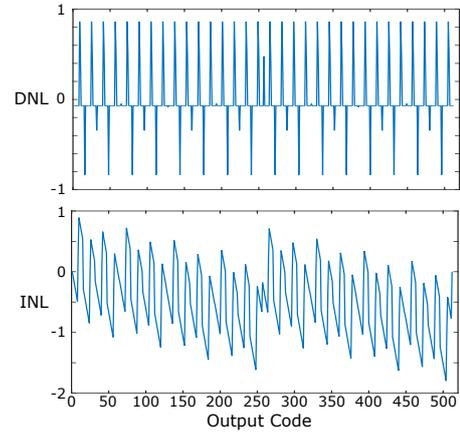


Figure 11. Static simulation results showing the DNL and INL of the TDC.

performance of the ADC. The number of bits out of the TDC will set the base SNDR, and DNL errors will affect the noise floor of the ADC, as described in equation (1) from [15]:

$$SN_{Q+DNL}R = 6.02N - 9.03 - 10^{10} \log \left( \frac{1}{12} + \frac{DNL^2}{2\lambda^2} \right) \quad (1)$$

where  $\lambda = DNL * T_{LSB} / \sigma_{jitter}$ ,  $T_{LSB}$  is the time LSB value of the TDC, and  $\sigma_{jitter}$  is the total time-domain noise of the TDC.

The DNL and INL of the post-layout TDC are presented in Figure 11 and the maximum and minimum values of DNL and INL are +0.86/-0.83 and +0.88/-1.79, respectively. Plugging these numbers into equation (1), we get an expected SNDR and effective number of bits (ENOB) of 60.7 dB and 9.8 bits, respectively.

The power consumption of the whole ADC is simulated to be 771 nW from a 0.5 V supply. In the pie chart of Figure 12(a), the power consumption contributions of the various sub-blocks of the converter are shown. As can be easily observed, the majority of the power is consumed in the coarse TDC delay elements. It should be noted that, the active energy dissipated during the creation of the delayed input signal DTIn is smaller than the leakage energy of the delay elements, as the delay elements remain idle for the majority of the conversion period.

The areas of the various ADC components are illustrated in the pie chart in Figure 12(b). It is easily observed that the

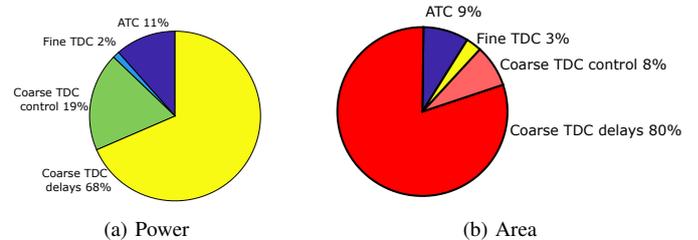


Figure 12. Pie chart of contributions of different components in the implemented ADC for a) Power, and b) Area.

Table I  
PERFORMANCE COMPARISON OF THE IMPLEMENTED ADC WITH STATE OF THE ART.

	[17]	[16]	[18]	[19]	This Work*
Technology (nm)	180	130	180	65	65
Resolution (bits)	8	10	8	9	10
Supply Voltage (V)	0.5	1	0.8	0.55	0.5
Input Range (Vpp)	0.25	1	2.25	NA	0.01
Input Bandwidth (kHz)	2.05	0.5	5.1	10	1.1
ENOB (bits)	6.9	9.1	7.9	8.21	9.8**
Power (nW)	850	53	840	159	771
Area (mm <sup>2</sup> )	0.11	NA	0.05	0.191	0.014
FoM <sub>Schreier</sub> (dB)	137	156	147	159	152

\*Post-layout simulation results. \*\* This value is obtained through extrapolation from the post-layout transient noise simulation results.

coarse TDC delay elements occupy the biggest part of the ADC area and the total ADC area is 0.01410mm<sup>2</sup>.

The performance summary of the ADC and comparison with state of the art ADCs for biomedical sensing applications is given in Table I. As can be observed from the table, the area of the presented ADC is substantially smaller than the compared ADCs. Moreover, for the achieved resolution, the power consumption is comparable with all the other converters. The power consumption of [16] is an order of magnitude lower, however, a full scale input has been applied during tests and the power consumption for signal amplification is not included in the power consumption number. In the presented ADC, there is no need for pre-amplification of the sensed signal as it is amplified internally through the programmable OSR time averaging mechanism in the ATC. The Schreier Figure of Merit (FOM) [15] is used for comparison, and it is given by:

$$\text{FoM}_{\text{Schreier}} = \text{SNDR} + 10 \log \left( \frac{f_{\text{sampling}}/2}{\text{Power}} \right) \quad (2)$$

Based on this FoM, the work presented in this paper has comparable FoM to other implementations in the literature while having the smallest area and best ENOB performance.

#### IV. CONCLUSIONS

This paper presents a low-voltage, low-power and small-area time-mode Analog-to-Digital Converter with a resolution of 10-bits for bio-signal sensing applications. The TM-ADC consists of a VCRO based ATC, followed by an asynchronous

unfolded SAR coarse TDC and an asynchronous, enhanced-range fine flash TDC. The implemented ADC uses programmable time-mode oversampling to improve the SNDR in the ATC. The delay elements of the coarse TDC are based on a modified version of DLS inverters improving the jitter performance and reducing process variation effects on the performance. The ADC has been designed to be implemented in a standard CMOS 65 nm process and, in post-layout circuit simulations, consumes 771 nW at a sampling rate of 2.2 kHz from a 0.5 V supply. The ADC delivers 10-bit accurate results with an ENOB of 9.8 bits for a 10 mVpp 1 kHz input signal.

#### REFERENCES

- [1] D. Miyashita, R. Yamaki, K. Hashiyoshi, H. Kobayashi, S. Kousai, Y. Oowaki, and Y. Unezawa, "An ldpc decoder with time-domain analog and digital mixed-signal processing," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 1, pp. 73–83, 2013.
- [2] Y. Lyu and F. Tavernier, "A 4-gs/s 39.9-dB SNDR 11.7-mW hybrid voltage-time two-step ADC with feedforward ring oscillator-based TDCs," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 7, pp. 1807–1818, 2020.
- [3] V. Ravinuthula, V. Garg, J. G. Harris, and J. A. Fortes, "Time-mode circuits for analog computation," *International Journal of Circuit Theory and Applications*, vol. 37, no. 5, pp. 631–659, 2009.
- [4] Z. Chen and J. Gu, "Analysis and design of energy efficient time domain signal processing," in *Proceedings of the 2016 International Symposium on Low Power Electronics and Design*, 2016, pp. 100–105.
- [5] Z. Cheng, M. J. Deen, and H. Peng, "A low-power gateable vernier ring oscillator time-to-digital converter for biomedical imaging applications," *IEEE transactions on biomedical circuits and systems*, vol. 10, no. 2, pp. 445–454, 2015.
- [6] M. Kanoun, L. Arpin, V.-P. Rheaume, M.-A. Tétrault, Y. Bérubé-Lauzière, and R. Fontaine, "A 10-bit, 3 ps rms precision time-to-digital converter for diffuse optical tomography measurements," in *2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. IEEE, 2014, pp. 554–557.
- [7] B. Ghanavati, E. Abiri, N. Azhdari, and M. R. Salehi, "A tlbco optimized tdc for biomedical applications," in *Electrical Engineering (ICEE), Iranian Conference on*. IEEE, 2018, pp. 76–80.
- [8] M. Miskowicz, *Event-based control and signal processing*. CRC press, 2018.
- [9] O. C. Akgun, Y. Leblebici, and E. A. Vittoz, "Current sensing completion detection for subthreshold asynchronous circuits," in *2007 18th European Conference on Circuit Theory and Design*. IEEE, 2007, pp. 376–379.
- [10] S. Suman, K. Sharma, and P. Ghosh, "Analysis and design of current starved ring vco," in *2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*. IEEE, 2016, pp. 3222–3227.
- [11] A. V. Oppenheim, *Discrete-time signal processing*. Pearson Education India, 1999.
- [12] O. C. Akgun, "An asynchronous pipelined time-to-digital converter using time-domain subtraction," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2018, pp. 1–5.
- [13] W. Lim, I. Lee, D. Sylvester, and D. Blaauw, "8.2 batteryless sub-nW cortex-m0+ processor with dynamic leakage-suppression logic," in *2015 IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*. IEEE, 2015, pp. 1–3.
- [14] D. Bol, R. Ambroise, D. Flandre, and J.-D. Legat, "Building ultra-low-power low-frequency digital circuits with high-speed devices," in *2007 14th IEEE International Conference on Electronics, Circuits and Systems*. IEEE, 2007, pp. 1404–1407.
- [15] M. J. Pelgrom, "Analog-to-digital conversion," in *Analog-to-Digital Conversion*. Springer, 2013, pp. 325–418.
- [16] D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.1-enob 1-ks/s SAR ADC in 0.13µm CMOS for medical implant devices," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1585–1593, 2012.
- [17] J. Sauerbrey, D. Schmitt-Landsiedel, and R. Thewes, "A 0.5-V 1-µW successive approximation ADC," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, pp. 1261–1265, 2003.
- [18] Y. Li, D. Zhao, and W. A. Serdijn, "A 0.8 V 8-bit low-power asynchronous level-crossing ADC with programmable comparison windows," in *2013 IEEE Biomedical Circuits and Systems Conference (BioCAS)*. IEEE, 2013, pp. 138–141.
- [19] M. Yip and A. P. Chandrakasan, "A resolution-reconfigurable 5-to-10b 0.4-to-1V power scalable SAR ADC," in *2011 IEEE International Solid-State Circuits Conference*. IEEE, 2011, pp. 190–192.