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A DPLL-Based Phase Modulator Achieving -46dB EVM with A Fast Two-Step DCO Nonlinearity Calibration and Non-Uniform Clock Compensation

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Abstract

We present a broadband digital PLL (DPLL)-based phase modulator supporting wide frequency modulation (FM) bandwidth (BW). It compensates for the EVM degradation due to the non-uniform period of the retimed updating clock and shortens the nonlinearity calibration time of the digitally controlled oscillator (DCO) with a phase-domain digital pre-distortion (DPD) and an encoding-assisted (EA)-LMS calibration. While generating a 10MHz 64-PSK signal, the prototype can achieve -46dB EVM with less than one-tenth of the calibration samples (time) required by the prior art.

Introduction

Using a DPLL-based phase modulator in a polar transmitter (TX) can greatly improve its system efficiency. Yet, several challenges impede the deployment of high-order modulation schemes (e.g., 256QAM) in such TXs for multi-band IoT. First, in a two-point modulation scheme, the inherent DCO nonlinearity due to its $f_0=1/\sqrt{LC}$ characteristic of resonant frequency and mismatches between the switched-capacitor (SC)-units in the DCO's modulation bank degrade EVM. This nonlinearity worsens with a wider FM-BW due to the increased feed-forward frequency division N (Fig.1) in supporting the multi-band operation [1]. Second, current calibration methods for DCO nonlinearities settle very slowly [2][3], taking a long time to reach acceptable EVM for demodulation, thus wasting energy. Third, since the DCO accumulates the desired phase by integrating the FM data over time, the inevitably non-uniform period of the FM updating clock introduces errors in phase modulation (PM). We tackle these issues by introducing: 1) a PVT-insensitive polynomial-based DPD to remove the DCO 1/√LC nonlinearity, 2) an EA-LMS to further linearize the DCO and shorten its calibration, and 3) a non-uniform clock compensation (NUCC) scheme to further improve EVM.

Proposed DPLL-based Phase Modulator

Fig.1 shows the proposed DPLL-based phase modulator. To avoid metastability, the digital blocks update the oscillator tuning words (OTWs) and FM at a non-uniform DCO-synchronous clock (i.e., CKU), resulting from retiming the reference (FREF) by the DCO output (CKV). The PM target, ϕ_M, is obtained by scaling the desired phase by $N/2\pi$ ($1/2\pi$ for normalization). Then, its differentiation, $\Delta\phi_M$, modulates the PLL via two paths: direct modulation (DM) and phase prediction (PP). On the DM path, $\Delta\phi_M$ modulates the DCO frequency by Δf_M, accumulating excess phase ϕ'_V, ideally equal to ϕ_M, over the CKU cycles. The final output is CKV phase ϕ_V, including both ϕ'_V and carrier phase ϕ_C (see the DCO phase model). On this path, a two-step calibration (DPD + EA-LMS) combats the DCO nonlinearity.

On the PP path, $\Delta\phi_M$ is accumulated together with the frequency control word (FCW) to output ϕ_R, which predicts the ideal ϕ_V at the CKU rising edges. However, to extract and correct the PM error, the sampled ϕ_V must be compared with its prediction, ϕ_S, at FREF's falling, instead of CKU's rising, edges. Hence, the NUCC is introduced to map ϕ_R to ϕ_S according to the delay between these two clock edges. In contrast to [4], which tackles only the constant delay, NUCC further considers its time-varying component (i.e., Δt_S, the instantaneous delay between FREF and subsequent CKV falling edges), and corrects for it by using the equation at the bottom of Fig.1.

As shown in Fig.2, the DCO phase accumulation time, $T_{acc}[n]$, differs from its ideal value, T_{REF} (FREF period). This results in a phase error, $\Delta\phi'_{V,e}[n]$, as the DCO accumulates the excess phase by integrating Δf_M over time. Therefore, the second task of NUCC is to estimate $\Delta\phi'_{V,e}[n]$ and compensate for it by adding an extra phase, ϕ_{DMC}, to $\Delta\phi_M$ in the next CKU cycle. The key point of calculating $\phi_{DMC}[n+1]=-\Delta\phi'_{V,e}[n]$ lies in $T_{acc}[n]$ estimation with the fractional part of ϕ_S ($\phi_{S,F}$), as shown in the equations in Fig.2.

Fig.3 shows the DCO schematic and block diagram of the proposed fast two-step calibration technique. Firstly, to remove the DCO's 1/√LC nonlinearity, a quadratic term ($\alpha\cdot\Delta\phi_M^2$) is subtracted from $\Delta\phi_M$. In contrast to [1][5], which require complex measurements to determine the scaling factor, here α is an accurate and design-independent value of 1.5/FCW, mainly because the DPD is applied to $\Delta\phi_M$ instead of its *de*-normalized OTW, OTW_M. This DPD eliminates the dominant static nonlinearity and gives a good initial point to the EA-LMS calibration to remove the residual nonlinearity dominated by the mismatches between the units of the coarsest modulation SC-bank, MCB. This calibration removes the integral nonlinearity (INL) related to each MCB codeword (OTW_{MCB}), by adding its paired compensating value, REG, through OTW_C to the finest SC-bank, TB. The REGs are estimated by accumulating the correlated TDC output. Considering the $\Delta\phi_M$ probability distribution in Fig.3, the OTW_{MCB} codes related to large $|\Delta\phi_M|$ occur rarely. Hence, due to the lack of training samples, an LMS-only algorithm, e.g. [2], converges slowly, since a REG can only be updated when its paired OTW_{MCB} is used. We notice that each code successively inherits INL from its neighbor in any thermometer-encoded structure. Therefore, the TDC output of a high probability OTW_{MCB} also reflects the INL inherited by certain lower probability codes. Exploiting this fact, the proposed EA-LMS calibration updates those slow REGs at multiple OTW_{MCB} to shorten the convergence time.

Measurements and Conclusion

The proposed phase modulator is fabricated in 40nm CMOS. Its active area is 0.31mm^2 (Fig.6) and it consumes 4.4mW at 40MHz FREF. Its output *centered* within 2.6—3.9GHz is divided by ÷N off-chip before measurements, thus requiring ×N wider FM-BW. The table in Fig.4 summarizes the measured EVM of a 10MSym/s 64-PSK 3.188GHz signal in different scenarios. When the proposed techniques are disabled (baseline), due to the worse DCO linearity for wider FM-BW (increasing N from 1 to 8), EVM degrades from -37.1 to -20.8dB. Next, by sequentially enabling the DPD, EA-LMS, and NUCC techniques at N=8, the EVM improves by 15dB, 8dB, and 2.7dB, respectively, and reaches -46.5dB. The

corresponding output spectrum and constellation diagram are shown in Fig.4. The EVM also remains <-43dB over the modulator's tuning range. To evaluate the performance with a 5MHz 256QAM signal, the measured PM signal at N=4 was combined with an ideal AM signal in Matlab. The EVM of -46.3dB and spurious emission of -47.8dB (Fig.4) indicate its capability to support high-order complex modulation schemes in polar TXs. Fig.5 shows the EVM settling trajectory. Compared to the LMS-only methods (with the same update step size, μ_{DCO} in Fig.3), our work benefits from a 15dB lower starting baseline and a 4× steeper descent due to the proposed DPD and EA-LMS, respectively. Therefore, the settling is 10× faster than with the conventional LMS-only method to reach its optimum EVM. Compared with the prior art in Table-I, our work demonstrates the lowest EVM, shortest calibration time, and the best energy efficiency while facing the severe DCO nonlinearity in covering the large f_0-normalized FM-BW.

References

[1] T. Buckel, T-MTT, 2018, pp. 2618. [2] N. Markulic, JSSC, 2016, pp. 3078. [3] N. Markulic, JSSC, 2019, pp. 1059. [4] G. Marzin, JSSC, 2012, pp.2974. [5] M.S. Yuan, ISSCC, 2018. [6] Z. Gao, ISSCC, 2022.

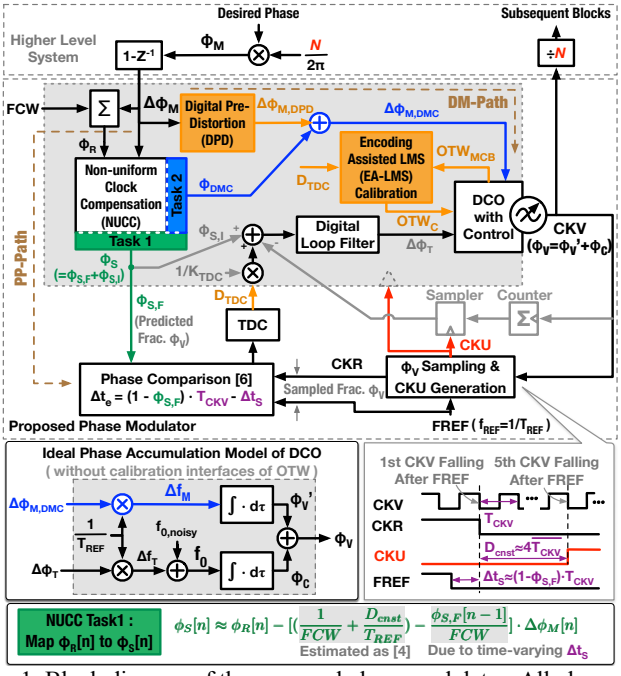

Fig. 1: Block diagram of the proposed phase modulator. All phases (with symbol ϕ) are normalized by $1/(2\pi)$.

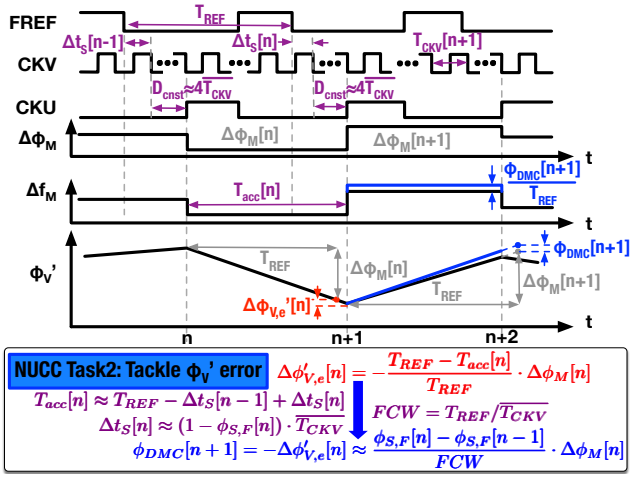

Fig. 2: Conceptual NUCC operation: estimating PM error ($\Delta\phi'_{V,e}$) due to time-variant T_{acc} and compensating it with ϕ_{DMC} in the next cycle.

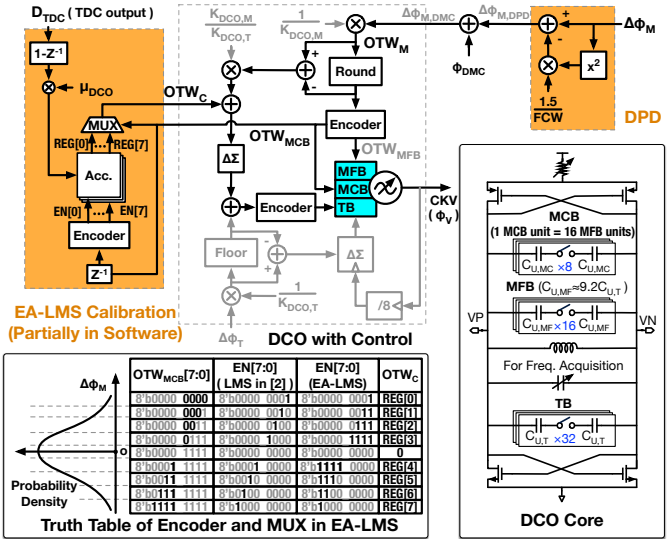

Fig. 3: DCO schematic and block diagram of its fast two-step calibration (DPD+EA-LMS).

Freq. Division Ratio (N)	DPD	EA-LMS	NUCC	EVM (dB, 64-PSK)
1	OFF	OFF	OFF	-37.1
2	OFF	OFF	OFF	-39
4	OFF	OFF	OFF	-30.6
8	OFF	OFF	OFF	-20.8
8	ON	OFF	OFF	-35.8
8	ON	ON	OFF	-43.8
8	ON	ON	ON	-46.5

Worse

Better

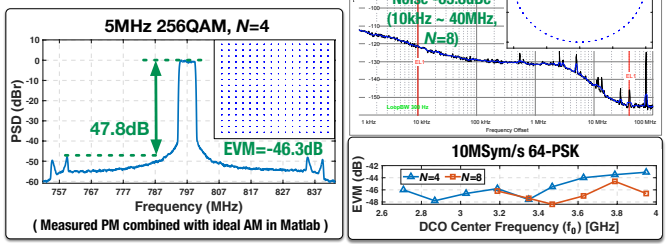

Fig. 4: Measured PM results with external frequency division ÷N.

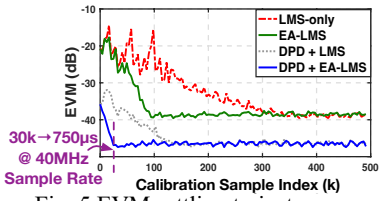

Fig. 5 EVM settling trajectory.

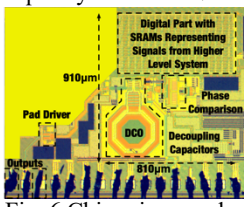

Fig. 6 Chip micrograph.

TABLE I: Comparison with the PLL-based phase modulators.

	This Work		G. Marzin JSSC' 12	N. Markulic JSSC'16	D. Cherniak SSCL' 20	Y. Liu RFIC'20	T. Buckel TMTT'18	N. Markulic JSSC'19
Modulation Type	64-PSK	256QAM[1]	QPSK	GMSK	32-PSK	GFSK	64QAM	1024QAM
DCO Freq. Range [GHz]	2.6-3.9		2.9-4.0	10.1-12.4	13.0-14.5	1.6-1.94	2.8-7.6	9.9-12.1
DCO Center Freq. (f_0)[2] [GHz]	3.188		3.6	10.24	13.75	1.81	5.1398	11
Freq. Divison Ratio (N)	8	4	1	1	1	2	2	2
Carrier Freq. [GHz]	0.399	0.797	3.6	10.24	13.75	0.905	2.5699	5.5
Data Rate [Mbit/s]	60	40	20	10	250	1	201.6	25
Ref. Freq. [MHz]	40	40	40	40	200	60	26	40
FM-BW [MHz]	176	160	40	<5	200	<1	416	≤80
FM-BW / f_0 [%]	5.52	5.02	1.11	<0.05	1.45	<0.06	8.09	≤0.71
EVM [dB]	-46.5	-46.3[1]	-36	-37.4	-42.2	-30.9	-28.7	-41.3
DCO Nonlinearity Calibration Time (ms)	0.75[3]		NA	NA	NA	NA	NA	>100
Power (mW)	4.4[4]		5	8.1	31.5	5.3	40.7[5]	17.7[5]
Energy/Bit (nJ/bit)	0.07	0.11[1]	0.25	0.81	0.13	5.3	0.2[5]	0.71[5]
IPN[6] (dBc)	-63.8	-57.8	-39	-41.7	-44.7	NA	-35.1	-47.6
Active Area (mm^2)	0.31		0.5	0.25	0.7	0.3831	2.12[5]	1.31
CMOS Process (nm)	40		65	28	28	65	28	28

1. Measured PM combined with ideal AM in Matlab (gray colored)
2. DCO center freq. in PM measurement
3. Estimated with calibration sample size
4. DCO supplied by 1.1V, the others by 1.0V
5. Including only the phase modulator part
6. Integrated phase noise (of the divided carrier)