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A Thermoelectric Energy Harvesting System Assisted by a Piezoelectric Transducer Achieving 10-mV Cold-Startup and 82.7% Peak Efficiency

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***Abstract*—This article presents a 10 mV-startup-voltage thermoelectric energy harvesting system, assisted by a piezoelectric generator (PEG) as a cold starter. It exploits the fact that when a thermoelectric energy harvesting system is implemented in a place where kinetic energy is also present, the PEG starter can provide a clock signal to start the system. Thanks to the high output impedance of the PEG, the generated clock voltage can easily go over several hundreds of mV, which can be used to drive the boost converter to harvest thermoelectric energy even at an extremely low thermoelectric generator (TEG) voltage. The proposed system was fabricated in a 180-nm BCD process. The measurement results show that the TEG system can start up from the cold state with a TEG voltage as low as 10 mV while maintaining a 63.9% efficiency. The peak power conversion efficiency reaches 83.7% when the TEG voltage is 55 mV.**

***Index Terms*—Boost converter, cold-startup, dc–dc converter, maximum power point tracking (MPPT), piezoelectric generator (PEG), thermoelectric energy generator (TEG), thermoelectric energy harvesting.**

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I. Introduction

With the rapid development of the Internet of Things (IoTs), powering techniques for electronic devices have attracted significant attention. Since the applied low-power sensors in an IoT system usually require a long operation lifetime with no battery replacement, harvesting energy from the ambient environment becomes a promising solution for the powering issue [1]. Thermal energy, RF energy, kinetic energy, and solar energy are the most common resources in the surrounding environment. Among these potential sources, thermal energy draws much interest because of its high power density and stability.

Thermoelectric energy generator (TEG) provides reliable thermal energy conversion to electrical energy. The TEG can generate an output voltage V_{TEG} when a temperature difference exists across it. The generated voltage is proportional to the temperature difference (ΔT), which can be written as

$$V_{\text{TEG}} = S \cdot \Delta T \tag{1}$$

where S is the Seebeck coefficient of the thermopile in the TEG [2].

The energy harvesting system is usually required to be small in terms of area and weight to make it compact to be integrated into an IoT system. Based on the temperature coefficient of common TEG products, which is roughly from 22 to 34 mV/K [3], [4], [5], [6], [7], a 10 cm^2 TEG with a temperature gradient between 0.5 and 2 K across it can only generate an open-circuit voltage (V_{TEG}) varying from 11 to 68 mV. Such V_{TEG} is usually much lower than the required supply voltages of the IoT electronics. Therefore, a dc–dc boost converter is needed to convert the low input voltage to a high output voltage, in a thermoelectric energy harvesting system.

In the typical implementation of a thermoelectric energy harvesting system, a cold-startup circuit is necessary to drive the dc–dc converter at the kick-off, as the V_{TEG} is even smaller than the typical threshold voltage (hundreds of mV) of a MOSFET transistor. Over the past years, different kinds of startup techniques, which require no extra battery to start the operation of the circuity, have been proposed. For instance, a mechanical switch is used in [8] to start up the circuit at a V_{TEG} of 35 mV. In [9], a one-shot cold-start technique has been proposed to generate a

single startup pulse to turn ONthe switch in the boost converter. In addition, a self-startup technique based on a low-voltage ring oscillator and a charge pump powered by V_{TEG} has been proposed, which can generate a stepping-up voltage to start up the circuit [10]. Although these designs can achieve cold-start without any battery assistance, their required startup voltages (>35 mV) are still higher than the minimum voltage (∼10 mV) that a small-area TEG can generate, thus limiting the operating range. To break through the limitations and achieve an even lower startup voltage, a new startup mechanism is proposed in this article.

The proposed thermoelectric energy harvesting system utilizes a piezoelectric starter to achieve an ultra-low startup voltage. It is worth noting that vibration and heat are generated together in many scenarios, e.g., the engines of airplanes and vehicles generate heat and mechanical vibrations, the human body generates heat together with body movements, etc. The proposed piezoelectric generator (PEG) starter can collect kinetic energy and generate an ac signal, which is then transformed into a clock signal to drive the switches in the boost converter during the startup state. Thanks to the high output impedance of the PEG, the generated signal can easily achieve several hundreds of mV or even higher, which is high enough to drive the low-side NMOS switch of a boost converter directly. The maximum power point tracking (MPPT) technique is also employed to match the converter input impedance with the TEG internal impedance, further maximizing the extracted energy and improving the power efficiency.

The rest of this article is organized as follows. Section II reviews the previous cold-startup techniques and presents the proposed piezoelectric starter. System architecture and working principle are shown in Section III. Section IV details several key circuit implementations. Section V exhibits the measurement results and compares the proposed design with state-of-the-art works. Finally, Section VI concludes this article.

II. Cold-Startup Techniques

A. Previous Cold-Startup Techniques

When a TEG experiences a near-zero temperature difference and generates little energy for a long period, the energy stored in the system may run out due to quiescent power dissipation and leakage. To let the system extract energy again when the TEG can generate more energy, a cold-startup circuitry is necessary to drive the boost converter with only a low-voltage source from the TEG. Several techniques have been proposed to fulfill this necessity.

To achieve the cold startup, Ramadass and Chandrakasan [8] presented a thermoelectric energy harvesting system for wearable applications with a starter that takes advantage of the movement of the human body. Body movements trigger a mechanical switch S0 in the startup circuit, as shown in Fig. 1. After several mechanical movement periods, energy can be stored in a capacitor to build a high voltage to drive switches in the boost converter. After that, this mechanical switch is disabled, and the internal oscillator can generate a much faster clock signal to extract energy from TEG with a higher efficiency.

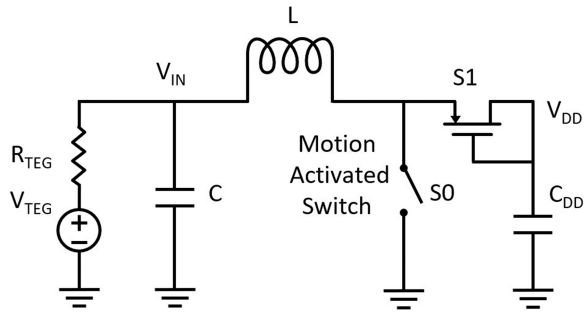

Fig. 1. Schematic of the startup circuit with the assistance of a mechanical switch [8].

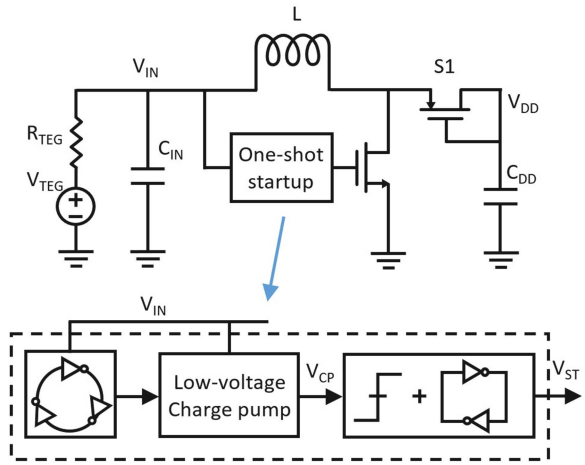

Fig. 2. Schematic of the one-shot startup technique based on a low-voltage charge pump [9].

In [9], a one-shot cold-startup technique is adopted for self-start. As shown in Fig. 2, during the cold-startup operation, a charge-pump-based on-chip voltage multiplier boosts the input voltage V_{IN} to a high voltage of V_{CP}. Thanks to the use of low-threshold voltage transistors, the voltage multiplier can be driven by a low-voltage ring oscillator directly powered by V_{IN}. A single startup strobe pulse, V_{ST}, is then generated by V_{CP}. During this short duration, the inductor is charged with the current from TEG. At the end of the startup pulse, the PMOS diode S1 is turned ON to transfer the power from the inductor to the on-chip capacitor, C_{DD}, generating a voltage V_{DD} higher than 500 mV to power a secondary oscillator to clock the entire system. The minimum self-startup voltage of this design is 50 mV due to the limitation of the threshold voltage of transistors in the low-voltage oscillator.

Fig. 3 shows the architecture of the low-voltage starter proposed in [10]. It consists of an LC-tank oscillator and a voltage multiplier. First, the oscillator converts the input dc energy into an ac signal. Then, a voltage multiplier transfers the ac energy back to dc with a boosted level. Unlike the one-shot design in [9], this work directly charges the output capacitor during the startup state instead of driving the boost converter to charge the intermediate storage capacitor, simplifying the system. However, the minimum start-up voltage of 50 mV is

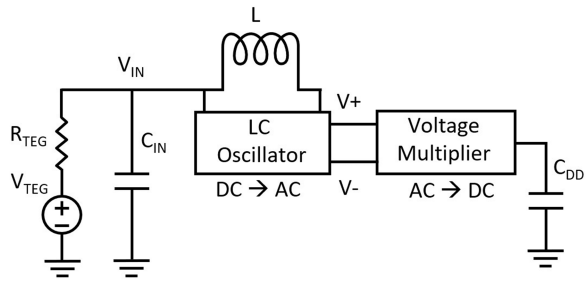

Fig. 3. Schematic of the low-voltage starter based on an *LC* oscillator and a voltage multiplier [10].

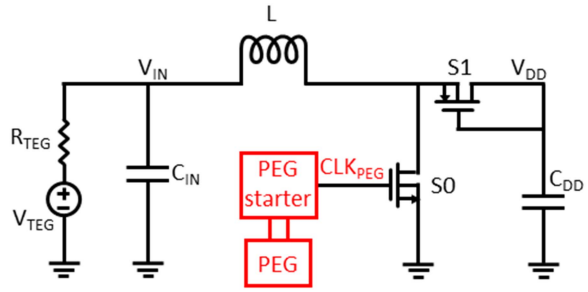

Fig. 4. Schematic of the proposed thermoelectric energy harvesting system with a PEG cold-starter.

still limited by the threshold voltage of the transistors in the oscillator.

B. Proposed Low-Voltage PEG Starter

By exploiting either kinetic energy or ac–dc energy conversion, the previous cold-startup designs achieve low start-up voltages around several tens of mV, which is still higher than the minimum voltage (∼10mV) that a compact TEG can provide. To further break the startup-voltage bottleneck, this work combines both TEG and PEG mechanisms, as shown in Fig. 4. It takes advantage of the kinetic energy collected by the PEG to generate a startup clock signal, $\mathrm{CLK_{PEG}}$, which is used to drive the boost converter to work at an extremely low V_{TEG} and store harvested thermal energy into a capacitor in the cold state.

To utilize the ac energy generated by the PEG, a full-bridge rectifier is employed to convert the ac input into a dc voltage, V_{PEG}, as shown in Fig. 5(a). As the PEG has an internal capacitor, which is charged and discharged periodically due to kinetic vibration, the polarity of IN+ and IN− is also reversed periodically [11]. To directly generate a clock signal from this flipping voltage IN+, four cascaded inverters powered by V_{PEG} are employed to reshape the PEG output to a square wave ($\mathrm{CLK_{PEG}}$), as shown in Fig. 5(b). Although the output of the inverter is not a perfect square wave due to the fluctuation in the supply, the falling edge is sharp enough to turn OFF the low-side NMOS in the boost converter in a short instant without reducing the current in the inductor too much.

Assuming that the proposed energy harvesting system is mounted on a surface with a vibration frequency of f_{PEG}, the input resistance of the boost converter in the startup state is

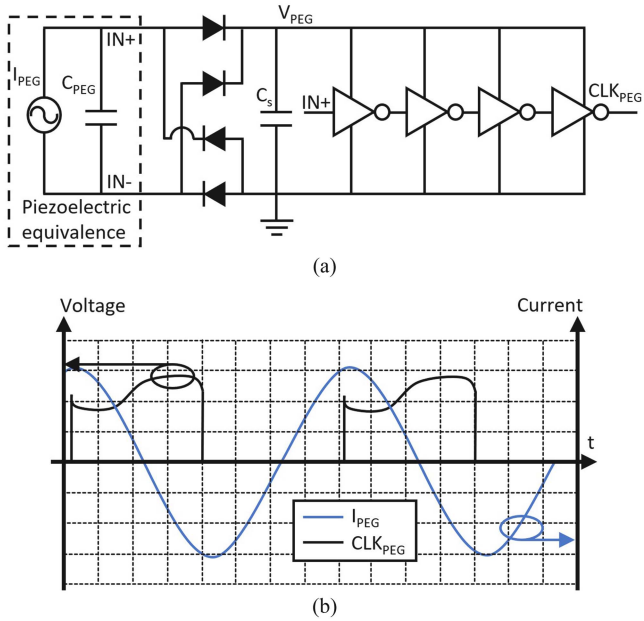

Fig. 5. PEG startup block and its waveforms. (a) Circuit diagram of the PEG startup block. (b) Associated waveform in two periods.

given as [12]

$$R_{\mathrm{IN,startup}} = \frac{2Lf_{\mathrm{PEG}}}{D^2} \tag{2}$$

where L is the value of the inductor and D is the duty cycle of the NMOS switch $S0$ (see Fig. 4). Then, the input power of the energy harvesting system can be rewritten as

$$P_{\mathrm{IN,startup}} = \frac{2Lf_{\mathrm{PEG}}V_{\mathrm{TEG}}^2D^2}{(2Lf_{\mathrm{PEG}} + R_{\mathrm{TEG}}D^2)^2} \tag{3}$$

where R_{TEG} and V_{TEG} are the TEG's internal resistance and generated voltage, respectively. The system will not harvest thermoelectric energy with the self-generated clock until the voltage on C_{CTRL} (the internal power supply capacitor) is charged to $V_{\mathrm{CTRL,min}}$, which is the lowest voltage ensuring a proper system operation. The lowest required energy is derived as

$$E_{\mathrm{startup}} = \frac{1}{2}C_{\mathrm{CTRL}}V_{\mathrm{CTRL,min}}^2 = P_{\mathrm{IN,startup}}t_{\mathrm{startup}} \tag{4}$$

where t_{startup} is the time of the startup state. Based on (3) and (4), the minimum startup V_{TEG} can be formulated as

$$V_{\mathrm{TEG,min}} = \sqrt{\frac{C_{\mathrm{CTRL}}V_{\mathrm{CTRL,min}}^2}{2t_{\mathrm{startup}}} \cdot \frac{(2Lf_{\mathrm{PEG}} + R_{\mathrm{TEG}}D^2)^2}{2Lf_{\mathrm{PEG}}D^2}}. \tag{5}$$

By setting the f_{PEG} as the only variable while the other parameters are constant, the simulated relation between the minimum TEG voltage (V_{TEG}) for startup and the frequency of the clock signal generated by the PEG starter ($\mathrm{CLK_{PEG}}$) is shown in Fig. 6. With a vibration frequency higher than 200 Hz, the minimum startup voltage can be lower than 10 mV.

Compared with the designs that only use vibration to drive mechanical switches, this work can control the startup process more subtly. Moreover, the proposed technique allows the startup circuit to overcome the limitation of the minimum startup

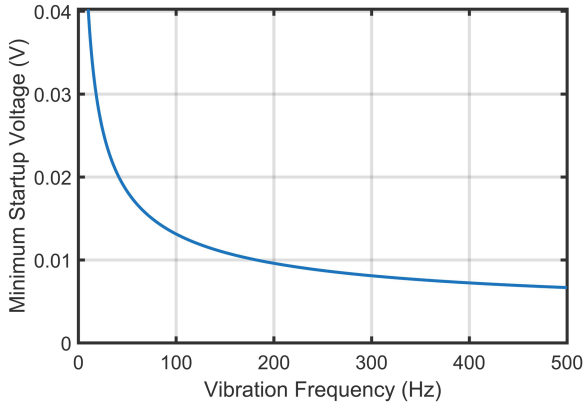

Fig. 6. Minimum TEG voltage for the startup versus the vibration frequency generated by the PEH starter.

voltage of the transistor, compared with the works that use a ring oscillator in the startup circuit. Furthermore, the startup block is solely powered by the harvested kinetic energy during the startup state. All the harvested energy from the thermoelectric source can be stored without sharing any portion with the startup clock generation, further lowering the required minimum startup V_{TEG}.

III. Proposed TEG Energy Harvesting System

A. System Architecture

The architecture of the proposed TEG harvesting system is presented in Fig. 7. It comprises a TEG-based power converter, a PEG-based cold startup circuit, and several control blocks. The TEG can be modeled as a voltage source V_{TEG} in series with an internal resistor R_{TEG}. During the startup period, the PEG starter provides the initial switching signal to drive the boost converter to achieve a sufficiently high V_{CTRL} from a low V_{TEG} until the control blocks can start operating autonomously. The converter stores the harvested energy into two capacitors, C_{OUT} and C_{TRL}. C_{CTRL} provides the supply voltage, V_{CTRL}, for the internal control circuits, and C_{OUT} is used to generate a supply voltage, V_{OUT}, for the external loads.

The control circuits are mainly composed of a state detection block, an MPPT block, a voltage-controlled oscillator (VCO), a zero-current switching (ZCS) block, and a low-dropout regulator (LDO). The voltage dividers in the state detector provide the divided versions of V_{CTRL} and V_{OUT}. By comparing them with a voltage reference, the state detection block can generate signals instructing the system to work in different operation states. More details about the operation states will be given in the next section. The MPPT and VCO blocks adjust the gate-driving signal of switch $S0$ and the system operating frequency according to the variation of V_{TEG}, thus ensuring the interface circuit collects power as much as possible from the TEG. The ZCS block detects the polarity of the current in the paths having switches $S1$ and $S2$. By turning OFF the conduction path precisely at the polarity reversing point, the circuit avoids the reverse current draining energy from the power supply capacitor; it also avoids the positive current being wasted because of the early cutting-off.

B. Operation Principle

The system has four operation states, which are cold-start state, internal-charging state, external-charging state, and output state, respectively. Fig. 8(a) shows the state transition flow with conditions. When the system starts from the cold-start state, V_{CTRL} is charged until it reaches about 0.6 V. After that, the internal oscillator can be powered to generate a much faster clock than that from the PEG starter. This state will continue to charge V_{CTRL} until it reaches 1.3 V, after which the system enters the output state to provide a stable output voltage V_{OUT} to the loads. The first three states, i.e., cold-start state, internal-charging state, and external-charging state, are counted as the cold-startup period of the system. In the output state, the system powers the external loads steadily.

As shown in Fig. 8(b), the system starts from the cold state without external battery assistance and any energy stored in the system. During this period, all the control circuits are in idleness. Triggered by ambient vibration, the PEG stater starts to generate the clock signal, CLK_{PEG}, to drive the low-side switch, $S0$. With a temperature difference across the TEG which induces a V_{TEG} higher than the minimum startup voltage, the inductor starts to be energized. After $S0$ turns OFF, the energy stored in the inductor is transferred to C_{CTRL} and C_{OUT} through the high-side switches, $S1$ and $S2$. Since the ZCS block cannot control the gate switching of $S1$ and $S2$ during the cold state, both transistors work as diodes. In this state, the PEG starter helps the converter collect energy from the TEG, establishing an increasingly high supply voltage for the control circuits. Once the V_{CTRL} increases to 600 mV, the system transitions from the cold-start state to the internal-charging state.

As the system enters the internal-charging state, the PEG starter will be disabled, and the ZCS block, the MPPT block, and the VCO start operating, as shown in Fig. 8(c). These control circuits are powered by V_{CTRL}. The MUX on the gate of $S0$ selects the switching clock, $S0_G$, generated by the MPPT block to optimize the operation of the boost converter. In this state, the boost converter accelerates the charging process of C_{CTRL} as the switching frequency of $S0_G$ is much higher than that of CLK_{PEG}. Also, the switch $S1$ works more efficiently with the driving signal generated by the ZCS block than working as a diode. Moreover, the boost converter operates in the discontinuous conduction mode (DCM) as the power harvested from the TEG is low [13]. The ZCS block dynamically adjusts the on-time of $S1$ to prevent reverse currents.

The state detection block monitors the level of V_{CTRL}. As soon as V_{CTRL} reaches 1.3 V, the system enters the external-charging state, and all control blocks are enabled, as shown in Fig. 8(d). Another energy harvesting path through the high-side switch $S2$ is activated in this state, and the energy harvested from the TEG is transferred to the output capacitor C_{OUT}. It should be noticed that the amplitude of V_{CTRL} is influenced by the operation of the boost converter in two aspects. On the one hand, the harvested energy is used to charge C_{OUT}, meaning there is no energy delivered to C_{CTRL} in some cycles. On the other hand, the control circuits keep consuming the energy stored in C_{CTRL}. As a result, V_{CTRL} can drop slowly. As C_{CTRL} provides energy

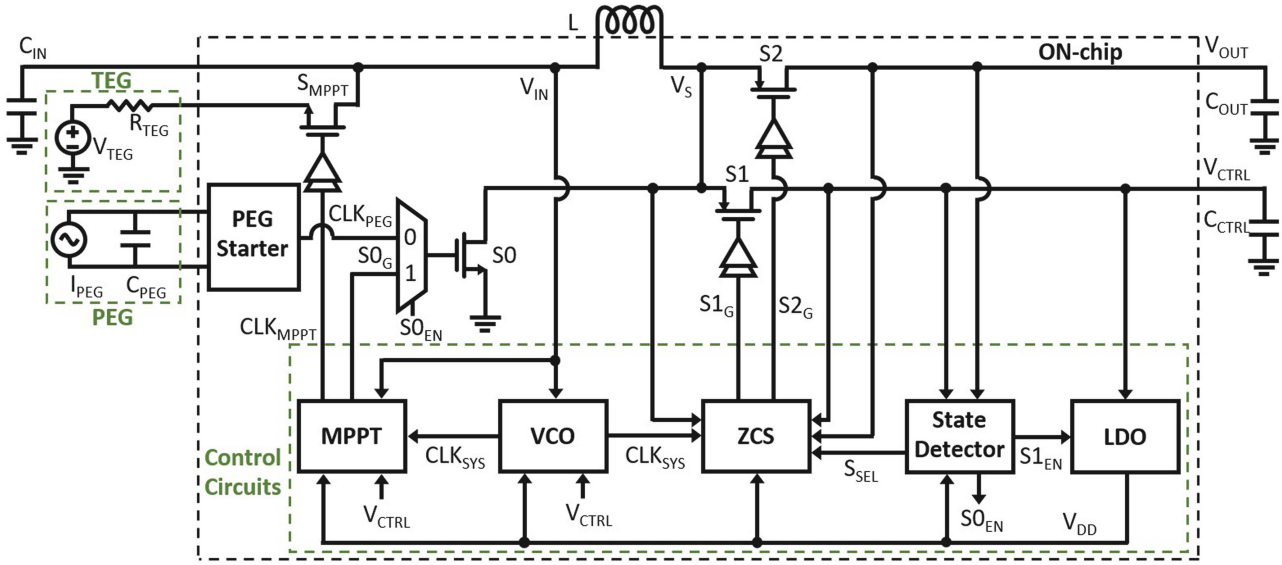

Fig. 7. Architecture of the proposed TEG energy harvesting system.

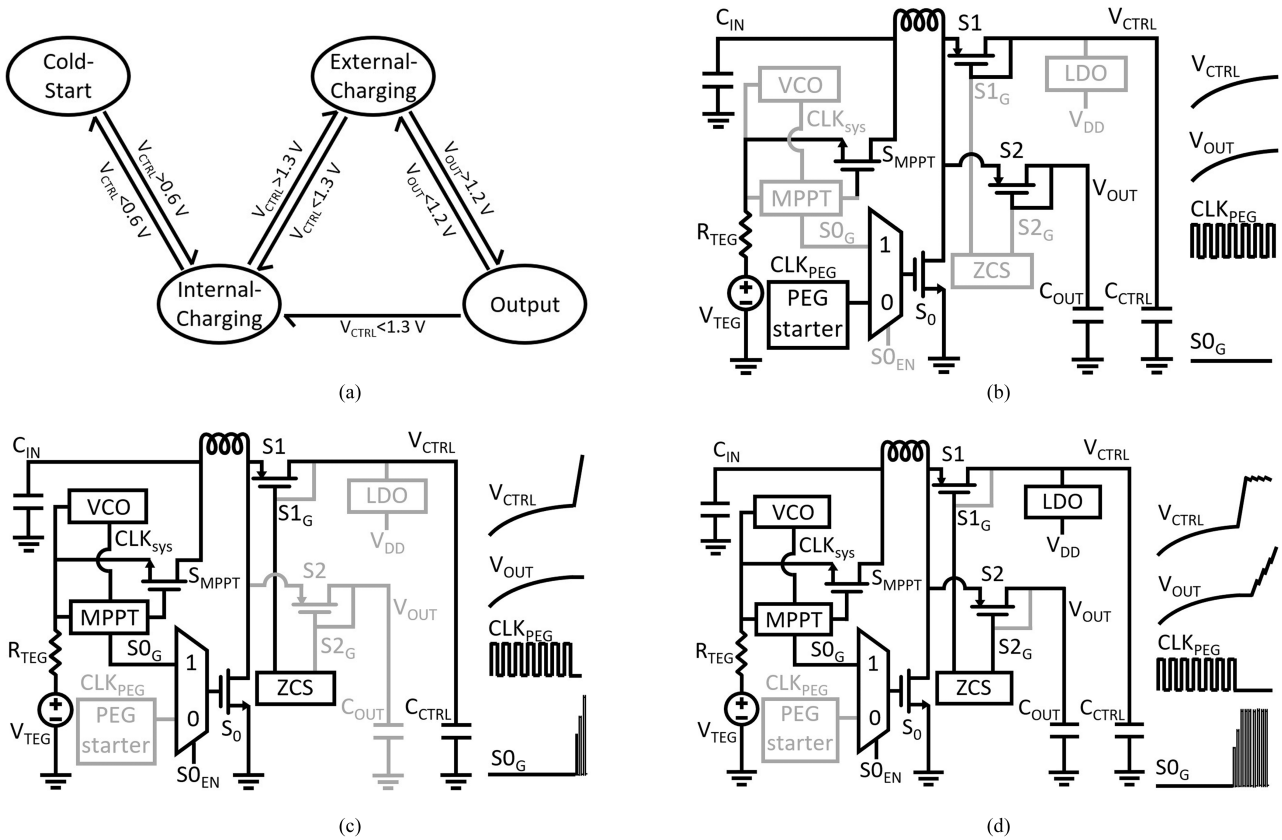

Fig. 8. Illustrated states of operation of the energy harvesting system. (a) States transition flow. (b) Cold-start state. (c) Internal-charging state. (d) External-charging state.

for all the internal circuits, it should have the priority to maintain V_{CTRL}. Consequently, once V_{CTRL} drops below 1.3 V, the energy harvesting path through $S2$ will be turned OFF temporarily, and $S1$ will be activated to charge C_{CTRL} until V_{CTRL} backs to 1.3 V. To avoid the impact of the fluctuation of V_{CTRL} on powering internal control circuits, an LDO is employed to generate a stable supply, V_{DD}, of 1.2 V for the internal circuits. Moreover, the dynamic bulk biasing technique connects the bodies of $S1$ and $S2$ to a higher potential port between their source and drain.

Finally, as V_{OUT} goes above 1.2 V, the system enters output mode. In this state, the switches $S1$ and $S2$ are turned ON alternately to ensure that the V_{CTRL} stays around 1.3 V, and the

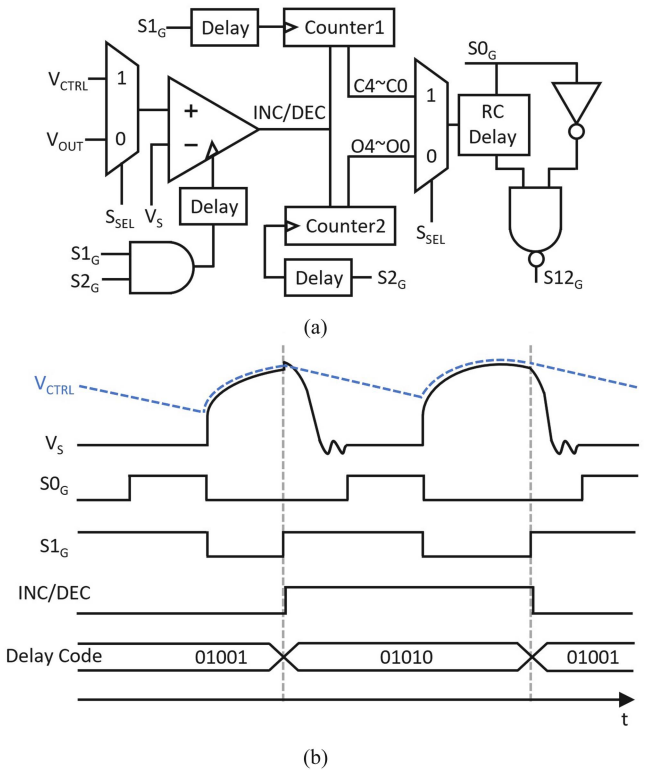

Fig. 9. ZCS block. (a) Circuit implementation. (b) Timing diagram of the DCM operation.

output port can provide a stable 1.2-V supply. When V_{CTRL} goes below 1.3 V, the system will switch to charge V_{CTRL} because it is the supply for the entire energy harvesting system. If the V_{TEG} is fluctuating and the harvested power is lower than that required by the external loads, the energy stored in the C_{OUT} will decrease, and V_{OUT} will drop. As V_{OUT} drops below the preset threshold voltage 1.2 V, the system will switch back to the external-charging state to recover V_{OUT}. In extreme cases where the input power remains insufficient, the V_{CTRL} may also drop. When V_{CTRL} decreases below 600 mV, the system will enter the cold-start state again.

IV. Key Circuit Implementations

A. Zero-Current Switching

As the proposed boost converter operates in the DCM, a ZCS circuit is required, as illustrated in Fig. 9(a). To sense the polarity of the current flowing through the inductor, a comparator is used to compare the voltages on the drain and the source of the conducting PMOS switch, $S1$ or $S2$. It is important to note that two PMOS switches work for two different energy storage capacitors. Therefore, a MUX chooses either V_{CTRL} or V_{OUT} to be one of the inputs of the comparator, which is selected by the state signal, S_{SEL}. The other input of the comparator is connected to the common terminal of $S1$ and $S2$, V_S. In each cycle, the comparator generates a polarity indicating signal, INC/DEC, based on the polarity of the voltage drops on the conducting PMOS switch. The comparator is triggered by a delayed version of the PMOS gate switching signal, either $S1_G$ or $S2_G$. This delayed trigger plays two roles in the operation of the comparator. On the one hand, V_S exhibits either an overshoot or an undershoot corresponding to the polarity of the current at the PMOS turn-OFF moment. Thus, a small time slot is necessary to settle the V_S after the rising edge of the gate-switching signal. On the other hand, the comparator needs a setup time when both inputs are settled. To achieve zero-voltage sensing (ZVS), the ON-time of $S1$ or $S2$ is defined by a 5-bit programmable delay cell (RC Delay), whose output, $S12_G$, can go to either $S1$ or $S2$. The 5-bit delay cell is controlled by 5-bit counters, Counter_1 and Counter_2, whose up/down behavior is controlled by the polarity indicating signal, INC/DEC. Therefore, the two counters store the delay codes for the gate-switching signals, where the delay codes are adjusted to achieve the ZVS. Each unit cell in the 5-bit delay cell can generate a delay of 35 ns.

As depicted in Fig. 9(b), at the first rising edge of $S1_G$, an overshoot appears at V_S because of the accumulation of positive charges delivered by the residual forward inductor current. Hence, a positive INC/DEC signal is generated. Then, the corresponding counter, Counter_1, is adjusted to enlarge the ON-time of the corresponding PMOS switch, $S1$, by tuning the 5-bit programmable delay cell. In contrast, an undershoot at V_S indicates that a negative current is flowing in the inductor at the moment that $S1$ is turned OFF. The ZCS block will then shorten the ON-time of $S1$ to avoid the reverse current discharging the output capacitor, C_{CTRL}, in the next cycle. In steady states, the delay code of the programmable delay cell will switch between two adjacent values with near-optimal switching behavior of $S1$. A similar ZCS operation applies when the system is charging C_{OUT} using $S2$.

B. Maximum Power Point Tracking

According to the equivalent circuit of the TEG and the MPPT theory [2], [12], [14], the maximum power can be extracted from TEG when the input resistance of the dc–dc converter, R_{IN}, is equal to the internal resistance of the TEG, R_{TEG}. The theoretical maximum extractable power from TEG can be expressed as

$$P_{\text{HAR,MAX}} = \frac{V_{\text{TEG}}^2}{4R_{\text{TEG}}}. \tag{6}$$

Since the converter works in the DCM with a high voltage conversion ratio, the ON-time of the PMOS switch is negligible compared with the ON-time of the NMOS switch. Thus, R_{IN} can be given by [15]

$$R_{\text{IN}} = \frac{2Lf_{\text{sys}}}{D^2} \tag{7}$$

where f_{sys} is the system switching frequency. Therefore, using (6) and (7), the MPPT efficiency, η_{MPPT}, can be written as

$$\eta_{\text{MPPT}} = \frac{8R_{\text{TEG}}Lf_{\text{sys}}D^4}{(2Lf_{\text{sys}} + R_{\text{TEG}}D^2)^2}. \tag{8}$$

Based on (6), the input voltage of the converter should be maintained equal to half of V_{TEG} to achieve the maximum extractable power from TEG. Also, (7) points out that the value of R_{IN} depends on D for a given f_{sys}. Therefore, MPPT can be

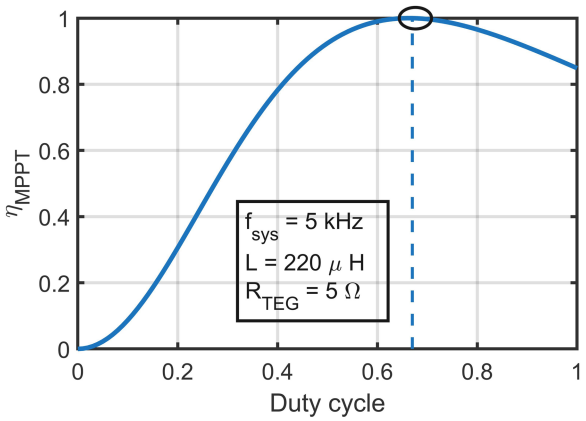

Fig. 10. MPPT efficiency versus duty cycle with a fixed f_{sys}.

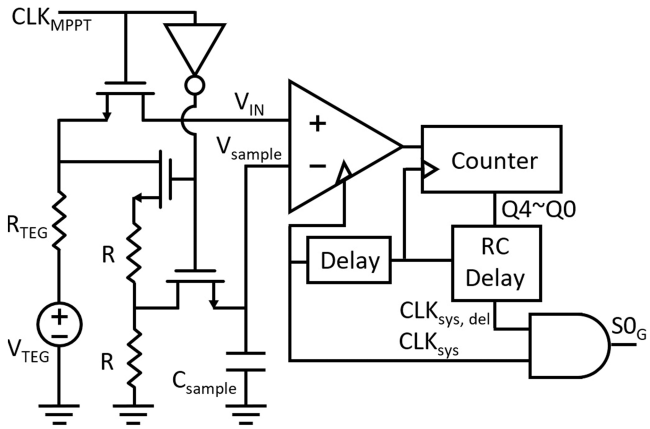

Fig. 11. Circuit implementation of the MPPT block.

achieved by tuning D. For instance, for a fixed system frequency, $f_{sys} = 5$ kHz, the optimal MPPT efficiency is achieved by tuning D around 0.67, as shown in Fig. 10. A sample-and-hold circuit is utilized to periodically sample the halved version of V_{TEG} on C_{sample} ($V_{sample} = 1/2V_{TEG}$), as shown in Fig. 11. The V_{sample} is then compared with V_{IN} to determine the ON-time of the switch $S0$. If V_{IN} is larger than $1/2V_{TEG}$, which means R_{IN} is larger than R_{TEG}, a pulse signal will be generated at the comparator output, which will be counted in the 5-bit counter. Consequently, the programmable delay cell (RC delay) increases the delay between CLK$_{sys}$ and CLK$_{sys,del}$. Thus, the D increases, and R_{IN} can decrease based on (7). Similarly, the programmable delay cell decreases the delay to decrease D when V_{IN} is smaller than $1/2V_{TEG}$.

Since the converter works in the DCM and there is no energy transfer when the PMOS switches disconnect the energy harvesting path, the operation of the MPPT is arranged during the disconnection period to avoid disturbing the energy harvesting process. Moreover, the sample-and-hold circuit samples $1/2$ V_{TEG} for every 64 system cycles (CLK$_{MPPT}$) as the temperature on TEG only changes gradually. In contrast, the comparison between V_{IN} and V_{sample} takes place for every cycle so that R_{IN} follows the change of R_{TEG} and the system tracks the maximum power point timely. Besides, the MPPT block is activated once

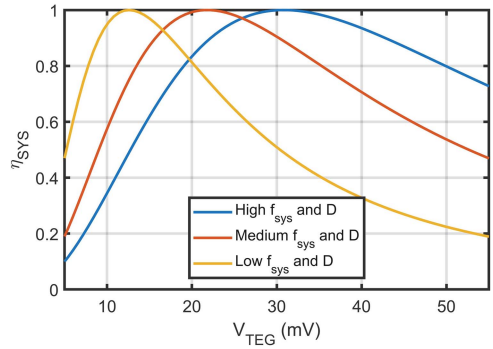

Fig. 12. System overall efficiency versus the TEG voltage, with different f_{sys} and D.

the system enters the internal-charging state, which facilitates the setup of V_{CTRL} and V_{OUT}.

C. Voltage-Controlled Oscillator

With an ideal MPPT block, the input resistance of the harvester should match the TEG internal resistance, $R_{IN} = R_{TEG}$. Thus, the system's overall efficiency can be expressed in terms of D and f_{sys} as

$$\eta_{SYS} = \frac{4(R_N + \frac{V_{IN}}{V_{OUT}} R_P)}{3R_{TEG}} \frac{1}{D} + \frac{C_G V_{OUT}^2 R_{TEG}}{V_{IN}^2} f_{sys} \quad (9)$$

where R_N and R_P are the ON-resistances of the NMOS and PMOS switches, respectively. Equation (9) demonstrates that for different values of V_{IN}, different kinds of losses can dominate. For example, if V_{TEG} is at an extremely low level (e.g., $10 - 30$ mV), the switching loss becomes the dominating loss. To reduce the converter loss while keeping the input matched as derived in (7), a smaller f_{sys} together with a reduced D can effectively reduce the switching loss and improve the system efficiency, as shown in Fig. 12. The decrease in D does not induce too much conduction loss because of the low V_{IN}.

As the V_{TEG} increases, the previous set of D and f_{sys} becomes no longer appropriate for minimizing power losses, as shown in Fig. 12. This is because the conduction loss starts to dominate. Consequently, a larger value of D together with a proportional increased f_{sys} is beneficial to decrease the conduction loss while maintaining the input resistance matched. The increase in frequency does not increase the switching loss as a percentage since V_{IN} is large.

A relation between V_{TEG} and f_{sys} can be found that as V_{TEG} increases, the f_{sys} also increases. Meanwhile, D and f_{sys} follow the (7) for MPPT. As described in [16], the optimal switching frequency is nearly proportional to $V_{TEG}^{4/3}$. Instead of making a sophisticated circuit design to satisfy the subtle relation, $f_{sys,optimal} \propto V_{TEG}^{4/3}$, a tradeoff is made to reduce the circuit complexity and maintain the high efficiency of the converter by simplifying it to $f_{sys,optimal} \propto V_{TEG}$.

The implementation of the VCO is shown in Fig. 13. It mainly consists of two parts: a biasing current generator and a ring oscillator. The amplifier and its feedback loop make up a voltage-to-current converter. The converted current is V_{TEG}/R, which is

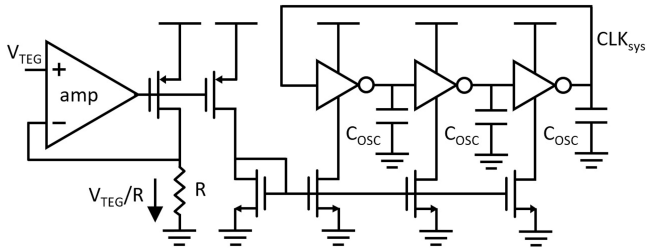

Fig. 13. Circuit implementation of the VCO.

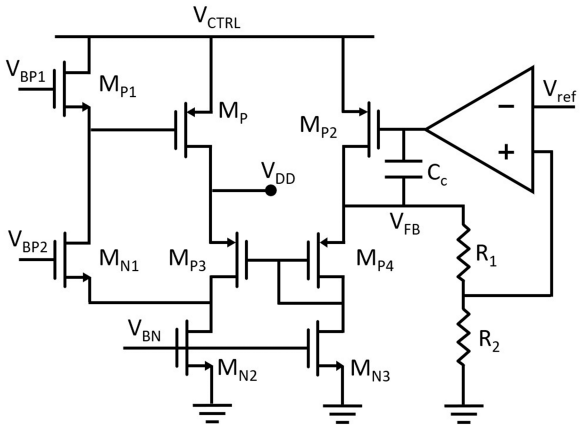

Fig. 14. Circuit implementation of the LDO.

replicated by a current mirror to bias the ring oscillator. Thus, the frequency of $\mathrm{CLK_{SYS}}$ is proportional to the biasing current, which can be expressed as

$$f_{\mathrm{sys}} = \frac{V_{\mathrm{TEG}}}{RC_{\mathrm{OSC}}V_{DD}} \tag{10}$$

where C_{OSC} is the capacitance in the oscillator.

D. Low-Dropout Regulator

The implementation of the LDO is shown in Fig. 14. M_P, M_{N1}, and M_{P3} form the core of the LDO. The bias currents in M_{N2}, M_{N3}, and M_{P1} are set to be 2:1:1 so that the two identical transistors M_{P3} and M_{P4} will have the same V_{GS}. Therefore, the output voltage of the LDO can be expressed as

$$V_{DD} = V_{FB} = \left(1 + \frac{R_1}{R_2}\right) V_{\mathrm{ref}} \tag{11}$$

where R_1 and R_2 form a resistive voltage divider of V_{FB}. The error amplifier is implemented with a single-stage differential pair to lower the power dissipation.

V. Measurement Results

The thermoelectric energy harvesting system was designed and fabricated in a 180-nm BCD process. A die micrograph is shown in Fig. 15 (VRG: voltage reference generator). The proposed system occupies an active area of $0.4\ \mathrm{mm}^2$. Fig. 16 shows the experimental measurement setup. The off-chip components consist of a 220 μH inductor, L, with an internal resistance of 0.3 Ω, an 84 MΩ resistor (for LDO), a 40 MΩ

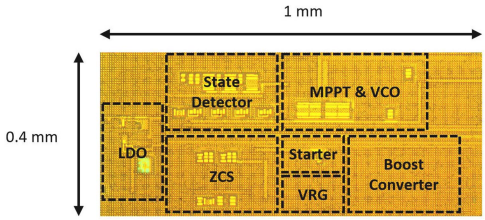

Fig. 15. Die micrograph of the proposed system.

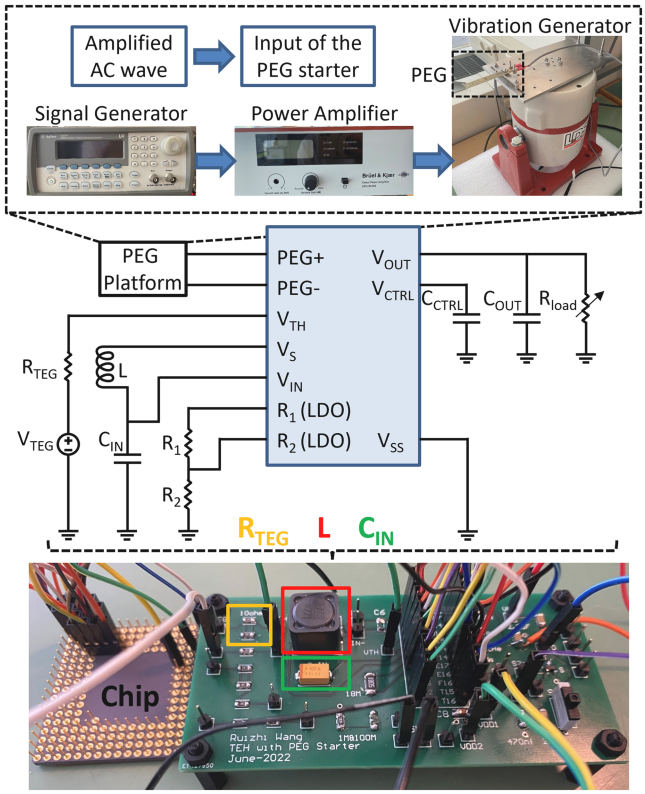

Fig. 16. Measurement setup.

resistor (for LDO), and several buffer capacitors. The TEG is mimicked by a dc voltage source (MX180TP) in series with a 5Ω resistor. A piezoelectric energy generation platform (PEG Platform) that vibrates the piezoelectric material (part number: S129-H5FR-1803YB) is used to provide the input of the PEG starter, which has an open-circuit voltage amplitude of 1.8 V and a frequency of 280 Hz. The PEG platform includes a signal generator (Agilent 33220 A), a power amplifier (LDS LPA100), and a vibration generator (LDS V406). The measurement results were extracted from a digital oscilloscope (RTB2004).

Fig. 17 shows the key signals during the cold startup of the system. The achieved minimum V_{TEG} for cold-startup is 10 mV. It takes about 2.36 s for the whole system to start from a zero-energy-stored state to a normal-output state. The startup time mainly depends on three factors. One is the capacitance of the energy storage capacitor. The larger the capacitance is, the longer it takes to reach the required voltage. Another major factor is the input power. At the minimum startup voltage, the system can only harvest a small amount of power from the

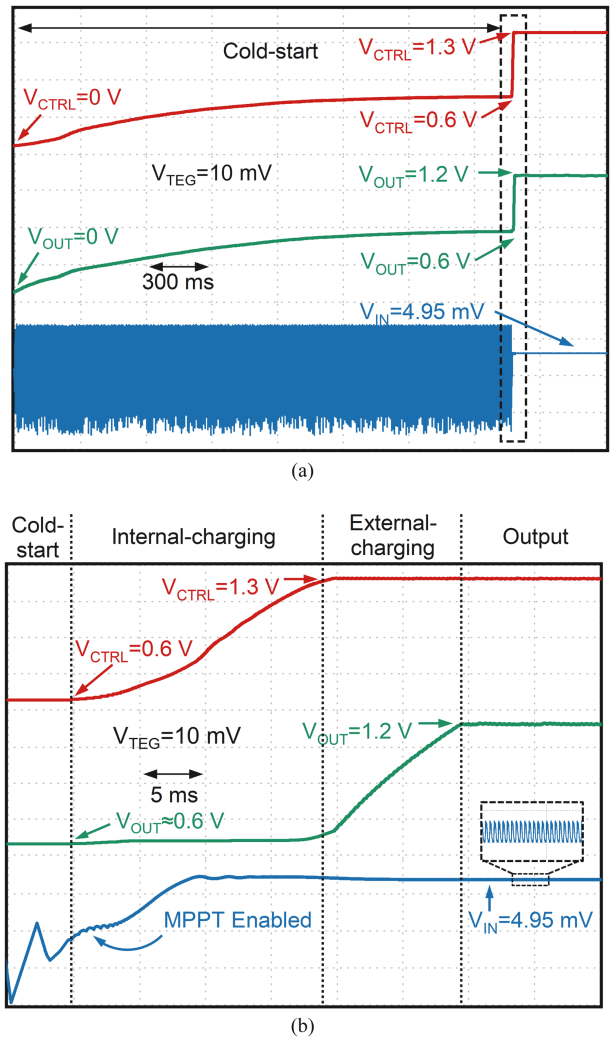

Fig. 17. Measured startup waveform at $V_{\mathrm{TEG}} = 10$ mV. (a) Full waveforms from the cold state to the normal operation state. (b) Zoomed-in waveforms showing the details of the internal-charging and external-charging state.

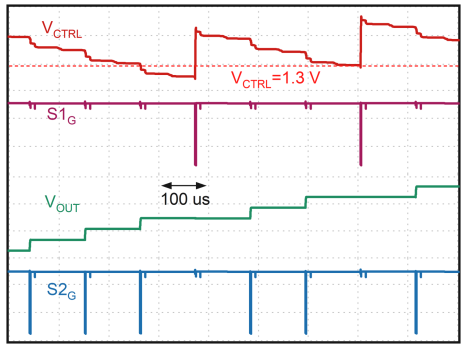

Fig. 18. Measured gate switching signals, $S1$ and $S2$, in the external-charging state.

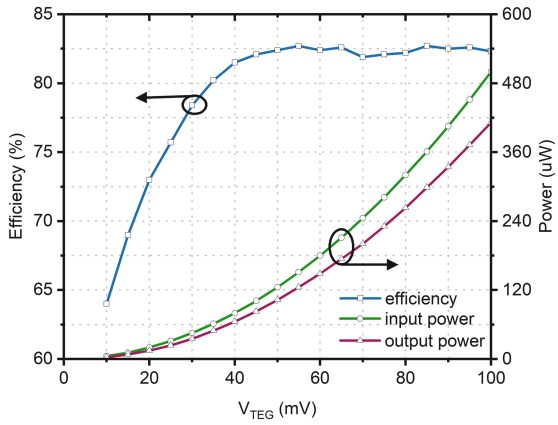

Fig. 19. Measured power efficiency and output power of the system versus the TEG voltage.

TEG. Therefore, the startup state takes a longer time. The last factor is the frequency of vibration. A higher vibration frequency promotes that the gate-driving signal has a higher switching frequency, which means the system can extract energy faster from the TEG.

In the cold-start state, only the PEG startup circuit works. As shown in Fig. 17(a), this state takes the longest time during the startup period, even though there is no active power consumption in the circuit. The low switching frequency and high voltage drop on the PMOS diode impede the rising speed of V_{CTRL}. The short startup period in the dotted box is zoomed in for a better explanation in Fig. 17(b).

As V_{CTRL} goes over 600 mV, the system enters the internal-charging state, as shown in Fig. 17(b). The PEG starter is no longer used in this state, and the system clock is generated from the internal oscillator (VCO). The MPPT block stabilizes the input voltage of the inductor, V_{IN}, at half of V_{TEG}. The involvement of MPPT maximizes the extractable power from the TEG source and reduces the time spent in this state.

Once V_{CTRL} reaches 1.3 V, it stops increasing and is regulated by the ON–OFF control of the ZCS block. During the external-charging state, the output voltage V_{OUT} keeps rising until it reaches 1.2 V. Eventually, in the output state, the output voltage, V_{OUT}, is regulated at 1.2 V.

Fig. 18 shows the gate-switching strategy of $S1$ and $S2$ in the external-charging state (which also applies to the output state). When the V_{CTRL} is higher than 1.3 V, all the harvested energy is transferred to the output capacitor. With each pulse of $S2_G$, the V_{OUT} increases step by step. Since V_{CTRL} is the power supply of the internal control circuit, it has the priority to be maintained at a certain level. Once V_{CTRL} drops below 1.3 V, $S2$ will be disabled temporarily. During this instant, $S1$ can transfer the harvested energy to C_{CTRL} and boost V_{CTRL}. Once V_{CTRL} surpasses 1.3 V, $S2$ will be enabled again and resume charging V_{OUT}.

The measured overall power conversion efficiency in a range of V_{TEG} is shown in Fig. 19. It is worth noting that the harvester can not only achieve the cold startup at an ultra-low V_{TEG} of 10 mV but also achieve an efficiency of 63.9% at this extremely low V_{TEG}. The peak efficiency of 82.7% is achieved at $V_{\mathrm{TEG}} = 55$ mV. For V_{TEG} larger than 35 mV, the overall efficiency is maintained over 80%. Fig. 20 shows the power distribution of the proposed system at $V_{\mathrm{TEG}} = 10$ mV.

The comparison of the performance with state-of-the-art works is given in Table I. Among all of the designs, this work

TABLE I
COMPARISON WITH STATE-OF-THE-ART WORKS

	[8]	[17]	[10]	[18]	[19]	[20]	[16]	[9]	[21]	**This Work**
Process	0.35 μm	N/A	65 nm	N/A	65 nm	65 nm	0.18 μm	0.18 μm	0.13 μm	**0.18 μm**
R_{TEG}	5 Ω	2 Ω	6.2 Ω	1 $\Omega \sim$ 5 Ω	2.2 Ω	5 Ω	210 Ω	5 Ω	200 Ω	**5 Ω**
# of inductors	2	2	3	1	2	1	1	1	1	**1**
MPPT	YES	NO	YES	YES	YES	YES	YES	YES	YES	**YES**
Adaptive Frequency	NO	N/A	YES	N/A	NO	YES	YES	YES	YES	**YES**
Peak efficiency	58%	55%	73%	68%	75%	71.5%	84%	80%	90%	**82.7%**
Startup Mechanism	Mechanical Switch	Resonant Oscillator	Charge Pump	Meissner Oscillator	10-stage volt. multiplier	3-stage charge pump	Charge Pump	One-shot	Charge Pump	**PEG Starter**
Min. Startup Voltage	35 mV	30 mV	50 mV	40 mV	40 mV	210 mV	129 mV	50 mV	140 mV	**10 mV**
Efficiency @ Min. V_{TEG}	N/A	37%	45%	43%	12%	50%	23%	58%	29%	**63.9%**

The bold values highlight the results from this work, to be distinguished from the prior arts for a clear comparison.

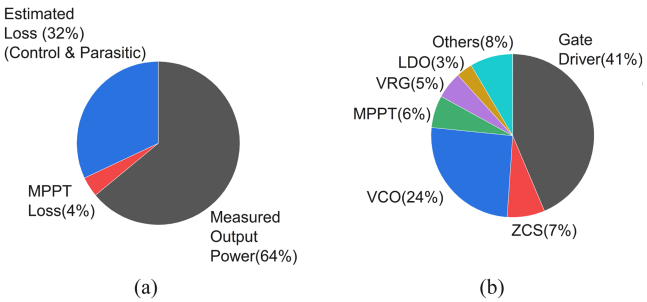

Fig. 20. System power distribution at $V_{\text{TEG}} = 10$ mV. (a) Measured output power with estimated loss. (b) Post-layout simulated chip power breakdown with a total power consumption of 1.6 nW.

achieves the lowest cold-start voltage at 10 mV, while other designs need at least 35 mV. In terms of the efficiency at the lowest cold-startup voltage, prior designs generally achieve around 40%, while this work reaches an efficiency of 63.9%, the highest value. The peak efficiency is achieved at 82.7%. The performance improvements regarding the cold-startup voltage and power efficiency are achieved with the help of the proposed PEG starter. Unlike state-of-the-art multi-input energy harvesting systems, which either have no focus on cold startup [22], [23] or simply let each energy harvester start up from the cold state without collaborative operation [24], the proposed system breaks through the bottleneck by benefiting the TEH startup process from the PEG starter. However, it is also worth noting that adding a PEG harvester means more cost required by the system implementation, which might, in some cases, limit the usage of the proposed system. Inspired by reported multi-input energy harvesting system works, some future upgrades of the proposed system can be expected, which include but are not limited to harvesting kinetic energy from the PEG harvester constantly in steady states as a parallel path to the TEG harvester.

VI. CONCLUSION

This article presents a thermoelectric energy harvesting system assisted by a PEG starter that can generate a startup clock when the system is vibrating. The VCO and MPPT circuits adaptively control the system switching frequency and duty cycle by sensing the TEG voltage to achieve high efficiency and high output power. The ZCS block tracks the near-optimal ON-time of PMOS power switches to maximize energy conversion. The prototype chip achieves a minimum startup voltage of 10 mV with an end-to-end efficiency of 63.9%, thanks to the PEG startup block. The peak efficiency reaches 82.7% with a 55 mV TEG voltage.

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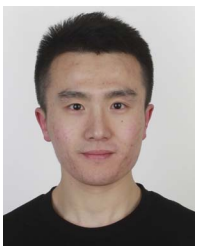

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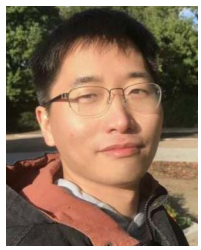

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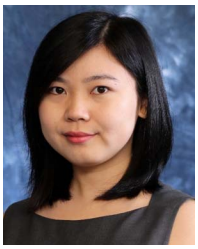

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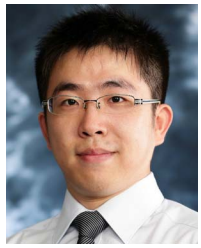

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