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A Sub-1 V Capacitively Biased BJT-Based Temperature Sensor With an Inaccuracy of ±0.15 °C (3σ) From −55 °C to 125 °C

Zhong Tang, *Member, IEEE*, Sining Pan, *Member, IEEE*, Miloš Grubor, and Kofi A. A. Makinwa, *Fellow, IEEE*

***Abstract*— This article presents a sub-1 V bipolar junction transistor (BJT)-based temperature sensor that achieves both high accuracy and high energy efficiency. To avoid the extra headroom required by conventional current sources, the sensor's diode-connected BJTs are biased by precharging sampling capacitors to the supply voltage and then discharging them through the BJTs. This capacitive biasing technique requires little headroom (∼150 mV), and simultaneously samples the BJTs' base–emitter voltages. The latter are then applied to a switched-capacitor (SC) ΔΣ ADC to generate a digital representation of temperature. For robust sub-1 V operation and high energy efficiency, the ADC employs auto-zeroed inverter-based integrators. Fabricated in a standard 0.18-μm CMOS process, the sensor occupies 0.25 mm^2 and consumes 810 nW from a 0.95-V supply at room temperature. It achieves an inaccuracy of ±0.15 °C (3σ) from −55 °C to 125 °C after a 1-point trim, which is at par with the state-of-the-art. It also achieves a resolution figure of merit (FoM) of 0.34 pJ·K^2, which is more than 6× lower than that of state-of-the-art BJT-based sensors with similar accuracy.**

***Index Terms*— ΔΣ ADC, capacitively biased bipolar junction transistor (BJT), inverter-based amplifier, temperature sensor, temperature to digital converter.**

I. Introduction

CMOS temperature sensors are widely used in IoT applications, such as wireless sensing nodes and environmental monitoring [1], [2], [3]. In such applications, temperature sensors should achieve good accuracy over a wide temperature range. Furthermore, since the sensors are powered by batteries or by energy harvesting, they also need to be low-power and energy-efficient.

Bipolar junction transistor (BJT)-based sensors are widely favored for their excellent accuracy with a low-cost 1-point trim [4]. However, they typically dissipate μWs of power and require supply voltages above 1 V [5], [6]. To further reduce their power dissipation, a lower supply voltage is desired. Although temperature sensors based on MOSFETs and resistors have demonstrated sub-1 V operation, this comes at the expense of accuracy [7], [8], [9], [10], [11].

To achieve both low-power dissipation and good accuracy, temperature sensors based on the capacitively biased "diode" (CBD) technique have been proposed [12], [13], [14]. As shown in Fig. 1, this involves charging a sampling capacitor C_S to the supply voltage V_{DD} and then discharging it across a diode. The resulting voltage across the diode over time can be expressed as [15]

$$V_D(t) = -mV_T \cdot \ln\left[\exp\left(\frac{-V_{DD}}{mV_T}\right) + \frac{I_S}{mV_T C_S}t\right] \quad (1)$$

where m is the nonideality factor of the diode, V_T is the thermal voltage, and I_S is the saturation current of the diode. After a short settling time (tens of ns), the impact of the $\exp(-V_{DD}/mV_T)$ term becomes negligible, and the residual voltage V_D on C_S will be determined by the diode's I/V characteristic, resulting in a supply independent logarithmic

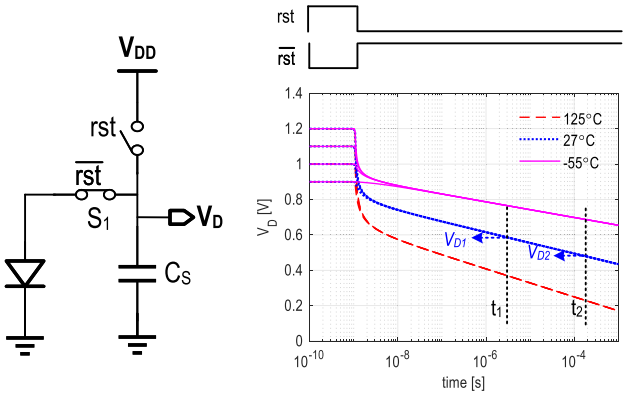

Fig. 1. Operating principle of the CBD structure.

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function of time [15], [16]. During this region, the bias current of the diode I_D is proportional to mV_TC_S/t. When the discharging time t_1 is fixed, the resulting voltage V_{D1} will be complementary to absolute temperature (CTAT). A proportional to absolute temperature (PTAT) voltage ΔV_D can then be generated by subtracting the outputs of two CB diodes (V_{D1}–V_{D2}) with a fixed discharging time ratio (t_2/t_1). Compared to the constant-current source biasing used in conventional temperature sensors, capacitive biasing requires little headroom and enables sub-1 V operation even at low temperatures when V_D is around 0.8 V [12], [16]. By using the CBD principle, several smart temperature sensors based on bulk diodes [12], dynamic threshold MOS transistors (DTMOSTs) [13], and diode-connected BJT [14] have been realized. Although these designs achieve sub-1-V operation, their relative inaccuracy (RIA) is much higher than that of conventional BJT-based designs with current source biasing [5], [6], [17].

In this article, which is an extended version of [18], the design of a sub-1-V CB p-n-p-based temperature sensor with both high accuracy and high energy efficiency is presented. It employs a CB p-n-p-based front-end and a switched-capacitor (SC) $\Delta\Sigma$ ADC to generate a digital representation of temperature. Dynamic techniques like auto-zeroing, chopping, and dynamic element matching (DEM) are used to mitigate circuit errors. For sub-1V operation and high energy efficiency, the ADC employs auto-zeroed inverter-based integrators. The sensor achieves a 1-point-trimmed inaccuracy of $\pm$ 0.15 °C (3σ) from −55 °C to 125 °C, which is at par with the state-of-the-art, as well as a resolution figure of merit (FoM) of 0.34 pJ · K^2, which is more than 6× better than that of state-of-the-art BJT-based sensors with similar accuracy.

The rest of this article is organized as follows. The error sources of previous CB p-n-p front-ends are analyzed and an improved front-end is proposed in Section II. Section III describes how the proposed front-end can be merged with the first integrator of a SC $\Delta\Sigma$ ADC. Furthermore, a charge-balancing $\Delta\Sigma$ modulator-based readout scheme is presented. Its circuit implementation is then described in Section IV. In Section V, the measurement results of the sensor are presented and compared to the state-of-the-art. Finally, conclusions are drawn.

II. CB P-N-P Front-End

Due to their ready availability, parasitic p-n-ps are widely used as the temperature sensing elements of CMOS temperature sensors. After a 1-point trim, the relative inaccuracy (RIA) of such designs is typically less than 0.2% over the military temperature range [2], [5], [6]. In such designs, however, the p-n-ps are biased by constant current sources, whose headroom limits their minimum supply voltage to about 1.2 V at cold temperatures, when V_{BE} approaches 0.8 V. In a bid to achieve lower supply voltages, the CBD technique can be used. In [14], a CB p-n-p-based temperature sensor is proposed that can operate from sub-1 V supply voltages and achieves a good energy efficiency of 3.2 pJ · K^2. However, its RIA (0.67%) is still much higher than that of state-of-the-art designs. The goal of this work is to bridge this gap.

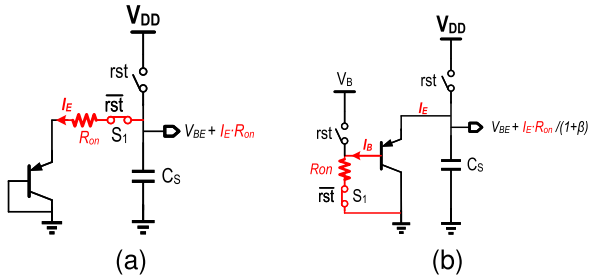

Fig. 2. (a) Block diagram of the CB p-n-p in [4]. (b) Block diagram of the proposed CB p-n-p.

A. Error Sources of the CB P-N-P

Fig. 2(a) illustrates the operation of the CB front-end used in [14]. Ideally, $V_{\rm BE}$ is solely determined by the p-n-p's I/V characteristic at the sampling moment [16]

$$V_{\rm BE} = V_T \cdot \ln\left(\frac{V_T \cdot C_S}{t \cdot I_S}\right) \tag{2}$$

where V_T is the thermal voltage and t is the discharging time. Apart from the process spread of the p-n-p itself, another important source of error in the sampled $V_{\rm BE}$ is the voltage drop across the ON-resistance $R_{\rm ON}$ of the switch S_1. Since $\Delta V_{\rm BE}$ is generated by two CB p-n-ps with different discharging times

$$\Delta V_{\rm BE} = V_T \cdot \ln\left(\frac{t_2}{t_1}\right) + R_{\rm ON} \cdot (I_{E1} - I_{E2}) \tag{3}$$

where t_1 and t_2 are the discharging times, and I_{E1} and I_{E2} are the corresponding emitter currents of the BJTs. If t_1 is much smaller than t_2, then $I_{E1} \gg I_{E2}$ and the error in $\Delta V_{\rm BE}$ voltage will be dominated by the $R_{\rm ON} \cdot I_{E1}$ term. Assuming that the temperature sensitivity of $\Delta V_{\rm BE}$ is 300 μV/°C, then with $R_{\rm ON} = 1$ kΩ and $I_{E1} = 100$ nA, the IR drop will cause an error of more than 0.3 °C. Although this can be mitigated by reducing $R_{\rm ON}$, this can be challenging with a sub-1 V supply. During the discharging phase, the voltage on the switch will change from $V_{\rm DD}$ to $V_{\rm BE}$, necessitating the use of a large switch whose charge injection and leakage will then become significant error sources.

B. Proposed CB P-N-P With Base Switching

To relax the switch $R_{\rm ON}$ requirement, an improved CB p-n-p front-end is proposed. As shown in Fig. 2(b), the discharging time is set by switching the base of a CB p-n-p. Compared to switching its emitter [14], this reduces the switch current by a factor $(1+\beta)$, where β is the BJT's current gain. Furthermore, since the switch is now connected to ground rather than to $V_{\rm BE}$, a sufficiently low $R_{\rm ON}$ can be achieved with a much smaller switch, thus mitigating errors due to charge injection and leakage. At the end of the sampling phase, the p-n-p can be turned off by switching its base to a higher cut-off voltage, denoted as V_B. To ensure that the p-n-p is turned off in a supply independent manner, V_B is designed to be a copy of $V_{\rm BE}$, which can be provided by an auxiliary CB p-n-p with conventional emitter switching [Fig. 2(a)].

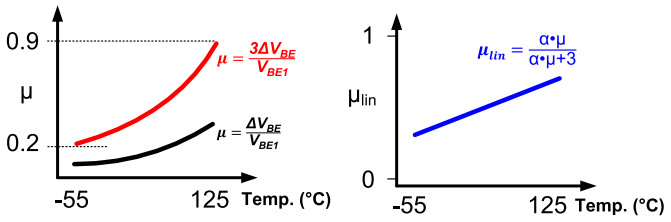

Fig. 3. Digitizing the ratio of $\Delta V_{\rm BE}$ and $V_{\rm BE}$ (left); linearization of μ (right).

To optimize the energy efficiency of the sensor, it is desirable to maximize $\Delta V_{\rm BE}$ by biasing the p-n-ps at a high current density ratio (CDR). This is usually done by combining several unit current sources and/or p-n-ps, which then need complex DEM schemes to mitigate mismatch [6]. In the case of capacitive biasing, however, the p-n-p's current at the sampling moment is set by the discharging time, and so the CDR can be accurately defined by using a clock divider to set the discharge time ratio (t_2/t_1) of two CB p-n-ps [12], [16]. To mitigate charge redistribution errors, the sampling capacitors C_S (4 pF) in this work are made much larger than the parasitic capacitors of the p-n-ps and switches (tens of fF). This choice also ensures good matching, low kT/C noise, and mitigates the effect of switch charge injection. A time ratio of 32 ($t_1 = 1\ \mu$s, $t_2 = 32\ \mu$s) is chosen to achieve a good balance between energy efficiency and accuracy. Both discharging times are defined by a 1-MHz system clock.

III. Readout Scheme

SC $\Delta\Sigma$ ADCs are widely used in precision BJT-based temperature sensor designs due to their high accuracy. As in [14], the sampled voltages $V_{\rm BE}$ and $\Delta V_{\rm BE}$ generated by the CB p-n-p pairs can be applied to a charge-balancing $\Delta\Sigma$ modulator to obtain a digital representation of temperature. As shown in Fig. 3, by using $\Delta V_{\rm BE} = V_{\rm BE1} - V_{\rm BE2}$ as the input signal, and $V_{\rm BE1}$ as the reference voltage, the modulator's bitstream average $\mu = \Delta V_{\rm BE}/V_{\rm BE1}$ is a well-defined function of temperature [14], [19]. As shown in [20], better use of the ADC's dynamic range can be made by digitizing $3\Delta V_{\rm BE}/V_{\rm BE1}$. Although μ is a nonlinear function of temperature, it can be linearized by computing

$$\mu_{\rm lin} = \frac{\alpha \cdot \mu}{(\alpha + \alpha_{\rm trim}) \cdot \mu + 3} \tag{4}$$

where α is a digital constant and $\alpha_{\rm trim}$ implements a PTAT trim that corrects the spread of $V_{\rm BE1}$ [5]. After this, the temperature output in degrees Celsius can be calculated from $A \cdot \mu_{\rm lin} - B$, where A and B are fitting parameters.

A. Charge-Balancing $\Delta\Sigma$ Modulator

To digitize $\mu = 3\Delta V_{\rm BE}/V_{\rm BE1}$, one solution is to use three CB pairs to generate $3\Delta V_{\rm BE}$ as the input signal, and then use another CB pair to generate 0 or $-V_{\rm BE1}$. This scheme, depicted in Fig. 4(a), requires a total of four CB pairs. By considering the error voltage e at the input of the loop filter, the circuit implementation can be further simplified. As illustrated in Fig. 4(b), when the output bitstream (BS) is 0, three CB pairs are configured to transfer a charge proportional to $3\Delta V_{\rm BE}$, while when the BS is 1, one of them is configured to generate $-V_{\rm BE2}$, thus transferring a charge proportional to $2\Delta V_{\rm BE} - V_{\rm BE2}$. This generates the same error signal as Fig. 4(a) scheme, but it only requires three CB pairs.

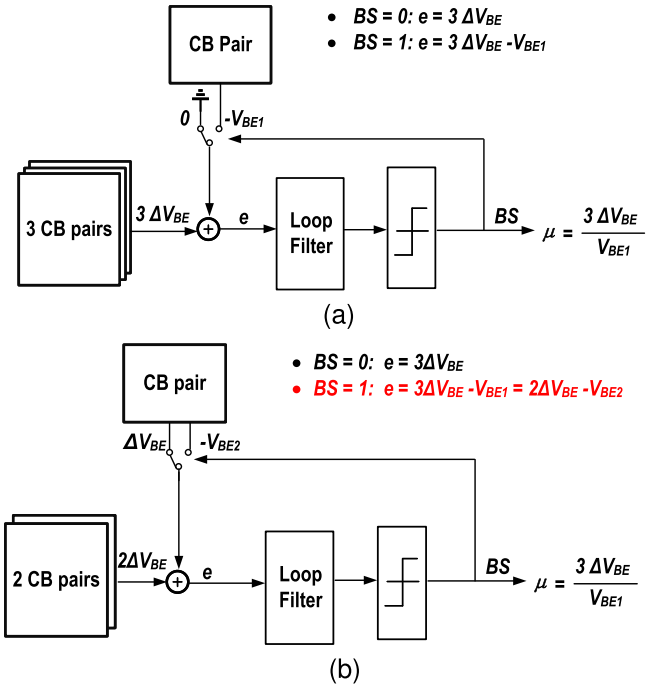

Fig. 4. (a) Simplified diagram of the direct $\Delta\Sigma$ modulator. (b) Simplified diagram of the proposed charge-balancing $\Delta\Sigma$ modulator.

B. CB P-N-P in an SC Integrator

The output of the CB pair is held on capacitors C_S, which has limited driving capability. As in [14], the CB pair is directly embedded into the first SC integrator of the ADC. To achieve this, the traditional sampling phase of the SC integrator is split into two sub-phases. This is illustrated in Fig. 5, for a single-ended integrator. Initially, C_S is precharged to $V_{\rm DD}$ by turning on $\rm SW_{1,2}$ in the reset phase (Fig. 5, top-left). Next, $\rm SW_1$ is turned off and $\rm SW_3$ is turned on, causing C_S to discharge via the p-n-p and $\rm SW_{2,3}$ (Fig. 5, top-right). Then $\rm SW_{2,3}$ are opened to stop the discharge and sample $V_{\rm BE}$ on C_S (Fig. 5, bottom-left). At the sampling moment, the voltage drop across $\rm SW_3$ due to the p-n-p's base current is negligibly small, while the PVT-dependent voltage drop across $\rm SW_2$ does not affect the sampled $V_{\rm BE}$. Finally, $\rm SW_{4,6}$ are closed to transfer the sampled $V_{\rm BE}$ on C_S to the integration capacitor $C_{\rm INT}$ and the base of the p-n-p is connected to V_B ($\sim V_{\rm BE}$).

Fig. 6(a) shows the differential circuit diagram of a CB pair that is connected to a SC integrator, with the corresponding control timing signals in Fig. 6(b). By applying different discharging times t_2 and t_1 for the CB pair, $\Delta V_{\rm BE}$ can be generated and processed by the loop filter. Controlled by the Φ_{0+} signal, one side of the CB pair can be connected to ground, thus generating a differential charge proportional to $-V_{\rm BE2}$. With $t_2 = 32\ \mu$s, the sampling frequency is approximately 15.6 kHz.

IV. Circuit Implementation

A. 1-bit Second-Order $\Delta\Sigma$ Modulator

Fig. 7 shows the circuit diagram of this sensor. A 1-bit second-order $\Delta\Sigma$ modulator is chosen in this work.

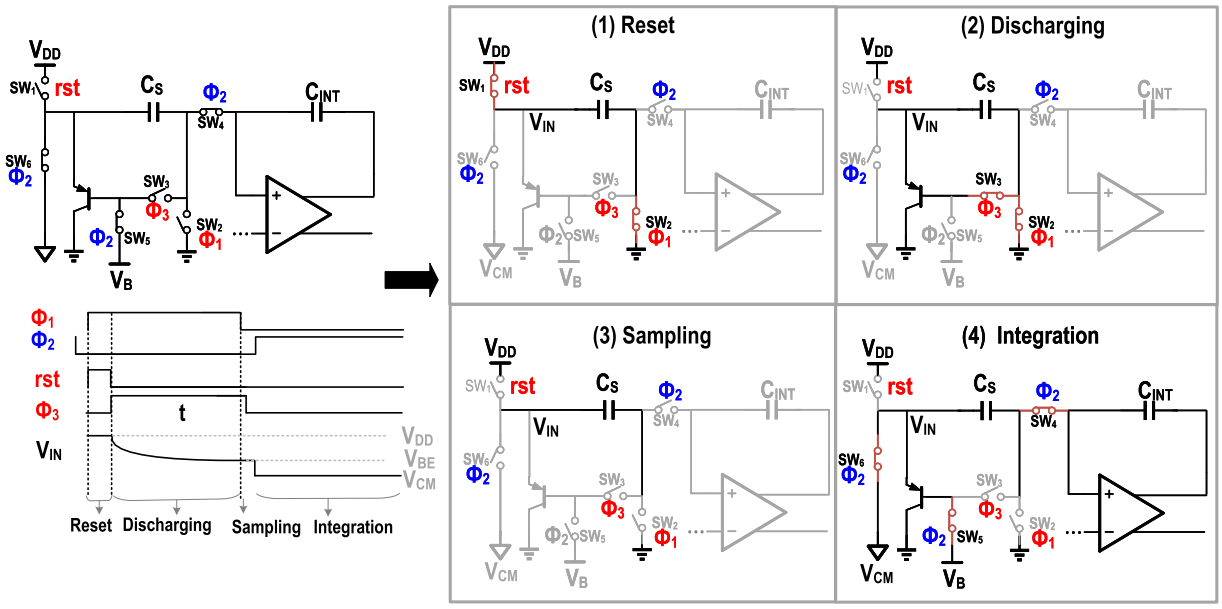

Fig. 5. Single-ended diagram of the CB p-n-p in an SC integrator and its working state at each phase.

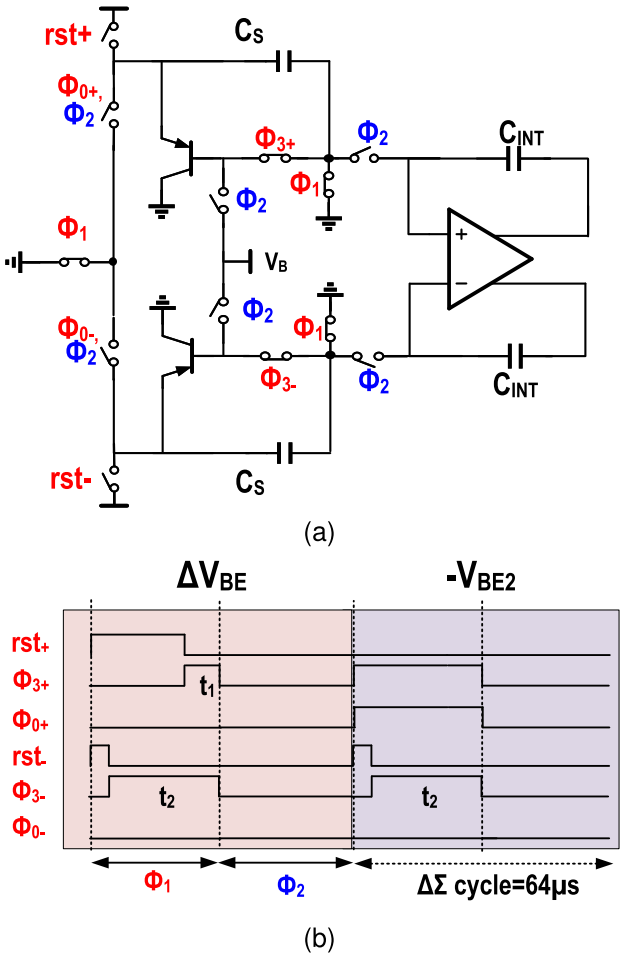

Fig. 6. (a) Differential circuit diagram of the CB p-n-p in an SC integrator. (b) Timing diagram of the CB p-n-p in an SC integrator.

Compared to the zoom-ADC used in [2], a simple 1-bit modulator minimizes the number of switches in the CB pairs, thus mitigating the impact of their nonidealities. A feed-forward architecture is used to reduce the output swing of the integrator, thus facilitating sub-1 V operation.

B. Auto-Zeroed Inverter-Based Amplifier

For robust sub-1 V operation and high energy efficiency, the modulator's integrators are built around inverter-based pseudo-differential amplifiers. One-half of the amplifier used in the first integrator is shown in Fig. 7 (right). During the sampling phase Φ_1, its bias current (160 nA) is set by a constant-gm bias generator via an NMOS current mirror, and the gate voltages of M_{N1} and M_{P1} are stored on capacitors $C_{\mathrm{AZN},P}$, respectively. Thanks to the auto-zero operation, the offset and $1/f$ noise of the amplifier are mitigated. The size of the auto-zero capacitors $C_{\mathrm{AZN},P}$ (17 pF) is chosen, such that the integrator's input noise is dominated by the kT/C noise of the CB pairs. During the integration phase Φ_2, the cascode transistors M_{P2} and M_{N2} ensure high dc gain (>70 dB over corners) in the target 180-nm CMOS process. The second integrator uses a scaled version of this amplifier and draws 40 nA.

Compared to the inverter-based amplifier in [21], where a floating current source is required to set the bias current, the proposed biasing scheme reduces the amplifier's minimum supply voltage from $2V_{\mathrm{gs}} + V_{\mathrm{dsat}}$ to $V_{\mathrm{gs}} + 2V_{\mathrm{dsat}}$, thus enabling sub-1 V operation with standard threshold voltage transistors. During the integration phase Φ_2, the differential output swing ranges from $\pm(V_{\mathrm{DD}} - 4V_{\mathrm{dsat}})$, which remains larger than $\pm$200 mV over corners with a 0.9-V supply. The integration capacitor of the first integrator C_{INT} is chosen as 12 pF, which ensures that the integrator output remains in its linear range over corners.

C. Dynamic Techniques

To achieve a V_{BE}-limited inaccuracy, component mismatch in the sensor should be minimized. Several dynamic techniques are employed in this work. To accurately realize 3 ΔV_{BE}, DEM is implemented by rotating the CB pair used to generate $-V_{\mathrm{BE2}}$. As in [5], a bitstream-controlled scheme is used, which is only activated when the BS is 1, since $-V_{\mathrm{BE2}}$ is only required in this state. The p-n-p and C_S mismatch inside the pair will also affect the accuracy of the generated

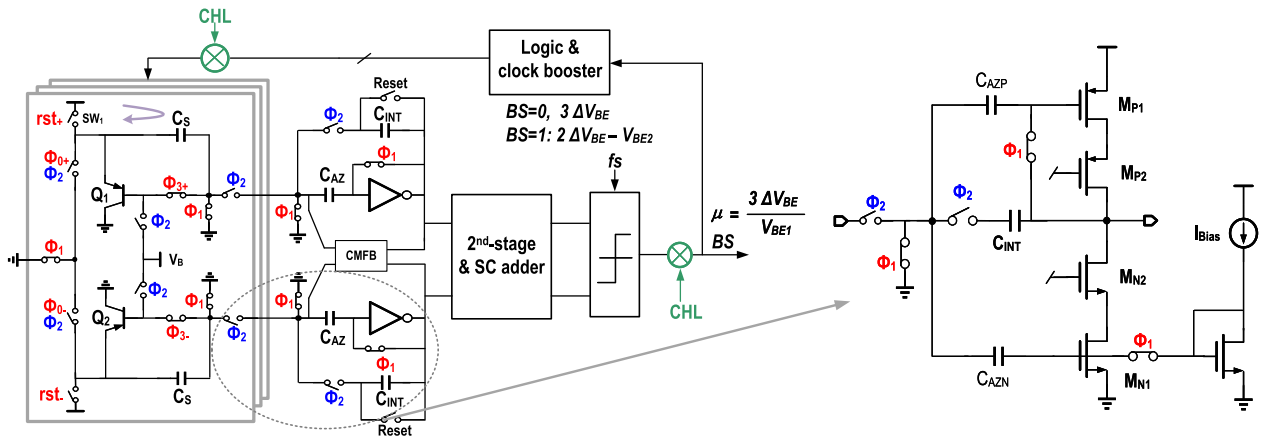

Fig. 7. Circuit diagram of the proposed CB-BJT based temperature sensor.

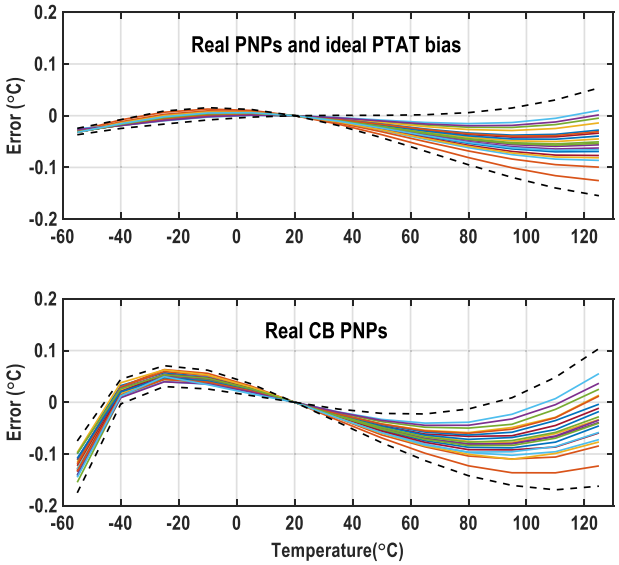

Fig. 8. 20 Monte-Carlo simulations including both process variation and mismatch after a 1-point PTAT trim. Top: real p-n-ps with ideal PTAT bias currents. Bottom: Real p-n-ps, switches, and capacitors. Dash lines indicate the 3σ error.

ΔV_{BE} voltage. This error is mitigated by using system-level low-frequency chopping (CHL), whose period is the same as the conversion time. Since the output voltage of the CB pairs is set by the clock timing, the input chopper is implemented by simply swapping the appropriate timing signals in the digital domain, thereby avoiding the need for extra analog switches. CHL also reduces the residual offset of the modulator caused by the charge injection mismatch and clock feedthrough of the switches.

D. Switches

To prevent CDR errors, and hence ΔV_{BE} errors, the leakage current of the associated switches should be minimized at high temperatures. To achieve both low leakage and low R_{ON} with a sub-1 V supply, $SW_{3,6}$ in Fig. 5 are implemented with high-threshold-voltage (HVT) NMOS transistors driven by clock boosters [14]. As in [14], SW_1 is implemented by a minimum size T-switch to reduce the leakage current.

After circuit implementation, Monte-Carlo simulation is performed to evaluate the accuracy of the CB p-n-p with all the real switches. Compared to p-n-ps with ideal PTAT bias currents, the CB p-n-ps achieve a similar inaccuracy ($<\pm 0.2$ °C) from -55 °C to 125 °C after a 1-point PTAT trim (Fig. 8).

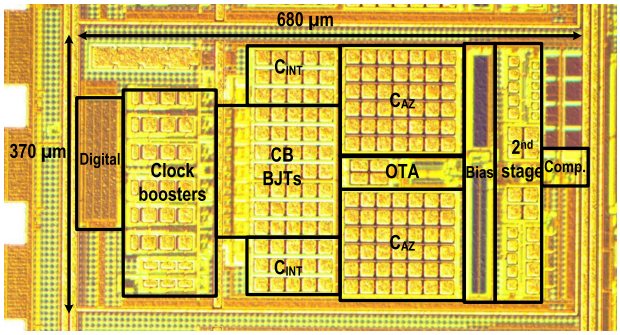

Fig. 9. Die micrograph of the proposed temperature sensor.

V. Measurement Results

The proposed temperature sensor was fabricated in a standard 180-nm CMOS process with an area of 0.25 mm^2. Fig. 9 shows the die photograph of this sensor. Most of it is occupied by the capacitors. Since metal-oxide-metal (MOM) capacitors scale well with process, a compact area can be achieved in an advanced process thanks to the capacitor-dominated design.

A. Power Consumption

As shown in Fig. 10, the sensor consumes 810 nW (620 nW analog, 190 nW digital) from a 0.95 V supply at room temperature, which increases to 2 μW at 125 °C due to the PTAT bias current and leakage. All the required timing signals are generated ON-chip from a 1-MHz external clock. For flexibility, the sinc^2 decimation filter and the linearization of μ are implemented OFF-chip.

B. FFTs and Resolution

Fig. 11 shows the FFTs of the sensor's bitstream at different temperatures, with the modulator operating in the free-running mode. In a conversion time of 128 ms, it achieves a kT/C-limited resolution of 1.8 mKrms at room temperature, and less than 2.1 mKrms over temperature (Fig. 12). This corresponds to a resolution FoM of 0.34 pJ $\cdot$ K^2 at room

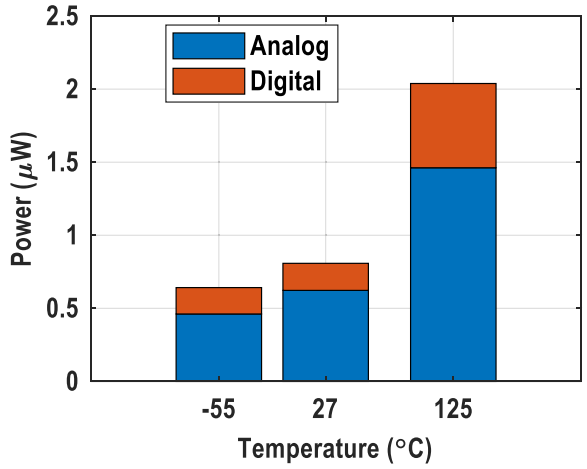

Fig. 10. Power breakdown at different temperatures.

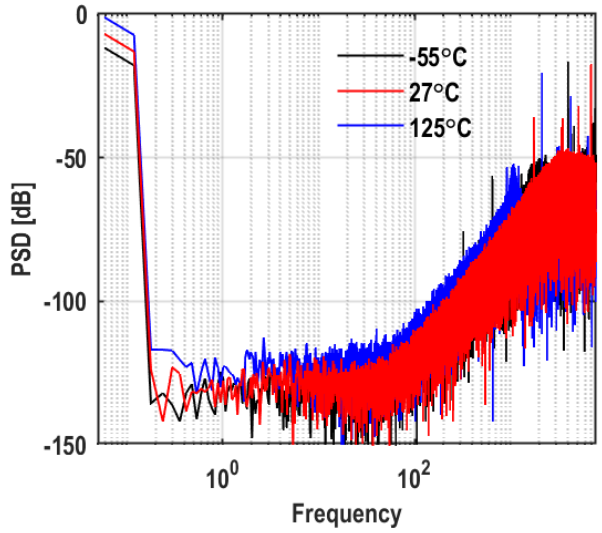

Fig. 11. FFTs of the sensor's bitstream at different temperatures.

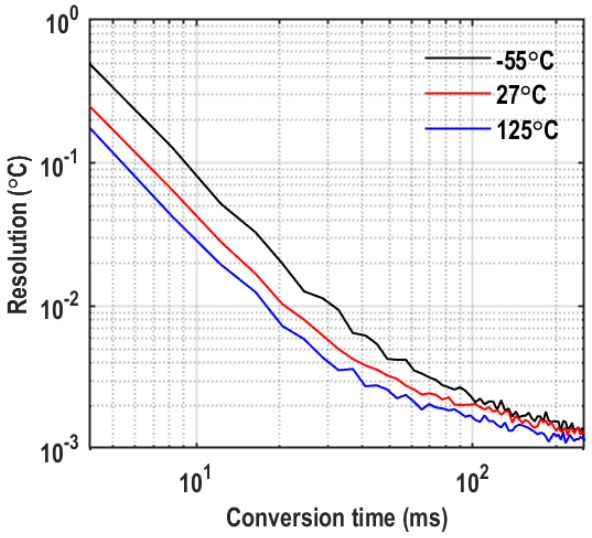

Fig. 12. Measured resolution at different conversion times.

temperature, and less than 0.53 pJ · K^2 over temperature, making it one of the most energy-efficient BJT-based sensors ever reported.

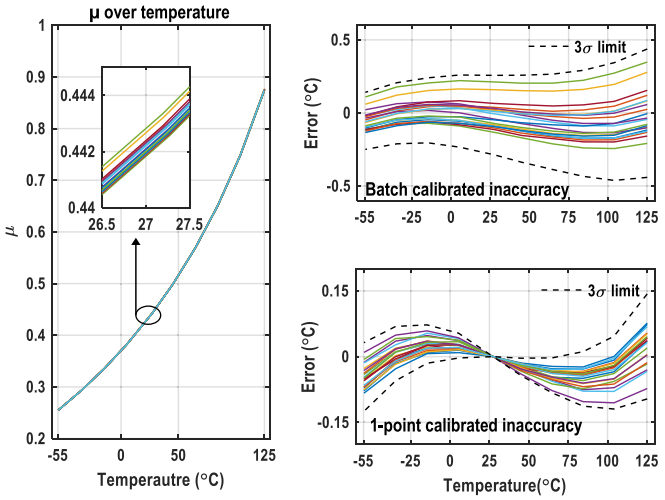

Fig. 13. Measured bitstream average μ of 20 chips over temperature (left); inaccuracy after batch calibration (top-right) and 1-point PTAT calibration (bottom-right).

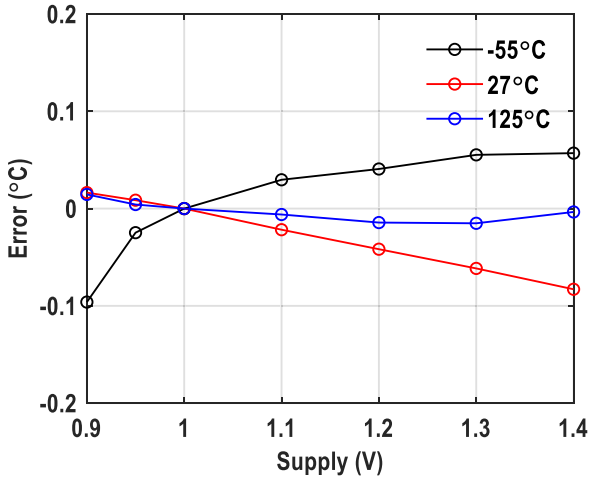

Fig. 14. Power supply sensitivity measurement at different temperatures.

Due to the use of large (12 pF) sampling capacitors to maximize accuracy, the resulting resolution (1.8 mK) exceeds the requirements of many applications. In future designs, these could be made smaller to reduce area and energy per conversion at the possible expense of accuracy.

C. Accuracy Measurement

As shown in Fig. 13 (left), the output of 20 chips in ceramic DIL packages was characterized from −55 °C to 125 °C. As expected, their BS average μ is a nonlinear function of temperature. After linearization with a fixed α (= 7.28), the sensor achieves a batch calibrated inaccuracy of ±0.45 °C (3σ). This improves to ±0.15 °C (3σ) after a 1-point PTAT trim, corresponding to an RIA of 0.17% (Fig. 13, right), which is at par with the state-of-the-art.

D. Supply Sensitivity

The sensor was also measured with different supply voltages over temperatures. As shown in Fig. 14, It can operate down to 0.9 V from −55 °C to 125 °C. The error only increases to 0.1 °C at −55 °C when operating with 0.9 V. This is due to the high V_{BE} (∼0.8 V) at low temperatures and some headroom (∼150 mV) is necessary for the generated V_{BE} to become

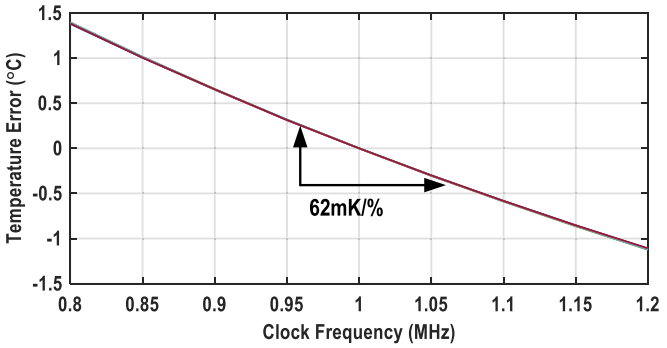

Fig. 15. Measured error with different input clock frequencies (normalized to 1 MHz).

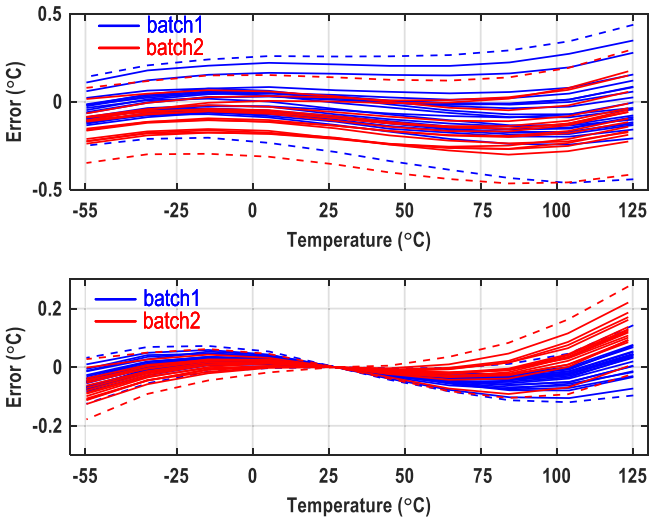

Fig. 16. Measured batch-to-batch inaccuracy using the same parameters $A = 604.26$, $B = 285.79$, $\alpha = 7.28$ from the first batch. Top: untrimmed inaccuracy; bottom: 1-pt trimmed inaccuracy; dash lines are $\pm 3\sigma$ limits.

sufficiently supply independent in the CB p-n-p. Over a 0.95 V to 1.4 V supply range, the sensor achieves a maximum power-supply sensitivity (PSS) of 0.2 °C/V from −55 °C to 125 °C without calibration at different supply voltages.

E. Clock Sensitivity

In this work, the discharging time is defined from an external 1-MHz clock. However, changing the clock frequency will change the bias current of the BJT at the sampling moment, which will affect the generated V_{BE} voltage. Since ΔV_{BE} is defined by the time ratio, it is independent of the time intervals. Seven sensors were measured with different system clock frequencies without any further calibration. Fig. 15 shows the measured error due to the clock frequency variation. It shows a clock sensitivity of only 62 mK/%, which is consistent among all chips. Thanks to the relatively low clock sensitivity, a low-cost *RC* oscillator can be used to provide the clock of the sensor, which can easily achieve a frequency inaccuracy of less than 1% after a 1-point trim [22].

F. Batch-to-Batch Variation

Batch-to-batch variation of the same design in the same package has also been investigated. Fig. 16 shows the measured inaccuracy from two batches. Using the parameters (A, B, and α) obtained from the first batch, the maximum error of sensors from the two batches is less than ±0.5 °C without trim (Fig. 16, top).

TABLE I
BATCH TO BATCH VARIATION OF THE SENSOR AND BATCH CALIBRATION PARAMETERS

Parameters	Batch1	Batch2
A	604.26	604.40
B	285.79	286.00
α	7.28	7.29
Untrimmed Inaccuracy (°C)	±0.45	±0.40
1-pt PTAT Trim Inaccuracy (°C)	±0.15	±0.17

After a 1-point PTAT trim by adjusting the α_{trim} term in (4), while keeping the same coefficients from the first batch for all the sensors, the maximum error from two batches is ±0.27 °C (Fig. 16, bottom). The increased inaccuracy is due to the slight shift optimal parameters (A, B, and α). Table I shows the sensor's inaccuracy after batch calibration is used to optimize these parameters. Together, the two batches then achieve an untrimmed inaccuracy of ±0.45 °C (3σ) and a 1-point PTAT trimmed inaccuracy of ±0.17 °C from −55 °C to 125 °C.

G. On-Chip Digital Backend

The decimation and linearization of the sensor's bitstream output can readily be implemented ON-chip. For instance, a 1024-tap sinc^2 decimation filter can be implemented with an adder, a register, and an up/down counter to generate the filter coefficients. The CHL ripple can then be eliminated by averaging the decimated results of two conversions. The implementation of the linearization equation (4) can be simplified by approximating it by a 6th-order polynomial. The resulting systematic error is then less than 10 mK over the military range, and so has a negligible effect on the sensor's accuracy. Furthermore, by implementing the polynomial in a recursive manner, only an adder, a register, and a multiplier are required, while the use of 20-bit arithmetic ensures that truncation errors are well below 1 mK and so will not impact the sensor's resolution. Since the linearization requires only 145 clock cycles, it can be done in parallel with the decimation in a pipelined manner. A synthesized implementation of the digital backend occupies about 0.05 mm^2, and consumes about 100 nW when it is clocked at the modulator's 15.625-kHz sampling frequency.

H. Comparison With the State-of-the-Art

The sensor's performance is summarized in Table II and compared to that of the state-of-the-art temperature sensors with similar accuracy and/or power consumption. To the best of the authors' knowledge, this is the first sub-1-V precision temperature sensor (RIA < 0.2%) over reported, which is suitable for biomedical applications and the temperature compensation of the low-power real-time-clocks. Compared to other CB sensors [12], [13], [14], it achieves the best accuracy (×4) and PSS (×1.3). Compared to conventional designs with current source biasing [6], [8], [17], this work achieves sub-1 V operation, similar accuracy, and state-of-the-art energy efficiency (×6.8).

Fig. 17 shows the comparison with other types of state-of-the-art temperature sensors in the CMOS process. This is

TABLE II
PERFORMANCE SUMMARY AND COMPARISON TO PREVIOUS WORK

	This work	SSCL'21 [14]	SSCL'19 [12]	CICC'20 [13]	JSSC'17 [6]	ISSCC'14 [8]	VLSI'22 [17]
Technology	**180nm**	55nm	16nm	28nm	160nm	160nm	180nm BCD
Type	**PNP DT ΔΣ**	PNP DT ΔΣ	Bulk Diode SAR	DTMOST OSC	PNP DT ΔΣ	DTMOST DT ΔΣ	NPN DT ΔΣ
Bias Method*	**CB**	CB	CB	CB	IB	IB	IB
Area [mm^2]	**0.25**	0.021	0.0025	0.017	0.16	0.085	0.058
Supply [V]	**0.95-1.4**	1-1.3	0.85-1	0.85-1.15	1.5-2	0.85-1.2	1.25
T. Range [°C]	**-55 to 125**	-55 to 125	-15 to 105	-10 to 90	-55 to 125	-40 to 125	-15 to 85
3σ error (Trim point)**	**±0.45 (0) ±0.15 (1)**	±1.4 (0) ±0.6 (1)	+1.5/-2.0 (0)	±2.0 (0) ±0.9 (1)	±0.4 (0) ±0.06 (1)	±1 (0) ±0.4 (1)	±0.4 (0) ±0.15 (1)
RIA[%] (Trim point)	**0.5 (0) 0.17 (1)**	1.6 (0) 0.67 (1)	2.9 (0)	4 (0) 1.8 (1)	0.44 (0) 0.07 (1)	1.3 (0) 0.5 (1)	0.8 (0) 0.3 (1)
Power [μW]	**0.81**	2.2	18	33.75	6.9	0.6	0.21
Tconv [ms]	**128**	6.4	0.013	0.1	5	6	50
Res. [mK]	**1.8**	15	300	10.2	15	63	15
PSS[°C/V]	**0.2**	3.7	1.5	0.27	0.01	0.45	0.07
Res. FoM* [pJ· K^2]**	**0.34****	3.2****	21	0.36****	7.8****	14.1****	2.3****

* CB: capacitively biasing; IB: current source biasing.
** 0: no individual trim; 1: 1-point individual temperature trim.
*** Res. FoM=(Energy/conversion)·(Resolution)^2.
**** Excluding the digital back-end, such as the decimation filter and the digital nonlinearity correction circuits.

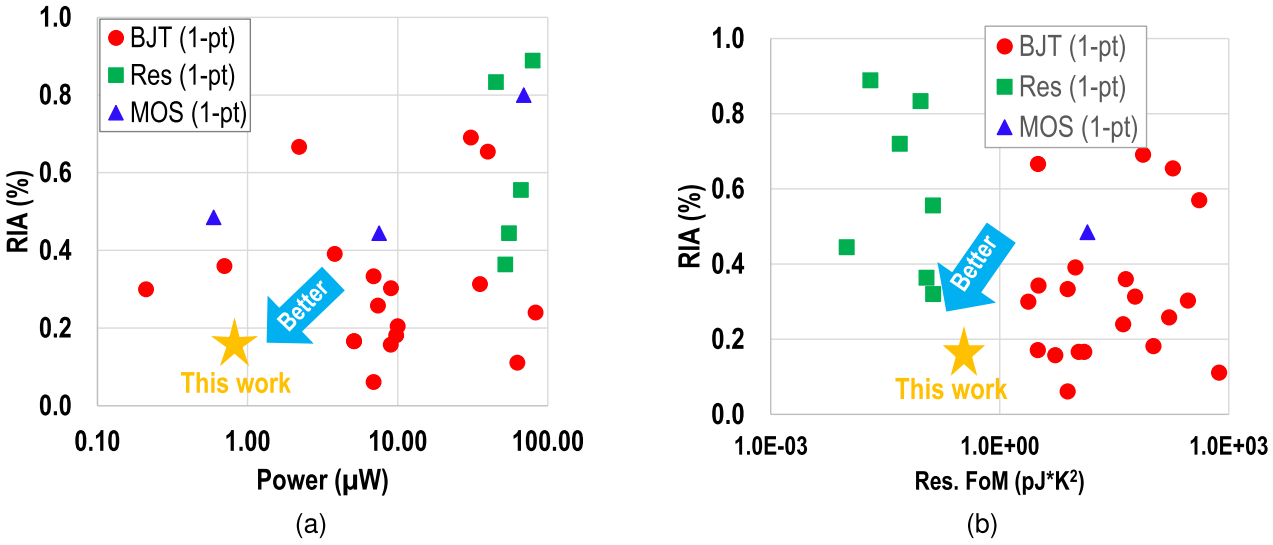

Fig. 17. (a) RIA versus power comparison. (b) RIA versus resolution FoM comparison.

the only temperature sensor that achieves a RIA $<$ 0.2% after a 1-point trim, together with sub-μW power and sub-pJ $\cdot$ K^2 energy efficiency.

VI. CONCLUSION

A sub-1 V BJT-based temperature sensor with a capacitively biased read-out scheme is proposed in this work. A high-accuracy CB-BJT front-end is proposed and then embedded into the first stage of a charge-balanced SC $\Delta\Sigma$ ADC. For robust sub-1 V operation and high energy efficiency, the ADC employs inverter-based integrators. Techniques, such as auto-zeroing, chopping, and DEM are used to mitigate circuit errors. Fabricated in a standard 0.18-μm CMOS process, the sensor consumes 810 nW from a 0.95-V supply at room temperature. it achieves a 1-point-trimmed inaccuracy of ±0.15 °C (3σ) from −55 °C to 125 °C.

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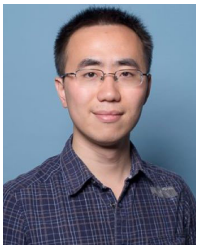

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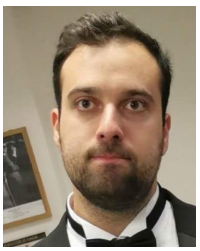

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