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Mao, Saijun

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# Modular High Voltage Pulse Converter for Short Rise and Decay Times

**Saijun Mao**

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# Modular High Voltage Pulse Converter for Short Rise and Decay Times

**Proefschrift**

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen;
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op
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Door

Saijun MAO

Master of Engineering, Power Electronics, Nanjing University of Aeronautics and Astronautics, China

geboren te Jiangsu, China

This dissertation has been approved by the:

Promotor: Prof. dr. J. A. Ferreira

Copromotor: Dr. J. Popovic

Composition of the doctoral committee:

Rector Magnificus, Chairman

Prof. dr. J. A. Ferreira, Delft University of Technology, promotor

Dr. J. Popovic, Delft University of Technology, copromotor

Independent members:

Prof. dr. R. Ross, Delft University of Technology

Prof. dr. L. Empringham, University of Nottingham, England

Prof. dr. J. Böcker, Paderborn University, Germany

Prof. dr. G.Q. Zhang, Delft University of Technology

*To my family*

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# Abbreviations and symbols

| | |
|---|---|
| 3D | Three dimensional |
| AC | Alternating current |
| $A_e$ | Effective core area |
| AP | Area product |
| $B_{max}$ | Maximum flux density |
| $C$ | Capacitance |
| $C_{eq}$ | Equivalent capacitance of the HV transformer loaded by the rectifier |
| $C_{eq}'$ | Equivalent capacitor of the sub-divided cell |
| $C_p$ | Parallel resonant capacitance |
| $C_p'$ | Parallel capacitor of the sub-divided cell |
| $C_r$ | Resonant capacitor |
| $C_{\mathrm{rec}}$ | Capacitor of rectifier or voltage multiplier |
| $C_{tot}$ | Total capacitance of the equivalent RC network |
| $C_{w,p}$ | Capacitance of the transformer primary winding |
| $C_{w,s}$ | Capacitance of the transformer secondary winding |
| $C_{\mathrm{wp}}$ | Parasitic winding capacitance of the HV transformer |
| $C_{vm}$ | Capacitance for the voltage multiplier |
| CCM | Continuous conduction mode |
| CT | Computed Tomography |
| CW | Cockcroft-Walton |
| $D$ | Duty cycle |
| DC | Direct current |

| | |
|---|---|
| ESP | Electrostatic precipitation |
| $f_s/\omega_s$ | Frequency/Angular frequency of the resonant tank input voltage |
| $f_{min}$ | Minim frequency |
| FHA | First Harmonic Approximation |
| $F_r$ | Ratio of ac resistance to dc resistance of transformer windings |
| FW | Full-wave |
| $G_\theta$ | Product of $\omega_s$, $C_{tot}$, $R_{eq}$ |
| GaN | Gallium nitride |
| GND | Ground |
| $h$ | Height of the transformer windings |
| $H$ | Gain of the LCC resonant converter |
| HV | High voltage |
| HW | Half-wave |
| $I_{crec\text{-}rms}$ | RMS value of the AC current flowing through the capacitor of the rectifier or multiplier |
| $I_{d\_Fav}$ | Average current flowing through the diode |
| $I_{d\_Fav}$ | RMS current flowing through the diode |
| $I_{rm}$ | Maximum resonant current |
| $i_r(t)$ | Instantaneous resonant current |
| $i_s$ | Instantaneous current of the transformer secondary side |
| $I_o$ | Output current |
| $I_p$ | RMS value of the transformer primary current |
| $I_s$ | RMS value of transformer secondary current |

| | |
|---|---|
| $I_{s,avg}$ | Average current of the transformer secondary side |
| $I_{s,RMS}$ | Root Mean Square (RMS) current of the transformer secondary side |
| $I_{in.RMS}$ | Input RMS current |
| IGBT | Insulated gate bipolar transistor |
| $J_w$ | Current density |
| $k$ | Turns ratio of the high voltage transformer |
| $k_c$ | Coefficients between $C_p$ and $C_{eq}$ |
| $k_{core}$ | Coefficients of magnetic core material |
| $k_i$ | Coefficients of the Fourier transformation of the parallel capacitor current |
| $k_{VM}$ | Voltage gain of the rectifier |
| $k_v$ | Coefficients of the Fourier transformation of the parallel capacitor voltage |
| $K_u$ | Core geometry factor |
| $K_w$ | Window utilization factor |
| $kV$ | kilovolt |
| $L_m$ | Magnetizing inductance |
| $L_r$ | Resonant inductance |
| $L_{lk}$ | Leakage inductance of the HV transformer |
| $L_{plk}$ | Primary side leakage inductance of the HV transformer |
| $L_{slk}$ | Secondary side leakage inductance of the HV transformer |
| $L_{r\_tot}$ | Total resonant inductance of the resonant tank |
| LCC | Series parallel |
| $m$ | Number of elemental HV transformers |
| mA | Milliampere |

| | |
|---|---|
| MOSFET | Metal oxide semiconductor field-effect transistor |
| $n$ | Stage number for the voltage multiplier |
| $n_1$ | Turns number of the HV transformer primary winding |
| $n_2$ | Turns number of the HV transformer secondary winding |
| $P$ | Polarities of the voltage multiplier |
| $P_{core}$ | Magnetic core loss |
| $P_{cap\_rec}$ | Power loss of the capacitors in the rectifier or multiplier circuit |
| $P_{diode\_rec}$ | Power loss of the diode in the rectifier or multiplier circuit |
| $P_{diode\_rec\_con}$ | Conduction power loss of the diode in the rectifier or multiplier circuit |
| $P_{diode\_rec\_rr}$ | Switching power loss of the diode in the rectifier or multiplier circuit |
| $P_{HV\_tank}$ | Total loss of the HV tank |
| $P_o$ | Output power |
| $P_{winding\_con}$ | Transformer winding conduction loss |
| $P_{winding\_die}$ | Dielectric loss of winding in the HV transformer |
| $P_{winding}$ | Total transformer winding loss |
| PCB | Printed circuit board |
| $PF$ | Power factor of the resonant tank |
| PWM | Pulse-wide-modulation |
| PRC | Parallel resonant converter |
| $Q$ | Quality factor of the resonant tank |
| $Q_o$ | Charge flowing through diodes |
| $Q_{rr}$ | Reverse recovery charge |
| $R_{AC}$ | AC resistance of the winding |

| | |
|---|---|
| $R_{DC}$ | DC resistance of the winding |
| $R_{eq}$ | Equivalent resistance of the high voltage transformer loaded by the rectifier |
| $R_{eq}'$ | Equivalent resistor of the sub-divided cell |
| $R_o$ | Output resistor |
| $R_o'$ | Output resistor of the sub-divided cell |
| $R_p$ | Resistance of the transformer primary winding |
| $R_s$ | Resistance of the transformer secondary winding |
| $R_{\mathrm{pw\_AC}}$ | AC resistance for the transformer primary winding, |
| $R_{\mathrm{sw\_AC}}$ | AC resistance for the transformer secondary winding |
| RMS | Root mean square |
| SF6 | Sulfur fluoride |
| Si | Silicon |
| SiC | Silicon carbide |
| SRC | Series resonant converter |
| $t$ | Time |
| $t_r$ | Rise times of the HV pulse |
| $t_f$ | Decay times of the HV pulse |
| TR | Transformer rectifier sets |
| UPS | Uninterruptible power supply |
| $V_{\mathrm{CWP}}$ | Voltage applied to parasitic winding capacitance |
| $v_p$ | Instantaneous voltage across the parallel capacitor |
| $V_{HV\text{-}tank\_elementary}$ | Output voltage for the each elemental HV tank |
| $V_{HV\text{-}tank\_posotive\_total}$ | Total output voltage for the positive polarity HV tank |

| | |
|---|---|
| $V_{HV\text{-}tank\_negtive\_total}$ | Total output voltage for the negative polarity HV tank |
| $V_{in}$ | Input DC voltage |
| $V_{\text{core}}$ | Volume of the magnetic core |
| $V_{Cr}$ | Maximum voltage across the resonant capacitor |
| $V_{cp,max}$ | Maximum voltage of the parallel capacitor |
| $V_o$ | Output voltage |
| $V_{\text{r}}$ | Reverse voltage of the diode |
| $V_{sec}$ | Voltage of transformer secondary winding |
| $V_{tr\_AC\_insulation}$ | AC insulation stress for the HV transformer |
| $V_{tr\_DC\_insulation}$ | DC insulation stress of the HV transformer |
| $V_{tr\_s}$ | Secondary voltage of the HV transformer |
| $V_{tr\_s\_pk}$ | Peak AC voltage of elemental HV transformer secondary winding |
| VF | Voltage frequency |
| ZCS | Zero-current switching |
| ZVS | Zero-voltage switching |
| $Z_{in}$ | Resonant tank input impedance |
| $\delta$ | Skin depth |
| $\varepsilon$ | Permittivity |
| $\varepsilon_r$ | Relative permittivity |
| $\varepsilon_o$ | Permittivity in vacuum |
| $\lambda$ | Wavelength |
| $\mu$ | Permeability |
| $\mu_r$ | Relative permeability |

| | |
|---|---|
| $\mu_o$ | Permeability in vacuum |
| $\varphi$ | Magnetic flux |
| $\theta$ | Conduction angle |
| $\eta$ | Efficiency of the HV pulse converter |
| $\psi$ | Phase lag between inverter output voltage and resonant current |
| $\rho$ | Conductor resistivity |
| $\xi$ | Normalized conductor height related to skin depth |
| $tan\delta$ | Dissipation factor of the insulation materials |
| $\Delta B$ | Magnetic flux density |

# Table of Contents

# Chapter 1

# Introduction

The main objective of this thesis is to investigate a modular high voltage (HV) pulse converter technology with fast rise and decay times, high efficiency, high power density. The focus of this thesis is to derive a systematic approach to classify and identify the optimal architecture, investigate the key subcomponent's technologies and derive a generic equivalent steady-state circuit modeling method and comprehensive design procedure for a HV pulse converter. More specifically, the research will concentrate on the effect of modularization, increased switching frequency for a HV transformer, and the key influence factors for HV pulse rise and decay times, as well as the method used to mitigate diode reverse recovery effect for multi-stage voltage multiplier. This chapter introduces the related research background, problem statement, research objectives and thesis layout.

## 1.1 Background

### 1.1.1 Overview of HV pulse converters

HV pulse converters are widely used in applications such as X-ray generation [1-1]-[1-5], electrostatic precipitation (ESP)[1-6]-[1-9], HV capacitor charger amongst other areas[1-10]-[1-12]. Generally, HV pulse converters convert low voltage DC voltage to high DC voltage, which typically is as high as tens to hundreds of kilovolts according to different applications. A HV pulse converter is also known as a HV pulse generator, HV generator, HV power supply or HV DC-DC converter in many applications. The HV pulse converter is the term used in this thesis. Compared to traditional low frequency HV pulse converters, switching mode high frequency HV pulse converters provide higher power density, higher efficiency and better steady and dynamic performance. During decades of research, high frequency HV generation technologies have been successfully industrialized and have accumulated abundant solutions for different applications. Generally, a HV pulse converter is composed of a DC-AC inverter, a resonant tank, a HV transformer and a HV rectifier, as illustrated in Fig.1-1. The series-parallel (LCC) resonant type converter is the common topology of choice in high frequency HV pulse converter systems due to its ability to utilize the parasitic components of a HV transformer and achieve soft switching for a wide operating range. The inverter converts low input DC voltage into high frequency low AC voltage. The basic topology for an inverter is half bridge or full bridge. In relatively high input voltage applications, multi-level inverters or cascaded inverters are alternative options. Resonant capacitors and inductors are often combined to form a resonant tank, where resonant current or voltage is used to ensure soft-switching of power semiconductor devices. The function of a HV transformer is to provide the voltage step-up with galvanic isolation by converting the high frequency low AC voltage to high frequency high AC voltage. The HV rectifier converts the high frequency high AC output voltage from the secondary winding of the HV transformer to even higher DC output voltage.

A full bridge rectifier is the basic topology for a HV rectifier. However, in some cases, the multi-stage multiplier circuit is adopted to acquire higher output voltage. Besides, the aforementioned components can be connected in series or parallel flexibly to achieve better performance depending on the applications.

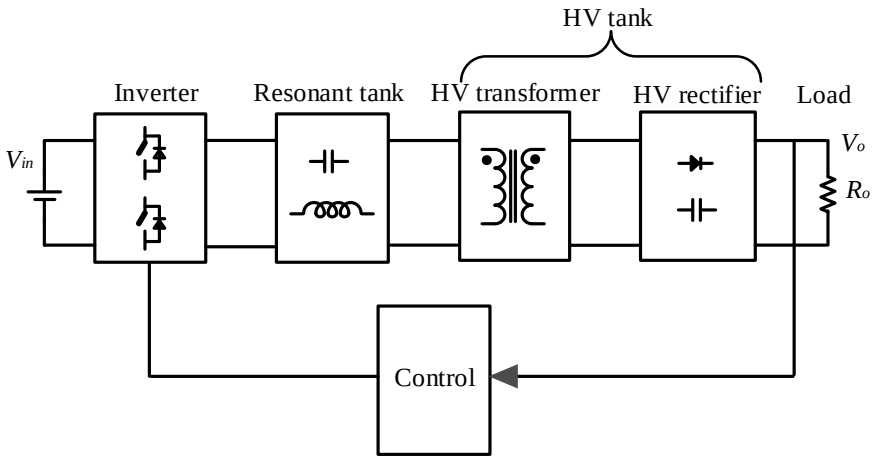



Fig. 1-1 HV pulse converter circuit diagram

### 1.1.2 HV pulse converter in CT and X-ray machine applications

Fig. 1-2 introduces HV pulse converter application examples of medical computed tomography (CT) machines and X-ray machines. Being one of the most useful tools in the medical field, Radiologists use X-Ray Generators to produce pictures of a patient's internal structures, allowing them to diagnose broken bones, locate tumors, and even see the digestive tract. The HV pulse converter is the key component for CT and X-ray machines to generate required high voltage, ranging from 20 kilovolt(kV) to 160kV across the X-ray tube anode and cathode in order to establish an intense electric field to accelerate the electrons. The X-ray will be generated when the electrons gain sufficient energy through the acceleration and collide with the anode of the X-ray tube. The required high voltage can be as high as 450kV for industrial non-destructive inspection application which requires high intensity high resolution X-ray from the x-ray tubes with focal spot sizes of 1μm or less. The flow of electrons from the current of a HV pulse converter is in the range of 1 to 1000 milliampere(mA).

The HV pulse converter circuit for CT and X-ray machine radiographic applications has been developing for almost a century with the continuous improvement of power semiconductor devices, magnetic materials, insulation materials and dielectric materials technology. The X-ray HV pulse converter was developed in the early 20th century by using mechanical switches at low frequency (50/60Hz) operation. Then the power semiconductor device such as a thyristor was introduced for X-ray HV pulse converters in the middle of the 20 century. Since the 1980s, the power semiconductor devices such as silicon IGBT and MOSFET were used for X-ray HV pulse converters at several tens of kHz to few hundreds of kHz switching frequency. The typical switching frequency for a HV pulse converter in existing CT and X-ray machines is around 20 to 80kHz. A photo of a HV pulse converter for the medical X-ray machine is shown in Fig. 1-3 as an example [1-15]. The size of X-ray HV pulse converter can be reduced significantly by high switching frequency operation compared with low switching frequency in early stage.


(a) CT machine [1-13]


(b) X-ray machine[1-14]

Fig. 1-2 The HV pulse converter applications examples: medical CT and X-ray machine

Fig. 1-3 Photo of a HV pulse converter for the X-ray machine [1-15]

Along with the development of medical CT and X-ray machines, HV pulse converter technology will also evolve for improved performance or advanced function requirements for CT and X-ray machines in the future. Some of the requirements for medical CT and X-ray machine development are listed below:

a) Better imaging quality, and image artefact mitigation due to motion
b) Radiation dose reduction
c) Dual energy, fast HV pulse switching between one HV to another HV within short time
d) Low energy consumption
e) Compactness, portable, light weight
f) Flexible, scalable
g) Reliable, easy maintenance
h) Cost effective

The development requirements of medical CT and X-ray machine raise the research needs for a HV pulse converter to meet the medical instruments system performance and function target. The research needs will be elaborated later.

### 1.1.3 HV pulse converter in electrostatic precipitator applications

The electrostatic precipitator is another industrial application example for the HV pulse converter illustrated in Fig. 1-4. Due to growing concerns about environmental pollution, the reduction of particle emissions by electrostatic precipitator is a highly important issue for coal fired power plants [1-6]. An ESP consists of parallel electrodes that use electrostatic charges to separate particles in the entering gas. Power converters are used to supply energy to the ESP electrodes at a high voltage level. These power supplies have a typical output power range of 10 to 250 kW and a high output DC voltage range of 30 to 150 kV [1-7].

(a) an electrostatic precipitator machine [1-16] (b) a HV pulse converter [1-17]

Fig. 1-4. HV pulse converter applications examples: an electrostatic precipitator and photo of a HV pulse converter for an electrostatic precipitator

The conventional electrostatic precipitator was driven by mains frequency transformer-rectifier based HV pulse converter technology which is commonly referred to “transformer rectifier sets” (TR). The mains frequency HV pulse converters are still the most commonly used for ESP. Fig. 1-5 provides the diagram of a mains frequency HV pulse converter for an electrostatic precipitator [1-7]. It comprises a single-phase mains frequency (50/60Hz) voltage step-up transformer with high turns ratio and high insulation capability followed by a rectifier which connects to the electrostatic precipitator. The HV pulse converter is controlled by changing the firing angles of an anti-parallel pair of thyristors in the transformer primary side [1-8].

Modern high frequency HV pulse converter technologies have been being developed for the electrostatic precipitator in power plants and industrial processes since the early 1990s. For the high frequency HV pulse converter technology, the mains are rectified by three-phase input rectification and the resulting smooth DC voltage is chopped by using a transistor bridge to a high frequency AC voltage, connected to the HV transformer with a high turn ratio and with sufficient insulation. The secondary winding of the HV transformer is connected to the output diode rectifier that supplies the required voltage and current to the electrostatic precipitator. Typical operation switching frequency for a HV pulse converter is 20 to 50kHz. An example

of a high frequency HV pulse converter diagram is depicted in Fig. 1-6 [1-9]. A power factor close to unity, and a better form factor of the input current over the entire operation range, can be achieved. The series parallel(LCC) resonant converters are an attractive choice for a high frequency HV pulse converter for an electrostatic precipitator because they can operate in soft-switching modes, reducing the switching losses and with the possibility to incorporate the HV transformer non-idealities. If a conventional hard-switching PWM converter were to be used, the leakage inductance and the winding parasitic capacitance of the HV transformer, would cause parasitic resonances that affect the HV pulse converter's behaviour.

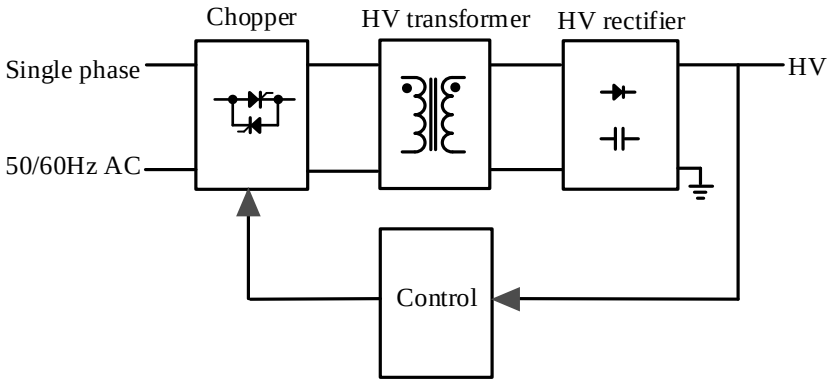



Fig. 1-5 Block diagram of a mains frequency HV pulse converter for an electrostatic precipitator [1-7]

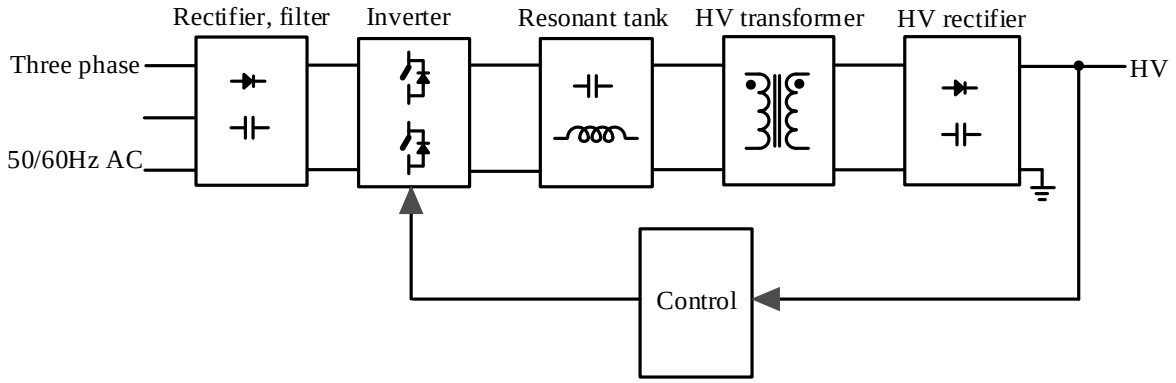



Fig. 1-6 Block diagram of a high frequency HV pulse converter for the electrostatic precipitator [1-9]

High frequency HV pulse converter technology provides significant advantages over conventional mains frequency HV pulse converter to improve electrostatic precipitator overall performance and reduce the dust emission level. The advantages of high frequency HV pulse converter technology are summarized below:

a) Comparatively overall size and weight reduction.
   The weight of the high frequency type is around 1/3 to 1/5 of the conventional mains frequency HV pulse converter since the HV transformer size and weight can be greatly reduced at high switching frequency.
b) Low output voltage ripple.

Very smooth high DC output voltage with negligible output voltage ripple can be achieved for a high frequency HV pulse converter. It will also increase the efficiency of the electrostatic precipitator.

c) Much faster control response, faster sparkover handling, low stress on the electrostatic precipitator electrodes.
   There is a delay between detection of a sparkover and the reaction of the HV pulse converter in the range of few ten ms because the thyristor is operated at mains frequency for the conventional mains frequency HV pulse converter. This delay drops down into the µs range. The power flow to the arc is much faster than a mains frequency HV pulse converter, resulting in shorter arcing time due to much faster control response. The duration of the precipitation outage, and thus average emissions can be reduced. Additionally, shorter arcing durations mean less stress on components of the electrostatic precipitator.
d) Ease for transportation, installation.
   The installation and commissioning time is reduced to half a day compared to several days for the conventional mains frequency HV pulse converter. The transportation and installation and commissioning cost can be also saved.
e) Low impact for the mains.
   High frequency HV pulse converter technology loads the 3-phase mains symmetrically, and the load is shared symmetrically between the three mains phases. The conventional mains frequency HV pulse converter has unbalanced conditions between the mains phases, with a higher apparent power. So, it suffers higher losses and thus increasing the size and cost of devices. The input currents per phase are significantly lower for a high frequency HV pulse converter compared with the single-phase connected mains frequency HV pulse converter.

The main differences between the conventional thyristor-based mains-frequency HV pulse converter technology and the high frequency HV pulse converter technology are summarized in Table 1-1.

Due to the stricter requirement for emissions reduction and electrostatic precipitator system operation cost saving, the performance of high frequency HV pulse converters needs to be further improved. Some of the requirements for high frequency HV pulse converters used in electrostatic precipitator development are listed below:

a) Better capability for emission reduction: faster response and sparkover handling capability, lower stress on the electrostatic precipitator electrodes.
b) System operation cost saving: low energy consumption
c) Reliable and easy maintenance
d) Cost effective

The development requirements of an electrostatic precipitator raise the research needs for HV pulse converters to meet the system performance and function target.

Table 1-1 Summary of the main differences between conventional mains frequency and high frequency HV pulse converter technology

| Features | Mains frequency HV generator | High frequency HV generator |
|---|---|---|
| Input phase | Single phase | Single phase |
| Mains impact | Power factor <0.7<br>3 phase unbalance for mains<br>High current stress | Power factor>0.9<br>3 phase balance for mains<br>Relative low current stress |
| Frequency | 50/60Hz | 20~50kHz |
| Switching power device | Thyristor | Transistor: IGBT, MOSFET |
| Output voltage ripple | ~30% | <1% |
| Power conversion efficiency | 80~85% | 90~95% |
| Dynamic performance | Slower control (10 ms), downtime due to sparkover up to 100 ms | Very fast (10-50 μs), downtime due to sparkover below 10 ms |
| Weight | 1000~3000kg | 200~500kg |

### 1.1.4 Research needs for HV pulse converter performance improvement

According to the above introductions about the development requirements of medical CT and X-ray machines, the research needs for a HV pulse converter can be concluded to meet the medical instrument's system performance and function target. High switching frequency, modular HV architecture, new emerging Silicon Carbide(SiC) power semiconductor device and high power density integration are four key aspects to achieve HV pulse converter performance improvement. The relationship of four key aspects and development requirements of a HV pulse converter for medical CT/X-ray machines are summarized in Table 1-2. The green stars illustrate that the four key aspects impact on the development requirements.

Table 1-2 Relationship of four key aspects and development requirements of the HV pulse converter for medical CT / X-ray machine

| | High switching frequency | Modular architecture | SiC power semiconductor technology | High density integration |
|---|---|---|---|---|
| Imaging quality | ★ | | | |
| Radiation dose reduction | ★ | | | |
| Low energy consumption | | ★ | ★ | |
| Dual energy | ★ | | | |
| Compact, light weight | ★ | ★ | ★ | ★ |
| Flexible, scalable | | ★ | | |
| Reliable, easy maintenance | | ★ | | |
| Cost effective | ★ | ★ | | ★ |

**High switching frequency**

Regarding the development requirements of medical CT/X-ray machine: high switching frequency plays a critical role for HV pulse converter development. The switching frequency for state-of-the art HV pulse converter products in medical CT/X-ray machines is below 100 kHz to limit the HV transformer insulation stress at high frequencies and HV transformer and voltage multiplier power losses challenges at high frequency. At these frequencies, the power density of a HV pulse converter is limited to around 1kW/L. Fig. 1-7 shows the volume distribution of a HV pulse converter [1-18].

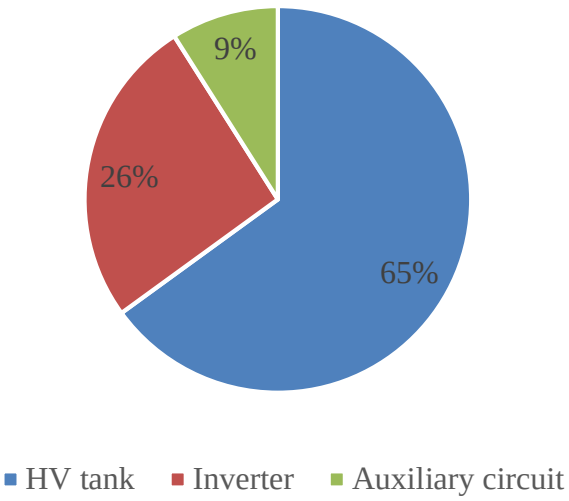



Fig. 1-7 Volume distribution for the HV pulse converter [1-18]

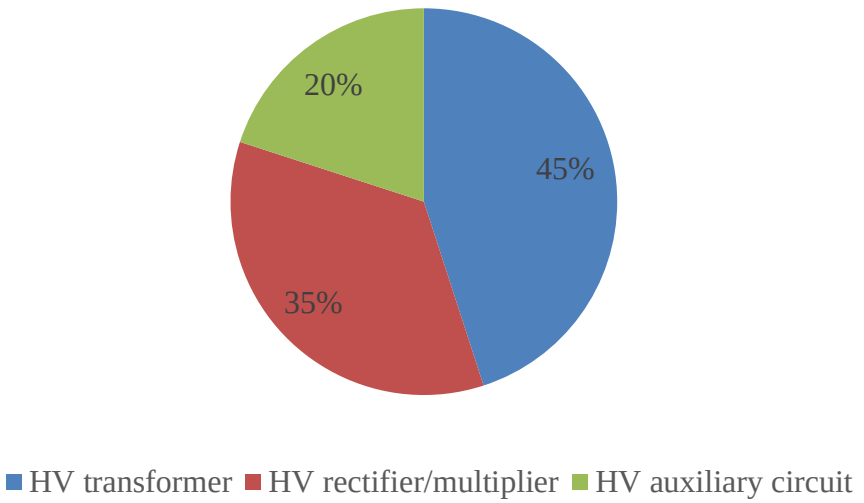



Fig. 1-8 Volume distribution for the HV tank [1-18]

The HV tank dominates the volume of a HV pulse converter. The volume distribution of a HV pulse converter is given in Fig. 1-8. HV transformers and HV rectifier/multipliers contribute to the majority of the volume. High switching frequencies can help to shrink the size of a HV pulse converter to achieve high power density and light weight performance, especially the

passive components such as the HV transformer, resonant inductor, resonant capacitor and voltage multiplier capacitors. With higher switching frequency, faster HV pulses can be realized since the HV tank capacitance can be significantly reduced. The image artefact can be mitigated due to the motion and better imaging quality can be achieved. Fast HV pulse will also help to reduce the radiation dose. Furthermore, a high switching frequency is the approach to achieve fast HV pulse switching between 80kV and 140kV with 100µs for dual energy CT. The mechanical enclosure size and required insulation oil volume can be reduced since the size and volume of the HV pulse converter can be shrunk at high frequency. The total HV pulse converter system cost can be reduced at high frequency operation.

**Modular HV architectures**

The conventional high voltage generator with a single HV transformer and rectifier or multiplier to achieve the high voltage generation suffers high insulation stress for the HV transformer and large size and low efficiency due to large parasitic-capacitance of HV transformer. High switching frequency can help to shrink the size of the HV pulse converter, especially the HV transformer and voltage multiplier capacitors. But the power loss will increase for the HV transformer due to high conduction loss and high frequency AC dielectric loss at high switching frequency. The modular HV generation architecture with a distributed HV transformer and multiplier will reduce the electrical and insulation stress for the key components in a HV pulse converter. Additionally, the power loss of a HV pulse converter can be reduced. With reduced HV insulation stress, lower voltage/power stress for the distributed HV transformer, the size of the HV tank can be reduced. In addition, the operation frequency can be further increased due to the lower parasitics from the HV transformer, reduced insulation stress, and lower winding dielectric loss. The modular architecture also helps to achieve compact size and high power density performance. Furthermore, the scalability for a HV generation system with modular HV architecture is important for mass production, and ease of manufacturing to save cost since smaller and lower voltage/power rating modules can be implemented in a cheaper technology platform, such as printed circuit board(PCB).

**SiC power semiconductor technology**

The new emerging wide band-gap materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) offer improved performance capabilities for power electronic devices compared to traditional Silicon (Si) power semiconductor devices due to the advantages of the wide band gap materials. SiC MOSFET power semiconductor devices are expected to displace silicon IGBTs and silicon MOSFETs in higher voltage and power applications wherein improved efficiency, power density and/or higher temperature operation are required. A comparison of power semiconductor device performance figures for various device technologies is shown in Fig. 1-9 [1-19]. From the device performance figure, SiC transistors are mostly targeted at high voltages beyond 1000V. SiC MOSFET power semiconductor devices provide potential loss reduction of 60 - 90% with low switching and conduction loss [1-19], [1-20]. Higher efficiency, reduced operational cost can be realized. The power density and HV pulse quality can be greatly improved since the SiC device is capable of operating at higher switching frequency (>100 kHz) due to inherent fast switching capability. It can also work at higher junction

temperature compared with existing Silicon devices and simplify the cooling requirement to enable a less expensive cooling system. The main challenge is the cost for high power SiC MOSFET module (around 5-10 times more expensive than a silicon IGBT module at current stage). The new emerging 6 inch fab will alleviate the challenge of high cost for the SiC MOSFET module.

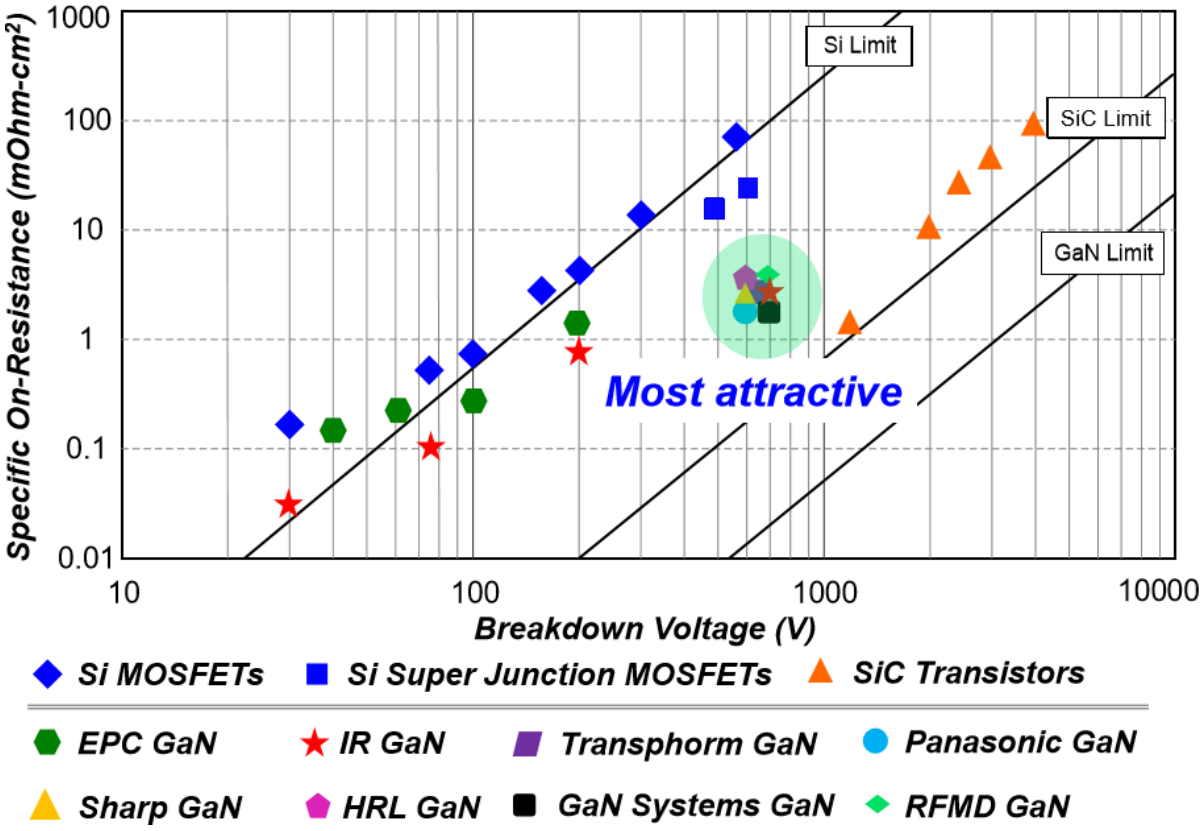



Fig. 1-9 Power semiconductor device figures of merits [1-19]

**High density integration**

Recent trends in the power electronics industry pursue higher levels of integration and better packaging techniques in order to meet the power electronics system requirements such as cost, size and power density, [1-12], [1-13]. The development trend toward increased miniaturisation of components and packages with high density integration is continuing in the electrostatic precipitator and medical CT/X-ray machine industries. High power density integration as well as packaging technologies can improve the interconnection, shrink the size of the HV pulse converter and reduce the cost of the HV pulse converter system. High density integration technologies can achieve structural, functional and processing integration to reduce component volume and labour cost. An extremely careful balance of electromagnetic, physical, thermal and spatial aspects is required for high density integration for a HV pulse converter.

There is synergy of the HV pulse converter research needed for electrostatic precipitators and medical CT/X-ray machines. The requirement of a better capability for emission reduction, faster response, sparkover handling capability and lower stress on the electrostatic precipitator electrodes request sharp pulse and higher switching frequency operation. A sharp HV pulse

and higher switching frequency operation is the enabling technology to improve the imaging quality, radiation doze reduction, and dual energy function for medical CT/X-ray machines. Low energy consumption, reliability and easy maintenance, as well as cost effectiveness are common requirements for electrostatic precipitators and medical CT/X-ray machines. So the research needs for HV pulse converter development are similar and the four key aspects are common for electrostatic precipitator and medical CT/X-ray machine applications. Low energy consumption will help to reduce the operation cost for hospital and power plants. In summary, high efficiency, a sharp HV pulse and high power density are the most critical requirements for future HV pulse converters.

## 1.2 Research questions

To meet the above requirement for further performance improvements such as efficiency, HV pulse quality and power density for HV pulse converters, the main research questions of this thesis are listed below:

**Identify the optimal HV architecture for a multi-kW 100kV HV pulse converter system supplying pulses with fast rise and decay times**

The different HV pulse converter architectures to generate high output voltages for different industrial applications with different high output voltage rating and output power rating are reported. However, state-of-the-art works do not give a systematic approach to the modularisation of architectures of a HV pulse converter. A systematic approach to derive and classify HV pulse converter architectures is required to provide a clear picture of existing or potential solutions for HV generation architectures. Furthermore, the comparative evaluation of different HV pulse converter architectures have not yet been completed in literature. It is expected that different architectures will be optimal for low power and high power applications. Therefore, it is necessary to perform an evaluation of different HV pulse converter architectures in order to select promising architectures for good performance such as high efficiency, fast HV pulse and high power density at different voltage and power levels.

**How does modularization, increasing switching frequency, packaging and insulation structures affect the HV transformer in a HV pulse converter system?**

High switching frequency operation can not only reduce the size of a HV pulse converter, especially the transformer and voltage multiplier capacitors, but it can also improve the HV pulse rise and decay times. However, the power loss will increase for the HV transformer due to high conduction loss and high frequency AC dielectric loss at high switching frequency. The modular HV pulse converter architecture with the modular HV transformer and modular multiplier is an enabler technology to reduce the stress and loss for the key components in a

HV pulse converter. However, the advantage and challenges of modularization for HV transformer has not yet been well discussed. The investigation and analysis of a HV transformer with planar and wire-wound packaging structure, as well as the HV insulation structure have not been mentioned for modular HV pulse converters.

**What are the key influence factors for multi-stage half-wave (HW) Cockcroft-Walton (CW) multiplier circuit output HV pulse waveforms?**

The HV pulse rise and decay times play a critical part for the performance of modular HV pulse converter system. But the HV pulse rise and decay times of the multi-stage voltage multiplier based HV pulse converter has not been well investigated and key influence factors of HV pulse rise and decay times have not been studied in detail. Furthermore, the diode reverse recovery process of the high frequency HV multiplier circuit has not been addressed in literature. It's important to investigate the diode reverse recovery process at a high switching frequency and to study the diode reverse recovery mitigation method in order to achieve good performance for a voltage multiplier based HV pulse converter.

**Find a generic steady state circuit model and design methodology for modular architectures**

The varying high voltage generation architectures offer greater alternatives to generate high output voltages. Simultaneously, more challenges are added in modeling and analysis due to various high voltage generation architectures. A unified steady-state model is essential and helpful to investigate the performance of modular HV pulse converter system with common architectures. This could offer effective guidelines in HV generation topology selection and find general parameter design strategies. Unfortunately, most state-of-the-art steady-state models are deduced only for the simple full-bridge rectifier and only for a specified architecture. For the voltage multiplier fed by the LCC resonant tank, the operation of the voltage multiplier is far more complex than that of the full bridge rectifier. In general, the modeling of the voltage multiplier fed by the LCC resonant tank and the various HV generation architectures are two remaining challenges to be solved. Furthermore, the design of the HV pulse converter is also challenging due to the lack of accurate models and the high degree of design freedom. The comprehensive design approach of a HV pulse converter based on power factor, quality factor and conduction angle to achieve the design of high efficiency and low components electrical stresses has not yet been mentioned.

## 1.3 Approach

Based on the aforementioned research questions, the following is the approach for this thesis:

i. *Develop a systematic approach to derive and classify the HV pulse converter architectures, evaluate different HV generation architectures and identify the most promising architectures in terms of output voltage and output power ratings.*
ii. *Analyse the effects of modularization, packaging and the insulation solution for the transformer which can be used in modular HV pulse converter architecture.*
iii. *Investigate the key factors that influence the HV pulse rise, decay times, and voltage multiplier diode reverse recovery mitigation solution.*
iv. *Develop a generic equivalent steady-state circuit model and comprehensive design procedure for modular HV pulse converter architectures.*

## 1.4 Thesis layout

A map showing the layout of this thesis is shown in Fig. 1-10, and a summary of each chapter is described below.

In Chapter 2, the state-of-the-art HV pulse converter technologies are reviewed. Firstly, the overview of existing HV pulse converter architectures are provided. Then the topology, the key power building blocks of HV pulse converter such as inverter, HV transformer and HV rectifier/multiplier are reviewed separately. Then the HV insulation and packaging for a HV pulse converter are reviewed. Finally, the research gap and thesis focus are identified from the review of HV pulse converter technologies.

In Chapter 3, the methodology of HV generation architecture derivation is developed to derive and classify HV pulse converter architectures based on modularization levels of key sub-components of a HV pulse converter. Then the comparative analysis of efficiency, power density, HV pulse quality, HV insulation stress, as well as modularity and evaluation of different HV pulse converter architectures are performed to compare the architecture's performance at different output voltage and output power ratings. Based on this, the optimal architecture is identified, and guidelines for architecture selections are recommended.

In Chapter 4, the advantages of modularization for a high frequency HV transformer are introduced firstly. Then the planar and wire-wound packaging structures, as well as HV insulation structures of a transformer in a modular HV pulse converter are presented. The detailed design considerations and technology demonstrator of a high frequency HV transformer for the modular HV pulse converter architecture are provided.

In Chapter 5, the steady state circuit analysis of the voltage multiplier is introduced to firstly provide the HV pulse drop and ripple characteristics. The key influence factors for HV pulse rise and decay times are investigated for a HV pulse converter with multi-stage voltage multiplier circuit. The diode reverse recovery process and mitigation method by using silicon carbide Schottky diodes for a high frequency multi-stage voltage multiplier circuit are addressed. Based on the analysis results performed, the hardware prototype experimental results are provided to validate the concept. The power loss analysis of high frequency voltage multiplier circuits is introduced.

In Chapter 6, the generic equivalent circuit model which can simplify the design and analysis of LCC resonant converter based HV pulse converter architectures is proposed to provide effective guidelines for analysis and design of the HV pulse converter with different architectures. The comprehensive design method by utilizing conduction angle, power factor and quality factor for the modular HV pulse converter is developed and verified by prototype experimental results.

In Chapter 7, the conclusions of the thesis and recommendations for the future research are given.

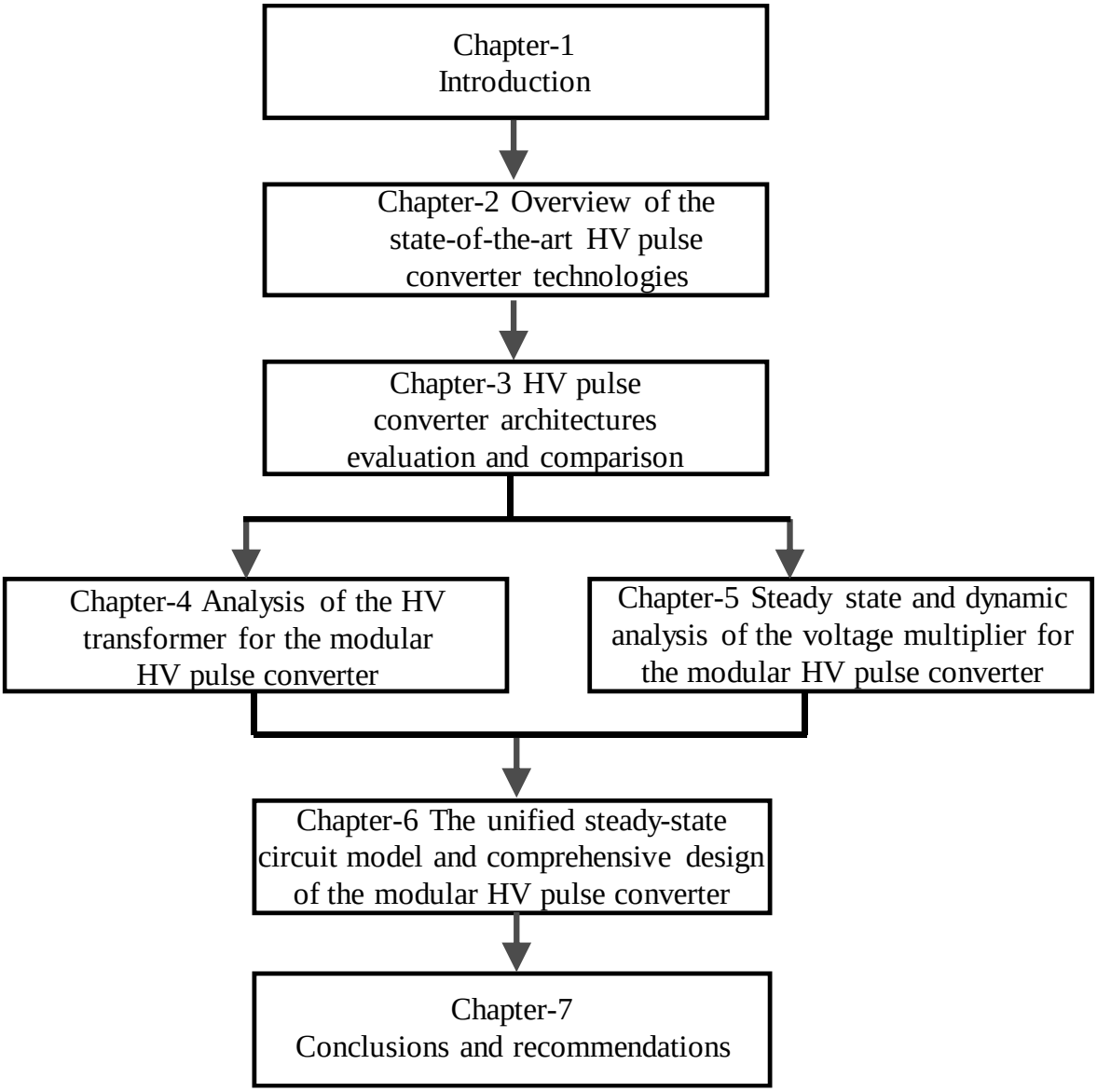



Fig. 1-10 Map of the thesis layout

## 1.5 References

[1-1] J. Bushberg, "The essential physics of medical imaging," ISBN 0-683-30118-7, 2nd edition, 2002

[1-2] J. A. Martin-Ramos, A. M. Pernia, J. Diaz, F. Nuno and J. A. Martinez, "Power Supply for a High-Voltage Application," IEEE Transaction Power Electron., vol. 23, no. 4, pp. 1608-1619, July 2008

[1-3] H. Hino, T. Hatakeyama, M. Nakaoka,"Resonant PWM inverter linked DC-DC convertor using parasitic impedances of high-voltage transformer and its applications to X-ray generator," in Proc. IEEE PESC 1988, pp. 1212-1219

[1-4] J. Sun, X. Ding, M. Nakaoka, H. Takano, "Series resonant ZCS-PFM DC-DC converter with multistage rectified voltage multiplier and dual-mode PFM control scheme for

medical-use high-voltage X-ray power generator", IEE Proceedings Electric Power Applications, 2000, vol. 147, Issue.6, pp.527-534

[1-5] S. Iqbal, G. K. Singh, R. Besar, "A dual-mode input voltage modulation control scheme for voltage multiplier based X-ray power supply," IEEE Transaction on Power Electron., vol. 23, no. 2, 2008, 1003-1008

[1-6] P. Ranstad, C. Mauritzson, M. Kirsten, and R. Ridgeway, "On experiences of the application of high-frequency power converters for ESP energization," in Proc. ICESP, 2004, pp. 1-16

[1-7] T. Soeiro, J. Biela, J. Nuhlethaler, J. Linner, P. Ranstad, and J. W. Kolar, "Optimal design of resonant dc-dc converter for electrostatic precipitators," in Proc. IPEC, 2010, pp. 2294-2301

[1-8] T. B. Soeiro, J. Mühlethaler, J. Linnér, P. Ranstad and J. W. Kolar, "Automated design of a high-power high-frequency LCC resonant converter for electrostatic precipitators," IEEE Transaction Ind. Electron., vol. 60, no. 11, pp. 4805-4819, Nov. 2013

[1-9] T. Soeiro, "High efficiency electrostatic precipitator systems with low effects on the mains," ETH PhD thesis, 2012

[1-10] H.J. Ryoo, S.R. Jang, Y.S. Jin, J.S. Kim, Y.B. Kim, S.H. Ahn, J.W. Gong, B.H. Lee and D.H. Kim, "Design of high voltage capacitor charger with improved efficiency, power density and reliability," IEEE Transaction on Dielectrics and Electrical Insulation, Vol. 20, No. 4, pp. 1076-1084, 2013.

[1-11] S. H. Ahn, H. J. Ryoo, J. W. Gong, and S. R. Jang, "Design and test of a 35-kJ/s high-voltage capacitor charger based on a delta-connected three phase resonant converter," IEEE Transaction Power Electron., vol. 29, no. 8, pp. 4039-4048, Aug. 2014.

[1-12] M. Jaritz and J. Biela, "Optimal design of a modular series parallel resonant converter for a solid state 2.88 MW/115-kV long pulse modulator," IEEE Transaction Plasma Sci., vol. 42, no. 10, pp. 3014-3022, Oct. 2014.

[1-13] Philips, http://www.usa.philips.com/healthcare/product/HCNCTB107/ct-big-bore-ct-simulator

[1-14] Siemens, https://w5.siemens.com/web/ua/ru/medecine/detection_diagnosis/surgery-c-arm-systems / Mobile-C-arm-systems/ARCADIS-Avantic/Documents/348_xp_arcadis avantic_final_26129945_5-00667284.pdf

[1-15] Spellman, https://www.spellmanhv.com/en/Products/HFe

[1-16] Alstom, http://img.saom.net.cn/pic/z114ede8-0x0-1/electrostatic_precipitator.jpg

[1-17] Alstom, the product brochure of high frequency power supplies for electrostatic precipitators (ESPs)

[1-18] S. Mao, C. Li; W. Li; J. Popovic, J. Ferreira, "A Review of High Frequency High Voltage Generation Architecture," in Proc. IEEE ECCE-Asia 2017, pp. 1-7

[1-19] S. Linder, "Power semiconductors in the electronics roadmap," in proc. International Seminar on Power Semiconductors Conference, 2008, pp. 1-29

[1-20] A. Hefner, R. Sei-Hyung, B. Hull, D. Berning, C. Hood, J. M. Ortiz-Rodriguez, A. Rivera-Lopez, D. Tam, A. Adwoa, and M. Hernandez-Mora, "Recent advances in high voltage, high-frequency silicon-carbide power devices," in Proc. IEEE IAS 2006, pp. 330-337

[1-21] J. Popović, J.A. Ferreira, “Concepts for high packaging and integration efficiency”, in Proc. IEEE PESC 2004, pp. 4188-4194
[1-22] J.A. Ferreira, J. Popović, “Packaging, Integration, Thermal management-From the State of the art to future trends”, in Proc. PCIM 2003, pp. 20-22

# Chapter 2

# Overview of the state-of-art HV pulse converter technologies

## 2.1 Introduction

HV pulse converter systems being compact in size, lightweight and with sharp pulse features are required in various industrial applications, such as X-ray generators and electrostatic precipitators. HV pulse converter technologies have been developed in past three decades. In order to choose the correct technologies to achieve good HV pulse converter performance and identify the bottlenecks against further improvements, it is important to understand HV pulse converter technologies which have already been developed. This chapter examines these HV pulse converter technologies to provide an overall picture. First, an overview of a series of architectures of HV pulse converter topologies are introduced. Then a review of HV pulse converter circuit topologies and control, key subcomponents such inverter, HV transformers, and HV rectification, as well as packaging technologies are discussed. Finally, a summary is drawn based on the review. Recommendations for HV pulse converter technologies are also given.

## 2.2 HV pulse converters architectures

Different HV pulse converter architectures have been investigated to generate HV output from low voltage input for various applications. As introduced in Chapter-1, the typical HV pulse converter circuit includes a high-frequency DC-AC inverter, a HV transformer and a HV rectifier/multiplier. The HV pulse converter circuit diagram is drawn in Fig. 2-1. The inverter, HV transformer and HV rectifier are the three key power building blocks for a HV pulse converter main circuit. In general, there are two kinds of HV pulse converter architectures according to whether the sub-components of the HV pulse converter main circuit are of single or multiple configuration. For example, a multi-level inverter or multi-phase inverter can be regarded as a multiple type inverter configuration. A combination of HV transformers in a HV pulse converter circuit can be treated as multiple transformer configurations. A rectifier or doubler is considered as a single type rectification circuit and a multi-stage voltage multiplier is considered a multiple rectification circuit. It is easier to achieve high power rating, and reduce the electric, as well as insulation stress of single sub-component for a multiple configuration HV pulse converter.

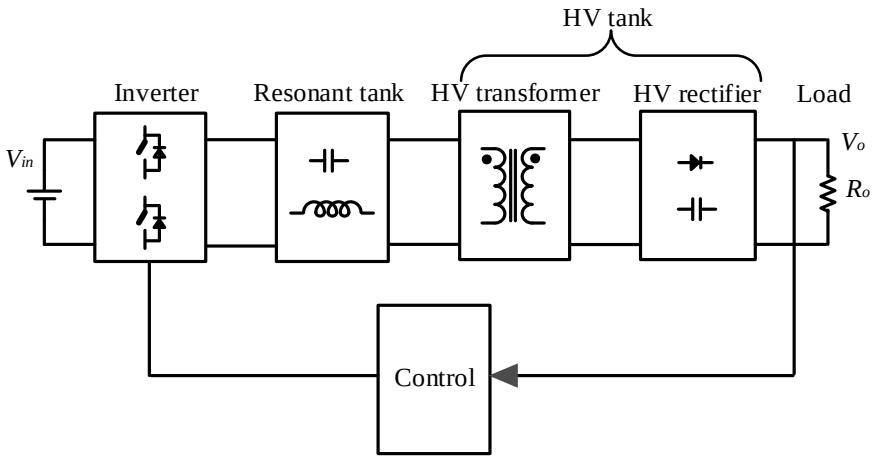



Fig. 2-1 HV pulse converter circuit diagram

### 2.2.1 Architectures with a single power building block sub-component

The HV pulse converter architecture with a single inverter, a single HV transformer and a single rectifier, shown in Fig. 2-2, is widely used for existing industrial applications [2-1]-[2-24]. The main pros and cons of HV pulse converter architectures with a single power building block are listed as follows:

*Advantages*

a) Simple structure.
b) Fast HV pulse speed, low output voltage ripple with diode rectifications.

*Disadvantages*

a) Insulation stress for the HV transformer is very large since it relies on a single HV transformer to achieve HV step up. The insulation design is complex and the size of HV transformer is large.
b) The switching frequency is limited due to large parasitic capacitance and high leakage inductance of HV transformer.
c) Not scalable for different output voltage and power rating
d) The power density and efficiency improvement are challenged due to high insulation stress and large parasitic components for the HV transformer when the switching frequency is further increased.

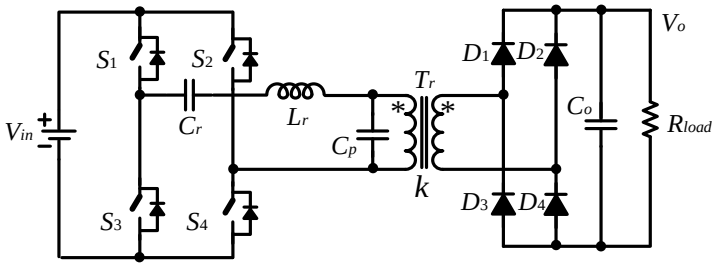



Fig. 2-2 Circuit diagram of HV pulse converter architecture with a single inverter, a single HV transformer and a single rectifier

### 2.2.2 Architectures with multiple power building block sub-components

The Cockcroft-Walton voltage multiplier was introduced for the HV pulse converter to achieve the required high output DC voltage [2-25]-[2-39]. With the voltage multiplier, the insulation stress for a HV transformer can be largely reduced, unlike with the single rectifier configuration architecture, and this leads to a reduction of insulation stress for a HV transformer.

The multiple transformers configurations based HV pulse converter architectures are used together with a rectifier and connected in series so that the insulation stress of each transformer can be greatly decreased. Fig. 2-3 illustrates the circuit diagram of an example of the modular HV pulse converter architecture with a single inverter, multiple HV transformers and single rectifier. The connection of the transformer's primary sides can be either series or parallel. The series connection is suitable for a higher input AC voltage, and parallel connection is suitable for a large current application [2-40]-[2-49].

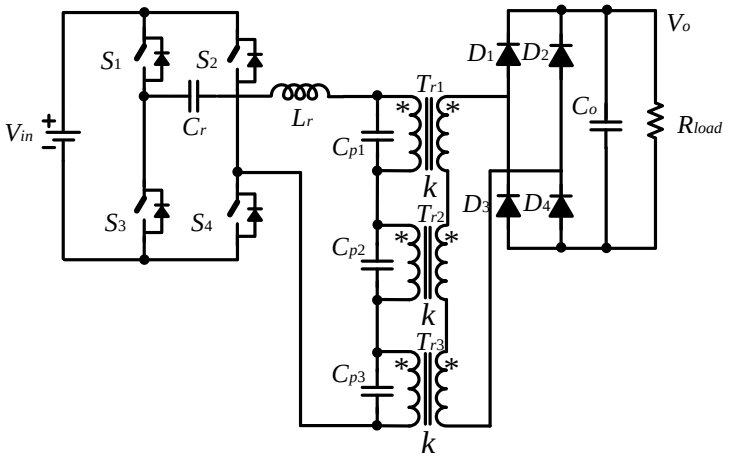



Fig. 2-3 Circuit diagram of a single inverter, multiple HV transformers and single rectifier based modular HV pulse converter architecture

Multi-level inverter or multi-phase inverter configurations will reduce the voltage stress or current stress for inverter power semiconductor devices at high power rating [2-50]-[2-56]. Furthermore, the most complex HV pulse converter architecture combines multiple inverters, multiple HV transformers, and multiple rectifiers provide full modularity for a power building block for HV pulse converter main circuit subcomponents [2-57]-[2-81]. The main pros and cons of HV pulse converter architectures with multiple power building blocks are listed as follows:

*Advantages*

a) Modular structure.
b) Scalable for different output voltage and power rating.
c) Insulation stress and parasitic components can be smaller due to reduced turns ratio for a HV transformer with multi-stage multiplier rectifications.
d) Power density and efficiency improvement with high switching frequency operation.

*Disadvantages*

a) Power sharing between multiple power building blocks.
b) The variance of HV transformer parasitics including magnetizing inductance, leakage inductance, winding capacitance due to the magnetic core characteristics difference and inconsistent manufacture process will lead to the voltage and current sharing challenges for modular HV pulse converter architectures. Furthermore, the variance of multiplier capacitor and the parasitic capacitance and inductance of the HV multi-stage multiplier circuits will also impact on the voltage and current sharing for modular HV pulse converter architectures.
c) HV pulse rise and decay time, low output voltage ripple challenges due to multi-stage multiplier rectifications
d) The HV pulse speed is related to the stage number of multi-stage multiplier rectifications. The HV pulse speed slows when the stage number of multi-stage multiplier are larger.

## 2.3 Topologies, model and control

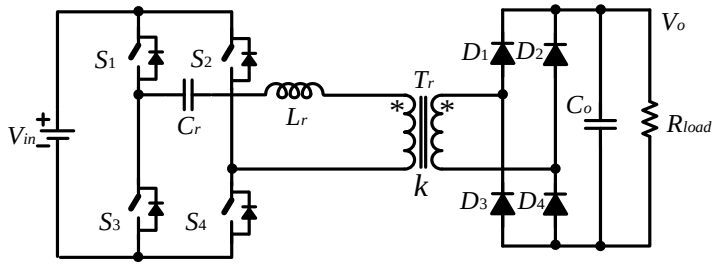
### 2.3.1 Topologies for HV pulse converter

Due to the required high output voltage level of a HV pulse converter, a high turns-ratio transformer is usually adopted to boost voltage and a large insulation distance is needed. As a result, the leakage inductance and parasitic capacitance of the transformer cannot be ignored when it comes to choose the appropriate topology for a HV pulse converter, especially in high frequency conditions. The resonant converters, which can utilize the transformer parasitic capacitance, provide obvious advantages compared with pulse width modulation (PWM) converters. Large leakage inductance and parasitic capacitance of HV transformers can be utilized as part of the resonant tank in resonant converters, while in PWM converters they are harmful to efficiency improvement. In resonant converters, resonant current in the primary side of transformer is approximately sinusoidal under all load conditions, which enables the zero-current switching (ZCS) or zero-voltage switching (ZVS) of devices including switches of the inverter and diodes of the rectifier. As a result, high efficiency operation can be ensured.

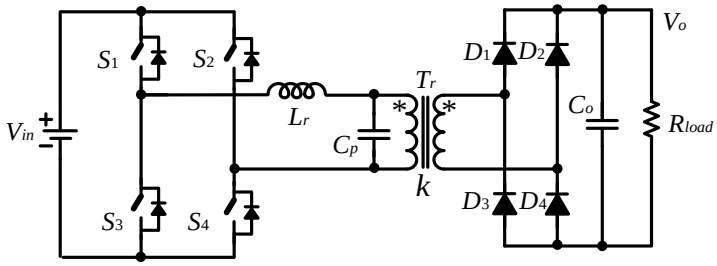
Series resonant converters (SRC) and parallel resonant converters (PRC) are two basic topologies of resonant converters [2-82], as depicted in Fig. 2-4(a) and (b). The capacitive output filter is preferred since HV filter inductor is not required. The advantage of SRC is the reduction in the current stress of power device with a decrease in load. This will lead to the conduction loss reduction for the power switching device as the load decreases, consequently preserving high part load efficiency. The parasitic capacitance of a HV transformer cannot be utilized by the SRC and will deteriorate circuit behaviour. Another drawback of the SRC is that the frequency band to achieve output voltage regulation over an entire range of loads will be very large. Therefore, the optimization of the SRC is very difficult from light load to full load. The maximum voltage gain of the SRC is only one. The limited voltage gain of SRC introduces the burden for the transformer and rectification circuit. A large turns ratio of the HV

transformer, and multi-stage multiplier circuit, can realize the required voltage gain lead to large leakage inductance and parasitic capacitance for the HV transformer as well as HV pulse speed decrease [2-83].

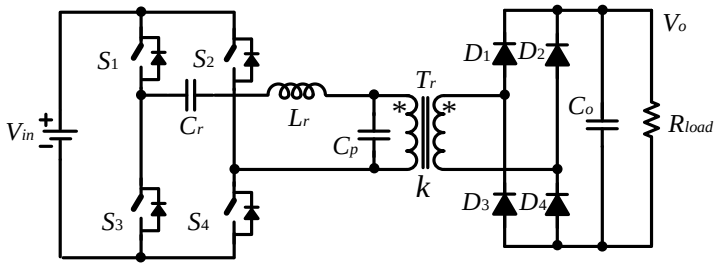
PRC makes use of the parasitic capacitance parameters of a HV transformer. Meanwhile, the transformer leakage inductance appears in series with the resonant inductor. Consequently, the PRC topology can integrate the HV transformer parasitics very well and then the transformer nonidealities do not degrade operation of the converter. The voltage gain of PRC can be larger than one, which can help to reduce the turns ratio of the HV transformer, or stage number of the voltage multiplier circuit. The main disadvantage of PRC is high device current stress which is relatively independent of load. The PRC will suffer poor efficiency at light load conditions. It's difficult for PRC to manage the good voltage regulation at the entire load range since PRC provides good voltage regulation at light load, but bad regulation at heavy load [2-83].




(a) SRC converter [2-83]




(b) PRC converter [2-83]




(c) LCC converter [2-84]

Fig. 2-4 Resonant converter topologies for the HV pulse converter

To combine the advantages of SRC and PRC, the Series-Parallel (LCC) resonant converter is widely adopted for HV pulse converter applications [2-84], as depicted in Fig. 2-4(c). The LCC converter can fully absorb the transformer parasitic components. The current in the inverter switches and resonant tank decreases as the load decreases, which ensures good efficiency at light load and no load. Furthermore, the LCC converter exhibits better control characteristics over the entire load range than the conventional two elements resonant converters with an additional resonant element.

### 2.3.2 Modeling and Control

It is complex to acquire the accurate model of a LCC converter due to coupling of different resonant frequencies. Some simplified analysis methods are proposed to acquire a mathematical model with acceptable accuracy. Since a resonant current in the primary side of the transformer is approximately sinusoidal, the most widely used method in modeling of an LCC converter is based on First Harmonic Approximation (FHA), which utilizes the fundamental components of current and voltage in analysis [2-21]. In [2-85], the secondary part of the transformer is replaced by an equivalent RC network, as depicted in Fig. 2-5. $R_{eq}$, $C_{eq}$ are equivalent models of rectifiers, capacitor and load network. Based on the FHA model, further analysis and design are achieved with satisfactory results. [2-5], [2-34] give a dynamic and steady-state model of LCC converter. The step by step design procedure for a LCC converter is provided in [2-6], [2-17].

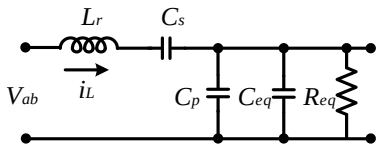



Fig. 2-5 Equivalent RC network of secondary side [2-85]

It can be demonstrated from Fig. 2-5 that the fundamental component of transformer voltage is decided by the impedance of the resonant tank and equivalent RC network, hence

$$\frac{V_{T(1)}(s)}{V_{ab(1)}(s)} = H(s) \tag{1}$$

To a given LCC converter, $H_{(s)}$ is influenced by an operating point including frequency and load resistance. Ignoring harmonics, $V_{T\ (1)}$ is proportional to output voltage. Thus, it is concluded that output voltage is controlled by switching frequency and duty cycle. The main control objective of a LCC converter is to regulate output voltage and enable soft switching at the entire load range. The output voltage can be controlled by frequency and duty cycle. The soft switching condition is deeply affected by impedance of the resonant tank. The simplest control schedule of the converter is 50% duty cycle with variable frequency, known as the voltage frequency (VF) method [2-6]. In this method, if impedance of the resonant tank is capacitive, it means that the fundamental component of input voltage has a phase lag behind the current. It is possible to turn off switches when the phase current reaches zero, however, hard turn-on occurs in this mode if the converter works in continuous conduction mode (CCM).

If the impedance of the resonant tank is inductive, ZVS can be achieved for all switches. However, VF control has reactive power in a resonant tank, as shown in the shaded area in Fig.2-6(a), the conducting loss increases especially under light load conditions. To solve this problem dual control, which regulates switching frequency to ensure ZCS of one phase leg of inverter and ZVS for the other and uses duty cycle to regulate output voltage, is proposed as an improvement of VF control in in Fig.2-6(b) [2-6]. In this control scheme, circuiting energy disappears and improved efficiency can be acquired. The drawback of this strategy is addition of a current polar detection circuit. The key waveform comparison of VF control and dual control strategy is depicted in Fig. 2-4.

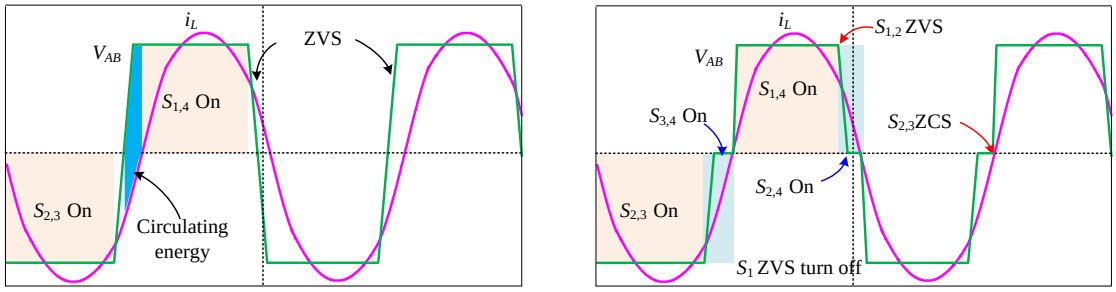
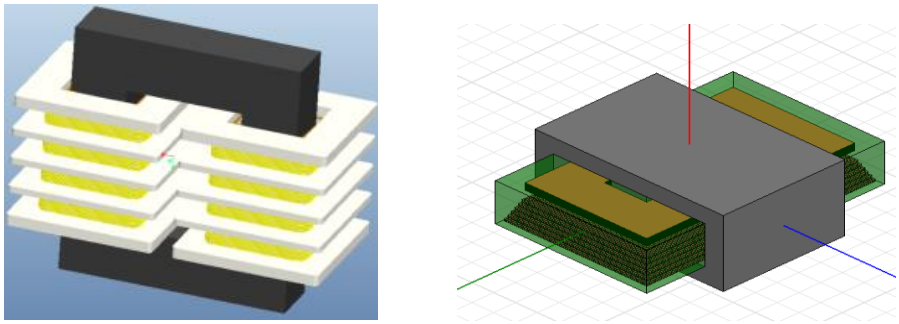



Fig. 2-6 Key waveform of LCC (a) VF control; (b) Dual control

## 2.4 HV transformers

### 2.4.1 Transformer structure



(a) non-planar barrel structure (b) planar structure

Fig. 2-7 Non-planar barrel and non-planar barrel HV transformer structures

Compared with a low voltage transformer, large turns ratio and insulation requirements are the main differences of a HV transformer. The transformer is implemented using magnetic cores of different shapes and various magnetic materials. The windings of the transformer can be implemented in different manners such as wire-wound, planar printed circuit board (PCB), copper foil and helical winding technologies. Regardless of the magnetic core shapes and winding technologies utilized, the transformer can be constructed using two packaging structures: planar and non-planar barrel type [2-87]. The non-planar barrel and planar HV transformer are illustrated in Fig. 2-7(a) and Fig. 2-7(b) respectively [2-15], [2-26], [2-88]. The non-planar barrel HV transformer is implemented using various core shapes, such as ring-shaped and E- and I-shaped cores. The primary and secondary windings which are composed of solid and litz wire or copper foil are wound on a bobbin. The bobbin provides the essential

insulation capability between the HV transformer windings to magnetic cores. The primary winding is typically low voltage winding. The secondary winding is high voltage winding. Sufficient insulation distance between secondary winding and primary winding and magnetic core is required. The wire ends are interconnected to the electrical terminals, in the form of pins, by welding. The conventional non-planar barrel HV transformers are widely used in most of today's HV pulse converters. However, due to construction process such as winding, the uniformity of transformers is poor. Additional limitations are large size, complex bobbin, and bad parameter repeatability for high power density low profile applications.

As there is an increasing demand for cost-effective automated assembly and miniaturization, the planar HV transformer is attractive. It is generally constructed by a multi-layer PCB, or a disk shape copper foil. The bobbin is usually not required for planar structure. Furthermore, the flat or planar ferrite core can be used together with a planar PCB or copper foil to achieve the low profiles. The advantages of planar structure are low profile, power density, excellent repeatability of component characteristics, easy manufacturing, modularity, and integration with a PCB [2-26]. The heat dissipation of the internal layer of multi-layer PCB windings of a planar HV transformer needs to be considered. Furthermore, the high frequency dielectric loss for the multi-layer PCB windings will contribute significant loss to the total HV transformer winding losses.

### 2.4.2 Magnetic core materials

Characteristics of magnetic core materials have an influence on the power density and efficiency of HV transformers. The commercial available magnetic core materials are shown in Fig. 2-8. They can be divided into metal soft magnetics and ferrite magnetics [2-86].

The available magnetic core materials in the frequency zone from 1kHz to 1MHz are depicted in Fig. 2-9 [2-86]. Comprehensively considerations are needed when choosing proper magnetic core material. The following aspects need to be considered.

1) Permeability: Core materials should have higher permeability to acquire high power density.

2) Saturation flux: High saturation flux is required to increase the current capability of a transformer.

3) Loss density characteristics: The core loss of a transformer is affected by many aspects such as flux and operation frequency, as well as temperature.

4) Cost: amorphous and nanocrystalline materials have preponderant properties, but due to the production process, their prices are relatively high compared with ferrite magnetic material.

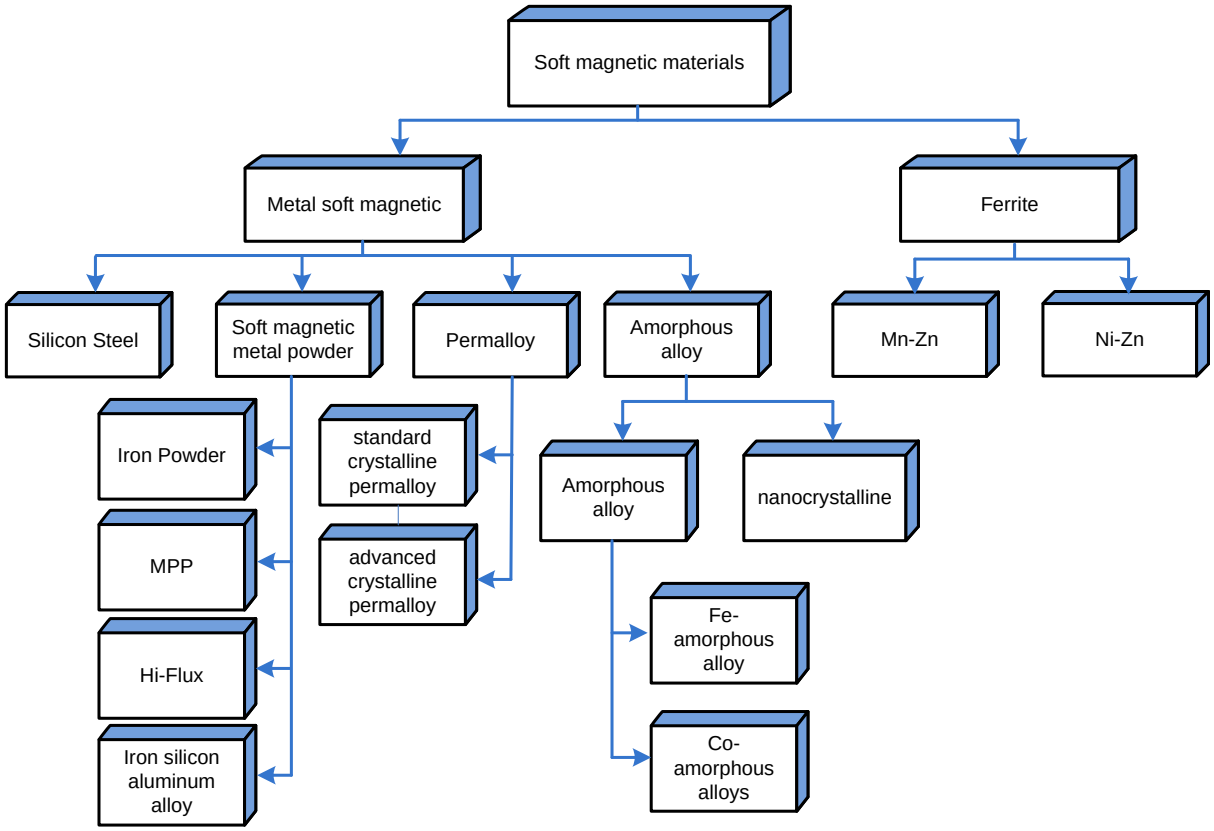



Fig. 2-8 Family of commercial available magnetic core materials [2-86]

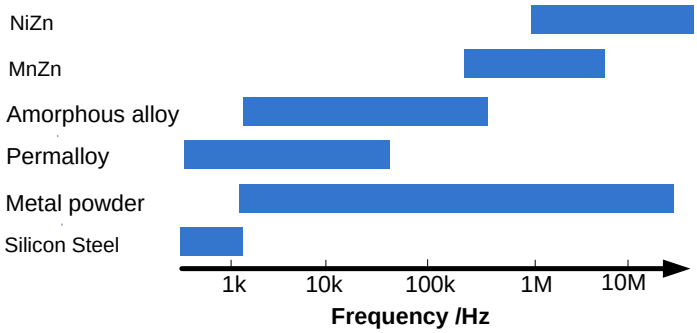



Fig. 2-9 Operating frequency of magnetic core materials [2-86]

### 2.4.3 Insulation materials

The output voltage ranges of the investigated HV transformer will be from a few tens to several hundreds of kilovolts. The insulation architecture is a key influencing factor for the volume and power density of a high frequency HV transformer. The insulation between the magnetic core to primary winding (low voltage winding) and the secondary winding (HV winding), insulation between the primary winding to secondary winding, and the insulation inside the secondary winding all need to be considered. Several factors need to be considered when choosing the insulation mediums:

1) Electric Insulation capability. Higher insulation capability will reduce the insulation distance, thus reducing the volume of the transformer and consequently converter.
2) Dielectric loss. Lower dielectric loss can improve the efficiency of the transformer, especially in high frequency high voltage applications, where dielectric loss proves to be a significant part of the total loss.
3) Thermal conductivity. The insulation medium fills the space between the transformer core and winding. It is vital to dissipate the heat generated by the transformer. Higher thermal conductivity materials should be chosen to lower temperature of the transformer and improve reliability.
4) Dielectric constant. Lower dielectric constant will help reduce the stray capacitance of the transformer, which influences the performance of resonant converters.

There are three types of insulation medium: insulation oil, gas or solid insulated materials. Their characteristics are shown in Table 2-1.

The insulation oil such as mineral oil, silicone oil or and synthetic oil is widely used for HV transformer insulation. Insulation oil serves the purpose of insulating HV components with different voltage potential. Meanwhile, the oil helps heat dissipation for the HV transformer. The advantage is the fluidity, making the insulation self-healing, and the ease of heat dissipation. So, the oil insulation is suitable for high power rating up to hundreds of kilowatts, but the mechanical and plastic bobbins are required as a support function. The insulation capability of oil can achieve 10~15kV/mm after oil filtering and vacuumization. However, the oil tank gives some concerns, such as leakage, and environmental issues. Dust, contamination, humidity and vibration typically will degrade or affect the oil tank insulation performance.

Silicon solid insulation resin can achieve high insulation capability above 20 kV/mm. The insulation structure is simple since the mechanical and plastic bobbin is not required. It is promising for low power rating around a few hundreds of watts for compact size, low maintenance and cost reduction. Drawbacks of solid insulation are not self-healing insulation and weak heat dissipation inside the solid insulated HV transformer.

The insulated gas such as sulfur fluoride (SF6) is widely used in gas insulated switchgear (GIS) up to 550kV. The insulation capability is around 8.5kV/mm. Gas insulation has the advantage of being lightweight and it is suitable for low power and portable applications. But the thermal conductivity of insulated gas is quite low, and the heat dissipation is challenged. So, the power rating is limited by several hundreds of watts to few kilo watts. Furthermore, the gas insulated structure has potential leakage and reliability issue.

The hybrid insulation solution with insulated oil plus solid insulation material such as polypropylene and polytetrafluoroethylene can be promising for high dielectric strength and, combined with high thermal conductivity, will lead to compact high density insulation and good thermal capability for the high voltage generator with increased power rating capability.

The high frequency, HV insulation properties of insulation oil, solid insulated materials, and Gas (SF6) are summarized in Table 2-1 [2-86]-[2-88]. The insulation material characteristics

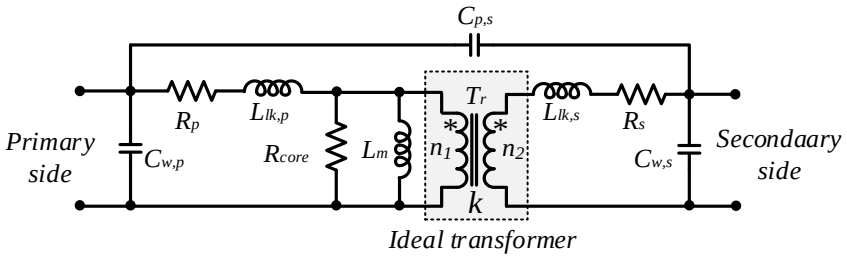
such as break-down voltage and dielectric power loss at high frequency AC voltage impact on the HV tank parasitical capacitance insulation margin, volume and thermal performance.

Table 2-1 Characteristics of insulation mediums

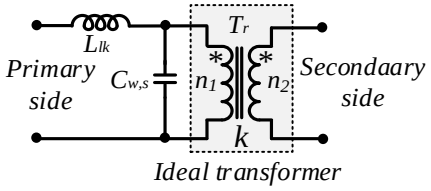
| Insulation mediums | Insulation capability | Advantages | Disadvantages |
|---|---|---|---|
| Transform oil | 10~15kV/mm | Self-healing, easy for heat dissipation | HV bobbin needed, leakages, and environmental issues |
| Solid insulated materials | >20 kV/mm | No HV bobbin needed | No self-healing, weak heat dissipation |
| Gas(SF6) | 8.5kV/mm | Light weight | Gas(SF6) |

### 2.4.4 Equivalent circuit model

The equivalent circuit model of a transformer is depicted in Fig. 2-10 (a). The equivalent circuit model of a HV transformer can be simplified for analysis as depicted in Fig. 2-10(b) [2-5]. It is important to acquire the leakage inductance and parasitic capacitance of HV transformers since they are part of the resonant tank and their values have an influence on the performance of LCC [2-12], [2-42], [2-76], [2-87]. The analytical calculation and finite element method (FEM) simulation are two basic methods to calculate stray parameters. [2-12], [2-42] give an analytical expression on the stray capacitance of transformers. The calculated error is around 20% compared to the measured one. [2-2] provides a theoretical calculation of the transformers.




(a) Equivalent circuit of a transformer [2-5]




(b) Simplified model for a HV transformer [2-5]

Fig. 2-10 Circuit model of a HV transformer

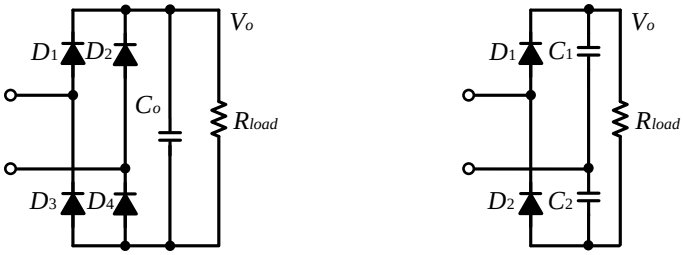
### 2.4.5 Design procedure of HV transformer

Traditional design methods for transformers do not consider insulation distance, which is the key feature of HV transformers, thus they are not suitable for HV transformers. [2-92] demonstrates a step by step design process of middle frequency transformers with a high insulation distance. A detailed design procedure is given in this article. [2-2] provides a simple introduction on planar HV transformer design. [2-93] discusses the optimized procedure to improve the performance of transformers. The loss calculation of HV transformers is another key area of concern. The power loss of high frequency transformers contains core loss, winding loss, dielectric loss. [2-92] gives a review on the loss calculation of HV transformers. The proposed loss calculation model is analytical and comprehensive.

## 2.5 HV rectification

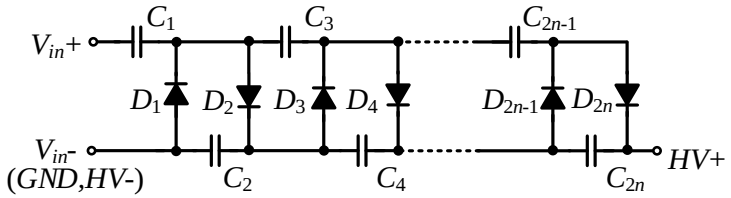
### 2.5.1 Topologies

The circuits of a full bridge rectifier and voltage double rectifier are illustrated in Fig. 2-11. The voltage multiplier combines diodes and capacitors to further increase the voltage of high voltage transformer, and to rectify high output voltage DC. The well-known series of voltage multipliers, Cockcroft-Walton(CW) voltage multipliers, are depicted in Fig. 2-12(a-d) [2-94].

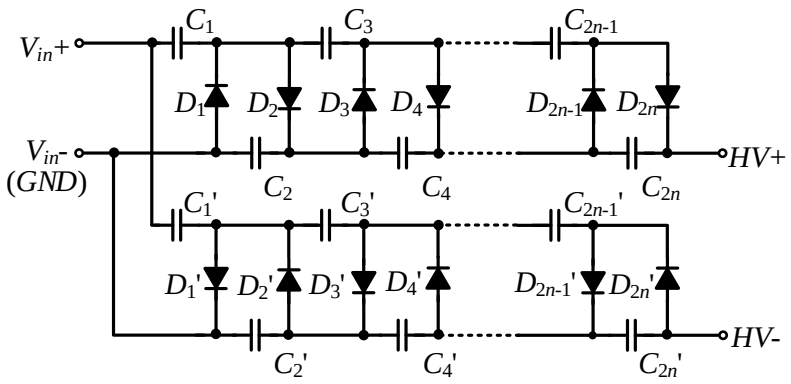



(a) Full bridge rectifier (b) Voltage doubler rectifier

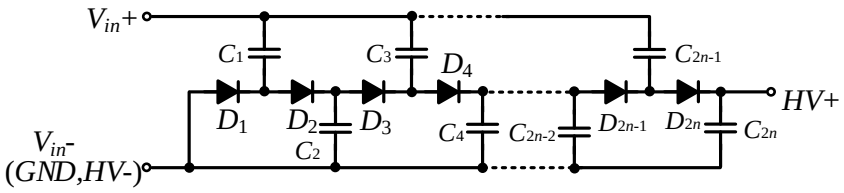
Fig. 2-11 Circuits of full bridge rectifier and voltage double rectifier



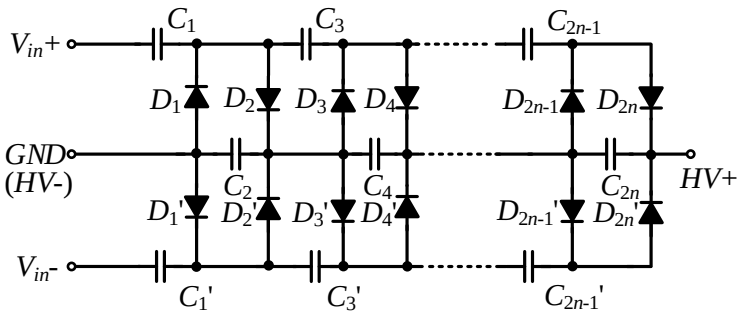

(a) Single polarity half-wave series CW voltage multiplier




(b) Dual polarity half-wave series CW voltage multiplier




(c) Single polarity half-wave parallel CW voltage multiplier




(d) Full-wave Series CW voltage multiplier

Fig. 2-12 Topology of Cockcroft-Walton voltage multiplier [2-94]

### 2.5.2 Characteristics of a voltage multiplier

Static analysis of a basic CW voltage multiplier has been investigated in [2-27], [2-94]. Both the voltage multiplier and transformer can boost output voltage. Thus, they are often combined to acquire high output voltage. The stage number of the voltage multiplier and turns ratio of a HV transformer need to be an optimal trade-off from the system's perspective. The high frequency HV multiplier design and packaging also has a large impact on the HV tank volume and weight. The forward and reverse recovery process, junction capacitance and equivalent parasitic capacitance characteristic's modelling of HV SiC Schottky diodes are introduced in [2-1], [2-14], and [2-32]. Based on steady state analysis of the voltage drop and voltage ripple, an improved distribution of capacitance on each stage to achieve high output voltage with minimum total capacitance is proposed [2-95].

## 2.6 Packaging

### 2.6.1 Packaging technology for the HV pulse converter

Packaging technology plays an important role for a high frequency HV pulse converter system. According to the definition of power electronics packaging, it is the combination of engineering and manufacturing technologies required to convert an electrical and thermal circuit as well as electromagnetic design into a manufactured assembly [2-96]. Packaging is performed on the assembly level and includes using packaging elements to convert the functional elements set into a power electronic converter according to the output of the fundamental function optimization (electrical circuit schematic, thermal circuit schematic and electromagnetic energy flow). Typical package elements include a semiconductors lead, a components lead, encapsulation and housings, carrier dielectrics, a bobbin and lead, and thermal adhesives [2-97]. Packaging technology greatly depends on different high voltage generation architecture. The power electronics packaging technology in the scope of this investigation means the components' packaging level such as the HV transformer, the voltage multiplier, other HV components and assembly packaging for the HV tank. There are 2 levels of packaging for a HV pulse converter:

a) Component packaging level: includes packaging elements that are physically part of a self-standing component. The main researches are high voltage, high power loss elements including a HV transformer, voltage multiplier and inverter.
b) Assembly packaging level: other packaging elements in a converter.

The packaging elements for a HV pulse converter are illustrated in Fig. 2-13. For the components packaging level, there are two kinds of technologies. One is surface mount technology(SMT), and the other is through hole technology(THT) [2-97]. The HV pulse converter system assembly and packaging technologies include HV transformer concentrated, PCB based packaging and 3D power packaging.

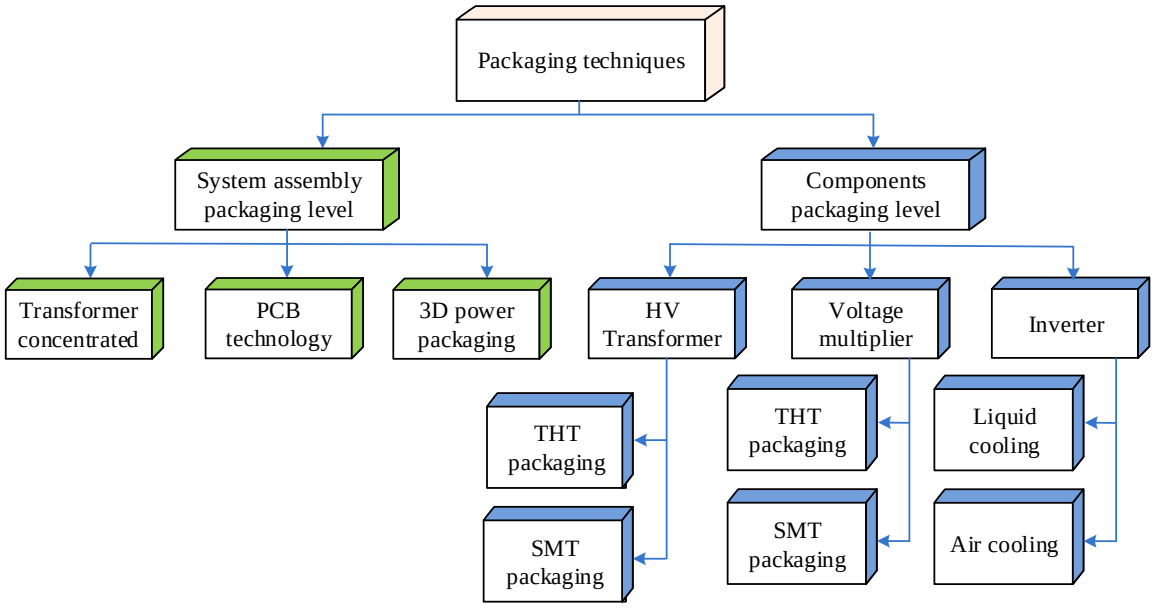



Fig. 2-13 Packaging elements for the HV pulse converter

### 2.6.2 Components packaging level

1) HV transformers

Planar and non-planar HV transformers are main structures. Fig. 2-14 demonstrates a series of transformers with different thermal dissipation or insulation methods. The HV transformer can be insulated by oil or solid materials. For large output power applications, oil insulation is commonly used as an insulation medium and heat dissipation medium.


(a) Planar HV transformer [2-14] (b) Non-planar barrel HV transformer [2-2]

Fig. 2-14 Packaging of HV transformers

2) Voltage multipliers

The interconnection of HV diodes and HV capacitors can be through direct soldering or based on PCB boards as shown in Fig. 2-15. Care needs to be taken with soldering to avoid sharp edges to prevent the generation of a high electric field. The planar packaging technology can help achieve a planar structure for a voltage multiplier. A planar diode and planar capacitor can be interconnected by a PCB board. Not only can the parasitic parameters of the loop circuit be reduced, but also planar compact packaging can be achieved.

(a) Interconnection by direct soldering (b) Interconnection with PCB

Fig. 2-15 Packaging structures of the voltage multiplier

3) Inverter

The packaging of a high frequency inverter is not a bottleneck since the inverter is usually out of the HV tank. The high frequency inverter will be considered only when the inverter components are packaged together with the HV tank. Air cooling is adopted for a low power

inverter. While in high power applications, liquid cooling package is an alternative, as shown in Fig. 2-16 [2-13].

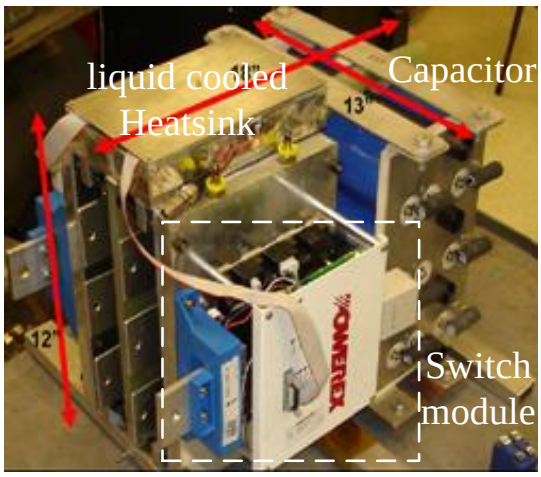


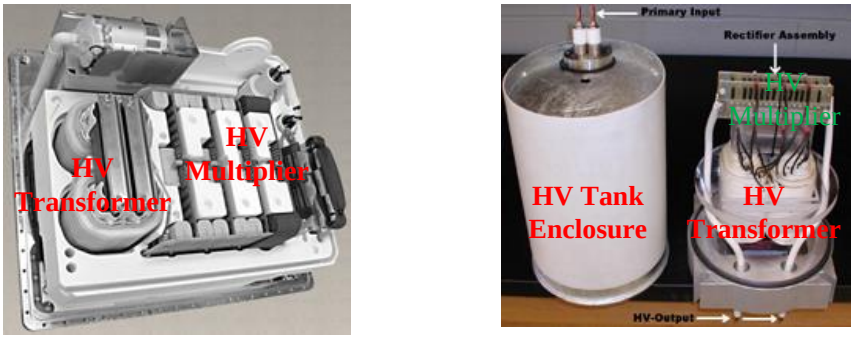

Fig. 2-16 Inverter packaged with liquid cooled heat sinks [2-13]

### 2.6.3 Assembly packaging level

(a) Packaging centralized on HV tank insulation

The majority of a HV tank packaging structure is centralized on HV transformer insulation since the high voltage transformer insulation dominates the HV tank volume and size. Fig. 2-17 illustrates two pictures of packaging centralized on HV transformer insulation [2-26], [2-32]. The HV bobbin is usually required for mechanical holding and insulation. The HV tank is covered with insulation oil for insulation and thermal management. Another option would be solid insulation for the HV tank. Silicone gel can be also used as solid insulation material. HV bobbin or oil are not required. The drawback is the limited heat dissipation inside the solid insulated HV tank.

For the HV multiplier, circuit boards and housing are required to achieve insulation and mechanical support and interconnection inside the voltage multiplier components. HV insulated cable is required for interconnection between the HV transformer and voltage multiplier. The insulation between the HV transformer, voltage multiplier, interconnection cable and enclosures needs to be carefully considered.




(a) [2-26] (b) [2-32]

Fig. 2-17 Packaging centralized on HV transformer insulation

(b) Packaging by PCB technology

The HV transformer windings and voltage multipliers are embedded in a multilayer PCB assembly with reduced interconnections between the subassemblies shown in Fig. 2-18. The insulation layer between each PCB layer needs to be added. This kind of HV packaging has good coherence, and easy interconnections.

For the voltage multiplier, the HV rectifier and capacitor can be packaged on the PCB by the through-hole or surface mounted methods. With the PCB technology, the interconnection between the HV transformer and voltage multiplier can be achieved with PCB traces embedded in the multilayer PCB. An integrated packaging structure can be achieved with a simplified insulation and interconnection structure [2-98].

There are some limits for PCB packaging technology for HV applications. The breakdown strength of the PCB needs to be considered for HV packaging. The typical FR-4 laminate will be about 0.2 W/m/K, the thermal characteristics of PCB laminates needs to be taken account of HV pulse converter packaging.

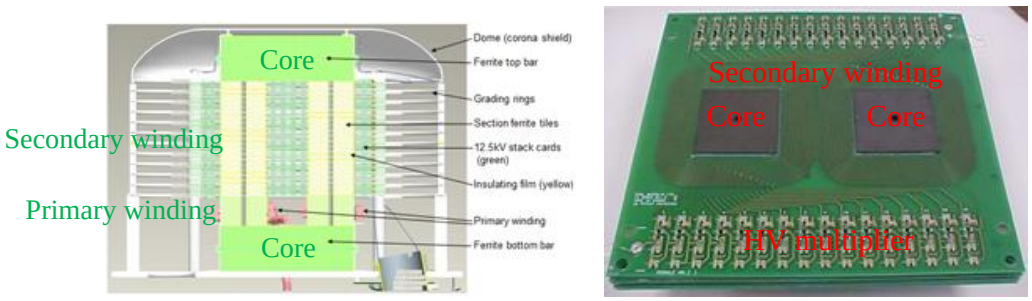



Fig. 2-18 Packaging by stacked printed circuit board (PCB) technology [2-98]

(c) Packaging centralized on HV tank insulation

The three-dimensional (3D) assembly and integration technologies will potentially help to achieve higher power density for HV pulse converters [2-99]-[2-100]. Fig.2-19 provides a 3D packaging example of a folded 3D PCB converter with 250W/L power density which is 67% higher than the conventional 2d design [2-99].

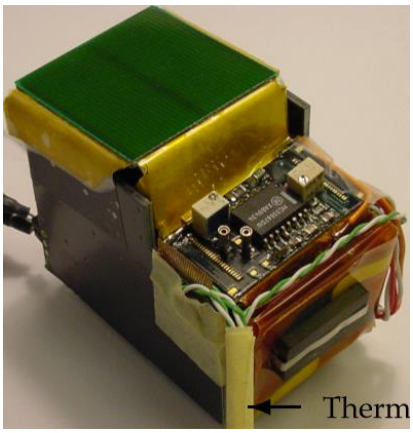


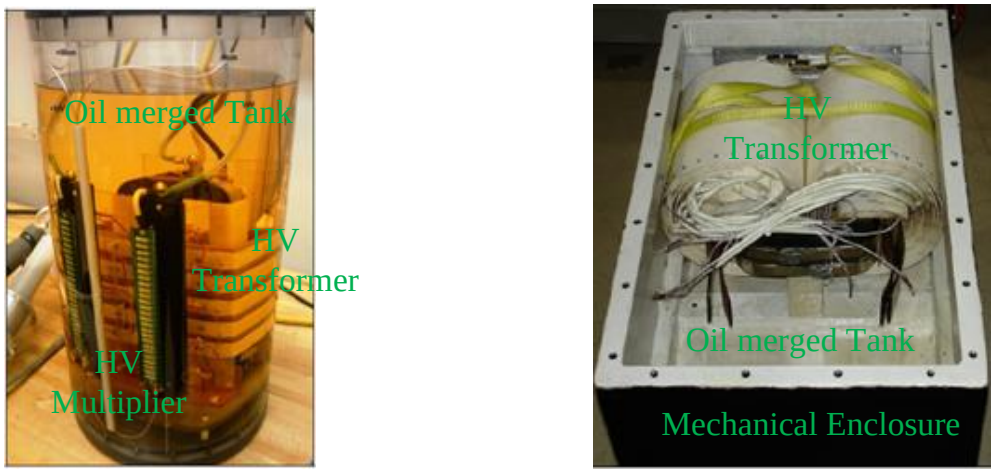

Fig. 2-19 Packaging by stacked printed circuit board (PCB) technology [2-99]

### 2.6.4 Cooling

Packaging of HV converters is deeply affected by HV insulation and cooling solutions. There are basically two cooling solutions, passive cooling and active cooling. Passive cooling refers to cooling technologies that rely solely on the thermo-dynamics of conduction, convection and radiation to complete the heat transfer process. This is one of the most common cooling methods, other examples being heat sinks, heat spreaders, heat pipes and thermal interface materials. Active cooling refers to cooling technologies that must introduce energy, typically from an external device, to augment the heat transfer process. Active cooling uses forced air (additional fan, air cooled), forced liquid, synthetic jet technology, solid-state heat pumps to dissipate heat [2-101]-[2-102].

The HV tank can be cooled with insulation oils by thermal convection. The heat can be dissipated through the HV tank enclosure by thermal conduction and radiation and heat of the HV tank enclosure can be dissipated to ambient air by heat radiation. The following are two HV transformers assembled in a HV tank with passive oil cooling in Fig. 2-20. The mechanical enclosure can also dissipate the heat through the oil in the HV tank. The passive cooling method is easy for packaging, and is cost effective. But the heat dissipation capability is limited, especially for high power rating [2-101]-[2-102].

In order to achieve high power density in the transformer construction, active cooling concepts are preferred over passive heat extraction. Some of these active cooling concepts are now outlined for each of the parts generating losses within the transformer. As shown in Fig. 2-21, The heat sinks attached to the transformer core can be forced-air-cooled or water-cooled. A water-cooled heat sink is placed around each leg of the core. The heat pipe can be used to surround the low voltage winding for heat dissipation. Furthermore, a water or forced air-cooled heat sink attached to the external face of the cast insulation, braided copper hollow conductor with internal plastic hose carrying water and forced-air-cooled HV cable can be used for HV tank cooling as illustrated in Fig. 2-22. The disadvantages are the complexity, additional cost and reliability [2-103].




(a) [2-101] (b) [2-102]

Fig. 2-20 HV tank with passive oil cooling

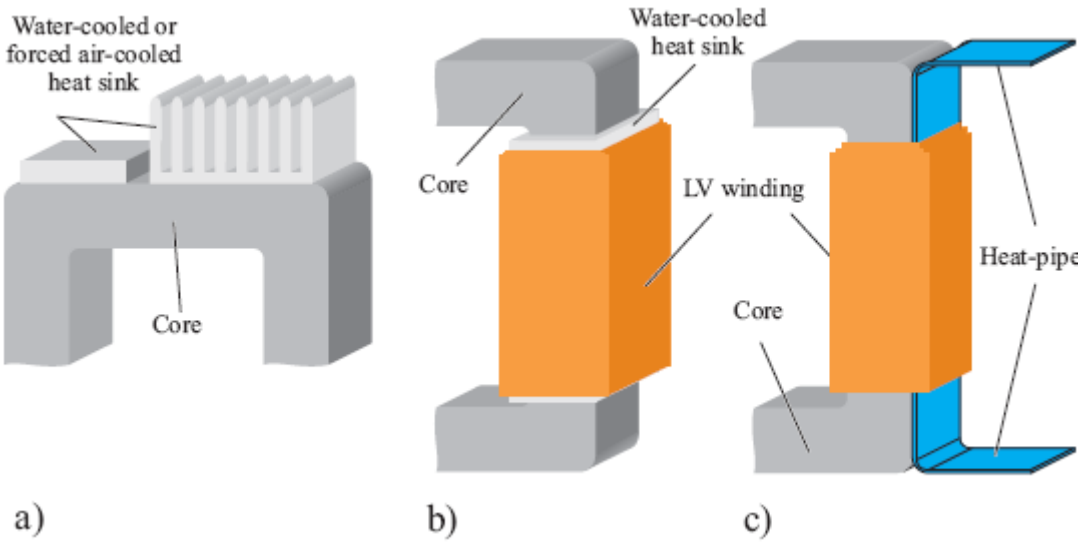



Fig. 2-21 Core and LV winding cooling concepts: a) Water or forced-air cooled heat sink attached to the top and bottom C-cut cores; b) Water cooled heat sink surrounding each leg of the core. c) Heat pipe surrounded by LV winding [2-103]

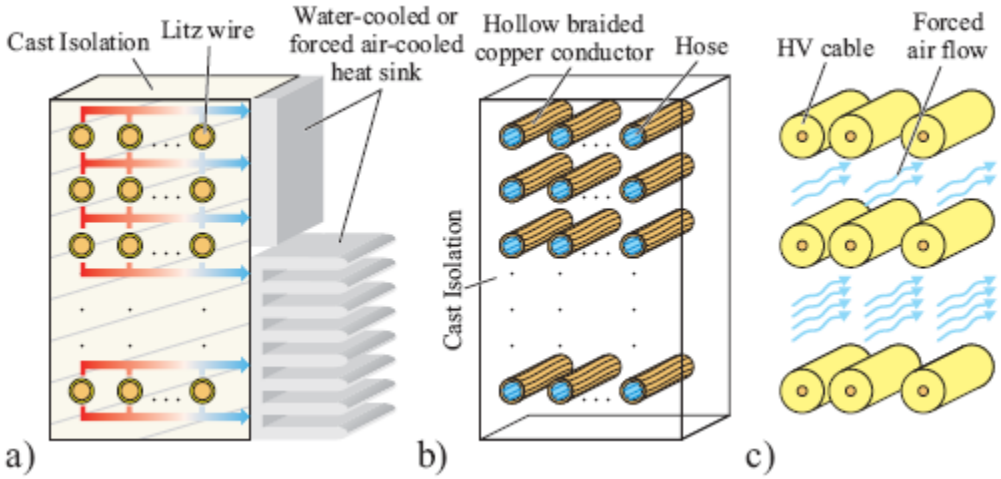



Fig. 2-22 HV cooling concepts: a) Water or forced-air cooled heat sink attached to the external face of the cast insulation; b) Braided copper hollow conductor with an internal plastic hose carrying water (self-cooled cable); c) Forced air cooled HV cable [2-103]

The voltage multiplier cooling generally is the same as HV transformer cooling. The voltage multiplier can be cooled with insulation oil inside the HV tank by passive cooling. Or a high voltage multiplier can be cooled with heat extraction active cooling such as special circuit boards, and additional fan, air-cooled or liquid-cooled heat sink.

The switching frequency increase can help to reduce the HV transformer and HV rectifier size for a HV pulse converter. At higher switching frequency, not only can the size of HV transformer core be reduced, but also the size of the capacitance of the HV rectifier can be decreased. However, more power loss will be generated from core loss, winding AC loss, high frequency dielectric loss of HV transformer and the HV rectifier inside the HV tank. Better magnetic core materials, and low AC resistance winding technology, ultra-fast diode rectifiers and better dielectric HV capacitors are required to mitigate the power loss at a higher switching

frequency. So, a higher switching frequency can help to improve the power density of a HV tank and more effective cooling solution is required to remove the heat from the HV tank.

## 2. 7 Summary

State-of-the-art HV pulse converter technologies are reviewed in this chapter. Firstly, HV pulse converter architectures are classified as single or multiple power building blocks. Secondly, the topologies of HV pulse converters are discussed. It is concluded that LCC topology is the most suitable topology to integrate large stray parameters to a HV transformer. Thirdly, the technologies for HV pulse converter key power building blocks such as inverters, HV transformers and HV rectification are presented. Finally, packaging techniques are reviewed and divided into component packaging level and assembly packaging level. State-of-the-art packaging techniques are concluded to guide the packaging design of HV pulse converter.

*a) HV pulse converter architectures*

State-of-the-art studies of HV pulse converters focus on one type of architecture for specific applications. HV pulse converter architectures with multiplier power building blocks provide the opportunity for power density, and further improvement for efficiency. A clearer picture to classify the HV pulse converter architecture is not provided. Furthermore, the evaluation of different HV pulse converter architectures, and guidelines for selecting the best HV pulse converter architectures for different output voltage and power rating are not available.

b) *Topology, modelling and control*

State-of-the-art research on topology, modelling and control of a HV pulse converter covers nearly every aspect of application. Frequency control strategy and combined frequency & PWM control strategy have been investigated. However, unified equivalent steady state circuit model for different architectures is not addressed.

c) *HV transformer*

HV transformer design consideration, characterization of parasitic components and electrical and thermal behaviour have been studied in the literature. Detailed loss analysis on high frequency HV transformers are given. However, state-of-the-art analysis of a loss model does not take dielectric loss into consideration, which is proven to be a significant part of the total loss at high switching frequency. This research does not cover characterization and packaging structures of a high frequency HV transformer for the modular HV pulse converter architecture.

d) *HV rectification*

HV multiplier steady state and dynamic characteristics, diode equivalent parasitic capacitance analysis, and optimal design solution of a HV multiplier with minimum total capacitance are reported. However, the high frequency reverse recovery process and HV pulse speed influence factors for the modular HV pulse converter architecture have not yet been addressed for high frequency modular HV pulse converter architecture.

*e) Packaging*

Two types of packaging technologies for a HV pulse converter are summarized. The novel component and system level packaging, as well as high power density integration technologies need further investigation for HV pulse converter performance improvement.

The inverter which is outside the HV tank of the HV pulse converter is not in the research scope of this thesis. There is no big technical reason or bottleneck for an inverter to achieve high frequency HV pulse converter system performance improvements. The high frequency capability with low parasic packaging inductance, high-speed gate driver circuits of the power semiconductor devices such as silicon IGBT or MOSFET have been widely studied in different industrial applications such as high frequency uninterruptible power supply (UPS), induction heating, etc. The new emerging SiC MOSFET discrete device or power module with low parasitic packaging inductance will help to further reduce the conduction and switching power loss. As an alternative to multi-level inverter configuration, SiC MOSFET with higher voltage rating such as 1.7kV, 3.3kV, and 4.5kV can operate at high frequency for a two level medium voltage inverter with higher DC input voltage which can help to reduce the turns ratio of a HV transformer, or stage number of a voltage multiplier.

Higher efficiency, higher power density and better static and dynamic performance are requirements for HV pulse converters from industrial applications. Below are the critical items which will be investigated in following chapters to further develop the HV pulse converter technologies:

a) Systematic HV pulse converter architectures derivation, a classification and evaluation method to provide guidance for architecture selections for specific applications. Chapter 3 will address the analysis and evaluation of HV pulse converter architectures.
b) The effect of modularization, increasing switching frequency, packaging and insulation structure for HV pulse converter. Chapter 4 will discuss the modularization, increasing switching frequency, packaging and insulation structure analysis for HV transformer.
c) The key influence factors of pulse rise and decay time and diode reverse recovery mitigation solution for a multi-stage voltage multiplier circuit. Chapter 5 will provide the HV pulse rise and decay time influence factors and propose a solution to solve the diode reverse recovery.
d) Genetic steady state circuit model to provide design guidance for a HV pulse converter with different architectures and a comprehensive design procedure for LCC resonant converter based HV pulse converter architectures. Chapter 6 will derive the unified circuit model and provide a detailed design methodology for modular HV pulse converter architectures.

## 2.8 References

[2-1] Y. Du, J. Wang, G. Wang, and A. Q. Huang, “Modeling of the high frequency rectifier with 10-kV SiC JBS diode in high-voltage series resonant type DC-DC converters,” IEEE Tran. Power Electron., vol.29, no.8, pp. 4288-4300, Aug. 2014.

[2-2] J. Liu, L. Sheng, J. Shi, Z. Zhang, and X. He, “Design of High Voltage, High Power and High Frequency Transformer in LCC Resonant Converter, pp. 1034-1038.

[2-3] J. Liu, L. Sheng, J. Shi, Z. Zhang, and X. He, “LCC resonant converter operating under discontinuous resonant current mode in high voltage high power and high frequency applications,” in Proc. Appl. Power Electron. Conf. Expo., 2009, pp. 1482-1486.

[2-4] J. Martin-Ramos, P. J. Villegas, A. M. Pernía, J. Díaz, and J. A. Martinez, “Optimal control of a high voltage power supply based on the PRC-LCC topology with a capacitor as output filter,” IEEE Transaction Ind. Appl., vol.49, no. 5, pp. 2323-2329, Sep./Oct. 2013.

[2-5] J. Martin-Ramos, A. M. Pernía, J. Diaz, F. Nuño, and J. A. Martínez, “Power supply for a high voltage application,” IEEE Transaction Power Electron., vol. 23, no. 4, pp. 1608-1619, Jul. 2008.

[2-6] T. B. Soeiro, J. M¨uhlethaler, J. Linn´er, P. Ranstad, and J. W. Kolar, “Automated design of a high-power high-frequency LCC resonant converter for electrostatic precipitators,” IEEE Transaction Ind. Electron., vol. 60, no. 11, pp. 4805-4819, Nov. 2013.

[2-7] M. G. Giesselmann, T. T. Vollmer and W. J Carey, “100-kV High Voltage Power Supply with Bipolar Voltage Output and Adaptive Digital Control,” IEEE Transaction Plasma Sci., vol. 42, no. 10, pp. 2913-2918, 2014.

[2-8] L. Zhao, D. Peng, J. D. van Wyk, “Analysis and Design of an LCLC Resonant Converter Suitable for X-ray Generator Power Supply,” in Proc. CPES Annu. Conf., 2000, pp. 360-365.

[2-9] V. García, M. Rico, J. Sebastián, M. Hernando, and J. Uceda, “An optimized DC–DC converter topology for high voltage pulse loads applications,” in Proc. IEEE PESC, 1994, pp. 1413-1421.

[2-10] V. Garcia, M. Rico, J. Sebastian, M. Hernando, and J. Uceda, “Study of an optimized resonant converter for high-voltage applications,” in Proc. Power Electronics Congress, 1994, pp. 114-121.

[2-11] V. García, M. Rico, J. Sebastián, and M. Hernando, “Using the hybrid series parallel resonant converter with capacitive output filter and PWM phase-shifted control for high-voltage applications,” in Proc. IEEE IECON, 1994, pp. 1659-1664.

[2-12] J. Biela and J. W. Kolar, “Using transformer parasitics for resonant converters—A review of the calculation of the stray capacitance of transformers,” in Proc. IEEE 40th IAS Annu. Meeting, 2005, pp. 1868-1875.

[2-13] M. Giesselmann, T. Vollmer, M. Lara, J. Mayes, “Compact HV-Capacitor Charger,” in Proc. IEEE International Power Modulator Conference, 2008, pp. 238-241.

[2-14] S. N. Vukosavić, L. S. Perić, and S. D. Sušić, “A novel power converter topology for electrostatic precipitators,” IEEE Transaction Power Electron., vol. 31, no. 1, pp. 152-164, Jan. 2016.

[2-15] C. Loef, R. W. Doncker and B. Ackermann, “On high frequency high voltage generators with planar transformers”, in Proc. APEC, 2014, pp. 1936-1940.

[2-16] D. G. Bandeira, T. B. Lazzarin, I. Barbi, “T-Type Parallel Resonant DC-DC Converter for High Voltage Application,” in Proc. IEEE International Conference on Industry Applications (INDUSCON), 2016, pp. 1-8.

[2-17] F. S. Cavalcante and J. W. Kolar, “Design of a 5kW high output voltage series-parallel resonant DC-DC converter,” in Proc. IEEE Power Electron. Spec. Conf., 2003, vol. 4, pp. 1807-1814.

[2-18] S. S. Lee; S. Iqbal; M. K. M. Jamil, “A digitally tuned resonant capacitance control with narrow range frequency modulation for ZCS high voltage X-ray power supply,” in Proc. International Conference on Electrical, Control and Computer Engineering 2011 (InECCE), pp. 113-118.

[2-19] T. Soeiro, J. Biela, J. Muhlethaler, J. Linner, P. Ranstad, and J. W. Kolar, “Optimal design of resonant converter for electrostatic precipitators,” in Proc. IPEC, Sapporo, Japan, Jun. 2010, pp. 2294-2301.

[2-20] A. Amir, S. Taib, S. Iqbal, “A fixed frequency continuous conduction LCCL series resonant inverter fed high voltage DC-DC converter,” in Proc. 2013 IEEE International Conference on Circuits and Systems (ICCAS), pp. 75-80.

[2-21] N. Shafiei, M. Pahlevaninezhad, H. Farzanehfard, A. Bakhshai, and P. Jain, “Analysis of a fifth-order resonant converter for high-voltage DC power supplies,” IEEE Transaction Power Electron., vol. 28, no. 1, pp. 85-100, Jan. 2013.

[2-22] J. Martin-Ramos, J. Diaz, A. M. Pernía, J. M. Lopera, and F. Nuño, “Dynamic and steady state models for the PRC-LCC topology with a capacitor as output filter,” IEEE Transaction Ind. Electron., vol. 54, no. 4, pp. 2262-2275, Aug. 2007.

[2-23] J. Martin-Ramos, J. Diaz, F. Nuño, P. J. Villegas, A. López-Hernández, J. F. Gutiérrez-Delgado, “A Polynomial Model to Calculate Stead0y-State Set Point in the PRC-LCC Topology With a Capacitor as Output Filter,” IEEE Transaction Industry Applications, vol. 51, no. 3, pp. 2520-2527, 2015.

[2-24] J. W. Gong, H. J. Ryoo, S. H. Ahn, S. R. Jang, “Development of 50-kV 100-kW Three-Phase Resonant Converter for 95-GHz Gyrotron,” IEEE Transaction on Plasma Science, vol. 42, no.11, 2014, pp. 3623-3632.

[2-25] W. C. Hsu; J.F.Chen, Y.P. Hsieh,Y.M. Wu, “Design and steady-state analysis of parallel resonant DC–DC converter for high-voltage power generator,” IEEE Transaction on Power Electronics, 2017, vol.32, no. 2, pp. 957-966.

[2-26] S. Mao, J. Popovic, J. A. Ferreira, “ An investigation into high frequency high voltage planar transformer for high voltage generator applications,” in Proc. IEEE 2016 9th International Conference on Integrated Power Electronics Systems(CIPS), pp. 1-6.

[2-27] J. Sun, X. Ding, M. Nakaoka, and H. Takano, “Series resonant ZCS-PFM DC-DC converter with multistage rectified voltage multiplier and dual-mode PFM control scheme for medical-use high-voltage X-ray power generator,” in Proc. Inst. Elect. Eng., vol. 147, no. 6, pp. 527-534, Nov. 2000.

[2-28] Z. Zhang, Z. Tang, “Pulse frequency modulation LLC series resonant X-ray power supply,” in Proc. IEEE 2011 International Conference on Consumer Electronics, Communications and Networks (CECNet), 2011, pp. 1532-1535.

[2-29] J. Wang, P. Luerkens, S. W. H. de Haan, and J. A. Ferreira, “Analytical analysis of the equivalent parasitic capacitance of the high-voltage cascade multiplier in medical application of X-ray power generator,” in Proc. IPEMC, Jun. 2012, vol. 1, pp. 463-470.
[2-30] Y. A. Wang, D. M. Xiao, and Y. L. Liu, “Design of a planar power transformer for high voltage, high frequency use,” in Proc. IEEE PES Transmission Distrib. Conf. Expo., Apr. 2010, pp. 1-6.
[2-31] S. Mao, J. Popovic, J. A. Ferreira, “High Voltage Pulse Speed Study for High Voltage DC-DC Power Supply Based on Voltage Multipliers,” in Proc. IEEE 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), pp.1-10.
[2-32] P. Lürkens, P. Guimaraes, P. Godignon, J. Millán, “High Voltage SiC Schottky Diodes in Rectifiers for X-Ray Generators,” Materials Science Forum Vols.717-720, 2012, pp 1245-1248.
[2-33] L. Katzir, D. Shmilovitz, “A High Voltage Split Source Voltage Multiplier with Increased Output Voltage,” in Proc. IEEE APEC, 2015, pp. 3272-3275.
[2-34] M. Rentzsch, F. Gleisberg, H. Guldner, F. Benecke, and C. Ditmanson, “Closed analytical model of a 20kV output voltage, 800W output power series–parallel-resonant converter with Walton Cockcroft multiplier,” in Proc. IEEE PESC, Jun. 2008, pp. 1923-1929
[2-35] L.Katzir, D. Shmilovitz, “A 1-MHz 5-kV Power Supply Applying SiC Diodes and GaN HEMT Cascode MOSFETs in Soft Switching,” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 4, pp. 1474-1482, 2016.
[2-36] L.Katzir, D. Shmilovitz, “Effect of the capacitance distribution on the output impedance of the half-wave Cockcroft-Walton voltage multiplier,” in Proc. IEEE APEC, 2016, pp 3655-3658.
[2-37] S. Iqbal, R. Besar y C. Venkataseshaiah, “A novel control scheme for voltage multiplier based X-ray power supply,” in Proc. Power and Energy Conference, PECON, 2008. pp 1456-1460.
[2-38] H.J. Ryoo, S.R. Jang, Y.S. Jin, J.S. Kim, Y.B. Kim, S.H. Ahn, J.W. Gong, B.H. Lee and D.H. Kim, “Design of high voltage capacitor charger with improved efficiency, power density and reliability,” IEEE Transaction on Dielectrics and Electrical Insulation, Vol. 20, No. 4, pp. 1076-1084, 2013.
[2-39] M. Hu, N. Froehlekw, W. Peters, and J. Boecker, “Multi-objective optimization of LCC resonant converter applied in VLF HV pulse converter,” in Proc. IEEE IECON, 2011, pp. 1456-1461.
[2-40] T. Filchev; D. Cook; J. Clare; P. Wheeler, “High voltage, high frequency transformer-switching converter integration,” in Proc. IET Conference on High Power RF Technologies, 2009, pp. 1-4.
[2-41] S. S. Lee, S. Iqbal, and M. Kamarol, “Control of ZCS-SR inverter-fed voltage multiplier-based high-voltage DC-DC converter by digitally tuning tank capacitance and slightly varying pulse frequency,” IEEE Transaction Power Electron., vol. 27, no. 3, pp. 1076-1083, Mar. 2012.

[2-42] G. L. Piazza, R. L. Alves, C. H. I. Font; I. Barbi, “Resonant circuit model and design for a high frequency high voltage switched-mode power supply,” in Proc. Brazilian Power Electronics Conference, 2009, pp. 326-331.

[2-43] W. Luo, X. Wang, “Development of Electric Control High Power Medical-Use X-ray Generator,” in Proc. International Conference on Information Engineering and Computer Science , 2009, pp. 1-5.

[2-44] S. Gavin et al., “A digitally controlled 125 kVdc, 30 kW power supply with an LCC resonant converter working at variable DC-link voltage: Full scale prototype test results,” in Proc.7th IET Int.Conf. PEMD, Apr. 2014, pp. 1-6.

[2-45] T. Filchev, D. Cook, P. Wheeler, and J. Clare, “Investigation of high voltage, high frequency transformers/voltage multipliers for industrial applications,” in Proc. IET 4th Int. Conf. Power Electron., Mach. Drives, 2008, pp. 209-213.

[2-46] S. S. Liang and Y. Y. Tzou, “DSP control of a resonant switching high voltage power supply for X-ray,” in Proc. IEEE Power Electron. and drive systems Conf., vol.2, Oct. 2001, pp. 522-526.

[2-47] S. H. Ahn, H. J. Ryoo, J. W. Gong, and S. R. Jang, “Robust design of a solid-state pulsed power modulator based on modular stacking structure,” IEEE Transaction Power Electron., vol. 30, no. 5, pp. 2570–2577, May 2015.

[2-48] J. Sun, H. Konishi, Y. Ogino, E. Chu, and M. Nakaoka, “Series resonant high-voltage PFM DC-DC converter with voltage multiplier based a two-step frequency switching control for medical-use X ray power generator,” in Proc. IEEE Power Electronics and Motion Control Conf., vol.2, 2000, pp. 596-601.

[2-49] J. Sun, H. Konishi, Y. Ogino, and M. Nakaoka, “Series resonant high-voltage ZCS-PFM DC-DC converter for medical power electronics,” in Proc. IEEE PESC, vol.3, Jun. 2000, pp. 1247-1252.

[2-50] J. A. Martín-Ramos; Ó. Pardo-Vaquero; P. J. Villegas; J. A. Martínez; A. M. Pernía, “Multilevel PRC-LCC resonant converter for X-ray generation,” Electronics Letters, Vol. 51, no.15, 2015, pp. 1189-1191.

[2-51] Y. Qiu, B. Lu, B. Yang, D. Fu, and F. C. Lee, “A high-frequency high-efficiency three-level LCC converter for high-voltage charging applications,” in Proc. IEEE PESC, 2004, vol. 6, pp. 4100-4106.

[2-52] H. Sheng et al., “Design and implementation of a high power density three-level parallel resonant converter for capacitor charging pulsed power supply,” IEEE Transaction Plasma Sci., vol. 39, no. 4, pp. 1131-1140, Apr. 2011.

[2-53] F. Dianbo, F. C. Lee, Q. Yang, and F. Wang, “A novel high-power-density three-level LCC resonant converter with constant-power-factor-control for charging applications,” IEEE Transaction Power Electron., vol. 23, no. 5, pp. 2411-2420, Sep. 2008.

[2-54] J. Martin-Ramos, Ó. P. Vaquero, J. D. González, M. A. J. Prieto, J. A. M. Esteban, A. M. Pernía, “Modeling a multilevel converter for radiography and fluoroscopy,” in Proc. 2016 EPE'16 ECCE Europe, pp. 1-10.

[2-55] A. M. Pernía, O.P. Vaquero, P. J. Villegas; F. Nuño; H. A. Mayor; J. A. Martín-Ramos, “Multilevel converter for X-ray generators,” in Proc. IEEE IECON 2016, pp. 1376-1381.

[2-56] T.F. Wu and J. C. Hung, “A PDM controlled series resonant multi-level converter applied for x-ray generators,” in Proc. IEEE PESC, 1999, pp. 1177-1182.

[2-57] S. Iqbal, “A three-phase symmetrical multistage voltage multiplier,” IEEE Transaction Power Electron., vol. 3, no. 2, pp. 30-33, Mar. 2005.
[2-58] A. Pokryvailo, C. Carp, and C. Scapellati, “A high-power high voltage power supply for long-pulse applications,” IEEE Transaction Plasma Sci., vol. 38, no. 10, pp. 2604-2610, Oct. 2010.
[2-59] M. Jaritz, T. Rogg, and J. Biela, “Control of a modular series parallel resonant converter system for a solid state 2.88mw/115-kV long pulse modulator,” in Proc. 17th Eur. Conf. Power Electron. Appl, Sep. 2015, pp. 1-11.
[2-60] M. Jaritz, S. Blume. D. Leuenberger, J. Biela, “Experimental Validation of a Series Parallel Resonant Converter Model for a Solid State 115-kV Long Pulse Modulator,” IEEE Transaction on Plasma Science,2015, vol.43, no.10, pp. 3392-3398.
[2-61] M. Giesselmann, T, Vollmer; L. Altgilbers, “Modular, Compact HV-Capacitor Charger,” in Proc. IEEE International Power Modulator Conference, 2008, pp. 409-412.
[2-62] M. Jaritz and J. Biela, “Optimal design of a modular series parallel resonant converter for a solid state 2.88 MW/115-kV long pulse modulator,” IEEE Transaction Plasma Sci., vol. 42, no. 10, pp. 3014-3022, Oct. 2014.
[2-63] S.H. Park; L. Katzir; D. Shmilovitz, “Reduction of voltage drop and ripple in voltage multipliers,” in Proc. 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), pp. 1-7.
[2-64] S Iqbal, R Besal, C. Venkataseshaiah, “Single-Three-phase Symmetrical Bipolar Voltage Multipliers for X-ray Power Supply,” in proc. Second International Conference on Electrical Engineering, 2008, pp. 30-33.
[2-65] S. Iqbal, G. K. Singh and R. Besar, “A Dual-Mode Input Voltage Modulation control scheme for Voltage Multiplier Based X-ray Power Supply,” IEEE Transaction on Power Electronics vol. 23, no. 2, pp. 1003-1008, March 2008.
[2-66] I. A. Krichtafovitch, “Modular high-voltage power supplies design,” in Proc. Thirty-Second Intersociety Energy Conversion Engineering Conference(IECEC), 1997, vol.1 pp. 375-380.
[2-67] A. Pokryvailo, C. Carp, C. Scapellati, “A 100 kW high voltage power supply for dual energy computer tomography applications,” IEEE Transaction on Dielectrics and Electrical Insulation, vol.22, no.4, 2015, pp. 1945-1953.
[2-68] L. M. Redondo, J. F. Silva, E. Margato, “Analysis of a modular generator for high-voltage, high-frequency pulsed applications,” Review of Scientific Instruments, 2007, vol.78, pp.1-7
[2-69] J. Biebach, P. Ehrhart, A. Muller, G. Reiner, and W. Weck, “Compact modular power supplies for superconducting inductive storage and for capacitor charging,” IEEE Transaction Magn., vol. 37, no. 1, pp. 353-357, Jan. 2001.
[2-70] S. R. Jang, J.H.,Seo , H. J. Ryoo, “Development of 50-kV 100-kW Three-Phase Resonant Converter for 95-GHz Gyrotron,” IEEE Transaction Industrial electronics, vol.63, no.11, 2016, pp. 6674-6683.
[2-71] A. K. Jain, C.P. Henze, C.B. Henze and K. Conroy, “Development of a 350kW,10kV pulse power converter for capacitor charging,” in Proc. IEEE APEC, 2007, pp. 1164-1170.

[2-72] C. Martins, M. Collins, “Development of a long pulse high power Klystron modulator for the ESS based on the stack multi-level topology,” in Proc. IPAC 2016, pp.3600-3602.
[2-73] B. Jacobson, M. Bamett, R. DiPemi, J, McGinty, “Planar integrated magnetics assembly for high voltage converters,” in Proc. IEEE APEC, 2000, pp. 622-632.
[2-74] L. Katzir and D. Shmilovitz, “A matrix-like topology for high-voltage generation,” IEEE Transaction Plasma Sci., vol. 43, no. 10, pp. 3681-3687, Oct. 2015.
[2-75] L. Katzir and D. Shmilovitz, “A split-source multisection high-voltage power supply for X-ray,” IEEE J. Emerg. Sel. Topics Power Electron., vol. 4, no. 2, pp. 373-381, Jun. 2016.
[2-76] S.-R. Jang, H.-J. Ryoo, J. Kim, and G. H. Rim, “Development and optimization of high-voltage power supply system for industrial magnetron,” IEEE Transaction Ind. Electron., vol. 59, no. 3, pp. 1453-1460, Mar. 2012
[2-77] D.-W. Yoo, J.-W. Baek, and H.-S. Son, “Full digital 150 kV–1 A ZVS converter for X-ray power applications,” IEEE Transaction Plasma Science, vol.31, no. 3, pp. 1313-1316, 2003.
[2-78] S. Iqbal, R.Besar, C. Venkataseshiah, “A Novel ZCS-SR Voltage Multiplier based High-Voltage DC Power Supply,” in Proc. IEEE International Power and Energy Conference, 2008, pp. 1451-1455.
[2-79] S. S. Lee; S. Iqbal; M. K. M. Jamil, “ A novel ZCS-SR voltage multiplier based high-voltage DC power supply,” in Proc. IEEE International Conference on Circuits and Systems (ICCAS), 2012, pp. 1-5.
[2-80] S. H. Ahn, H. J. Ryoo, J. W. Gong, and S. R. Jang, “Design and test of a 35-kJ/s high-voltage capacitor charger based on a delta-connected three phase resonant converter,” IEEE Transaction Power Electron., vol. 29, no. 8, pp. 4039-4048, Aug. 2014.
[2-81] Y. M. Seo, M. S. Byun; S.C. Hong, “Hybrid type X-ray generator for fluoroscopy X-ray system available in low-capacity AC power source,” in Proc. IEEE ICPE-ECCE Asia Conf., 2015, pp. 2938-2943.
[2-82] S. D. Johnson, A. F. Witulsky, and R. W. Erickson, “Comparison of resonant topologies in high voltage DC applications,” IEEE Transaction Aerosp. Electron. Syst., vol. 24, no. 3, pp. 263-274, May 1988.
[2-83] J. Wang, Modeling of parasitic elements in high voltage multiplier modules, PhD Thesis, Delft University of Technology, Delft, The Netherlands, Dec. 2014.
[2-84] T. Soeiro, “High efficiency electrostatic precipitator systems with low effects on the mains,” PhD thesis, Swiss Federal Institute of Technology in Zurich, Switzerland, 2012.
[2-85] G. Ivensky, A. Kats, and S. Ben-Yaakov, “An RC load model of parallel and series parallel DC–DC converters with capacitive output filter,” IEEE Transaction Power Electron., vol. 14, no. 3, pp. 515-521, May 1999.
[2-86] I. Josifovic, The Power Sandwich: A Three-Dimensional Power Electronics Assembly Technology, PhD Thesis, Delft University of Technology, Delft, The Netherlands, Dec. 2014.
[2-87] L. Dalessandro, F. S. Cavalcante, and J. W. Kolar, “Self-capacitance of high-voltage transformers,” IEEE Transaction Power Electron., vol. 22, no. 5, pp. 2081-2092, Sep. 2007.

[2-88] F. C. Lee and Q. Li, “High frequency integrated point-of-load converters: Overview,” IEEE Transaction Power Electron., vol. 28, no. 9, pp. 4127-4236, Sep. 2013.
[2-89] M. Nagel, T. Leibfried, “Investigation on the high frequency, high voltage insulation properties of mineral transformer-oil”, in Proc. 2006 Annual Report IEEE Conference on Electrical Insulation and Dielectric Phenomena, pp. 226-228, 2006.
[2-90] K. Elanseralathan, J.M. Thomas and G. R. Nagabhushana, “Breakdown of Solid Materials Under High Frequency High Voltage Stress”, in Proc. IEEE 6th Intern. Conf. Properties & Applications of Dielectric Materials, pp. 999-1001, 2000.
[2-91] M. G. Giesselmann, A. Bilbao, “Digital control of a rapid capacitor charger with sensor-less voltage feedback,” IEEE Transaction on Dielectrics and Electrical Insulation, 2015, vol. 22, no.4, pp. 1930-1936.
[2-92] G. Ortiz, J. Biela, and J. W. Kolar, “Optimized design of medium frequency transformers with high isolation requirements,” in Proc. IEEE Ind. Electron. Soc., 2010, pp. 631-638.
[2-93] S. Blume, M. Jaritz, J.Biela, “Design and Optimization Procedure for High-Voltage Pulse Power Transformers,” IEEE Transaction Plasma Science, vol. 43, no. 10, pp. 3385-3391, 2015.
[2-94] I. C. Kobougias, E. C. Tatakis, “Optimal design of a half-wave Cockcroft–Walton voltage multiplier with minimum total capacitance,” IEEE Transaction Power Electron., vol. 25, no. 9, pp. 2460-2468, Sep. 2010.
[2-95] J. S. Brugler, “Theoretical performance of voltage multiplier circuits,” IEEE J. Solid-State Circuits, vol. 6, no. 3, pp. 132-135, Jun. 1971.
[2-96] G. R. Blackwell, The electronic packaging handbook, Boca Raton CRC Press 2000.
[2-97] J. Popovic, Improving packaging and increasing the level of integration in power electronics, PhD Thesis, Delft University of Technology, Delft, The Netherlands, Dec. 2005.
[2-98] U. Uhmeyer, “Cross Transformer Technology(CTT) High Voltage Power Supplies,” in Proc. PESP 2008, pp. 1-31.
[2-99] I. Josifović, The Power Sandwich: A Three-Dimensional Power Electronics Assembly Technology, PhD Thesis, Delft University of Technology, Delft, The Netherlands, Dec. 2014.
[2-100] E. D. Jong, Three-dimensional integration of power electronic converters on printed circuit board, PhD Thesis, Delft University of Technology, Delft, The Netherlands, Dec. 2007.
[2-101] J. Biela, J. W. Kolar, “Cooling concepts for high power density magnetic devices,” in Proc. PCC, Nagoya, Japan, 2007, pp. 1-8.
[2-102] M. Pavlovsky, S. W. H. de Haan, and J. A. Ferreira, “Design for better thermal management in high-power high-frequency transformers,” in Proc. Ind. Appl. Conf., 2005, pp. 2615-2621.
[2-103] Ortiz, G., Biela, J., Kolar, J.W.,” Optimized design of medium frequency transformers with high isolation requirements”, IEEE Industrial Electronics Society Annual Conference, 2010, pp. 631-638.

# Chapter 3

# HV pulse converter architectures evaluation and comparison

This chapter will introduce the methodology to derive, classify and evaluate the HV pulse converter architectures based on the modularization level of key power building blocks. The performance of HV architectures is compared to identify the optimal architecture candidate for varying output voltage and power levels. Finally, the recommendations of HV pulse converter architectures selections are given.

## 3.1 Introduction

There are various architectures used for HV pulse converter technologies with different output voltages and output power ratings. However, a comprehensive overview of various architecture possibilities has not yet been made. There is lack of a clear methodology to evaluate the performance for HV architectures and provide the guidelines for selecting the best HV architectures to achieve good performance in a multidimensional criteria space (high power density, high efficiency and good HV pulse quality, to name a few).

From the typical HV pulse converter circuit diagram shown in Fig. 3-1, 3 key power building blocks can be identified: inverter, HV transformer and HV rectifier. The resonant tank includes a series resonant inductor, a series resonant capacitor and a parallel resonant capacitor for LCC resonant topology illustrated in Fig. 3-2. The parasitic components of a HV transformer such as a leakage inductor and winding parasitic capacitance are used as a series resonant inductor, and parallel resonant capacitor, or a part of the resonator. The series resonant capacitor and series resonant inductor are typically packaged together with the inverter in a low voltage enclosure. So, the resonant tank is not identified as a separated power building block. The HV transformer and HV rectifier are usually packaged together in a HV insulated enclosure which is called a HV tank.

As described in Chapter 2, HV pulse converter architectures can be divided into two types according to whether the power building blocks of the HV pulse converter main circuit are in single or multiple configurations: HV architectures with single power building block sub-component or HV architectures with multiple power building block power building blocks. Furthermore, the HV architectures can be further classified according to the level of modularity (or “distributedness”) of the key power building blocks (inverter, transformer, rectifier) to disclose the characteristics of different architectures. The basic power building block diagram with a general function for HV pulse converter topology is provided in Fig. 3-3.

In this chapter, the systematic method to derive HV architectures is proposed to provide an overview and classification of existing architectures and explore possible new ones according to the level of modularity of key power building blocks. Furthermore, the performance

evaluation of HV architectures are performed to identify and select most promising architectures.

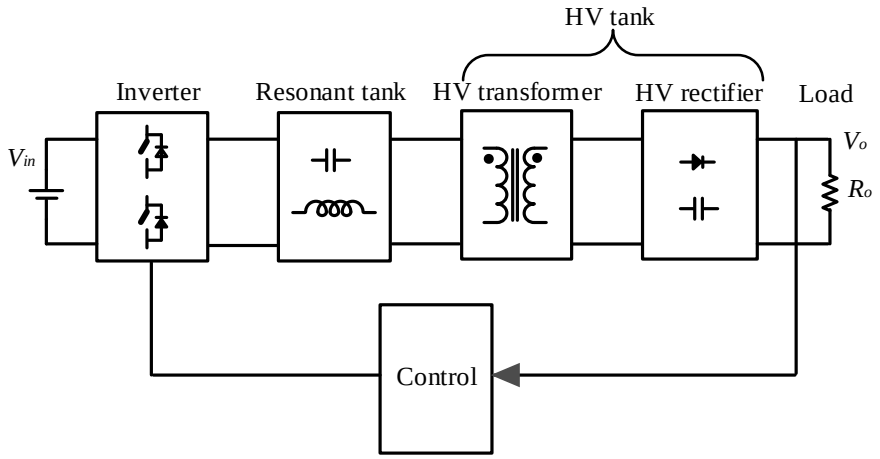



Fig. 3-1 HV pulse converter circuit diagram

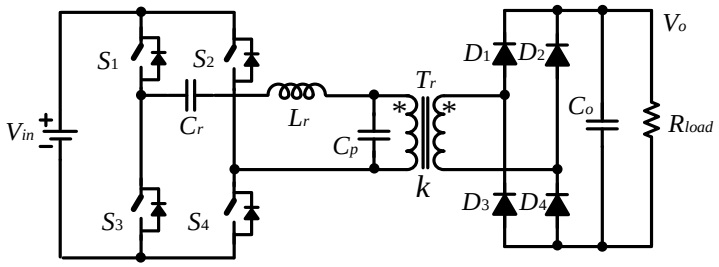
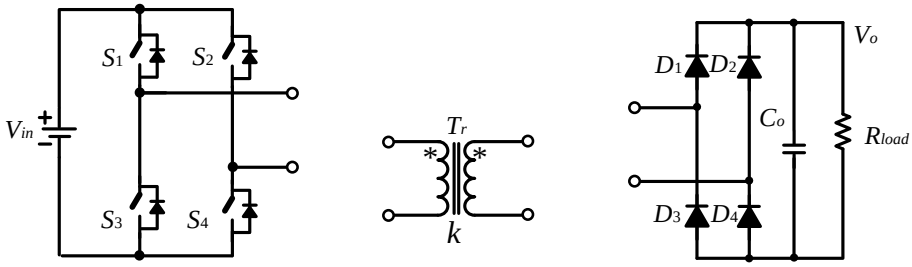



Fig. 3-2 LCC topologies for the HV pulse converter circuit




(a) Inverter (b) HV transformer (c) HV rectifier

Fig. 3-3 Basic power building block diagram for HV pulse converter architecture

## 3.2 HV pulse converter architectures derivation and classifications

### 3.2.1 HV pulse converter architecture derivation methodology

The main benefits of the distributed power building blocks of the HV pulse converter system are lower electrical and insulation stress on the power building blocks and scalable design for high power and high voltage rating. There are different HV architectures according to the level of modularity of the key power building blocks (inverter, transformer, rectification) as shown in Table 3-1.

The definition of modularity level for the key HV pulse converter power building blocks (inverter, HV transformer, HV rectification) is listed below:

a) Inverter
   Two level or single phase full bridge or half bridge inverter is defined as a single type inverter power building block. The multi-level inverter or multi-phase inverter can be regarded as a multiple type inverter configuration.

b) HV transformer
   Single HV transformer is defined as a single type HV transformer power building block. The combination of several HV transformer units in a HV pulse converter circuit will be treated as multiple transformer configurations.

c) HV rectifier
   Rectifier/doubler is considered as a single type rectifier circuit, and multi-stage voltage multiplier is regarded as multiple rectifier circuit.

Based on the above derivation methodology, there are eight different HV architectures according to whether the key power building blocks are single or multiple type of power building blocks as shown in Table 3-1.

Table 3-1 HV pulse converter architectures derivation according to the level of modularity of key HV pulse converter power building blocks

| | Inverter | HV transformer | HV rectifier | Key feature |
|---|---|---|---|---|
| Architecture-1 | single | single | single | basic architecture |
| Architecture-2 | single | single | multiple | voltage multiplication |
| Architecture-3 | single | multiple | single | multiple transformer |
| Architecture-4 | single | multiple | multiple | multiple transformer, voltage multiplication |
| Architecture-5 | multiple | single | single | multiple inverter |
| Architecture-6 | multiple | multiple | single | multiple inverter & transformer |
| Architecture-7 | multiple | single | multiple | multiple inverter & voltage multiplication |
| Architecture-8 | multiple | multiple | multiple | multiple inverter & transformer, voltage multiplication |

### 3.2.2 HV pulse converter architectures classifications

In this section, each HV pulse converter architecture will be introduced in terms of its main characteristics and its representation in literature will be given.

a) Architecture-1: Single inverter + single transformer + single rectifier [3-1]-[3-19].

   HV Architecture-1 shown in Fig. 3-4 is composed of a single inverter, a single HV transformer and a single rectifier. Architecture-1 relies on only a single HV transformer to

achieve the voltage step-up. The performance of output HV pulse speed and voltage ripple is good with diode rectifications. However, this architecture cannot offer the scalability since the power inverter, HV transformer and rectifier are all centralized. The efficiency and power density improvement is a challenge due to high insulation stress and large parasitics for the HV transformer when the switching frequency increases. When the output rating voltage is high, the insulation stress for the HV transformer becomes very large, the high frequency dielectric loss increases and leads to a very complex insulation, large size and low efficiency.

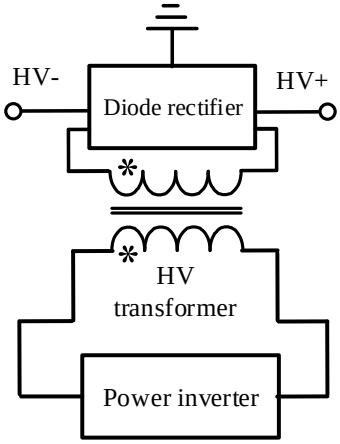



Fig. 3-4 Circuit diagram for Architecture-1

b) Architecture-2: Single inverter + single transformer + multiple rectifier [3-20]-[3-42].

HV architecture-2 in Fig. 3-5 is composed of a single power inverter, a single HV transformer and a voltage multiplier. Compared with HV architecture-1, the Cockcroft-Walton (CW) voltage multiplier is introduced for HV architecture-2 to achieve the required high output voltage. The insulation stress for a HV transformer is largely reduced compared to Architecture-1. This makes the HV transformer insulation design and assembly straightforward.

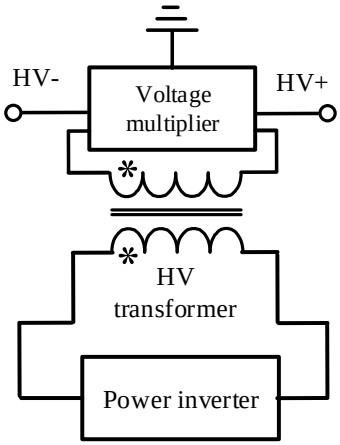



Fig. 3-5 Circuit diagram for Architecture-2

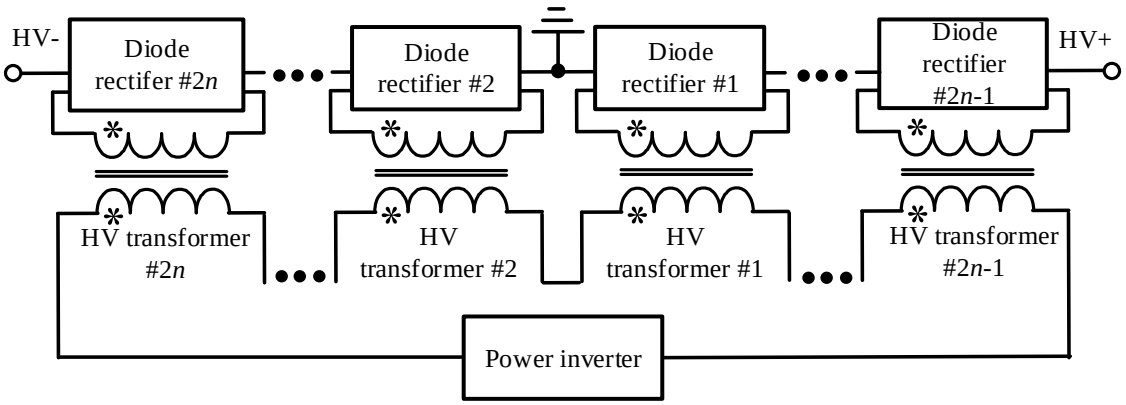
The performance of Architecture-2 can achieve optimal trade-off between the HV transformer turns ratio and the stage number of the voltage multiplier. The HV pulse response times and voltage drop will be influenced by the number of stages of a voltage

multiplier. Voltage multiplier based HV architectures can be widely used in low power to medium power range with optimal energy density and power efficiency performance. The voltage multiplier with different stage numbers provides the scalability for different output voltage rating applications.

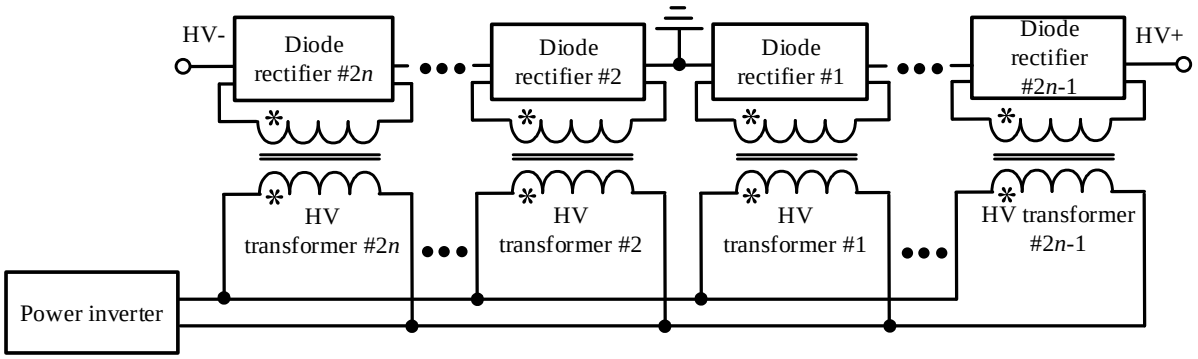
c) Architecture-3: Single inverter + multiple transformers + single rectifier [3-43]-[3-50].

This architecture contains a single power inverter, multiple HV transformers and a single rectifier as depicted in Fig. 3-6. In Architecture-3, the multiple transformers are connected in series through rectifiers to generate high output voltage with reduced insulation stress of each transformer. The connection of the transformer primary side depends on different applications. Series connection is suitable for high input AC voltage and parallel connection is suitable for large current applications.

Compared with Architecture-1, the insulation and power stress for each transformer in Architecture-3 is much lower. Similar to Architecture-1, the output voltage drop of Architecture-3 is low for the rectifier, and suitable for high output current applications. It also provides fast HV pulse and low voltage ripple with diode rectifications for large output current applications with scalability on the numbers of HV transformers. However, HV insulation between distributed HV transformers will a challenge. The size of the HV transformer is primarily dependent on the insulation and packaging. The variance of HV transformer parasitics including magnetizing inductance, leakage inductance, winding capacitance due to the magnetic core characteristics difference and inconsistent manufacture process need to be considered to achieve the voltage and current sharing for multiple HV transformers in Architecture-3.




(a)HV transformer primary side series connection configurations

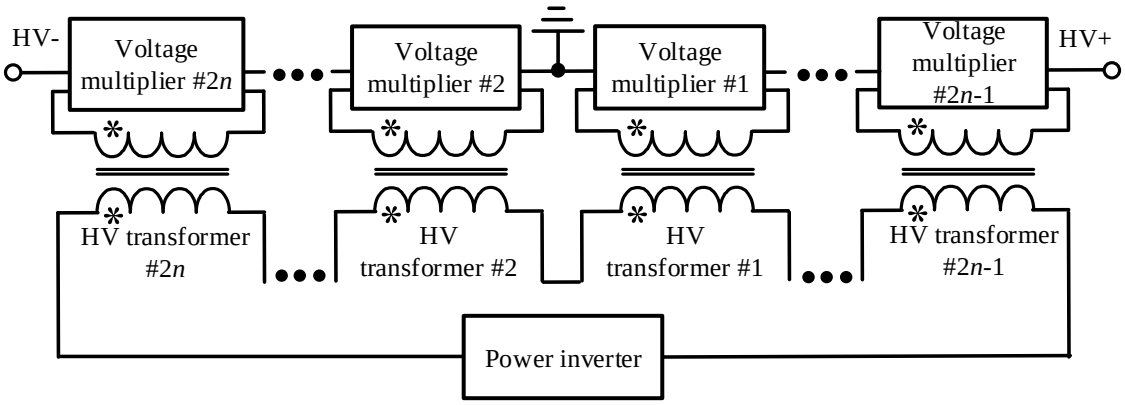



(b) HV transformer primary side parallel connection configurations

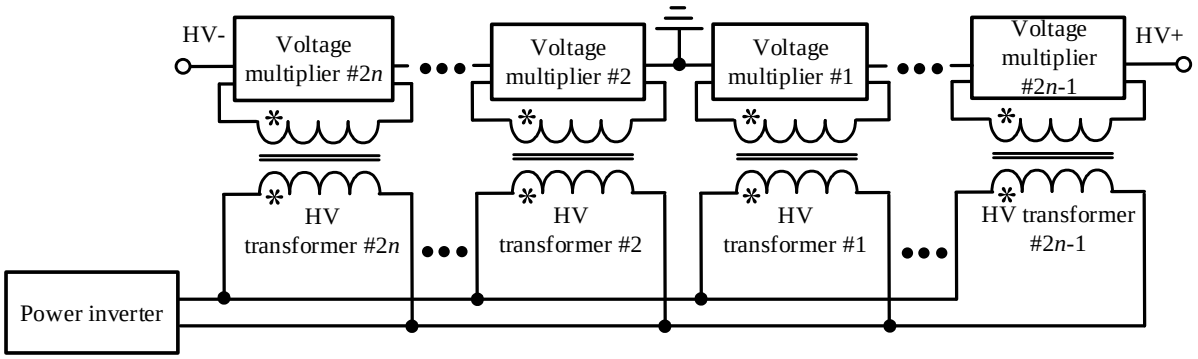
Fig. 3-6 Circuit diagram for Architecture-3

d) Architecture-4: Single inverter + multiple transformers+ multiple rectifiers [3-51]

HV architecture-4 in Fig. 3-7 is composed of a single power inverter, multiple HV transformers and voltage multiplications. The same as Architecture-3, the connection structure of the primary side of the transformer and inverter can be divided into series connection and parallel connection. The modular HV transformers and voltage multipliers are major characteristics for Architecture-4. For HV pulse converter Architecture-4, the insulation stress for the HV transformer can be further reduced compared with Architecture-3. Architecture-4 provides the possibility of optimal design with scalability on the numbers of HV transformers and stage numbers of the voltage multiplier when the output voltage rating is high and the power rating is large. The power density is related to the HV transformer technology, voltage multiplier technology and insulation and packaging for distributed HV transformers and the voltage multiplier. Architecture-4 provides balanced performance to achieve good performance in a multi-dimensional criteria space such as high power density, high efficiency, and good HV pulse quality, to name a few). However, the research on this HV pulse converter architecture is very limited. The advantage and challenges of modularization for the HV transformer, the HV pulse speed influence factor and multiplier diode reverse recovery process in the modular HV pulse converter have not been addressed.




(a)HV transformer primary side series connection configurations




(b) HV transformer primary side parallel connection configurations

Fig. 3-7 Circuit diagram for Architecture-4

e) Architecture-5: Multiple inverters + single transformer + single rectifier [3-52]-[3-59].

Architectures 5-8 are based on multiple power inverters configurations. The split DC energy source is required for multiple power inverters stacked in series. The advantages and disadvantages of these HV pulse converter architectures are similar to HV Architectures 1-4. The multi-level inverter or multi-phase inverter configurations will reduce the voltage stress or current stress for power semiconductor devices in the inverters. Architecture-5 in Fig. 3-8 is composed of multiple power inverters, a single HV transformer and single diode rectification. Compared with Architecture-1, the multi-stage inverter is introduced to connect with the HV transformer and rectifier. This architecture will enable the usage of low voltage semiconductor devices for an inverter, or higher input DC voltage application.

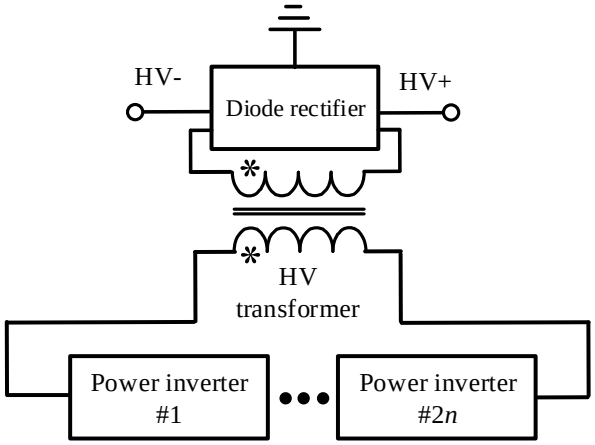



Fig. 3-8 Circuit diagrams for Architecture-5

f) Architecture-6: Multiple inverters + multiple transformers + single rectifier [3-60]-[3-68].

HV Architecture-6 in Fig. 3-9 is composed of multiple power inverters, multiple HV transformers and a single rectifier. This architecture is suitable for a high power, high output current application due to low voltage drop and loss in the rectifier. This structure

provides the flexibility to scale to higher output voltage rating. The configuration of multiple inverters provides the possibility for using low voltage semiconductor devices for inverter, or higher input DC voltage application.

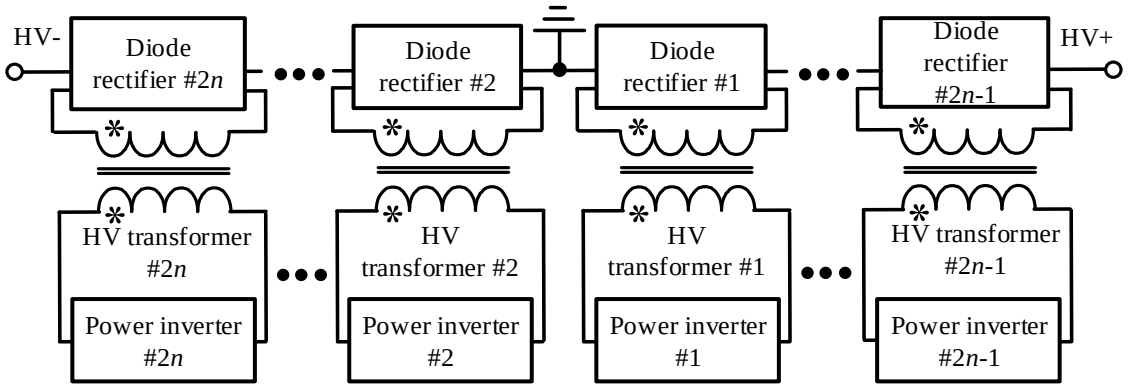



Fig. 3-9 Circuit diagrams for Architecture-6

g) Architecture-7: Multiple inverters + single transformer + multiple rectifiers

HV Architecture-7 in Fig. 3-10 is composed of multiple power inverters, a single HV transformer and voltage multiplication. With the introduction of voltage multiplication, the insulation stress for the HV transformer will be reduced. The input voltage for a power inverter in this architecture is lower than the architecture with a single power inverter. This architecture will enable to use of low voltage semiconductor devices for the inverter, or reduce the turn's ratio for a HV transformer. This architecture is new HV architecture which has not been reported in the literature. It is suitable for high input voltage and low to middle power range applications with low insulation stress for a HV transformer.

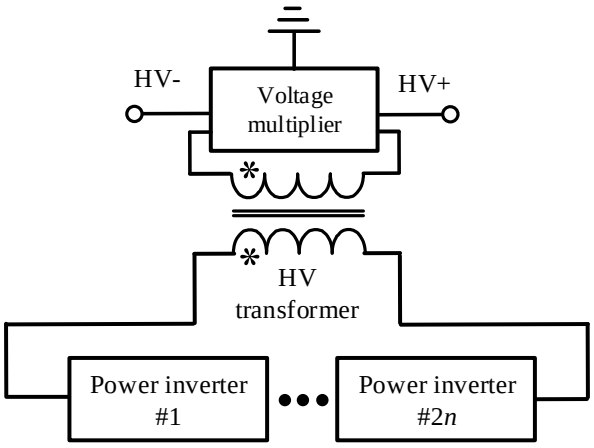



Fig. 3-10 Circuit diagrams for Architecture-7

h) Architecture-8: Multiple inverters + multiplier transformers + multiple rectifiers [3-69]-[3-81].

HV Architecture-8 in Fig. 3-11 is composed of multiple power inverters, multiple HV transformers and voltage multipliers. Architecture-8 with fully distributed inverters, HV transformers and a multiplier are the most complicated architecture among the eight HV architectures. This Architecture is suitable for medium to high power rating, high output voltage rating applications. The insulation stress and electrical stress for subcomponents have been reduced by fully distributed inverters, HV transformers and multipliers.

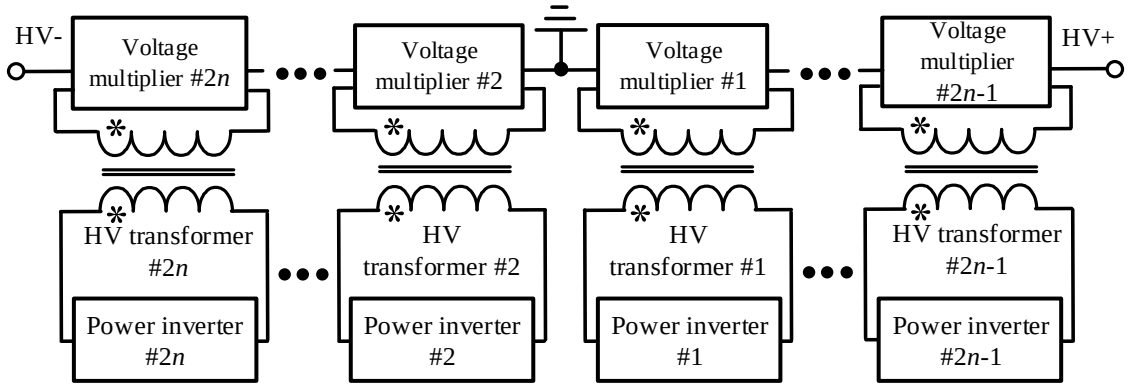



Fig. 3-11 Circuit diagrams for Architecture-8

### 3.2.3 Discussions

Taking single inverter configuration as a case study, the map of HV pulse converter Architecture at different output voltage levels and output power levels is illustrated in Fig.3-12. The distributed architecture with modular HV transformers and modular rectifications provides scalability for high output voltage and power applications with low electric stress for subcomponents in a HV tank.

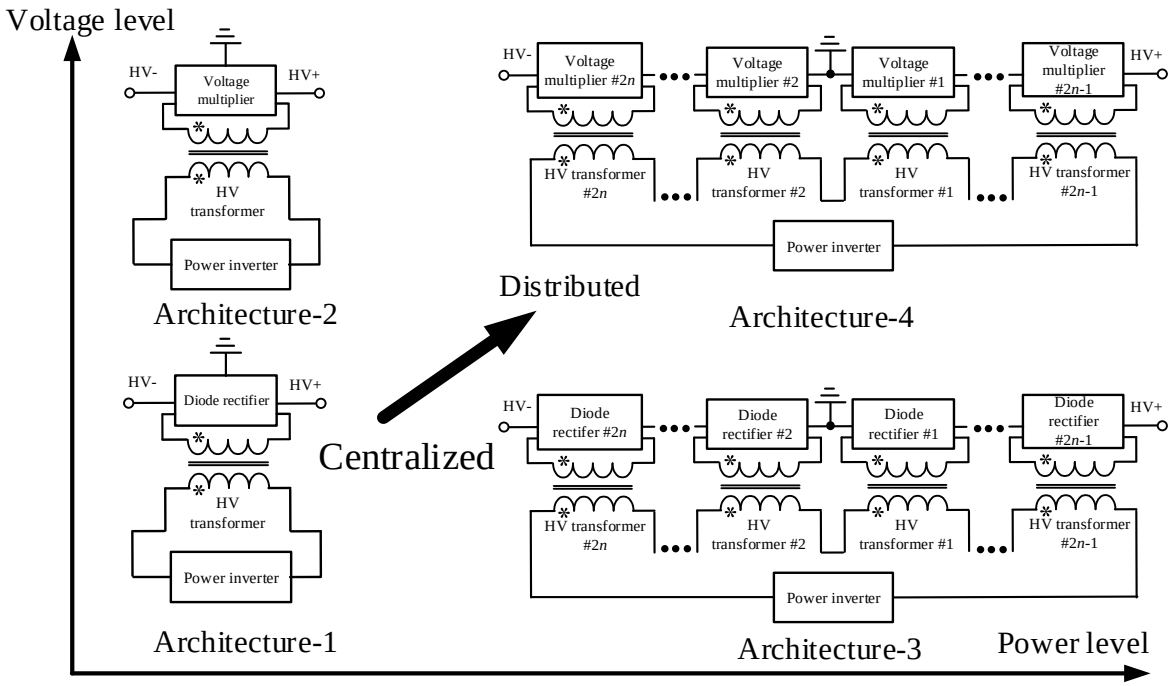


Fig. 3-12 Map of HV pulse converter architectures for different output voltage and power levels

Architecture classification provides a clear overview of all possible architectures. Each HV architecture may fit only one kind of application. The centralized architecture with a single power building block behaves as a simple configuration, but suffers from large electric stress for power building blocks when the output voltage and power rating get higher. The power density and efficiency improvement are a challenge due to high insulation stress and large parasitic components for the HV transformer when the switching frequency further increases. Furthermore, it is not scalable for different output voltage and power rating. The distributed architecture with a modular HV transformer, a HV rectifier, and inverter provides the flexibility of scalability for different output voltage and power rating. The electric stress for subcomponents can be greatly reduced. The reduced parasitic components enable high switching frequency for size reduction and efficiency improvement. The challenges will be a larger number of components and consistence of multiple power building blocks.

There are multiple criteria based on different performance requirements for a HV pulse converter. There are trade-offs in criteria (such as pulse speed and HV insulation stress), which means that the choice of the right architecture for particular applications is not obvious.

## 3.3 Evaluation of HV pulse converter architectures

### 3.3.1 Performance requirements

The key performance requirements for a HV pulse converter are discussed in Chapter 1 and listed below:

- High efficiency
- High power density
- Good HV pulse quality (dynamic: a HV pulse with short rise and decay time; steady state: small HV ripple)
- Low HV insulation stress
- Modularity

HV architectures will impact all of the above performances. Evaluations on the advantages and disadvantages of HV architectures will be introduced based on the key performance items such as power density, HV pulse rise and decay times, HV pulse ripple, efficiency and scalability.

**(a)** Efficiency

The efficiency of a HV pulse converter is a critical requirement for reducing the power loss. The efficiency is related to the electrical stress of the main power building blocks of the HV pulse converter system (inverter, transformer, rectifier) based on different HV architectures. The efficiency is also influenced with transformer technology based on magnetic core materials and winding structure, rectification or multiplication technology based on HV diode characteristics, dielectric characteristics of the HV capacitor, switching

frequency, transformer coupling coefficient, HV insulation technology, and packaging technology. A typical power loss distribution chart for a 300kHz 2kW 120kV HV pulse converter in Architecture-4 is provided in Fig.3-13[3-82]. From the power loss distribution chart, the MOSFETs, resonator, HV transformer and HV multiplier have critical contribution for the power loss. The distribution of power loss will be changed with different HV architectures, switching frequency and power building block technologies, as well as insulation materials for components and system packaging.

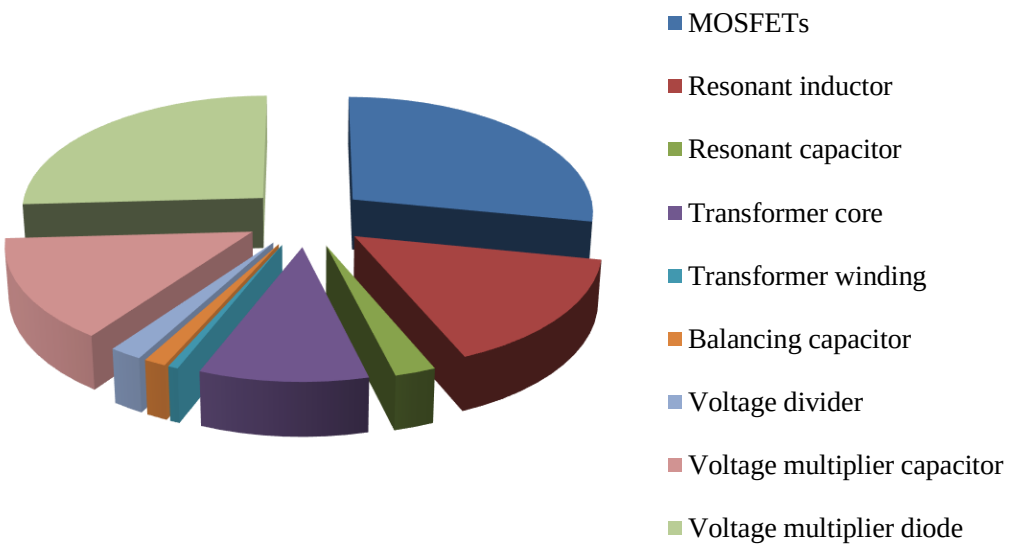



Fig. 3-13 Power loss distribution chart for a 300kHz 2kW 120kV HV pulse converter [3-82]

**(b)** Power density

Power density is a key performance item for a HV pulse converter. High power density will provide a compact size, mobility and cost effectiveness for industrial applications. The weight distribution and HV tank size distribution charts are illustrated in Fig. 3-14 and Fig. 3-15 by taking 50kHz switching frequency 50kW, 120kV industrial HV pulse converter products with a single HV transformer and six stages HV multipliers as a case study. From the weight distribution chart, the HV tank which mainly includes a HV transformer, a HV multiplier, resonators and auxiliary HV circuits, dominates the weight. The HV multiplier contributes the largest portion of the HV tank, while the HV transformer also accounts for more than one third of the HV tank volume. The volume distribution portion for the HV multiplier and HV transformer can be changed with different HV architectures, different components' technology and packaging [3-82].

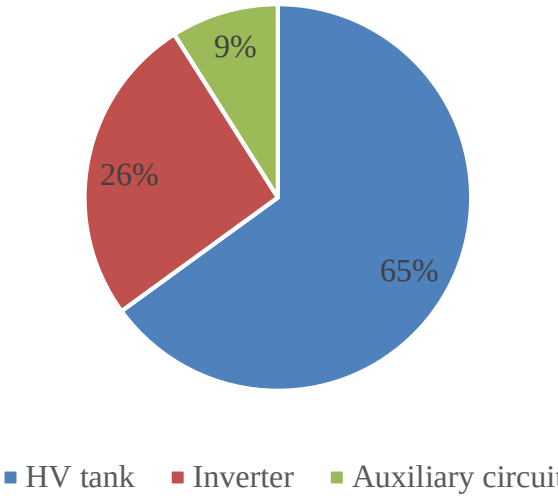



Fig. 3-14 Volume distribution for the HV pulse converter [3-82]

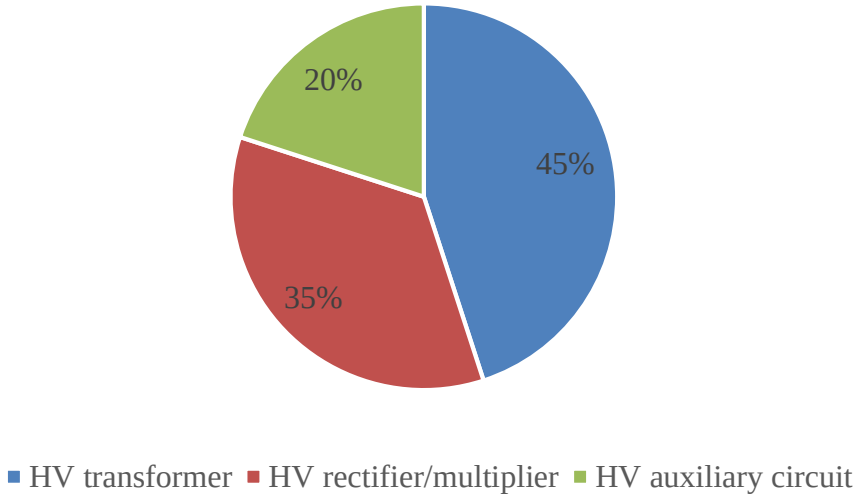



Fig. 3-15 Size distribution for the HV tank [3-82]

The relationship curve between power density and switching frequency are shown in Fig. 3-16 based on medical X-ray generator HV pulse converter products [3-82]. It can be seen from the curve that the power density will keep increasing when the switching frequency increases. The high switching frequency will help to reduce the size of HV passive components such the HV transformer, HV multiplier capacitor and resonators. High switching frequency will also generate large power loss for magnetic core and windings. Furthermore, the high frequency insulation stress needs to be considered for the HV transformer operating at a high switching frequency. As the switching frequency gets higher, the power density keeps increasing. However, the power density increase at higher switching frequency will not be linear at 300-500kHz, and it will start to flatten since sufficient insulation is required for the HV pulse converter though the magnetic core size can be reduced. The increased power loss at high frequency will also limit the power density

increase. From another viewpoint, it also needs better semiconductor devices such as silicon carbide MOSFETs and a rectifier as well as packaging and thermal management technology to address the HV pulse converter power density improvement [3-82].

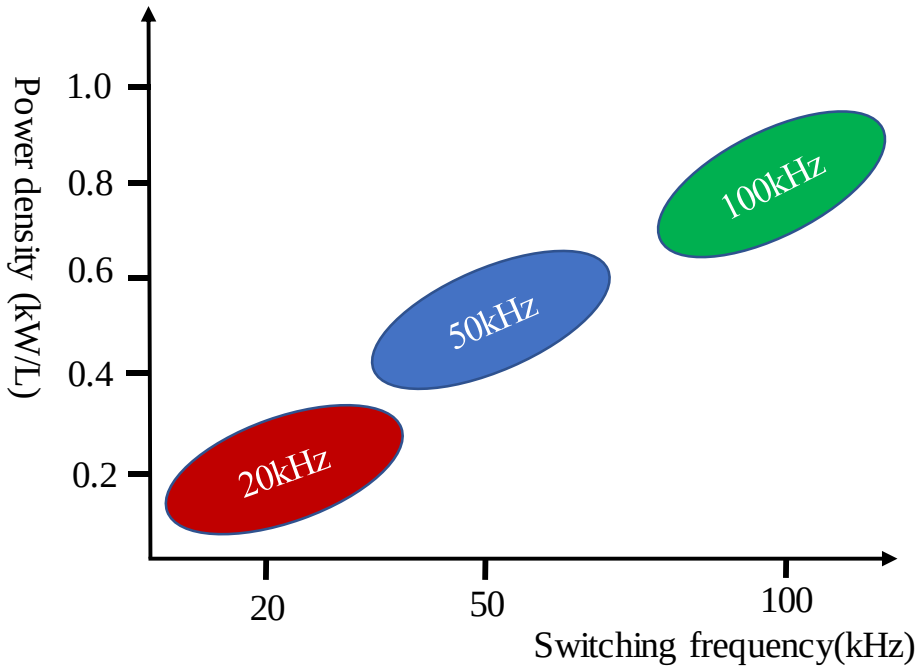



Fig. 3-16 The relationship curve between power density and switching frequency [3-82]

**(c)** HV pulse rise and decay time

HV pulse rise and decay time is critical to the HV pulse converter system performance. Sharp HV pulse with short rise and decay time is requested based on different industrial applications. The HV pulse rise and decay time will be different for different HV architectures. It will be affected by the output capacitance, load resistance, switching frequency and inverter power capability. The output capacitance is the most critical point for HV pulse rise and decay times.

**(d)** HV pulse ripple

HV pulse ripple is also important for HV pulse converter system performance such as imaging quality for CT and X-ray machines. The HV pulse ripple is impacted by different HV architectures.

**(e)** HV insulation

HV insulation has high impact on the HV pulse converter system volume and weight. HV insulation stress will lead to large dielectric loss. Besides, HV insulation also affects the HV insulation materials, assembly and packaging costs. Different HV architectures will lead to different insulation stress for the subcomponents and packaging for a HV pulse converter system.

**(f)** Modularity

Based on the level of modularity of the main power building blocks of the HV pulse converter system (inverter, transformer, rectifier), the distribution of power building blocks provides the scalability for a HV pulse converter system. The power rating, HV pulse converter and HV insulation capability can be enhanced with the distribution of power building blocks, and maintains the same electrical and insulation stress for power building blocks of the HV pulse converter system. Higher power or high output voltage rating can be achieved by parallel or series combinations of standard power building blocks. The scalability for the HV pulse converter system is important for mass production, and ease of manufacturing to save cost and development time.

### 3.3.2 Evaluation specifications

In order to compare the strengths and weaknesses of each HV architecture, the architectures are analysed in detail using the specifications in Table 3-2 as a case study. The input voltage is 400VDC and the output voltage is from 10 to 100kVDC. The output power is from 1 to 10kW. The HV architectures' performance evaluation with other voltage and power rating can be performed with similar methods. From the HV architectures' performance analysis in the case study, the most suitable architecture can be identified based at different output voltage and power ranges.

Table 3-2 The specifications of HV pulse converter for architectures' evaluation study

| | |
|---|---|
| Input voltage | 400VDC |
| Output voltage | 10~100kVDC |
| Output power | 1~10kW |

### 3.3.3 Evaluation assumptions

The following are some assumptions to simplify the HV architectures evaluations:

1. Analysis and evaluation will focus on the HV Architecture-1 to Architecture-4 with single inverter configuration. HV Architecture-5 to Architecture-8 are based on multiple inverter configurations. The performance of the HV pulse converter are mainly determined by the HV transformer and HV rectifier in the HV tank. Single or multiple configurations of the inverters has only minor impact on the HV pulse converter performance.

2. Ferrite magnetic core is considered and planar shape magnetic core is used as much as possible to achieve a compact size. Ferrite magnetic core is a promising magnetic material for the HV transformer operate from a few tens of kHz to several hundreds of kHz. The planar shape magnetic core can effectively reduce the height of HV transformer.

3. The current density for transformer windings is fixed at $4A/mm^2$. The same current density is adopted for the transformer winding design for all 4 HV architectures.

4. The capacitance of the multiplier is chosen to achieve the same HV pulse ripple. Low HV pulse ripple for the HV pulse converter is required to achieve good system performance such as good imaging quality for CT/X-ray generators [3-43]. 1% of the HV pulse ripple is set for capacitance calculation for HV rectifiers.

5. The multiplier stage number is limited to six to avoid very long HV pulse rise and decay time. Large stage numbers of multipliers can help to reduce the insulation stress for a HV transformer. But the HV pulse rise and decay time will become very long if the multiplier stage number is large. Six multiplier stages are the maximum number for architectures' comparisons.

6. The switching frequency investigation range is 100~300kHz. The highest switching frequency for existing HV pulse converter product is below 100kHz.

7. The parasitic capacitance value of a HV transformer refers to the HV transformer prototype parameters measurements in the laboratory. The parasitic capacitance value of the HV transformer is required to calculate the high frequency AC dielectric loss for the HV transformer windings.

8. Thermal management is not taken into consideration for the design at this stage. It is assumed that the oil merged HV tank and enclosure can dissipate the heat generated by HV pulse converter.

### 3.3.4 Evaluation criteria

Table 3-3 gives the HV architecture performance evaluation criteria to provide quantitative analysis using 100kV, 10kW power rating in a case study based on performance scores for efficiency, power density, HV ripple, HV pulse rise and decay time, HV insulation and modularity. The HV architecture performance evaluation criteria are applied for all four HV architectures.

- Efficiency: If the efficiency is between 60% to 70%, the ranking score is 1. If the efficiency is higher than 95%, the ranking score is 5.
- Power density: based on the size of key components, the HV transformer and HV rectifier in a HV tank. If the size of the HV tank is between 4000$cm^3$ and 5000$cm^3$, the ranking score is 1. If the size of the HV tank is smaller than 1000$cm^3$, the ranking score is 5.
- HV ripple: based on peak to peak value of the HV ripple. If the HV ripple is between 2.0%-3.0%, the ranking score is 1. If the HV ripple is less than 1% of rated HV voltage, the ranking score is 5.
- HV pulse rise and decay times: the HV pulse decay is used for the ranking score. If the HV pulse decay times are between 2.0ms and 3.0ms from 100% to 50%, the ranking score is 1. If the HV pulse decay times are faster than 0.1ms, the ranking score is 5.
- HV insulation: based on high frequency AC stress for the HV transformer. If the high frequency AC stress for the HV transformer is between 50% to 100% of out voltage, the ranking score is 1. If the high frequency AC stress for the HV transformer is lower than 1% of out voltage, the ranking score is 5.
- Modularity: based on the modularity level of the HV pulse converter subcomponents. If the transformer, rectifier are all single configurations, the ranking score is 1. If both the transformer and rectifier are multiple configurations, the ranking score is 4. The ranking core achieves 5 when the transformer, rectifier, as well as the inverter are multiple configurations.

Table 3-3 HV architecture performance evaluation criteria (100kV/10kW)

| Score | Efficiency | Power density | HV ripple | HV pulse decay time | HV insulation | Modularity |
|---|---|---|---|---|---|---|
| 1 | 60% | 2.0kW/L | 3.0% | 2.0ms | 100% HV output | Single transformer, single rectifier |
| 2 | 70% | 2.5kW/L | 2.5% | 1.5ms | 50% HV output | Multi-rectifier Single transformer |
| 3 | 80% | 3.3kW/L | 2.0% | 1.0ms | 10% HV output | Multi-transformer Single rectifier |
| 4 | 90% | 5.0kW/L | 1.5% | 0.5ms | 5% HV output | Multi-transformer and multi-rectifier |
| 5 | 95% | 10.0kW/L | 1.0% | 0.1ms | 1% HV output | Multi-transformer and multi-rectifier, multi-inverter |

### 3.3.5 Evaluation methodology and first-order evaluation flow chart

The HV architectures' evaluation is based on the above assumptions, specifications and criteria for different out voltage and power rating. Firstly, the switching frequency is chosen at the minimum HV tank power loss for the first order design and evaluation to understand the advantages and challenges. Then, according to the requirements of input voltage, output voltage, and output power, HV transformer magnetic cores, windings and HV rectifiers will be calculated based on the first order design. Finally, ranking scores are calculated and summarized based on the first order design results for all four HV architectures. The HV architecture evaluation flow chart is illustrated in Fig. 3-17. Iterations are required when the design step cannot meet the target.

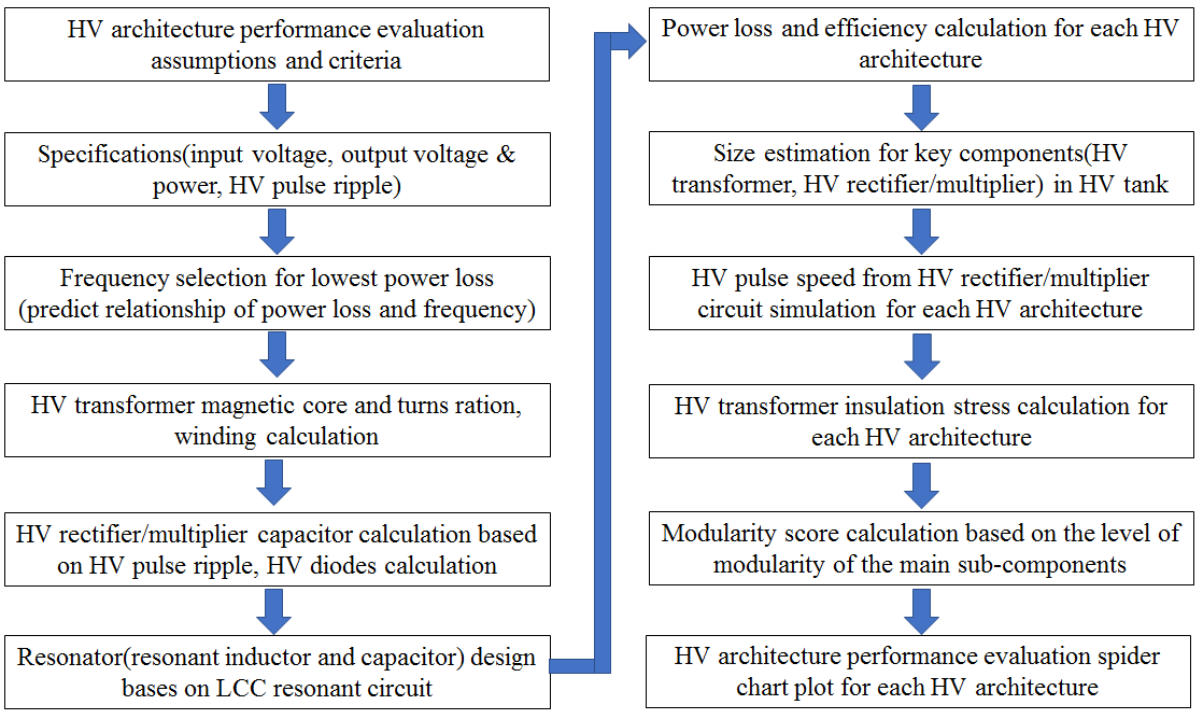



Fig. 3-17 HV architecture evaluation flow chart

The required magnetic core of the HV transformer is based on the AP method in expression (3-1)

$$AP = \frac{P_O(1+\frac{1}{\eta})}{2\pi f K_u K_w J_w B_{\max}} \tag{3-1}$$

where, $P_o$ is the output power, $\eta$ is the efficiency, $f$ is the minim frequency, $B_{max}$ is the maximum flux density, $K_u$ is core geometry factor, $K_w$ is window utilization factor, $J_w$ is the winding current density.

The turns number of the HV transformer primary and secondary windings can be determined by (3-2) and (3-3):

$$n_2 = \frac{V_{\text{sec}}}{2 f B_{\max} A_e} \tag{3-2}$$

$$n_1 = n_2 \cdot \frac{V_{in}}{V_{\text{sec}}} \tag{3-3}$$

where, $V_{sec}$ is the voltage of transformer secondary winding, $A_e$ is the effective core area, $n_1$ and $n_2$ are the turns numbers of the HV transformer primary and secondary windings.

**Transformer magnetic core loss**

The magnetic core loss can be calculated based on the Steinmetz equation which expresses core loss density as a power law with a fixed exponent of frequency and flux density

$$P_{core} = k_{core} \cdot f^m \cdot B_{\max}^n \cdot V_{core} \tag{3-4}$$

where $k_{core,}$ $m$, and $n$ are constants provided by the magnetic core manufacturer, $f$ is the switching frequency and $B_{max}$ is the maximum flux density. $V_{core}$ is the volume for the magnetic core.

**Transformer winding loss**

The transformer winding conduction loss is expresses as:

$$P_{winding\_con} = I_p^2 \cdot R_{pw\_AC} + I_s^2 \cdot R_{sw\_AC} \tag{3-5}$$

where, $I_p$ is the RMS value of the transformer primary current. $I_s$ is RMS value of transformer secondary current. $R_{pw\_AC}$ is the AC resistance for primary winding, and $R_{sw\_AC}$ is the AC resistance for secondary winding.

Winding losses in transformers dramatically increase with high frequency due to eddy current effects. For a sinusoidal excitation with frequency $f$, the skin depth $\delta$ is given by

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{3-6}$$

where, $\rho$ is the conductor resistivity, $\mu$ is the permeability and $f$ is the frequency.

The ratio of ac resistance to dc resistance of transformer windings $F_r$ is calculated based on Dwell's formula [3-83]:

$$F_r = \frac{R_{AC}}{R_{DC}} \tag{3-7}$$

where, $R_{DC}$ is the DC resistance of the winding and $R_{AC}$ is the AC resistance of the winding.

$$F_r(\xi, m) = \frac{\xi}{2} \frac{\sinh \xi + \sin \xi}{\cosh \xi - \cos \xi} + (2m-1)^2 \frac{\sinh \xi - \sin \xi}{\cosh \xi + \cos \xi} \tag{3-8}$$

where $h$ is the height of windings and $m$ is the layer of windings. $\xi$ is the normalized conductor height related to skin depth and

$$\xi = \frac{\sqrt{\pi}}{2} \frac{h}{\delta} \tag{3-9}$$

where $\delta$ is the skin depth in the conductor and $h$ is the height of windings.

The dielectric loss of winding in the HV transformer can be calculated as [3-84]

$$P_{winding\_die} = 2\pi f * C_{wp} * V_{cwp}^2 * \tan \delta \tag{3-10}$$

where $C_{\mathrm{wp}}$ is the parasitic winding capacitance of the HV transformer. It is related to the dielectric constant of the winding insulation materials and the electric field strength across the winding. $V_{\mathrm{CWP}}$ is the voltage applied to parasitic winding capacitance. tanδ is the dissipation factor of the insulation materials.

The total winding loss can be expressed as

$$P_{winding} = P_{winding\_con} + P_{winding\_die} \tag{3-11}$$

**HV rectifier loss**

The power loss of the capacitors in the rectifier or multiplier circuit is:

$$P_{cap\_rec} = \frac{\tan \delta I_{crec\text{-}rms}^2}{2\pi f C_{rec}} \tag{3-12}$$

where $C_{rec}$ is the capacitor of rectifier or multiplier and $I_{crec\text{-}rms}$ is the RMS value of the AC current flowing through the capacitor of the rectifier or multiplier.

The power loss of the diode in the rectifier or multiplier circuit mainly consists of two parts: conduction loss and reverse recovery loss. The conduction loss can be calculated using the following expression:

$$P_{\text{diode}\_rec\_con} = V_{F0} I_{\text{d\_Fav}} + I_{\text{d}\_rms} R_d^2 \tag{3-13}$$

where $I_{d\_Fav}$ is the average current flowing through the diode and $I_{d\_Fav}$ is the RMS current. The conduction losses of the anti-parallel diode can be estimated by using a diode approximation with a series connection of DC voltage source ($V_{F0}$) representing the diode on-state zero-current voltage and a diode on-state resistance ($R_d$).

The switching loss can be approximated as follows:

$$P_{\text{diode}\_rec\_\text{rr}} = fQ_{rr}V_r \tag{3-14}$$

where $Q_{rr}$ is the diode reverse recovery charge and $V_r$ is the reverse voltage of the diode.

The total loss of the diode can be expressed as

$$P_{d\,\text{iode}\_rec} = V_{F0} I_{\text{d\_Fav}} + I_{\text{d}\_rms} R_d^2 + fQ_{rr}V_r \tag{3-15}$$

The total loss of the HV tank is expressed as

$$P_{HV\_\text{tank}} = P_{core} + P_{winding} + P_{\text{diode}\_rec} + P_{cap\_rec} \tag{3-16}$$

Since the inverter is outside the HV tank enclosure, the power loss of the HV tank is critical to evaluate the performance of the HV pulse converter. The total power loss of the HV transformer and voltage multiplier in HV tank is a function of frequency. The relationship curve between HV tank power loss compared to different frequencies for 100kV/10kW HV pulse converter is shown in Fig. 3-18. This shows that the operation frequency for different architectures will be different. The optimal switching frequency is determined at the minimum HV tank power loss for each HV architecture.

Fig. 3-19 gives the relationship curve of HV tank power loss against. frequency (100kHz ~1MHz) and magnetic flux density for a 100kV/10kW rating HV pulse converter. The preferred switching frequency investigation range is 100kHz~300kHz. The relationship curve of a HV tank's power loss against frequency (100kHz~300kHz) and magnetic flux density for 100kV/10kW rating HV pulse converter is shown in Fig. 3-20. The switching frequency with the lowest HV tank power loss for HV Architecture-1 and Architecture-3 are 100kHz. Meanwhile, the optimum switching frequencies to achieve minimum HV tank power loss for HV Architecture-2 and Architecture-4 are 110kHz and 126kHz respectively.

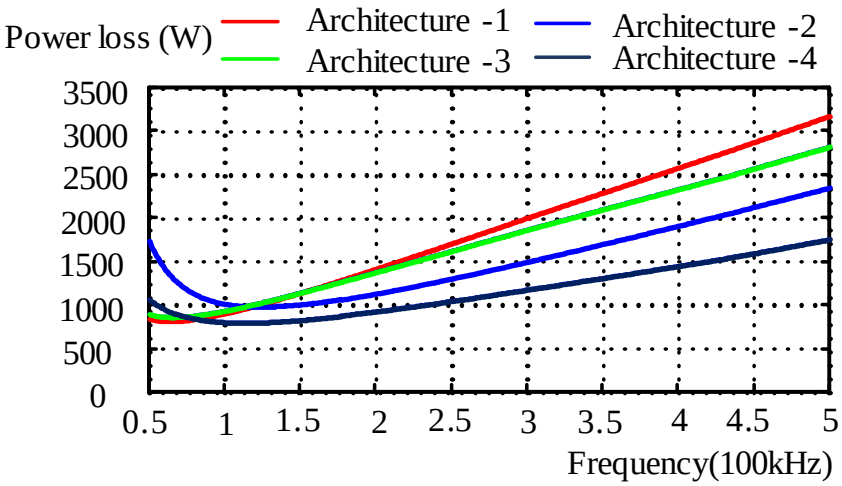



Fig. 3-18 Relationship curve between HV tank power loss against frequency (100kV/10kW HV pulse converter as case study)

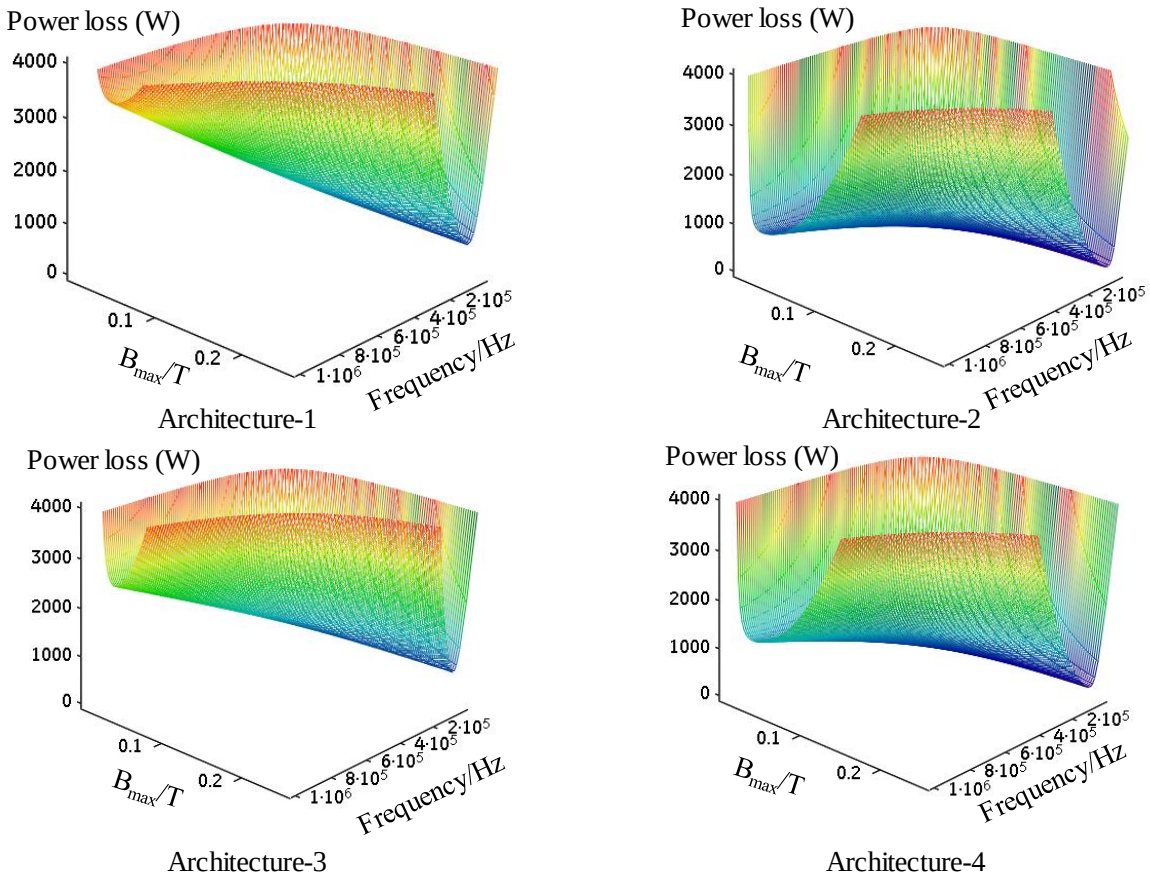



Fig. 3-19 Relationship curve between HV tank power loss against. frequency (100kHz ~1MHz) and magnetic flux density for a 100kV/10kW rating HV pulse converter

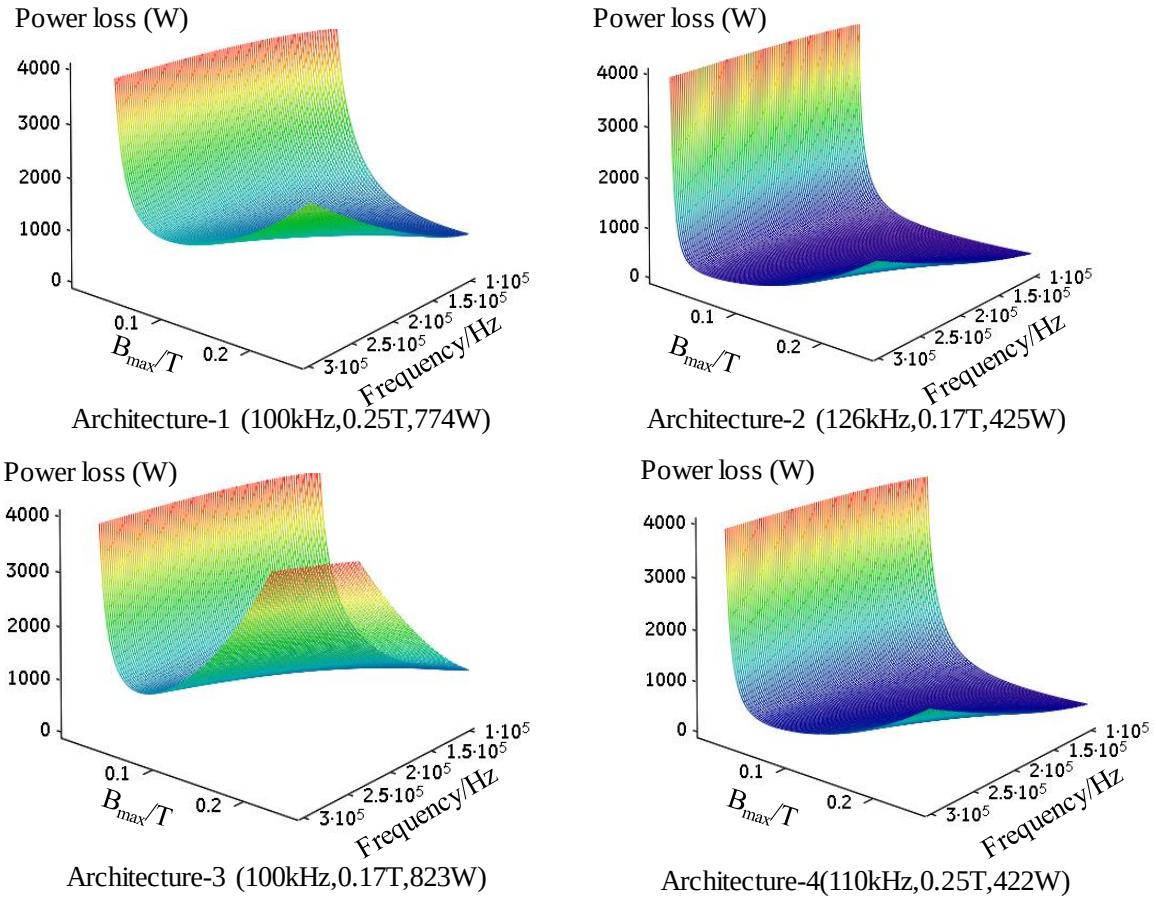



Fig. 3-20 Relationship curve between HV tank power loss against frequency (100kHz ~300kHz) and magnetic flux density for a 100kV/10kW rating HV pulse converter

From the relationship curve of HV tank power loss against frequency and magnetic flux density, the magnetic core loss dominates the total HV tank power loss at low frequency, and the winding loss will increase greatly at high frequency. The lowest HV tank power loss occurs at balanced copper loss and iron loss, as well as multiplier loss. HV Architecture-4 outperforms the other three architectures at high frequency (above 100kHz). It is the most promising option with high efficiency above 100kHz frequency.

### 3.3.6 Evaluation results

Based on the first order design and calculation, the circuit diagrams for four HV architectures under evaluation are illustrated in Fig. 3-21.

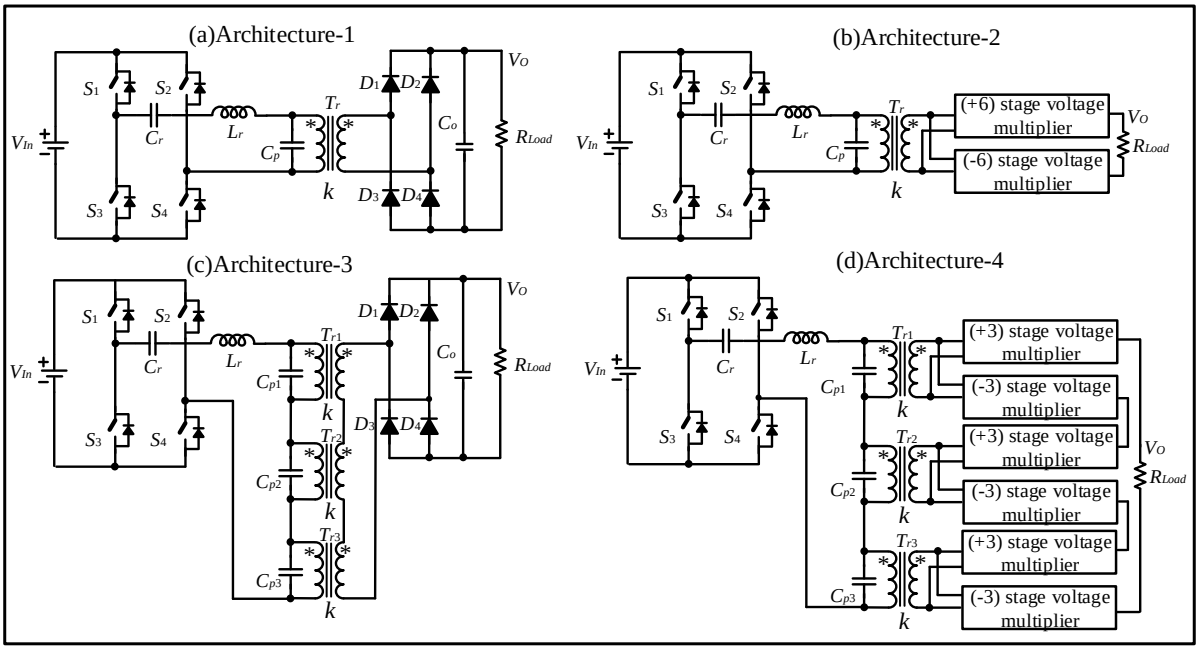



Fig. 3-21 Circuit diagrams for four HV pulse converter architectures under evaluation

**(1)100kV/10kW**

According to Table 3-3 HV architecture performance evaluation criteria (100kV, 1~10kW), the performance evaluation results for a 100kV, 10kW rating HV pulse converter are given in Table 3-4. Architecture-4 achieves the highest-ranking core among the four HV architectures. The ranking score for Architecture-1 is the lowest due to large insulation stress and low modularity level. Fig. 3-22 illustrates the HV architecture performance charts for a 100kV, 10kW rating HV pulse converter. HV pulse converter Architecture-4 overall outperforms the other three architectures based on the performance chart at 100kV/10kW rating. Architecture-3 suffers the lowest power density. HV Architecture-1 and Architecture-3 with a single HV rectifier behave with short HV pulse rise and decay times. The HV pulse pulse rise and decay times for Architecture-2 are the longest. The HV insulation stress for Architecture-1 and Achitecture-3 with a single HV rectifier are larger than Architecture-2 and Architecture-4 with multiple rectifiers. The efficiency for all four architectures is between 90% to 95%. The HV ripple is designed to meet 1% for all four architectures.

The reason of the big performance score differences for the HV pulse rise and decay times for the four HV architectures is due to the difference in HV tank capacitance. The voltage multiplier capacitance value is determined to meet the HV pulse ripple at lower than 1% of HV output voltage.

The peak-to-peak HV pulse ripple of the multi-stage half-wave Cockcroft–Walton voltage multiplier is approximated in [3-74] if the capacitors throughout all the multiplier stages are equal:

$$\delta Vpp = \frac{n(n+1)P_O}{2fC_{VM}V_O} \tag{3-17}$$

where, $P_O$ is the output power, $V_O$ is the output voltage, $f$ is the operation switching frequency, $n$ represents the total stage number of voltage multiplier and $C_{VM}$ is capacitance for the voltage multiplier.

Based on (1), larger voltage multiplier capacitance is required for HV Architecture-2 with positive and negative six stage multipliers compared with HV Architecture-2 with positive and negative three stage multipliers. Furthermore, the operation frequency for HV Architecture-2 is 110kHz, which is slightly lower than the 126kHz for HV Architecture-4. Larger voltage multiplier capacitance is required for lower operation frequency. As a result, more than three times larger capacitance is requested for HV Architecture-2 in order to meet the HV pulse ripple target compared with HV Architecture-4. So, HV Architecture-2 suffers from long HV pulse rise and decay times.

For the diode bridge rectifier based HV pulse converter Architecture-1 and Architecture-3, the HV pulse rise and decay times are shorter than HV Architecture-1 and Architecture-3 using a multi-stage voltage multiplier to meet the same HV pulse ripple requirement.

The big performance score differences for HV insulation come from the insulation stress for the transformer. As shown in Fig. 3-21, the HV insulation stress of the transformer for Architecture-1 is the highest, at around 100% of rated output voltage. With the introduction of three HV transformer modules, HV insulation stress of the transformer for HV Architecture-3 can be limited to below 50kV. More modular transformers can be adopted to further reduce the transformer HV insulation stress, but it needs to balance the performance of power density and insulation stress. With the help of multistage voltage multipliers, the transformer HV insulation stress of HV Architecture-2 and Architecture-4 has been significantly reduced to below 5% of the rated HV pulse converter output voltage.

HV Architecture-4 with a distributed HV transformer and HV multiplier structure outperforms the other three architectures overall, with lowest electrical and insulation stress based on performance comparison. HV Architecture-4 with a distributed HV transformer and HV multiplier structure provides the trade-off performance over Architecture-2 with only multiple HV rectifiers and Architecture-3 with only multiple HV transformers.

The HV pulse converter system can be either optimized based on either the overall performance or the most critical performance item from the HV architecture performance chart. For example, if the HV pulse rise and decay are the most important performance requirement, HV pulse converter Architecture-1 and Architecture-4 will be the best choice although other performance such as power density, HV insulation and modularity are not the best. If the low insulation stress is the most critical performance requirement, HV Architecture-2 with multi-stage voltage multipliers is one of the promising candidates. The selection of optimal HV architecture depends on the most critical requirements the of HV pulse converter system for different industry applications.

Table 3-4 HV architecture performance evaluation results for 100kV/10kW rating HV pulse converter

| | Efficiency | Power density | HV ripple | HV pulse decay time | HV insulation | Modularity | Total score |
|---|---|---|---|---|---|---|---|
| Architeture-1 | 4 | 4 | 5 | 4 | 1 | 1 | 19 |
| Architeture-2 | 4 | 5 | 5 | 1 | 4 | 2 | 21 |
| Architeture-3 | 4 | 3 | 5 | 4 | 2 | 3 | 22 |
| Architeture-4 | 4 | 5 | 5 | 3 | 4 | 4 | 25 |

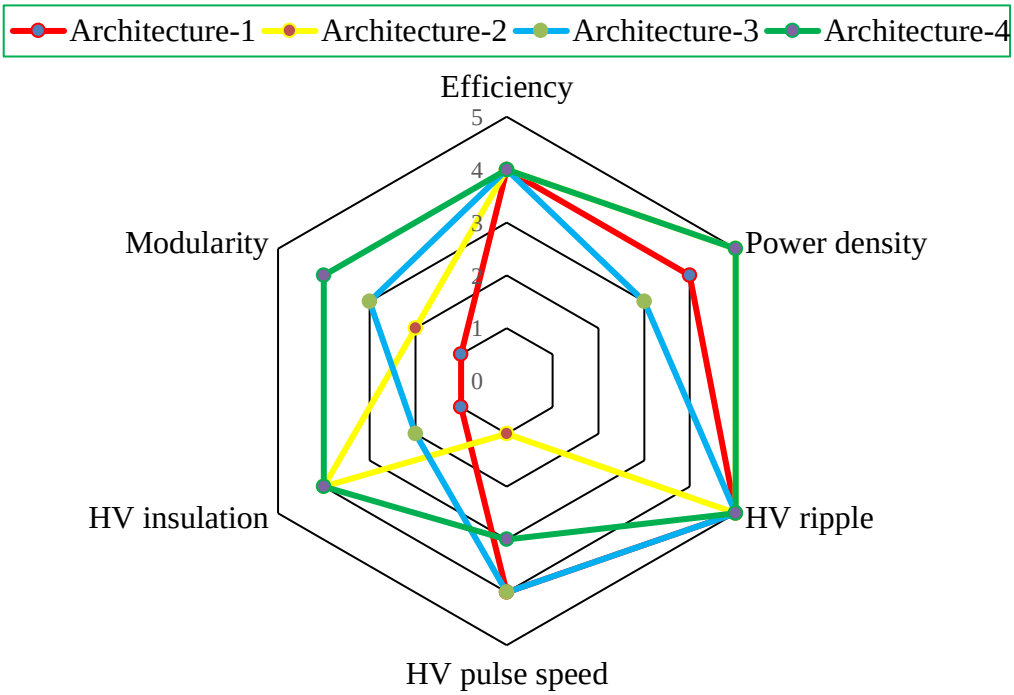



Fig. 3-22 HV Architecture performance charts for a 100kV/10kW rating HV pulse converter

**(2)100kV/1kW**

The performance evaluation criteria and results for a 100kV/1kW rating HV pulse converter are summarized in Table 3-5, Table 3-6 and Fig. 3-23. The efficiency for Architecture-1 is lowest due to high dielectric loss for the HV transformer. Architecture-2 and Architecture-4 with multiple HV rectifiers provide higher efficiency higher than Architecture-1 and Architecture-3 with a single HV rectifier. The score for other performance requirements at 100kV/1kW rating are similar to 100kV/10kW rating. Architecture-4 gets the highest-ranking core among the four architectures. The ranking score for Architecture-1 is the lowest.

Table 3-5 HV architecture performance evaluation criteria (100kV/10kW)

| Score | Efficiency | Power density | HV ripple | HV pulse decay time | HV insulation | Modularity |
|---|---|---|---|---|---|---|
| 1 | 60% | 0.20kW/L | 3.0% | 2.0ms | 100% HV output | Single transformer, single rectifier |
| 2 | 70% | 0.25kW/L | 2.5% | 1.5ms | 50% HV output | Multi-rectifier Single transformer |
| 3 | 80% | 0.33kW/L | 2.0% | 1.0ms | 10% HV output | Multi-transformer Single rectifier |

| | | | | | | |
|---|---|---|---|---|---|---|
| 4 | 90% | 0.5kW/L | 1.5% | 0.5ms | 5% HV output | Multi-transformer and multi-rectifier |
| 5 | 95% | 1.0kW/L | 1.0% | 0.1ms | 1% HV output | Multi-transformer and multi-rectifier, multi-inverter |

Table 3-6 HV architecture performance evaluation results for a 100kV/1kW rating HV pulse converter

| | Efficiency | Power density | HV ripple | HV pulse decay time | HV insulation | Modularity | Total score |
|---|---|---|---|---|---|---|---|
| Architeture-1 | 1 | 4 | 5 | 4 | 1 | 1 | 16 |
| Architeture-2 | 3 | 5 | 5 | 1 | 4 | 2 | 20 |
| Architeture-3 | 2 | 3 | 5 | 4 | 2 | 3 | 19 |
| Architeture-4 | 3 | 5 | 5 | 3 | 4 | 4 | 24 |

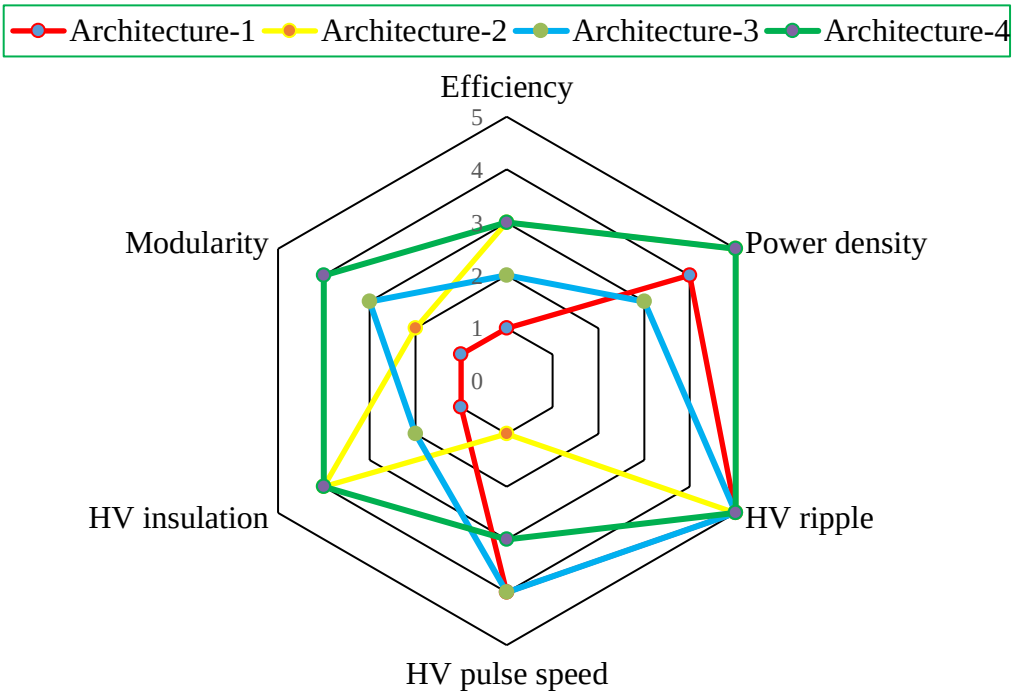



Fig. 3-23. HV architecture performance charts for a 100kV/1kW rating HV pulse converter

**(3)10kV/10kW**

The HV architecture performance evaluation criteria and results for power density at 10kV/ 10kW rating are slightly different with 100kV/10kW rating due to lower output voltage as shown in Table 3-7 and Table 3-8. Architecture-4 ranks highest among the four architectures. Architecture-1 and Architecture-3 achieve the highest efficiency due to low core loss and conduction loss at the primary side. Architecture-3 suffers the lowest power density among the four architectures. Architecture-2 shows the shortest HV pulse rise and decay times. The highest-ranking score is Architecture-4 modular HV tank structures.

Table 3-7 HV architecture performance evaluation criteria (10kV/10kW)

| Score | Efficiency | Power density | HV ripple | HV pulse decay time | HV insulation | Modularity |
|---|---|---|---|---|---|---|
| 1 | 60% | 2.5kW/L | 3.0% | 2.0ms | 100% HV output | Single transformer, single rectifier |
| 2 | 70% | 3.3kW/L | 2.5% | 1.5ms | 50% HV output | Multi-rectifier Single transformer |
| 3 | 80% | 5.0kW/L | 2.0% | 1.0ms | 10% HV output | Multi-transformer Single rectifier |
| 4 | 90% | 10.0kW/L | 1.5% | 0.5ms | 5% HV output | Multi-transformer and multi-rectifier |
| 5 | 95% | 20.0kW/L | 1.0% | 0.1m | 1% HV output | Multi-transformer and multi-rectifier, multi-inverter |

Table 3-8 HV architecture performance evaluation results for a 10kV/10kW rating HV pulse converter

| | Efficiency | Power density | HV ripple | HV pulse decay time | HV insulation | Modularity | Total score |
|---|---|---|---|---|---|---|---|
| Architeture-1 | 5 | 4 | 5 | 4 | 1 | 1 | 21 |
| Architeture-2 | 4 | 4 | 5 | 3 | 4 | 2 | 23 |
| Architeture-3 | 5 | 3 | 5 | 4 | 2 | 3 | 23 |
| Architeture-4 | 4 | 4 | 5 | 4 | 4 | 4 | 26 |

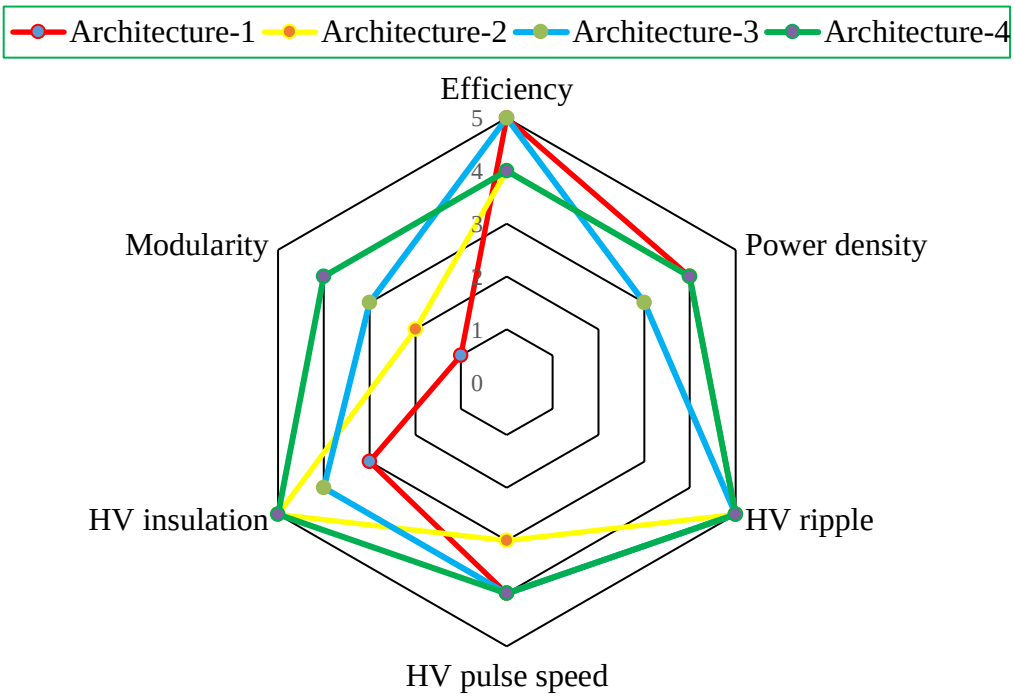



Fig. 3-24. HV architecture performance charts for a 10kV/10kW rating HV pulse converter

**(4)10kV/1kW**

Table 3-9 HV architecture performance evaluation criteria (10kV, 1kW)

| Score | Efficiency | Power density | HV ripple | HV pulse speed | HV insulation | Modularity |
|---|---|---|---|---|---|---|
| 1 | 60% | 1.7kW/L | 3.0% | 2.0ms | 100% HV output | Single transformer, single rectifier |
| 2 | 70% | 2.0kW/L | 2.5% | 1.5ms | 50% HV output | Multi-rectifier Single transformer |
| 3 | 80% | 2.5kW/L | 2.0% | 1.0ms | 10% HV output | Multi-transformer Single rectifier |
| 4 | 90% | 3.3kW/L | 1.5% | 0.5ms | 5% HV output | Multi-transformer and multi-rectifier |
| 5 | 95% | 5.0kW/L | 1.0% | 0.1ms | 1% HV output | Multi-transformer and multi-rectifier, multi-inverter |

Table 3-10 HV architecture performance evaluation results for a 10kV/1kW rating HV pulse converter

| | Efficiency | Power density | HV ripple | HV pulse speed | HV insulation | Modularity | Total score |
|---|---|---|---|---|---|---|---|
| Architeture-1 | 3 | 4 | 5 | 4 | 3 | 1 | 20 |
| Architeture-2 | 4 | 4 | 5 | 1 | 5 | 2 | 21 |
| Architeture-3 | 4 | 1 | 5 | 4 | 4 | 3 | 21 |
| Architeture-4 | 4 | 3 | 5 | 3 | 5 | 4 | 24 |

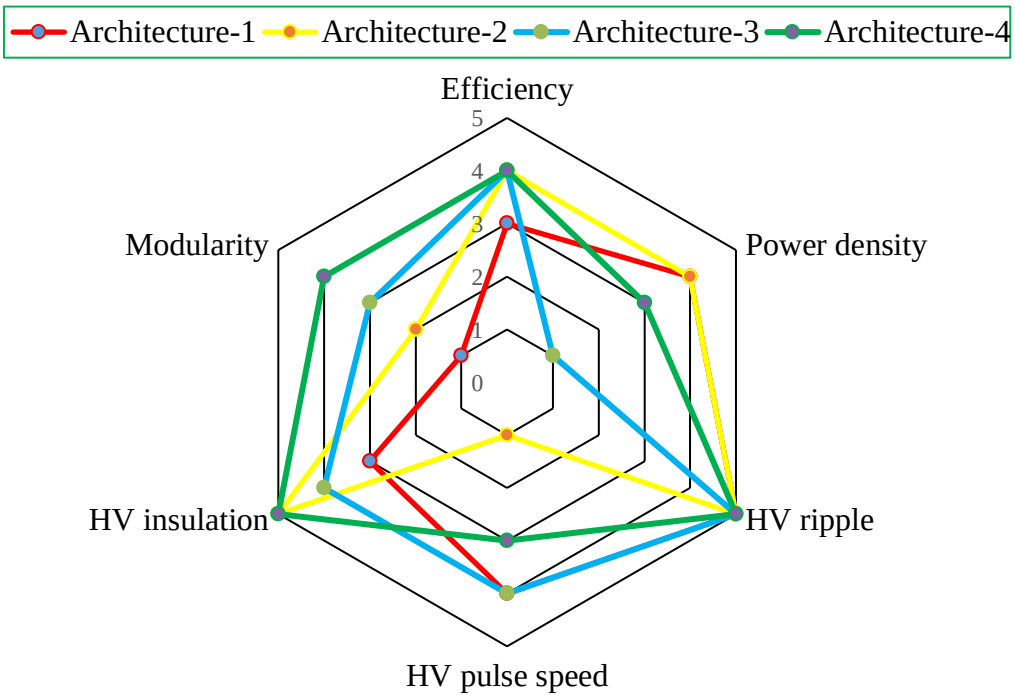



Fig. 3-25 HV architecture performance charts for a 10kV/10kW rating HV pulse converter

HV architecture performance evaluation criteria for power density at 10kV/1kW rating are different to 100kV/1kW rating due to a relative lower output voltage as shown in Table 3-9. The detailed evaluation result and performance charts for the 10kV/1kW rating are given in

Table 3-10 and Figure. 3-25. Architecture-1 suffers the lowest efficiency due to large HV transformer winding loss. Architecture-3 with a multiple HV transformer structure suffers the lowest power density among the four architectures. Architecture-4 scores the highest among all 4 architectures.

### 3.3.7 Discussions

The HV pulse converter architectures evaluation above assumes that each criterion has a weighting of 1. Then the total weight can be calculated. In some industrial applications, certain criteria will be more important than others, which means it will score a higher weighting factor. Then the rank of the total score will be changed accordingly. For example, if a sharp pulse is required for the HV pulse converter, a larger weight (larger than 1) value will change the ranking score. Here, Architecture-3 will be the best candidate compared with other three architectures.

The HV architecture performance charts for all four output power ratings are summarized to provide an overview of the four HV architectures in Fig. 3-26. HV Architecture-4 with distributed HV transformer and HV multiplier structure overall outperforms the other 3 HV architectures with the lowest electrical and HV insulation stress based on architecture performance comparisons.

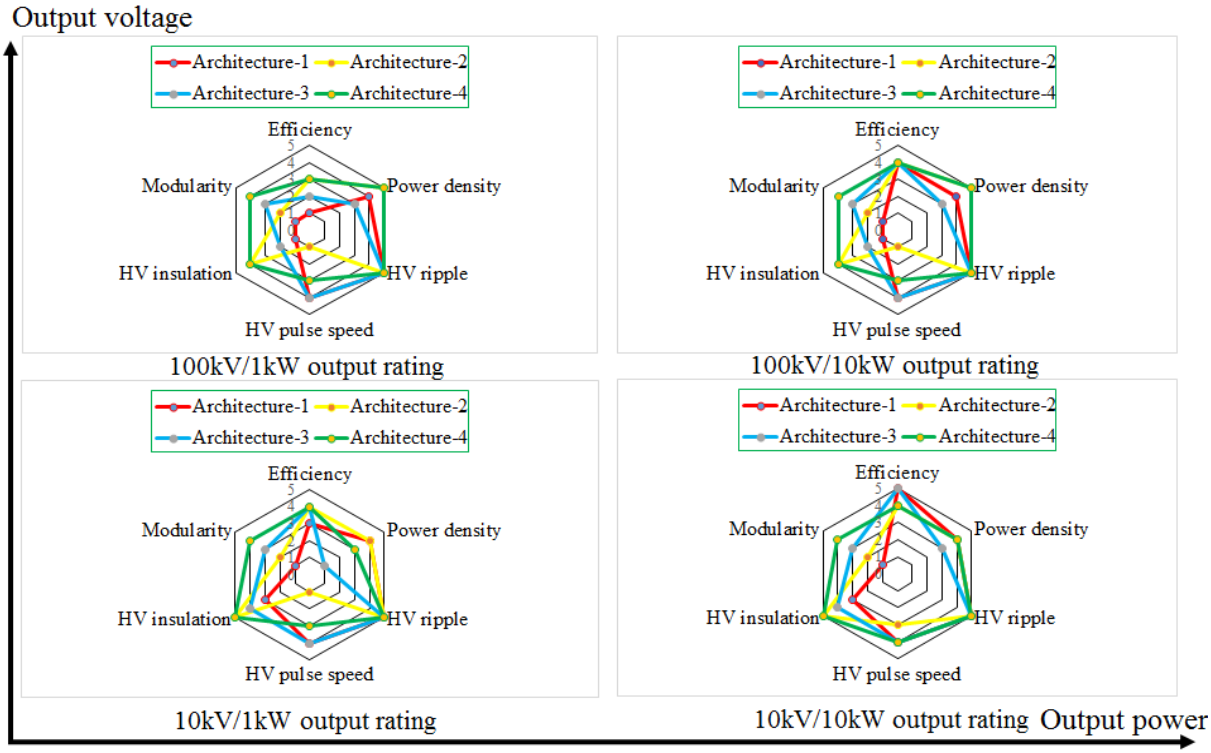



Fig. 3-26 HV pulse converter architecture performance charts

The HV pulse converter system can be either optimized based on either the overall performance or the most critical performance from the HV pulse converter architecture performance chart. For example, if the HV pulse rise and decay time is the most important performance requirement, Architecture-1 and Architecture-4 will be the best choice although the other performance such as power density, HV insulation and modularity are not the best. If low

insulation stress is the most critical performance requirement, Architecture-2 is one of the promising candidate.

## 3.4 Summary

In this chapter, the systematic methodology to derive and classify HV architectures based on the modularization level of power building blocks of HV pulse converter are proposed to summarize the existing architectures and explore new possible ones, such as Architecture-7 with multiple inverters, a single transformer, and multiple rectification structures. The advantages and challenges for each HV architecture are discussed. Furthermore, these HV architectures are evaluated to understand the performance at all four voltage and powers rating: 100kV/10kW, 100kV/1kW, 10kV/10kW, 10kV/1kW. It provides guidelines for HV architecture selection to achieve best performance for different output voltage and power applications.

From the HV architecture performance charts, Architecture-4 with single inverter, multiple transformer, and multiple rectification structure demonstrates the best overall performance on efficiency, power density, HV ripple, HV pulse speed, HV insulation and modularity for single inverter configuration. Similarly, full distributed Architecture-8 with multiple inverter, multiple transformer, and multiple rectification structure outperforms other architecture with multiple inverter configuration for medium to high power rating HV power generation applications. In summary, the modular HV tank architecture (multiple transformer, and multiple rectification structure for Architecture-4 and Architecture-8) is the most promising candidate for further investigation to achieve good performance. However, there are some research gaps for modular HV tank architecture to fully exert the capability.

Firstly, the advantages of modularization for high frequency HV transformer have not been addressed yet. The planar and non-planar packaging structures, as well as HV insulation structures of high frequency HV transformer for modular HV pulse converter architecture need investigations. Chapter 4 will focus on the above analysis for modular HV architecture.

Secondly, the multi-stage multiplier circuit is a key element for modular HV tank architecture. Steady state circuit analysis and HV pulse speed influence factors of a HV multiplier needs investigation. The influence of the diode reverse recovery and the mitigation method for a high frequency multi-stage multiplier circuit needs to be analysed. Chapter 5 will address these research gaps, and provide the analysis and hardware prototype experimental results to validate the concept.

Thirdly, there is a lack of a unified equivalent circuit model which can simplify the design and analysis of LCC resonant converters based HV pulse converter architectures to provide effective guidelines in analysis and design of the HV pulse converter with different HV architectures. The comprehensive design method of modular HV pulse converter architecture has not been well addressed yet. Chapter 6 will introduce the unified equivalent circuit modelling approach for different HV architectures and a comprehensive design method for modular architecture.

## 3.5 References


[3-1] T. Soeiro, J. Biela, J. Muhlethaler, J. Linner, P. Ranstad, and J. W. Kolar, "Optimal design of resonant converter for electrostatic precipitators," in Proc. IEEE IPEC, Jun. 2010, pp. 2294-2301.

[3-2] J. Liu, L. Sheng, J. Shi, Z. Zhang, and X. He, "LCC resonant converter operating under discontinuous resonant current mode in high voltage, high power and high frequency applications," in Proc. IEEE Appl. Power Electron. Conf. Expo., 2009, pp. 1034-1038.

[3-3] J. Liu, L. Sheng, J. Shi, Z. Zhang, and X. He, "LCC resonant converter operating under discontinuous resonant current mode in high voltage high power and high frequency applications," in Proc. Appl. Power Electron. Conf. Expo., 2009, pp. 1482-1486.

[3-4] J. Martin-Ramos, P. J. Villegas, A. M. Pernía, J. Díaz, and J. A. Martinez, "Optimal control of a high voltage power supply based on the PRC-LCC topology with a capacitor as output filter," IEEE Transaction Ind. Appl., vol.49, no. 5, pp. 2323-2329, Sep./Oct. 2013.

[3-5] J. Martin-Ramos, A. M. Pernía, J. Diaz, F. Nuño, and J. A. Martínez, "Power supply for a high voltage application," IEEE Transaction Power Electron., vol. 23, no. 4, pp. 1608-1619, Jul. 2008.

[3-6] T. B. Soeiro, J. M¨uhlethaler, J. Linn´er, P. Ranstad, and J. W. Kolar, "Automated design of a high-power high-frequency LCC resonant converter for electrostatic precipitators," IEEE Transaction Ind. Electron., vol. 60, no. 11, pp. 4805-4819, Nov. 2013.

[3-7] M. G. Giesselmann, T. T. Vollmer and W. J Carey, "100-kV High Voltage Power Supply with Bipolar Voltage Output and Adaptive Digital Control," IEEE Transaction Plasma Sci., vol. 42, no. 10, pp. 2913-2918, 2014.

[3-8] A. Amir, S. Taib, S. Iqbal, "A fixed frequency continuous conduction LCCL series resonant inverter fed high voltage DC-DC converter," in Proc. 2013 IEEE International Conference on Circuits and Systems (ICCAS), pp. 75-80.

[3-9] V. García, M. Rico, J. Sebastián, M. Hernando, and J. Uceda, "An optimized DC–DC converter topology for high voltage pulse loads applications," in Proc. IEEE PESC, 1994, pp. 1413-1421.

[3-10] V. Garcia, M. Rico, J. Sebastian, M. Hernando, and J. Uceda, "Study of an optimized resonant converter for high-voltage applications," in Proc. Power Electronics Congress, 1994, pp. 114-121.

[3-11] V. García, M. Rico, J. Sebastián, and M. Hernando, "Using the hybrid series parallel resonant converter with capacitive output filter and PWM phase-shifted control for high-voltage applications," in Proc. IEEE IECON, 1994, pp. 1659-1664.

[3-12] N. Shafiei, M. Pahlevaninezhad, H. Farzanehfard, A. Bakhshai, and P. Jain, "Analysis of a fifth-order resonant converter for high-voltage DC power supplies," IEEE Transaction Power Electron., vol. 28, no. 1, pp. 85-100, Jan. 2013.

[3-13] M. Giesselmann, T. Vollmer, M. Lara, J. Mayes, "Compact HV-Capacitor Charger," in Proc. IEEE International Power Modulator Conference, 2008, pp. 238-241.

[3-14] S. N. Vukosavić, L. S. Perić, and S. D. Sušić, "A novel power converter topology for electrostatic precipitators," IEEE Transaction Power Electron., vol. 31, no. 1, pp. 152-164, Jan. 2016.

[3-15] C. Loef, R. W. Doncker and B. Ackermann, “On high frequency high voltage generators with planar transformers”, in Proc. APEC, 2014, pp. 1936-1940.
[3-16] J. Martin-Ramos, J. Diaz, A. M. Pernía, J. M. Lopera, and F. Nuño, “Dynamic and steady state models for the PRC-LCC topology with a capacitor as output filter,” IEEE Transaction Ind. Electron., vol. 54, no. 4, pp. 2262-2275, Aug. 2007.
[3-17] J. Martin-Ramos, J. Diaz, F. Nuño, P. J. Villegas, A. López-Hernández, J. F. Gutiérrez-Delgado, “A Polynomial Model to Calculate Stead0y-State Set Point in the PRC-LCC Topology With a Capacitor as Output Filter,” IEEE Transaction Industry Applications, vol. 51, no. 3, pp. 2520-2527, 2015.
[3-18] S. S. Lee; S. Iqbal; M. K. M. Jamil, “A digitally tuned resonant capacitance control with narrow range frequency modulation for ZCS high voltage X-ray power supply,” in Proc. International Conference on Electrical, Control and Computer Engineering 2011 (InECCE), pp. 113-118.
[3-19] W. Luo, X. Wang, “Development of Electric Control High Power Medical-Use X-ray Generator,” in Proc. International Conference on Information Engineering and Computer Science , 2009, pp 1 – 5.
[3-20] L. Zhao, D. Peng, J. D. van Wyk, “Analysis and Design of an LCLC Resonant Converter Suitable for X-ray Generator Power Supply,” in Proc. CPES Annu. Conf., 2000, pp. 360-365.
[3-21] J. Biela and J. W. Kolar, “Using transformer parasitics for resonant converters-A review of the calculation of the stray capacitance of transformers,” in Proc. IEEE 40th IAS Annu. Meeting, 2005, pp. 1868-1875.
[3-22] D. G. Bandeira, T. B. Lazzarin, I. Barbi, “T-Type Parallel Resonant DC-DC Converter for High Voltage Application,” in Proc. IEEE International Conference on Industry Applications (INDUSCON), 2016, pp. 1-8.
[3-23] F. S. Cavalcante and J. W. Kolar, “Design of a 5kW high output voltage series-parallel resonant DC-DC converter,” in Proc. IEEE Power Electron. Spec. Conf., 2003, vol. 4, pp. 1807-1814.
[3-24] J.W. Gong, H.J. Ryoo, S.H. Ahn, S. R. Jang, “Design and Implementation of a 40-kV, 20-kJ-s Capacitor Charger for Pulsed-Power Application,” IEEE Transaction Plasma Science, vol. 42, no. 11, 2014, pp. 3623-3632.
[3-25] W. C. Hsu; J.F.Chen, Y.P. Hsieh,Y.M. Wu, “Design and Steady-State Analysis of Parallel Resonant DC-DC Converter for High-Voltage Power Generator,” IEEE Transaction on Power Electronics, 2017, vol.32, no. 2, pp. 957-966.
[3-26] S. Mao, J. Popovic, J. A. Ferreira, “ An Investigation into High Frequency High Voltage Planar Transformer for High Voltage Generator Applications,” in Proc. IEEE 2016 9th International Conference on Integrated Power Electronics Systems(CIPS), pp. 1-6.
[3-27] J. Sun, X. Ding, M. Nakaoka, and H. Takano, “Series resonant ZCS-PFM DC-DC converter with multistage rectified voltage multiplier and dual-mode PFM control scheme for medical-use high-voltage X-ray power generator,” in Proc. Inst. Elect. Eng., vol. 147, no. 6, pp. 527-534, Nov. 2000.
[3-28] Z. Zhang, Z. Tang, “Pulse frequency modulation LLC series resonant X-ray power supply,” in Proc. IEEE 2011 International Conference on Consumer Electronics, Communications and Networks (CECNet), 2011, pp. 1532-1535.

[3-29] J. Wang, P. Luerkens, S. W. H. de Haan, and J. A. Ferreira, “Analytical analysis of the equivalent parasitic capacitance of the high-voltage cascade multiplier in medical application of X-ray power generator,” in Proc. IPEMC, Jun. 2012, vol. 1, pp. 463-470.
[3-30] Y. A. Wang, D. M. Xiao, and Y. L. Liu, “Design of a planar power transformer for high voltage, high frequency use,” in Proc. IEEE PES Transmission Distrib. Conf. Expo., Apr. 2010, pp. 1-6.
[3-31] S. Mao, J. Popovic, J. A. Ferreira, “High Voltage Pulse Speed Study for High Voltage DC-DC Power Supply Based on Voltage Multipliers,” in Proc. IEEE 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), pp.1-10.
[3-32] P. Lürkens, P. Guimaraes, P. Godignon, J. Millán, “High Voltage SiC Schottky Diodes in Rectifiers for X-Ray Generators,” Materials Science Forum Vols.717-720, 2012, pp 1245-1248.
[3-33] L. Katzir, D. Shmilovitz, “A High Voltage Split Source Voltage Multiplier with Increased Output Voltage,” in Proc. IEEE APEC, 2015, pp. 3272-3275.
[3-34] M. Rentzsch, F. Gleisberg, H. Guldner, F. Benecke, and C. Ditmanson, “Closed analytical model of a 20kV output voltage, 800 W output power series–parallel-resonant converter with Walton Cockcroft multiplier,” in Proc. IEEE PESC, Jun. 2008, pp. 1923-1929
[3-35] L.Katzir, D. Shmilovitz, “A 1-MHz 5-kV Power Supply Applying SiC Diodes and GaN HEMT Cascode MOSFETs in Soft Switching,” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 4, pp. 1474-1482, 2016.
[3-36] L.Katzir, D. Shmilovitz, “Effect of the capacitance distribution on the output impedance of the half-wave Cockcroft-Walton voltage multiplier,” in Proc. IEEE APEC, 2016, pp 3655-3658.
[3-37] S. Iqbal, R. Besar y C. Venkataseshaiah, “A novel control scheme for voltage multiplier based X-ray power supply,” in Proc. Power and Energy Conference, PECON, 2008. pp 1456-1460.
[3-38] H.J. Ryoo, S.R. Jang, Y.S. Jin, J.S. Kim, Y.B. Kim, S.H. Ahn, J.W. Gong, B.H. Lee and D.H. Kim, “Design of high voltage capacitor charger with improved efficiency, power density and reliability,” IEEE Transaction on Dielectrics and Electrical Insulation, Vol. 20, No. 4, pp. 1076-1084, 2013.
[3-39] M. Hu, N. Froehlekw, W. Peters, and J. Boecker, “Multi-objective optimization of LCC resonant converter applied in VLF HV pulse converter,” in Proc. 37th IEEE IECON, Nov. 2011, pp. 1456-1461.
[3-40] S.H. Park; L. Katzir; D. Shmilovitz, “Reduction of voltage drop and ripple in voltage multipliers,” in Proc. 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), pp. 1-7.
[3-41] S. S. Lee, S. Iqbal, and M. Kamarol, “Control of ZCS-SR inverter-fed voltage multiplier-based high-voltage DC–DC converter by digitally tuning tank capacitance and slightly varying pulse frequency,” IEEE Transaction Power Electron., vol. 27, no. 3, pp. 1076-1083, Mar. 2012.

[3-42] Y. Du, J. Wang, G. Wang, and A. Q. Huang, “Modeling of the high frequency rectifier with 10-kV SiC JBS diode in high-voltage series resonant type DC-DC converters,” IEEE Tran. Power Electron., vol.29, no.8, pp. 4288-4300, Aug. 2014.

[3-43] J. Sun, H. Konishi, Y. Ogino, and M. Nakaoka, “Series resonant high-voltage ZCS-PFM DC-DC converter for medical power electronics,” in Proc. IEEE Power Electronics Specialist Conf., vol.3, Jun. 2000, pp. 1247-1252.

[3-44] J. Sun, H. Konishi, Y. Ogino, E. Chu, and M. Nakaoka, “Series resonant high-voltage PFM DC-DC converter with voltage multiplier based a two-step frequency switching control for medical-use X ray power generator,” in Proc. IEEE Power Electronics and Motion Control Conf., vol.2, 2000, pp. 596-601.

[3-45] T. Filchev, D. Cook, P. Wheeler, and J. Clare, “Investigation of high voltage, high frequency transformers/voltage multipliers for industrial applications,” in Proc. IET 4th Int. Conf. Power Electron., Mach. Drives, 2008, pp. 209-213.

[3-46] S. S. Liang and Y. Y. Tzou, “DSP control of a resonant switching high voltage power supply for X-ray,” in Proc. IEEE Power Electron. and drive systems Conf., vol.2, Oct. 2001, pp. 522-526.

[3-47] S. S. Liang and Y. Y. Tzou, “DSP control of a resonant switching high voltage power supply for X-ray,” in Proc. IEEE Power Electron. Drive Syst. Conf., Oct. 2001, vol. 2, pp. 522-526.

[3-48] G. L. Piazza, R. L. Alves, C. H. I. Font; I. Barbi, “Resonant circuit model and design for a high frequency high voltage switched-mode power supply,” in Proc. Brazilian Power Electronics Conference, 2009, pp. 326-331.

[3-49] S. Gavin et al., “A digitally controlled 125 kVdc, 30 kW power supply with an LCC resonant converter working at variable DC-link voltage: Full scale prototype test results,” in Proc.7th IET Int.Conf. PEMD, Apr. 2014, pp. 1-6.

[3-50] T. Filchev; D. Cook; J. Clare; P. Wheeler, “High voltage, high frequency transformer-switching converter integration,” in Proc. IET Conference on High Power RF Technologies, 2009, pp. 1-4.

[3-51] S. Iqbal, R.Besar, C. Venkataseshiah, “A Novel ZCS-SR Voltage Multiplier based High-Voltage DC Power Supply,” in Proc. IEEE International Power and Energy Conference, 2008, pp. 1451-1455

[3-52] H. Sheng et al., “Design and implementation of a high power density three-level parallel resonant converter for capacitor charging pulsed power supply,” IEEE Transaction Plasma Sci., vol. 39, no. 4, pp. 1131-1140, Apr. 2011.

[3-53] F. Dianbo, F. C. Lee, Q. Yang, and F. Wang, “A novel high-power-density three-level LCC resonant converter with constant-power-factor-control for charging applications,” IEEE Transaction Power Electron., vol. 23, no. 5, pp. 2411-2420, Sep. 2008.

[3-54] J. Martin-Ramos, Ó. P. Vaquero, J. D. González, M. A. J. Prieto, J. A. M. Esteban, A. M. Pernía, “Modeling a multilevel converter for radiography and fluoroscopy,” in Proc. 2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), pp. 1-10.

[3-55] A. M. Pernía, O.P. Vaquero, P. J. Villegas; F. Nuño; H. A. Mayor; J. A. Martín-Ramos, “Multilevel converter for X-ray generators,” in Proc. IEEE IECON 2016, pp. 1376-1381.

[3-56] T.F. Wu and J. C. Hung, “A PDM controlled series resonant multi-level converter applied for x-ray generators,” in Proc. IEEE PESC, 1999, pp. 1177-1182.
[3-57] J. A. Martín-Ramos; Ó. Pardo-Vaquero; P. J. Villegas; J. A. Martínez; A. M. Pernía, “Multilevel PRC-LCC resonant converter for X-ray generation,” Electronics Letters, Vol. 51, no.15, 2015, pp. 1189-1191.
[3-58] M. Giesselmann, T, Vollmer; L. Altgilbers, “Modular, Compact HV-Capacitor Charger,” in Proc. IEEE International Power Modulator Conference, 2008, pp. 409-412.
[3-59] Y. Qiu, B. Lu, B. Yang, D. Fu, and F. C. Lee, “A high-frequency high-efficiency three-level LCC converter for high-voltage charging applications,” in Proc. IEEE PESC, 2004, vol. 6, pp. 4100-4106.
[3-60] M. Jaritz, S. Blume. D. Leuenberger, J. Biela, “Experimental Validation of a Series Parallel Resonant Converter Model for a Solid State 115-kV Long Pulse Modulator,” IEEE Transaction on Plasma Science,2015, vol.43, no.10, pp. 3392-3398.
[3-61] B. Jacobson, M. Bamett, R. DiPemi, J, McGinty, “Planar integrated magnetics assembly for high voltage converters,” in Proc. IEEE APEC, 2000, pp. 622-632.
[3-62] M. Jaritz and J. Biela, “Optimal design of a modular series parallel resonant converter for a solid state 2.88 MW/115-kV long pulse modulator,” IEEE Transaction Plasma Sci., vol. 42, no. 10, pp. 3014-3022, Oct. 2014.
[3-63] A. Pokryvailo, C. Carp, and C. Scapellati, “A high-power high voltage power supply for long-pulse applications,” IEEE Transaction Plasma Sci., vol. 38, no. 10, pp. 2604-2610, Oct. 2010.
[3-64] A. K. Jain, C.P. Henze, C.B. Henze and K. Conroy, “Development of a 350kW,10kV pulse power converter for capacitor charging,” in Proc. IEEE APEC, 2007, pp. 1164-1170.
[3-65] S. H. Ahn, H. J. Ryoo, J. W. Gong, and S. R. Jang, “Design and test of a 35-kJ/s high-voltage capacitor charger based on a delta-connected threephase resonant converter,” IEEE Transaction Power Electron., vol. 29, no. 8, pp. 4039-4048, Aug. 2014.
[3-66] I. A. Krichtafovitch, “Modular high-voltage power supplies design,” in Proc. Thirty-Second Intersociety Energy Conversion Engineering Conference(IECEC), 1997, vol.1 pp. 375-380.
[3-67] A. Pokryvailo, C. Carp, C. Scapellati, “A 100 kW high voltage power supply for dual energy computer tomography applications,” IEEE Transaction on Dielectrics and Electrical Insulation, vol.22, no.4, 2015, pp. 1945-1953.
[3-68] L. M. Redondo, J. F. Silva, E. Margato, “Analysis of a modular generator for high-voltage, high-frequency pulsed applications,” Review of Scientific Instruments, 2007, vol.78, pp.1-7
[3-69] J. Biebach, P. Ehrhart, A. Muller, G. Reiner, and W. Weck, “Compact modular power supplies for superconducting inductive storage and for capacitor charging,” IEEE Transaction Magn., vol. 37, no. 1, pp. 353-357, Jan. 2001.
[3-70] S. Iqbal, G. K. Singh and R. Besar, “A Dual-Mode Input Voltage Modulation control scheme for Voltage Multiplier Based X-ray Power Supply,” IEEE Transaction on Power Electronics vol. 23, no. 2, pp. 1003-1008, March 2008.

[3-71] L. Katzir and D. Shmilovitz, “A split-source multisection high-voltage power supply for X-ray,” IEEE J. Emerg. Sel. Topics Power Electron., vol. 4, no. 2, pp. 373-381, Jun. 2016.
[3-72] C. Martins, M. Collins, “Development of a long pulse high power Klystron modulator for the ESS based on the stack multi-level topology,” in Proc. IPAC 2016, pp.3600-3602.
[3-73] J. W. Gong, H. J. Ryoo, S. H. Ahn, S. R. Jang, “Development of 50-kV 100-kW Three-Phase Resonant Converter for 95-GHz Gyrotron,” IEEE Transaction on Plasma Science, vol. 42, no.11, 2014, pp. 3623-3632.
[3-74] L. Katzir and D. Shmilovitz, “A matrix-like topology for high-voltage generation,” IEEE Transaction Plasma Sci., vol. 43, no. 10, pp. 3681-3687, Oct. 2015.
[3-75] S. Iqbal, “A three-phase symmetrical multistage voltage multiplier,” IEEE Transaction Power Electron., vol. 3, no. 2, pp. 30-33, Mar. 2005.
[3-76] S.-R. Jang, H.-J. Ryoo, J. Kim, and G. H. Rim, “Development and optimization of high-voltage power supply system for industrial magnetron,” IEEE Transaction Ind. Electron., vol. 59, no. 3, pp. 1453-1460, Mar. 2012
[3-77] D.-W. Yoo, J.-W. Baek, and H.-S. Son, “Full digital 150 kV–1 A ZVS converter for X-ray power applications,” IEEE Transaction Plasma Science, vol.31, no. 3, pp. 1313-1316, 2003.
[3-78] S. Iqbal, R. Besar and C. Venkataseshiah, “A low ripple voltage multiplier for X-ray power supply,” IEEE International Conference on Power and Energy (PECon 08), 2008, pp. 1451-1455.
[3-79] M. Jaritz, T. Rogg, and J. Biela, “Control of a modular series parallel resonant converter system for a solid state 2.88mw/115-kV long pulse modulator,” in Proc. 17th Eur. Conf. Power Electron. Appl, Sep. 2015, pp. 1-11.
[3-80] S Iqbal, R Besal, C. Venkataseshaiah, “Single-Three-phase Symmetrical Bipolar Voltage Multipliers for X-ray Power Supply,” in proc. Second International Conference on Electrical Engineering, 2008, pp. 30-33.
[3-81] Y. M. Seo, M. S. Byun; S.C. Hong, “Hybrid type X-ray generator for fluoroscopy X-ray system available in low-capacity AC power source,” in Proc. IEEE ICPE-ECCE Asia Conf., 2015, pp. 2938-2943.
[3-82] S. Mao, C. Li; W. Li; J. Popovic, J. Ferreira, “A Review of High Frequency High Voltage Generation Architecture,” in Proc. IEEE ECCE-Asia 2017, 2017, pp. 1-7.
[3-83] J. Ferreira, “Improved analytical modeling of conductive losses in magnetic components,” IEEE Transaction Power Electron., vol. 9, no. 1, pp. 127– 131, Jan. 1994.
[3-84] T. Guillod, R. Färber, F. Krismer, C. M. Franck, J. W. Kolar, “Computation and analysis of dielectric losses in MV power electronic converter insulation,” in Proc. IEEE ECCE Conf., 2016, pp. 1-8.

# Chapter 4
# Analysis of the HV transformer for the modular high frequency HV pulse converter

## 4.1 Introduction

As addressed in Chapter 3, the modular HV pulse converter architecture with modular HV transformers and modular voltage multipliers provide advantages for alleviating the requirements on the insulation, reduce electrical stress and power loss for the key components. However, the advantages and challenges of the modularization, the interconnection structure for the modular HV transformers have not been well investigated. The investigation and analysis of the HV transformer with planar and wire-wound packaging structure, as well as the HV insulation structure has not been addressed for the modular HV generator. High switching frequency operation can not only shrink the size of the HV pulse converter, especially the transformer and voltage multiplier capacitors, but also improve the HV pulse speed. However, the power loss will be increased for the HV transformer due to high conduction loss and high frequency AC dielectric loss at high switching frequency. The influence of the increased switching frequency for the HV transformer needs to be analysed. The packaging and HV insulation structure, as well as insulation stress for the HV transformer also need to be studied.

In Chapter 4, the advantages of modularization for the high frequency HV transformer are introduced firstly. Then the planar and wire-wound packaging structures, as well as the HV insulation structures of the high frequency HV transformer for the modular HV pulse converter architecture are presented. The influence of the increased switching frequency for the HV transformer is discussed. The detailed design considerations and prototype experimental results of high frequency HV transformers for the modular HV pulse converter architecture are finally given.

## 4.2 The modularization of the HV transformer

### 4.2.1 The advantage of the modularization of the HV transformer

As introduced in Chapter 3, HV pulse converter Architecture-2 shown in Fig. 4-1 with a single inverter, a single HV transformer and multiplier rectifications is widely used in low- to medium-power range with optimal power density and satisfying efficiency. The multiplier with different stage numbers provides the scalability for different output voltage rating applications. Though the insulation stress of the HV transformer in HV Architecture-2 with a multi-stage multiplier circuit is reduced compared with HV pulse converter Architecture-1 with a single inverter, a single HV transformer and single rectification, the high frequency AC dielectric loss of the HV transformer still limits the switching frequency further increase for power density improvement.

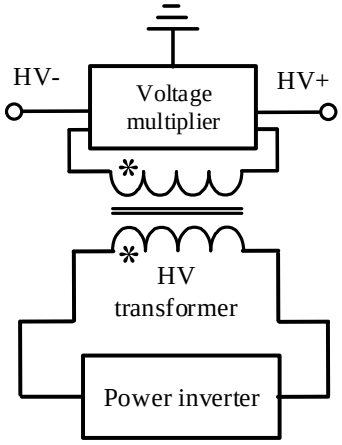



Fig. 4-1 Circuit diagram of HV pulse converter Architecture-2

The two particularities of the HV step-up transformer are large parasitic winding capacitance due to high turns ratio, as well as large number of winding turns in the secondary side, and large leakage inductance due to the required HV isolation distances between primary and secondary sides [4-1]. The equivalent circuit of the HV step-up transformer is illustrated in Fig. 4-2. $L_m$ and $L_{plk}$ are the magnetizing inductance and leakage inductance of the transformer respectively. $C_p$ is the parasitic winding capacitance reflected in the transformer's primary side. The turns ratio of the HV step-up transformer is 1:$k$. Assuming that the stage number for the dual polarity half-wave CW voltage multiplier in Fig. 4-3 is $n$, the output voltage is $V_o$, and the voltage multiplier conversion coefficient $k_{vm}$. The secondary voltage of the HV transformer $V_{tr\_s}$ is as follows:

$$V_{tr\_s} = \frac{V_o}{4nk_{vm}} \tag{4-1}$$

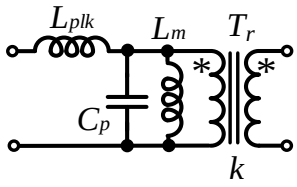



Fig. 4-2 Equivalent circuit of a HV step-up transformer

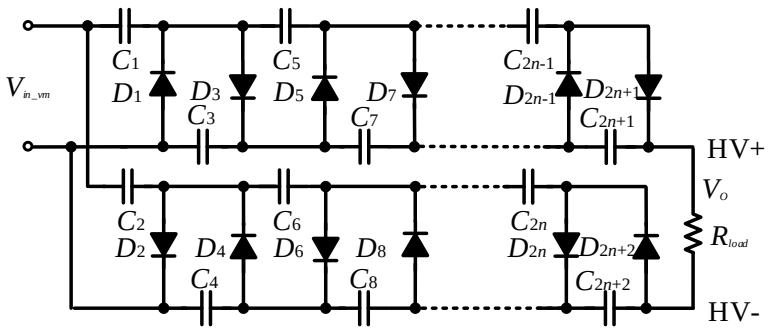
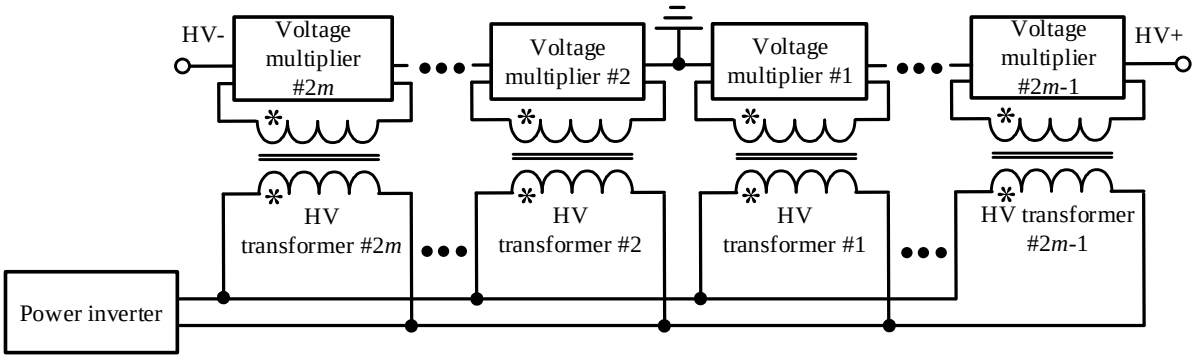


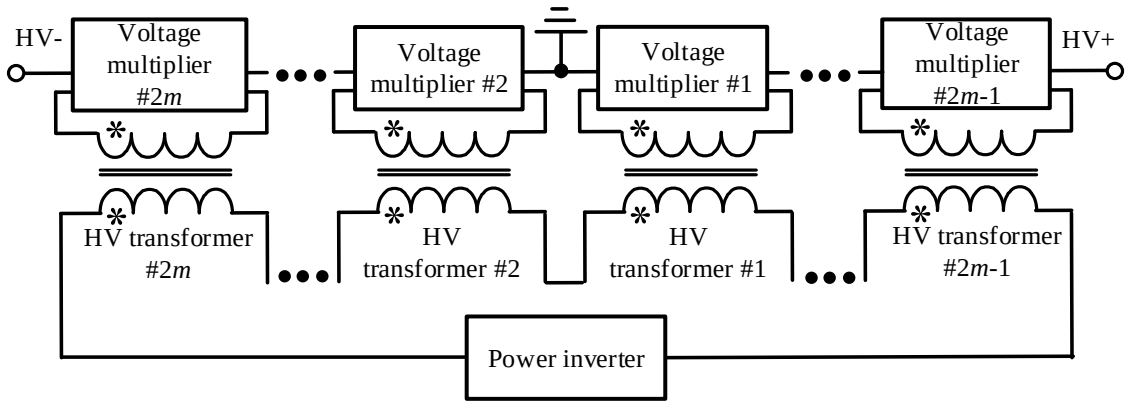

Fig. 4-3 Dual polarity half-wave CW voltage multiplier

Compared with the HV pulse converter Architecture-2, Architecture-4 with distributed HV transformers and multipliers illustrated in Fig. 4-4 can further reduce the voltage stress of the HV transformer [4-2]. The HV pulse converter is composed of 2*m* transformer modules and 2*m* voltage multiplier modules. The secondary voltage of the HV transformer $V_{Tr\_s}$ in HV Architecture-4 is 2*m* times lower than the secondary voltage of the HV transformer in HV pulse converter Architecture-2 with same stage number as for a dual polarity half-wave CW voltage multiplier. Compared with the single HV transformer architecture, the HV insulation stress will be shared by each transformer module. As a result, the HV DC and high frequency AC insulation stress for each transformer module is greatly reduced. This will enable a reduction of the high frequency AC dielectric loss for the HV transformer operating at high frequency [4-3]- [4-4].

$$V_{tr\_s} = \frac{V_o}{8mnk_{vm}} \tag{4-2}$$




(a)HV transformer primary side series interconnection structure



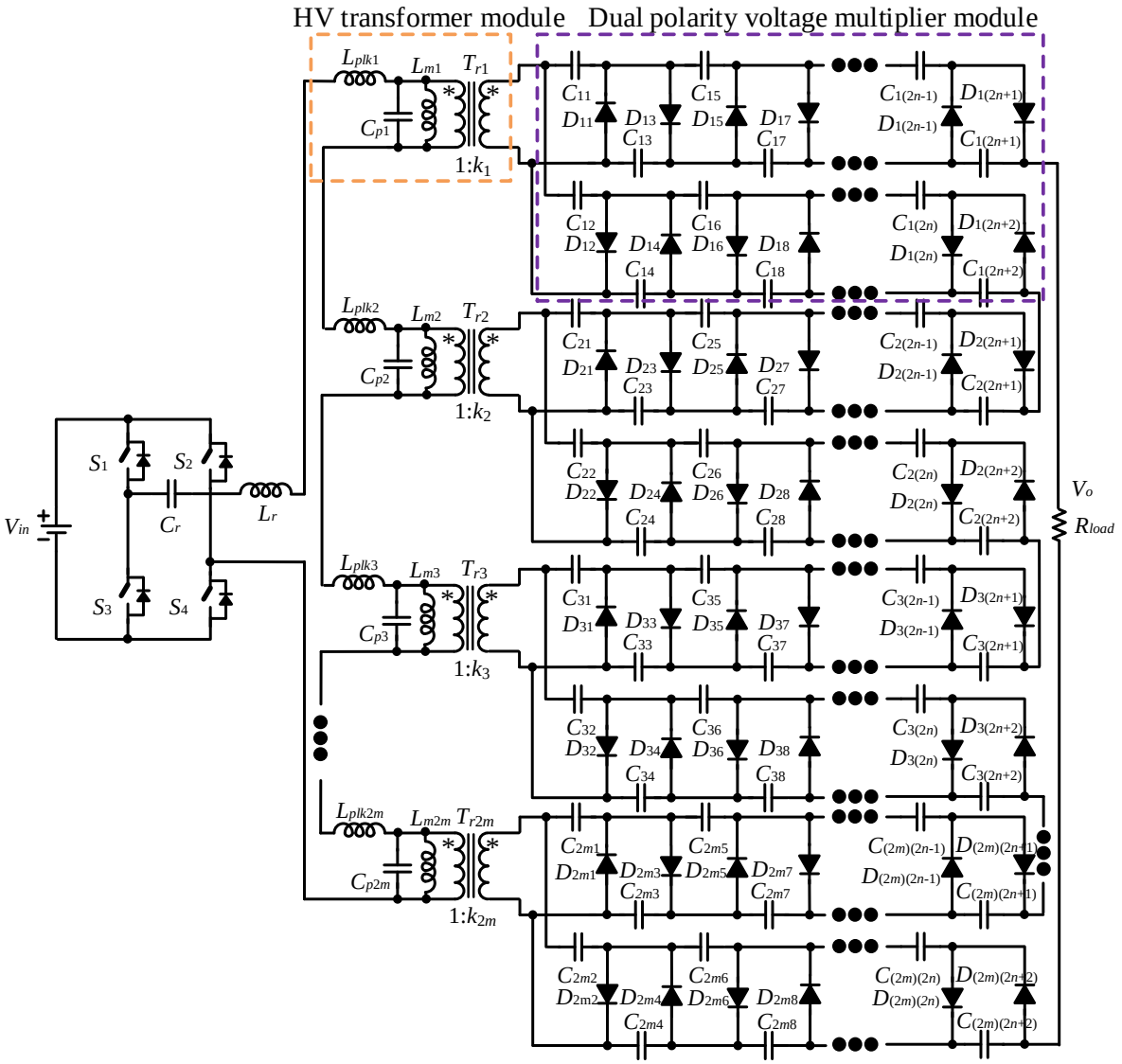

(b) HV transformer primary side parallel interconnection structure

Fig. 4-4 Circuit diagram of HV pulse converter Architecture-4

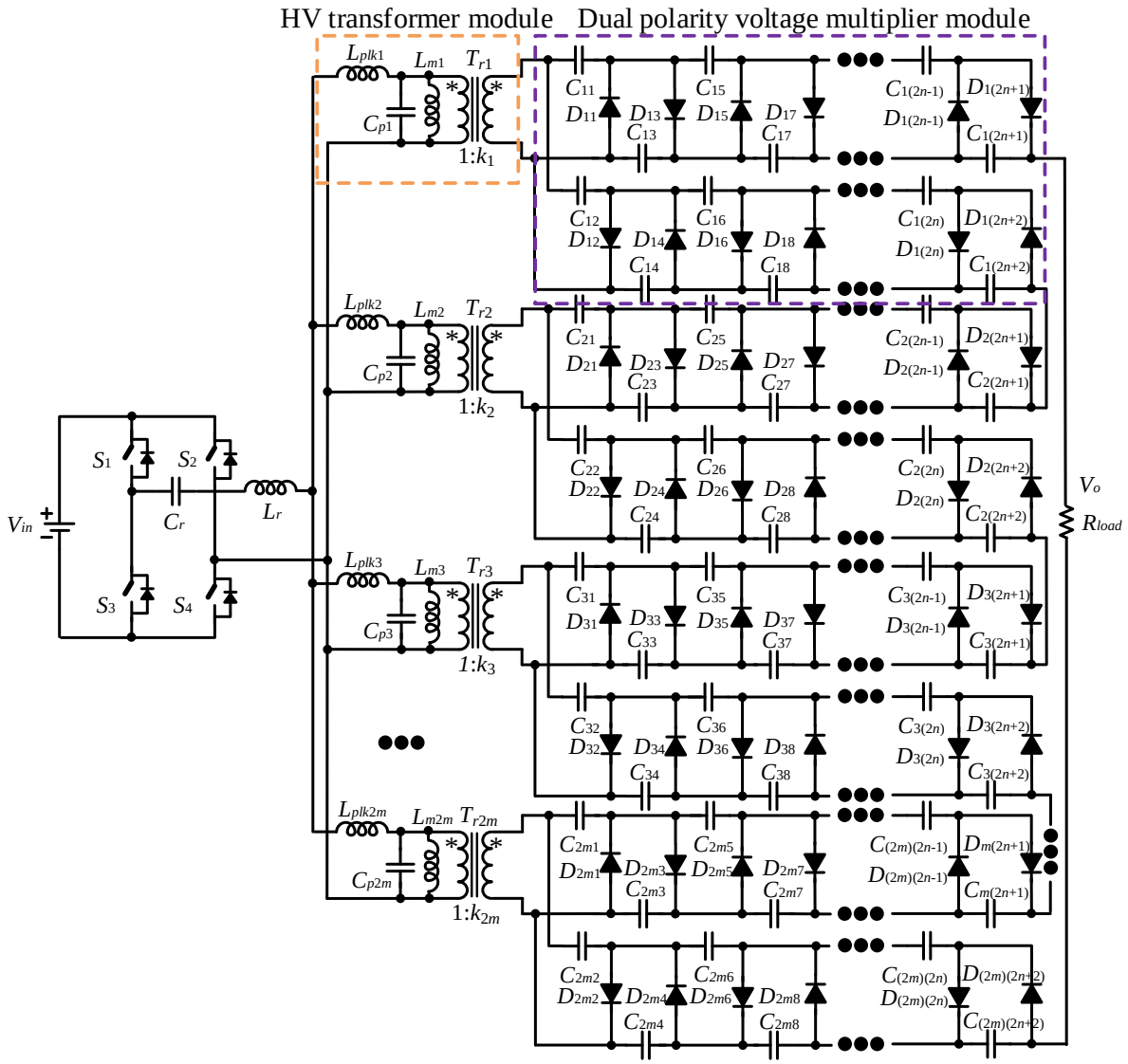
### 4.2.2 Interconnection of the modular HV transformers and the converter

The interconnection structure of the modular transformers for the HV pulse converter can be basically divided into two types: series and parallel interconnection based on the interconnection structure between the primary side of the transformer and inverter shown in

Fig. 4-5 with 2*m* elemental HV transformers and *n* stage dual polarity half-wave CW voltage multipliers. The series interconnection is suitable for higher input AC voltage, and parallel interconnection is suitable for large current applications. The outputs of the voltage multiplier circuits are connected in series to generate high output voltage.




(a) HV transformer primary side series interconnection structure




(b) HV transformer primary side parallel interconnection structure

Fig. 4-5 Circuit diagram of the modular HV pulse converter with 2*m* elemental HV transformers and *n* stage dual polarity half-wave CW voltage multipliers based on Architecture-4

*A. HV transformer primary side series interconnection structure*

The key features of the HV transformer primary side series interconnection structure are:

1) Since the transformer primary winding of each module is connected in series, the primary currents for all HV transformer modules are identical. Good static and dynamic current sharing for both the HV transformer primary and secondary winding can be achieved if the HV transformer winding parasitic capacitance and voltage multiplier capacitance are identical.
2) The total transformer parasitic capacitance reflected in the primary side is reduced 2*m* times compared with the parasitic capacitance of the elementary transformer due to the series interconnections. The reactive power of the converter can be also reduced.

3) The input voltage is shared by the HV transformer modules. The voltage sharing depends on the parameters' uniformity of primary winding magnetizing inductance, winding parasitic capacitance and voltage multiplier. The output voltage sharing is affected by input voltage sharing, transformer turns ratio and voltage multiplier.
4) The leakage inductors of elemental HV transformers are connected in series. The inductance of the external series resonant inductor can be greatly reduced, or even eliminated by only using the leakage inductor of the HV transformer for the resonant tank.
5) Easy assembly and manufacturing can be achieved since the HV transformer modules share the same primary winding and insulation between the primary to core and secondary winding. The surface of the soldering points for elemental HV transformers interconnection can be reduced.
6) Compared with the centralized HV transformer, the power rating for the elemental HV transformer is reduced *m* times and the thermal stress can also be reduced.
7) Though modular transformers are used, the required turns ratio for the elemental HV transformer is the same as with a centralized HV transformer with the same stage number of HV multiplier due to the series interconnection of transformer primary windings with the converter.

*B. HV transformer primary side parallel interconnection structure*

The main characteristics of this type of interconnection are listed below:

1) The input voltage sharing of the elementary HV transformer can be achieved naturally due to the parallel interconnection.
2) The input current sharing depends on the impedance of the elemental HV transformer and voltage multiplier.
3) The output voltage sharing depends on the input voltage sharing, turns ratio, and voltage multiplier.
4) The required turns ratio for the elemental HV transformer will be 2*m* times lower than the centralized HV transformer with the same stage number of voltage multiplier.
5) The total transformer parasitic capacitance reflected in the primary side is increased several times compared with the parasitic capacitance of the elementary transformer due to the parallel interconnection. The reactive power of the converter can be also increased.

### 4.2.3 Equivalent circuit

The equivalent circuit diagram can help better understand the characteristics of the modular HV pulse converter architectures with HV transformer primary side series and parallel interconnection structures and provide a tool for the analysis and design of the transformer. The dual polarity half-wave CW voltage multiplier circuit and the load in Fig. 4-3 can be modelled as an equivalent circuit with a RC parallel connection as shown in Fig. 4-6 [4-5]-[4-7].

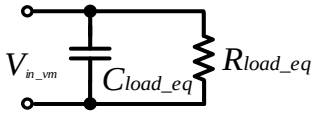
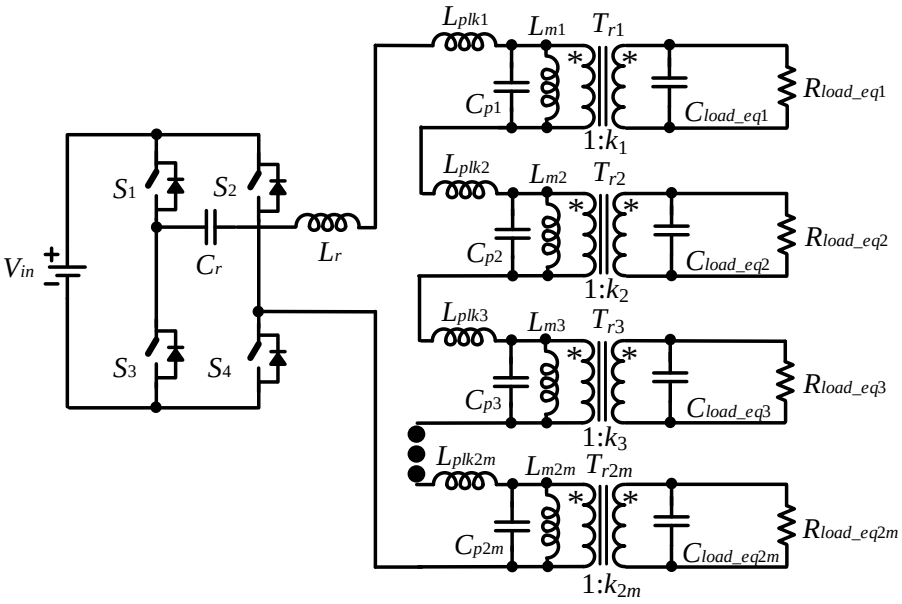
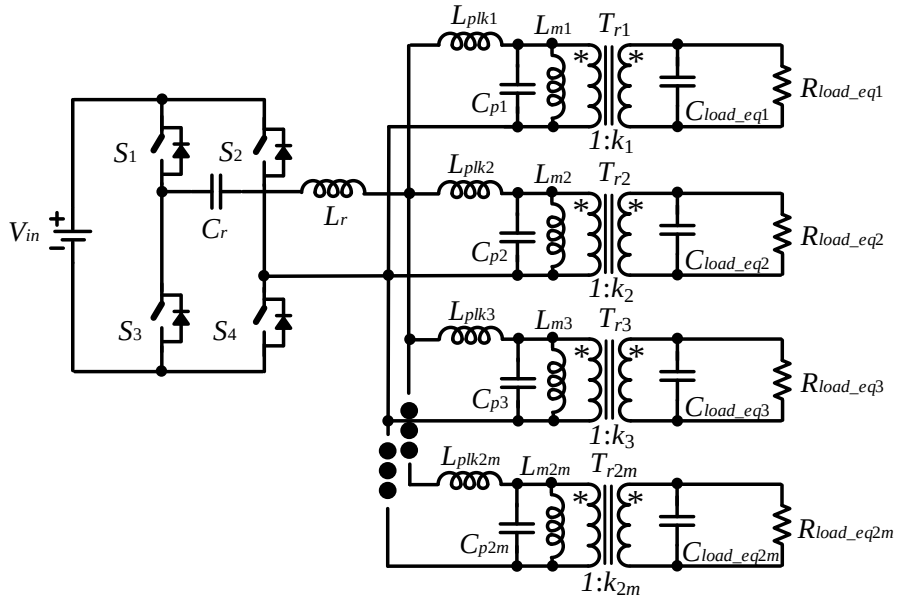



Fig. 4-6 Equivalent circuit for dual polarity half-wave CW voltage multiplier circuit

Assuming the voltage and power for each elementary transformer and voltage multiplier circuit are all the same, the equivalent circuit diagrams of the modular HV pulse converter architecture with HV transformer primary side series and parallel interconnection structures are illustrated in Fig. 4-7 (a) and (b) respectively, based on the equivalent circuit for a dual polarity half-wave CW voltage multiplier circuit.



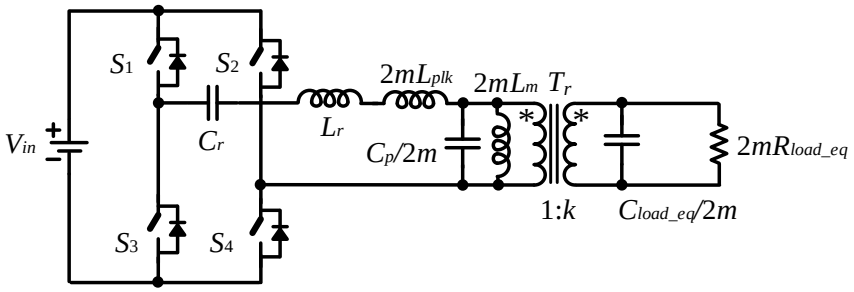

(a) HV transformer primary side series interconnection structure



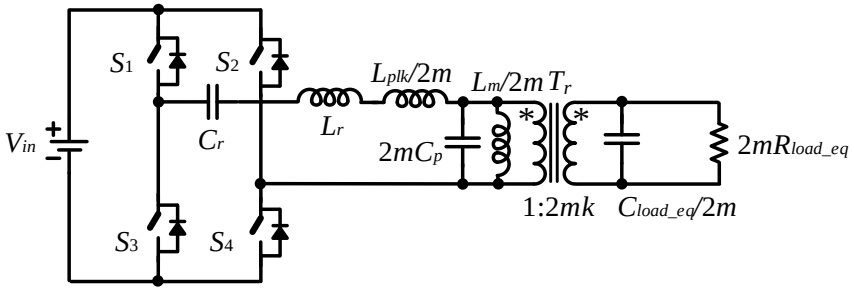
(b) HV transformer primary side parallel interconnection structure

Fig. 4-7 Circuit diagram of the modular HV pulse converter architecture by using an equivalent circuit for the multiplier

It is assumed that all the parameters for the elementary transformer and the equivalent capacitor and resistor for the voltage multiplier and load are all the same. Then the equivalent circuit diagram of the modular HV pulse converter architecture can be derived in Fig. 4-8.




(a) HV transformer primary side series interconnection structure




(b) HV transformer primary side parallel interconnection structure

Fig. 4-8 Equivalent circuit diagram of the modular HV pulse converter architecture

Based on the equivalent circuit for the modular HV pulse converter architecture with the HV transformer primary side series and parallel interconnection structure, some implications follow:

1) Regarding the modular HV pulse converter architecture with the HV transformer primary side series and parallel interconnection structure, the leakage and magnetizing inductances will be increased 2*m* times. The increased leakage inductance provides the possibility for reducing or eliminating the resonant inductor. The parasitic capacitor of the HV transformer reflected in the primary side and the equivalent capacitor of the voltage multiplier and load will be decreased 2*m* times. Lower parasitic capacitor and equivalent capacitor of the voltage multiplier and load will help to reduce the reactive power of the HV pulse converter, increasing the circuit efficiency. The turns ratio of the equivalent circuit remains the same as the turns ratio of the elementary HV transformer. The equivalent resistor of voltage multiplier and load will be increased by *m* times for the equivalent circuit.

2) For the modular HV pulse converter architecture with the HV transformer primary side series and secondary parallel interconnection structure, the leakage and magnetizing inductances will be decreased $2m$ times. However, the parasitic capacitor of the HV transformer reflected in the primary side will be increased $m$ times. This adds the challenges of higher reactive power and larger power loss for the HV pulse converter circuit. The turns ratio of the equivalent circuit will be increased $2m$ times compared with the turns ratio of the elementary HV transformer. It provides the advantage of a reduction of the HV transformer turns ratio or the stage number of voltage multiplier circuits.

Table 4-1 Summary of the key parameters of the equivalent circuit for the modular HV pulse converter architecture with the HV transformer primary side series and parallel interconnection structure

| Key parameters | HV transformer primary side series interconnection structure | HV transformer primary side parallel interconnection structure |
|---|---|---|
| Turns ratio | $1:k$ | $1:2mk$ |
| Leakage inductance | $2mL_{plk}$ | $L_{plk}/2m$ |
| Magnetizing inductance | $2mL_m$ | $L_m/2m$ |
| Parasitic capacitor of the HV transformer reflected in the primary side | $C_p/2m$ | $2mC_p$ |
| Equivalent capacitor of the voltage multiplier and load | $C_{load\_eq}/2m$ | $C_{load\_eq}/2m$ |
| Equivalent resistor of the voltage multiplier and load | $2mR_{load\_eq}$ | $2mR_{load\_eq}$ |

In summary, the modularization of the HV transformer provides the following advantages:

a) Insulation stress reduction for HV transformer modules
b) Dielectric loss reduction for HV transformer modules
c) Size reduction of HV transformer modules due to low insulation stress
d) Distributed thermal stress on HV transformer modules
e) Reduction of parasitic capacitance, low reactive power for the inverter (elaborated in the following session-equivalent circuit diagram of the modular HV transformers for HV generation architecture)
f) Higher operation switching frequency to reduce the size of the magnetic and multiplier capacitor without sacrificing the efficiency
g) Multiplier stage number reduction with lower diode loss, less HV capacitor, faster HV pulse or HV transformer turns ratio reduction with the decrease of parasitic capacitance.
h) Possibility of an optimal system trade-off with scalability on the numbers of HV transformers and a stage number of voltage multiplier to achieve superior performance in a multi-dimensional criteria space such as high power density, high efficiency, and good HV pulse quality, amongst others when the output voltage rating is high and the power rating is medium to large.

i) Modular, easy to scale to different HV pulse converter rating with low rating HV transformer and multiplier modules.
j) Easy assembly and manufacturing of the HV transformer modules compared with centralized HV transformer structure.

### 4.2.4 Challenges of the modularization of the HV transformer

Besides the advantages from the modularization of the HV transformer such as parasitic capacitance reduction, suitability for high frequency operation, high frequency AC dielectric loss and primary reactive power reduction, the following are few challenges for modularization of the HV transformer.

1) The variance of HV transformer parasitics including magnetizing inductance, leakage inductance, winding capacitance due to the magnetic core characteristics difference and inconsistent assembly and manufacture process will lead to the voltage and current sharing challenges for modular HV pulse converter architectures. However, the variance can be well controlled if the transformer is realised in the manufacturing technology with high repeatability and precision of parasitics, such as PCB construction. Furthermore, the variance of the multiplier capacitor and the parasitic capacitance and the parasitic inductance of the HV multi-stage multiplier circuits will also impact on the voltage and current sharing for modular HV pulse converter architectures.

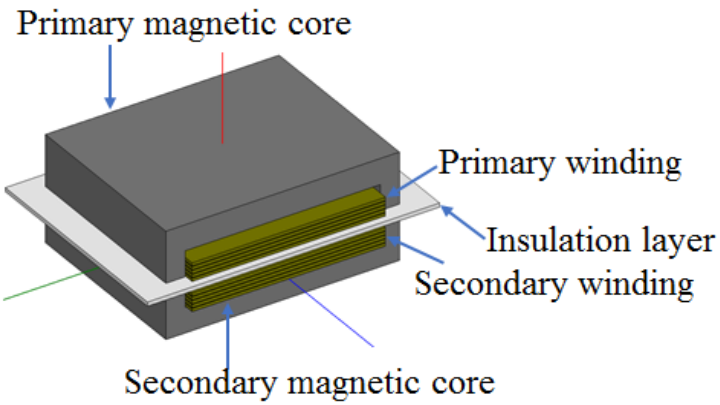
2) The modularization level (or the number of elemental HV transformer) does not follow that more is better. When the number of HV transformer modules increase, the magnetic core loss may get large and the size and cost of HV pulse converter may also be increased.

3) While the high frequency AC insulation stress for the elemental HV transformer is the same, the HV DC insulation stresses are different for the elemental HV transformer. The insulation design for the elemental HV transformer should consider the largest HV DC insulation stress if uniform insulation and packaging design is used for each elemental HV transformer.

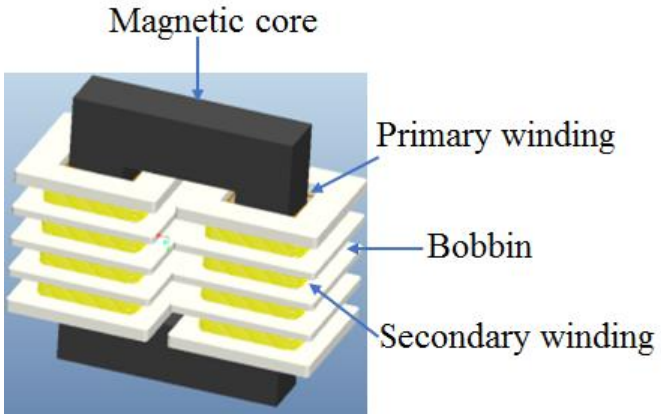
## 4.3 Packaging and insulation of HV transformer

### 4.3.1 Planar HV transformer

According to the shape of the HV transformer, it can be divided into planar and conventional wire-wound types. The planar HV transformer structure is illustrated in Fig. 4-9(a) and the wire-wound HV transformer structure is in Fig. 4-9(b). In recent years, with the rapid development of PCB technology, the low-profile planar magnetics have been widely used in both academia and industry to achieve better integration and planarization [4-8]- [4-12].




(a) Planar structure




(b)Wire-wound structure

Fig. 4-9 HV transformer structure

The planar structure transformer is generally composed of a low-profile planar magnetic core and planar windings with multilayer PCB or laminating copper layers. Planar high insulation capability materials such as polypropylene can be used to achieve the required isolation between the transformer's primary and secondary sides. The height of the planar transformer is much lower than the conventional wire-wound structure.

The major advantages for planar transformers are summarized as follows [4-8]- [4-12]:

1. Low package profile—the height of a planar transformer is shorter than the height of the conventional wire-wound type. It is generally constructed by multi-layer PCB, or copper foil. The flat or planar ferrite core can be used together with planar PCB or copper foil to achieve the low profiles.
2. Good repeatability—the planar transformer can be fabricated, with high repeatability, by automatic assembly process.
3. Ease of manufacturability—the PCB winding techniques are easily adapted for mass production.
4. Predictable parasitics—the windings manufactured automatically by PCB machines are precise and consistent. The transformer parasitic parameter is controllable and predictable.

5. Ease of system integration and planarization—the planar transformer with PCB winding is easily interconnected with other components by PCB. The PCB not only performs the basic purpose of winding layout, but also provides the electrical interconnection between transformer and other components. Furthermore, the planar construction lends itself well to high density integration, such as shown in the planar electromagnetic integration with high dielectric substrate materials [4-11].

There are some limitations for the planar transformer. They are summarized as follows [4-12]:

1. Large footprint area—the large surface area of planar magnetics increases the footprint area though planar magnetic cores with higher surface area to volume ratio than conventional magnetic cores are more efficient in conducting heat and lead to lower temperature rises compared with a conventional wire-wound type transformer.
2. Large parasitic winding capacitance—PCB windings with intrinsically larger surface areas leads to parasitic winding capacitance increase when compared to conventional wire-windings.
3. Low window utilization factor—a PCB is used to implement the planar windings, the window utilization factor is low compared with the conventional wire-wound type transformer due to inter-turn spacing and a required dielectric thickness based on the capabilities of PCB fabrication and dielectric materials.

Besides the aforementioned advantages and limitations of the planar transformer, there are some particularities when the planar transformer is used for HV applications [4-9].

1. Planar insulation structure—the planar shape of the HV transformer with the planar solid insulation layer such as FR4 epoxy and polypropylene, which can provide high insulation capability above 30 kV/mm, make the assembly and packaging easy.
2. HV bobbin elimination—the HV bobbin for windings is not required since the winding can be embedded into the PCB and FR4 epoxy can provide the essential insulation between layers. The planar solid insulation layer realizes the insulation between the transformer's primary and secondary winding.
3. Sharp edges of the outer PCB winding—the PCB HV winding suffers a high electric field due to the sharp edges of the outer PCB winding. The electric field of the PCB winding is larger than the round wire.
4. Limited number of turns for windings—with a given window area of magnetic core, the number of turns is limited since it requires many layers which will not only add to the cost of multilayer PCB lamination manufacturing, but also adds challenges for interconnection of the multilayer PCB lamination and heat dissipation of internal layers of the PCB windings. This is an important limitation for HV transformers with high numbers of turns for secondary winding.
5. High frequency dielectric loss for PCB winding—the dielectric loss for the multi-layer PCB windings will contribute significant loss to the total HV transformer winding losses when the HV transformer operates at high switching frequency [4-22]- [4-23].

6. Heat dissipation—due to the high frequency dielectric loss for the transformer secondary winding, the heat dissipation of the internal layer of the multi-layer PCB windings of the planar HV transformer needs to be considered.

Fig. 4-10 gives a possible packaging structure of a modular HV tank with planar HV transformers. The interconnection between the HV transformer and voltage multiplier can be achieved by the PCB. The assembly and packaging of the HV tank is based on PCB technologies. This will enable high density integration and planarization. The shape of this planar packaging structure is very flat. It can be scalable to high output voltage and power rating with more elementary HV transformers and HV multipliers.

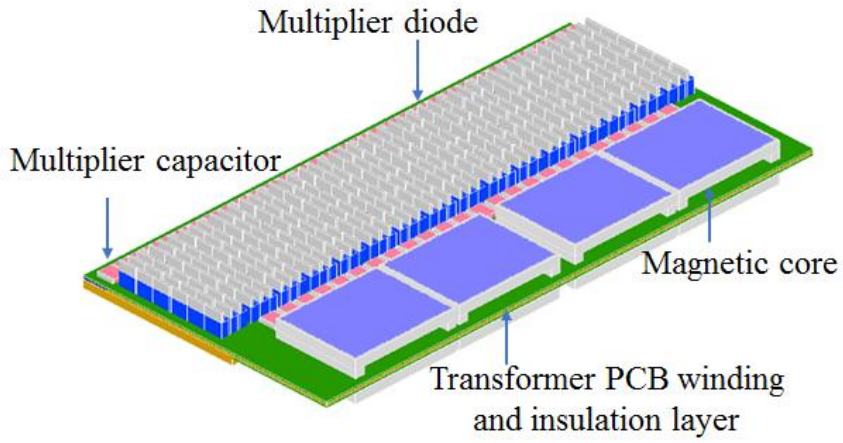
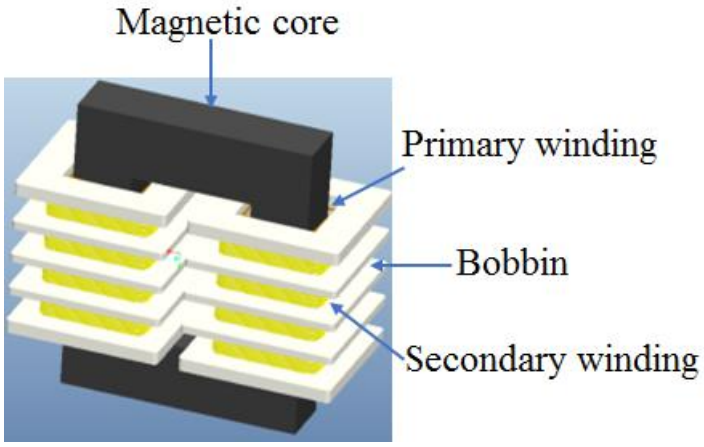


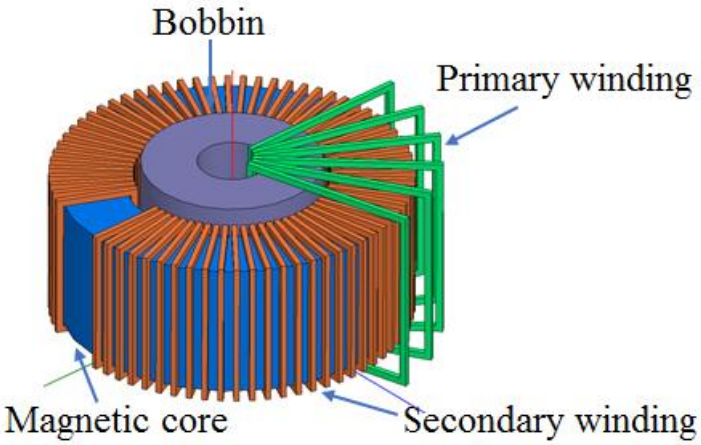

Fig. 4-10 Packaging structure of the modular HV tank with planar HV transformers

### 4.3.2 Wire-wound HV transformer structure

The wire-wound HV transformer structure in Fig. 4-11 is widely used in the HV pulse converter [4-13]- [4-14]. The E shape, U shape, as well as toroid shape cores are normally adopted for a wire-wound HV transformer. The primary winding and secondary winding based on round wire is wound in the magnetic core. The HV bobbin is used to provide the HV isolation between the core and winding and between the primary winding and secondary winding. The multi-slot HV bobbin is typically used for the E shape and U shape magnetic core to reduce the parasitic capacitance of the HV transformer's secondary winding.



(a) U shape core based HV transformer




(b) Toroid shape core based HV transformer

Fig. 4-11 Wire-wound HV transformer structure

Fig. 4-12 shows the packaging structure of the modular HV tank with a wire-wound HV transformer based on a toroid shape core. Multiple elementary HV transformers are stacked together to share the same primary winding and tubing shape plastic insulation between the primary winding to core and secondary windings. The secondary windings of HV transformers are connected to the PCB with surface mounted HV diodes and capacitors. The electrical interconnections of the elementary HV tank with the elementary HV transformer and HV multiplier are also implemented by the PCB. This packaging structure is modular and scalable to higher output voltage and power rating with more elementary HV transformers and HV multipliers.

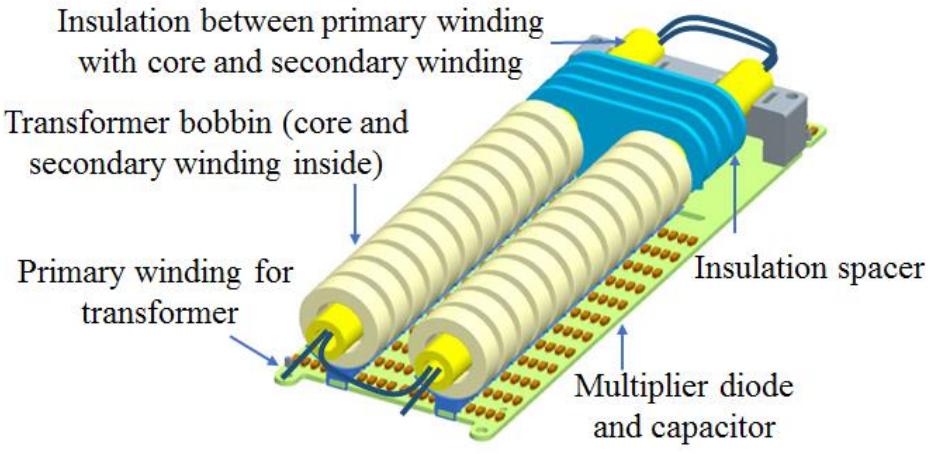



Fig. 4-12 Packaging structure of a modular HV tank with wire-wound HV transformer

An integrated packaging structure of the modular HV tank with wire-wound HV transformer based on toroid shape core is illustrated in Fig. 4-13. The exploded view of the integrated

packaging structure of the elementary HV wire-wound transformer and HV multiplier is given in Fig. 4-14.

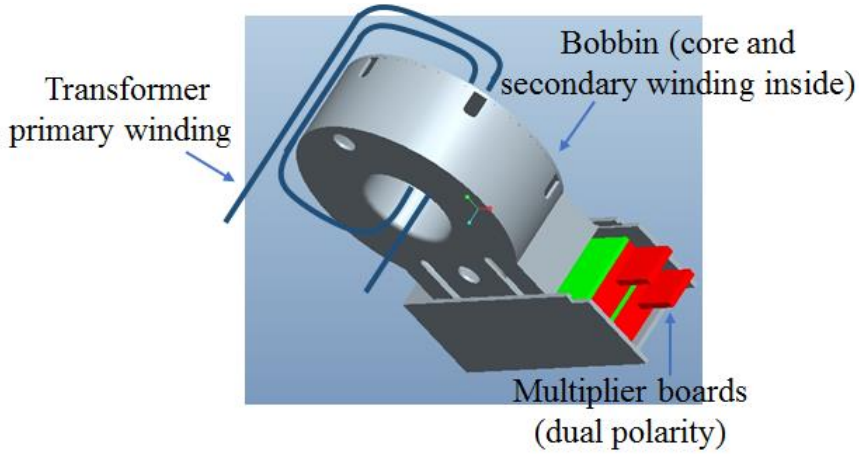



Fig. 4-13 Integrated packaging structure of the elementary HV wire-wound transformer and HV multiplier

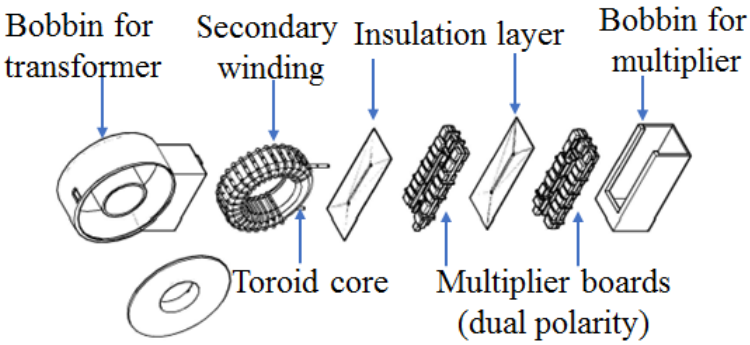



Fig. 4-14 Exploded view of the integrated packaging structure of elementary HV wire-wound transformer and HV multiplier

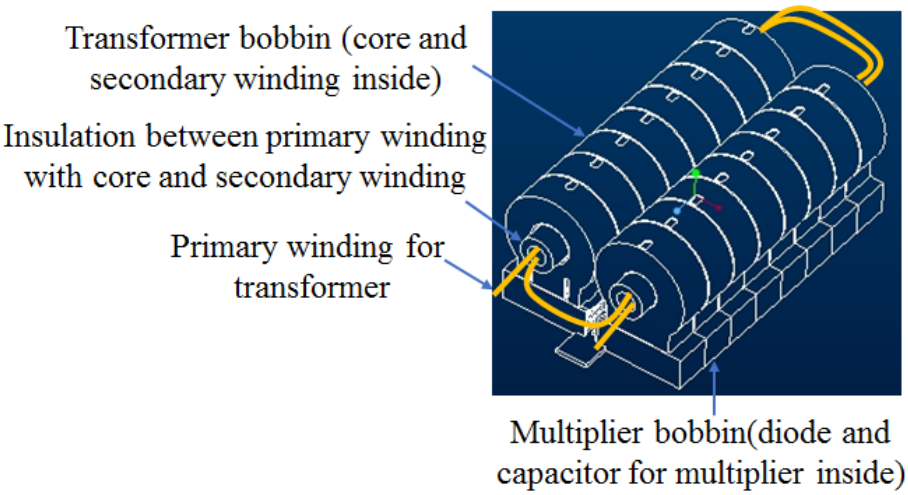


Fig. 4-15 Integrated packaging structure of the modular HV tank with HV wire-wound transformer

Different to the packaging structure in Fig. 4-12, the HV multiplier circuit boards of the each elementary HV tank are integrated together with the elementary HV transformer. The elementary HV multiplier circuit boards and the HV transformer share the same HV bobbins. This integrated modular packaging structure in Fig. 4-15 provides more flexibility of high output voltage and power packaging structure. The integrated packaging structure is more distributed, and easy for assembly and manufacture.

### 4.3.3 Insulation stress analysis of the HV transformer for the modular HV pulse converter

*A. DC and AC insulation stress analysis of the HV transformer for the modular HV pulse converter*

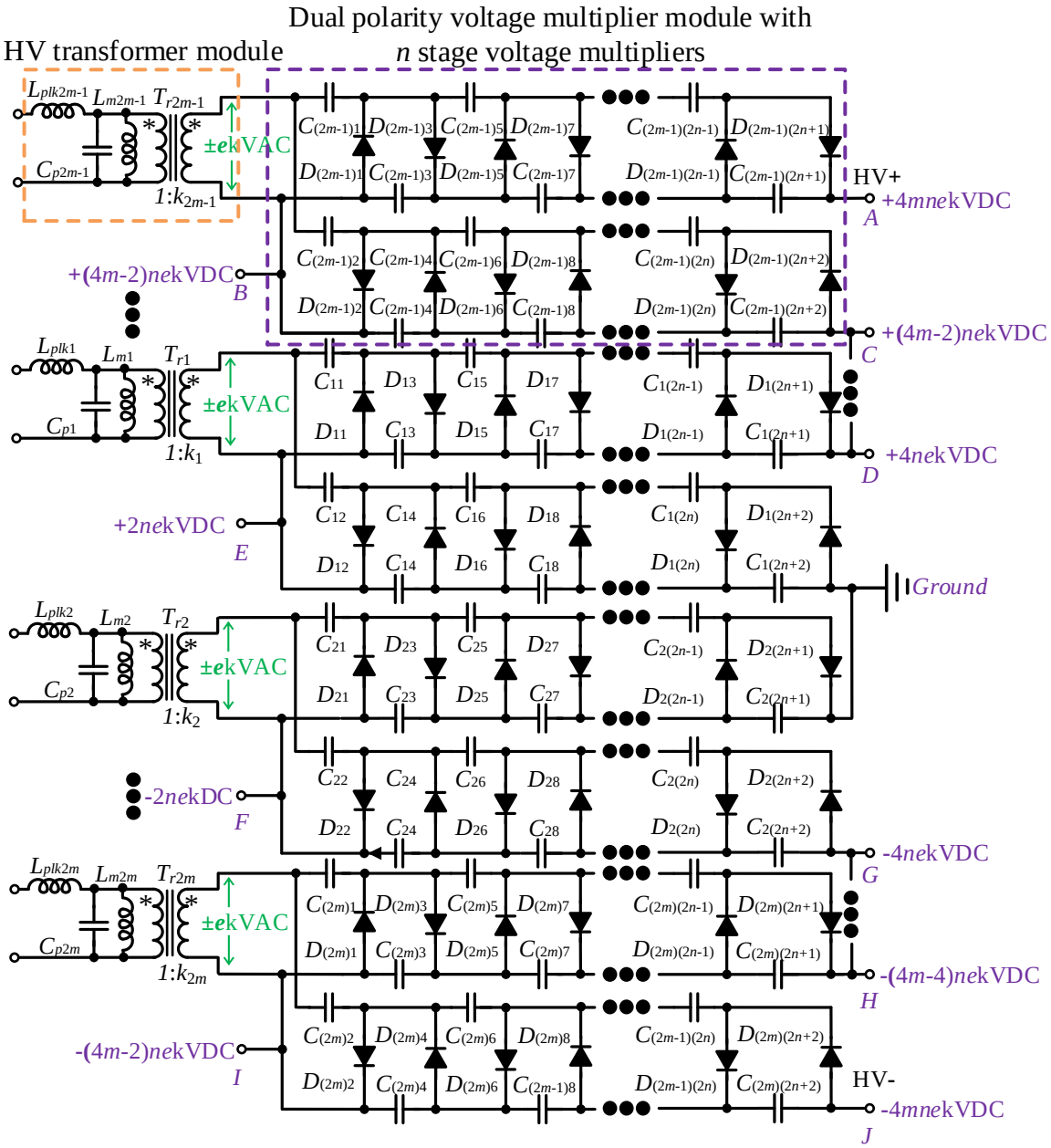


Fig. 4-16 Circuit diagram of the modular HV pulse converter with 2*m* elemental HV transformers and *n* stage dual polarity half-wave CW voltage multipliers

To simplify the insulation stress analysis, the following are some assumptions:

(a) The voltage drop across the voltage multiplier is neglected.
(b) The voltage ripple of each stage of the voltage multiplier is neglected.
(c) The output voltage of the positive and negative voltage multiplier is symmetrical.
(d) The output voltage and power for the each elementary HV tank are all the same.

For the modular HV pulse converter with 2*m* elemental HV transformers and *n* stage dual polarity half-wave CW voltage multipliers shown in Fig. 4-16, assume the peak AC voltage of elemental HV transformer secondary winding is

$$V_{tr\_s\_pk} = \pm e\text{kV} \tag{4-3}$$

This is also the AC insulation stress for the elemental HV transformer.

$$V_{tr\_AC-insulation} = V_{tr\_s\_pk} = \pm 2ne\text{kV} \tag{4-4}$$

Then the output voltage for the each elemental HV tank is

$$V_{HV-\text{tank\_elementary}} = 4ne\text{kV} \tag{4-5}$$

The total positive and negative polarity HV tank output voltage with 2*m* elemental HV transformers and *n* stage dual polarity half-wave CW voltage multipliers can be expressed as

$$V_{HV-\text{tank\_positive\_total}} = 4mne\text{kV} \tag{4-6}$$

$$V_{HV-\text{tank\_negtive\_total}} = -4mne\text{kV} \tag{4-7}$$

The total HV output is the sum of the positive and negative polarity HV tank output voltage is given by the following:

$$V_{HV-\text{tank\_negtive\_total}} = 8mne\text{kV} \tag{4-8}$$

The DC insulation stress of the elemental HV transformer $T_{r1}$ and $T_{r2}$ can be expressed as:

$$V_{tr1\_DC-insulation} = +2ne\text{kV} \tag{4-9}$$

$$V_{tr2\_DC-insulation} = -2ne\text{kV} \tag{4-10}$$

The DC insulation stress of the elemental HV transformer $T_{r2m\text{-}1}$ and $T_{r2m}$ can be derived as follows:

$$V_{tr2m-1\_DC-insulation} = +(4m-2)ne\text{kV} \tag{4-11}$$

$$V_{tr2m\_DC-insulation} = -(4m\text{-}2)ne\text{kV} \quad (4\text{-}12)$$

The total insulation stress of the elemental HV transformer $T_{r2m\text{-}1}$ and $T_{r2m}$ is the sum of the DC and AC insulation stress. It can be derived as follows:

$$V_{tr2m-1\_insulation} = V_{tr2m-1\_DC-insulation} + V_{tr2m-1\_AC-insulation} = (4m-2\pm1)ne\text{kV} \quad (4\text{-}13)$$

$$V_{tr2m\_insulation} = V_{tr2m\_DC-insulation} + V_{tr2m\_AC-insulation} = -(4m-2\pm1)ne\text{kV} \quad (4\text{-}14)$$

From the insulation stress analysis results for the modular HV pulse converter, the DC insulation stress for the elementary HV transformer is different though the high frequency AC insulation stress for the elementary HV transformer is uniform. As a result, the insulation design for different elementary HV transformers is different. If a uniform insulation design for different elementary HV transformers is adopted, the insulation design of HV transformers needs to meet the highest insulation stress of elementary HV transformers.

*B. Insulation stress for elementary planar HV transformer*

The electric field analysis for the elementary planar HV transformer is performed by Maxwell finite element analysis. The key parameters of the planar HV transformer are summarized in Table 4-2. The prototype photo and exploded view of the planar HV transformer are shown in Fig. 4-17 and Fig. 4-18 respectively. From the electric field simulation result of the elementary HV planar transformer in Fig. 4-19, the maximum electric field strength between the secondary winding and the ferrite core is around 10.4kV/mm. The insulation between the HV transformer secondary winding and the ferrite core needs to be considered.

Table 4-2 Summary of the key parameters of the planar HV transformer

| | |
|---|---|
| Core | Planar ER64 core, ferrite 3F3 material from Ferroxcube, floating |
| Insulation layer | 1.0mm polypropylene |
| Primary winding | 7 turns, 6 layer PCB, total thickness: 4.9mm, Fr4 layer thickness:0.8mm, copper layer thickness: 4 OZ, copper width: 5mm, trace space:2mm |
| Secondary winding | 68 turns, 6 layer PCB, total thickness: 4.9mm, Fr4 layer thickness:0.8mm, copper layer thickness: 4 OZ, copper width: 0.3mm; trace space:0.3mm |
| Output voltage | 6.8kVAC peak voltage |

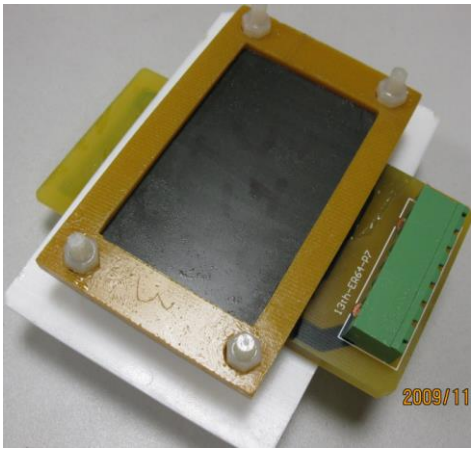



Fig. 4-17 Prototype photo of the elementary HV planar transformer

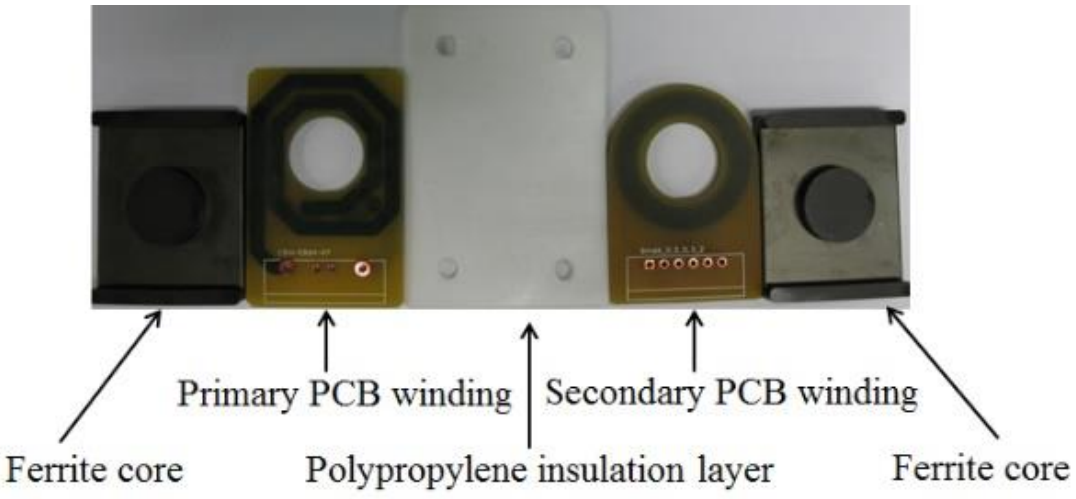



Fig. 4-18 Exploded view of the elementary HV planar transformer

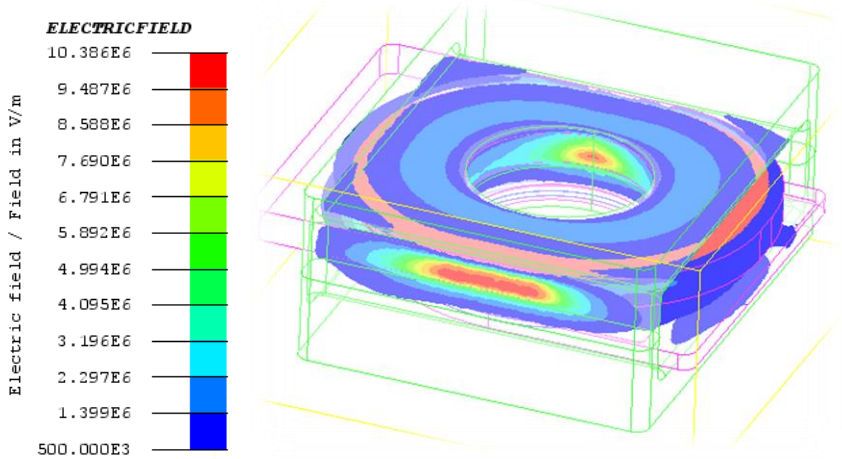



Fig. 4-19 Electric field simulation result of the elementary HV planar transformer

*C. Insulation stress for the elementary HV wire-wound transformer*

The insulation stress for the elementary HV wire-wound transformer with a toroid core structure is performed by Maxwell finite element analysis. The key parameters of the HV wire-

wound transformer with wire wounded toroid core structure is summarized in Table 4-3. The prototype photo and layout of the HV wire-wound transformer with wire wound toroid core structure are shown in Fig. 4-20 and Fig. 4-21 respectively. Fig. 4-22 gives the electric field simulation result of the elementary HV wire wound transformer with wire wound toroid core structure. The maximum electric field strength is about 13.1kV/mm and occurs between the HV transformer's secondary winding and the ferrite core in Fig. 4-21. The insulation between the HV transformer's secondary winding and the ferrite core is guaranteed by the coating layer of ferrite core and insulation layer of litz wire.

Table 4-3 Summary of the key parameters of the HV wire-wound transformer

| | |
|---|---|
| Core | R41.8×26.2×12.5, toroid N87 ferrite material from EPCOS, exoxy coating, floating |
| Insulation layer | 7.0mm polypropylene between primary and secondary windin and core |
| Primary winding | 7 turns, 14 AWG 5X5X42/44, NEW ENGLAND litz wire |
| Secondary winding | 79 turns, 24 AWG 3/35/44, NEW ENGLAND litz wire |
| Output voltage | 6.8kVAC peak voltage |

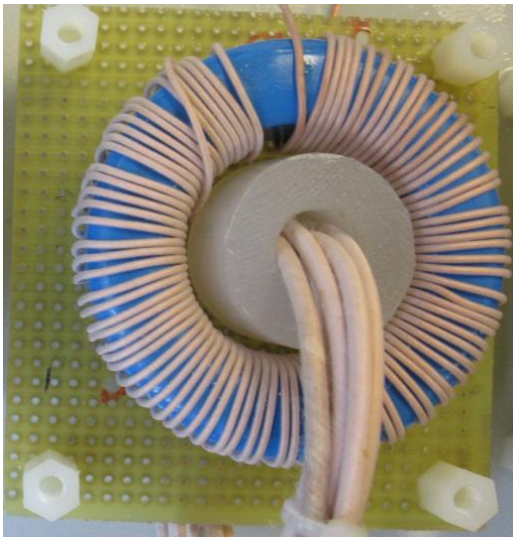


Fig. 4-20 Prototype photo of the elementary HV wire-wound transformer

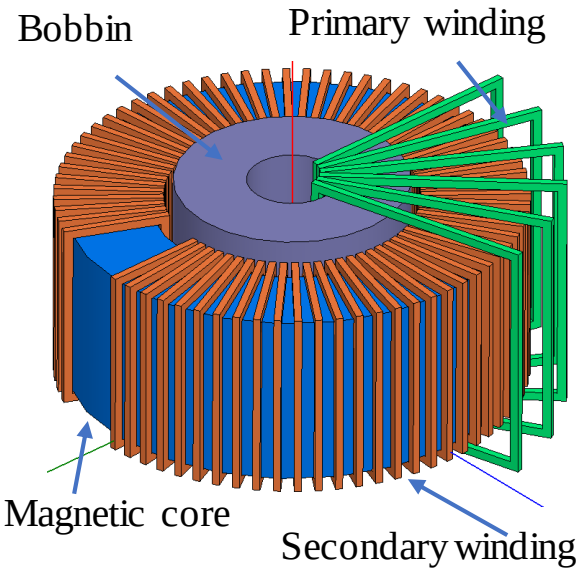



Fig. 4-21 Layout of the elementary HV wire-wound transformer

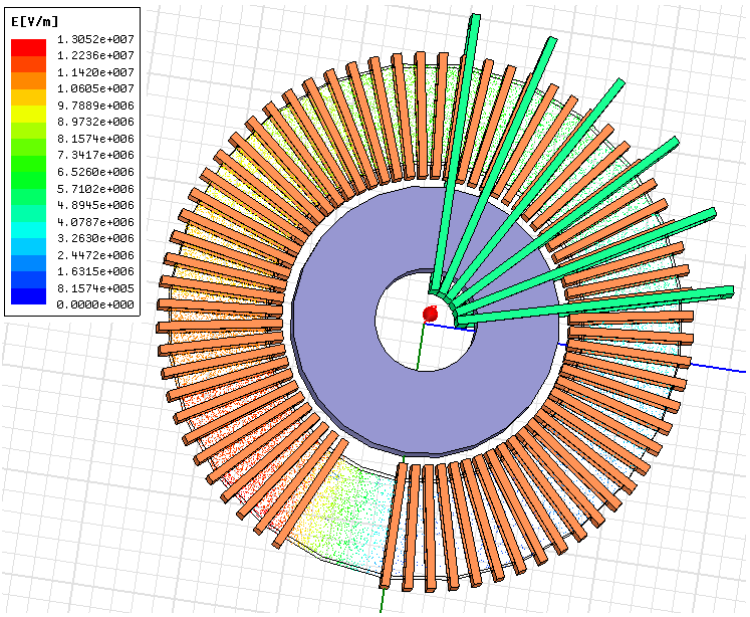



Fig. 4-22 Electric field simulation result of the elementary HV wire-wound transformer

*D. Voltage distribution and insulation stress of the HV planar transformer for modular HV pulse converter*

Different structure options are investigated for the voltage distribution and insulation stress of the modular HV pulse converter with the HV planar transformer. There are some assumptions to simplify the analysis.

(a) The output peak voltage of the HV planar transformer is limited to 10kVAC.
(b) Two stage dual polarity half-wave CW voltage multipliers are used for the analysis.
(c) The voltage drop across the voltage multiplier is neglected.
(d) The voltage ripple of each stage of the voltage multiplier is neglected.

(e) The output voltage of the positive and negative voltage multiplier is symmetrical.
(f) The output voltage and power for the each elementary HV tank are all the same.
(g) The electrical potential of the planar ER ferrite core is the same as the corresponding PCB winding wound on the planar ER ferrite core.

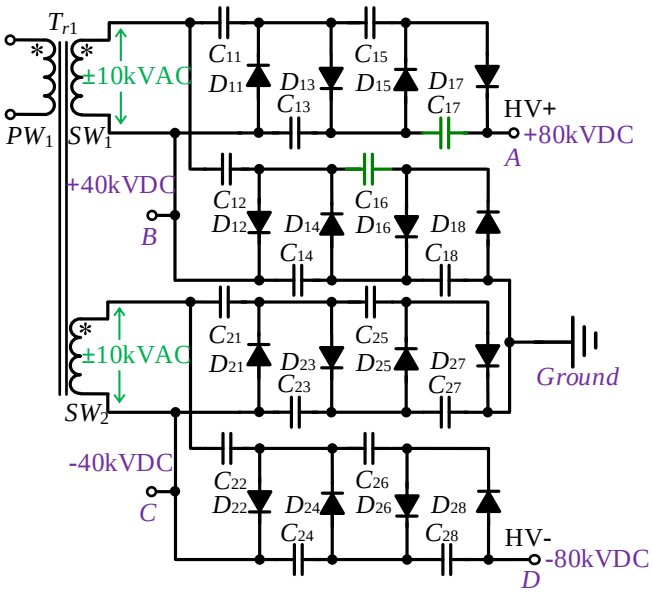
There are five structure options for the modular HV pulse converter with HV planar transformers to generate the positive and negative 80kVDC output. The circuit diagram, simplified circuit diagram and voltage distribution of the planar HV transformer for different structure options are illustrated in Fig. 4-23 to Fig. 4-27.

It's a single HV transformer with one primary winding and wo secondary windings for structure option-1. The AC insulation stress of the secondary winding is 10kVAC, and the DC insulation stress of secondary winding is 40kVDC. Based on the insulation stress analysis, a 1.5mm polypropylene insulation layer with 40kVDC insulation capability is required to achieve the insulation. The structure option-1 is simple, however the AC insulation stress for the transformer secondary winding is 10kVAC, which leads to high dielectric loss at high switching frequency.

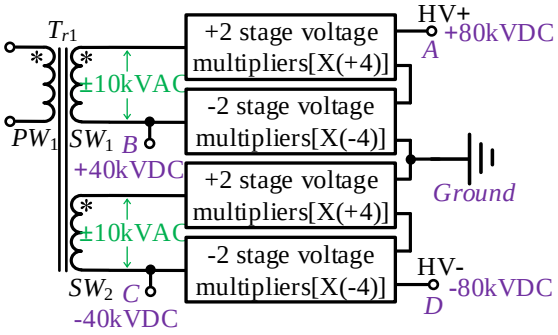
Structure option-2 with two elementary HV transformers, one primary winding and two secondary windings for the elementary HV transformer can reduce the AC insulation stress of the transformer secondary winding by half compared to structure option-1. This is promising for a high switching operation frequency with low dielectric loss for the transformer's secondary winding. However, the DC insulation stresses for the secondary winding and ferrite core are 20 kVDC and 60 kVDC. Since the DC insulation stress is not uniform, the insulation design of the HV transformer should be considered based on the maximum 60 kVDC insulation stress. A 2.5mm polypropylene insulation layer is required to achieve the insulation. A thicker insulation layer will lead to lower magnetizing inductance and coupling coefficient for the HV planar transformer in Fig. 4-28. The coupling coefficient decreases with the air-gap increase, so the air gap should be as thin as possible. Low magnetizing inductance and coupling coefficient will increase the reactive power and power rating, as well as the power loss for the HV pulse converter.

To improve the ununiform DC insulation stress in structure option-2, the secondary winding of two elementary transformers are connected in series, then connected to two stage dual polarity half-wave CW voltage multipliers in structure option-3. The AC insulation stress of the secondary winding for the elementary transformer is 5kVAC, The DC insulation stress of the secondary winding is 40kVDC. Though the AC insulation stress is low, and the DC insulation stress is uniform, the insulation structure for the HV transformer with one primary winding and two secondary windings is still complex and heat dissipation for three multilayer PCB windings is also a challenge.

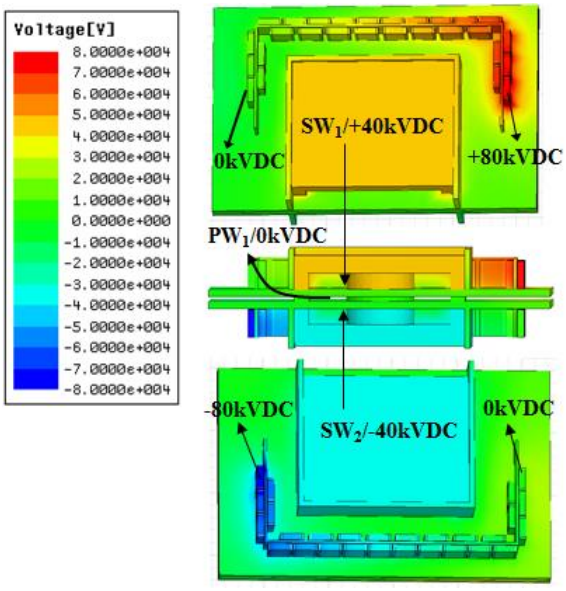
1 HV transformer; 2 stage voltage multipliers




(a) Circuit diagram

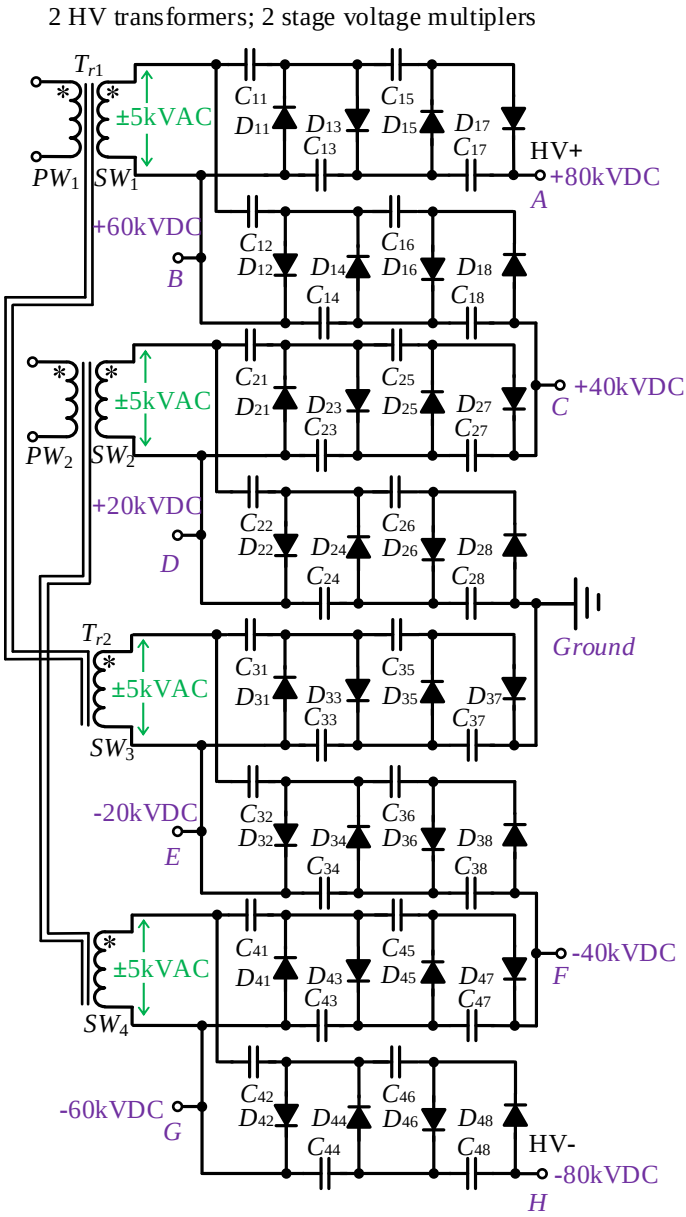



(b) Simplified circuit diagram

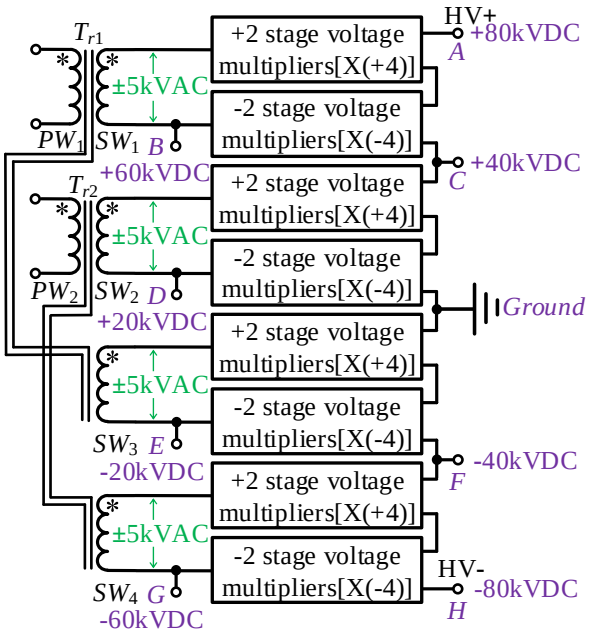



(c) Voltage distribution chart

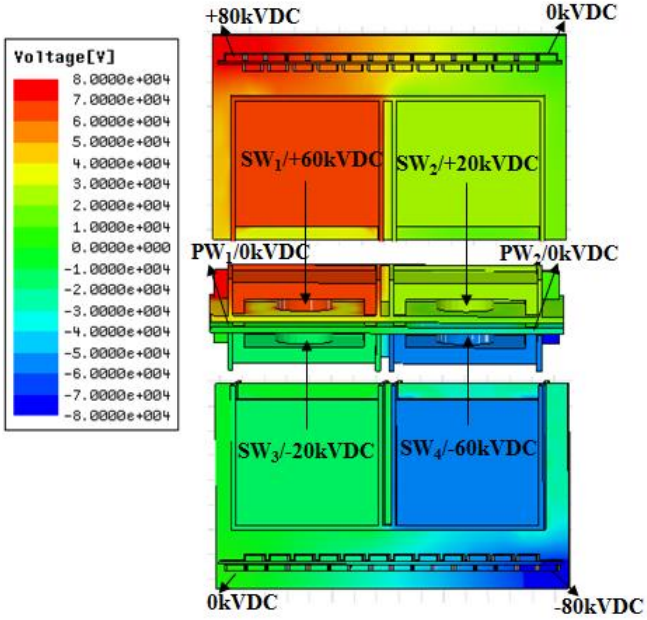
Fig. 4-23 Circuit diagram, simplified circuit diagram and voltage distribution of the planar HV transformer for the modular HV pulse converter: structure option-1




(a) Circuit diagram



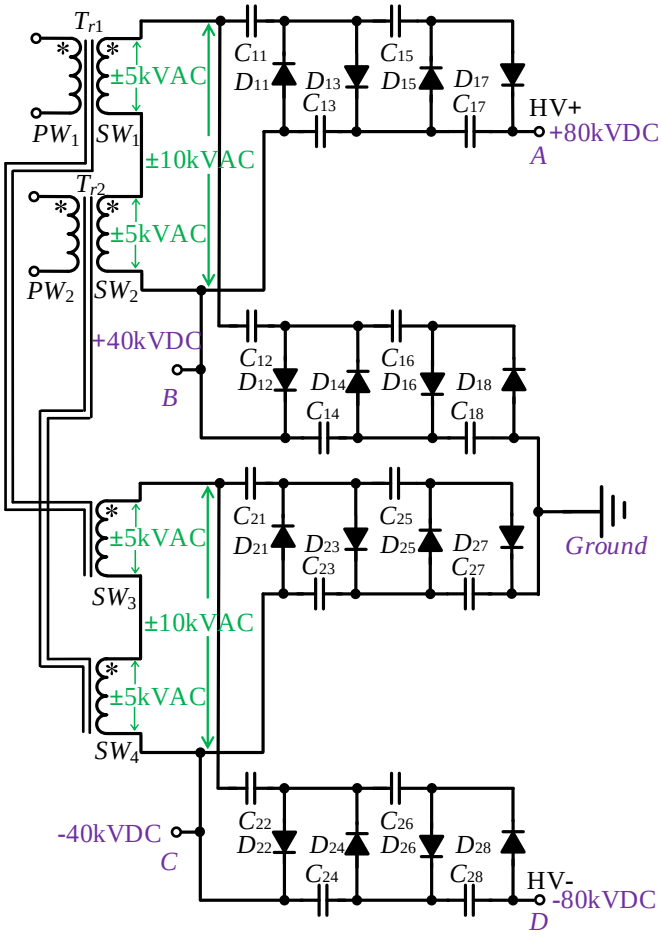

(b) simplified circuit diagram



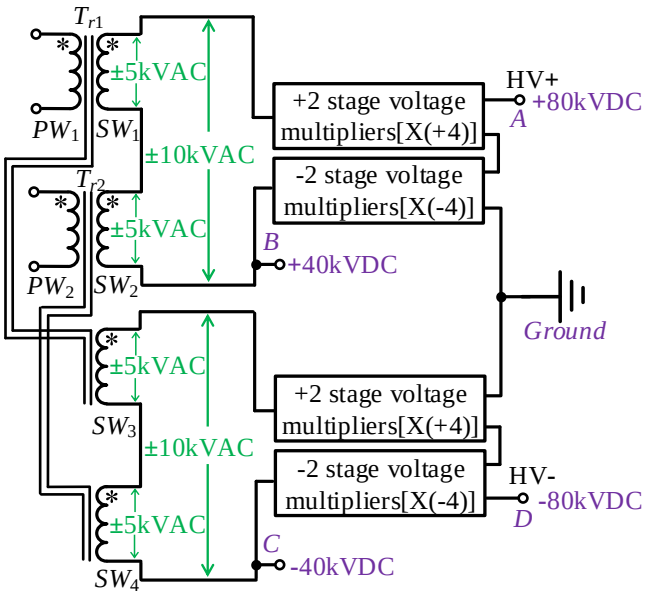

(c) voltage distribution chart

Fig. 4-24 Circuit diagram, simplified circuit diagram and voltage distribution of the planar HV transformer for the modular HV pulse converter: structure option-2

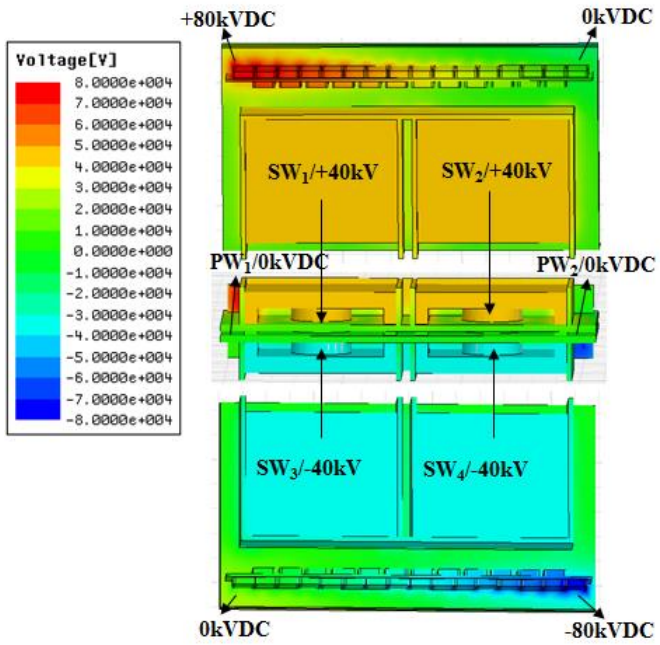
2 HV transformers; 2 stage voltage multiplers




(a) Circuit diagram




(b) Simplified circuit diagram



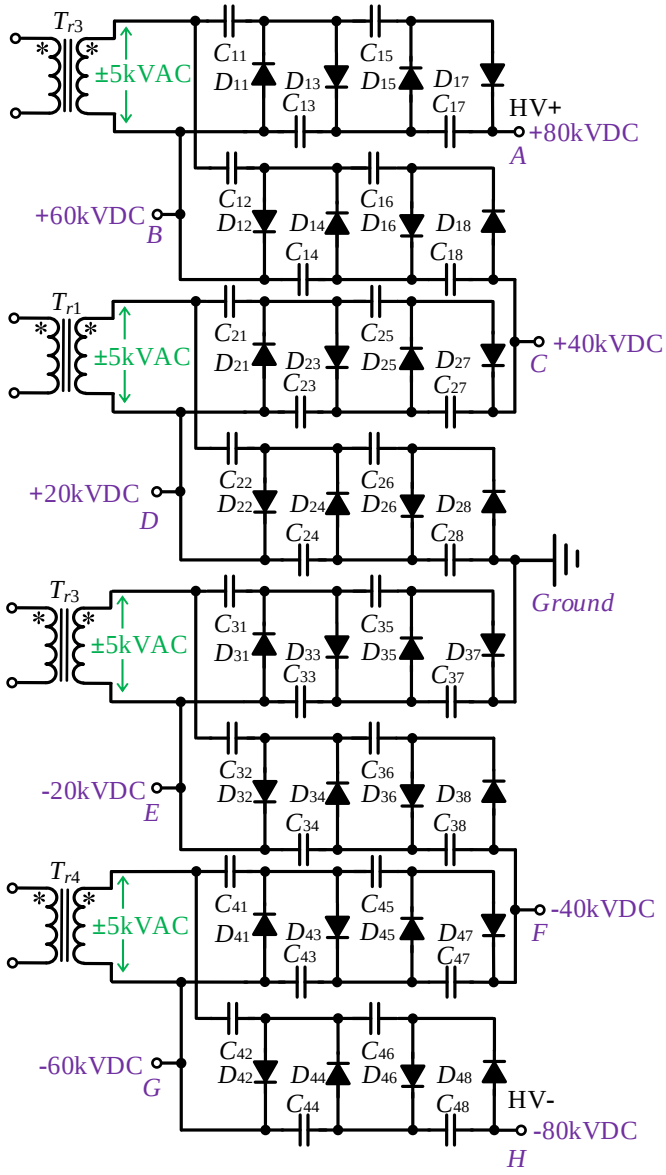

(c) Voltage distribution chart

Fig. 4-25 Circuit diagram, simplified circuit diagram and voltage distribution of the planar HV transformer for the modular HV pulse converter: structure option-3

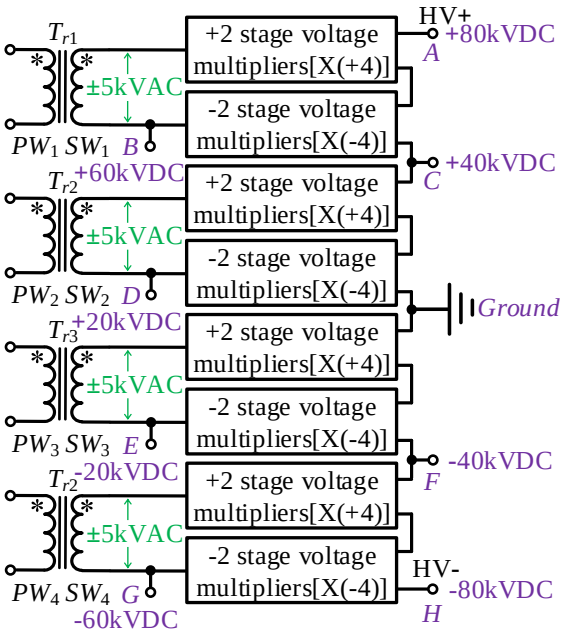
In structure option-4, four elementary HV transformers with one primary winding and one secondary winding simplify the insulation structure and heat dissipation for PCB windings. As for structure option-2, the DC insulation stress for the secondary winding and ferrite core is 20 kVDC and 60 kVDC since the DC insulation stress is not uniform.

To achieve low AC insulation, uniform DC insulation stress, easy insulation structure and heat dissipation structure, structure option-5 with four elementary HV transformers with one primary winding and one secondary winding is proposed. As for structure option-3, the secondary winding of two elementary HV transformers are connected in series, then connected to two stage dual polarity half-wave CW voltage multipliers. Structure option-5 outperforms the other four structures for the modular HV pulse converter based on planar transformers. The simulated maximum insulation stress is around 38.4 kV/mm.

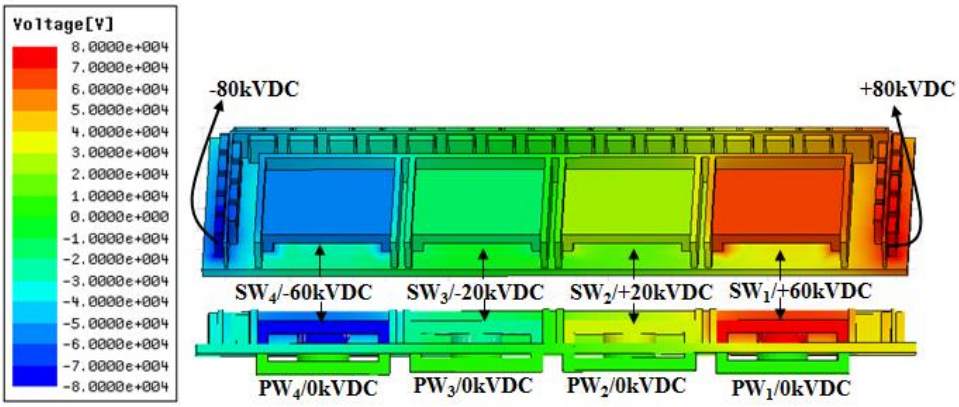
4 HV transformers; 2 stage voltage multipliers




(a) Circuit diagram

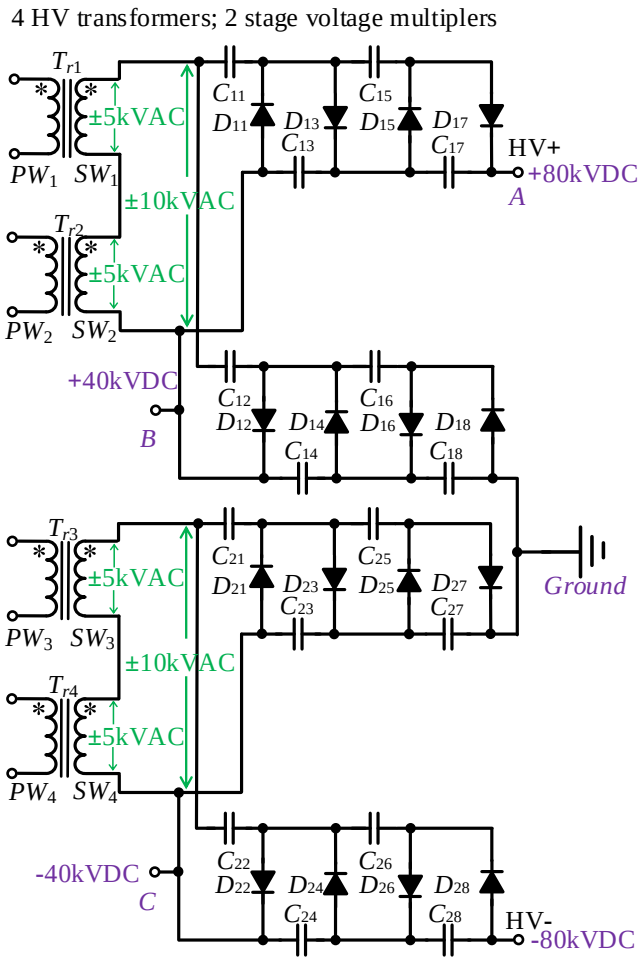



(b) Simplified circuit diagram

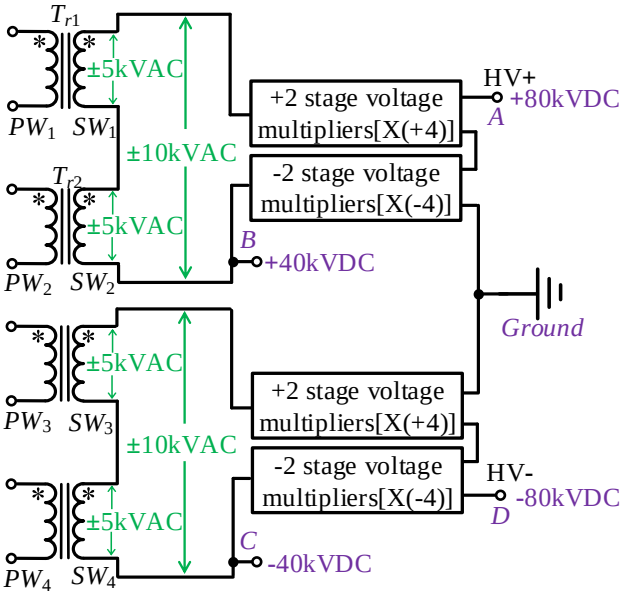



(c) Voltage distribution chart

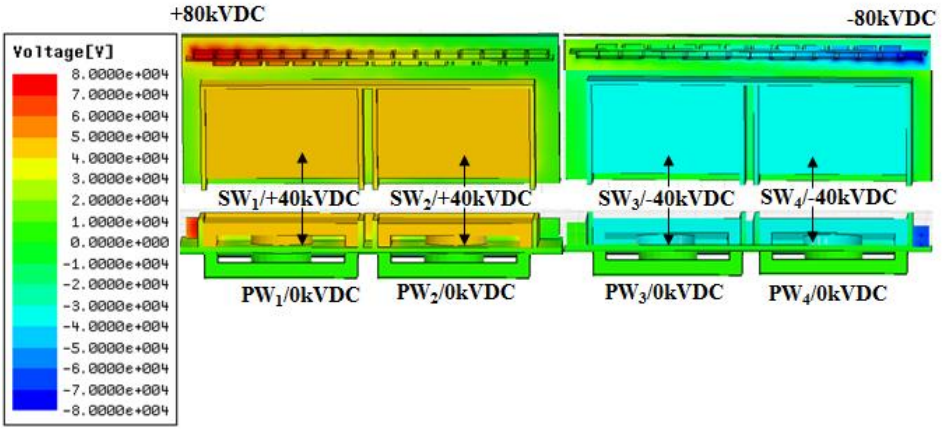
Fig. 4-26 Circuit diagram, simplified circuit diagram and voltage distribution of the planar HV transformer for the modular HV pulse converter: structure option-4




(a) Circuit diagram



(b) Simplified circuit diagram




(c) Voltage distribution chart

Fig. 4-27 Circuit diagram, simplified circuit diagram and voltage distribution of the planar HV transformer for the modular HV pulse converter: structure option-5

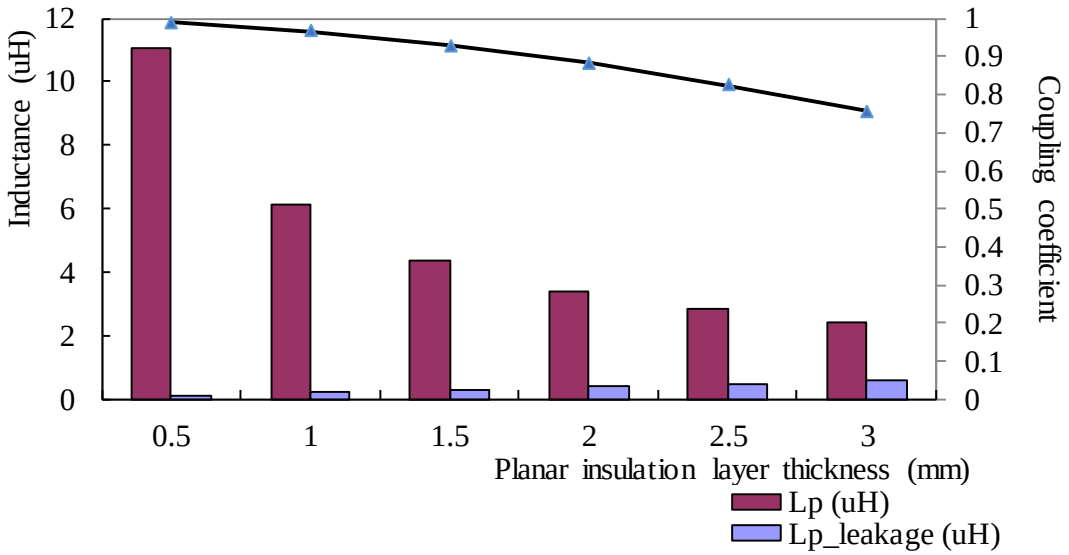



Fig. 4-28 Magnetizing inductance and coupling coefficient of the planar transformer with different planar insulation layer thicknesses for option 2

Based on the voltage distribution results, the summary of insulation stress for different planar HV transformer structures is given in Table 4-4.

Table 4-4 Summary of insulation stress for different planar HV transformer structures

| Planar HV transformer structure | Core and winding arrangement | AC insulation stress of secondary winding | DC insulation stress of secondary winding | Thickness of polypropylene insulation layer |
|---|---|---|---|---|
| Structure option-1 | 1 core, 1PW, 2SW | 10kVAC | 40kVDC | 1.5mm |
| Structure | 2 cores, | 5kVAC | 20kVDC/60kVDC | 2.5mm |

| | | | | |
|---|---|---|---|---|
| option-2 | 2PW, 4SW | | | |
| Structure option-3 | 2 cores, 2PW, 4SW | 5kVAC | 40kVDC | 1.5mm |
| Structure option-4 | 4 cores, 4PW, 4SW | 5kVAC | 20kVDC/60kVDC | 2.5mm |
| Structure option-5 | 4 cores, 4PW, 4SW | 5kVAC | 40kVDC | 1.5mm |

Fig. 4-29 gives a layout example of the planar HV transformer for the modular HV pulse converter based on structure option-5. The compromise between HV insulation, coupling coefficient & heat dissipation is needs to be considered for a compact and efficient HV pulse converter.

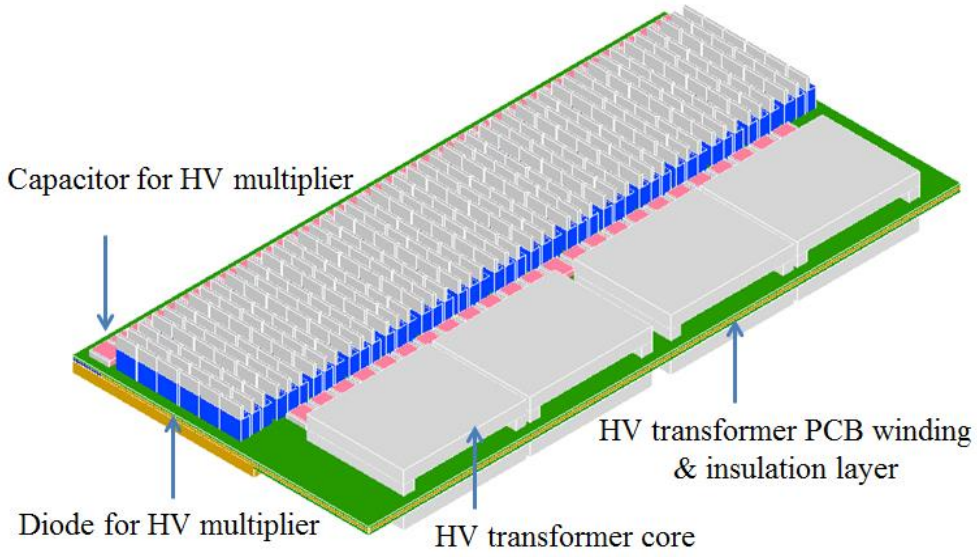
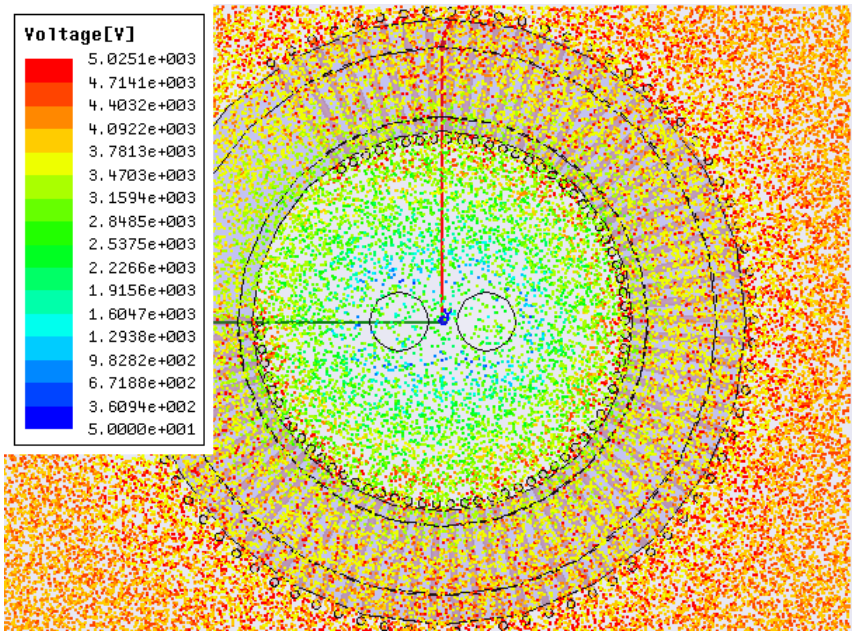


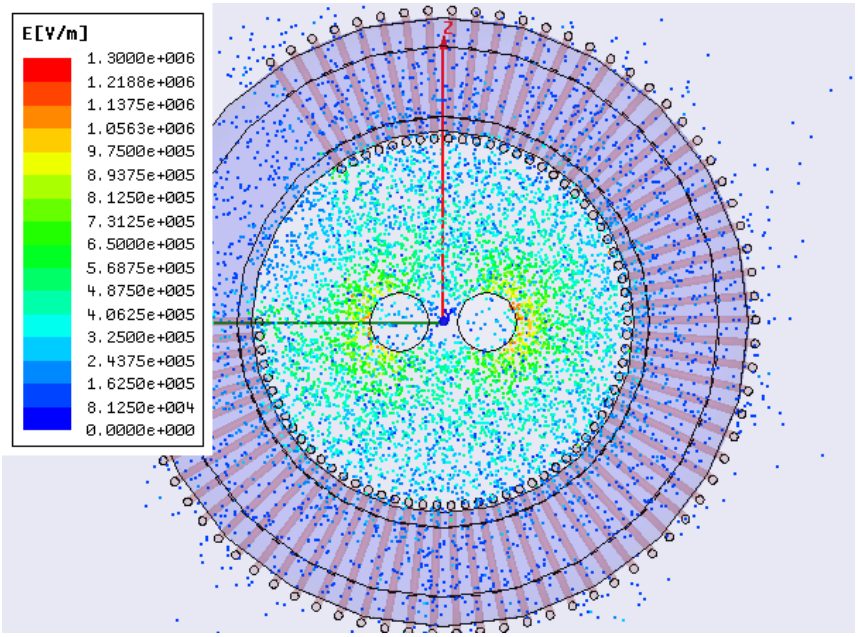

Fig. 4-29 Layout of planar HV transformer for modular HV pulse converter based on structure option-5

*E. Insulation stress for a HV wire-wound transformer with a toroid core structure based HV transformer for a modular HV pulse converter*

The voltage and insulation stress simulation for the packaging structure of the modular HV tank with a HV wire-wound transformer in Fig. 4-15 at 5kVDC, 80 kVDC and 160 kVDC are performed in Fig. 4-30 to Fig. 4-32. The key parameters of the HV wire-wound transformer with a toroid core structure are listed in Table 4-3. There are thirty-two elementary HV wire-wound transformers to generate 160kVDC output. The maximum electric field is located between the primary and secondary winding. The simulated maximum insulation stress at 80 kVDC and 160 kVDC is around 20 and 40 kV/mm respectively. Thick polypropylene tubing is required to provide sufficient insulation capability between the primary winding and the secondary winding and magnetic core.

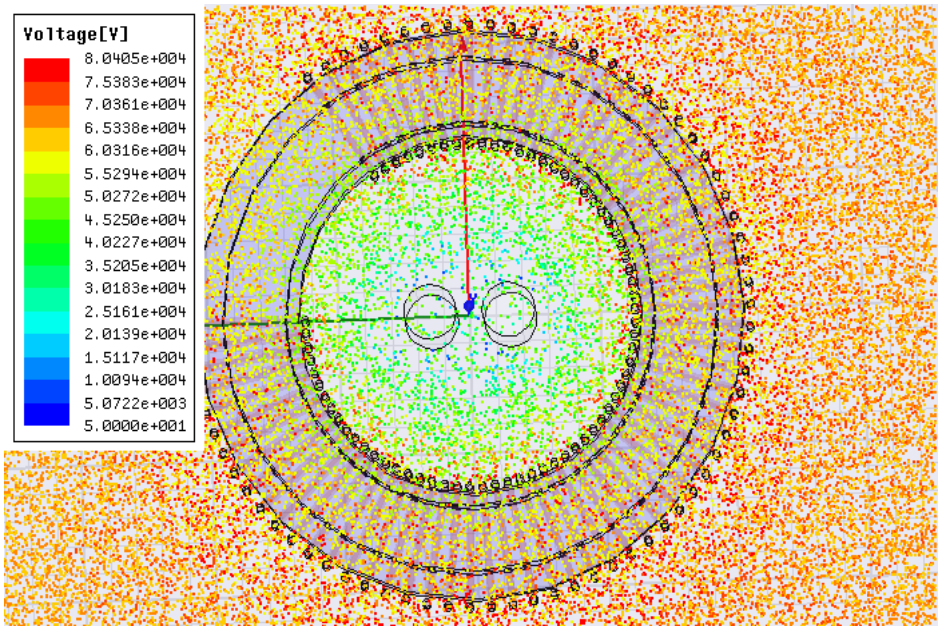



(a)Voltage simulation result at 5kVDC output

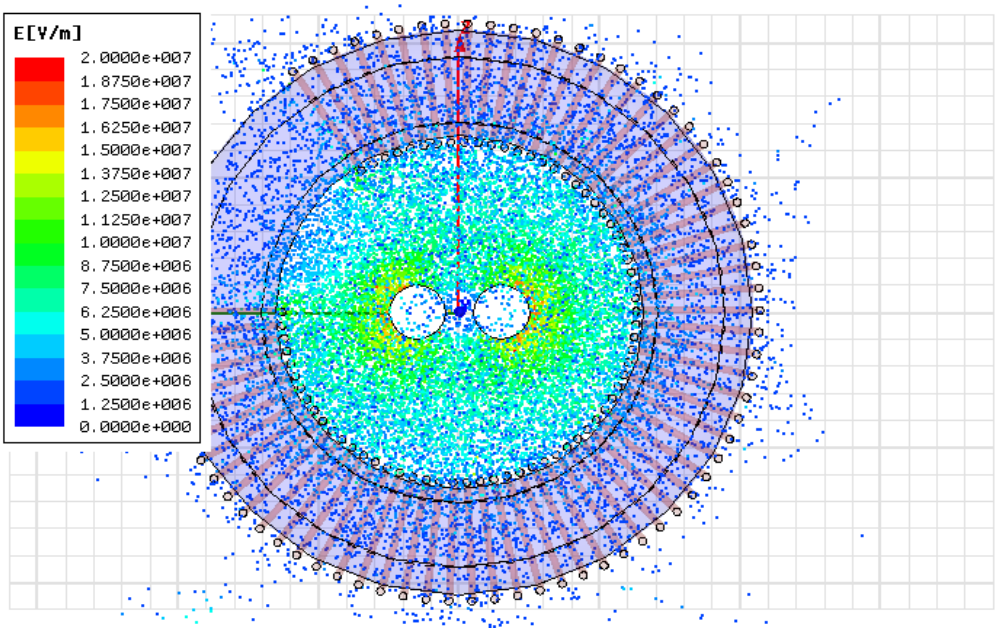



(b) Electric field simulation results at 5kVDC output

Fig. 4-30 Insulation stress analysis for the HV wire-wound transformer at 5kVDC output

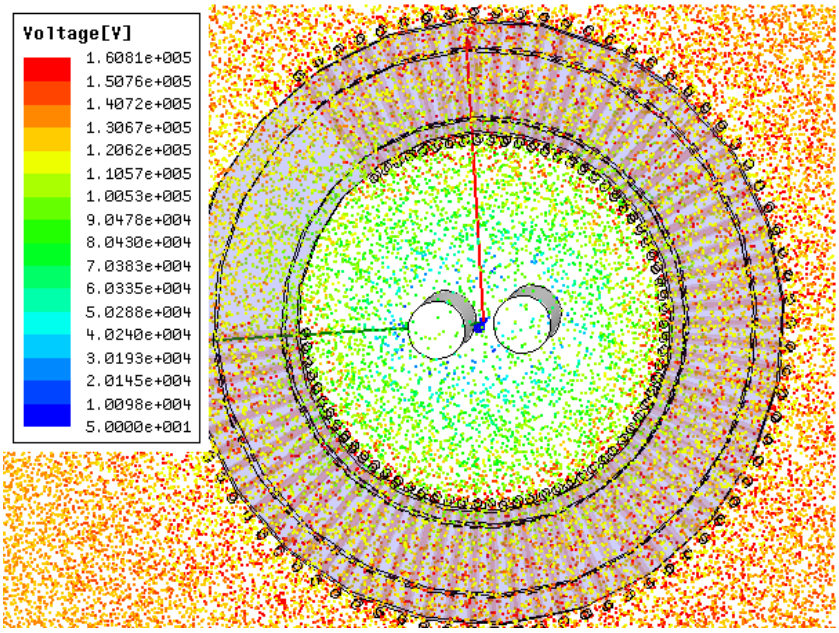



(a)Voltage simulation result at 80kVDC output

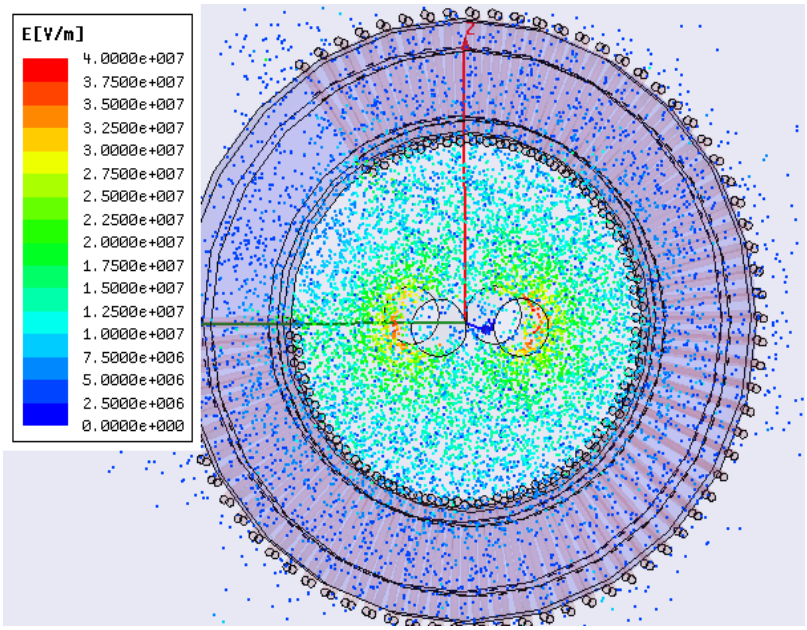



(b) Electric field simulation results at 80kVDC output

Fig. 4-31 Insulation stress analysis for the HV wire-wound transformer at 80kVDC output




(a) Voltage simulation result at 160kVDC output




(b) Electric field simulation results at 160kVDC output

Fig. 4-32 Insulation stress analysis for a HV wire-wound transformer at 160kVDC output

## 4.4 The influence of increasing switching frequency on a modular HV transformer

### 4.4.1 The advantage of increasing switching frequency

Operation at higher switching frequency results in a size reduction for the magnetic components based on the magnetic core size calculation equation (4-15) [4-21]. However, when the switching frequency reaches a certain frequency limit, excessive power losses need

to be considered to avoided increasing the size of the magnetic components to offset the advantage of size reduction at high switching frequency [4-15]-[4-16].

$$SQ = \frac{2 \cdot D \cdot P_O}{\Delta B \cdot \eta \cdot K_c \cdot K_u \cdot f_{\min} \cdot j} \tag{4-15}$$

where $\Delta B$ is the flux density, $\eta$ is the efficiency, $K_c$ is the core geometry factor, $K_u$ is the window utilization factor, $f_{\min}$ is the minim frequency, $j$ is the winding current density.

The relationship curve between the HV pulse converter power density and the switching frequency introduced in Fig. 3-16 based on the medical X-ray generator HV pulse converter products is redrawn in Fig. 4-33. The power density of the HV pulse converter will continue to increase as the switching frequency increases since high switching frequency will help to reduce the size of the HV passive components such the HV transformer, HV multiplier capacitor and resonators. On the other hand, high switching frequency will also generate a dramatically large power loss for the magnetic core and windings due to eddy current effects. Furthermore, the high frequency insulation stress needs to be considered for the HV transformer operating at a high switching frequency. The power density increase curve at higher switching frequency will not be linear. It will start to flatten at 300-500kHz switching frequency since sufficient insulation is required for the HV pulse converter though the magnetic core size can be reduced.

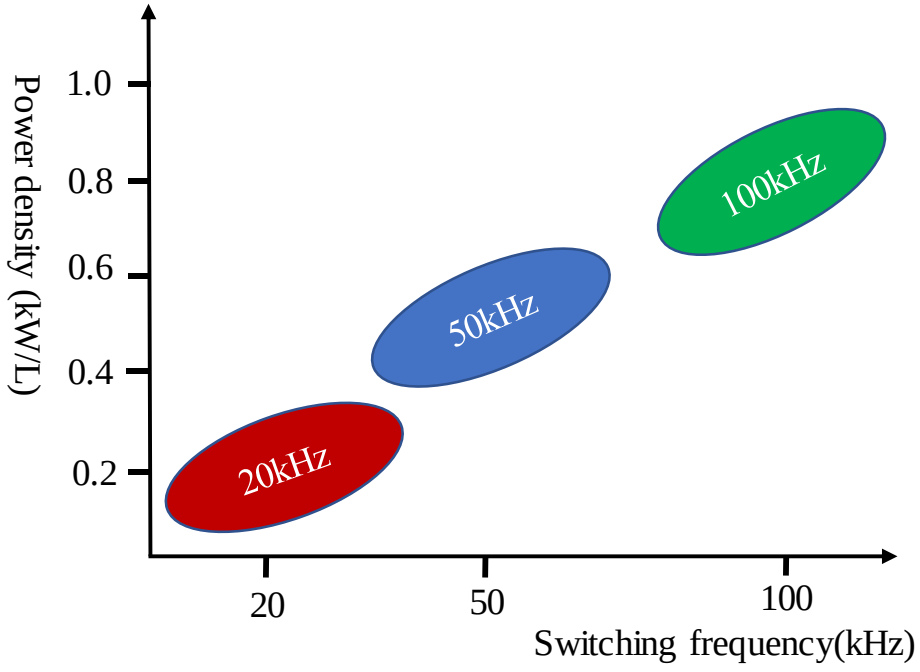



Fig. 4-33 The relationship curve between the HV pulse converter power density and switching frequency [4-17]

The magnetic core loss can be calculated based on Steinmetz equation which expresses core loss density as a power law with a fixed exponent of frequency and flux density

$$P_{core} = k_{core} \cdot f^{m} \cdot B_{\max}^{n} \cdot V_{core} \tag{4-16}$$

where $k_{core}$, $m$, and $n$ are constants provided by the magnetic core manufacturer, $f$ is the switching frequency and $B_{max}$ is the maximum flux density. $V_{core}$ is the volume of the magnetic core.

$$B_{\max} = \frac{V_{\sec}}{2 f A_e n_2} \tag{4-17}$$

High frequency will reduce the maximum flux density for the magnetic core. The magnetic loss depends on the constants of the magnetic materials, operating frequency and maximum flux density, as well as the core volume.

The transformer winding loss which includes winding conduction loss and dielectric loss is expressed as

$$P_{winding} = I_p^2 \cdot R_{pw\_AC} + I_s^2 \cdot R_{sw\_AC} + 2\pi f * C_{wp} * V_{cwp}^2 * \tan\delta \tag{4-18}$$

where, $I_p$ is the RMS value of the transformer primary current. $I_s$ is the RMS value of the transformer secondary current. $R_{pw\_AC}$ is the AC resistance for the primary winding, and $R_{sw\_AC}$ is the AC resistance for the secondary winding, $C_{wp}$ is the parasitic winding capacitance of the HV transformer. The loss is related to the dielectric constant of the winding insulation materials and the electric field strength across the winding. $V_{CWP}$ is the voltage applied to the parasitic winding capacitance. tanδ is the dissipation factor of insulation materials.

High frequency will not only increase the AC resistance of the transformer's primary and secondary windings, but will also increase the high frequency dielectric loss for the secondary winding.

As discussed in Chapter-3, the total power loss of the HV transformer and voltage multiplier in the HV tank is a function of frequency. The relationship curve between the HV tank power loss with a different switching frequency for the 100kV/10kW HV pulse converter shown in Fig. 3-18 is redrawn in Fig. 4-34. The operation frequency to achieve the minimum power loss of the HV tank for different HV generation architectures will be different.

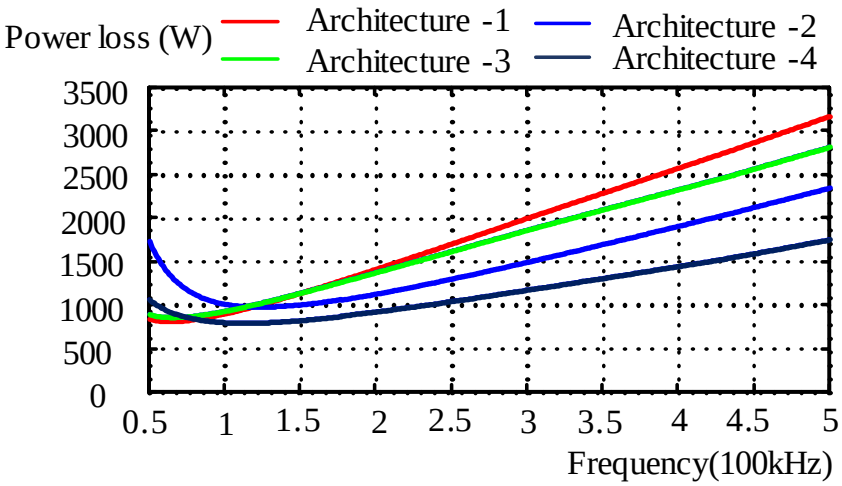



Fig. 4-34 Relationship curve between the HV tank power loss with frequency (100kV/10kW HV pulse converter as case study)

### 4.4.2 The challenges of increasing the switching frequency for the HV transformer

The following are some challenges of increasing switching frequency for the HV transformer in the modular HV pulse converter architectures.

1) High frequency low loss magnetic material needs to be considered when the switching frequency increases [4-19].
2) High frequency winding technology and winding arrangements such as litz wire and PCB or foil windings can effectively reduce the winding AC resistance when the switching frequency increases [4-24].
3) HF insulation materials with a low dissipation factor will effectively reduce the dielectric loss for the HV transformer secondary winding.

## 4.5 Design considerations and experimental results

### 4.5.1 Specifications

A planar HV transformer is taken as a case study for the elementary HV transformer for the modular HV pulse converter. The electrical and insulation design of 2kW 400kHz 5kV HV planar transformers for a 2kW 35kVDC HV pulse converter are discussed in detail.

The electrical parameters for the HV pulse converter are listed in Table I. The design requirements for the HV transformer are high power density and ease of insulation and manufacturing assembly. The targeted power density is 2kW/L for the 2kW, 35kV HV pulse converter. The 400kHz high switching frequency which is around four times higher than the switching frequency of a benchmark HV pulse converter and industry standard is investigated to achieve the high power density for a 2kW 35kV HV pulse converter.

Besides the standard electrical design, the dedicated HV insulation design for the transformer needs to be addressed. The electrical insulation requirements have a strong influence on the volume of the HV transformer and the HV pulse converter.

Table 4-5 Specifications of the HV pulse converter prototype

| Items | Values |
|---|---|
| Input voltage | 400VDC |
| Output voltage | 35kVDC |
| Output power | 2kW |
| Switching frequency | 400kHz |
| HV pulse converter power density | 2kW/L |

### 4.5.2 Insulation design

State of the art planar transformer design which integrates the primary and secondary winding into one PCB to the HV transformer will not be feasible for the HV transformer due to HV insulation, and manufacturing issues [4-20]. The planar transformer should handle the high frequency AC insulation and HV DC insulation in a voltage multiplier based HV pulse converter. Further, with high switching frequency operation, the dielectric power loss will be high inside the PCB. Based on the insulation analysis in the previous section, a new design with separated PCBs for the HV transformer primary and secondary windings is expected to meet the target. Additional FR4 layers in both the and bottom side are used as a cover insulation layer to improve the insulation between core and winding as shown in Fig. 4-35. The primary and secondary parts of the transformer are separated with a 1mm polypropylene insulation layer between the primary and secondary sides for sufficient insulation capability in Fig. 4-36. The insulation oil provides around 10kV/mm insulation and a good heat dissipation environment for the HV planar transformer.

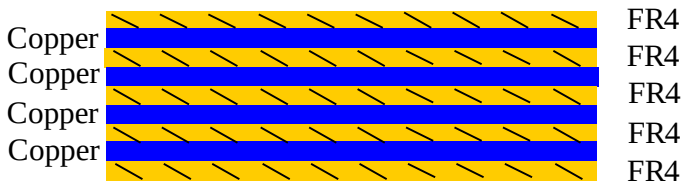



Fig. 4-35 Cross-section of 6-layer PCB for windings

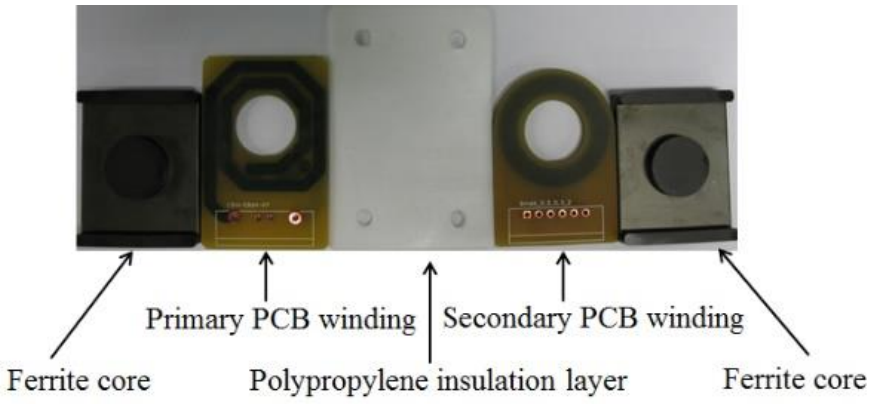



Fig.4-36 Photo of the HV transformer subcomponents

### 4.5.3 Electrical design

The two stage positive and negative dual polarity voltage multipliers are used to further increase the high frequency high voltage AC voltage from the HV transformer. The secondary

winding voltage can be controlled to about 5kVAC for easy high frequency insulation and reduced high frequency dielectric loss. The current rating for the HV transformer secondary winding will be around 400mA for 2kW output power.

Based on the input voltage and output voltage, the transformer turn ratio *n* can be derived by:

$$n = N_S : N_p = \frac{V_o}{V_{in} * D * H} \tag{4-19}$$

where *D* is the duty cycle of LCC resonant converter and *H* is the gain of the LCC resonant converter.

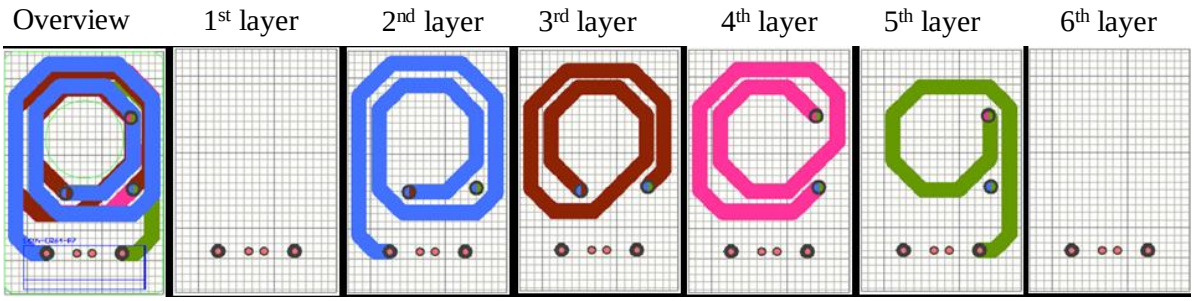
The required transformer core area can be calculated based on equation (4-15). The planar ER64 ferrite core with 3F3 high frequency materials from Ferroxcube are chosen for enough winding area.

The turn number of the secondary winding of the HV windings can be derived by equation (4-20). The turns number of the primary winding can be calculated based on the secondary winding and transformer turns ratio in equation (4-20).

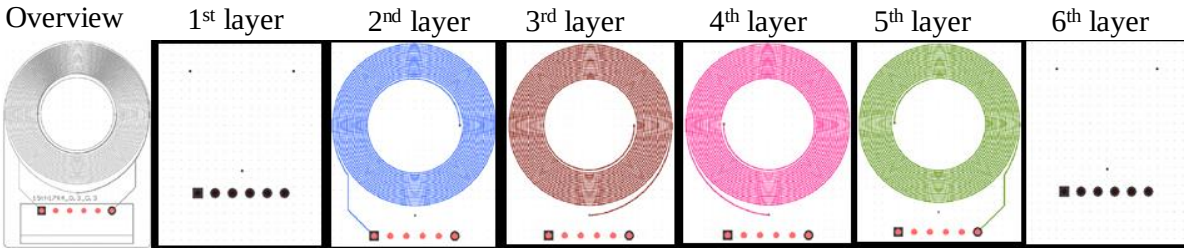
$$N_S = \frac{V_{Sec} * D_{Sec}}{4 * f_S * B_m * A_e} \tag{4-20}$$

$$N_p = N_S * n \tag{4-21}$$

The turn number of the primary winding is seven, and the turn number of the secondary winding is sixty-eight. The thickness of both primary and secondary winding is 4OZ for low winding loss. A detailed layout of the HV transformer primary and secondary windings is illustrated in Fig. 4-37.




(a) Primary winding layout



(b) Secondary winding layout

Fig. 4-37 Detailed layout of the HV transformer primary and secondary winding

Based on the HV transformer primary and secondary winding turn calculation, the window space factor can be verified. The planar ER64 ferrite core provides a sufficient window space factor for the HV transformer primary and secondary PCB windings.

The maximum electric field strength inside the HV transformer is the sharp edges of the outer PCB winding. The maximum electric field strength is around 6.9kV/mm based on Maxwell simulation. The HV planar transformer prototype has passed the 400kHz high frequency AC and HV DC insulation test at a full rating 35kVDC generator.

### 4.5.4 Power loss anlysis

HFHV planar transformer losses are analysed at around a 400kHz switching frequency in Table 4-6. The power loss can be obtained from equations (4-21) to (4-23). The magnetic core loss is based on the unit volume ferrite core loss characteristics. The winding loss is calculated by the winding current and resistances calculated by Dowell's formula. The power loss distribution chart for the planar HV transformer is illustrated in Fig. 4-38. The dielectric loss dominates the transformer power loss at a high switching frequency.

Table 4-6 Power loss of the HV planar transformer at 400 kHz

| Items | Power loss (W) |
|---|---|
| Dielectric loss | 47.44 |
| Core loss | 31.60 |
| Winding loss | 22.76 |
| Total loss | 101.80 |

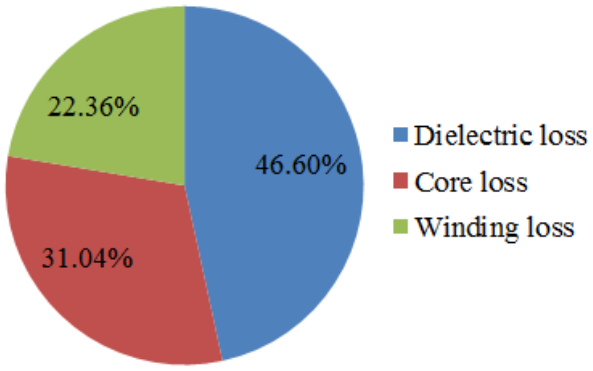



Fig. 4-38 Power loss distribution chart for planar HV transformer

$$P_{dielectric} = \omega C * V^2 * \tan\delta \tag{4-22}$$

$$P_{core} = P_V * V \tag{4-23}$$

$$P_{winding} = I_{winding}{}^2 * R_{winding\_ac} \tag{4-24}$$

The planar HV transformer magnetic core loss is calculated based on the unit volume ferrite core power loss characteristics. The winding loss is calculated by the winding current and resistances calculated by Dowell's formula. The core loss for the HV planar transformer at 400kHz is 31.60W and the winding loss is 22.76W. The calculated dielectric loss for the HV planar transformer is 47.44W. The power loss distribution chart for the planar HV transformer is illustrated in Fig. 4-39. The dielectric loss dominates the high frequency HV planar transformer power loss at a high switching frequency.

Based on the above detailed planar HV transformer structure, electrical and insulation design, the design parameters of the 2kW 400kHz 5kV HFHV planar transformer for a 35kV HV pulse converter can be calculated. The HV planar transformer parameters are summarized in Table 4-7.

Table 4-7 HV planar transformer parameters

| Items | Values |
|---|---|
| Input voltage | 400VAC |
| Switching frequency | around 400kHz |
| Output voltage | 5kVAC |
| Power | 2kW |
| Core | Planar ER64, 3F3 ferrite |
| Insulation layer | 1.0mm polypropylene |
| Primary winding | 7 turns, 4 OZ, 22μH |
| Secondary winding | 68 turns, 4 OZ, 3400μH |
| Coupling coefficient | 0.92 |

### 4.5.5. Experimental results

To verify the conceptual design, a 2kW 400kHz 5kV HV planar transformer hardware prototype is built in the lab for a 35kV DC HV pulse converter prototype shown in Fig. 4-39. The circuit diagram and prototype photo of the HV pulse converter hardware prototype are shown in Fig.4-39 and Fig. 40 respectively. The input voltage is 400VDC. $C_r$ is the series resonant capacitor as well as DC blocking capacitance, $L_r$ is the series resonance inductor, $L_m$ is the transformer magnetizing inductance, $L_{plk}$ is the transformer leakage inductance and $C_p$ is the parallel resonant capacitor including the parasitical capacitance of high voltage transformer. The HV pulse converter includes the high frequency inverter part, HV transformer and voltage multiplier parts which help to achieve the high voltage conversion. $L_r$=27.0μH, $C_r$=15.4nF, $L_m$=18.7μH, $L_{plk}$=3.3μH, $C_p$=12.1nF (including 3.3nF parasitic capacitance of HV transformer reflected into primary side). The magnetizing inductance $L_m$ is smaller compared with a conventional transformer without insulation layer.

There are three resonances for the resonant tank. The resonant frequencies for these resonances are shown in equations (4-25) to (4-27).

$$f_1 = \frac{1}{2\pi\sqrt{(L_m + L_s + L_{plk})C_r}} \tag{4-25}$$

$$f_2 = \frac{1}{2\pi\sqrt{L_m C_p}} \tag{4-26}$$

$$f_3 = \frac{1}{2\pi\sqrt{\frac{(L_s + L_{plk}) * L_m}{L_s + L_{plk} + L_m} C_p}} \tag{4-27}$$

In order to achieve the sine wave primary resonant tank current, and keep zero voltage switching, an operation frequency range higher than $f_3$ is chosen to guarantee the above resonance operation with zero voltage switching for switches. A 400kHz operation switching frequency is adopted in the hardware prototype.

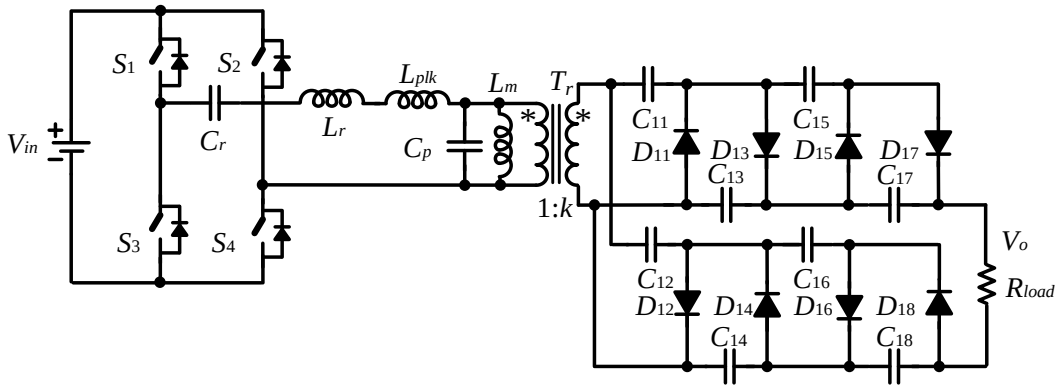



Fig. 4-39 Circuit diagram of a 2kW 35kVDC HV pulse converter with the planar transformer

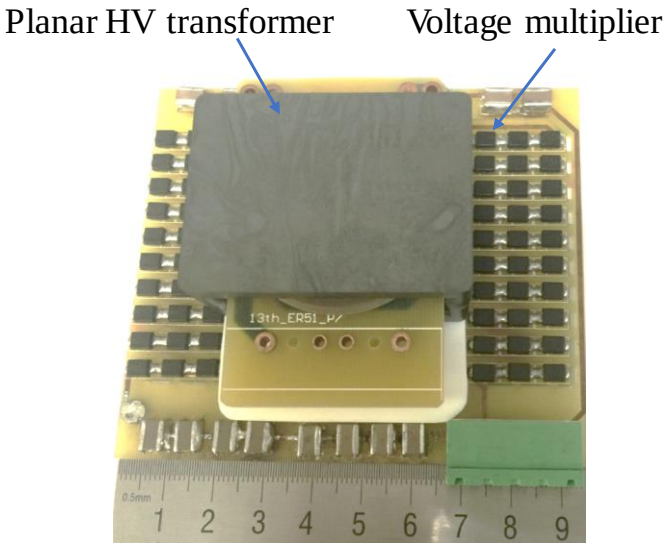



Fig. 4-40 Prototype photos of a 2kW 35kVDC HV pulse converter with the planar transformer

The key experimental waveforms of a 35kVDC HV pulse converter prototype are shown in Fig. 4-41. The switches of the high frequency inverter can achieve zero voltage switching. Both the electrical and insulation performance of the planar transformer can meet design

requirements. The power density of the 2kW 35kV HV pulse converter prototype is 2.2kW/L, which is higher than power density design target of 2kW/L. The thermal performance of the HV planar transformer prototype is experimentally evaluated at 50˚C oil environment by FLUKE thermal camera as shown in Fig. 4-42. The maximum temperature rise for the planar HV transformer is below 20˚C. The secondary winding of the planar HV transformer exhibits higher temperature rise due to the high dielectric loss inside the PCB. The temperature rise of PCB winding needs to be tightly controlled below the FR4 epoxy glass transition temperature($T_g$) to avoid a thermal runaway. Another important physical change that can occur with changing $T_g$ in an adhesive is the change in coefficient of thermal expansion (CTE). As the temperature rises past the $T_g$, the adhesive will begin to soften and lose some tensile strength.

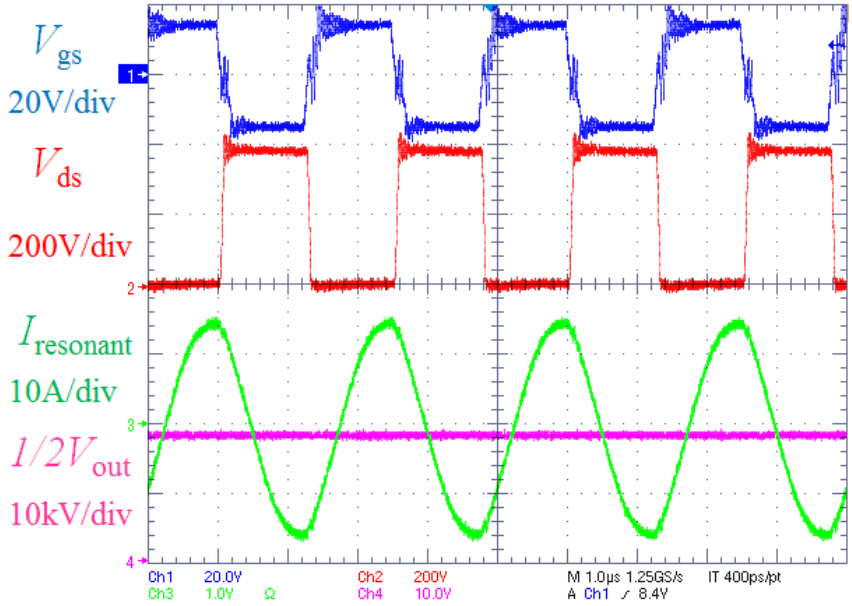



Fig. 4-42 Key waveforms for a 2kW 35kV HV pulse converter with a 5kV planar HV transformer

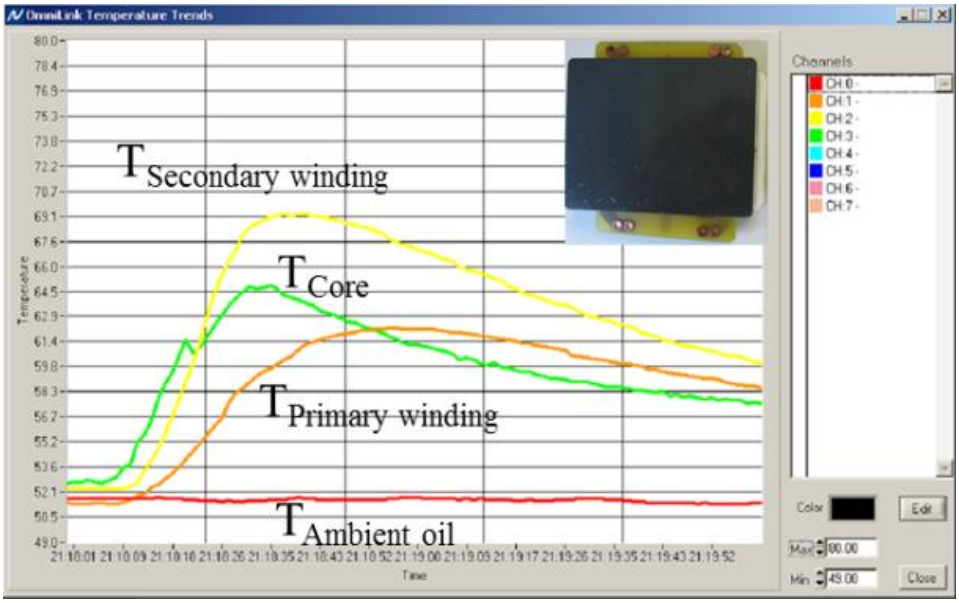



Fig. 4-42 A planar HV transformer thermal test at 50°C oil environment

Furthermore, the insulation capability of FR4 epoxy and other dielectric materials at elevated temperature will degrade. The resistors of the PCB windings will also increase when the temperature rises. Since the width of the copper trace is limited to achieve a large turns number with the space of planar magnetics, the thermal performance of the high frequency HV planar transformer can be improved with thicker copper layer. The dielectric material with high thermal conductivity can help to reduce the temperature rise of PCB windings.

The detailed electrical and insulation designs of a 400kHz 5kV HFHV planar transformer for a 2kW 35kVDC HV pulse converter are introduced. The prototype experimental results validate the conceptual design of the high frequency FHV planar transformer. The planar HV transformer can meet the high voltage isolation requirements and achieve the high power density. The power density of the 2kW 35kVDC HV pulse converter with a proposed HV planar transformer is higher than 2kW/L and the size of the HV transformer in the HV pulse converter can be reduced with high switching frequency operation. However, the power loss and high frequency insulation requirements need to be carefully considered when the switching frequency increases. The bottleneck will be the increased power loss due to high core loss, winding loss and the dielectric loss at high switching frequency. The thermal management and heat dissipations need to be considered at high frequency. A system level optimal trade-off study on the switching frequency, transformer structure and electrical, insulation and thermal design are required for superior performance in the HV pulse converter system. The proposed design methodology for a high frequency high voltage planar transformer can be applied to other HV pulse converter applications.

The modular HV pulse converter demonstrators with the planar and wire-wound HV transformer are provided in the Appendix.

## 4.6 Summary

In this chapter, firstly the advantages of modularization for HV transformers for the HV pulse converter are introduced. The modularization of HV transformers provide advantages such as low insulation stress, low dielectric loss, distributed thermal stress and size reduction at high frequency without sacrifice on efficiency. It also provides the scalability to different HV pulse converter ratings and easy assembly and manufacturing. The interconnection structures of the modular HV transformers for the HV pulse converter which can basically be divided into series and parallel interconnection between the primary side of the HV transformer and inverter are discussed. Then the equivalent circuit diagram is derived to better understand the characteristics of the modular HV pulse converter architectures. The planar and wire-wound packaging and insulation structure for the HV transformer is presented. The detailed HV AC and DC insulation stress of HV transformer for the modular HV pulse converter is analysed. The advantages and challenges of increasing the switching frequency for the HV transformer are discussed. Finally, the electrical and insulation design and prototype experimental results of the high frequency HV transformer for the modular HV pulse converter architecture are provided.

## 4.7 References

[4-1] J. Martin-Ramos, A. M. Pernía, J. Diaz, F. Nuño, and J. A. Martínez, “Power supply for a high voltage application,” IEEE Transaction Power Electron., vol. 23, no. 4, pp. 1608-1619, Jul. 2008.
[4-2] S. Mao, C. Li; W. Li; J. Popovic, J. Ferreira, “A Review of High Frequency High Voltage Generation Architecture,” in Proc. IEEE ECCE-Asia 2017, 2017, pp. 1-7.
[4-3] T. Guillod, R. Färber, F. Krismer, C. M. Franck, J. W. Kolar, “Computation and analysis of dielectric losses in MV power electronic converter insulation,” in Proc. IEEE ECCE Conf., 2016, pp. 1-8.
[4-4] H. Kurita, T. Hasegawa, Y. Shibuya, T. Gohnai, H. Ohsuga, Y. Honda, “Dielectric loss of high voltage-high frequency transformers used in switching power supply for space,” in Proc. IEEE PESC Conf., 1988, pp. 1120-1126.
[4-5] G. Ivensky, A. Kats and S. Ben-Yaakov, "An RC load model of parallel and series-parallel resonant DC-DC converters with capacitive output filter," IEEE Transaction Power Electron., vol. 14, no. 3, pp. 515-521, May. 1999.
[4-6] J. Martin-Ramos, J. Diaz, A. M. Pernía, J. M. Lopera, and F. Nuño, “Dynamic and steady state models for the PRC-LCC topology with a capacitor as output filter,” IEEE Transaction Ind. Electron., vol. 54, no. 4, pp. 2262-2275, Aug. 2007.
[4-7] Y. Du, J. Wang, G. Wang, and A. Q. Huang, “Modeling of the high frequency rectifier with 10-kV SiC JBS diode in high-voltage series resonant type DC-DC converters,” IEEE Tran. Power Electron., vol.29, no.9, pp. 4888-4900, Aug. 2014.
[4-8] Z. Ouyang, M. A. E. Andersen, “Overview of planar magnetic technology-fundamental properties,” IEEE Tran. Power Electron., vol.29, no.8, pp. 4288-4300, Aug. 2014.
[4-9] S. Mao, J. Popovic, J. A. Ferreira, “ An Investigation into High Frequency High Voltage Planar Transformer for High Voltage Generator Applications,” in Proc. IEEE 2016 9th International Conference on Integrated Power Electronics Systems(CIPS), pp. 1-6.
[4-10] Y. A. Wang, D. M. Xiao, and Y. L. Liu, “Design of a planar power transformer for high voltage, high frequency use,” in Proc. IEEE PES Transmission Distrib. Conf. Expo., Apr. 2010, pp. 1-6.
[4-11] R. Chen, F. Canales, B. Yang, P. Barbosa, J. D. van Wyk, and F. C. Lee, “Integration of electromagnetic passive components in DPS front-end DC/DC converter—A comparative study of different integration steps,” in Proc. IEEE APEC, 2003, pp. 1137-1142.
[4-12] C. Loef, R. W. Doncker and B. Ackermann, “On high frequency high voltage generators with planar transformers”, in Proc. APEC, 2014, pp. 1936-1940.
[4-13] L. Dalessandro, F. S. Cavalcante, and J. W. Kolar, “Self-capacitance of high-voltage transformers,” IEEE Transaction Power Electron., vol. 22, no. 5, pp. 2081-2092, Sep. 2007.
[4-14] J. Liu, L. Sheng, J. Shi, Z. Zhang, and X. He, “Design of High Voltage, High Power and High Frequency Transformer in LCC Resonant Converter,” in Proc. APEC, 2009, pp. 1034-1038.
[4-15] W.-J. Gu and R. Liu, “A study of volume and weight vs. frequency for high-frequency transformers,” in Proc. IEEE PESC, 1993, pp. 1123-1129.

[4-16] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Leitermann, R. C. N. Pilawa, Podgurski, A. Sagneri, and C. R. Sullivan, “Opportunities and challenges in very high frequency power conversion,” in Proc. IEEE APEC, 2009, pp. 1-14.

[4-17] S. Mao, C. Li, W. Li, J. Popovic, J. Ferreira, “A Review of High Frequency High Voltage Generation Architecture,” in Proc. IEEE ECCE-Asia, 2017, pp. 1-7.

[4-18] S. Mao, C. Li, W. Li, J. Popovic, J. Ferreira, “Comparative Analysis and Evaluation of High Voltage Power Generation Architectures,” in Proc. IEEE ECCE, 2017, pp. 1-8.

[4-19] W. Pfeiffer, “High-frequency voltage stress of insulation, methods of testing,” IEEE Transaction on Electrical Insulation, vol. 26, no. 2, April 1991, pp. 239-246.

[4-20] C. Quinn, K. Rinne, T. O'Donnell, M. Duffy, C.O. Mathuna, “A review of planar magnetic techniques and technologies”, in Proc. IEEE APEC 2001, pp. 1175-1183.

[4-21] Colonel Wm T. McLyman, Transformer and Inductor Design Handbook, 2011

[4-22] S. Mao, C. Li, W. Li, J. Popovic, J. Ferreira, “Planar Transformer for High Frequency High Voltage Generation Applications,” in Proc. IEEE ECCE-Asia, 2016, pp. 1-4.

[4-23] S. Mao, C. Li, W. Li, J. Popovic, J. Ferreira, “Investigations of High Frequency High Voltage Planar Transformer for High Voltage Generator Applications,” in Proc. IEEE International Conference on Integrated Power Electronics Systems (CIPS), 2016, pp.1-6.

[4-24] Charles R. Sullivan, “Prospects for advances in power magnetics,” in Proc. IEEE International Conference on Integrated Power Electronics Systems (CIPS), 2016, pp.1-9.

# Chapter 5

# Steady state and dynamic analysis of the volatge multiplier for the modular HV pulse converter

## 5.1 Introduction

A voltage multiplier circuit is one of the power building blocks for the modular HV pulse converter. HV pulse rise and decay times play a critical part for the modular HV pulse converter system's performance such as for the imaging quality for CT and X-ray machines and the sparkover handling capability, efficiency, and electrodes stress for electrostatic precipitators. However, the steady state and dynamic response characteristics of the voltage multiplier based HV pulse converter has not been well investigated. The key influence factors of HV pulse rise and decay times have not been studied in detail. Furthermore, the high frequency voltage multiplier diode reverse recovery process which limits the switching frequency of the voltage multiplier has not been addressed in literature. It is important to investigate the diode reverse recovery process and its mitigation solution for a multistage voltage multiplier at high switching frequency.

In Chapter 5, firstly the steady stage analysis of the voltage multiplier circuit will be introduced. The HV pulse dynamic response characteristics are investigated for the voltage multiplier based HV pulse converter. Key factors which influence the pulse response characteristics for the HV power supply such as stage number, switching frequency, load resistance, and capacitance for the voltage multiplier are analysed. Then the diode reverse recovery process for multi-stage voltage multiplier is investigated. The power loss calculations for the high frequency voltage multiplier are given. Finally, the demonstrator of the high frequency voltage multiplier validates the steady state and dynamic analysis of the voltage multiplier.

## 5.2 Steady state circuit analysis of the voltage multiplier

The half-wave (HW) Cockcroft–Walton (CW) voltage multiplier in Fig. 5-1 is a popular voltage multiplier because of its HV boosting features, compact size, low voltage stress on diodes and capacitors, as well as its cost effectiveness [5-1]-[5-3]. A three-stage HWCW voltage multiplier is shown as a case study in Fig. 5-2. $V_s$ is a sinusoidal voltage source. $L_s$ represents the circuit parasitic inductor, which can be the transformer leakage inductor or a real inductor introduced into the voltage multiplier circuit.

The positive half cycle of the 3-stage HWCW voltage multiplier circuit is analysed as an example. There are four operation modes, as shown in Fig. 5-4, and the characteristics in each operation mode are depicted as follows.

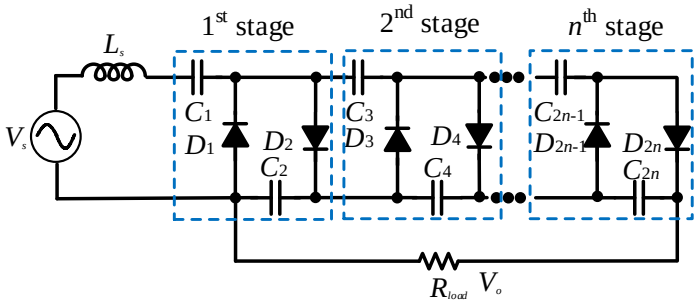



Fig. 5-1 Circuit diagram of the *n*-stage HWCW voltage multiplier circuit

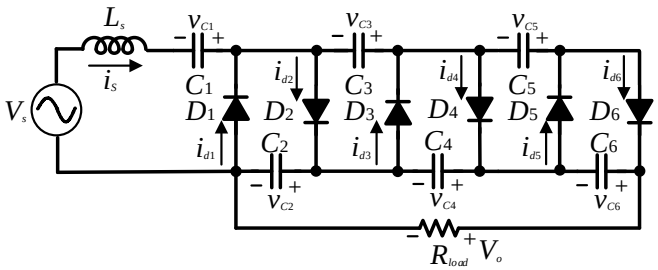



Fig. 5-2 Circuit diagram of the 3-stage HWCW voltage multiplier circuit

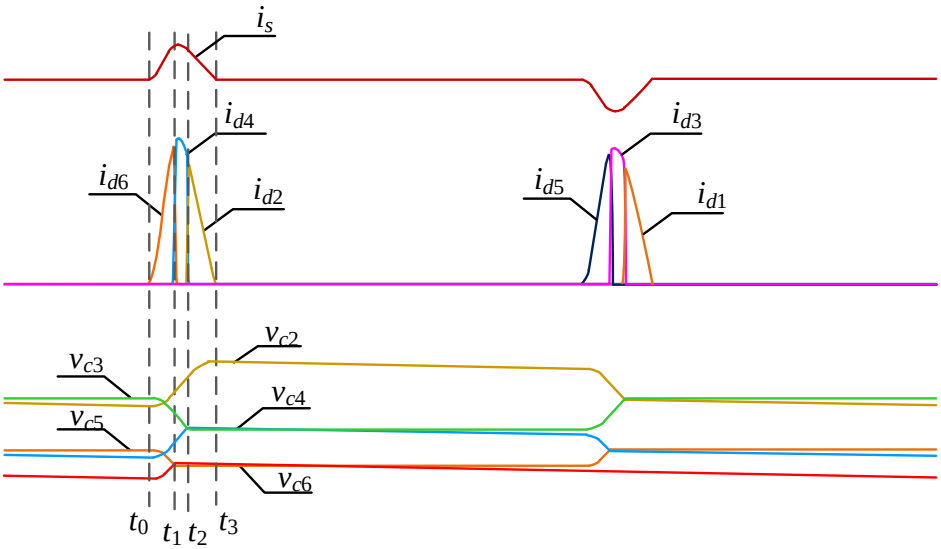



Fig. 5-3 Key waveforms for the HWCW voltage multiplier

Mode 1 (before $t_0$): In this mode, as shown in Fig. 5-4(a), $i_s$ is zero and all diodes are blocked. Capacitor $C_2$, $C_4$ and $C_6$ charge the load, while $C_1$, $C_3$ and $C_5$ are floating. At $t_0$, the voltage of even diodes is lower than that of odd diodes in the same stage, respectively. So, $v_{c2}< v_{C}$

$_{c1}+v_S$, $v_{c4}<v_{c3}$ and $v_{c6}<v_{c5}$.

Mode 2 ($t_0$~$t_1$): The equivalent circuit of this mode is shown in Fig. 5-4(b). $i_s$ is positive. As $v_{c6}<v_{c5}$ and $v_{c4}<v_{c3}$, $D_2$ and $D_4$ are still blocked and $D_6$ is conducted firstly. Odd capacitors $C_1$,

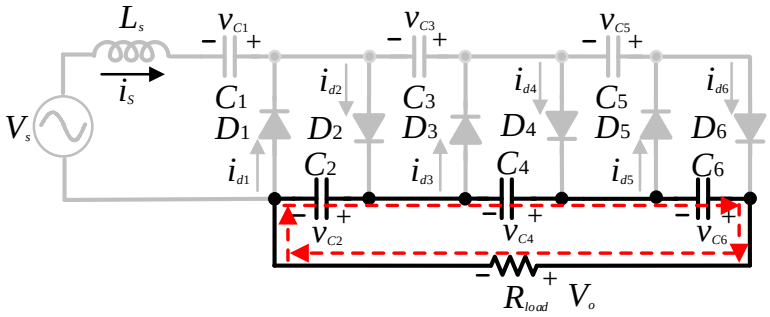
$C_3$ and $C_5$ are discharged by $i_s$ and even capacitors $C_2$, $C_4$ and $C_6$ are charged. Simultaneously, even capacitors supply the load current.

Mode 3 ($t_1$~$t_2$): The equivalent circuit of this mode is shown in Fig. 5-4(c). At $t_1$, $v_{c6}$ is equal to $v_{c5}$ and $D_6$ is blocked. $D_4$ begins to be conducted. $C_2$ and $C_4$ are charged by $i_s$, while $C_1$ and $C_3$ are discharged. Simultaneously, even capacitors supply the load current, while $C_5$ is floating.

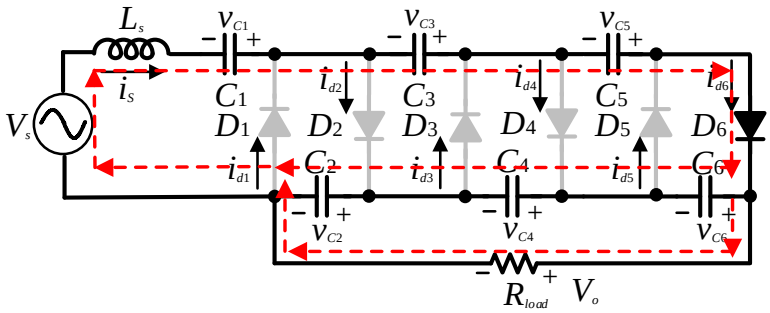
Mode 4 ($t_2$~$t_3$): The equivalent circuit of this mode is shown in Fig. 5-4(d). At $t_2$, $v_{c4}$ is equal to $v_{c3}$ and $D_4$ is blocked, while $D_2$ begins to conduct. $C_2$ is charged by $i_s$, while $C_1$ is discharged. Simultaneously, even capacitors supply the load current, while $C_3$ and $C_5$ are floating.

The circuit operation principle in the negative half cycle is similar to the positive half cycle.

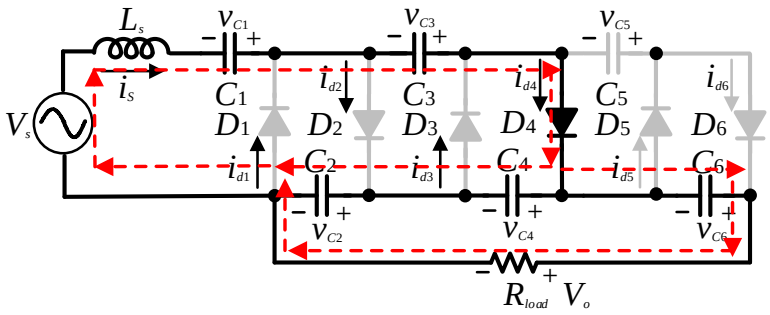
According to Fig. 5-3, in the positive half cycle of the sinusoidal voltage, only one of the even diodes conducts with the sequence $D_6$, $D_4$ and $D_2$. Similar behaviour occurs during the negative half cycle. The odd diodes conduct in the sequence $D_5$, $D_3$ and $D_1$.



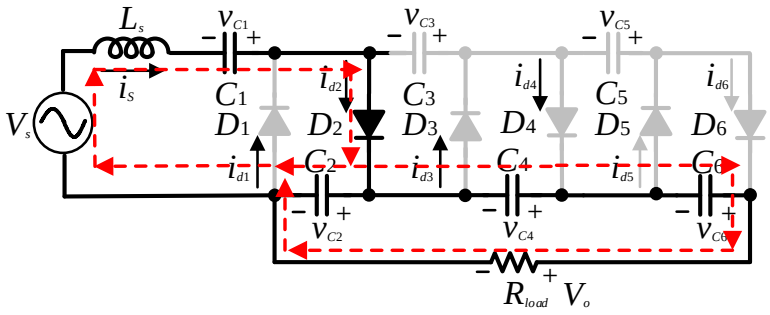

(a) Before $t_0$




(b) $t_0$~$t_1$




(c) $t_1$~$t_2$




(d) $t_2$~$t_3$

Fig. 5-4 Equivalent circuits of modes for the HWCW voltage multiplier

According to the above analysis, the following conclusions can be obtained.

(1) Only one of the diodes will conduct in a specific time frame when $i_s \neq 0$.
(2) The conducting sequence is from right to left for even diodes in a positive half cycle and odd diodes in a negative half cycle.
(3) The maximum value of $v_{C2k}$ is equal to the minimum value of $v_{C2k\text{-}1}$. Similarly, the maximum value of $v_{C2k\text{-}1}$ is equal to the minimum of $v_{C2k\text{-}2}$, where $k$ represents the $k$th stage in the HWCW voltage multiplier circuit.

At no load condition, the output voltage of the multi-stage HWCW voltage multiplier is given by

$$V_o = 2nV_s \tag{5–1}$$

where $V_S$ is the peak value of the transformer secondary winding output voltage or input voltage to the voltage multiplier and $n$ represents the total number of stages of the voltage multiplier. However, when the voltage multiplier circuit supplies the current to the loads, the voltage multiplier suffers from voltage drop and the voltage ripple appears at its output voltage.

The deduction of the HV pulse ripple in a $n$-stage HWCW voltage multiplier circuit is based on the charge flowing through the circuit. Assuming that the capacitance for each voltage multiplier stage is the same, the charge supplied to the load in a period, $Q_o$, is given,

$$Q_o = \frac{I_o}{f} \tag{5-2}$$

where $f$ is the frequency of the voltage source, $I_o$ is the load current.

If the HWCW voltage multiplier circuit is in steady state, the average charge flowing through the capacitors in a period will be zero as the capacitors voltage will not change. Then, the charge flowing through diodes is equal to $Q_o$.

$$Q_{d1} = Q_{d2} = \ldots = Q_{d2n} = Q_o = \frac{I_o}{f} \tag{5-3}$$

In steady state, the voltage of capacitors is stable. However, the voltage of capacitors will still fluctuate in a period, caused by the charge flowing into and out of the capacitors. Additionally, the charge through $k$th stage capacitors is equal to the charge through the $k$+1th stage capacitor and the charge flowing through the $k$th stage diodes. The charge through the $n$th stage capacitors is equal to $Q_o$.

$$Q_{2k-1} = Q_{2k} = Q_{2(k+1)} + Q_{d2k} \tag{5-4}$$

$$Q_{2n-1} = Q_{2n} = Q_o = \frac{I_o}{f} \tag{5-5}$$

$$Q_{2k-1} = Q_{2k} = (n - k + 1)\frac{I_o}{f} \tag{5-6}$$

So, the voltage fluctuation of the $k$th stage capacitors is:

$$\delta V_{c2k-1} = \delta V_{c2k} = (n - k + 1)\frac{I_o}{fC} \tag{5-7}$$

and the output voltage fluctuation is equal to the sum of the even capacitors voltage fluctuation:

$$\delta V_o = \sum_{k=1}^{n} \delta V_{2k} = \frac{n(\mathrm{n}+1)}{2}\frac{I_o}{fC} \tag{5-8}$$

According to the third conclusion in the operation principle section, the voltage drop of the $k$th stage even (odd) capacitor is equal to the sum of the voltage fluctuation of even (odd) capacitors in stages which are before the $k$th stage.

$$\Delta V_{2k-1} = \sum_{i=1}^{k-1} \delta V_{2i-1} = \frac{(n+k+1)(\mathrm{n}-\mathrm{k})}{2}\frac{I_o}{fC} \tag{5-9}$$

$$\Delta V_{2k} = \sum_{i=1}^{k-1} \delta V_{2i} = \frac{(n+k+1)(\mathrm{n}-\mathrm{k})}{2}\frac{I_o}{fC} \tag{5-10}$$

The output voltage drop is equal to the sum of the voltage drop of even capacitors. The output voltage drop is related to the switching frequency, the capacitance and stage number of the HWCW voltage multiplier and output current.

$$\Delta V_o = \frac{(4n^3 + 3n^2 - n)}{6} \frac{I_o}{fC} \tag{5-11}$$

The output voltage of the multi-stage HWCW voltage multiplier with load is given by

$$V_o = 2nV_S - \frac{(4n^3 + 3n^2 - n)}{6} \frac{I_o}{fC} \tag{5-12}$$

The increase of the number of the voltage multiplier stages *n* increases the no-load gain proportionally, but also increases the rate of voltage drop cubically.

If the capacitors throughout all the voltage multiplier stages are equal, the peak-to-peak HV pulse ripple of the multi-stage HWCW voltage multiplier is approximated as:

$$\delta V_{pp} = \frac{n(n+1)P_o}{2fCV_o} \tag{5-13}$$

where, $P_o$ is the output power, $V_o$ is the output voltage and $C$ is the capacitance for the voltage multiplier [5-4]-[5-5].

The output voltage ripple depends on $n^2$, which is another factor that limits the stage number of the voltage multiple besides the output voltage drop. The choices of the stage number of the voltage multiplier is a compromise between the voltage gain and the output voltage drop and ripple.

## 5.3 HV pulse rise and decay times analysis

The HV pulse rise and decay times play a critical part for HV pulse converter systems. The pulse responses are important requirements for applications such as radar systems, linear accelerators or klystron and magnetron modulators, where a nearly rectangular pulse shape is needed. The fast HV rise and decay times are also important for imaging quality and radiation dose management in CT/X-ray generator applications. It also impacts on the sparkover handling capability, efficiency, and electrodes stress for electrostatic precipitators [5-6]-[5-10]. The key characteristics and influence factors of HV pulse rise and decay times of the voltage multiplier based HV pulse converter circuits are analysed and verified in detail in the following sections.

### 5.3.1 HV pulse rise times analysis

The circuit diagram of a 2-stage HWCW voltage multiplier based LCC resonant HV pulse converter is illustrated in Fig. 5-5 as a case study. The rise time is defined as the time duration from 10% of to 90% of the full voltage rating of the HV pulse. Assume all the voltage multiplier capacitances are equal ($C_1$=$C_2$=$C_3$=$C_4$=$C$).

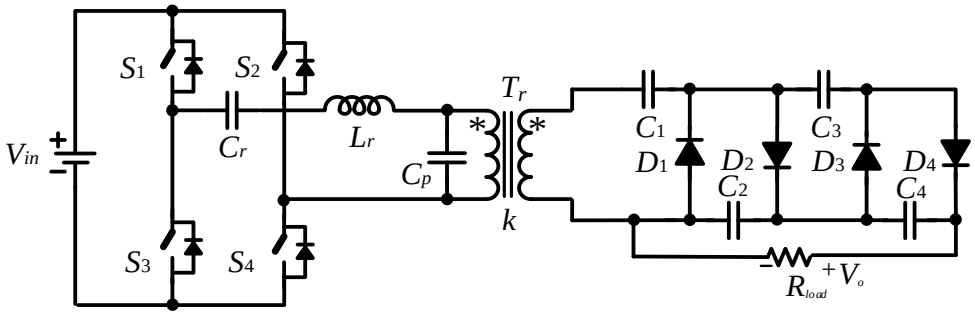



Fig. 5-5 Circuit diagram of a 2-stage HWCW voltage multiplier based HV pulse converter

The equivalent circuits for a 1-stage HWCW voltage multiplier in Fig. 5-6 at negative and positive half switching cycle are illustrated in Fig. 5-7 (a) and Fig. 5-7 (b).

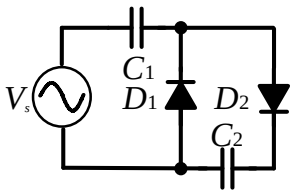



Fig. 5-6 1-stage half-wave series voltage multiplier circuit


(a) Negative half switching cycle (b) Positive half switching cycle

Fig. 5-7 Equivalent circuit for 1-stage HWCW voltage multiplier

At negative half switching cycle, $C_1$ is charged through rectifier $D_1$ to $E$ which is the peak value of the input sinusoidal supply $V_s$. Rectifier $D_2$ is blocked at this time slot. At the half switching cycle, $C_2$ is charged through rectifier $D_2$ to $E$ by input sinusoidal supply $V_s$ and $C_1$ is discharged through rectifier $D_2$ from $E$ to zero. Fig. 5-8 gives the capacitor voltage per switching cycle for a 1-stage HWCW voltage multiplier. It needs around four switching cycles for the rise times. The output voltage will finally approach to $2E$.

$$\begin{cases} V_{C2}(0+) - V_{C1}(0+) = E \\ V_{C1}(0+) = V_{C1}(0-) - \dfrac{1}{C}\int_{t_{0-}}^{t_{0+}} i_C(t)dt \\ V_{C2}(0+) = V_{C2}(0-) + \dfrac{1}{C}\int_{t_{0-}}^{t_{0+}} i_C(t)dt \end{cases} \tag{5-14}$$

| | Cycle 1 | | Cycle 2 | | Cycle 3 | | Cycle 4 | | Cycle 5 | | Cycle 6 | | Cycle * | | Cycle *n* | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | N | P | N | P | N | P | N | P | N | P | N | P | N | P | N | P |
| $V_{C1}$ | *E* | 0 | *E* | *E*/2 | *E* | 3*E*/4 | *E* | 7*E*/8 | *E* | 15*E*/16 | *E* | 31*E*/32 | | | *E* | $\frac{2^{n-1}-1}{2^{n-1}}E$ |
| $V_{C2}$ | 0 | *E* | *E* | 3*E*/2 | 3*E*/2 | 7*E*/4 | 7*E*/4 | 15*E*/8 | 15*E*/8 | 31*E*/16 | 31*E*/16 | 63*E*/32 | | | $\frac{2^{n-1}-1}{2^{n-2}}E$ | $\frac{2^{n}-1}{2^{n-1}}E$ |

Fig. 5-8 Capacitor voltage per switching cycle for a 1-stage HWCW voltage multiplier

Similarly, the HV pulse rise times are investigated for the 2-stage HWCW voltage multiplier circuits in Fig. 5-9. The equivalent circuits for a 2-stage HWCW voltage multiplier at the negative and positive half switching cycles are illustrated in Fig. 5-10 (a) and Fig. 5-10 (b).

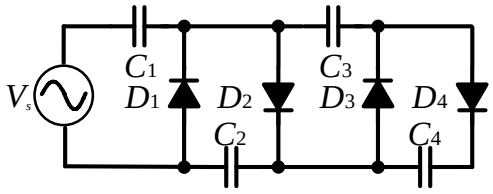
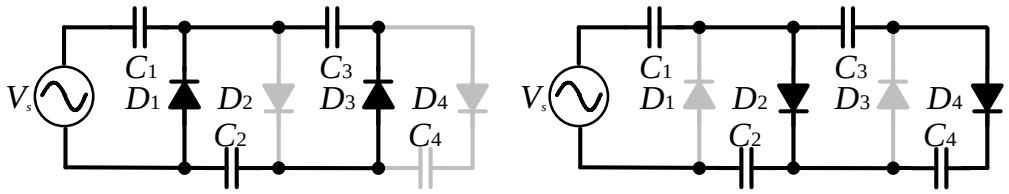



Fig. 5-9 2-stage HWCW voltage multiplier circuits




(a) Negative half switching cycle (b) Positive half switching cycle

Fig. 5-10 Equivalent circuit for a 2-stage HWCW voltage multiplier

At the first negative half switching cycle, $C_1$ is charged through rectifier $D_1$ to $E$ by input voltage $V_s$. At the first positive half switching cycle, $C_2$ is charged through rectifier $D_2$ to $E$ by input voltage $V_{ac}$ and $C_1$ is discharged through rectifier $D_2$ from $E$ to zero. At the next negative switching cycle, $C_1$ is charged through rectifier $D_1$ to $E$ by input voltage $V_{ac}$. $C_3$ is charged through rectifier $D_3$ to 0.5$E$, and $C_2$ is discharged through rectifier $D_3$ from $E$ to 0.5$E$. At the next positive switching cycle, $C_2$ is charged through rectifier $D_2$ to 1.25$E$ by input voltage $V_s$ and $C_1$ is discharged through rectifier $D_2$ from $E$ to 0.25 $E$. At the same time, $C_3$ is discharged through rectifier $D_4$ from 0.5$E$ to 0.25$E$ and $C_4$ is charged through rectifier $D_4$ from *0* to 0.25 $E$. The capacitor voltage per switching cycle for a 2-stage half-wave series voltage multiplier can be derived in equation (5-15) and (5-16). The capacitor voltage per switching cycle for a 2-stage half-wave series voltage multiplier is shown in Fig. 5-11. It needs around twenty switching cycles for the rise times, though the exact expression is difficult to achieve. The output voltage will finally near 4$E$.

$$\begin{cases} V_{C2}(0+) = V_{C3}(0+) \\ V_{C2}(0+) + V_{C3}(0+) = V_{C2}(0-) + V_{C3}(0-) \end{cases} \tag{5-15}$$

$$\begin{cases} V_{C2}(0+) - V_{C1}(0+) = E \\ V_{C2}(0+) + V_{C1}(0+) = V_{C1}(0-) + V_{C2}(0-) \\ V_{C3}(0+) = V_{C4}(0+) \\ V_{C3}(0+) + V_{C4}(0+) = V_{C3}(0-) + V_{C4}(0-) \end{cases} \tag{5-16}$$

| | Cycle 1 | | Cycle 2 | | Cycle 3 | | Cycle 4 | | Cycle 5 | | Cycle 6 | | Cycle * | | Cycle $n \to \infty$ | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | N | P | N | P | N | P | N | P | N | P | N | P | N | P | N | P |
| $V_{C1}$ | $E$ | 0 | $E$ | $E/4$ | $E$ | $3E/8$ | $E$ | $15E/32$ | $E$ | $35E/64$ | $E$ | $157E/256$ | | | $\approx E$ | |
| $V_{C2}$ | 0 | $E$ | $E/2$ | $5E/4$ | $3E/4$ | $11E/8$ | $15E/16$ | $47E/32$ | $35E/32$ | $99E/64$ | $157E/128$ | $413E/256$ | | | $\approx 2E$ | |
| $V_{C3}$ | 0 | 0 | $E/2$ | $E/4$ | $3E/4$ | $E/2$ | $15E/16$ | $23E/32$ | $35E/32$ | $29E/32$ | $157E/128$ | $273E/256$ | | | $\approx 2E$ | |
| $V_{C4}$ | 0 | 0 | 0 | $E/4$ | $E/4$ | $E/2$ | $E/2$ | $23E/32$ | $23E/32$ | $29E/32$ | $29E/32$ | $273E/256$ | | | $\approx 2E$ | |
| $V_o$ | 0 | 0 | $E/2$ | $3E/2$ | $E$ | $15E/8$ | $23E/16$ | $35E/16$ | $29E/16$ | $157E/64$ | $273E/128$ | $343E/128$ | | | $\approx 4E$ | |

Fig. 5-11 Capacitor voltage per switching cycle for a 2-stage HWCW voltage multiplier

Fig. 5-12 to Fig. 5-14 provide the HV pulse rise time simulation result with several influence factors such as switching frequency, output load and capacitance for a 2-stage HWCW voltage multiplier. The input voltage of a voltage multiplier is $V_s$=10kV (peak value). Fig. 5-12 shows the HV pulse rise times simulation results with switching frequency $f_s$=300kHz and $f_s$=30kHz, output load $R_L$=400kΩ and voltage multiplier capacitance $C$=300pF. From simulation results, the rise times are about twenty switching cycles for a 2-stage HWCW voltage multiplier circuit. The HV pulse rise times simulation results match with analytical calculation. It is obvious that a higher switching frequency will lead to shorter rise times.

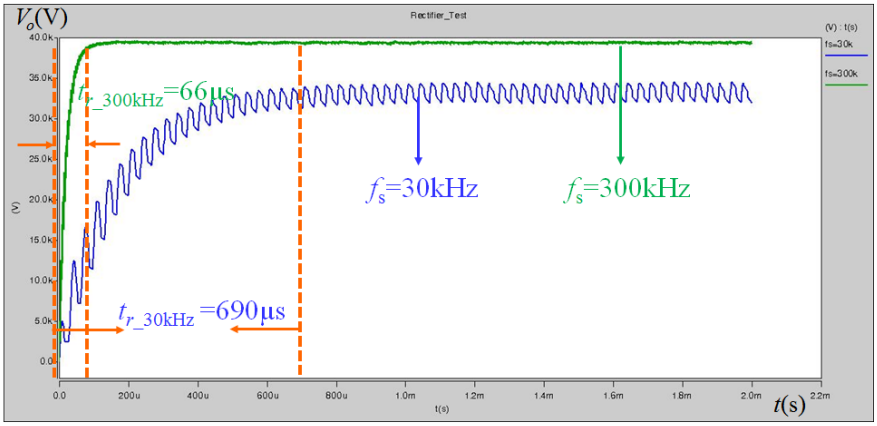



Fig. 5-12 HV pulse rise times simulation results at different switching frequencies for a 2-stage HWCW voltage multiplier

Fig. 5-13 illustrates HV pulse rise times simulation results with switching frequency $f_s$=300kHz, voltage multiplier capacitance $C_1$=$C_2$=$C_3$=$C_4$=$C$=300pF, output load $R_{Load}$=400kΩ ($I_o$=100mA) and $R_{Load}$=4MΩ ($I_o$=10mA). Rise times have little to do with load resistance.

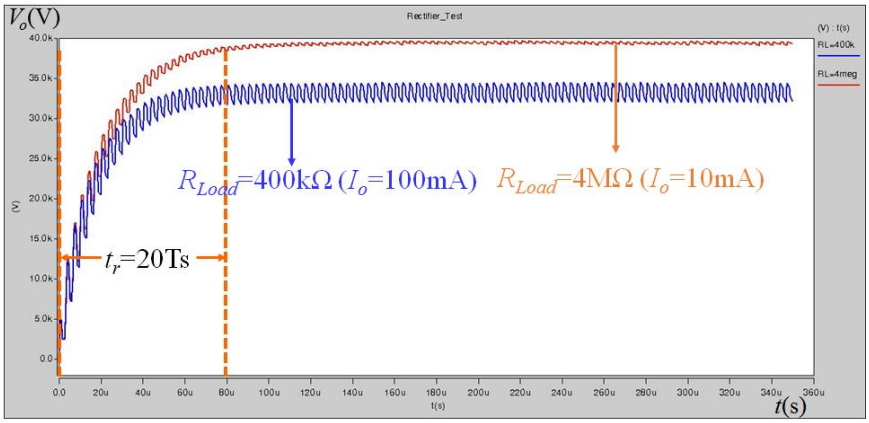



Fig. 5-13 HV pulse rise time simulation results at different loads for a 2-stage HWCW voltage multiplier

Fig. 5-14 gives the HV pulse rise times simulation results with switching frequency $f_s$=300kHz, output load $R_{Load}$=400kΩ and voltage multiplier capacitance $C_1$=$C_2$=$C_3$=$C_4$=$C$=300pF and $C_1$=$C_2$=$C_3$=$C_4$=$C$=600pF. When there is no limitation for the input current (assuming sufficient energy for voltage multiplier), the output capacitor has little influence on the HV pulse rise. However, when the input current or energy is limited for a voltage multiplier, short rise times can be achieved with smaller output capacitors.

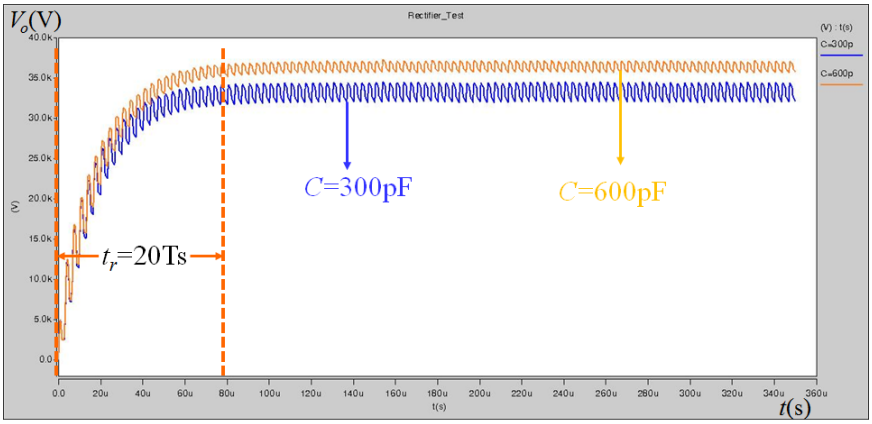



Fig. 5-14 HV pulse rise times simulation results with different capacitance values for a 2-stage HWCW voltage multiplier

In summary, the stage number of the voltage multipliers and the switching frequencies are key influence factors for the HV pulse rise times. HV pulse rise times are about four switching cycles for a HWCW voltage multiplier circuit. HV pulse rise times are around twenty switching cycles for a 2-stage HWCW voltage multiplier. The HV pulse rise times will lengthen when more stages voltage multiplier circuits are used. The voltage rating of the HV transformer and stage number of the voltage multiplier need to be considered for optimal system performance. When the stage number of the voltage multiplier is determined, the switching frequency is the key influence factor for the HV pulse rise times. Higher switching frequency will lead to shorter HV pulse rise times. Assuming the inverter power capability is sufficient, the load resistance

and filter capacitor have little influence on the HV pulse rise times according to the simulation results.

### 5.3.2 HV pulse decay times analysis

The HV pulse decay process of the 2-stage HWCW voltage multiplier based HV pulse converter in Fig. 5-15 can be divided into three stages in Fig. 5-16. The decay times are defined as the time duration from full rating HV pulse voltage to 10% of the full rating HV pulse voltage.

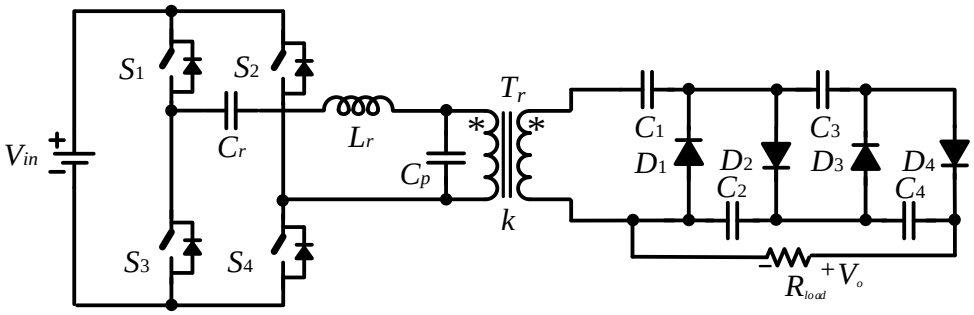
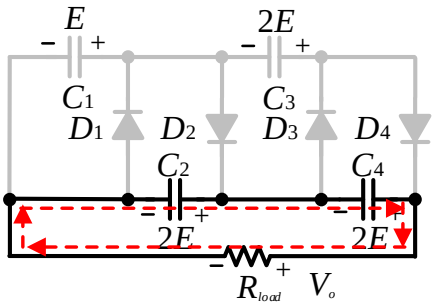
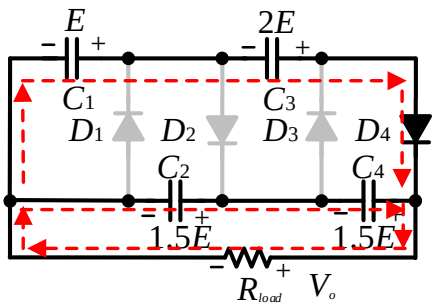


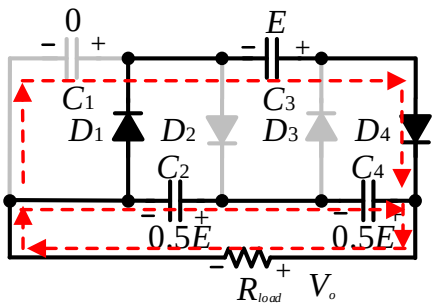

Fig. 5-15 Circuit diagram of a 2-stage HWCW voltage multiplier based HV pulse converter




(a) stage 1




(b) stage 2




(c) stage 3

Fig. 5-16 Equivalent circuits of the HV pulse decay process for a 2-stage HWCW voltage multiplier ($C_1$=$C_2$=$C_3$=$C_4$=$C$)

Stage 1: $C_2$ and $C_4$ discharge to supply the load. The voltages of $C_2$ and $C_4$ decrease from $2E$ to $1.5E$. The output voltage $V_o$ decreases from $4E$ to $3E$.

Stage 2: After the voltage of $C_2$ and $C_4$ decrease from 2$E$ to 1.5$E$, $D_4$ starts to conduct. $C_1$ and $C_3$ together while $C_2$ and $C_4$ discharge in parallel until the voltage of $C_1$ reaches zero. At this state, $V_{C2}$= $V_{C3}$=0.5$E$, $V_{C4}$=$E$.

Stage 3: $D_1$ starts to conduct, $C_2$ and $C_4$ are in parallel with $C_3$ to discharge to near zero, 10% of the full rating HV pulse voltage.

Table 5-1 summarizes the time constant and time duration for each stage of the 2-stage HWCW voltage multiplier. $t_3$ is the time interval during which $V_o$=$E$ reduce to 0.4$E$ (10%). The time from 0.4$E$ to zero can be expressed as another time variable, $t_4$, for example. The total fall time from full rating HV pulse voltage to 10% of the full rating HV pulse voltage is:

$$t_f = t_1 + t_2 + t_3 = 2.61 R_L C \tag{5-17}$$

Table 5-1 HV pulse decay times for each stage in a 2-stage voltage multiplier ($C_1$=$C_2$=$C_3$=$C_4$=$C$)

| | $V_o$ | Time constant | Time |
|---|---|---|---|
| Stage 1 | 4$E$→3$E$ | $\lambda$=$C$*$R_L$/2 | $t_1$ =-$ln$(3/4)*$\lambda$=0.14$R_LC$ |
| Stage 2 | 3$E$→$E$ | $\lambda$=$C$*$R_L$ | $t_2$ =-$ln$(1/3)*$\lambda$=1.10$R_LC$ |
| Stage 3 | $E$→2/5$E$*(10% of rated HV pulse voltage* | $\lambda$=3$C$*$R_L$/2 | $t_3$ =-$ln$(2/5)*$\lambda$=1.37$R_LC$ |

For the $n$-stage voltage multiplier, the total decay times can be expressed as:

$$t_f = t_1 + t_2 + t_3 = \left[ -\frac{1}{n}\ln\frac{2n-1}{2n} - \frac{2}{n}\ln\frac{n-1}{2n-1} - \frac{2n-1}{n(n-1)}\ln\frac{0.2n}{n-1} \right] R_L C \tag{5-18}$$

The first stage voltage multiplier capacitance is chosen to be larger than other stages in order to achieve the low pulse ripple ($C_1 \neq C_2=C_3=C_4=C$) for some industrial applications. Taking $C_1$=4$C$, $C_2$=$C_3$=$C_4$=$C$ as an example study, the four operation stages in Fig.5-17 are slightly different from the previous case with equal voltage multiplier capacitance.

Stage 1 and stage 2 with $C_1 \neq C_2=C_3=C_4=C$ are the same as the stage with $C_1$=$C_2$=$C_3$=$C_4$=$C$.

Stage 3: $D_2$ starts to conduct when the voltage of $C_1$, $C_2$, $C_3$ and $C_4$ decrease to 2$E$/3.
Stage 4: $D_4$ starts to conduct when the voltage of $C_3$ and $C_4$ decrease to zero. $C_1$, in parallel with $C_2$, discharges to supply the load until the voltages of $C_3$ and $C_4$ decrease to zero.

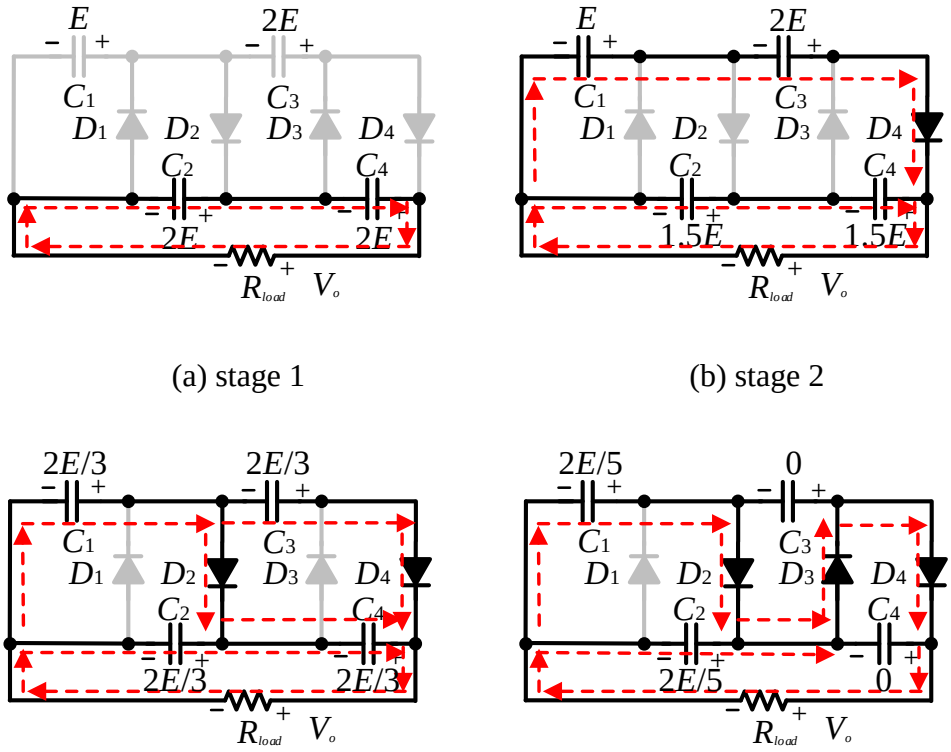
**T**able 5-2 HV pulse decay times for each stage in a 2-stage HWCW voltage multiplier ($C_1 \neq C_2=C_3=C_4=C$)

| | Vo | Time constant | Time |
|---|---|---|---|
| Stage 1 | 4E→3E | $\lambda$=$C$*$R_L$/2 | $t_1$ =-$ln$(3/4)*$\lambda$=0.14$R_LC$ |
| Stage 2 | 3E→4E/3 | $\lambda$=1.3$C$*$R_L$ | $t_2$=-$ln$(4/9)*$\lambda$=1.01$R_LC$ |
| Stage 3 | 4E/3→2E/5 | $\lambda$=10$C$*$R_L$/7 | $t_3$ =-$ln$(3/10)*$\lambda$=1.72$R_LC$ |

The summarized time constant and decay times can be found in Table 5-2. $V_o$ is reduced from 4$E$ to 0.4$E$ (10%). This time slot can be defined as the decay times. The time duration of stage

4 is not included in to the total decay time since the output voltage has already decreased to 10% of the rated output HV pulse voltage.

$$t_f = t_1 + t_2 + t_3 = 2.87 R_L C \tag{5-18}$$




(a) stage 1 (b) stage 2

(c) stage 3 (d) stage 4

Fig. 5-17 Equivalent circuits of the HV pulse decay process for a 2-stage HWCW voltage multiplier($C_1 \neq C_2 = C_3 = C_4 = C$)

Fig. 5-18 shows the decay times simulation results with $V_{in}$=10kV (peak); $f_s$=300kHz; $R_L$=400kΩ; $C$=300pF. The simulation times match with calculation results in Table 5-3.

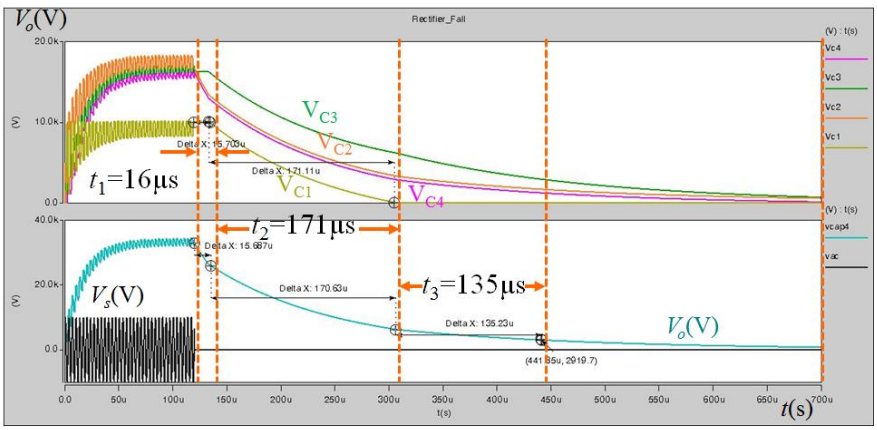



Fig. 5-18 HV pulse decay times simulation results for 2-stage HWCW voltage multiplier

Table 5-3 HV pulse decay times calculation and simulation comparison ($C_1$=$C_2$=$C_3$=$C_4$=$C$)

| | $t_1$ | $t_2$ | $t_3$ | $t_{otal}$ |
|---|---|---|---|---|
| Calculated | 17μs | 132μs | 165μs | 314μs |
| Simulated | 16μs | 171μs | 135μs | 322μs |

Fig. 5-19 and Fig. 5-20 give the HV pulse decay times simulation for different values of load and capacitance. The pulse peak voltage is $V_s$=10kV, the switching frequency is $f_s$=300kHz. The load values are $R_{load}$=400kΩ and $Rl_{oad}$=1.2MΩ. The capacitance values are $C_1$=$C_2$=$C_3$=$C_4$=$C$=300pF and $C_1$=$C_2$=$C_3$=$C_4$=$C$=900pF. From the simulation results, the decay time is proportional to the load resistance and proportional to the voltage multiplier capacitance. The HV pulse decay times lengthen when the voltage multiplier capacitance and load resistances increase.

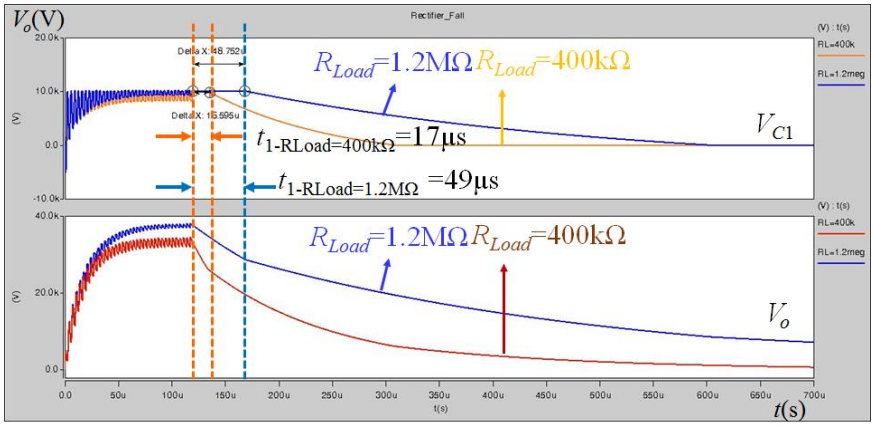



Fig. 5-19 HV pulse decay times simulation results at different loads for a 2-stage HWCW voltage multiplier ($V_s$=10kV peak; $f$s=300kHz; $C_1$=$C_2$=$C_3$=$C_4$=$C$=300pF)

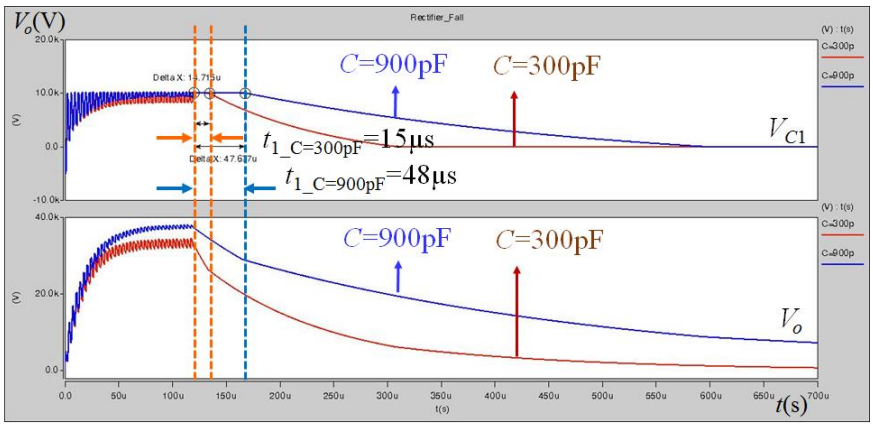



Fig. 5-20 HV pulse decay times simulation results at different capacitances for a 2-stage HWCW voltage multiplier

To summarize, the decay times are proportional to the load resistance and voltage multiplier capacitance. There is no direct relationship between the switching frequency and decay times. Lower voltage multiplier capacitance can be used at higher switching frequency, which yields

shorter decay times. As a result, both the HV pulse rise times and decay times can be effectively improved by increasing the switching frequency for the HWCW voltage multiplier.

### 5.3.3 Experimental verifications

To verify the HV pulse rise and decay times' analysis and simulation, experiments are performed on a 400VDC input, 35kVDC output, 500W HV pulse converter circuit prototype with a 2-stage HWCW voltage multiplier shown in Fig.5-21. The load value is $R_{Load}$=2.45MΩ, and the capacitance values are $C_{11}$=$C_{12}$=1.2nF, $C_{13}$=$C_{15}$=$C_{17}$=$C_{14}$=$C_{16}$=$C_{18}$=0.3nF. $C_r$=35.4nF, $L_r$=37.3nF, $L_m$=850μH, transformer turns ratio is 7:125, $C_p$=17.9nF. From the experimental and simulation results in Fig.5-22 and Fig.5-23, the rise times are around 400μs at 300kHz switching frequency. The experimental HV pulse decay times are 250339μs which is close to the HV pulse decay time from simulation results. The HV pulse decay times of experimental and simulation results match each other. The error between the experimental and simulation results are due to the circuit parasitic components stray capacitances.

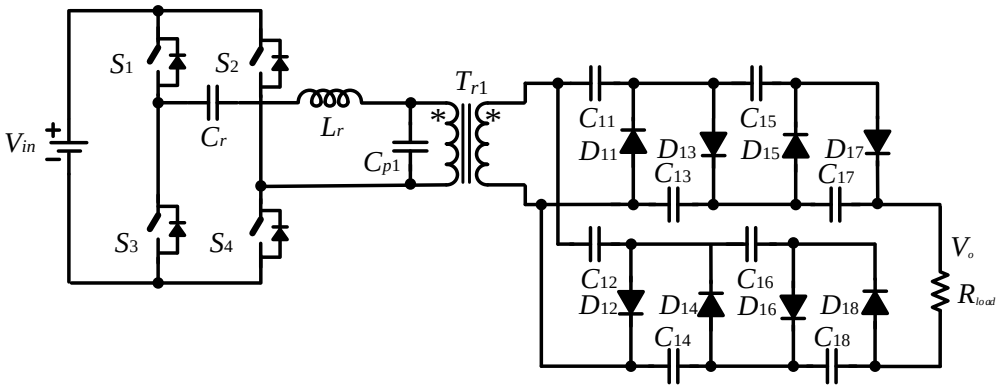
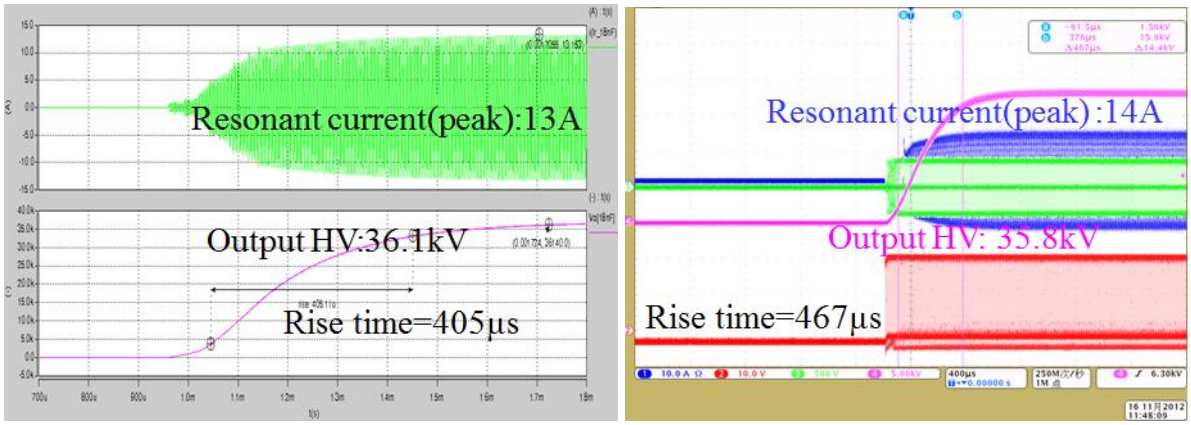
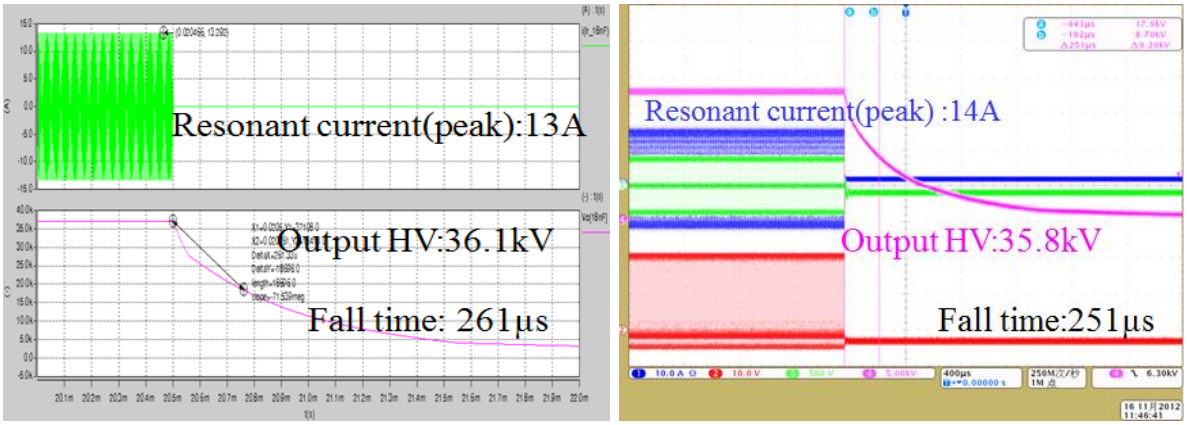



Fig. 5-21 Circuit diagram for 35kVDC output, 500W HV pulse converter circuit prototype with a 2-stage HWCW voltage multiplier




(a) rise times simulation result (b) rise times experimental result

Fig. 5-22 HV pulse rise times simulation and experimental results




(a) decay times simulation result (b) decays time experimental result

Fig. 5-23 HV pulse decay times simulation and experimental results

### 5.3.4 HV pulse rise and decay times experimental results from technology demonstrators

*A. HV pulse rise and decay times experimental results from a 2kW 110kV HV pulse converter technology demonstrator*

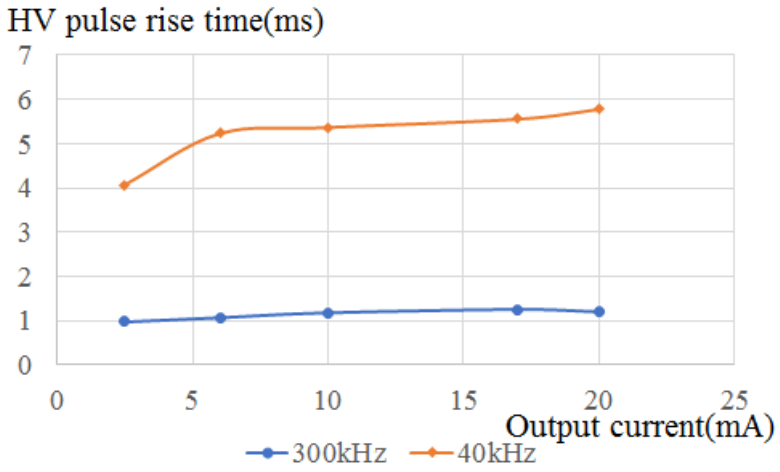



Fig. 5-24 Pulse rise times for 40kHz and 300kHz 2kW 110kV HV pulse converter prototypes

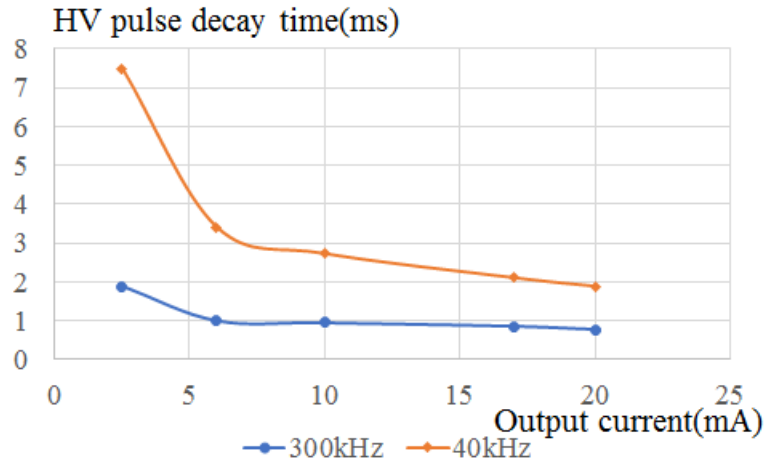


Fig. 5-25 Pulse decay times for 40kHz and 300kHz 2kW 110kV HV pulse converter prototypes

The technology demonstrator of a 2kW output power, 110kV output voltage and 300kHz switching frequency HV pulse converter based on the modular HV architecture with modular HV transformers and a 3-stage voltage multiplier is built in the laboratory to demonstrate the advantages of HV pulse response compared with the conventional 40kHz HV pulse generator. Detailed parameters of the technology demonstrator can be found in the Appendix. From experimental results in Fig. 5-24 and Fig. 5-25, the 300kHz modular design can achieve the following advantages compared with the 40kHz legacy design:

- About five times shorter HV pulse rise times
- About three times shorter HV pulse decay times
- About seven times size reduction for the HV rectifier board
- 5~10% higher efficiency higher efficiency for the HV pulse converter

*B. HV pulse rise and decay times experimental results from an 8kW 110kV HV pulse converter technology demonstrator*

With a higher output current and out power for a high frequency HV pulse converter, the power loss of a multi-stage voltage multiplier will increase. The stage number of a voltage multiplier is reduced from three to two at 8kW power compared with the 2kW HV pulse converter. A 300kHz 8kW 110kV HV pulse converter prototype based on the modular HV architecture with modular HV transformers and a 2-stage voltage multiplier is built in the laboratory to validate the advantages of shorter rise and decay times compared with the conventional 40kHz 8kW 110kV HV pulse converter. The experimental results of HV pulse rise and decay times at 300kHz and 40kHz are given in Fig. 5-26 and Fig. 5-27. Compared with the 40kHz design, the 300kHz modular design behaves with the following advantages on HV pulse response, size reduction and efficiency improvement.

- About three times shorter HV pulse rise times
- About nine times shorter kV decay times at light load, two-three times shorter kV decay times at other loads
- About five times size reduction for voltage multiplier boards
- 5~10% higher efficiency for the HV pulse converter

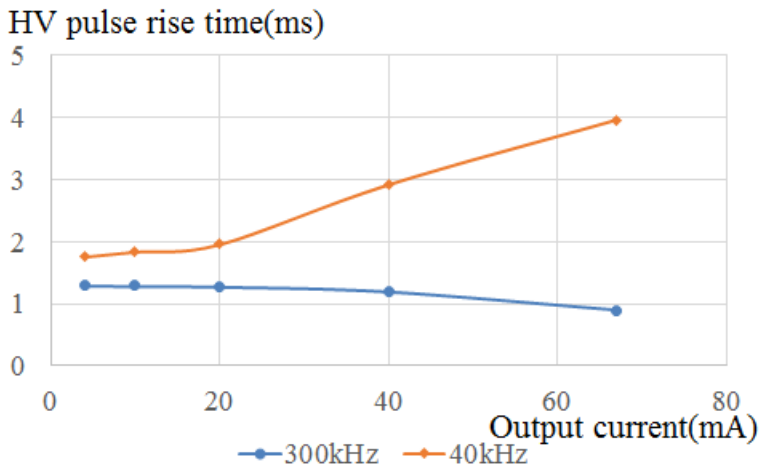



Fig. 5-26 HV pulse rise times experimental results of 40kHz and 300kHz 8kW 110kV HV pulse converter prototypes

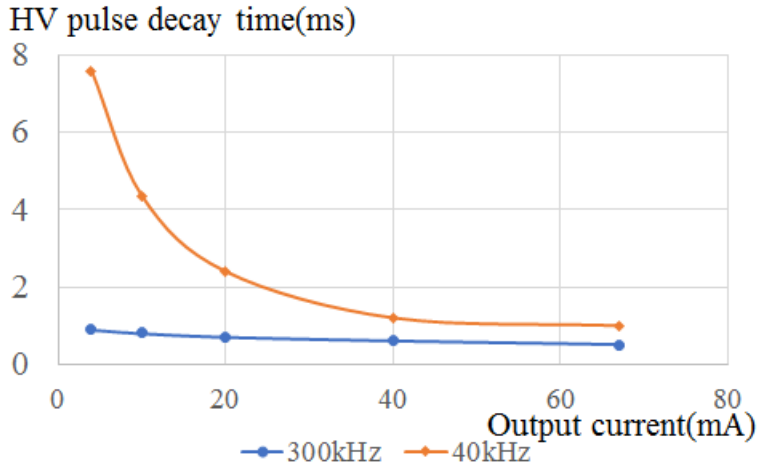



Fig. 5-27 HV pulse decay times experimental results of 40kHz and 300kHz 8kW 110kV HV pulse converter prototypes

### 5.3.5 Practical design guidelines

Based on the above analysis, simulation and experimental study of HV pulse rise and decay times, the practical design guidelines are recommended to achieve the desired HV pulse rise and decay times for the HV pulse converter based on a voltage multiplier. It is assumed that there is only a single HV transformer and single half-wave series voltage multiplier circuit in the HV pulse converter (multiple transformers and multiple multiplier circuits are not included in the scope). The input and output voltages for the voltage multiplier, load profiles are defined. Assume that the input current has no limitation, then sufficient energy can be provided for voltage multiplier circuit. The following parameters need to be determined for the circuit design:

(1) Determine the stage number of the voltage multiplier according to the requirements of input and output voltage and high frequency HV transformer maximum output voltage.

(2) Determine the capacitance of the voltage multiplier according to the HV pulse decay times.

(3) Determine the switching frequency based on voltage multiplier capacitance and HV pulse ripple.

(4) Check if the switching frequency and stage number of the voltage multiplier can meet the high voltage pulse rise time. If not, increase the switching frequency. But the high frequency insulation stress, high frequency dielectric loss of HV transformer and high frequency loss for voltage multiplier should be taken into consideration. The pulse rise, decay times and power loss at high frequency need study for the optimal trade-off.

## 5.4 Diode reverse recovery process analysis for voltage multiplier

The fundamental operational principle and reverse recovery problems of the HWCW voltage multiplier circuit at high switching frequency have not yet been investigated in the state-of-the-art works [5-11]-[5-17]. The voltage multiplier diode reverse recovery problem is mainly caused by the diodes in the first stage voltage multiplier. The multiplier diode reverse recovery problem is the bottle neck of further increasing the circuit operation switching frequency to achieve high power density, HV pulse with short rise and decay times [5-17].

### 5.4.1 Diode reverse recovery in voltage multiplier circuit

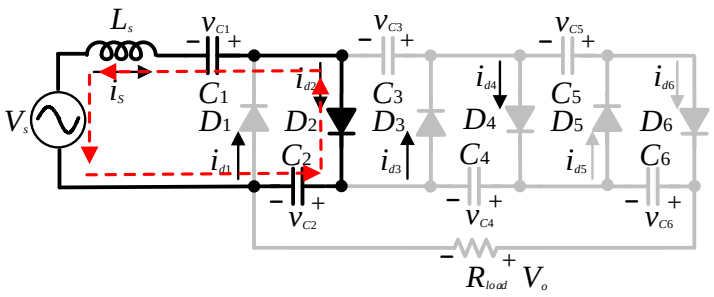
The analysis above is based on the ideal diode model. However, if the actual diode model is taken into considerations, the reverse recovery of the diodes should not be neglected. Because of the different circuit conditions, the switching process of the diodes in the first stage and the diodes in the other stages are different. So, these will be analysed separately.

*A. Reverse recovery procedure of diodes in the first stage multiplier circuit*

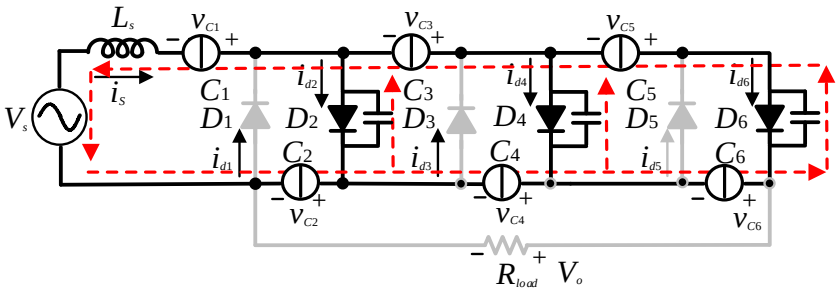
$D_2$ is taken as an example for the analysis in the positive half cycle. The current flowing through $D_2$, which is equal to $i_s$, decreases to zero at $t_3$ in mode 3, and then $D_2$ is blocked. The equivalent circuits for stage 1 and stage 2 are illustrated in Fig. 5-28 respectively. The waveform of $i_{d2}$ with the actual diode model is shown in Fig. 5-29. Before $t_3$, the working process is the same. Beyond $t_3$, the working process is analysed in two stages.

Stage 1 ($t_3$~$t_4$): In this stage, the equivalent circuit is as shown in Fig. 5-28(a). To eliminate the minor carrier stored in $D_2$, the $i_{d2}$ continues to increase reversely after $t_3$. The slope of $i_{d2}$ in this stage is determined by the voltage across the inductor $L_s$. The voltage across $i_{d2}$ is zero in this stage. At $t_4$, this stage is completed when all minor carriers are eliminated.

Stage 2 ($t_4$~$t_5$): Beyond $t_4$, the inductor $L_s$, with the initial current value $i_{s1}$, begins to resonate with the parasitic capacitors of the diodes. The equivalent resonant circuit is as shown in Fig. 5-28(b). Compared to diodes parasitic capacitors, capacitors $C_1$~$C_6$ are very large and the voltage can be regarded as constant during the resonant period. They are modeled as constant voltage sources. The resonance will not complete until $t_5$, when $D_5$ conducts.




(a) stage-1




(b)stage 2

Fig. 5-28 Equivalent circuit for multiplier stages 1 and 2

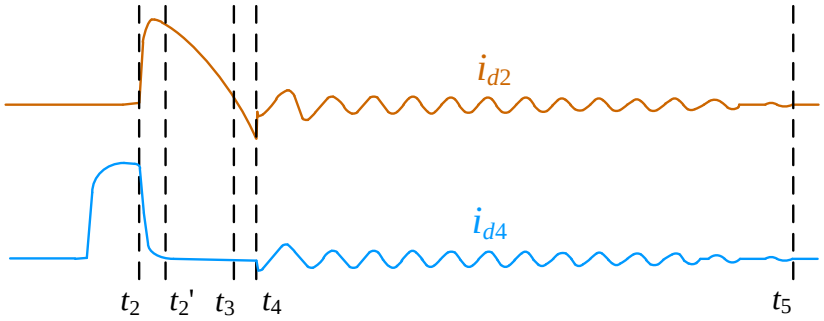



Fig. 5-29 The actual waveforms of $i_{d2}$ and $i_{d4}$

*B. Reverse recovery procedure of diodes in the other stages*

In mode 3, when $v_{C3}$ equals $v_{C4}$ at $t_3$, $D_4$ is blocked and $D_2$ begins to conduct. However, with the actual diode model, the waveform of $i_{d4}$ is as shown in Fig. 5-29. The equivalent circuit for diodes in other voltage multiplier stages is as shown in Fig. 5-30.

At $t_2$', $i_{d4}$ decreases to zero. According to the model, the voltage across $D_4$ is equal to $V_d$ as $v_{C4}$ ($v_{C3}$) stops to increase (decrease) after $t_2$'. $D_4$ is not blocked although $i_{d4}$ is zero.

Beyond $t_3$, the diode parasitic capacitor begins to resonate with $L_s$, and $D_4$ begins to be blocked. However, as $i_{d4}$ was zero, zero current turn-off is realized for $D_4$ and there is no reverse recovery loss. Similarly, ZCS is also realized for $D_6$.

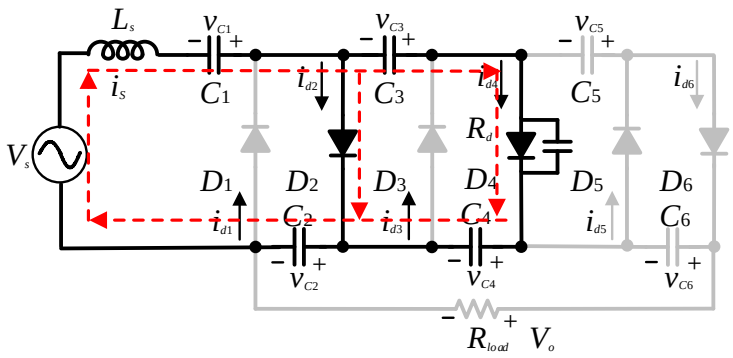



Fig. 5-30 The equivalent circuit for diodes in other multiplier stages

According to the analysis above, some conclusions can be obtained:

1) The reverse recovery in the HWCW voltage multiplier circuit is contributed by the diodes in the first stage. There is no reverse recovery for diodes in the other stages.

2) The resonant process is mainly influenced by the reverse recovery of the diodes in the first stage. So, the reverse recovery problem in the HWCW voltage multiplier circuit depends on the performance of the diodes in the first stage.

### 5.4.2 Experimental results

Based on the above analysis and simulations study, the hardware prototype of a 3-stage HWCW voltage multiplier circuit with the positive side voltage multiplier circuit is built in the laboratory to validate the concept. The key parameters for the voltage multiplier circuit prototype is provided in Table 5-4.

Table 5-4 Key parameters for voltage multiplier circuit prototype

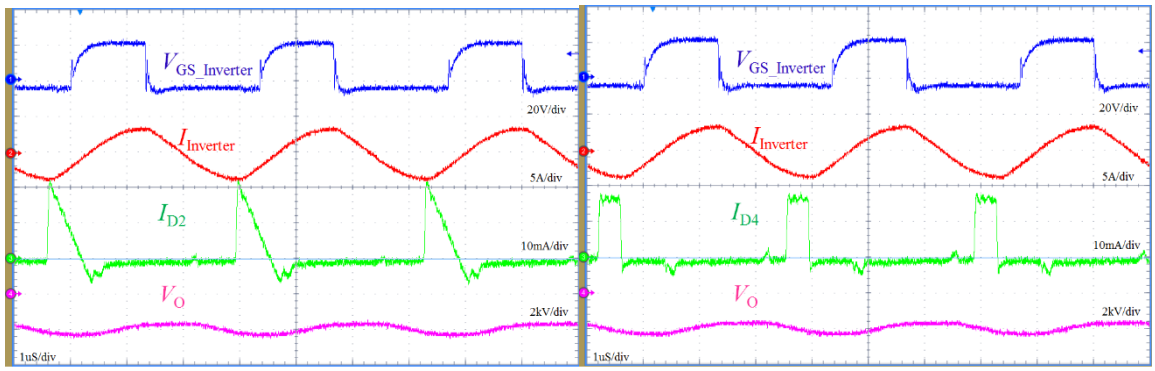
| Items | Key parameters |
|---|---|
| Input voltage | 50VAC |
| Output voltage | Around 2kVDC |
| Output power | 30W |
| Switching frequency | 300kHz |
| Multiplier diode | Silicon diode: BYV26E (1kV, 1A), 2 in series for each multiplier stage diode unit<br>Silicon carbide diode: GB01SLT12(1.2kV, 1A), 2 in series for each multiplier stage diode unit |
| Multiplier capacitance | 0.47nF, 3kV ceramic capacitor |

The input voltage is 50VAC with 300kHz frequency. The output voltage is 2kVDC and the output power is around 30W. The silicon diode BYV26E and silicon carbide diodes are adopted in the first stage diode $D_2$, $D_4$ and $D_6$ for three stages voltage multiplier circuit respectively. The second and third stage diode $D_4$ and $D_6$ are all silicon diodes. Two diodes are connected in series for each multiplier stage diode unit.

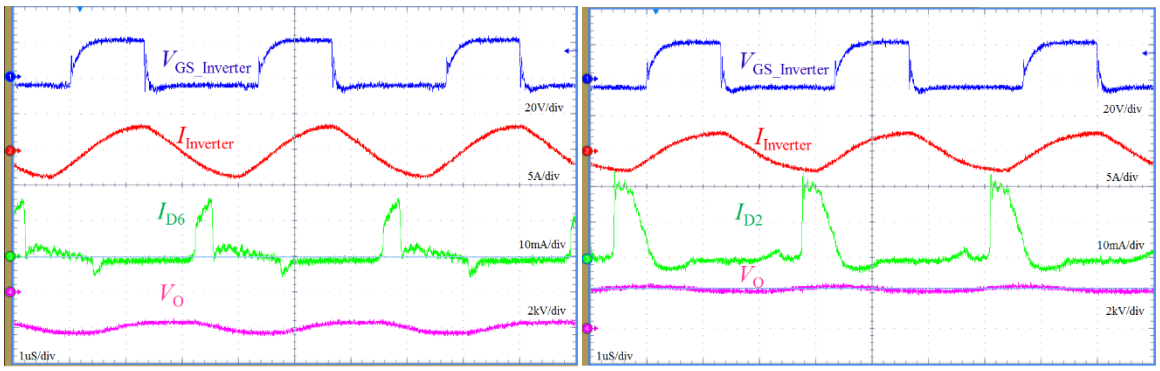
The key experimental waveforms of the first, second and third stage diodes $D_2$, $D_4$ and $D_6$ for the three stages CW voltage multiplier circuit with all silicon rectifiers BYV26E are shown in

Fig. 5-31 (a), (b) and (c) respectively. The reverse recovery current can only be found from the first stage silicon diode $D_2$. There are no reverse recovery currents for the second and third stage diode $D_4$ and $D_6$. The experimental results validate the analysis.

The key waveforms of the first stage diode $D_2$ with a silicon carbide Schottky diode GB01SLT12 for a 3-stage CW voltage multiplier circuit with all are shown in Fig.5-31 (d). The second and third stage diodes $D_4$ and $D_6$ are silicon diodes. According to the experimental waveforms, there is no reverse recovery current for the first stage silicon carbide diode $D_2$. The reverse current for the first stage silicon carbide diode $D_2$ is due to the resonance of diode junction capacitance with the circuit parasitical inductance for the voltage multiplier circuit. The reverse current for the first stage silicon carbide diode $D_2$ can be reduced with lower circuit parasitical inductance and smaller diode junction capacitance. The silicon carbide Schottky diode without reverse recovery used only in the first stage of voltage multiplier circuit can effectively mitigate the reverse recovery problems in a high switching frequency HWCW voltage multiplier circuit with good circuit performance.




(a) Experimental waveforms of $D_2$ (b) Experimental waveforms of $D_4$




(c) Experimental waveforms of $D_6$ (d) Experimental waveforms of the SiC diode $D_2$

Fig. 5-31 The experimental waveforms for 3-stage voltage multiplier circuit

## 5.5 Power loss for the voltage multiplier

As mentioned in Chapter 3, the power loss for the voltage multiplier can be calculated based on the following analysis.

The power loss of capacitors in the voltage multiplier circuit:

$$P_{cap\_vm} = \frac{\tan\delta I_{cvm\text{-}rms}^2}{2\pi f C_{vm}} \tag{5-19}$$

where $C_{vm}$ is the capacitor of the voltage multiplier, $I_{cvm\text{-}rms}$ is the RMS value of the AC current flowing through the capacitor of the voltage multiplier and tanδ is the dissipation factor of the capacitor.

The power loss of the diode in the voltage multiplier circuit mainly consist of two parts: conduction loss and reverse recovery loss. The conduction loss can be calculated with the following expression:

$$P_{diode\_vm\_con} = V_{F0} I_{d\_Fav} + I_{d\_rms} R_d^2 \tag{5-20}$$

Where where $I_{d\_Fav}$ is the average current flowing through the diode, and $I_{d\_Fav}$ is the RMS current. The conduction losses of the anti-parallel diode can be estimated using a diode approximation with a series connection of DC voltage source ($V_{F0}$) representing diode on-state zero-current voltage and a diode on-state resistance ($R_d$).

The switching loss can be approximated as follows:

$$P_{diode\_rec\_rr} = f Q_{rr} V_r \tag{5-21}$$

where $Q_{rr}$ is the diode reverse recovery charge, $V_r$ is the reverse voltage of the diode.

Based on the analysis of the diode reverse recovery in the voltage multiplier circuit, only the diodes in the first stage of the voltage multiplier circuit suffer the reverse recovery loss. The silicon carbide Schottky diode without reverse recovery can be employed to effectively eliminate the diode reverse recovery loss in the multistage voltage multiplier circuit.

The total power loss of the diode in the voltage multiplier can be expressed as:

$$P_{diode\_vm} = V_{F0} I_{d\_Fav} + I_{d\_rms} R_d^2 + f Q_{rr} V_r \tag{5-21}$$

The total power loss of the voltage multiplier with silicon diode can be calculated with the following expression:

$$P_{vm\_si-diode} = \frac{\tan\delta I_{cvm\text{-}rms}^2}{2\pi f C_{vm}} + V_{F0} I_{d\_Fav} + I_{d\_rms} R_d^2 + f Q_{rr} V_r \tag{5-22}$$

The total power loss of the voltage multiplier with a silicon carbide Schottky diode can be expressed as:

$$P_{vm\_SiC-diode} = \frac{\tan\delta I_{cvm\text{-}rms}^2}{2\pi f C_{vm}} + V_{F0} I_{\mathrm{d\_Fav}} + I_{\mathrm{d\_}rms} R_d^2 \qquad (5\text{-}23)$$

## 5.6 Summary

The key characteristics and influence factors of the rise and decay time of the voltage multiplier based HV pulse converter are analysed. The HV pulse rise time is about four switching cycles for a 1-stage HWCW voltage multiplier circuit and around twenty switching cycles for a 2-stage HWCW voltage multiplier. The HV pulse rise time will lengthen when a more stages voltage multiplier circuit is used. The voltage rating of the HV transformer and stage number of the voltage multiplier need to be considered for the optimal system performance. When the stage number of the voltage multiplier is determined, the switching frequency is the key influence factor for the HV pulse rise time. A higher switching frequency will lead to a shorter HV pulse rise time. Load resistance and the voltage multiplier capacitor have little influence on the pulse rise time when the input current is not limited (assuming sufficient energy for the voltage multiplier). The HV pulse decay time is proportional to the load resistance and the voltage multiplier capacitance. Voltage multiplier capacitance can be reduced with a higher switching frequency. The high switching frequency can effectively reduce the HV pulse rise and decay times. The 2kV 300 kHz HV pulse converter circuit prototype experimental results verify the analysis of the HV pulse rise and decay times. The HV pulse response advantages of the high frequency modular architecture have been validated from two technology demonstrators.

The diode reverse recovery effect of the HWCW voltage multiplier circuit is investigated for the HV pulse converter. The diode reverse recovery problem is mainly caused by the diodes in the first stage voltage multiplier. The diode reverse recovery problem is the bottle neck to further increasing the circuit operation switching frequency for achieving high power density and short rise and decay times. It is suggested that the most effective and economic way to alleviate the diode reverse recovery problem is by employing diodes without reverse recovery such as silicon carbide Schottky diodes in the first stage only. The silicon carbide Schottky diode without reverse recovery needs to be used in the first stage of the voltage multiplier to effectively mitigate the reverse recovery problems at high frequency. The 300kHz switching frequency 3-stage voltage multiplier circuit hardware prototype experimental results finally validate the analysis and simulation results. At a high temperature operation environment, the silicon carbide Schottky diode will enable further benefits to achieve optimal performance for a multistage voltage multiplier circuits.

## 5.7 References

[5-1] J.A. Martin-Ramos, A.M. Pernia, J. Diaz, F. Nuno, J.A. Martinez, “Power supply for a high-voltage application,” IEEE Transaction on Power Electronics, 2008, vol. 23, no.4, pp. 1608-1619.

[5-2] Hino, H.; Hatakeyama, T.; Nakaoka, M.,” Resonant PWM inverter linked DC-DC convertor using parasitic impedances of high-voltage transformer and its applications to

X-ray generator," IEEE Power Electronics Specialists Conference, 1988. vol. 2, pp. 1212-1219.

[5-3] E.E. Bowles; S. Chapelle; G. X. Ferguson; D. S. Furuno," A high power density, high voltage power supply for a pulsed radar system," IEEE Power Modulator Symposium, Jun. 1994, pp.170-173.

[5-4] M. Khalifa, High-Voltage Engineering: Theory and Practice. New York, NY, USA: Marcel Dekker, Mar. 1990.

[5-5] L. Katzir and D. Shmilovitz, "A matrix-like topology for high-voltage generation," IEEE Transaction Plasma Sci., vol. 43, no. 10, pp. 3681-3687, Oct. 2015

[5-6] S. Mao, "A high frequency high voltage power supply," in Proc. IEEE EPE, ECCE-Europe, 2011, pp.1-5.

[5-7] Y. Du, J. Wang, G. Wang, and A. Q. Huang, "Modeling of the high frequency rectifier with 10-kV SiC JBS diode in high-voltage series resonant type DC-DC converters," IEEE Tran. Power Electron., vol.29, no.8, pp. 4288-4300, Aug. 2014.

[5-8] S. Mao, J. Popovic, J. A. Ferreira, "High voltage pulse speed study for high voltage DC-DC power supply based on voltage multiplier," in Proc. IEEE EPE, ECCE-Europe, 2015, pp.1-10.

[5-9] Bortis, D.; Ortiz, G.; Kolar, J.W.; Biela, J.," Design procedure for compact pulse transformers with rectangular pulse shape and fast rise times," IEEE Transaction on Dielectrics and Electrical Insulation, vol. 18, issue. 4, Mar., 2011. pp.1171-1180.

[5-10] Iqbal, S.; Singh, G.K.; Besar, R.," A dual-mode input voltage modulation control scheme for voltage multiplier based X-Ray power supply," IEEE Transaction on Power Electronics, vol. 23, no. 2, Mar., 2008. pp. 1003-1008.

[5-11] I.C. Kobougias, E.C. Tatakis, "Optimal design of a half-wave Cockcroft–Walton voltage multiplier with minimum total capacitance," IEEE Transaction on Power Electronics, 2010, 25(9), Pages: 2460-2468.

[5-12] S. Mao, T. Wu, X. Lu, J. Popovic, J. A. Ferreira, "High frequency high voltage power conversion with silicon carbide power semiconductor devices," in Proc. IEEE Electronic System-Integration Technology Conference (ESTC), 2016, pp.1-5.

[5-13] J. S. Brugler, "Theoretical performance of voltage multiplier circuits," IEEE Journal of Solid-State Circuits, 1971, 6(3), pp.132-135.

[5-14] A. Shenkman, Y. Berkovich, and B. Axelrod, "Novel AC–DC and DC–DC converters with a diode-capacitor multiplier," IEEE Transaction Aerosp. Electron. Syst., vol. 40, no. 4, pp. 1286–1293, Oct. 2004.

[5-15] Sun, J.; Ding, X.; Nakaoka, M.; Takano, H.," Series resonant ZCS-PFM DC-DC converter with multistage rectified voltage multiplier and dual-mode PFM control scheme for medical-use high-voltage X-ray power generator," Electric Power Applications Proceedings, Volume 147, issue.6, Nov. 2000, pp.527-534.

[5-16] S. Iqbal, G. K. Singh, and R. Besar, "A dual-mode input voltage modulation control scheme for voltage multiplier based X-ray power supply," IEEE Transaction Power Electron., vol. 23, no. 2, pp. 1003–1008, Mar. 2008.

[5-17] S. Mao, P. Zhang, J. Popovic, J. A. Ferreira, "reverse recovery Analysis of Cockcroft-Walton Voltage Multiplier for High Voltage Generation," in Proc.IEEE ECCE-Aisa, 2017, pp.1-6.

# Chapter 6

# The unified steady-state circuit model and the comprehensive design of modular HV pulse converters

## 6.1 Introduction

As introduced in Chapter-3, there are different HV pulse converter architectures for various industrial applications [6-1]-[6-4]. These HV pulse converter architectures can be classified based on the modularization level of key power building blocks of the HV pulse converter as shown in Fig. 6-1. The map of HV pulse converter architectures for different output voltages and power levels with single power inverter configurations is illustrated in Fig. 6-2. HV rectifiers have different circuit configurations, such as the full-bridge rectifier, single or dual polarity half-wave(HW) Cockcroft-Walton (CW) voltage multiplier and full-wave(FW) CW voltage multiplier, as shown in Fig. 6-3[6-5]-[6-19]. These varying HV pulse converter architectures with different HV rectifier circuit configurations offer more alternatives to generate high output voltages. Simultaneously, more challenges are added in modelling and analysis due to various HV pulse converter architectures [6-20]-[6-25].

Circuit modelling for the HV pulse converter is challenging due to the complex operation modes and large values of transformer parasitics [6-26]-[6-27]. The first harmonic approximation (FHA) is a classical modelling solution, which replaces the voltages and currents by the fundamental components of the Fourier transformation to linearize the original circuit [6-28]-[6-29]. In these linearized models [6-7], [6-8], [6-19], [6-22]- [6-25], [6-30], the behaviour of the LCC resonant converter with a simple full-bridge rectifier is described in detail. Unfortunately, most state-of-the-art steady-state models are deduced only for the simple full-bridge rectifier and only for a specified architecture. For the voltage multiplier fed by the LCC resonant tank, the operation of the voltage multiplier is far more complex than that of the full bridge rectifier. The equation of a LCC converter feeding a 3-stage full-wave CW voltage multiplier is proposed in [6-19], where the voltage multiplier is replaced by the 1-stage CW rectifier and cannot represent the complex operation modes of the CW voltage multiplier. Generally, the modelling of the voltage multiplier fed by the LCC resonant tank and the various HV pulse converter architectures are two remaining challenges to be solved. A FHA-based steady-state model is proposed in [6-31], where the HV transformer and the full-bridge rectifier is modelled by a resistor and capacitor (RC) network. This simple and extendable RC model is a promising solution to deduce a unified model of HV pulse converter architectures. However, the model needs to be further improved to describe the voltage multiplier fed by the LCC resonant tank and to be extended to all HV pulse converter architectures with different voltage multiplier topologies, stage numbers and polarities.

In addition to the lack of unified circuit models, the design of the HV pulse converter is also challenged by the high degree of design freedom. An iterative design procedure with the analytical RC model is given in [6-9]. A design based on the normalized characteristic diagram is given in [6-21]. In these design methods, some parameters are assumed to simplify the calculation. The parallel-series capacitor ratio $A=C_p/C_r$ is one of the most widely adopted assumption. However, ratio $A$ is not intuitive to reflect the HV pulse converter's performance and does not ensure overall optimized parameters. Moreover, the computer algorithms to search a large space of variables to acquire optimized designs are proposed in [6-10], [6-18]. However, this approach is time consuming.

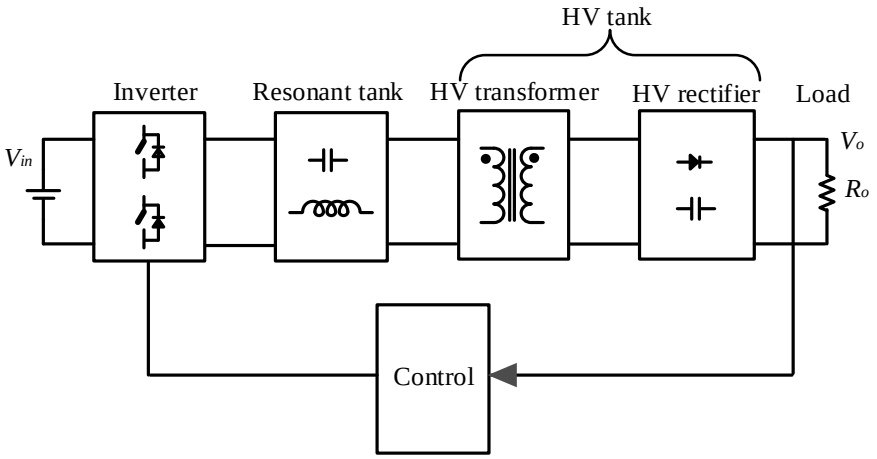



Fig. 6-1 HV pulse converter circuit diagram

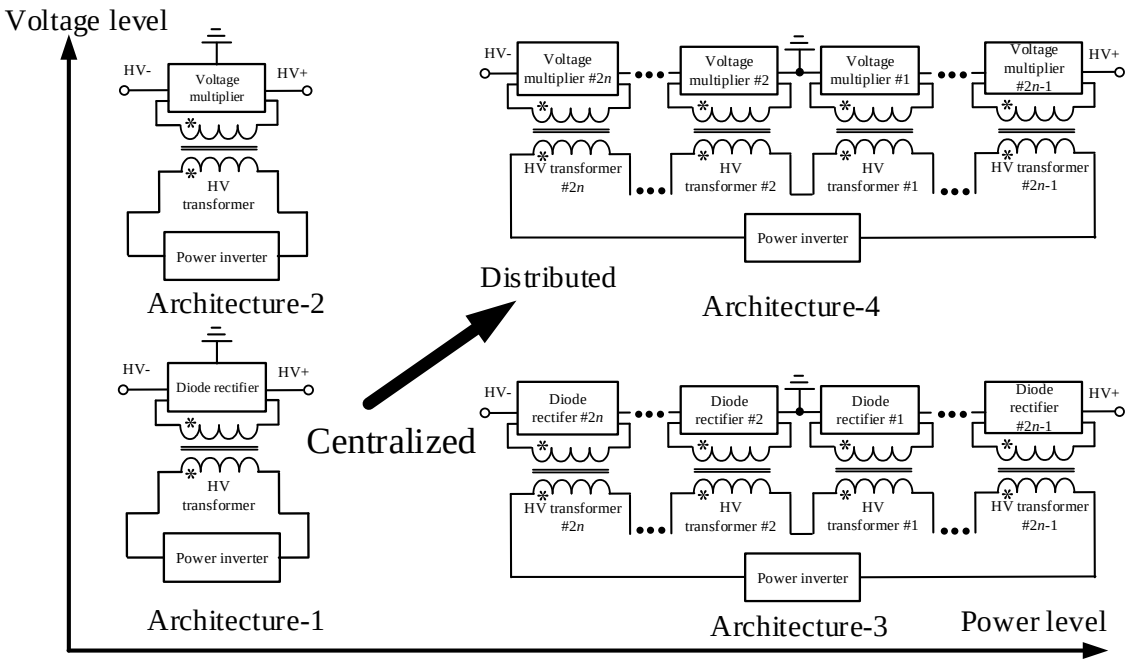
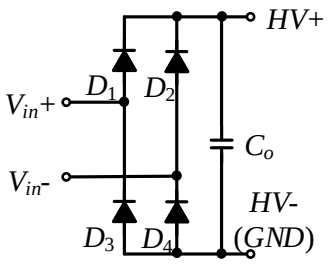
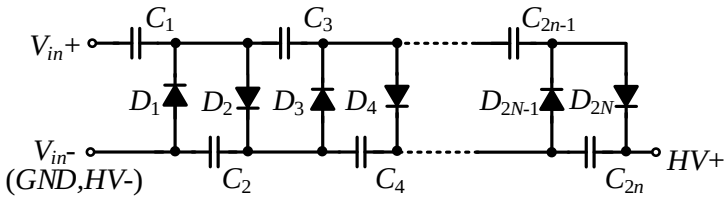


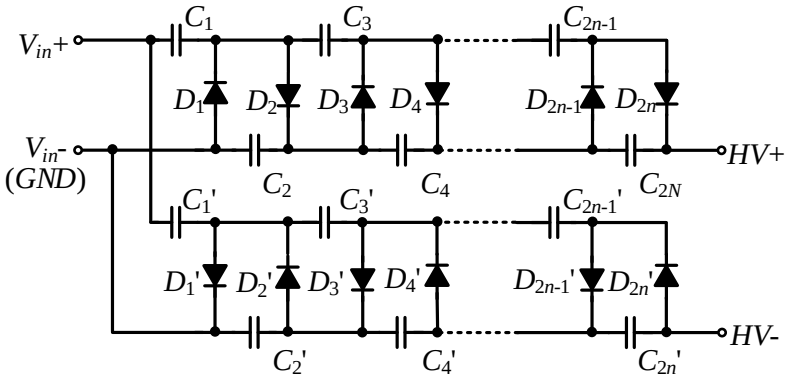

Fig. 6-2 Map of HV pulse converter architectures for different output voltages and power levels with single power inverter configurations



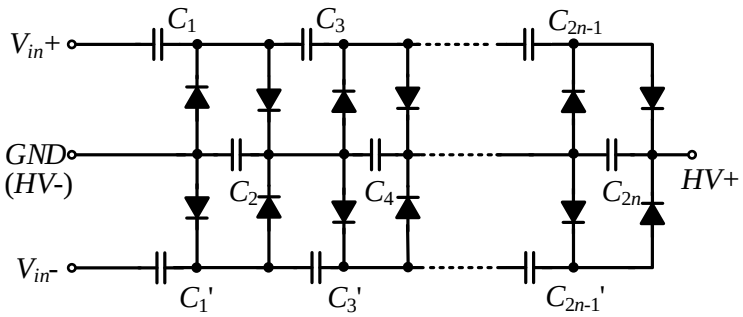

(a) Full bridge rectifier [6-5]-[6-11]




(b) Single polarity half-wave CW voltage multiplier [6-12]- [6-15]




(c) Dual polarity half-wave CW voltage multiplier [6-16[, [6-17]




(d) Full-wave CW voltage multiplier [6-18], 6-19]

Fig. 6-3 Topologies of HV rectifiers

In summary, there is a need for a unified equivalent circuit model which can provide effective guidelines in analysis, for the design of the HV pulse converter with different HV pulse converter architectures. The comprehensive design method of a LCC resonant converter based

modular HV pulse converter architecture has not yet been well addressed. A unified steady-state circuit model is essential and it is helpful to investigate HV pulse converter performance for various architectures with different voltage multiplier topologies, stage numbers and polarities, which could offer effective guidelines for architectures' selection and parameter design. Chapter 6 will derive the unified steady-state equivalent circuit modelling approach for different HV pulse converter architectures. The generic model can then be applied to HV generators with different architectures, different voltage multiplier topologies, stage and polarity numbers. This model is then used to develop a comprehensive design methodology utilizing conduction angle, power factor and quality factor and verified by the modular HV pulse converter prototype experimental results.

## 6.2 Unified equivalent steady-state circuit modeling

### 6.2.1 Modelling assumptions

In this section, firstly an analytical electrical circuit model of a voltage multiplier fed by the LCC resonant tank is derived. Then a unified model for the four architectures with different rectifiers is given. To simplify the derivation of the steady-state model, the following assumptions are made:

1) The switching devices are ideal;

2) The quasi-sinusoidal resonant current $i_l(t)$ is equivalent to the ideal sinusoidal current, which is given by

$$i_l(t) = I_{lm} \sin(\omega_s t) \tag{6-1}$$

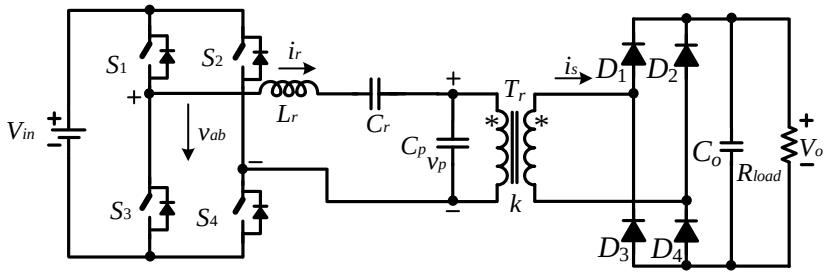
3) The output voltage ripple and drop are ignored due to the large DC voltage and high operating frequency.

### 6.2.2. Modeling of the LCC resonant HV pulse converter with the single polarity half-wave Cockcroft-Walton voltage multiplier

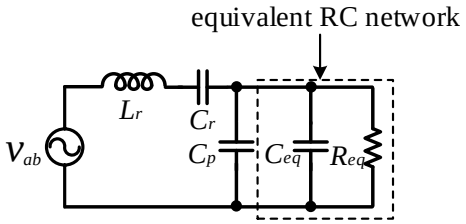
Due to the high insulation requirements, the equivalent circuit model of the HV transformer is described by the series leakage inductance, the parallel winding capacitance reflected to the primary side and the ideal transformer [6-8]. Besides, the parasitic capacitance of rectifiers affects the operation of the LCC resonant converter [6-33] and needs to be considered. A widely used analytical model of the LCC resonant converter is proposed in [6-31], where the HV transformer with a full-bridge rectifier is replaced by an equivalent RC network, as shown in Fig. 6-4. However, for the HV transformer loaded by the half-wave single polarity CW voltage multiplier, shown in Fig. 6-5, the output capacitors are charged in parallel and discharged in series. The voltage and current distribution among the output diodes should be considered as opposed to the for the full-bridge rectifier. Thus, an improved RC model needs to be derived.

The typical waveforms of a LCC resonant converter with voltage multiplier is given in Fig. 6-6 [6-31]. By replacing $v_P$ and $i_s$ with gain fundamental element of the Fourier transformation, the equivalent resistance $R_{eq}$ and capacitance $C_{eq}$ is calculated by the impedance of the

transformer input side. The voltage gain and current gain of the voltage multiplier are taken into consideration for equivalent circuit modeling.




(a) Circuit diagram of the LCC resonant converter with the full-bridge rectifier




(b) Equivalent circuit of the LCC resonant converter with the full-bridge rectifier proposed in [6-31]

Fig. 6-4 LCC resonant converter with the full-bridge rectifier

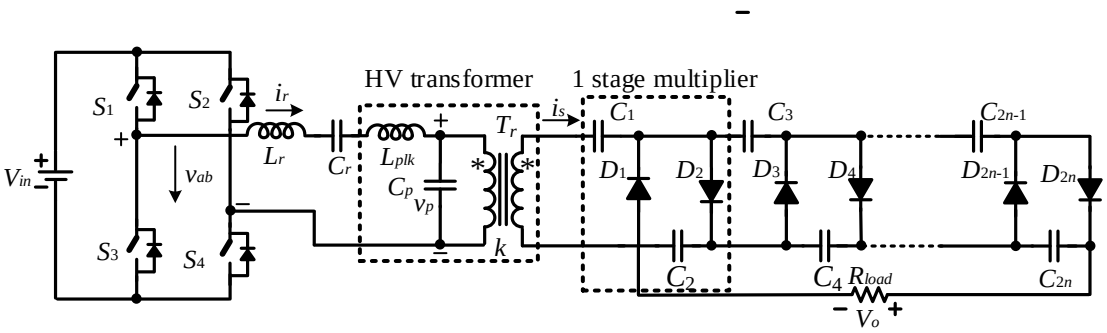



Fig. 6-5 Single polarity voltage multiplier fed by the LCC resonant tank.

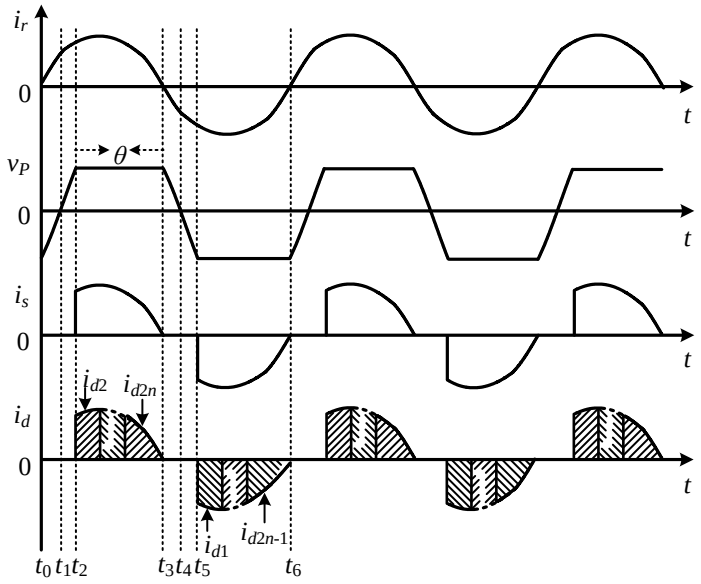



Fig. 6-6 Waveforms of the LCC resonant converter with a voltage multiplier

From Fig. 6-6, the expression of the parallel capacitor voltage and transformer secondary side current is

$$v_{cp}(t)=\begin{cases}\dfrac{V_{sec}(1-\cos(\theta)-2\cos(\omega_s t))}{k(1+\cos(\theta))}, & 0\le\omega_s t\le\pi-\theta\\ \dfrac{V_{sec}}{k}, & \pi-\theta\le\omega_s t\le\pi\\ \dfrac{V_{sec}(-1+\cos(\theta)-2\cos(\omega_s t))}{k(1+\cos(\theta))}, & \pi\le\omega_s t\le 2\pi-\theta\\ -\dfrac{V_{sec}}{k}, & 2\pi-\theta\le\omega_s t\le 2\pi\end{cases} \tag{6-2}$$

$$i_s(t)=\begin{cases}0, 0\le\omega_s t\le\pi-\theta, \pi\le\omega_s t\le 2\pi-\theta\\ \dfrac{I_{Lm}\sin(\omega_s t)}{k}, \pi-\theta\le\omega_s t\le\pi, 2\pi-\theta\le\omega_s t\le 2\pi\end{cases} \tag{6-3}$$

$$i_{cp}(t)=\begin{cases}I_{Lm}\sin(\omega_s t), 0\le\omega_s t\le\pi-\theta, \pi\le\omega_s t\le 2\pi-\theta\\ 0, \pi-\theta\le\omega_s t\le\pi, 2\pi-\theta\le\omega_s t\le 2\pi\end{cases} \tag{6-4}$$

During period [0, π-$\theta$], the parallel capacitor is charged by the resonant current, thus

$$-\frac{V_{sec}}{k}=\frac{V_{sec}}{k}+\frac{1}{C_p}\int_0^{\pi-\theta} i_r(t)dt \tag{6-5}$$

$I_{rm}$ is expressed by

$$I_{rm} = \frac{2\omega_s C_p V_{sec}}{k(1+\cos(\theta))} \tag{6-6}$$

The average current of secondary side is

$$I_{s,avg} = \frac{2}{k\pi} I_{rm} \sin^2(\frac{\theta}{2}) \tag{6-7}$$

The voltage gain of the voltage multiplier is

$$k_{VM} = \frac{V_o}{V_{sec}} = 2n \tag{6-8}$$

In steady-state, since capacitors cannot enable the DC current to flow, the output DC current only flows through the series connected diodes. As a result, each diode transfers the same amount of charge in a switching period. For the *N*-stage voltage multiplier, the transformer secondary side current is divided into *N* parts with same area, as shown in Fig. 6-6. The current ratio between the average current of transformer secondary side and output current is

$$\frac{I_{sec,avg}}{I_o} = k_{VM} \tag{6-9}$$

From (6-6) to (6-9) the conduction angle is calculated by

$$\theta = 2\arctan\sqrt{\frac{{k_{VM}}^2 k^2 \pi}{2\omega_s C_p R_{load}}} \tag{6-10}$$

Applying a Fourier transformation for $v_{cp}$, the fundamental element of the parallel capacitor voltage is expressed by

$$\vec{v}_{cp,1} = V_{cp,1}\angle\alpha \tag{6-11}$$

Utilizing a Fourier transformation, coefficients of the fundamental elements in $v_{cp}$ is

$$\begin{aligned} a_{v1} &= \frac{2}{\pi}\left(\frac{\sin(\theta)-\pi+\theta}{1+\cos(\theta)} - \sin(\theta)\right) \\ b_{v1} &= \frac{2}{\pi}(1-\cos(\theta)) \\ k_v &= \sqrt{a_{v1}^2 + b_{v1}^2} \end{aligned} \tag{6-12}$$

$V_{cp,1}$, $\alpha$ are

$$V_{cp,1} = \frac{k_v}{K} V_{sec}$$
$$\alpha = \arcsin\left(\frac{a_{v1}}{\sqrt{a_{v1}^2 + b_{v1}^2}}\right) \tag{6-13}$$

Applying the Fourier transformation for $i_{cp}$, the fundamental element of the parallel capacitor current is expressed by

$$\dot{i}_{cp,1} = I_{cp,1} \angle \beta \tag{6-14}$$

The coefficients of the fundamental elements in the Fourier transformation is

$$a_{i1} = \frac{1}{\pi}\left(\frac{1-\cos(\theta)}{2}\right)$$
$$b_{i1} = \frac{1}{\pi}\left(\pi - \theta + \frac{\sin(2\theta)}{2}\right) \tag{6-15}$$
$$k_i = \sqrt{a_{i1}^2 + b_{i1}^2}$$

$i_{cp,1}$, $\beta$ are

$$I_{cp,1} = k_i I_{rm}$$
$$\beta = \arcsin\left(\frac{a_{i1}}{\sqrt{a_{i1}^2 + b_{i1}^2}}\right) \tag{6-16}$$

The HV transformer and voltage multiplier can be equivalent by using a resistor and parallel capacitor. Assuming that the conversion efficiency of the HV pulse converter circuit is $\eta$, the power dissipated in $R_e$ satisfies

$$\frac{V_{cp,1}^2}{2R_e} \cdot \eta = \frac{V_o^2}{R_o} \tag{6-17}$$

Applying (6-15), (6-16), (6-17), $R_e$ is calculated by

$$R_{eq} = \frac{\eta k_v{}^2 R_{load}}{2k^2 k_{VM}{}^2} \tag{6-18}$$

According to phase relation, $C_{eq}$ is calculated by

$$C_{eq} = \frac{I_{rm} \sin\alpha - I_{cp,1}}{\omega_s V_{cp,1}} \tag{6-19}$$

Substituting (6-13), (6-16) into (6-19),

$$C_{eq} = k_c C_p \tag{6-20}$$

where $k_c$ is only function of the conduction angle

$$k_c = \frac{2}{k_v(1+\cos(\theta))}\left( \frac{-a_{v1}}{k_v} - \frac{1}{\pi}\sqrt{\left(\frac{1}{2} - \frac{\cos(2\theta)}{2}\right)^2 + \left(\pi - \theta + \frac{\sin(2\theta)}{2}\right)^2} \right) \tag{6-21}$$

In summary, the derived $R_{eq}$ and $C_{eq}$ are given by

$$\begin{aligned} R_{eq} &= \frac{\eta {k_v}^2 R_{load}}{2k^2 {k_{VM}}^2} \\ C_{eq} &= k_c C_p \end{aligned} \tag{6-22}$$

where $\eta$ is the conversion efficiency of the HV pulse converter circuit, $K$ is the turns ratio of the HV transformer and $k_{VM}$ is the voltage gain of the voltage multiplier. The coefficients $k_v$ and $k_c$ originate from the Fourier analysis of the waveforms. The conduction angle $\theta$ is the interval when the voltage of the HV transformer is clamped by the output capacitors.

The total parallel capacitance of the HV pulse converter circuit is

$$C_{tot} = C_P + C_{eq} = (1 + k_c) C_P \tag{6-23}$$

The expression of $R_{eq}$, $C_{eq}$ is also applicable for the full-bridge rectifier or the full-wave CW voltage multiplier. The detailed derivation procedure is similar and not considered in this paper. $k_{VM}$=1 would hold in the case of the full-bridge rectifier.

During the nonconductive interval [$t_0$, $t_2$] and [$t_3$, $t_5$] of the multiplier diodes, as shown in Fig. 6, the parasitic capacitors of the diodes are charged by the output current of the HV transformer. The equivalent circuit model during the nonconductive interval [$t_0$, $t_2$] and [$t_3$, $t_5$] of the multiplier diodes is illustrated in Fig. 6-7. During this period, the charge current loop contains multiplier capacitors and parasitic capacitors. Since the output capacitors are far larger than the parasitic capacitors, the voltage drop across the output capacitors caused by the charge current can be ignored and all output capacitors can be approximately viewed as shorted together, as shown in Fig. 6-8. As a result, all parasitic capacitors of the diodes are connected in parallel and can be included in the parallel capacitance $C_p$.

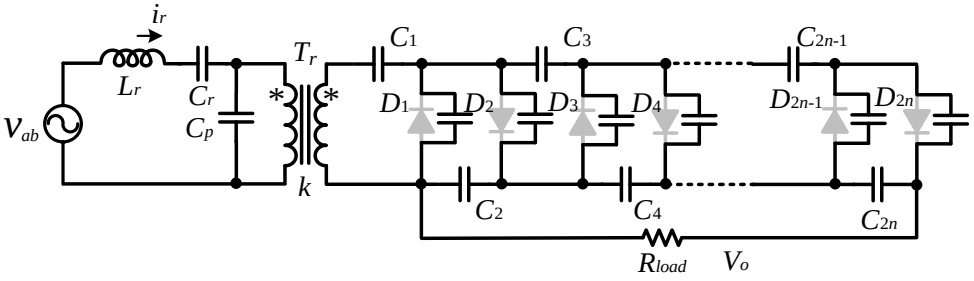


Fig. 6-7 **Equivalent circuit model during the nonconductive interval [$t_0$, $t_2$] and [$t_3$, $t_5$] of multiplier didoes**

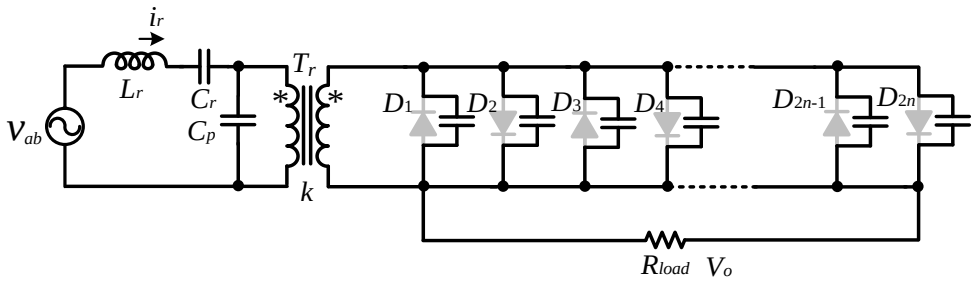
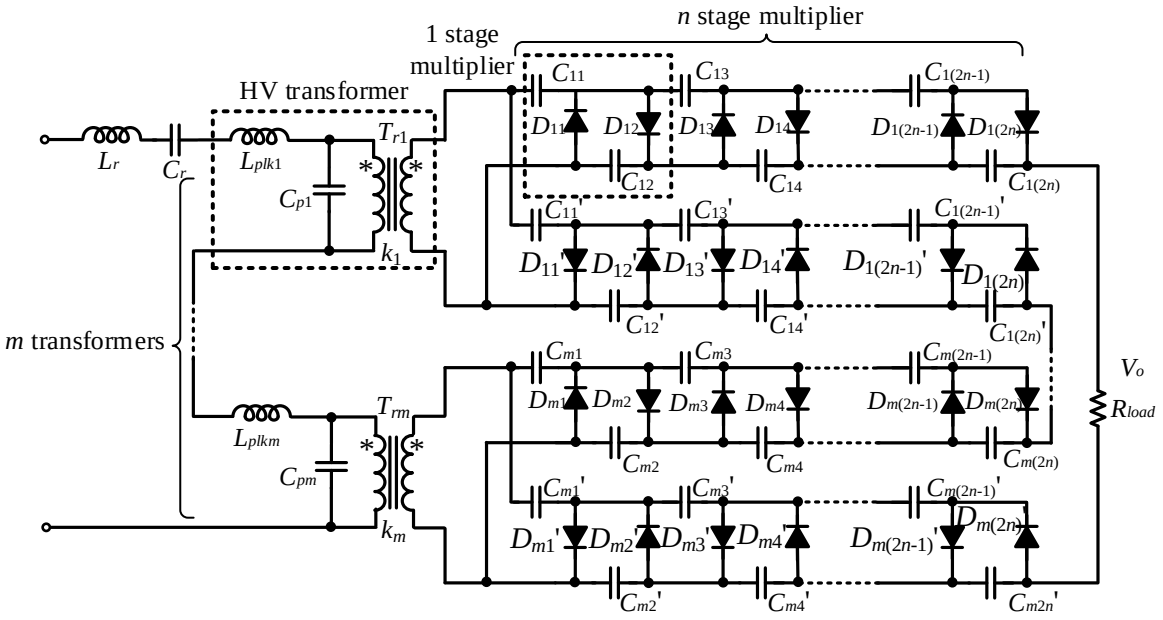



Fig. 6-8 **Simplified equivalent circuit model during the nonconductive interval [$t_0$, $t_2$] and [$t_3$, $t_5$] of multiplier didoes**

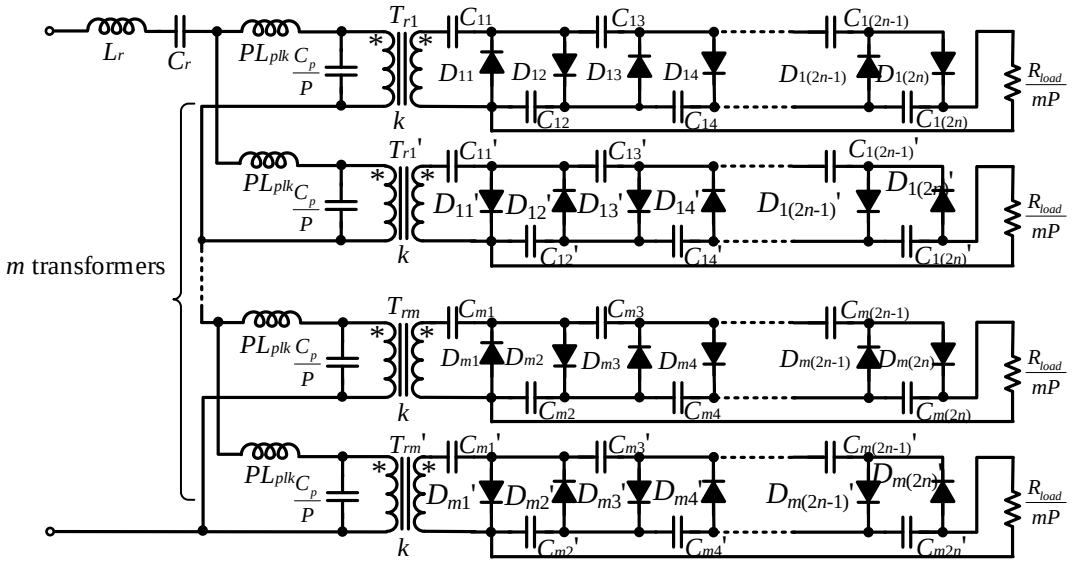
### 6.2.3 Generic steady-state circuit model of four HV pulse converter architectures

Considering the different HV pulse converter architectures, a HV transformer loaded by the full-bridge rectifier or the voltage multiplier is the basic structure of the HV pulse converter circuits. As the basic structure has been modelled by an equivalent RC model, the model of the combined HV pulse converter architectures is established by breaking down architectures into its basic structure. Since Architecture-4 is the most complex architecture, modeling of modular HV pulse converter Architecture-4 is presented in detail.

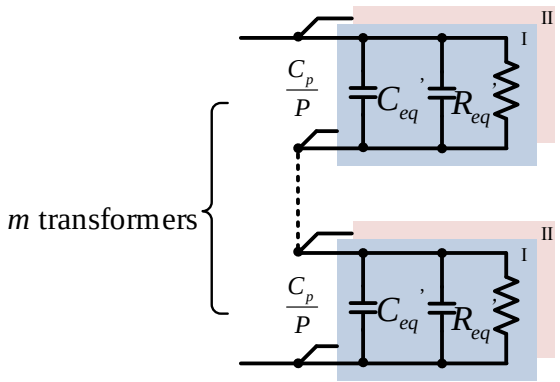
Fig. 6-9 demonstrates the subdivision process of Architecture-4 with *m* distributed transformers loaded by *n*-stage half-wave voltage multipliers. As shown in Fig. 6-9(a), due to symmetry, the output voltage of each voltage multiplier is equal. Hence, Architecture-4 can be equally divided into *m* parts separately, without making any difference on the input side. Besides, for the dual polarity ($P$=2) CW voltage multiplier, the positive half output voltage and current is symmetrically equal to the negative half output voltage and current. Each multiplier is further divided into *P* single polarity *n*-stage voltage multipliers connected in parallel which makes no difference on the input side of the voltage multiplier. As a result, Architecture-4 is split into $m \times P$ basic structures separately, as illustrated in Fig. 6-9(b). Each part is modelled individually by an equivalent parallel resistor and capacitor, as shown in Fig. 6-9(c). Finally, a merged equivalent RC model is acquired in Fig. 6-9(d).



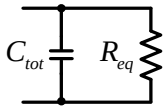

(a) Topology of HV pulse converter Architecture-4




(b) Input side equivalent transformation



(c) Equivalent RC network




(d) Merged equivalent RC model

Fig. 6-9 Modeling of HV pulse converter Architecture-4

In the sub-divided single polarity half-wave CW voltage multiplier, the output resistor is

$$R_o^{'} = \frac{R_{load}}{m \cdot P} \tag{6-24}$$

The parallel capacitor is

$$C_P^{'} = \frac{C_P}{P} \tag{6-25}$$

The conduction angle, equivalent resistor and capacitor of the split HV transformer loaded by the CW voltage multiplier are calculated by replacing the output resistor and parallel capacitor in (6-10), (6-22) with (6-24), (6-25), The total equivalent capacitance and resistance of the HV transformer and voltage multiplier are calculated by

$$\begin{aligned} R_{eq} &= \frac{m}{P} R_{eq}^{'} \\ C_{eq} &= \frac{P}{m} C_{eq}^{'} \end{aligned} \tag{6-26}$$

Since there are *m* parallel capacitors connected in series, the total input capacitance of the HV pulse converter circuit is

$$C_{tot} = \frac{C_P}{m} + C_{eq} = \left( \frac{1}{m} + k_c \right) C_P \tag{6-27}$$

The *m* leakage inductors of the transformer are connected in series, thus the total resonant inductance of the LCC resonant tank is

$$L_{r\_tot} = L_r + mL_{plk} \tag{6-28}$$

It is evident that the modelling procedure of HV pulse converter Architecture-4 can be applied to the other distributed architectures by assigning numbers of transformers (*m*), stages of voltage multipliers (*n*), and polarities (*P*) of the voltage multiplier accordingly, as shown in Table 6-1.

Table 6-1 Parameters to describe the four HV pulse converter architectures

| Architecture | Numbers of transformers | Stages of voltage multipliers | Polarity |
|---|---|---|---|
| 1 | 1 | 1 | 1 |
| 2 | 1 | *n* | *P* |
| 3 | *m* | 1 | 1 |
| 4 | *m* | *n* | *P* |

Above all, a general model of the four HV pulse converter architectures is concluded by

$$
\begin{aligned}
k_{vm} &= \begin{cases} 2n\text{, voltage multiplier} \\ 1\text{, diode rectifier} \end{cases} \\
\theta &= 2\arctan\sqrt{\frac{mP^2{k_{VM}}^2k^2}{4f_sC_PR_{load}}} \\
R_{eq} &= \frac{\eta k_V^2}{2P^2k^2k_{VM}^2}\cdot R_{load} \\
C_{tot} &= \frac{(1+k_c)C_P}{m}
\end{aligned}
\tag{6-29}
$$

where $k_v$, and $k_c$ are calculated in (6-11) and (6-20). By replacing the highly nonlinearity HV pulse converter circuit with the equivalent RC circuit model, the HV pulse converter analysis is significantly simplified.

### 6.2.4 Simulation verifications of the steady-state circuit model

To verify the presented model, HV pulse converters with the four different architectures are simulated and compared with the proposed model. The parameters of the HV pulse converters are designed to meet output voltage $V_o$ and output power $P_o$ specifications, as shown in Table 6-2. The switching frequency is chosen as 400kHz and the input voltage is 250VDC. The comparison between the proposed model and the simulation are given in Table 6-3. In most cases, the error is below 6%, which verifies the validity of the proposed model. However, the large error occurs at designs (6) and (14), where the double polarity 4-stage voltage multiplier is adopted and the output current is relatively large. In large output current cases, the voltage ripple and drop of the voltage multiplier cannot be ignored and modelling assumption three is not satisfied. As a result, a large deviation occurs in the Fourier analysis leads to a large modelling error. So, the proposed model is suitable for low output voltage ripple conditions.

Table 6-2 Parameters of the HV pulse converters

| | *No.* | $V_o$ /kV | $P_o$ /kW | $L_r$/ μH | $C_r$/ nF | $C_p$/ nF | *k* | *m* | *n* | *P* |
|---|---|---|---|---|---|---|---|---|---|---|
| Architecture-1 | (1) | 20.0 | 0.5 | 138.8 | 2.2 | 1.5 | 44.4 | 1 | 1 | 1 |
| | (2) | 20.0 | 20 | 34.7 | 6.6 | 4.6 | 66.7 | 1 | 1 | 1 |
| | (3) | 100.0 | 0.5 | 138.8 | 12.3 | 1.2 | 111.1 | 1 | 1 | 1 |
| | (4) | 100.0 | 20 | 34.7 | 49.3 | 4.6 | 111.1 | 1 | 1 | 1 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Architecture-2 | (5) | 20.0 | 0.5 | 138.8 | 1.6 | 1.2 | 5.6 | 1 | 3 | 2 |
| | (6) | 20.0 | 20 | 37.9 | 6.3 | 5.0 | 4.6 | 1 | 3 | 2 |
| | (7) | 100.0 | 0.5 | 101.5 | 4.6 | 1.5 | 13.9 | 1 | 4 | 2 |
| | (8) | 100.0 | 20 | 34.7 | 4.6 | 4.6 | 20.8 | 1 | 4 | 2 |
| Architecture-3 | (9) | 20.0 | 0.5 | 89.7 | 4.1 | 5.1 | 57.1 | 2 | 1 | 1 |
| | (10) | 20.0 | 20 | 22.4 | 13.0 | 18.5 | 74.8 | 2 | 1 | 1 |
| | (11) | 100.0 | 0.5 | 138.8 | 2.2 | 6.2 | 222.2 | 4 | 1 | 1 |
| | (12) | 100.0 | 20 | 24.2 | 11.4 | 23.4 | 375.0 | 4 | 1 | 1 |
| Architecture-4 | (13) | 20.0 | 0.5 | 138.8 | 2.2 | 3.1 | 5.6 | 2 | 2 | 2 |
| | (14) | 20.0 | 20 | 34.7 | 6.6 | 9.3 | 8.3 | 2 | 2 | 2 |
| | (15) | 100.0 | 0.5 | 138.8 | 12.3 | 2.3 | 9.3 | 2 | 3 | 2 |
| | (16) | 100.0 | 20 | 34.7 | 6.6 | 9.3 | 27.8 | 2 | 3 | 2 |

Table 6-3 Comparison between the simulation (Sim.) and the model

| *No.* | $V_o$/kV | | | $I_{Lm}$/A | | | $I_s$/A | | |
|---|---|---|---|---|---|---|---|---|---|
| | Sim. | Model | Error | Sim. | Model | Error | Sim. | Model | Error |
| (1) | 19.62 | 20.00 | 1.9% | 3.35 | 3.5 | 4.2% | 0.0037 | 0.0039 | 5.4% |
| (2) | 19.45 | 20.00 | 2.8% | 13.31 | 14.0 | 4.9% | 0.1258 | 0.1328 | 5.6% |
| (3) | 98.20 | 100.00 | 1.8% | 3.28 | 3.5 | 6.4% | 0.0094 | 0.0098 | 4.0% |
| (4) | 98.18 | 100.00 | 1.9% | 13.59 | 14.0 | 2.7% | 0.0039 | 0.0039 | 0.0% |
| (5) | 20.49 | 20.00 | -2.4% | 3.58 | 3.5 | -2.5% | 0.3934 | 0.3985 | 1.3% |
| (6) | 23.50 | 20.00 | -14.9% | 17.43 | 13.2 | -24.1% | 1.8252 | 1.6959 | -7.1% |
| (7) | 96.23 | 100.00 | 3.9% | 3.16 | 3.5 | 6.1% | 0.1167 | 0.1257 | 7.7% |
| (8) | 99.20 | 100.00 | 0.8% | 13.76 | 14.0 | 1.5% | 0.4112 | 0.4251 | 3.4% |
| (9) | 19.12 | 20.00 | 4.6% | 4.46 | 4.5 | 0.7% | 0.0039 | 0.0039 | 0.0% |
| (10) | 19.54 | 20.00 | 2.4% | 18.16 | 18.0 | -1.1% | 0.1420 | 1.1413 | -0.5% |
| (11) | 95.02 | 100.00 | 5.2% | 3.50 | 3.5 | -0.3% | 0.0077 | 0.0079 | 2.0% |
| (12) | 93.34 | 100.00 | 3.8% | 15.15 | 14.0 | 3.7% | 0.0253 | 0.0266 | 4.9% |
| (13) | 20.38 | 20.00 | -1.9% | 3.55 | 3.5 | -1.7% | 0.3030 | 0.3142 | 3.7% |
| (14) | 22.00 | 20.00 | -9.1% | 12.75 | 14.0 | 9.8% | 1.1097 | 1.0627 | -4.2% |
| (15) | 95.67 | 100.00 | 4.5% | 2.37 | 3.5 | 4.2% | 0.1128 | 0.1179 | 4.5 |
| (16) | 98.17 | 100.00 | 1.9% | 13.70 | 14.0 | 2.4% | 0.3065 | 0.3188 | 4.0 |

In the resonant type HV generators, the output voltage changes with the switching frequency. The frequency response of the design (16), with multiple HV transformers and double polarity rectifiers, is simulated and calculated as an example. As displayed in Fig. 6-10, the simulation is in perfect alignment with the mathematical model, which verifies the validity of the proposed model in the given frequency range.

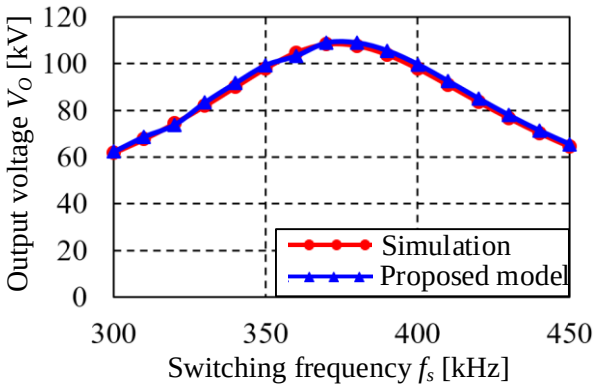



Fig. 6-10 Frequency response of the output voltage by simulation and the proposed model

## 6.3 Comprehensive analysis and design of the HV pulse converter

### 6.3.1 Power factor

Based on the equivalent RC model derived in 6.2, further analysis including the power factor of the resonant tank, voltage gain, quality factor and stresses of the devices is given in this section. These are important parameters to analyze the performance and facilitate the design of the HV pulse converters.

The power factor of the resonant tank is defined as the ratio of real power flowing to the resonant tank to the product of the RMS value of input voltage and current. This yields

$$PF = \frac{P_o}{\eta V_{in} I_{in,RMS}} \tag{6-30}$$

where $P_o$ is the output power, $V_{in}$ is the input voltage, $I_{in,RMS}$ is the RMS value of the input current and $\psi$ is defined as the phase angle between the fundamental component of the resonant tank input voltage and the resonant current. Since the energy is only transferred by the fundamental components, $PF$ is expressed by [6-11] as

$$PF = \frac{2\sqrt{2}}{\pi}\cos\psi \tag{6-31}$$

The equivalent circuit of the resonant tank in steady state is depicted in Fig. 6-4. The impedance of the resonant tank is

$$Z_{in} = j\omega_s L_r + \frac{1}{j\omega_s C_r} + \frac{R_{eq}}{1 + j\omega_s C_{tot} R_{eq}} = |Z_{in}| \angle \psi \tag{6-32}$$

Solving (6-32), the power factor angle is calculated by

$$\psi = \arctan\left(\frac{1}{\left(\frac{\omega_s L_r}{R_{eq}} - \frac{1}{\omega_s C_r R_{eq}}\right)\left(1+\left(\omega_s C_{tot} R_{eq}\right)^2\right) - \omega_s C_{tot} R_{eq}}\right) \tag{6-33}$$

### 6.3.2 Voltage gain

Ignoring the output voltage ripple, the output power is

$$P_o = V_o I_o \tag{6-34}$$

Substituting (6-30), (6-31) into (6-34) yields

$$\frac{V_o}{V_{in}} = \frac{2\sqrt{2}\eta\cos(\psi)}{\pi} \cdot \frac{I_{in,RMS}}{I_o} = \frac{2\sqrt{2}\cos(\psi)}{\pi} \cdot \frac{I_{in,RMS}}{I_{Lm}} \cdot \frac{I_{Lm}}{I_{s,avg}} \cdot \frac{I_{s,avg}}{I_o} \tag{6-35}$$

For the full bridge inverter, the input current is

$$i_{in}(t) = \begin{cases} I_{Lm}\sin(\omega_s t), -\psi \le \omega_s t \le \pi - \psi \\ -I_{Lm}\sin(\omega_s t), \pi - \psi \le \omega_s t \le 2\pi - \psi \end{cases} \tag{6-36}$$

The RMS value of the input current is calculated by

$$I_{in,RMS} = \frac{I_{Lm}}{\sqrt{2}} \tag{6-37}$$

From Fig. 6-10, the coefficients between the resonant current $I_{Lm}$ and transformer secondary side average current $I_{s,avg}$ is

$$\frac{I_{Lm}}{I_{s,avg}} = \frac{k\pi}{2\sin^2(\frac{\theta}{2})} \tag{6-38}$$

Substituting (6-8), (6-37), (6-38) into (6-35) yields

$$\frac{V_o}{V_{in}} = \frac{\eta P k k_{VM}\cos\psi}{\sin^2(\frac{\theta}{2})} \tag{6-39}$$

Equation (6-39) demonstrates that the stages and polarities of the voltage multiplier, turns ratio of the HV transformer, power factor and conduction angle contribute to the HV gain. For the LCC resonant converter, the conduction angle is due to the parallel capacitor. $\theta \subset (0,\pi)$ yields

$$\frac{1}{\sin^2(\frac{\theta}{2})} \geq 1 \tag{6-40}$$

It is indicated that the LCC resonant converter is especially suitable for the HV pulse converter applications since the conduction angle contributes to the voltage gain. When the conduction angle decreases, the voltage gain increases. For the same voltage gain, the turns ratio of the HV transformer or the stages of the voltage multiplier is reduced.

### 6.3.3 Electrical stress

The electrical stresses on the components are derived under the conditions that the input voltage, output voltage and output power are defined. From (6-28), the resonant current is

$$I_{lm} = \frac{\pi}{2\eta \cos\psi} \cdot \frac{P_o}{V_{in}} \tag{6-41}$$

the voltage of the resonant capacitor is

$$V_{cr} = \frac{\pi}{2\eta \cos\psi} \cdot \frac{P_o}{\omega_s C_r V_{in}} \tag{6-42}$$

Equations (6-41) and (6-42) indicate that the resonant current and series capacitor voltage are inversely proportional to the power factor. To reduce the voltage and current stresses, the power factor selected should be as large as possible.

The voltage stress of the parallel capacitor is

$$V_{cp,\max} = \frac{\pi(1+\cos\theta)}{4\eta \cos\psi \cdot \omega_s C_P} \cdot \frac{P_o}{V_{in}} \tag{6-43}$$

From Fig. 6-6, the RMS value of the transformer secondary side current is calculated by

$$I_{s,RMS} = \frac{I_{Lm}}{k} \sqrt{\frac{2\theta - \sin 2\theta}{4\pi}} \tag{6-44}$$

To analyze the influence of the conduction angle on the RMS value of the transformer secondary side current, utilizing (6-39) and (6-44) to eliminate *K*, gives

$$\frac{I_{s,RMS}}{I_o} = \frac{\eta n P \sqrt{\pi(2\theta - \sin 2\theta)}}{4\sin^2(\frac{\theta}{2})} \tag{6-45}$$

Fig. 6-11 displays an example of the relationship between the RMS value of the secondary side current and conduction angle. In the low conduction angle region, $I_{s,RMS}$ increases dramatically.

Hence, a low $\theta$ is not recommended for reducing the power losses of the HV transformer secondary side.

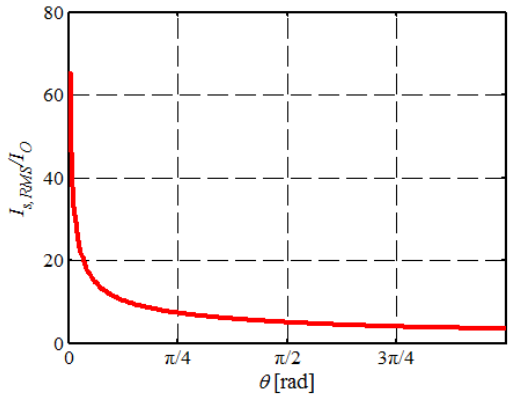



Fig. 6-11 RMS value of the secondary side current versus the conduction angle ($n$=2, $P$=2, $\eta$=1)

### 6.3.4 Design method

A comprehensive HV pulse converter design method is proposed in this section to achieve the required voltage gain at the optimal efficiency, high power density and low voltage and current stress of the components. The design discussed here mainly focuses on the resonant tank and the HV transformer, while components such as the output capacitor and the switching devices are not discussed.

The power factor, conduction angle and quality factor are selected to support the design of the HV pulse converter. In the proposed analytical model, the power factor angle and the conduction angle are two characteristic parameters describing the properties of the HV pulse converter. The voltage gain and the component stresses can be directly calculated from these parameters which is different to the widely adopted design assumption $A=C_p/C_r$. It is not practical to reflect the performance of the HV pulse converter. In addition, a high quality factor of the resonant tank is preferred to produce high fidelity sinusoidal current to reduce the component stress.

Moreover, previous modelling and design approaches usually neglect the power loss of the HV pulse converter. The power losses of the HV high frequency transformer and the rectifier are relatively large, which introduce a large error in the mathematical model. It is very complex to model the power loss of the HV pulse converter and rectifier. Based on test results of previous prototypes, the efficiency of the HV pulse converter circuit at a rated output is usually around $\eta$=0.80. This value could be adopted in the design instead of the complex loss analysis.

In the design, the following specifications need to be given as inputs:

a) Input voltage $V_{in}$, output voltage $V_O$, output current $I_O$;

b) The chosen architecture: Fig. 6-2 offers some advices on the selection of HV pulse converter architecture at different output voltage and power rating. Then the number of

transformers *m* and the polarity of voltage multiplier *P* is determined previously.

c) The HV transformer output voltage $V_{sec}$: Unlike the case of the low voltage transformers, the output voltage of the HV transformer is limited by HV insulation materials and packaging, thus this needs to be determined with priority over other parameters.

Then parameters of the HV pulse converter are calculated step by step. The voltage multiplier stage number *n* is calculated by

$$n = \frac{1}{2P} \cdot \frac{V_o}{V_{sec}} \tag{6-46}$$

From (6-39), the turns ratio of the HV transformer is

$$k = \frac{\sin^2(\frac{\theta}{2})}{2\eta n P \cos\psi} \cdot \frac{V_o}{V_{in}} \tag{6-47}$$

The selection of the values for conduction angle $\theta$ and power factor angle $\psi$ will be discussed later. From (6-29), the parallel capacitor is calculated by

$$C_P = \frac{mnP^2 k_{VM} k^2}{2 f_s R_o \tan^2(\frac{\theta}{2})} \tag{6-48}$$

The equivalent resistor and capacitor values are calculated from (6-29).

The quality factor of the resonant tank is defined as the ratio between the stored energy and dissipated energy in the circuit. For the circuit shown in Fig. 6-4 the quality factor *Q* is calculated by

$$Q = \frac{1 + (\omega_s \mathrm{C}_{tot} \mathrm{R}_{eq})^2}{\mathrm{R}_{eq}} \cdot \sqrt{\frac{L_r}{C_r} + \frac{L_r (\omega_s \mathrm{C}_{tot} \mathrm{R}_{eq})^2}{C_{tot}\left(1 + (\omega_s \mathrm{C}_{tot} \mathrm{R}_{eq})^2\right)}} \tag{6-49}$$

From (6-29), the product $\omega_s C_{tot} R_{eq}$ is expressed by

$$G_\theta = \omega_s C_{tot} R_{eq} = \frac{\pi(1 + \mathrm{k}_c)\mathrm{k}_v^2}{4\eta \tan^2(\frac{\theta}{2})} \tag{6-50}$$

(6-50) demonstrates that $G_\theta$ is only a function of the conduction angle. To simplify the calculation of $G_\theta$, the right side of (6-50) can be approximated by

$$G_\theta \approx \frac{1}{\eta} \cot^2\left(\frac{\theta}{2}\right) \tag{6-51}$$

From (6-33) and (6-49), $L_r$, $C_r$ are given by

$$L_r = \frac{\tan\psi + \sqrt{\tan\psi^2 + 4Q^2}}{2\left(1+G_\theta{}^2\right)} \cdot \frac{R_{eq}}{\omega_s}$$

$$C_r = C_{tot} \cdot \frac{1}{\frac{2Q^2}{G_\theta(\tan\psi + \sqrt{\tan\psi^2 + 4Q^2})} - 1} \cdot \left(1 + \frac{1}{G_\theta{}^2}\right) \tag{6-52}$$

As given in (6-52), to ensure that $C_r$ >0, then the following inequality must be satisfied

$$Q > \sqrt{G_\theta^2 + G_\theta \cdot \tan\psi} \tag{6-53}$$

Equation (6-53) demonstrates that there is a general constraint in the resonant converter independently to the architecture. Fig. 6-12 demonstrates the boundary of (6-53) at cosψ = 0.88. The solid curve is plotted using the exact value of $G_\theta$, while the dashed curve is plotted using the approximated value of $G_\theta$. The $Q$ and $\theta$ values should be selected in the shaded region to give the desired design outputs.

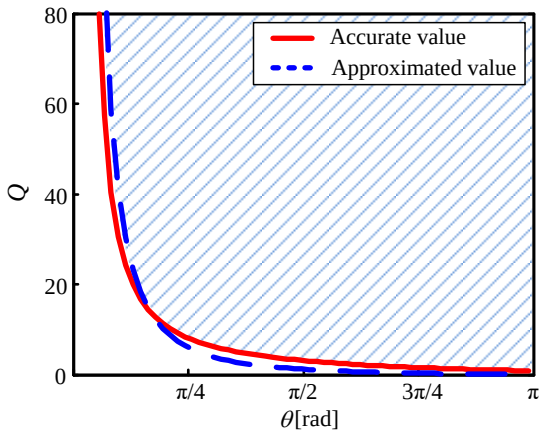



Fig. 6-12 $Q$-$\theta$ curve at $cos\psi$ = 0.88

Generally, $PF$, $Q$ and $\theta$ are determined based on the following considerations:

1) Power factor: A small power factor means a large circulating energy between the resonant tank and the DC source. As a result, the device current stresses and resonant tank conduction losses will increase. The $PF$ is desired to be as large as possible. However, if the power factor angle is near zero, which means that the instant current at the commutation time of the inverter is near zero, then there is not enough energy to ensure soft switching of the switches. Hence, there exists a trade-off in properly selecting a power factor for the resonant tank in the design. In [6-11], the $PF$ = 0.88 is suggested to achieve low circulating energy as well as ensuring ZVS of the inverter.

2) Conduction angle $\theta$: From the voltage gain perspective, the conduction angle should be

selected to be as small as possible in order to reduce the turns ratio of the HV transformer and the stages of the voltage multiplier. However, consequently, the voltage stress of the parallel capacitor and the current of the transformer secondary side is increased. Besides, from Fig. 6-12, the quality factor $Q$ increases dramatically when the conduction angle decreases. Thus, a small conduction angle is not desired in the HV pulse converter. In this thesis, $\theta$=2/3π is empirically selected by experience to balance the voltage gain requirement and stresses of the components.

3) Quality factor $Q$: $Q$ is selected under the premise of (6-53). When $\theta$=2/3π, $Q$>1.27. From (6-52), a large $Q$ value means a large series inductance. The power losses and the volume of the inductor will increase as a result. A low $Q$ value means poor frequency selectivity of the resonant tank, leading to large harmonic resonant currents. So, $Q$ should be selected neither too large nor too small and is suggested in the range of 2.5 to 20 [6-32].

Finally, after selection of $Q$, $PF$ and $\theta$, the parameters to be designed include the turns ratio, the parallel capacitor, the resonant inductor and the capacitor. These can be calculated by (6-48), (6-50). A design flowchart of the HV pulse converter is given in Fig. 6-13.

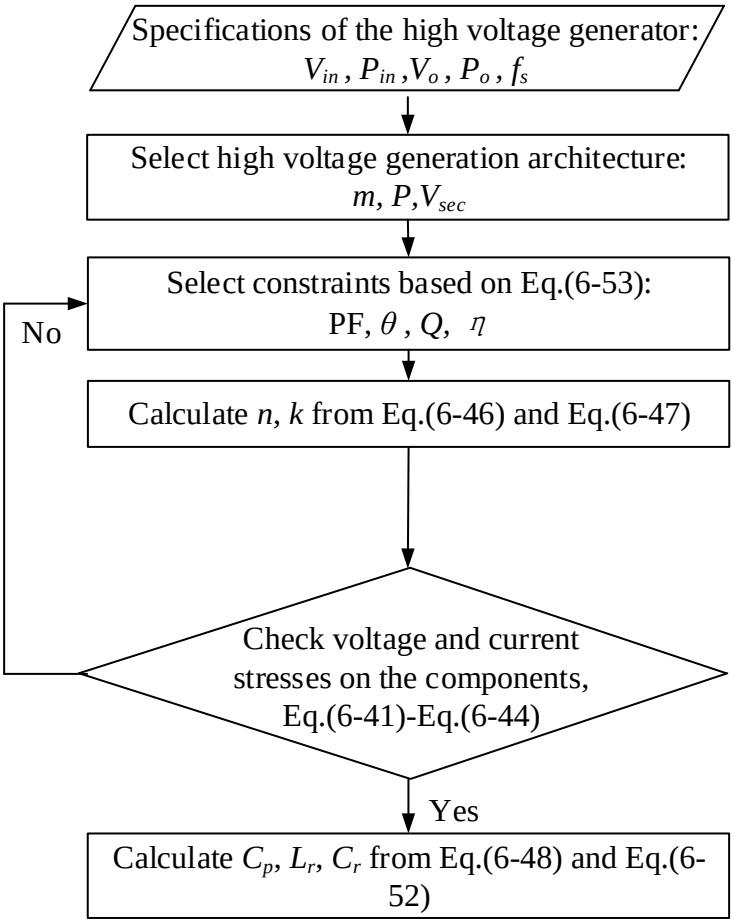



Fig. 6-13 Design flowchart of the HV pulse converter

## 6.4 Experimental results

A 500W 20kV output HV pulse converter with Architecture-4 (HV pulse converter architecture with distributed transformer and multiplier) is designed and built to validate the analysis and design method. The specifications of the HV pulse converter are shown in Table 6-4. The parameters in the design are provided in Table 6-5. Based on the proposed design procedure, the parameters of the HV pulse converter are shown in Table 6-6.

Table 6-4 Specifications of the HV pulse converter prototype

| **Specifications** | **Value** |
|---|---|
| Input voltage $V_{in}$ | 250V |
| Output Voltage $V_o$ | 20kV |
| Output Power $P_o$ | 500W |
| Switching frequency $f_s$ | 400kHz |

Table 6-5 Design constraints

| **Parameters** | **Value** |
|---|---|
| HV transformer output voltage $V_{sec}$ | 1.25kV |
| Conduction angle $\theta$ | $\frac{2\pi}{3}$ |
| Power factor PF | 0.88 |
| Quality factor $Q$ | 4.0 |
| Designed Efficiency $\eta$ | 0.80 |

Table 6-6 Parameters of the designed HV pulse converter prototype

| $m$ | $n$ | $P$ | $k$ | $C_P$/nF | $L_{r\_total}$/μH | $C_r$/nF | $C_o$/nF |
|---|---|---|---|---|---|---|---|
| 2 | 2 | 2 | 4:45 | 3.5 | 88.0 | 2.5 | 1.5 |

HV pulse converter Architecture-4 with modular HV transformers and modular HV rectifiers enables a flexible combination of sub-modules to form higher power or higher output voltage. The centralized packaging of the HV transformer is proposed to fulfil characteristics of Architecture-4. Fig. 6-14 shows the prototype of the HV transformers and voltage multipliers. The HV transformer magnetic core, secondary winding and the voltage multiplier are packaged in an integrated enclosure for compact structure. The two HV transformers share the same primary winding.

The equivalent capacitance $C_p$ is composed of the HV transformer secondary side parasitic capacitance, the diode junction capacitance and added parallel capacitance. In the HV transformer, the measured parallel capacitor is 7pF. A SiC diode is chosen for high frequency switching characteristics and the total diode junction capacitance is 5pF, at 2.5kV. Thus, another 2nF parallel capacitor needs to be added to the primary side to satisfy the designed parallel capacitance. Besides, the measured total leakage inductance of the two HV transformers at the primary side is 2.0μH, thus the added series resonant inductance is 86.0μH.

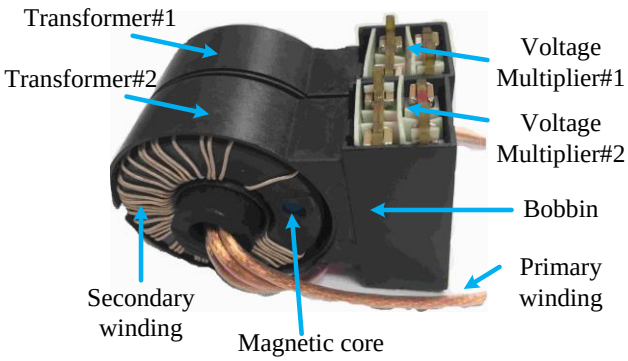



Fig. 6-14 Prototype of the HV transformer and voltage multiplier

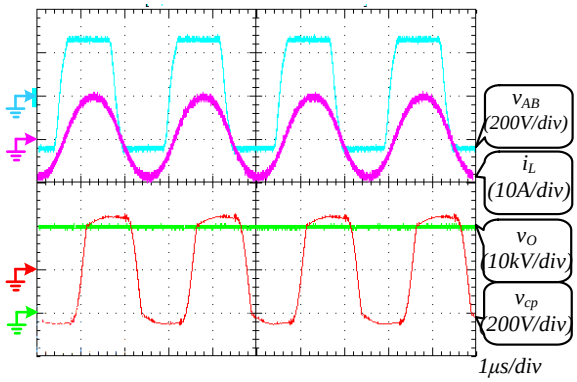



Fig. 6-15 Experimental waveforms at $P_o$ = 500W, $V_o$=20kV, $f_s$=400kHz

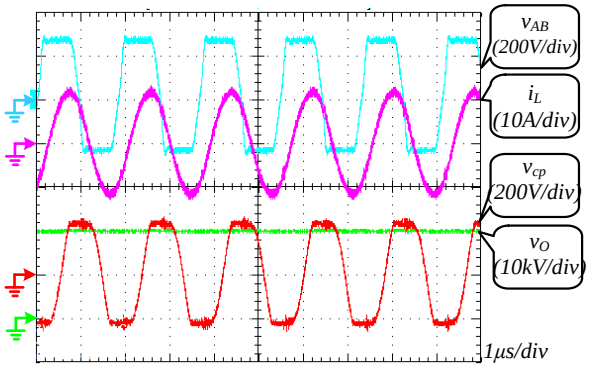



Fig. 6-16 Experimental waveforms at $P_o$ = 125W, $V_o$=20kV, $f_s$=550kHz

Fig. 6-15 illustrates the waveforms at full load and Fig. 6-16 illustrates the light load conditions at the same output voltage. The waveform of the inverter output voltage shows that the soft switching is fully realized at rated and light load conditions. At light load conditions, where the output power is 125W, to maintain the same output voltage, the switching frequency rises to 550kHz. Table 6-7 and Fig. 6-17 give a comparison between the model and the experiments. The results show a high degree of accuracy between the design and experiments in high output power areas, whereas in light load conditions, the error between experiments and calculation is relatively large. Fig. 6-18 gives the frequency response of the output voltage by the experiment and the proposed model. The model matches well with the prototype when the switching frequency is around 400kHz, whereas a larger error occurs when the switching

frequency is below or near to the resonant frequency. The error between the model and the experiment mainly comes from the following aspects:

1) The designed efficiency $\eta$ = 0.8 is not satisfied in light load conditions. Fig. 6-19 gives the efficiency versus the output power curve. From the diagram, it can be seen that when the output power is around 500W, efficiency is around 0.8 and the analytical model gives results with acceptable error. However, when the output power decreases, the efficiency also decreases and the error increases.

2) The proposed model is deduced under ideal conditions. Some non-ideal factors are not included in the model, such as the voltage drop of diodes and the resistance of devices. These factors play a bigger role under light load and bring error between the model and prototype.

Table 6-7 Comparison between the experiment and the model

| $f_s$/kHz | $R_o$/MΩ | $V_o$/kV | | | $I_{Lm}$/A | | |
|---|---|---|---|---|---|---|---|
| | | Experiment | Model | Error | Experiment | Model | Error |
| 400 | 0.75 | 19.16 | 19.30 | 0.73% | 4.80 | 4.86 | 1.27% |
| 425 | 1.05 | 19.50 | 20.01 | 2.62% | 3.91 | 3.84 | -1.82% |
| 450 | 1.35 | 19.69 | 20.18 | 2.49% | 3.33 | 3.36 | 0.86% |
| 465 | 1.50 | 19.55 | 20.17 | 3.17% | 3.15 | 3.15 | 0.07% |
| 482 | 1.80 | 20.09 | 21.10 | 5.03% | 2.95 | 3.03 | 2.78% |
| 504 | 2.10 | 19.28 | 20.91 | 8.45% | 2.71 | 2.95 | 9.03% |
| 520 | 2.40 | 20.14 | 22.39 | 11.17% | 2.58 | 2.90 | 12.29% |
| 539 | 2.70 | 19.68 | 22.99 | 16.82% | 2.42 | 2.87 | 18.74% |
| 550 | 3.00 | 19.83 | 23.30 | 17.50% | 2.37 | 2.94 | 23.84% |

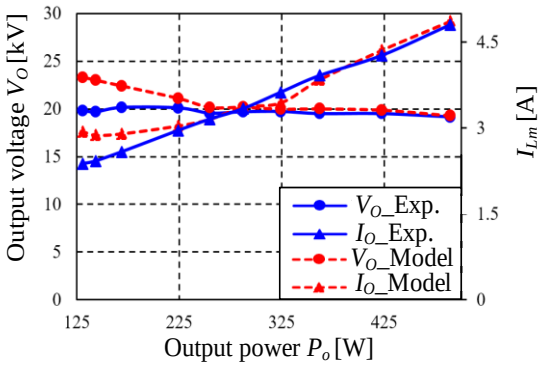



Fig. 6-17 Comparison between the experiments and model

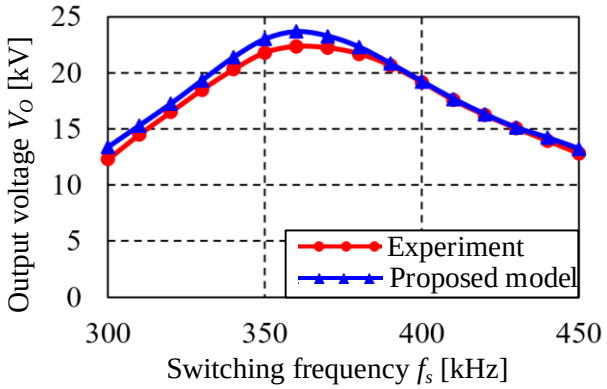



Fig. 6-18 Frequency response of the output voltage by experiment and proposed model

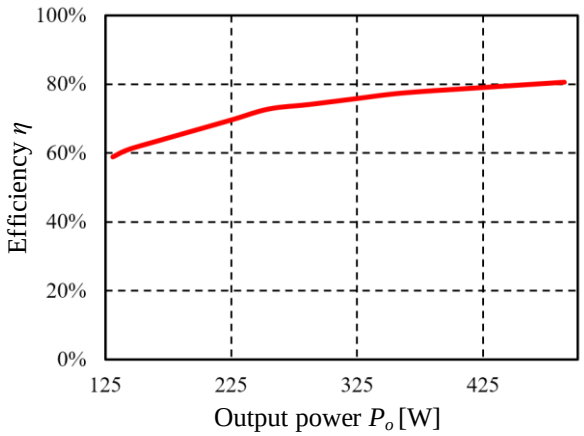



Fig. 6-19 Measured efficiency of the HV pulse converter prototype

Fig. 6-20 gives a comparison between the measured waveform and the equivalent circuit in Fig. 6-8. The purple line represents the experimental results of the resonant current, the blue line represents the calculated resonant current in which the HV pulse converter is replaced by the computed equivalent loading of $R_{eq}$ = 99.1Ω, $C_{tot}$ = 3.58nF.

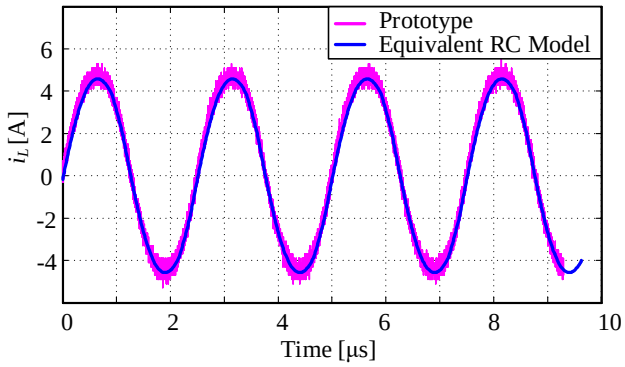



Fig. 6-20 Resonant current comparison between the experimental and the proposed model

## 6.5 Summary

In this chapter, a unified equivalent circuit model is proposed for various HV generator architectures with different voltage multiplier topologies, stage numbers and polarities. These complicated HV structures can be broken down into the basic circuit structure and then a generic equivalent circuit model is derived to simplify the converter analysis and designs. Further analysis of the power factor, the voltage gain of HV pulse converters and electrical stresses of the power components is achieved with the derived RC model. The analysis reveals the inherent circuit properties among HV pulse converters with different configurations. Subsequently, a comprehensive design, considering the power factor, conduction angle and quality factor, is presented which leads to a high efficiency and low components electrical stresses. Furthermore, the parameter selection constraint by power factor, conduction angle and quality factor is derived, which can ensure effective design outputs. Finally, the proposed unified equivalent model and comprehensive design is validated by the experimental results of a 250V input, 20kV output 300W HV pulse converter hardware prototype with modular transformers and voltage multipliers.

## 6.6 References


[6-1] S. R. Jang, H. J. Ryoo, S. H. Ahn, J. Kim and G. H. Rim, "Development and Optimization of High-Voltage Power Supply System for Industrial Magnetron," IEEE Transaction Ind. Electron., vol. 59, no. 3, pp. 1453-1461, Mar. 2012.

[6-2] M. G. Giesselmann, T. T. Vollmer and W. J. Carey, "100-kV High Voltage Power Supply with Bipolar Voltage Output and Adaptive Digital Control," IEEE Transaction Plasma Sci., vol. 42, no. 10, pp. 2913-2918, Oct. 2014.

[6-3] M. Jaritz, S. Blume, D. Leuenberger and J. Biela, "Experimental Validation of a Series Parallel Resonant Converter Model for a Solid State 115-kV Long Pulse Modulator," IEEE Transaction Plasma Sci., vol. 43, no. 10, pp. 3392-3398, Oct. 2015.

[6-4] S. Mao, C. Li, W. Li, J. Popovic and J. Ferreira, “Review of High Frequency High Voltage Generation Architectures,” accepted for Proc. IEEE 14th Int. Conf. on Power Electronics - ECCE Asia, Jun. 2017.

[6-5] I. Batarseh, R. Liu, C. Q. Lee and A. K. Upadhyay, "Theoretical and experimental studies of the LCC-type parallel resonant converter," IEEE Transaction Power Electron., vol. 5, no. 2, pp. 140-150, Apr. 1990.

[6-6] R. Yang, H. Ding, Y. Xu, L. Yao and Y. Xiang, "An Analytical Steady-State Model of LCC type Series‐Parallel Resonant Converter with Capacitive Output Filter," IEEE Transaction Power Electron., vol. 29, no. 1, pp. 328-338, Jan. 2014.

[6-7]J. A. Martin-Ramos, A. M. Pernia, J. Diaz, F. Nuno and J. A. Martinez, "Power Supply for a High-Voltage Application," IEEE Transaction Power Electron., vol. 23, no. 4, pp. 1608-1619, July 2008.

[6-8] J. A. Martin-Ramos, J. Diaz, A. M. Pernia, J. M. Lopera and F. Nuno, "Dynamic and Steady-State Models for the PRC-LCC Resonant Topology with a Capacitor as Output Filter," IEEE Transaction Ind. Electron., vol. 54, no. 4, pp. 2262-2275, Aug. 2007.

[6-9] F. Cavalcante and J. W. Kolar, “Design of a 5kW high output voltage series-parallel resonant DC–DC converter,” in Proc. IEEE 34th Annu. Conf. Power Electron. Spec. (PESC 2003), Jun. 15–19, vol. 4, pp. 1807– 1814.

[6-10] T. B. Soeiro, J. Mühlethaler, J. Linnér, P. Ranstad and J. W. Kolar, "Automated Design of a High-Power High-Frequency LCC Resonant Converter for Electrostatic Precipitators," IEEE Transaction Ind. Electron., vol. 60, no. 11, pp. 4805-4819, Nov. 2013.

[6-11] D. Fu, F. C. Lee, Y. Qiu and F. Wang, "A Novel High-Power-Density Three-Level LCC Resonant Converter with Constant-Power-Factor-Control for Charging Applications," IEEE Transaction Power Electron., vol. 23, no. 5, pp. 2411-2420, Sept. 2008.

[6-12] J. S. Brugler, "Theoretical performance of voltage multiplier circuits," IEEE J. Solid-State Circuits, vol. 6, no. 3, pp. 132–135, Jun. 1971.

[6-13] W. C. Hsu, J. F. Chen, Y. P. Hsieh and Y. M. Wu, "Design and Steady-State Analysis of Parallel Resonant DC – DC Converter for High-Voltage Power Generator," IEEE Transaction Power Electron., vol. 32, no. 2, pp. 957-966, Feb. 2017.

[6-14] L. Katzir and D. Shmilovitz, "A Matrix-Like Topology for High-Voltage Generation," IEEE Transaction Plasma Sci., vol. 43, no. 10, pp. 3681-3687, Oct. 2015.

[6-15] L. Malesani and R. Piovan, "Theoretical performance of the capacitor-diode voltage multiplier fed by a current source," IEEE Transaction Power Electron., vol. 8, no. 2, pp. 147-155, Apr. 1993.

[6-16] S. S. Lee, S. Iqbal and M. Kamarol, "Control of ZCS-SR Inverter-Fed Voltage Multiplier-Based High-Voltage DC – DC Converter by Digitally Tuning Tank Capacitance and Slightly Varying Pulse Frequency," IEEE Transaction Power Electron., vol. 27, no. 3, pp. 1076-1083, Mar. 2012.

[6-17] S. Mao, "A high frequency high voltage power supply," in Proc. EPE, Birmingham, U.K., 2011, pp. 1-5.

[6-18] M. Hu, N. Froehleke, W. Peters and J. Boecker, "Multi-objective optimization of LCC resonant converter applied in VLF HV pulse converter," in Proc. 37th Annu. Conf. IEEE Ind. Electron. Soc., Melbourne, VIC, 2011, pp. 1456-1461.

[6-19] Z. Cao, M. Hu, N. Fröhleke and J. Böcker, "Modeling and Control Design for a Very Low-Frequency High-Voltage Test System," IEEE Transaction Power Electron., vol. 25, no. 4, pp. 1068-1077, Apr. 2010.

[6-20] L. Katzir and D. Shmilovitz, "A split-source multisection high-voltage power supply for X-ray," IEEE J. Emerg. Sel. Topics Power Electron., vol. 4, no. 2, pp. 373–381, Jun. 2016.

[6-21] A. J. Gilbert, C. M. Bingham, D. A. Stone and M. P. Foster, "Normalized Analysis and Design of LCC Resonant Converters," IEEE Transaction Power Electron., vol. 22, no. 6, pp. 2386-2402, Nov. 2007.

[6-22] N. Shafiei, M. Pahlevaninezhad, H. Farzanehfard and S. R. Motahari, "Analysis and Implementation of a Fixed-Frequency LCLC Resonant Converter with Capacitive Output Filter," IEEE Transaction Ind. Electron., vol. 58, no. 10, pp. 4773-4782, Oct. 2011.

[6-23] Y. A. Ang, C. M. Bingham, M. P. Foster, D. A. Stone, and D. Howe, "Design oriented analysis of fourth-order LCLC converters with capacitive output filter," IET Power Electron., vol. 152, no. 2, pp. 310–322, 2005.

[6-24] N. Shafiei, M. Pahlevaninezhad, H. Farzanehfard, A. Bakhshai and P. Jain, "Analysis of a Fifth-Order Resonant Converter for High-Voltage DC Power Supplies," IEEE Transaction Power Electron., vol. 28, no. 1, pp. 85-100, Jan. 2013.

[6-25] F. Cavalcante and J. W. Kolar, “Small-signal model of a 5kW high output voltage capacitive-loaded series-parallel resonant DC-DC converter,” in Proc. Power Electron. Spec. Conf., 2005, pp. 1271–1277.

[6-26] L. Dalessandro, F. da Silveira Cavalcante and J. W. Kolar, "Self-Capacitance of High-Voltage Transformers," IEEE Transaction Power Electron., vol. 22, no. 5, pp. 2081-2092, Sept. 2007.

[6-27] Y. Du, J. Wang, G. Wang and A. Q. Huang, "Modeling of the High-Frequency Rectifier With 10-kV SiC JBS Diodes in High-Voltage Series Resonant Type DC – DC Converters," IEEE Transaction Power Electron., vol. 29, no. 8, pp. 4288-4300, Aug. 2014.

[6-28] S. R. Sanders, J. M. Noworolski, X. Z. Liu and G. C. Verghese, "Generalized averaging method for power conversion circuits," IEEE Transaction Power Electron., vol. 6, no. 2, pp. 251-259, Apr. 1991.

[6-29] V. A. Caliskan, O. C. Verghese and A. M. Stankovic, "Multifrequency averaging of DC/DC converters," IEEE Transaction Power Electron., vol. 14, no. 1, pp. 124-133, Jan. 1999.

[6-30] J. A. Martin-Ramos, J. Diaz, A. M. Pernia, M. J. Prieto and F. F. Linera, "Modelling of the PRC-LCC resonant topology with a capacitor as output filter using EDF," in Proc. IEEE 33th Annu. Conf. Power Electron. Spec. (PESC 2002), Jun. 2002, vol.3, pp. 1337-1342.

[6-31] G. Ivensky, A. Kats and S. Ben-Yaakov, "An RC load model of parallel and series-parallel resonant DC-DC converters with capacitive output filter," IEEE Transaction Power Electron., vol. 14, no. 3, pp. 515-521, May. 1999.

[6-32] Gilbert, "Analysis, design and control of LCC resonant power converters," Ph.D. dissertation, Dept. of Electronic and Electrical Engineering, University of Sheffield, Sheffield, UK, 2007.

[6-33] J. Wang, S. W. H. de Haan and J. A. Ferreira, "Detailed Derivation and Minimization of the Equivalent Parasitic Capacitances of a High-Voltage Multiplier Based on the Complete Model," IEEE Transaction on Industry Applications, vol. 51, no. 1, pp. 362-372, Feb. 2015

# Chapter 7
# Conclusions and recommendations

## 7.1 Conclusions

As mentioned in Chapter 1, modular HV pulse converter technology with fast rise and decay times is addressed in this thesis to improve the HV pulse converter performance for X-ray generation, electrostatic precipitation, HV capacitor charger and other applications. In this thesis, a systematic approach is derived to evaluate different HV architectures for the HV pulse converter. The key subcomponents such as HV transformer and voltage multiplier for the modular HV pulse converter are investigated. A unified equivalent steady-state circuit modelling approach and comprehensive design procedure for the LCC resonant based modular HV pulse converter is developed. The conclusions of this thesis are presented as follows:

**A classification methodology to identify optimal HV architecture for a multi-kW 100kV pulse converter system supplying short rise and decay-time pulses**

A systematic methodology is derived to classify HV architectures based on the modularization level of power building blocks for the HV pulse converter. A new HV architecture with multiple inverters, single transformer, and multiple rectifiers configuration is generated. Furthermore, all HV architectures are evaluated to provide an architecture selection guideline at different output voltage and power outputs rating. The HV architecture with a single inverter, multiple transformers, and multiple rectifiers configuration gives the best overall performance for efficiency, power density, HV ripple, HV pulse rise and decay time, HV insulation and modularity compared with other architectures with the single inverter configuration. Similarly, the full distributed HV architecture with multiple inverters, multiple transformers and multiple rectifiers configuration outperforms the other architectures with a multiple inverters configuration for medium to high power rating applications. In summary, the conclusion is that modular HV architectures with multiple transformers and multiple rectifiers configuration are identified as the most promising architecture candidates to achieve the best performance for the HV pulse converter.

**The effect of modularization and increasing switching frequency, as well as insulation stress analysis for a planar and wire-wound structure HV transformer**

The advantages of modularization for HV transformers for the HV pulse converter are identified. The modularization of HV transformers provide advantages such as low insulation stress, low dielectric loss and distributed thermal stress. Furthermore, the modularization of HV transformers achieves a size reduction at increasing frequency without any sacrifice on efficiency. It also provides the advantages of modular structures, scalability for to the different HV pulse converter rating and ease of assembly and manufacturing. The equivalent circuit diagram is derived to better understand the trade-off for modular HV architecture with multiple HV transformers and voltage multipliers. High frequency achieves a size reduction of passive

components in the HV tank. Low loss magnetic material, winding technology and insulation materials with low dissipation factor need to be considered at the increasing frequency. The frequency for achieving the minimum power loss of the HV tank for different architectures will be different. The HV transformer insulation design guideline is provided by the HV AC and DC insulation stress analysis for planar and wire-wound structures. Finally, prototype experimental results validate the analysis of the high frequency HV transformer for the modular HV architecture.

**The key influence factors of HV pulse rise and decay times, diode reverse recovery effect and mitigation method for multi-stage half-wave(HW) Cockcroft–Walton (CW) multiplier circuit**

The key factors that influence the rise and decay times of multistage voltage multiplier circuit are analysed and experimentally verified. The pulse rise times lengthen when more voltage multiplier circuit stages are used. The voltage rating of the HV transformer and voltage multiplier stage number need to be optimized for the best performance. Once the voltage multiplier stage number is determined, the switching frequency becomes the most important influence factor for the HV pulse rise times. A higher switching frequency will lead to shorter pulse rise times. Load resistance and filter capacitor have little influence on the pulse rise times. The HV pulse decay times are proportional to the load resistance and multiplier capacitance. High switching frequency can effectively reduce the HV pulse rise and decay times. Experimental work shows that the multiplier diode reverse recovery problem is the bottle neck for further increasing the circuit operation switching frequency to achieve high power density, short rise and decay times pulse operation. The multiplier diode reverse recovery problem is mainly caused by the diodes in the first stage voltage multiplier. The most effective and economic way to alleviate the diode reverse recovery problem is by employing diodes with good reverse recovery performance such as silicon carbide Schottky diodes, but only in the first stage.

**Generic steady state circuit model and design methodology for modular HV pulse converter architectures**

A unified equivalent circuit model for the series-parallel (LCC) resonant converter based HV pulse converter with different architectures, voltage multiplier stages and polarity numbers is developed. The unified equivalent circuit model provides a universal analysis and design of a family of the LCC resonant converter based HV generation. The steady-state, unified equivalent resistor and capacitor (RC) model is derived to replace the complex HV transformers and rectifiers. The analysis of the power factor, voltage gain and electrical stresses of the LCC resonant converter with equivalent circuit model reveals inherent circuit properties among HV pulse converters with different architectures. Subsequently, a comprehensive design methodology considering the power factor, conduction angle and quality factor of the LCC resonant converter is provided. This leads to high efficiency and low components electrical stresses. Furthermore, the parameter selection constraint by power factor, conduction angle and quality factor is derived, which can ensure effective design outputs. Finally, the experimental results of a 250V input, 20kV output 300W HV pulse converter hardware

prototype with modular HV transformers and voltage multipliers validate the unified equivalent circuit model and comprehensive design methodology.

## 7.2 Thesis contributions

The scientific contributions of this thesis are summarized as follows:

*1)* A systematic methodology to classify the HV pulse converter architectures, and identify the modular architectures with multiple transformers and multiple rectifiers as the most promising architecture candidates for the best performance such as high efficiency, short rise and decay-time pulse, high power density, low insulation stress, low voltage ripple and modularity.

2) The effects of modularization and increasing frequency on the HV transformer have been investigated for the modular HV pulse converter architectures. The insulation stress for a planar and wire-wound structure HV transformer has been investigated to provide an insulation design guideline.

3) The key influence factors for HV pulse rise times in multi-stage HV half-wave (HW) Cockcroft-Walton (CW) multiplier circuit have been proved to be the voltage multiplier stage number and switching frequency The HV pulse decay time is proportional to load resistance and voltage multiplier capacitance. High switching frequency can effectively reduce the HV pulse rise and decay time.

4) It is proved that the voltage multiplier diode reverse recovery cause comes from the diodes in the first stage voltage multiplier. The most effective and economic way to alleviate the diode reverse recovery problem at high frequency has been developed by employing diodes without reverse recovery such as silicon carbide Schottky diodes only in the first voltage multiplier stage.

5) A generic steady state equivalent circuit model has been derived to simplify the design and analysis of the HV pulse converter with different architectures, voltage multiplier stages and polarity numbers.

6) The systematic design methodology considering the power factor, conduction angle and quality factor of the LCC resonant tank is developed to achieve low components electrical stresses and high efficiency.

## 7.3 Recommendations for future research

**Characterization and analytical modelling of the frequency dependent dielectric loss for the HV insulation materials used in high frequency HV transformer at specific operating frequency, voltage and temperature range**

Since the dielectric loss constitutes a large part of loss in the HV transformer at high frequency and high ambient temperature, it is desirable to accurately model and predict the dielectric loss for the HV insulation materials such as PCB substrate, mineral oil, as well as epoxy resin and other solid insulation materials used in high frequency HV transformers, so the total loss and temperature rise of HV transformer can be determined and controlled to avoid a thermal runaway for reliable operation.

**Optimal capacitance distribution methods for multi-stage CW voltage multiplier to achieve short rise and decay times pulse and low output voltage ripple**

The capacitance of the multi-stage CW voltage multiplier not only influences the dynamic HV pulse quality, but also impacts on steady state performance such as voltage drop and voltage ripple. The optimal capacitance values per voltage multiplier stage will provide a possibility to improve the HV pulse performance at dynamic and steady state, and minimize the size and cost of the multi-stage CW voltage multiplier for the HV pulse converter.

**Power unbalanced analysis and power sharing methods for the elementary HV tank for the modular HV pulse converter**

The variance of HV transformer parasitic including magnetizing inductance, leakage inductance, winding capacitance due to the magnetic core material characteristics difference and inconsistent assembly and manufacturing process will lead to voltage and current sharing challenges for modular HV pulse converter architectures. Furthermore, the variance of the multiplier capacitor and the parasitic capacitance and inductance of the HV multi-stage multiplier circuits will also impact on the voltage and current sharing for modular HV pulse converter architectures. To avoid overstress such as insulation stress or thermal stress for the HV tank of HV pulse converter, it is worth investigating the power unbalance due to the parameter variance of the modular HV tank. The passive and active power unbalance mitigation methods are to be investigated for the modular HV pulse converter.

**Thermal management of the modular HV pulse converter**

To prevent a thermal runaway and insulation materials' failures of the HV tank in the HV pulse converter, the thermal model of the entire HV tank and key subcomponents such as the HV transformer and voltage multiplier of the HV tank in an oil immersed enclosure need to be accurately built and validated. Active cooling methods for the HV tank can help to further improve the power density and reliability of the HV pulse converter.

**HV pulse converter system packaging and integration**

The interconnection of key subcomponents such as the HV transformer and voltage multiplier of the HV tank, and interconnection between the HV tank and inverter, as well as other circuits can be further optimized from system level packaging to increase the power density and reliability of a HV pulse converter. The integration of subcomponents will help to simplify the interconnection and improve the power density. For example, the winding of a planar resonant inductor and primary PCB winding of the planar HV transformer can be integrated together with a multilayer PCB or high frequency inverter. The secondary PCB winding of a planar HV transformer is possible to integrate with the HV multiplier PCB.

# Appendix

# Technology demonstrators of the modular HV pulse converter

## A.1 Technology demonstrator of a 4kW 140kV modular HV pulse converter prototype with distributed planar HV transformers

A technology demonstrator of a 4kW 140kV modular HV pulse converter prototype with distributed planar HV transformers is built in the lab. The circuit diagram is shown in Fig. A-1 and the simplified circuit diagram of the modular HV pulse converter architecture is illustrated in Fig. A-2. A hardware prototype of a 4kW 300kHz 140kVDC HV power supply with the modular planar transformer architecture is built to validate the concept. The primary and secondary parts of the planar transformer are separated with a 1.5 mm polypropylene layer between the primary and secondary parts for 40kVDC insulation capability.

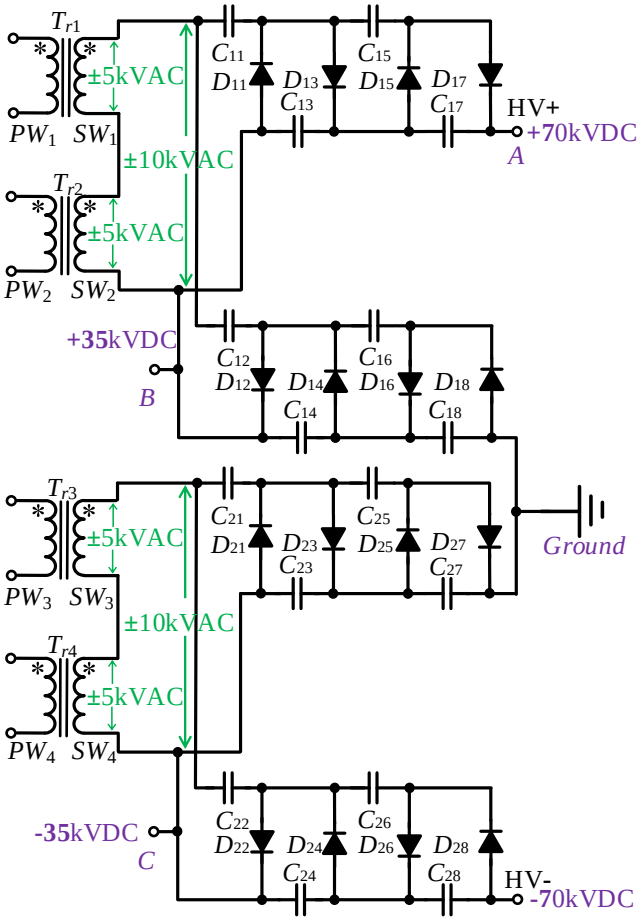



Fig. A-1 Circuit diagram of the modular HV pulse converter architecture

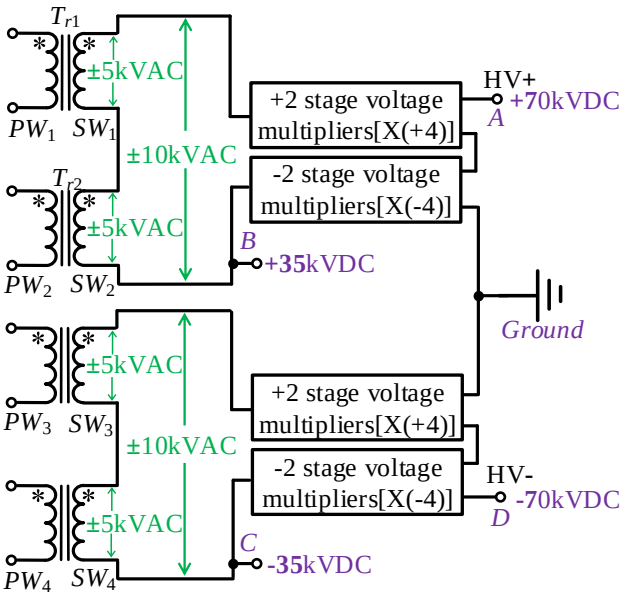


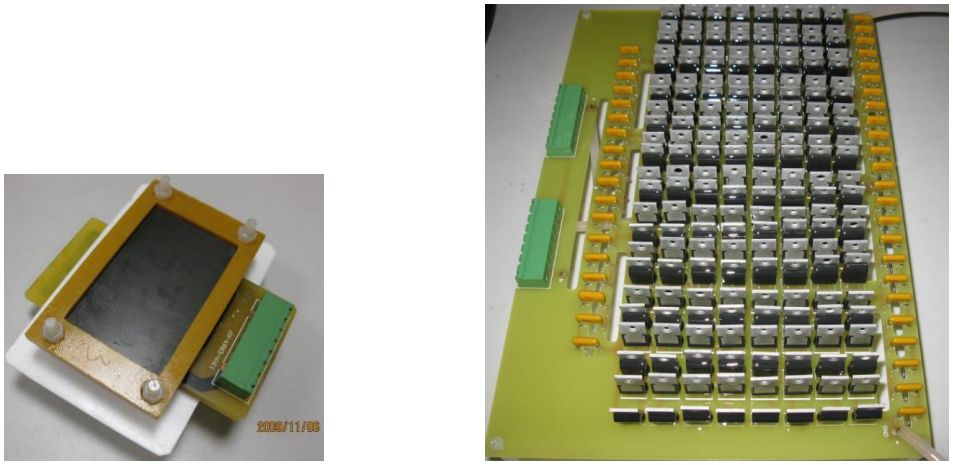

Fig. A-2 Simplified circuit diagram of the modular HV pulse converter architecture

Other devices used for the prototype are:

- MOSFET: ST STW20NM60FD, 600V rating, two parts in parallel
- Resonant inductor: 25.2nF
- Resonant capacitor: 3.9uH
- Multiplier diode: CREE C2D20120D, 1.2kV rating, twenty four parts in series.
- Multiplier capacitor: AVX 5kV, 0.39nF, four parts in series

A prototype photo of the HV pulse converter with modular architectures and the planar transformer and voltage multipliers (positive HV half part) is shown in Fig. A-3. The key experimental waveforms at 300kHz 4kW 140kVDC are provided in Fig. A-4. The tested efficiency is above 86.5% at 300kHz 4.08kW full power, 141.76kVDC rated output voltage.

The modular high frequency HV pulse converter architecture with the planar transformer behaves with even voltage distribution, reduced high frequency AC stress, easy insulation design and good thermal performance. The transformer equivalent circuit model for the modular HV pulse converter architecture with multi-module transformers are discussed. A 300kHz 4kW 140kVDC HV pulse converter prototype with modular architecture and a planar transformer is built and the experimental results are provided to validate the design and analysis.



(a) HV planar transformer (b) HV multiplier with 1.2HV SiC diodes

Fig. A-3 A prototype photo of the HV pulse converter with modular architecture and the planar HV transformer

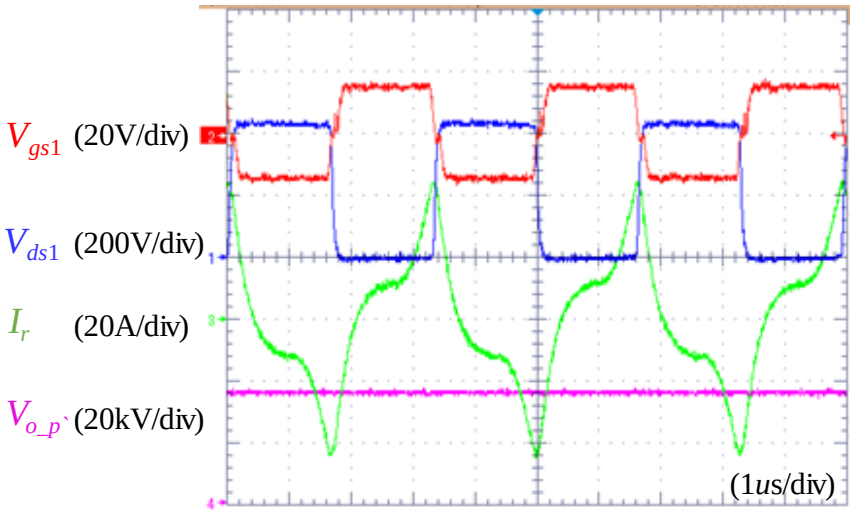



Fig. A-4 Key experimental waveforms at 300 kHz, 140kVDC

## A.2 Technology demonstrator of a 2kW 110kV modular HV pulse converter prototype with distributed non-planar wire wounded toroid core based HV transformers

The demonstrator of the voltage multiplier for a HV pulse converter with 2kW output power, 110kV output voltage and a switching frequency of 300kHz. HV pulse converter prototype is built in the laboratory to demonstrate the advantages of fast HV pulse speed, high efficiency and high power density compared with a conventional 40kHz HV pulse converter.

**Design considerations**

The circuit diagram of the conventional 40kHz HV pulse converter based on the HV pulse converter architecture with a single inverter, single transformer and multiple HV rectifications is illustrated in Fig. A-5. The legacy design relies on the centralized HV transformer with one

primary winding and two secondary windings together with two voltage doubler circuits to provide the voltage step-up. The output voltage of the secondary winding of the HV transformer is around 20kV. A 30kV 2.1nF, cylinder HV film capacitor is used as the capacitor for voltage doubler circuit. Five 10kV HV diodes 2CL2FM with axial lead, Φ4.3mm, 15mm length are series connected for the unit rectifier of the voltage doubler circuit.

The circuit diagram for a 300kHz 2kW 110kV HV pulse converter prototype is based on the modular HV pulse converter architecture with a single inverter, multiple transformers and multiple HV rectifiers as shown in Fig. A-6. The circuit diagram of the elementary power building block with dual polarity positive and negative three stage half wave Cockcroft-Walton voltage multipliers for a 300kHz frequency 2kW 110kV HV pulse converter prototype is illustrated in Fig. A-6. The voltage rating for the elementary power building block with dual polarity positive and negative three stage half wave Cockcroft-Walton voltage multipliers shown in Fig. A-7 have been reduced to around 7kV. As a result, the AC output voltage of elementary HV transformer can be reduced to below 1 kV. With reduced turns ratio for the HV transformer, the parasitic capacitance of the HV transformer can be reduced by more than four times compared with the legacy 40kHz design. The high frequency AC insulation design will become more straightforward, the high frequency AC insulation stress is 1/20 of 40kHz design. The high frequency AC dielectric loss can be significantly reduced.

Based on the calculations, the maximum magnetic flux density of the toroid ferrite core R41.8×26.2×12.5 with N87 material from EPCOS is 0.75mT. The primary winding turns number and secondary winding turns number of the HV transformer are three and forty-five respectively. Litz wires 14 AWG 5X5X42/44 and 24 AWG 3/35/44 are used for the HV transformer primary and secondary windings for 300 kHz ~500 kHz frequency operations. To guarantee sufficient insulation above 20kV/mm, 3mm polypropylene cylindrical insulation and mineral oil are placed between the transformer's primary to secondary winding. The toroid ferrite core is electrical floating, and insulated with HV transformer secondary windings with plastic bobbins.

The ultrafast recovery diode or Silicon carbide Schottky diodes without recovery are preferred for this high frequency range with low power losses. Furthermore, the HV tank will be submerged in the insulation oil, the oil temperature can be as high as 80$^{o}$C. Based on a continuous power characterization test of the diode for the elementary HV pulse converter unit, only Silicon carbide Schottky diode without reverse recovery and ultrafast silicon diodes with 30ns reverse recovery time can meet the requirements without any thermal runaway. The highest voltage rating for an ultrafast silicon diode with 30ns reverse recovery time is 600V. So more than ten pieces of 600V Vishay USB 260 silicon diodes need to be connected in series to achieve above 5.5kV voltage rating. In total, eighty pieces of 600V Vishay USB 260 silicon diodes are required for a 10kV elementary HV pulse converter unit. However, due to the limited size of voltage multiplier circuit boards inside the HV tank, silicon diodes cannot be accepted.

The HV rectifier capacitance can be largely reduced at a higher switching frequency. It will provide a faster HV pulse speed with reduced HV rectifier capacitance. With modular architecture, the voltage stress for the capacitors and diodes in the HV rectifier can be

significantly reduced by eight times. Low voltage rating surface mounted package ceramic capacitors and diodes can be used to achieve size reduction for the HV rectifier board.

Table A-1 provides the summary of the key parameters for a 40kHz and 300kHz 110kV HV pulse converter prototype. The size of the 40kHz and 300kHz 110kV HV rectifier prototype is given in Table A-2. HV rectifier prototype photos for the 2kW 110kV HV pulse converter prototype are given in Fig. A-8. The size comparisons of the 40kHz and 300kHz 2kW 110kV HV rectifier prototypes is given in Table A-2.

The 300kHz 2kW 110kV HV pulse converter prototype outperform the 40kHz 2kW 110kV HV pulse converter prototype when considering HV pulse speed, HV rectifier size and HV pulse converter efficiency perspectives. The prototype performance results validate the advantages of the high frequency modular HV pulse converter architecture. Compared with the 40kHz operation, the 300kHz modular design can achieve the following advantages:

- About five times shorter HV pulse rise times
- About three times shorter HV pulse decay times
- About seven times size reduction for the HV rectifier board
- 5~10% higher efficiency higher efficiency for the HV pulse converter

The improved HV pulse converter pulse speed will enable more system benefits.

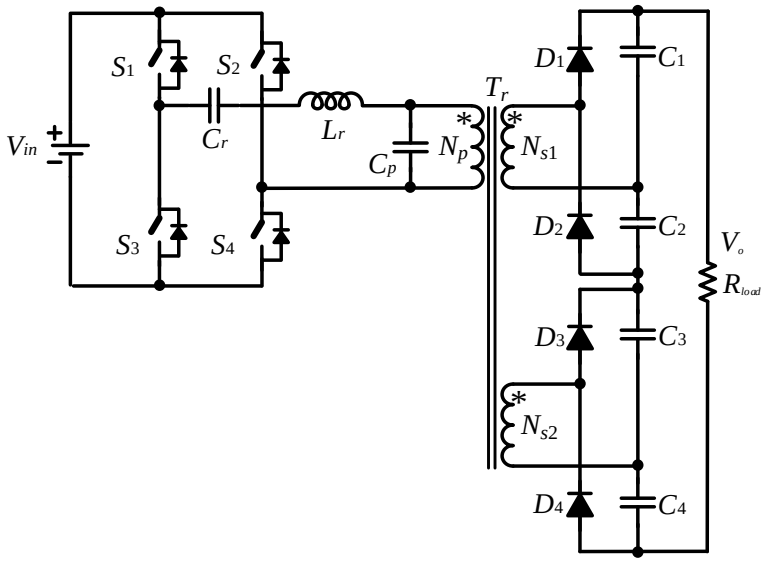



Fig. A-5 Circuit diagram for the 40kHz frequency 2kW 110kV HV pulse converter prototype

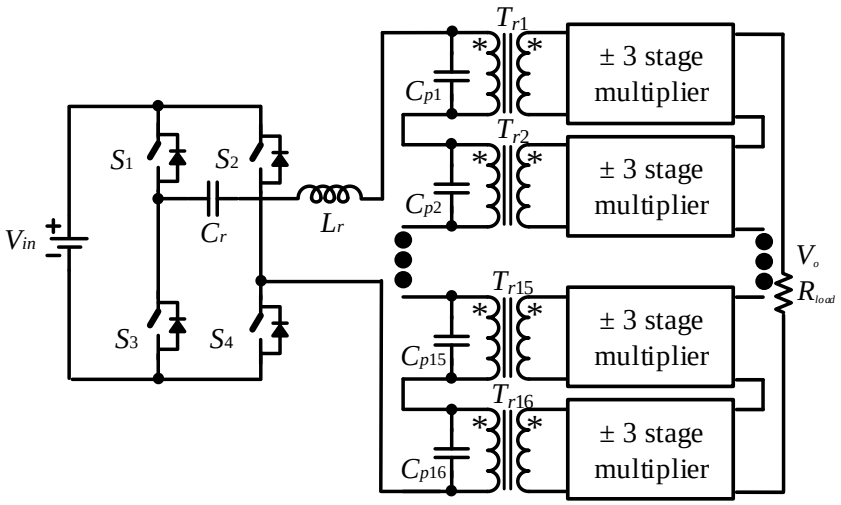



Fig. A-6 Circuit diagram for the 300kHz frequency 2kW 110kV HV pulse converter prototype

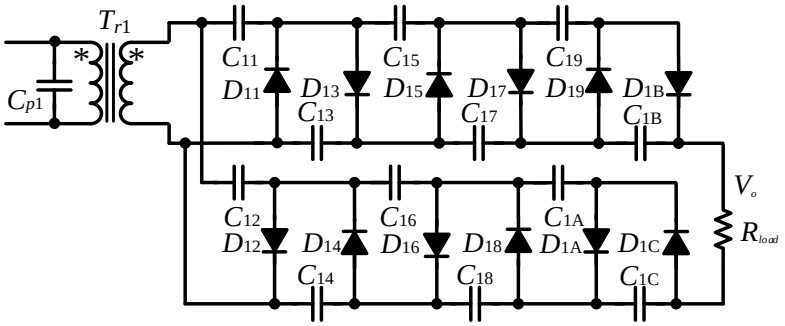
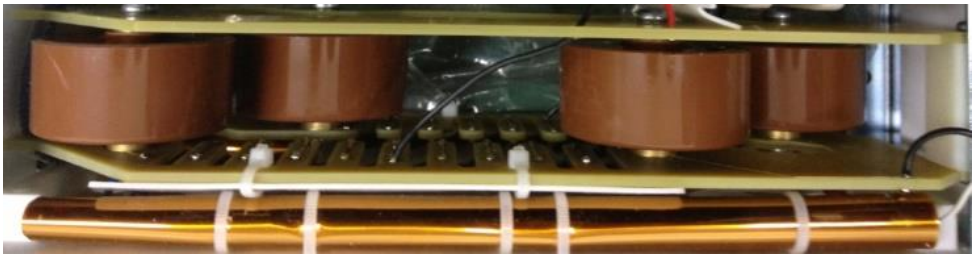


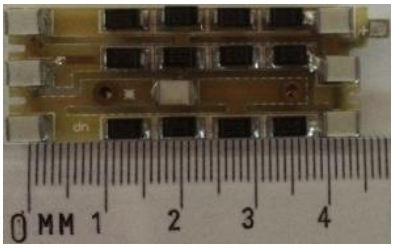

Fig. A-7 Circuit diagram of the elementary power building block with dual polarity positive and negative three stage half wave Cockcroft-Walton voltage multipliers

Table A-1 key parameters for the 40kHz and 300kHz 2kW 110kV HV pulse converter prototypes

| Key parameters | 40kHz frequency porotype | 300kHz frequency prototype |
|---|---|---|
| Input voltage | 300VDC | 300VDC |
| Output voltage | 110kVDC | 110kVDC |
| Output power | 2kW | 2kW |
| Architecture | Single inverter+single HV transformer(1P2S)+voltage doubler | Single inverter+16 HV transformer(1P1S)+16 voltage multipliers(3 stage) |
| HV transformer turns ratio | 8:1000:1000<br>Lp=119.62uH, Lp(lk)=1.52uH,<br>Ls1=1533mH, Ls2=1521mH<br>Cp=7.78nF | 3:68<br>Lp=22.86uH, Lp(lk)=0.55uH<br>Ls=11.92mH<br>Cp=1.6nF |
| HV multiplier | Capacitor: 2.1nF/30kV, cylinder<br>Diode: 2CL2FM, 10kV, 5 in series, Axial Lead, Φ4.3mm×15mm | Capacitor: 0.47nF/3kV, 1825 package, 2 in series Diode: BYG23T, 1.3kV, SMA, 4 in series |



(a) 40kHz HV doubler




(b) 300kHz 3 stage multiplier

Fig. A-8 HF rectifier prototype photo for the 40kHz and 300kHz 2kW 110kV HV pulse converter prototypes

Table A-2 size of 40kHz and 300kHz 2kW 110kV HV rectifier prototypes

| | 40kHz frequency HV voltage doubler prototype | 300kHz frequency HV voltage multiplier prototype |
|---|---|---|
| Size for HV rectifier power building block | 23cm*10cm*6cm | 4.6cm*1.7cm*0.7cm for elementary single polarity multiplier power building block |
| Volume for total HV rectifier | 1.38L | 0.18L |

## A.3 Technology demonstrator of an 8kW 110kV modular HV pulse converter prototype with distributed non-planar wire wound toroid core based HV transformers

The circuit diagram of a 40kHz 8kW 110kV HV pulse converter prototype is the same as the 40kHz 2kW 110kV HV pulse converter prototype. Fig. A-9 shows the circuit diagram for the 300kHz 8kW 110kV HV pulse converter prototype. It is based on the HV pulse converter architecture with a single inverter, multiple transformers and multiple HV rectifiers. With higher output current and out power for the high frequency HV pulse converter, the power loss of the multi-stage voltage multipliers will increase. The 300kHz 8kW 110kV HV pulse converter prototype is built in the laboratory to provide the design considerations and demonstrate the advantages of short HV pulse times and high power density compared with the conventional 40kHz 8kW 110kV HV pulse converter. Since the output current and power is much larger for the 8kW 110kV HV pulse converter prototype compared with the 2kW 110kV HV pulse converter prototype, two stage voltage multipliers shown in Fig. A-10 are

used to reduce the power loss for the multiplier circuits compared with three stage voltage multipliers for the 300kHz 2kW 110kV HV pulse converter. The AC output voltage of the elementary HV transformer can be reduced to below 2 kV, which is more than ten times lower than 40kHz design. Furthermore, with a reduced turns ratio, the parasitic winding capacitance of the HV transformer can be significantly reduced and the reactive power for the inverter can be also reduced.

To achieve compact packaging for the HV multiplier circuit boards, a surface mounted ceramic capacitor is used together with a surface mounted SiC Schottky diode. The new emerging surface mounted 1.2kV, 1A SiC Schottky diode GB01SLT12-21 from Genesic is quite promising for achieving high power density and operates at high frequency elevated temperature environments. Compared with the ten pieces of 600V Vishay USB 260 silicon diodes needs to be connected in series to achieve above 5.5kV voltage rating, only five pieces of 1.2kV SiC Schottky diodes GB01SLT12-21 are required for above 5.5kV voltage rating. The diode number can be reduced by 50% with 1.2kV SiC Schottky diodes. The compact size HV voltage multiplier boards can be realized with 1.2kV SiC Schottky diodes. The 1.2kV SiC Schottky diodes without reverse recovery will enable low power loss at high switching frequency and elevated temperature environment. Two pieces surface mounted of 3kV rating 1nF HV ceramic capacitors are connected in series to achieve above 5.5kV voltage rating. Both the surface mounted SiC Schottky diodes and surface mounted ceramic capacitors of the HV multiplier circuit are interconnected in printed circuit boards (PCB) to eliminate the additional insulated wire connection. The surface mounted SiC Schottky diodes and surface mounted ceramic capacitors will be placed in both top and bottom sides of PCB. The dimensions of the elementary HV multiplier circuit boards are 4.6cm (length) * 1.7cm (width) * 0.7cm (height). The HV multiplier circuit boards will be connected to the HV transformer secondary winding. The HV multiplier circuit boards and the HV transformer will be packaged in a HV plastic bobbin to achieve the HV insulation capability. The size of the HV rectifier boards for the 300kHz 8kW 110kV HV pulse converter prototype is five times smaller than 40kHz prototype. The multiplier capacitance for the 300kHz design is around 1/4 of 40kHz design. It will provide a faster HV pulse rise and decay times with lower HV tank capacitance.

Table A-3 provides the summary of the key parameters for a 40kHz and 300kHz 8kW 110kV HV pulse converter prototype.

Fig. A-11 shows a HV rectifier prototype photo for the 8kW 110kV HV pulse converter. The size of the 40kHz and 300kHz 8kW 110kV HV rectifier prototypes is given in Table A-3.

The 8kW power inverter and 110kV HV pulse converter prototypes are shown in Fig. A-12 and Fig. A-13 respectively. The dimensions of the HV pulse converter tank including the HV enclosure are 210mm*150mm*75mm. The total size of the HV pulse converter tank is 2.39L. The high frequency inverter size is around 1.90L, and the total size of the HV pulse converter including the power inverter and the HV tank is around 4.29L. The power density of the HV pulse converter is 1.86kW/L, which leads to a two times higher power density compared to the existing 40kHz design.

The key experimental waveforms of the 300kHz 8kW 110kV pulse converter are shown in Fig. A-14. All the SiC MOSFETs can achieve zero-voltage-switching due to the above-resonance operation. The measured total circuit efficiency from DC voltage input of the power inverter to the 110kV HV output is above 82%. The efficiency is over 10% higher than the legacy 40kHz HV pulse converter.

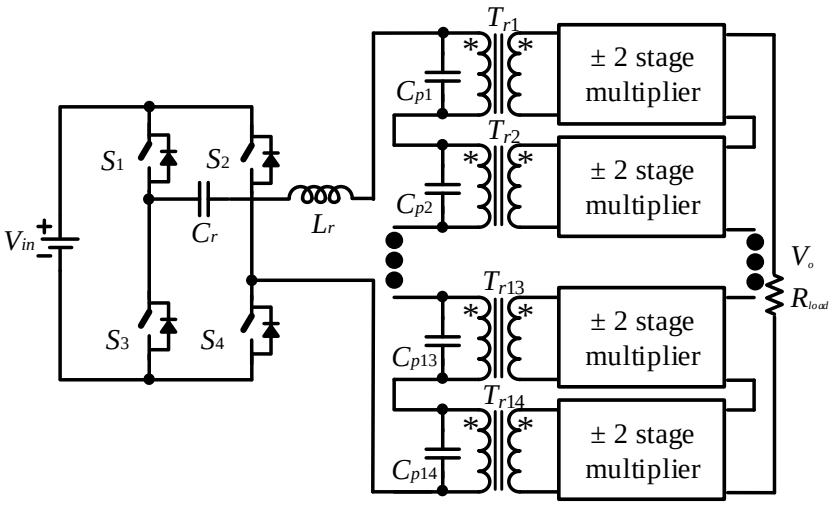



Fig. A-9 Circuit diagram for the 300kHz frequency 8kW 110kV HV pulse converter prototype

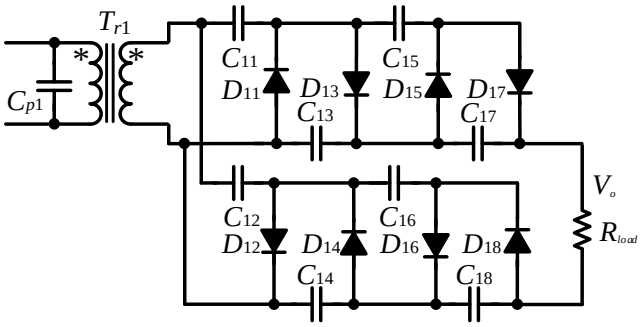
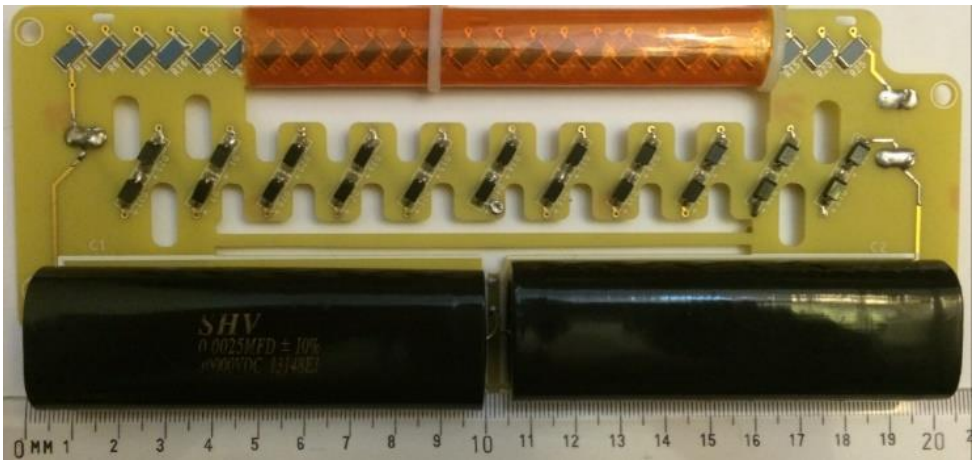



Fig. A-10 Circuit diagram of the elementary power building block with dual polarity positive and negative two stage half wave Cockcroft-Walton voltage multipliers

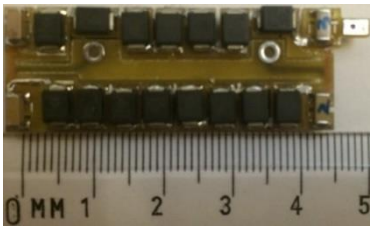
Table A-3 key parameters for the 40kHz and 300kHz 8kW 110kV HV pulse converter prototypes

| Key parameters | 40kHz frequency porotype | 300kHz frequency prototype |
|---|---|---|
| Input voltage | 600VDC | 600VDC |
| Output voltage | 110kVDC | 110kVDC |
| Output power | 8kW | 8kW |
| Architecture | Single inverter+single HV transformer(1P2S) + voltage doubler | Single inverter+12 HV transformer(1P1S) + 12 voltage multiplier (2 stage) |
| HV transformer turns ratio | 10:1000:1000<br>Lp=26.76uH, Lp(lk)=0.87uH, | 3:72<br>Lp=22.89uH, Lp(lk)=0.55uH |

| | | |
|---|---|---|
| | Ls1=329.12mH, Ls2=329.20Mh<br>Cp=176nF | Ls=13.36mH<br>Cp=1.7nF |
| HV multiplier | Capacitor: 2.5nF/30kV, cylinder<br>Diode: SP5L,5kV, SMA, 11 series | Capacitor: 1nF/3kV, 1825 MLCC package, 2 in series<br>Diode: GB01SLT12,1.2kV, SMB, 7 series |




(a) Half of voltage doubler circuit board(40kHz)




(b) Elementary two stage multiplier boards (300kHz)

Fig. A-11 HV rectifier prototype photo for the 8kW 110kV HV pulse converter prototype

Table A-4 size of the 40kHz and 300kHz 8kW 120kV HV rectifier prototypes

| | 40kHz frequency HV voltage doubler prototype | 300kHz frequency HV voltage multiplier prototype |
|---|---|---|
| Size for HV rectifier power building block | 21cm*8.5cm*2.5cm for half of doublers | 4.6cm*1.7cm*0.7cm for single polarity multiplier |
| Volume for total HV rectifier | 0.89L | 0.16L |

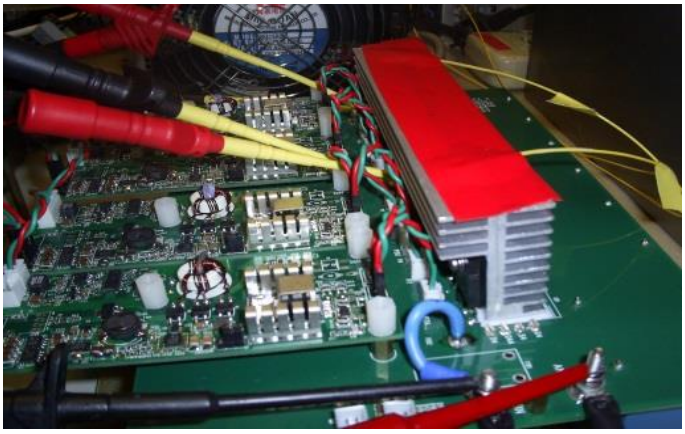


Fig. A-12 The photo of the 8kW SiC MOSFET inverter prototype

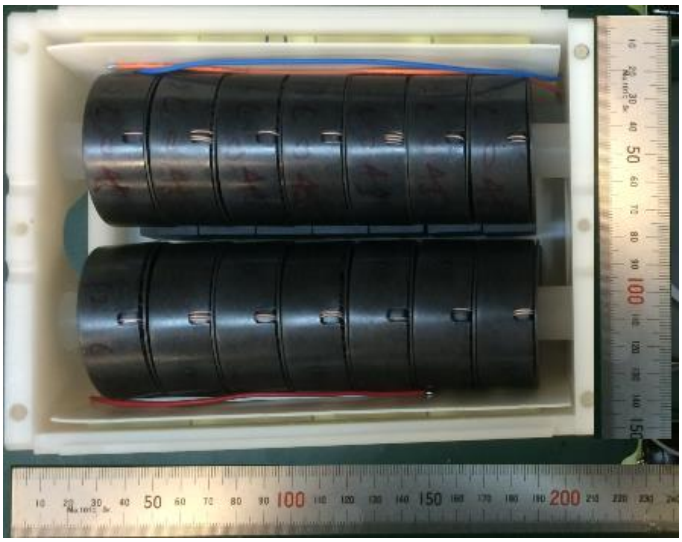


Fig. A-13 The photo of the 8kW 110kV HV tank prototype

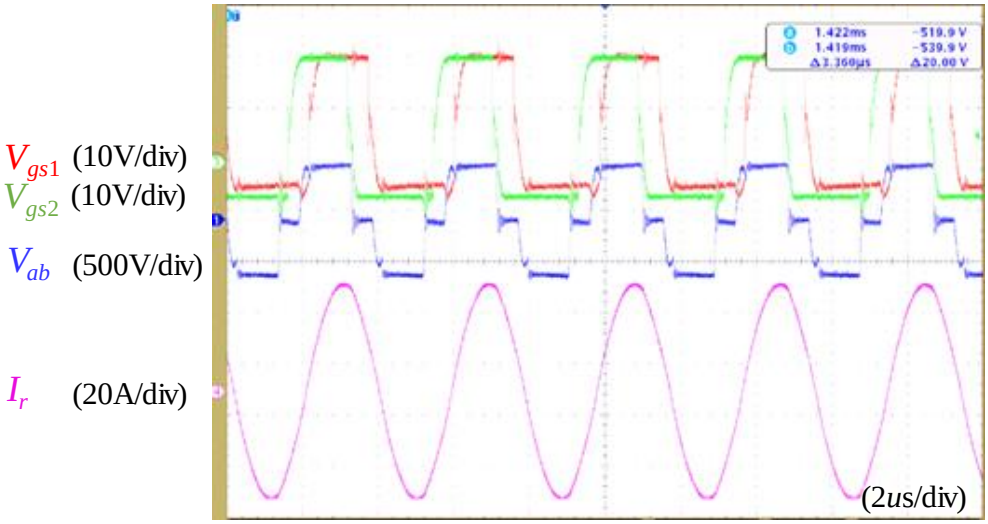



Fig. A-14 Key experimental waveforms of the 300kHz 8kW 110kV HV pulse converter

# Summary

Continuing research is needed to improve the performance of HV pulse converters to meet the system requirements such as high power density, high efficiency, low insulation stress, modularity and scalability, high quality pulse for steady and dynamic state.

This thesis explores a modular HV pulse converter technology with short rise and decay times. A systematic approach is derived to classify the HV architectures. The optimal architecture has been identified and recommendations for architecture selections are provided. The effect of modularization and increasing switching frequency for the HV transformer are addressed. The key influence factors for HV pulse rise and decay times are studied. A method is proposed to mitigate the diode reverse recovery effect for the multi-stage voltage multiplier. A generic equivalent steady-state circuit model and comprehensive design methodology are developed to simplify the analysis and design of the series parallel(LCC) resonant based modular HV pulse converters.

**HV pulse converter architectures classifications and evaluations**

A systematic methodology to derive and classify HV architectures based on a modularization level of power building blocks of the HV pulse converter is developed to summarize existing architectures and explore new possible architectures. Furthermore, all architectures are evaluated to identify the optimal architecture and provide an architecture selection guideline at different output voltages and power output ratings according to system performance requirements. The modular HV tank architecture with multiple transformers and multiple rectifiers configurations outperform other architectures for the best HV pulse converter performance on efficiency, power density, HV ripple, HV pulse rise and decay times, HV insulation and modularity.

T**he effect of the modularization and increasing switching frequency for modular HV transformers**

The modularization of the HV transformers provide advantages such as low insulation stress, low dielectric loss, distributed thermal stress and size reduction at high frequency without any sacrifice to the efficiency. It also provides the scalability to different HV pulse converter ratings and easy assembly and manufacturing. The equivalent circuit diagram of modular HV transformers is derived to better understand the characteristics of the modular architectures. High frequency achieves a size reduction of passive components in the HV tank. Low loss magnetic material, winding technology and insulation materials with a low dissipation factor need to be considered at the increasing frequency. The frequency to achieve the minimum power loss of the HV tank for different architectures will be different. The detailed HV AC and DC insulation stress analysis of the planar and wire-wound HV transformers for modular HV pulse converter architectures is addressed to provide an insulation design guideline. Finally, the electrical and insulation designs and prototype experimental results validate the analysis of the high frequency HV transformer for the modular architecture.

**Key influence factors for Cockcroft–Walton voltage multiplier circuit output HV pulse waveforms**

The key characteristics and influence factors of the rise and decay times of voltage multiplier based HV pulse converter circuits are analysed and experimentally verified. The HV pulse rise times will lengthen when a more stages voltage multiplier circuit is used. The voltage rating of the HV transformer and the stage number of the voltage multiplier need to be considered for the optimal circuit performance. Once the voltage multiplier stage number is determined, the switching frequency becomes the key most important influence factor for the HV pulse rise times. The HV pulse decay times are proportional to load resistance and multiplier capacitance. High switching frequency can effectively reduce the HV pulse rise and decay times. The multiplier diode reverse recovery problem is mainly caused by the diodes in the first stage voltage multiplier. The multiplier diode reverse recovery problem is the bottle neck of further increasing the circuit operation switching frequency to achieve high power density, good HV pulse quality. It is suggested that the most effective and economic solution to alleviate the diode reverse recovery problem is to employ diodes with good reverse recovery performance such as silicon carbide Schottky diodes in the first stage, only, of the voltage multiplier.

**Generic steady state circuit model and design methodology for modular HV pulse converter architectures**

A unified equivalent steady state circuit model is derived for various HV pulse converter architectures with different voltage multiplier topologies, stage number and polarities. These complicated HV structures can be broken down into the basic circuit structure. Then a generic equivalent circuit model is derived to simplify the converter analysis and design for the HV pulse converter. Based on the equivalent circuit model of the HV pulse converter, the power factor, voltage gain and component stresses are analysed and verified through circuit simulations. Furthermore, a general design method utilizing the conduction angle, power factor and quality factor of the LCC resonant tank, can achieve reduced low electrical stresses on the component, and a high efficiency. Finally, the experimental results of a HV pulse converter prototype based on the architecture with multiple transformers and voltage multipliers validate the equivalent steady state circuit model and the comprehensive design methodology.

# Samenvatting

Om de prestaties van HV-pulsomvomers te verbeteren en om aan de systeemvereisten te voldoen is voortdurend onderzoek nodig. Belangrijke vereisten zijn een hoge vermogensdichtheid, hoge efficiëntie, lage isolatiebelasting, goede modulariteit en schaalbaarheid, en een hoge puls kwaliteit in zowel statische als dynamische toestand.

In dit proefschrift wordt een modulaire HV-pulsomvormer technologie onderzocht met korte stijg- en daaltijden. Er is een systematische aanpak gebruikt om de HV-architecturen te classificeren. De optimale architectuur is geïdentificeerd en aanbevelingen voor de architectuurselecties zijn bepaald. Het effect van modularisatie en de toenemende schakelfrequentie op de HV-transformator worden benoemd. De belangrijkste factoren die HV stijg- en daaltijden beïnvloeden worden bestudeerd. Er wordt een methode voorgesteld om het reverse-recovery effect in de meertraps spanningsvermenigvuldiger te verminderen. Er is een generiek equivalent steady-state circuitmodel en uitgebreide ontwerpmethodiek ontwikkeld, om de analyse en het ontwerp te vereenvoudigen. Dit is gebaseerd op serie-parallelle (LCC) resonantie van de HV-pulsomvormer.

**HV-pulsomvormer architecturen, classificaties en evaluaties**

Om bestaande HV-architecturen samen te vatten en mogelijk nieuwe architecturen te onderzoeken, is een systematische methode afgeleid en geclassificeerd. Deze methode is gebaseerd op het modularisatieniveau van de bouwstenen van de HV-pulsomvormer. Bovendien worden alle architecturen geëvalueerd om de optimale architectuur te identificeren. Voor de systeemeisen verschaft dit tevens een richtlijn voor architectuurselectie bij verschillende uitgangspanningen en vermogens. De modulaire HV-tankarchitectuur met meerdere transformatoren en gelijkrichters presteren beter dan andere architecturen voor HV-pulsomvormers. De parameters gebruikt voor vergelijking zijn: efficiëntie, vermogensdichtheid, rimpelspanning, stijg- en daaltijden, isolatie en modulariteit.

**Het effect van modularisatie en toenemende schakelfrequentie op modulaire HV-transformatoren**

De modularisatie van HV-transformatoren biedt voordelen, zoals lage isolatiebelasting, lage diëlektrische verliezen, gedistribueerde thermische belasting en een volume afname bij hoge frequenties, en dit alles zonder rendementsafname. Het biedt ook schaalbaarheid bij verschillende HV-pulsomvomer vermogensreeksen en hierdoor wordt de montage en fabricage eenvoudiger. Om de eigenschappen van deze modulaire architecturen beter te begrijpen is het equivalente schema van modulaire HV-transformatoren afgeleid. Het gebruik van hogere frequenties reduceert de grootte van de passieve componenten in de HV-tank. Bij een

toenemende frequentie moet magnetisch materiaal met een laag verlies, moderne wikkeltechnologieën en isolatiematerialen met een lage dissipatiefactor, worden overwogen. De frequentie waarbij het minimale vermogensverlies in de HV-tank optreedt, zal voor verschillende architecturen verschillend zijn. De gedetailleerde HV AC en DC isolatie stress analyse, van platte en draadgewonden HV-transformatoren voor modulaire HV- pulsconverter architecturen, is gebuikt om een ontwerprichtlijn voor de isolatie te geven. Tenslotte valideren, het elektrische ontwerp, het isolatie ontwerp, het prototype en de experimentele resultaten, de analyse van de modulaire hoogfrequente HV-transformator architectuur.

**De belangrijkste factoren die een Cockcroft-Walton spanningsvermenigvuldiger beïnvloeden**

De belangrijkste kenmerken en factoren, die de stijg- en daaltijden van een spanningsvermenigvuldiger gebaseerd op een HV-pulsomvormer circuit beïnvloeden, worden geanalyseerd en experimenteel geverifieerd. De HV-puls stijgtijden worden groter naar mate een spanningsvermenigvuldiger van meer trappen wordt voorzien. De maximale spanning van de HV-transformator en het aantal trappen van de spanningsvermenigvuldiger moeten in overweging worden genomen om tot een optimale schakeling te komen. Zodra het aantal trappen van de spanningsvermenigvuldiger is bepaald, wordt de schakelfrequentie de belangrijkste factor voor de stijgtijden van de HV-puls. De daaltijden van de HV-puls zijn evenredig met de belastingsweerstand en capaciteit van de spanningsvermenigvuldiger. Een hoge schakelfrequentie kan de stijg- en daaltijden van de HV-puls reduceren. In een spanningsvermenigvuldiger is diode reverse-recovery voornamelijk een probleem in de eerste trap. Reverse-recovery is het knelpunt voor het verhogen van de schakelfrequentie, waarmee een hoge vermogensdichtheid en een goede HV-puls kwaliteit kan worden bereikt. De meest effectieve en economische oplossing om het reverse recovery probleem te verlichten, is om alleen in de eerste trap van de spanningsvermenigvuldiger gebruik te maken van diodes met goede reverse-recovery eigenschappen. Siliciumcarbide Schottky diodes kunnen hier uitkomst brengen.

**Generiek steady-state circuitmodel en ontwerp methodologie voor modulaire HV-pulsconverter architecturen.**

Voor verschillende HV-pulsconverter architecturen met verschillende vermenigvuldiger typologieën, aantal trappen en polariteiten, is een uniform equivalent steady-state circuitmodel is afgeleid. Deze ingewikkelde HV-structuren kunnen worden vereenvoudigd tot een basis circuit. Vervolgens is een generiek equivalent circuitmodel afgeleid om de omzettingsanalyse en het ontwerp voor de HV-pulsomvormer te vereenvoudigen. Op basis van simulaties met het equivalente circuitmodel van de HV-pulsomvormer worden de power factor, spanningsversterking en componentbelasting geanalyseerd en geverifieerd. Bovendien kan een algemene ontwerpmethode die de geleidingshoek, de power factor en kwaliteitsfactor van de LCC resonantietank gebruikt, leiden tot lagere elektrische belasting van componenten en een

hogere efficiëntie. Tenslotte is het equivalente steady-state circuitmodel en de uitgebreide ontwerpmethodiek, gevalideerd met experimentele resultaten van een prototype van de HV-pulsomvormer. Dit was op basis van een architectuur met meerdere transformatoren en spanningsvermenigvuldigers.

# List of Publications

## A. IEEE Journal papers

1. **S. Mao**, C. Li, W. Li, J. Popovic, J. Ferreira, "Unified Equivalent Steady-State Circuit Model and Comprehensive Design of the LCC Resonant Converter for HV Generation Architectures," IEEE Transaction on Power Electronics, Accepted, Early access.
2. **S. Mao**, J. Popovic, J. Ferreira, "Analysis of the Voltage Pulse Rise and Decay Times in a Half-Wave Series Cockcroft-Walton Voltage Multiplier based High Voltage Generator," IEEE Transaction on Power Electronics, Submitted, Under review.
3. **S. Mao**, J. Popovic, J. Ferreira, "Diode Steady State and Reverse Recovery Analysis of Half-Wave Series Cockcroft-Walton Voltage Multiplier," IEEE Transaction on Power Electronics, Submitted, Under review.
4. **S. Mao**, J. Popovic, J. Ferreira, "Analysis of Transformer Modularization for High Frequency Isolated HV Generator," IEEE Transaction on Power Electronics, Submitted, Under review.
5. **S. Mao**, J. Popovic, J. Ferreira, "A 300kHz 4kW 140kVDC Output Voltage Power Supply with Modular Architecture and Planar PCB Transformer," IEEE Transaction on Power Electronics, Submitted, Under review.
6. **S. Mao**, C. Li, W. Li, J. Popovic, J. Ferreira, "Classification and Comparative Evaluation of High Frequency High Voltage Generator Architectures," IEEE Transaction on Power Electronics, Submitted, Under review.
7. **S. Mao**, C. Li, W. Li, J. Popovic, J. Ferreira, "Coreless Transformer based High Voltage Generator for Intense Magnetic Field Applications," IEEE Transaction on Power Electronics, Submitted, Under review.
8. **S. Mao**, Y. Chen, C. Li, W. Li, J. Popovic, J. Ferreira, "An Output-Voltage-Automatic-Balancing Multi-transformer LCC Resonant Converter with the Coupled Inductor for High Voltage Generator Applications," IEEE Transaction on Power Electronics, Submitted, Under review.
9. **S. Mao**, J. Popovic, J. Ferreira, "High Frequency Isolated High Voltage Generators: An Overview," IEEE Transaction on Power Electronics, Submitted, Under review.
10. **S. Mao**, J. Popovic, J. Ferreira, "Planar PCB Transformers for High Frequency High Voltage Generator Applications: Advantages and Challenges" IEEE Transaction on Power Electronics, Submitted, Under review.
11. **S. Mao**, J. Popovic, J. Ferreira, "A Modular High Frequency High Voltage Generator with Silicon Carbide Power Semiconductor Devices," IEEE Transaction on Power Electronics, to be submitted, Manuscript in preparation.
12. **S. Mao**, Y. Chen, C. Li, W. Li, J. Popovic, J. Ferreira, "Analysis of the Output Voltage Imbalance Alleviation for Different HV Generator Configularations with Modular HV Transformers," IEEE Transaction on Power Electronics, to be submitted, Manuscript in preparation.

## B. IEEE Conference Papers

13. **S. Mao**, C. Li, W. Li, J. Popovic, J. Ferreira, "Equivalent Circuit model for High Voltage Power Generation Architectures," IEEE Energy Conversion Congress and Exposition (ECCE) conference, 2017, pp.3098-3102.
14. **S. Mao**, C. Li, W. Li, J. Popovic, J. Ferreira, "Comparative Analysis and Evaluation of High Voltage Power Generation Architectures," IEEE Energy Conversion Congress and Exposition (ECCE) conference, 2017, pp.4753-4760.
15. **S. Mao**, C. Li, W. Li, J. Popovic, J. Ferreira, "Review of High Frequency High Voltage Generation Architecture," IEEE Energy Conversion Congress and Exposition (ECCE)-Asia conference, 2017, pp.2260-2266.
16. **S. Mao**, T. Song, C. Li, W. Li, J. Popovic, J. Ferreira, "Power Packaging Design Considerations for High Frequency High Voltage Generator," IEEE Energy Conversion Congress and Exposition (ECCE)-Asia conference, 2017, pp.2267-2272.
17. **S. Mao**, P. Zhang, C. Li, J. Popovic, J. Ferreira, "Diode Reverse Recovery Analysis of Cockcroft-Walton Voltage Multiplier for High Voltage Generation," IEEE Energy Conversion Congress and Exposition (ECCE)-Asia conference, 2017, pp.1765-1770.
18. **S. Mao**, C. Li, T. Song, J. Popovic, J. Ferreira, "High Frequency High Voltage Generation with Air-core Transformer," IEEE International Workshop on Integrated Power Packaging (IWIPP) 2017, pp.1-5.
19. **S. Mao**, T. Wu, X. Lu, J. Popovic, J. Ferreira, "High Frequency High Voltage Power Conversion with Silicon Carbide Power Semiconductor Devices," IEEE Electronics System-Integration Technology Conferences (ESTC), 2016, pp.1-5.
20. **S. Mao**, T. Wu, X. Lu, J. Popovic, J. Ferreira, "Three-phase Active Front-end Rectifier Efficiency Improvement with Silicon Carbide Power Semiconductor Devices," IEEE Energy Conversion Congress and Exposition (ECCE) conference, 2016, pp.1-8.
21. **S. Mao**, R. Ramabhadran, J. Popovic, J. Ferreira, "Analysis, Design and Implementation of CLL Resonant DC-DC Converter for Wide Output Power Range Application," IEEE Energy Conversion Congress and Exposition (ECCE)-Asia conference, 2016, pp.2193-2197.
22. **S. Mao**, J. Popovic, J. Ferreira, "Planar Transformer for High Frequency High Voltage Generation Applications," IEEE Energy Conversion Congress and Exposition (ECCE)-Asia conference, 2016, pp.1660-1663.
23. **S. Mao**, J. Popovic, J. Ferreira, "Investigations of High Frequency High Voltage Planar Transformer for High Voltage Generator Applications," IEEE International Conference on Integrated Power Electronics Systems (CIPS), 2016, pp.1-6.
24. **S. Mao**, R. Ramabhadran, J. Popovic, J. Ferreira, "Investigation of CCM Boost PFC Converter Efficiency Improvement with 600V Wide Band-gap Power Semiconductor Devices," IEEE Energy Conversion Congress and Exposition (ECCE) Conference, 2015, pp.388-395.
25. **S. Mao**, J. Popovic, R. Ramabhadran, J. Ferreira, "Comparative Study of Half-Bridge LCC and LLC Resonant DC-DC Converters with Ultra-Wide Output Power Range Applications," IEEE Conference on Power Electronics and Applications (EPE-ECCE Europe) Conference, 2015, pp.1-10.

26. **S. Mao**, J. Popovic, J. Ferreira, "High Voltage Pulse Speed Study for High Voltage DC-DC Power Supply Based on Voltage Multipliers," IEEE Conference on Power Electronics and Applications (EPE-ECCE Europe) Conference, 2015, pp.1-9.
27. **S. Mao,** J. Popovic, J. Ferreira, "Efficiency impacts of 1.2kV Silicon Carbide MOSFETs for isolated two stage AC-DC power conversion," 2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Submitted, Under review.
28. **S. Mao**, J. Popovic, J. Ferreira, "300W 175$^{o}$C Half Bridge Power Building Block with SiC MOSFETs for Harsh Environment Applications," 2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia) Submitted, Under review.
29. **S. Mao**, J. Popovic, J. Ferreira, "Switching Characterization and Low Inter-winding Capacitance Gate Driver Power Supply Design of SiC MOSFET for the 300kHz 10kW Inverter," 2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Submitted, Under review.

**C. IEEE ECCE Conference Tutorial Proposal**

30. **S. Mao**, J. Ferreira, "Analysis, Design and Implementation of High Frequency High Voltage Power Supply," Tutorial Proposal for ECCE 2018 conference in Portland, Oregon, USA, tutorial proposal in preparation, to be submitted.

# Curriculum Vitae

Saijun Mao was born in Changzhou, China, in 1980. He received the BSc and MSc degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2003 and 2006, respectively.

Since December 2014, he joined the Electrical Power Processing group in the department of Electrical Sustainable Energy at the Delft University of Technology, Delft, the Netherlands, to pursue the Ph.D. degree supported by GE Global Research Center, Shanghai, China.

From 2006 to 2017, he was a senior engineer and project leader with the GE Global Research Center, Shanghai, China.

His research interests include high power density, high efficiency, and high frequency power conversion systems, especially high voltage generator systems, wide-bandgap power semiconductor devices based power conversion systems, as well as power conversion and packaging for harsh environment such downhole and subsea power systems applications.