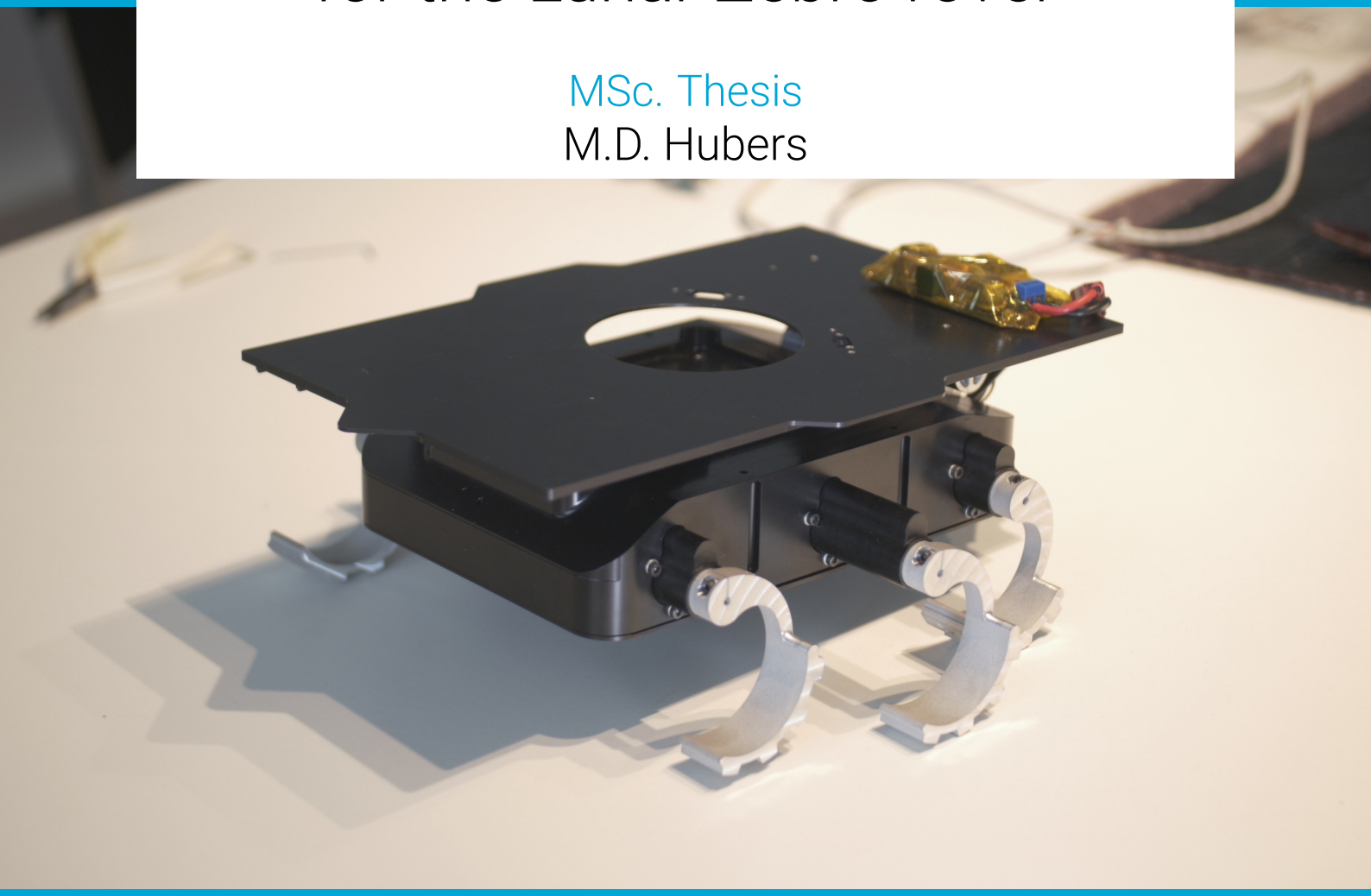
Design and Implementation of the Power Electronic System for the Lunar Zebro rover

MSc. Thesis

M.D. Hubers



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Design and Implementation of the Power Electronic System for the Lunar Zebro Rover

MSc. Thesis

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Abstract

The small and lightweight Lunar Zebro rover must survive in the harsh lunar environment for several Earth days following its moon landing. The mission of the rover is to map the radiation environment on the moon. The success of the entire mission depends on the Power Electronic System (PES), which supplies power to all subsystems and charges the batteries using solar panels. The current PES of the Lunar Zebro rover does not comply with all mission-specific requirements and does not perform satisfactorily when integrated into the rover. Therefore, the need for a reliable PES that conforms to all requirements arises for the Lunar Zebro rover.

In this research, the design and implementation of an efficient, compact, and redundant PES for the Lunar Zebro rover is developed. First, the optimal Direct Current (DC) bus is designed to obtain a system with the highest efficiency. This is done by modelling the efficiency of the DC/DC converters for different bus voltages and estimating the overall losses in these converters during the deployment of the rover. Moreover, the effect of the bus voltage on the size of the passive components is investigated, and the bus voltage resulting in the most compact system is obtained. It is found that a 12 V bus results in the most efficient and compact system. No additional converter is required that regulates the 12 V output, and the inductance required for each converter is decreased compared to higher bus voltages.

Besides the DC bus design, redundancy methods are compared to obtain the best tradeoff between redundancy and footprint added. The two-phase interleaved converter was found to have only an 8.59% increase in footprint compared to single-phase converters, while failure in a switch, diode, input capacitor, and output capacitor are accounted for in each converter.

Finally, the mode of operation that results in the highest efficiency is obtained by designing each converter and modelling the corresponding losses for Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) operation. For both the single-phase and two-phase interleaved converters hold that operating in CCM results in a significant increase in efficiency compared to DCM operation. Moreover, the PES utilising two-phase interleaved converters is more efficient during rover operation than the single-phase counterpart. However, charging is less efficient than for the single-phase counterpart. Simulink and LTspice simulations have been carried out to verify the operation of each converter. Finally, experiments on a functional prototype are carried out to provide experimental validation of the design.

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Martijn Hubers

Delft, the Netherlands

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List of Abbreviations

ADC Analog-to-Digital Converter

BCM Boundary Conduction Mode

BJT Bipolar Junction Transistor

BMS Battery Management System

CCM Continuous Conduction Mode

COTS Commercial Off-The-Shelf

DC Direct Current

DCM Discontinuous Conduction Mode

DD Displacement Damage

E-HEMT Enhancement mode High Electron Mobility Transistor

EM Electromagnetic

EMI Electromagnetic Interference

ESR Equivalent Series Resistance

PES Power Electronic System

FET Field Effect Transistor

GaN Gallium Nitride

GCR Galactic Cosmic Radiation

IC Integrated Circuit

IGBT Insulated Gate Bipolar Transistor

LDO Low-Dropout Regulator

LET Linear Energy Transfer

LSB Least Significant Bit

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

MPP Maximum Power Point

MPPT Maximum Power Point Tracking

MRC Multi Resonant Converter

NMOS N-channel Metal-Oxide-Semiconductor

PCB Printed Circuit Board

PEC Power Electronic Component

PI Proportional Integral

PMOS P-channel Metal-Oxide-Semiconductor

PV Photovoltaic

PWM Pulse Width Modulation

RMS Root Mean Square

RPC Resonant Power Converter

RTC Resonant Transition Converter

SEB Single Event Burnout

SEDR Single Event Dielectric Rupture

SEE Single Event Effect

SEFI Single Event Functional Interrupt

SEGR Single Event Gate Rupture

SEL Single Event Latchup

SELC Single Event Leakage Current

SET Single Event Transient

SEU Single Event Upset

SOA Safe Operating Area

Si Silicon

SiC Silicon Carbide

SiO_2 Silicon Dioxide

TID Total Ionising Dose

QRC Quasi Resonant Converter

ZCS Zero Current Switching

ZVS Zero Voltage Switching

Chapter 1

Introduction

Interest in exploration of the moon has regained interest lately [1]. The Artemis program of NASA has as its goal to send humans to the moon yearly to establish sustainable moon bases and surface capabilities [2]. Similarly, SpaceX is also planning to land humans on the moon with Starship [3]. The radiation-rich environment on the moon poses serious health risks for astronauts [4]. Locations with the least amount of radiation will be most suitable for establishing moon bases. To find these locations, a map of the radiation environment on the moon is required. This is the goal of the Lunar Zebro project, which will ultimately send a swarm of small, lightweight rovers to map the radiation environment on the moon [5].

The Lunar Zebro project is a project of the University of Technology Delft. It is the world's smallest and lightest rover, built by students from the TU Delft. The first rover will be sent to the moon's South pole and has several goals for its mission. First, it will image the ground around the moon lander to study the effects of traditional landing methods on the lunar surface. Second, it will demonstrate its unique locomotion system consisting of 6 C-shaped legs, as well as its autonomous navigation system. In addition, it will carry out radiation measurements with the in-house developed radiation measurement payload. Finally, it should cover as much ground as possible during one day on the moon, which is equal to 14 days on Earth, before going into hibernation during the night. If it ever wakes up again, it will send a beacon to Earth.

Besides its technical goals, the overall goal of the project is to provide education on lunar missions to students. Therefore, most of the systems inside the rover are in-house developed by students. Currently, the Power Electronic System (PES) of the rover is a Commercial Off-The-Shelf (COTS) product. Integration in the rover is challenging since it does not comply with all mission-specific requirements, for example shutting down parts of the power supply during the flight to the moon. Moreover, the PES does not perform satisfactorily when integrated into the rover and unexpected behaviour occurs. Finally, no modifications can be made since it is the intellectual property of the manufacturer. Therefore, the need arises for an in-house developed PES that is specifically designed for the mission. Besides the educational purposes, an in-house developed system has several advantages. The PES can be optimised in size and weight for mission-specific requirements. Furthermore, the PES can be made modular so future missions can easily integrate new functionalities or adapt current modules.

The PES is one of the most critical systems of the Lunar Zebro rover. If the PES fails, the rover loses all functionalities. The PES must be able to store energy using batteries and is responsible for distributing power to all subsystems inside the rover at voltages of 12 V, 5 V, and 3.3 V. Moreover, it should charge the batteries from the solar panels mounted on top of the rover. Finally, it must operate in the harsh conditions of the moon. The radiation environment on the moon can cause early failure in Power Electronic Components (PECs) [6]. Furthermore, it must be able to withstand the extreme temperatures on the South pole of the moon, ranging from -203°C in some craters to 54°C at sunlit surfaces during the day [7]. By including redundancy the reliability of the PES is increased [8]. Contradictory, the PES should be made small and lightweight to reduce the cost of sending it to the moon.

In a battery-powered system where multiple sources and loads are interconnected, it is common practice to have a central DC bus [9, 10]. This has several advantages. First of all, the power flowing into and out of the batteries is controlled using a single DC/DC converter. Second, the system is made modular as additional systems can be connected to the DC bus. Finally, the input voltages of the DC/DC converters for the 12 V, 5 V, and 3.3 V outputs are regulated instead of the fluctuating battery voltage. This simplifies the design of these converters. The value of the DC bus voltage will influence the design and efficiency of the PES. The efficiency is a key parameter, as a higher efficiency results in longer operation of the rover. Furthermore, the temperature increase in the components is reduced, increasing their reliability and reducing the size of the radiators [11].

The DC/DC converters are operated in Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). In CCM, the current ripple in the inductor is smaller, reducing the core losses, and reducing the conduction losses in the switch, diode, and output capacitor. However, the inductor required is larger, increasing the winding resistance thus the conduction losses [11, 12]. In DCM, the switch turns on at zero current and without diode reverse recovery current, which reduces the switching losses [13]. However, the inductor current ripple is increased, increasing the conduction losses in the switch, diode, and output capacitor, as well as the core losses in the inductor [14, 15]. Thus, it is non-trivial which mode of operation results in the most efficient PES.

In this thesis, the design of the PES is developed with the primary objectives of achieving a high level of efficiency, and the integration of redundancy measures to address the challenging environmental conditions present on the lunar surface, while keeping the size of the system small. The research delves into the impact of the bus voltage on system size and efficiency, as well as the impact of the operational modes of the DC/DC converters on system efficiency, with the overall goal of optimizing efficiency levels. Furthermore, the design is verified using simulations in Matlab Simulink and LTspice.

1.1 Research Objectives

The focus of this thesis is to design the PES of the Lunar Zebro rover and verify the design with a prototype. Because this thesis is design-oriented, three research questions are composed which together result in a system that is compact, efficient, and includes redundancy. The first step of the design is determining the topology of the PES. The DC bus voltage determines the topology and DC/DC converters required, which in turn affects the size, weight, and efficiency of the system. This gives rise to the first research question:

1. How can the DC bus voltage be selected such that it results in the most efficient and compact system?

Two bus voltages are compared. The efficiency of each DC/DC converter is modelled, as well as the system efficiency during deployment of the rover. In this way, the DC bus that results in the highest efficiency is obtained. The mode of operation of the DC/DC converters also influences the design and efficiency of the converters. This results in the second research question:

2. What mode of operation (CCM or DCM) should the DC/DC converters be operated in to obtain the highest efficiency?

By modelling the efficiency in CCM and DCM the mode of operation resulting in the most efficient system is determined. The PES is the most critical system of the rover. Therefore, redundancy should be included in the design. However, redundancy increases the size of the system. The size of the system should be as small as possible for two reasons. Firstly, size constraints inside the rover limit the PCB size. Secondly, sending 1 gram to space costs approximately €1000. Thus, sending more and larger, heavier components to space increases the cost significantly. The final research question is therefore:

3. How can the system be made redundant while minimising the additional footprint required?

1.2 Thesis Outline

The thesis is structured as follows. First, in Chapter 2 background information is provided, giving an overview of the effects of radiation on PECs, together with DC/DC converter topologies considered for the PES. Next, Chapter 3 compares the efficiency of two bus voltages based on the design of single-phase DC/DC converters to obtain the bus voltage that results in the most efficient system. Then, different redundancy methods and their corresponding increase in size and component count are compared in Chapter 4. This is followed by the design of the PES using interleaved converters in Chapter 5, together with solutions to technical challenges that come to play for realising a functional prototype. In Chapter 6 the controllers of the DC/DC converters and their implementation on the microcontroller are developed. These controllers are required for stabilising the output voltages under fluctuating loads and for Maximum Power Point Tracking (MPPT) of the solar panel. Next, in Chapter 7, a simulation model of the complete PES is created to verify the operation and analyze the performance of each converter when operated simultaneously. Chapter 8 provides the experimental results on the developed prototype, verifying both steady-state operation and dynamic operation of the PES. Finally, Chapter 9 gives the conclusions and recommendations for future work.

Chapter 2

Literature Review

2.1 Cosmic Radiation and Power Electronic Components

It is generally known that cosmic radiation can be responsible for early failure in PECs [6]. Depending on the radiation profile the rover encounters, measures must be taken in the design of the PES to maintain full functionality during the mission. The three types of radiation damage are Total Ionising Dose (TID), Displacement Damage (DD), and Single Event Effects (SEEs) [16]. TID and SEEs are caused by ionising radiation, while DD is caused by non-ionising radiation [17]. The susceptibility to radiation depends on the type of device, (e.g. Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) or Insulated Gate Bipolar Transistor (IGBT)), the technology used (e.g. Silicon (Si) or Silicon Carbide (SiC)), and the structure of the device (e.g. planar vertical MOSFET or lateral MOSFET) [18–21].

Both during spaceflight and on the moon high amounts of radiation are encountered. This significantly increases the probability of early failure of PECs if no countermeasures are taken. It must therefore be known what the effects of radiation on PECs are and which devices are most radiation proof. In this chapter, the susceptibility of each PEC to radiation damage and the corresponding effects are compared. This is done for Bipolar Junction Transistors (BJTs), Si IGBTs, Si and SiC MOSFETs, Gallium Nitride (GaN) Field Effect Transistors (FETs), and finally Si and SiC power diodes. First, some basic terminology about radiation is explained.

2.1.1 Quantifying Radiation and Radiation Encountered on the Moon

Radiation is usually expressed in rads or Gray (Gy), where 1 Gy = 100 rads. The amount of radiation that passes a surface for a standard unit of time is called flux. Finally, fluence is the amount of radiant-energy particles incident on a surface in a given time, divided by the surface. Linear Energy Transfer (LET) is an indicator of the effects of radiation on matter. It is defined as the rate of energy deposited to a material by ionisation due to a particle that travels through this material [22]. The LET of the material determines the amount of electron-hole pairs created inside the material [23]. Higher energy ions will penetrate deeper into the material for a given LET, resulting in more generation of electron-hole pairs [24].

Radiation can consist of Electromagnetic (EM) or particle radiation, and can either be ionising or non-ionising. Ionising radiation contains enough energy to remove an electron from a molecule [4]. Particle radiation consists of protons, neutrons, beta particles (electrons), alpha particles, and heavy ions [4, 25]. Only ultraviolet, gamma and X-rays are ionising of the EM radiation, while all particle radiation is ionising. The origin of the radiation is both from the sun and from Galactic Cosmic Radiations (GCRs). The moon has no magnetosphere to deflect or trap charged particles. Additionally, it has no atmosphere to create secondary radiation and to provide attenuation of the incident radiation [22]. Therefore, the radiation encountered origins from the sun and GCRs. However, compared to free space, the moon blocks almost half of the GCRs when on the surface [22].

2.1.2 Total Ionising Dose

TID is defined as the energy absorbed in a material with a unit mass that originates from the energy deposited by ionising radiation [26]. Charges are trapped into the dielectric of a device and electron traps are created [27]. This alters the threshold voltage and increases the drain-source and gate leakage currents I_{DS} and I_{G}, and can eventually lead to failure [16, 28]. MOSFETs and IGBTs with a dielectric consisting of Silicon Dioxide (SiO_2) have the same mechanism for TID, which is explained in more detail in Appendix A.1.

BJTs

BJTs are sensitive to TID [17]. The base leakage current increases significantly, the collector leakage current increases slightly, and the gain decrease significantly when exposed to doses of 20 krad [29]. Oxide trap charges at the oxide layers near the base-emitter junctions and interface traps at the Si-SiO_2 interface result in an increased recombination rate, hence an increase of the base leakage current [30]. The decreased gain is a result of the increased base leakage current [30, 31].

MOSFETs

Despite the fact Si and SiC MOSFETs have the same gate insulator (SiO_2), SiC devices have a higher TID tolerance than Si devices [32]. This is because SiC has higher ionisation energy than Si, meaning that fewer electron-hole pairs are generated for an incident particle with the same energy. Thus, SiC has fewer TID effects [32]. It is shown that SiC MOSFETs show no degradation of the threshold voltage for doses up to several hundred krad [33, 34]. On the other hand, Si devices show degradation of the threshold voltage at doses larger than 10 krad [35]. Further, the drain-source leakage current of Si devices is increased by 2 orders of magnitude after exposure to 20 krad. This is because the threshold voltage is significantly reduced due to the positive trapped charge in the channel, therefore the channel is partially turned on [36].

IGBTs

Similar to Si MOSFETs, Si IGBTs are susceptible to a shift in the threshold voltage, as well as an increase of the leakage currents after several tens of krad [37]. When the gate is biased, the gate leakage current increases slightly, while the collector current increases rapidly for this dose. When the gate is unbiased, however, the leakage currents are barely affected [38]. The reverse blocking leakage current is more radiation resistant and is only affected after several hundreds of krad [38, 39].

GaN FETs

GaN Enhancement mode High Electron Mobility Transistors (E-HEMTs) are not susceptible to TID [40]. This can be accounted for by the fact that they do not have an SiO_2 gate insulator [41]. Nonetheless, a positive shift in the threshold voltage is observed after heavy irradiation. Also, a permanent increase of the leakage current occurs which can destroy the device. However, this is due to SEEs and not due to TID [41]. The increase in threshold voltage is due to trapping of charges in the GaN buffer region and at the Al-GaN surface. These effects start to occur after doses larger than 100 krad [28].

Diodes

Diodes do not have a gate oxide, and therefore diodes do not suffer from the aforementioned mechanism. The damage done due to radiation is classified into DD.

2.1.3 Displacement Damage

DD creates defects in the semiconductor lattice due to collisions with energetic electrons, protons, neutrons, or heavy ions [28]. These collisions knock out atoms in the semiconductor lattice and create defects. These defects alter the carrier mobility and create carrier traps, which degrade the electrical properties of the semiconductor until the point it results in failure [16, 17, 42]. The displacement energy threshold of the device determines the susceptibility to this damage [43]. SiC has a larger displacement energy threshold around 25 eV [44]. Si has a displacement energy threshold around 14 eV [45, 46]. Thus, SiC is more robust to DD than Si in general [47].

BJTs

BJTs are sensitive to DD. Due to the defects created, changes in the free carrier properties are produced. Because the BJT is a minority carrier device, DD quickly results in altering of the electrical properties [17]. The primary action of the BJT is due to the concentration of minority carriers in the base and emitter-base depletion region. Defects increase the base current required for a given collector current causing gain

degradation. PNP devices are more sensitive to DD than NPN devices, as the doping in the base is much lower for PNP devices [17].

MOSFETs

Compared to BJTs. MOSFETs are relatively robust to DD. This is because they are majority carrier devices, thus more defects are required before altering the device properties. Additionally, because the channel is the active region and is thin, it requires a lot of radiation before this region has enough defects to alter its properties [17]. SiC has higher energy required for ionisation and defects, thus is more suitable than Si regarding DD [47].

IGBTs

Since IGBTs are made from Si, they are more susceptible to DD than SiC MOSFETs. Additionally, they are majority carrier devices, thus are more robust to DD than BJTs.

GaN FETs

GaN has a displacement energy around 19 eV [46]. Therefore, they more radiation hardened than Si MOSFETs and IGBTs, but less radiation hardened than SiC MOSFETs [28]. Furthermore, because they are majority carrier devices, they are not susceptible to DD [41].

Diodes

The threshold voltage of Si and SiC PiN and Schottky diodes is barely affected by radiation exposure [48]. However, the on-state voltage drops increases. The increase of voltage drop is caused by the decrease of electron and hole concentration, which increases the drift region resistivity [48, 49]. Schottky diodes are majority carrier devices, while PiN diodes are minority carrier devices. Hence, Schottky diodes are more robust than PiN diodes to DD. It is shown that Si devices are more robust to the increase of forward voltage drop than SiC, devices because the forward voltage drop start increasing for larger fluences [48]. On the other hand, SiC devices show an increase in breakdown voltage, while Si devices show a decrease in breakdown voltage [50]. Thus, SiC Schottky diodes are more robust against degradation until failure but become less efficient while conducting compared to Si Schottky diodes.

2.1.4 Single Event Effects: Single Event Gate Rupture and Dielectric Rupture

Single Event Effects (SEEs) can be destructive or non-destructive. Non-destructive SEEs are called Single Event Transients (SETs), which in turn consists of Single Event Upsets (SEUs), Single Event Latchups (SELs), and Single Event Functional Interrupts (SEFIs). These events are temporary and recovery is possible. SETs can result in a measurable current small enough not to damage the device, a bit flip, and data corruption [17]. The latter two can be circumvented by using error correction code.

Destructive SEEs include Single Event Burnout (SEB), Single Event Gate Rupture (SEGR), Single Event Dielectric Rupture (SEDR), and Single Event Leakage Current (SELC). Each can cause permanent damage or can destroy the component [16]. Each of these will be discussed in more detail, as the reliability of the PES depends mainly on destructive SEEs.

A SEGR can occur when a heavy ion hits the neck region of the device. The neck region is defined as the epitaxial area directly under the gate oxide between the p-body regions [18]. The electrons drift towards the drain, and holes accumulate at the Si/SiO_2 interface. These holes attract electrons at the gate, increasing the electric field in the gate oxide. If the sum of this induced electric field and the field created due to the applied gate voltage exceeds the critical field of the gate oxide, the oxide breaks down resulting in a short circuit [17, 27]. This effect can occur for any device containing a dielectric, for example capacitors, and is then called SEDR. The oxide thickness is most important for determining the susceptibility of a device to SEGR. The damage induced increases with an increasing voltage applied as well as with an increasing LET [51]. A SEGR or SEDR increases the dielectric leakage current and can destroy the device [18].

Si MOSFETs are more susceptible to SEGRs than SiC MOSFETs. This is because the sensitive volume, which is defined as the active die area multiplied by the drift layer thickness, is larger [33]. Because GaNs

have no gate oxide, no SEGR occurs for these devices. However, a similar phenomenon occurs, which is described in Section 2.1.6. Similarly, diodes have no gate oxide and thus show no SELC.

2.1.5 Single Event Effects: Single Event Burnout

In general, after the SEB threshold voltage is reached, the rate of failure of PECs increases exponentially with an increasing blocking voltage [20, 52, 53]. The threshold voltage depends on the technology used, for example a SiC MOSFET has a lower SEB threshold voltage than a Si MOSFET [16, 54]. When a heavy ion travels through a switch that is in blocking state or through a reversed biased diode, it induces nuclear spallation reactions that frees electrons along the path it travels. This creates electron-hole pairs, and results in highly localised currents [6]. These currents in turn results in a highly localised increase in temperature, which depends on the amount of current generated as well as the bias voltage that is applied. During a SEB, this temperature reaches a critical value that destroys the device. The exact mechanism that triggers the SEB depends on the device and will be discussed next.

BJTs

Electron-hole pairs are generated when an ion hits the BJT. In [55] is discussed that these electrons and holes flow in opposite ways and the emitter-base junction becomes forward biased. Electrons are injected from the emitter, increasing the current density and electric field. If this electric field reaches the critical value for the avalanche multiplication effect, additional electron-hole pairs are generated which results in overheating and destruction of the device. The SEB threshold voltage is larger for BJTs with a thicker epitaxial layer and lighter base doping. Further, they show that the SEB threshold ranges from $10\% V_{\text{CE,rated}}$ to $50\% V_{\text{CE,rated}}$ [55].

IGBTs

In [52] is shown that when incoming heavy ions travel through the high electric field region of the IGBT when it is in blocking state, a shift in the electric field inside the device occurs. This shift causes impact ionisation, which ultimately results in latch-up of the parasitic thyristor during a SEB. A more detailed explanation of the mechanism is given in Appendix A.2.1. Si IGBTs are susceptible for SEBs, and failure starts occurring at bias voltages of $V_{\text{DS}} = 10\% V_{\text{DS,rated}}$ [56].

MOSFETs

The mechanism of a SEB in Si MOSFETs is due to activating the parasitic npn transistor (latch up), or due to directly going into second breakdown [52]. Secondary breakdown is explained in Appendix A.3.2. The main mechanism of SEB in SiC MOSFETs is due to the shift in the electric field and the punch-through in the n+ source diffusion region, not due to the parasitic npn transistor action [57]. This is similar to a SiC diode [20]. A detailed description of the mechanism is given in Appendix A.2.2.

For both Si and SiC, the occurrence of a SEB depends on the V_{DS} applied as well as the LET of the radiation. A larger LET means a SEB may occur at a lower V_{DS}. Si devices are more susceptible for SEBs at LET values larger than 20 MeV$\cdot$ cm^2/mg, and SEBs occur at 25% of their rated V_{DS}. SiC devices started to show SEBs at 40% of their rated V_{DS} for these LET values. However, they are more susceptible for SEBs at LET values less than 20 MeV$\cdot$ cm^2/mg [32]. Proton and neutron-induced SEBs also occur easier in Si than in SiC [53, 58]. Another study found that SiC MOSFETs, when operated below 60% of their breakdown voltage, outperform Si MOSFETs [59]. Note that the previous discussion was for NMOS devices. P-channel Metal-Oxide-Semiconductor (PMOS) devices do not suffer from SEB effects. This is because holes have a lower impact ionisation coefficient than electrons, and because the parasitic transistor is less prone to turn on [27, 60].

GaN FETs

Low voltage E-HEMTs have high SEB tolerances [61, 62]. It is shown that devices up to 300 V can operate up to 90% of $V_{\text{DS,rated}}$ without showing SEBs [40]. Therefore, GaN FETs are more robust to SEBs than Si and SiC MOSFETs, IGBTs, and BJTs [62].

Diodes

Unlike MOSFETs and IGBTs, diodes do not have a parasitic transistor that can be the cause of a SEB. Therefore, the voltage at which a SEB occurs is higher for diodes. The cause of destruction due to radiation in Si power diodes is similar to secondary breakdown [52]. A detailed description of the mechanism is given in Appendix A.2.3.

It is expected that SiC devices have a lower susceptibility to SEBs than Si diodes because of their wide bandgaps and high critical electric fields [63]. For a SiC Schottky and PiN diode, SEBs start to occur at 40% of their rated operating voltage [32, 54]. However, Si Schottky diodes show no SEBs at voltage up to 50% of their rated value [32]. Thus, Si diodes are more robust to SEBs than SiC diodes. Additionally, the 1200 V Si CAL diode showed no failure up to its rated voltage and is even more robust [6, 59].

2.1.6 Single Event Effects: Single Event Leakage Current

Beside SEBs, SiC devices show SELCs. Only SiC devices have shown SELCs, while Si devices do not show this behaviour. The SiC lattice is damaged, which creates a permanent increase of the leakage currents in the device. SELC is different from DD, as it is caused by ionised charge in electric fields [16, 32, 47].

MOSFETs

SELC results in a permanent increase of the gate and drain leakage current. This effect increases with increasing heavy-ion fluence, as well as with increasing V_{DS}. For increasing V_{DS}, after reaching a threshold voltage, the gate and drain leakage currents are increasing linearly with the fluence. After reaching a second threshold voltage, the drain leakage current starts increasing exponentially with the fluence with some saturation behaviour, while the gate current keeps increasing linearly with the fluence [58]. This is similar to SiC diodes and is caused by Joule heating [47]. SiC shows degradation of the gate and drain leakage current for low bias voltages. It is shown that for a $V_{\text{DS}} < 10\% V_{\text{DS,rated}}$ the gate and drain leakage are increased [32].

Diodes

Similar to SiC MOSFETs, SiC diodes also show SELC where their leakage current permanently increases [32]. Due to the temperature increase when hit by radiation, the semiconductor and metal at the Schottky interface are mixed, which causes the increase of the leakage current [19]. It is shown that Schottky SiC diodes start to degrade at 20% of their rated voltage, both for neutrons and heavy ions [16, 54].

GaN

Despite that GaN has no SiC, a phenomenon occurs that is similar to SEGR and SELC. This effect occurs in the intermetallic region between the drain and the source, and results in a permanent increase of the leakage current. This phenomenon can be contributed to impact ionisation, however, the exact mechanism is not known [61]. The leakage current increases rapidly after $V_{\text{DS}} > 50\% V_{\text{DS,rated}}$ for devices rated larger than 200 V [16, 64]. For devices rated to 40 V, no increase of the leakage current is observed [41]. GaN FETs are more robust to this increase in leakage current than SiC MOSFETs, IGBTs, and BJTs [62].

2.1.7 Radiation Hardened Si Devices

There are a couple of radiation hardening techniques for TID and SEEs that are used by manufacturers for radiation-hardened Si devices.

TID

By reducing the gate oxide thickness, the susceptibility to TID is reduced. With a reduced oxide thickness, fewer charges can be trapped. Therefore, the shift in the threshold voltage is lower. Reducing the oxide thickness comes at the cost of increased susceptibility to SEGR [65].

SEGR

Since the neck region is the sensitive region of a MOSFET for SEGR, one method is to reduce the width of the neck region [19, 32]. Another SEGR hardening technique is to add an additional oxide region above the neck region of the MOSFET. This local oxidation silicon layer (LOCOS) reduces the on-resistance and increases the SEGR threshold voltage [66].

SEB

One method to improve the SEB tolerance is to add an additional n^- buffer layer [18–20]. This increases the breakdown voltage and changes the electric field distribution. However, this additional buffer layer increases the on-resistance of the device. This can be done for all device types [52]. For MOSFETs and IGBTs, other methods are focused on optimising the parasitic bipolar transistor region to prevent latch up. Factors that are optimised include the doping and layout of both the source and p-body region [18]. This comes at the cost of reducing the electrical performance of the device, such as an increase in on-resistance. Finally, shielding the device using for example gold, copper, or nickel will reduce the generated electron-hole pairs inside the device [66].

There are radiation-hardened Si MOSFETs available that can withstand TID doses up to 1Mrad. Furthermore, these devices are SEE hardened [67]. For these devices, the Safe Operating Area (SOA) for radiation with different LETs and energies is specified. Using this data, it is ensured that little degradation occurs within the specified dose, as well as no SEEs within the specified gate and drain-source voltages. Similarly, there are radiation hardened GaN devices available with the aforementioned data available.

2.1.8 Passive Components

Not only do semiconductors degrade when exposed to radiation, but passive components as well. The influence of radiation on resistors and capacitors is discussed briefly.

Resistors

Radiation effects on metal film resistors are minimal. It is shown that the resistance value reduces by less than 2% when exposed to 180 krad [68]. Space grade resistors are usually tantalum nitride on silicon, used for communication systems, or nichrome and tin oxide on alumina cores, used for power supplies [69]. If a resistor fails, it fails as an open circuit [70].

Capacitors

Change in the spacing of the plates of the capacitor due to radiation causes a change in capacitance. Organic materials create the most change in spacing and result in the largest change in capacitance. They swell and produce gas that builds up pressure inside the capacitor [71]. Capacitors also suffer from TID, as they have a dielectric material that can accumulate charge. Due to ionisation, the insulation property of the dielectric is degraded [71]. This results in a temporary increase of the leakage current, which disappears when the exposure to radiation is stopped [72]. Finally, capacitors also show SEDR, which is similar to SEGR in MOSFETs. When a heavy ion hits the dielectric, electron-hole pairs are created. This induces an electric field. If the combination of this induced electric field and the electric field created due to the applied voltage exceeds the breakdown voltage locally, SEDR has happened. This results in a permanent increase of the leakage current [72]. If the dielectric is severely damaged, a short circuit is created. Thus, a failed capacitor can act as an open circuit or as a short circuit [70]. Space grade capacitors used are ceramic, tantalum, aluminium, and plastic film capacitors [69].

2.1.9 Comparison Radiation Hardness of Semiconductors

From the previous discussion, the type of semiconductor that is the most radiation-hard can be chosen. This device will result in the highest reliability of the PES in the radiation environment during the mission. The radiation hardness of the switches and diodes is compared.

Switches

An overview of the radiation effects on each of the switches discussed, together with typical dose rates and bias voltages, is given in Table 2.1.

Table 2.1: Overview of the Total Ionising Dose (TID), Displacement Damage (DD), and Single Event Effects (SEEs) on BJTs, MOSFETs, IGBTs, GaN FETs, and rad-hard Si MOSFETs

	TID		**DD**		**SEE**		
	Leakage current	**Threshold shift**	**Sensitivity**	**Effects**	**SEGR sensitivity**	**SEB**	**SELC**
BJT	Increases significantly at 20 krad [29]	-	High [17]	Gain degradation	-	Starts between 10% and 50% of $V_{\text{CE,rated}}$ [55]	-
Si MOSFET	Increases 2 orders of magnitude at 20 krad [36]	Degradation at doses larger than 10 krad [35]	Low [17]	-	Medium [33]	Starts at $25\% V_{\text{DS,rated}}$ [32]	-
SiC MOSFET	See SELC	No degradation up to several hundred krad [33] [34]	Very low [47]	-	Low [33]	Starts at $40\% V_{\text{DS,rated}}$ [32]	Starts at $10\% V_{\text{DS,rated}}$ [32]
Si IGBT	Increases rapidly at several tens of krad [37]	Degradation at doses of several tens of krad [37]	Low [49]	Increase in forward voltage drop	Medium [18]	Starts at $10\% V_{\text{CE,rated}}$ [56]	-
GaN FET	See SELC	Degradation at doses larger than 100 krad [28]	Very low [41]	-	Very low [61]	Starts at $90\% V_{\text{DS,rated}}$ [40]	Starts at $50\% V_{\text{DS,rated}}$ [16] [64]
Rad-hard Si MOSFET	No significant increase up to several hunderds of krad [65]	Small degradation at several hunderds of krad [65]	Low [17]	-	Low [66]	Starts at $50\% V_{\text{DS,rated}}$ [18]	-

In general, Si devices are more vulnerable to threshold voltage shifts and to permanent degradation of the gate and drain leakage due to TID. Significant change occurs at doses of 20 krads. On the other hand, SiC MOSFETs and rad-hard Si MOSFETs are less susceptible to these TID effects, and can withstand several hundreds of krads. However, SiC MOSFETs are more vulnerable to permanent degradation of the gate and drain leakage currents due to SELC, which starts at low bias levels of $10\% V_{\text{DS,rated}}$. Finally, IGBTs have the worst SEB hardness, where SEBs start at $10\% V_{\text{CE,rated}}$. Si MOSFETs show SEBs at $25\% V_{\text{DS,rated}}$, while SiC MOSFETs at $40\% V_{\text{DS,rated}}$. BJTs show SEB between 10% and 50% of $V_{\text{CE,rated}}$, depending on the base doping and epitaxial layer width. Rad-hard Si has the largest SEB hardness, where SEBs start at $50\% V_{\text{DS,rated}}$. Thus, rad-hard Si MOSFETs show the most radiation hardness of all Si-based devices, as they have the largest TID hardness, the highest SEB threshold voltage, and show no SELC.

Comparing GaN FETs and rad-hard Si MOSFETs, GaN FETs suffer less from TID effects because they have no gate oxide. Furthermore, because of the higher displacement energy of GaN, these devices also suffer less from DD. They also have large resistance against SEB, which starts at $90\% V_{\text{DS,rated}}$. The only radiation effect they are susceptible to is SELC. However, devices rated to 40 V show no SELC, only a positive shift in threshold voltage. Therefore, GaN FETs are the most radiation-hard switches.

Diodes

In Table 2.2, an overview of the radiation hardness of the diodes is given.

Table 2.2: Overview of the DD, and SEEs on Si and SiC PiN and Schottky diodes

	DD		SEE	
	Sensitivity	**Effects**	**SEB**	**SELC**
Si Schottky diode	Low [17] [48]	Increase in forward voltage drop at larger fluences, decrease in breakdown voltage	Starts at $50\%V_{\text{rated}}$ [32]	-
Si PiN diode	High [17] [48]	Increase in forward voltage drop at larger fluences, decrease in breakdown voltage	Starts at $50\%V_{\text{rated}}$ [32]	-
SiC Schottky diode	Very low [17] [48]	Increase in forward voltage drop at lower fluences, increase in breakdown voltage	Starts at $40\%V_{\text{rated}}$ [32]	Starts at $20\%V_{\text{rated}}$ [16] [54]
SiC PiN diode	Medium [17] [48]	Increase in forward voltage drop at lower fluences, increase in breakdown voltage	Starts at $40\%V_{\text{rated}}$ [32]	Starts at $20\%V_{\text{rated}}$ [16] [54]

Just as with Si switches, Si diodes are more vulnerable to TID effects than SiC diodes, but less vulnerable to SEBs. Schottky diodes are less susceptible to TID effects than PiN diodes because they are majority carrier devices while PiN diodes are minority carrier devices. Si diodes show better efficiency over time during exposure but have a reduced blocking capability. Finally, SiC also show SELC at low bias voltages of $20\%V_{\text{rated}}$. Thus, Si Schottky diodes are the most radiation hardened diodes, as they have the largest TID hardness, highest SEB threshold voltage, and show now SELC. However, they should be derated to more than 50% to show no SEBs, accounting for the reduced breakdown voltage.

2.2 DC/DC Converter Topologies

The PES contains multiple DC/DC converters. There will be one bidirectional converter connected to the battery, multiple buck converters for the outputs, and either a boost or buck-boost converter connected at the Photovoltaic (PV) panel. In this chapter, different topologies of the aforementioned DC/DC converters are compared. Only hard-switching topologies are considered. No isolated topologies are considered for two reasons. First, the voltages are low enough that they do not pose danger to human interaction. Second, isolation requires bulky transformers. Finally, the advantages and disadvantages of operating the DC/DC converters in CCM and DCM are compared.

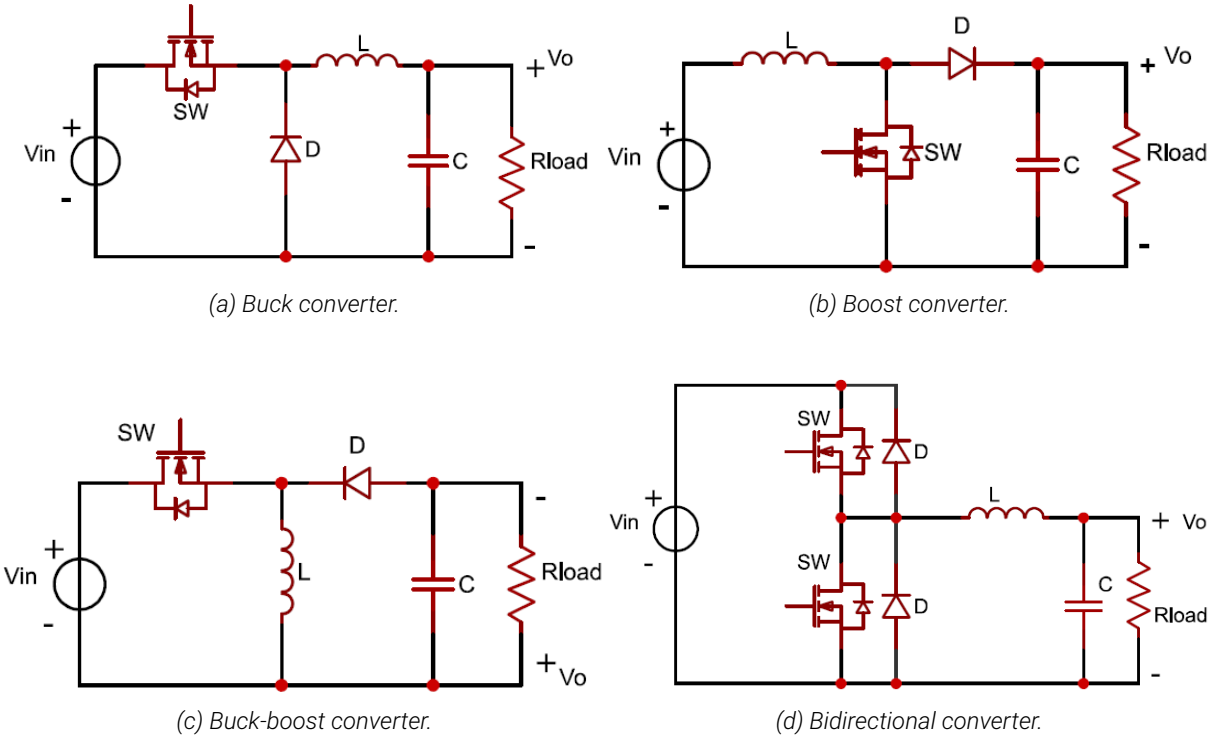
2.2.1 Hard Switching and Soft Switching

DC/DC converters can either have hard switching or soft switching. With hard switching, switching losses occur due to the overlap of non-zero voltage and current during the switching transient. This introduces more Electromagnetic Interference (EMI) than with soft switching due to large di/dt and dv/dt [73, 74]. On the other hand, less reactive components are required and the design is less complicated. Many soft-switching topologies exist [73–80]. They can be divided into Quasi Resonant Converters (QRCs), Multi Resonant Converters (MRCs), Resonant Power Converters (RPCs), and Resonant Transition Converters (RTCs). Compared to single-phase converters, QRCs require the least amount of additional components of all soft-switching topologies, having two additional passive components. Since the design should be as compact as possible, only hard switching topologies are considered. Furthermore, GaN switches have low switching losses compared to other switch types [81]. Hence, the need to reduce the switching losses becomes less apparent.

2.2.2 Single-Phase Converters

Single-phase converters have as advantage that they require the least amount of components. The single-phase buck, boost, and buck-boost converters require a single switch, diode, inductor and capacitor. The bidirectional converter requires two switches and two diodes, as well as an inductor and capacitor. Figure 2.1 shows the topologies of the single-phase buck, boost, buck-boost, and bidirectional converters. The disadvantage of these converters is that soft switching is not possible over their complete operating range.

When operated in CCM, the switch turns off at non-zero current. Only when operated at Boundary Conduction Mode (BCM) or DCM, Zero Current Switching (ZCS) can be achieved because the switch current is zero when turned off. For all three operating regions, Zero Voltage Switching (ZVS) can not be achieved. On the other hand, the peak voltage and current stress on the switch and diode are lower compared to the soft switching topologies. Other single-phase buck-boost topologies, such as the Cuk, SEPIC, and Zeta converters, are not considered. Each of these converters requires two additional passive components while their control complexity is increased [82–86].



(a) Buck converter. *(b) Boost converter.*

(c) Buck-boost converter. *(d) Bidirectional converter.*

Figure 2.1: Single-phase converters.

2.2.3 Interleaved Converters

An interleaved converter has multiple channels of a single-phase converter in parallel. Each channel consists of the switch, diode, and inductor of the corresponding single-phase converter. Further, each channel should be identical to the other channels to share the current equally. The topology of a two-phase interleaved buck, boost, buck-boost, and bidirectional converter is shown in Figure 2.2.

The main advantage of interleaved converters is that the current is shared equally among the channels. This results in a reduction of the conduction losses in the switch, diode, and inductor. Therefore, the efficiency of the converter is increased [87]. Furthermore, the required inductance and capacitance are lower than for single-phase converters. Due to the current sharing, the peak values of the input and output current ripples are reduced, as well as the input and output voltage ripples [88]. Because of the parallel, phase-shifted operation, the multiplicity of the input and output ripples is increased, increasing the frequency of these ripples by N [87, 89]. Here, N is the number of parallel phases. Finally, the transient response is increased, the EMI is reduced, and the reliability of the converter is increased [90–93]. When a failure occurs in a channel, the other channel can still provide power provided that the components in a single-phase can handle the current. The disadvantage of interleaved converters is that more components are required, making the system more expensive.

Interleaved converters are preferred over their conventional counterparts. They have increased efficiency, reduced current and voltage ripples, better transient response, and lower EMI. Finally, they have improved reliability. By ensuring that both channels can handle the maximum output current, one channel alone can still power the load when the other channel fails. This comes at the cost of increased component sizes to handle the full output current instead of half. Because reliability is of utmost importance, interleaved converters are most suitable in terms of reliability, efficiency, size, cost, and complexity.

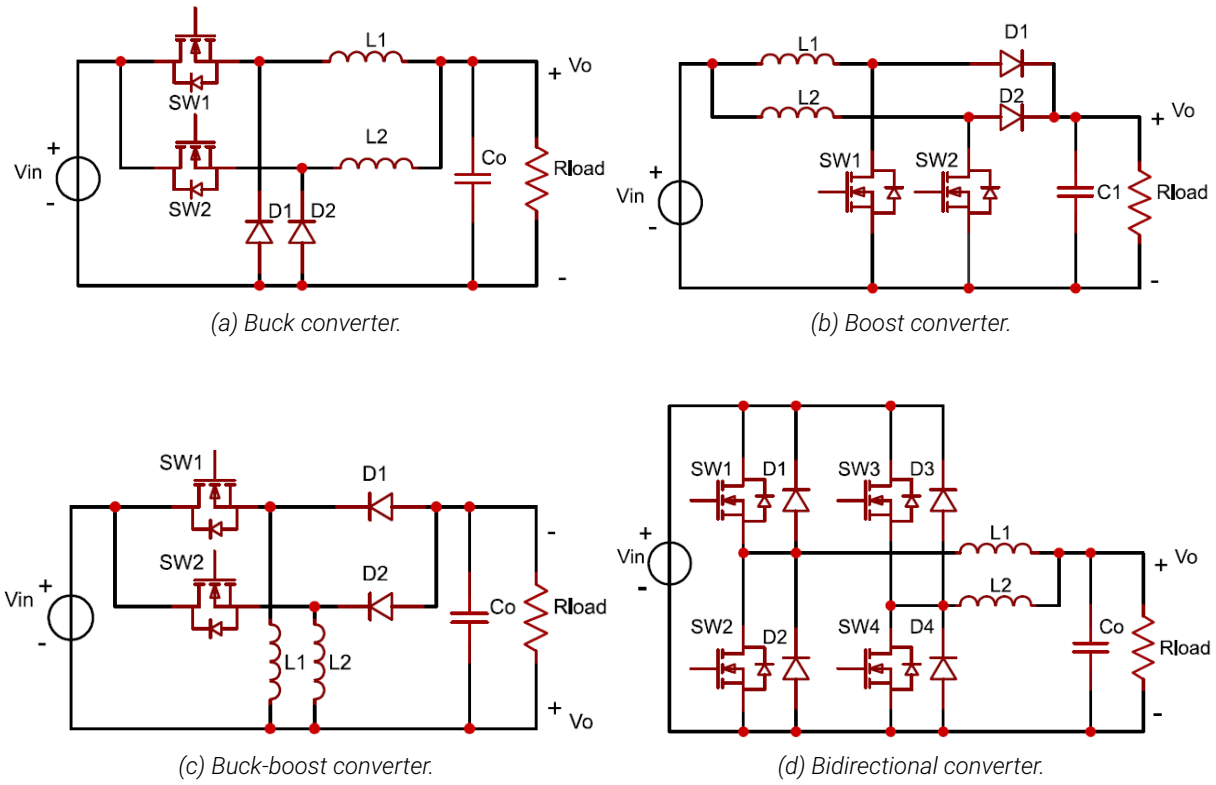


Figure 2.2: Interleaved converters.

2.2.4 Mode of Operation of the DC/DC Converters

The DC/DC converters can be operated in CCM, BCM, and DCM. When operated in CCM, the inductor current never goes to zero during a switching period T_S. At BCM, the inductor current reaches zero exactly at time T_S. With DCM, the inductor current reaches zero before T_S, and remains zero until T_S.

Usually, converters are operated at CCM to obtain high power densities [94]. In this way, the conduction losses at typical load currents are minimised. However, the switching losses are higher than for BCM and DCM. When switching on, the inductor current is non-zero. Thus, the switch is turned on at non-zero current, resulting in switching losses. Furthermore, the diode is still conducting prior to switching on. Therefore, the reverse recovery current of the diode flows through the switch, creating additional turn-on switching losses in the switch. Operating at BCM or DCM do not suffer from these losses [13, 15]. Furthermore, the current ripple is smaller in CCM, resulting in smaller Root Mean Square (RMS) currents. This reduces the conduction losses in the switch, diode, and capacitor, as well as the core losses [14, 15]. However, the inductor required is larger, increasing the winding resistance thus the conduction losses in the inductor [11, 12].

Another disadvantage of CCM is that the transfer function of boost and buck-boost topologies has a right half plane zero [12, 95]. For example, when the load current increases suddenly for a boost converter, the output current of this converter must increase. However, due to the right half plane zero, the output current is decreased initially. Only after a couple of switching cycles, the output current is increased. This problem can be alleviated by reducing the controller bandwidth, which results in a slower transient response. This right half plane zero is not present in the transfer function when operated at DCM.

Operating in DCM results in a smaller inductor. The size of the capacitor must therefore be increased to obtain the desired voltage ripple and cutoff frequency. The equation of the cutoff frequency of the output filter of the DC/DC converters is given in (2.1).

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{2.1}$$

It is desired to have a large capacitance instead of a large inductance for two reasons. First of all, a large

inductor results in more windings, resulting in a higher DC resistance so more conduction losses. A larger capacitance does not suffer from increased conduction losses. Secondly, more energy is stored in the converter when the load current is zero. This energy can be used during transients from no-load conditions to load conditions.

To summarise, DCM has the following advantages:

- Reduced turn-on switching losses due to ZCS and due to the absent of reverse recovery of the diode.
- Smaller inductor required.
- Reduced inductor conduction losses due to reduction of inductor windings.
- No right half plane zero in the transfer function of boost and buck-boost topologies, improving the transient response.
- Large capacitance, increasing the energy stored in the converter at no load.

DCM has the following disadvantages:

- The current ripple is larger than for CCM, resulting in more core losses in the inductor as well as more conduction losses in the switch, diode, and capacitor.
- The current rating of the components must be larger due to the increased RMS currents.
- The saturation current of the inductor must be larger.

It is non-trivial which mode of operation results in the most efficient system. Therefore, one of the research objectives is to compare the efficiency of the PES operating the DC/DC converters in CCM and DCM. This will be discussed in detail in Chapters 3 and 5.

Chapter 3

Design of the Optimal DC Bus Voltage

The value of the DC bus voltage will influence the design and efficiency of the Power Electronic System (PES). It will determine the topology of the PES, the type of DC/DC converters required, the voltage rating of the components, the efficiency of each DC/DC converter, as well as the system efficiency during operation. Two bus voltages are considered: a bus voltage of 12 V and 24 V.

First, in Section 3.2, the specifications of the PES together with its topology for the two different bus voltages are presented. Second, the design of the single-phase converters, as well as the influence of the bus voltage on the design, is covered in Section 3.2. Next, Section 3.3 gives an overview of the specifications and the resulting designs of each converter. This is followed by an analysis of the losses in the converters in Section 3.4. Then, an estimation of the losses during operation is given in Section 3.5. Finally, Section 3.6 gives a summary and the most efficient bus voltage is selected.

3.1 Comparison Topology 12 V and 24 V DC bus

A bus voltage of 12 V and 24 V is considered only, because the voltage of the battery pack varies between 13.5 V and 21 V. Thus, a bus voltage in between this range results in a bidirectional buck-boost converter. This is undesirable, because a buck-boost converter results in larger voltage stress, thus more losses than a buck or boost converter [96]. The core hardware of the PES consists of the following sub-systems:

- The battery pack, consisting of five Panasonic NCR18650B batteries in series having a voltage between 13.5 V and 21 V.
- The PV panel, capable of generating 20.9 W on the moon at Maximum Power Point (MPP) voltage $V_{\text{mpp}} \approx 15.14$ V and MPP current $I_{\text{mpp}} \approx 1.38$ A.
- The bidirectional converter connected to the battery pack, controlling the charging and discharging of the battery pack.
- The DC/DC converter for MPPT of the PV panel.
- The 48 W buck converter that regulates the 12 V output.
- The 20 W buck converter that regulates the 5 V output.
- The 13.2 W buck converter that regulates the 3.3 V output.

These systems together ensure all subsystems in the Zebro rover can be powered and the battery pack can be charged from the PV panel.

3.1.1 12 V bus

The topology of the PES using a 12 V bus is shown in Figure 3.2. With a 12 V bus, the bidirectional converter always operates in buck mode when discharging the batteries. No DC/DC converter is required for the 12 V output. The 12 V output is regulated by the bidirectional converter. However, a buck-boost converter is required for the PV panel. Because the voltage of the PV panel ranges from 0 V to 16.14 V while the bus voltage is 12 V, it should be able to step-up or step-down the voltage to achieve MPPT. A buck-boost converter has larger voltage stress than a buck or boost converter, therefore resulting in more losses [96].

3.1.2 24 V bus

The topology of the PES using a 24 V bus is shown in Figure 3.1. Discharging the batteries results in boost operation of the bidirectional converter. One of the advantages is that a boost converter is required at the PV panel instead of a buck-boost converter. Furthermore, the conduction losses in the DC bus are reduced due to the increase of the voltage. However, a buck converter is required for the 12 V output which introduces additional losses.

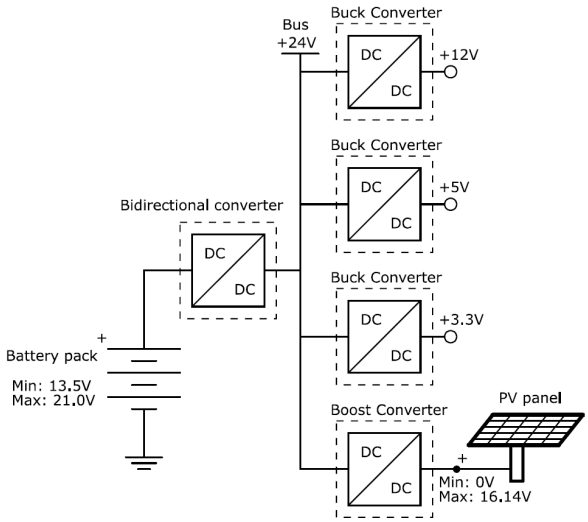


Figure 3.1: PES topology using a 24 V DC bus.

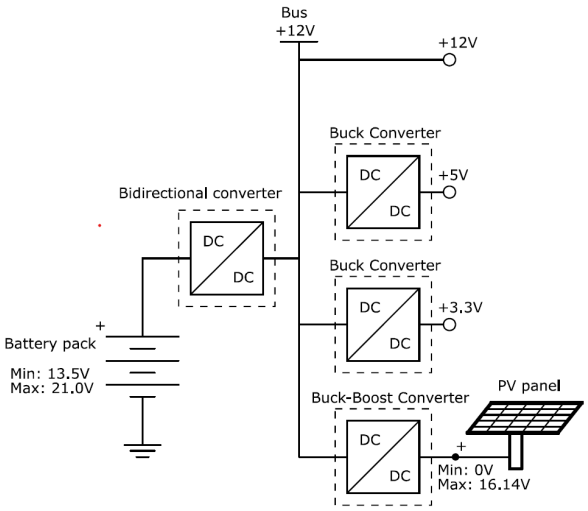


Figure 3.2: PES topology using a 12 V DC bus.

The biggest advantage of the 12 V bus topology is that there is no 12 V buck converter required. This reduces the losses corresponding to the 12 V output. Furthermore, the amount of components is reduced, reducing the cost, size, and weight of the system. However, more losses occur in the PV converter during charging than for the 24 V bus. Therefore, the losses in each DC/DC converter for both topologies are calculated to see which topology results in the highest efficiency. This is done for CCM and DCM operation of the converters for both bus voltages to determine which mode and bus voltage results in the highest efficiency. In addition, the losses based on the usage profile of the rover are estimated for the two bus voltages. The bus voltage and mode of operation that results in the lowest total losses will be determined. The analysis is done for single-phase converters for simplification. It is expected that the results also hold for the interleaved converters since they are a more efficient version of the single-phase converters [87].

3.2 Design Single-Phase DC/DC Converters

The design of the DC/DC converters for a 12 V bus and 24 V bus is discussed next. Each converter is designed for CCM and DCM, where the design equations are derived from [73]. A switching frequency of 100 kHz is used in the analysis. To simplify the design, the following assumptions are made:

- The switches, diodes, inductors, and capacitors are ideal.
- The output capacitor is large enough to maintain a constant output voltage.

3.2.1 Buck Converter CCM

The inductance that results in BCM is calculated using (3.1).

$$L_{\text{BCM}} = \frac{D(V_{\text{bus}} - V_{\text{o}})}{2I_{\text{o,min}}F_{\text{s}}} \tag{3.1}$$

Here, V_{o} is the output voltage, V_{bus} the input voltage, $I_{\text{o,min}} = \frac{1}{2}\Delta I_{\text{L}}$ the minimum inductor current that results in BCM, and F_{s} the switching frequency. The duty cycle D is calculated using (3.2).

$$D = \frac{V_o}{V_{bus}} \tag{3.2}$$

The influence of the bus voltage and output current on the inductance required for the 5 V buck converter to operate in CCM is shown in Figure 3.3. The minimum inductance value required for CCM increases by increasing the bus voltage. Therefore, the inductors for the buck converters using the 12 V bus will be smaller than for the 24 V bus. Furthermore, the inductance required to operate in CCM increases when the output current decreases. Thus, to limit the size of the inductance, $I_{o,min}$=12.5%$I_{o,max}$=0.5 A for all three buck converters.

The minimum output capacitance required is calculated using (3.3).

$$C_{o,min} > \frac{V_o(1-D)}{8LF_s^2\Delta V_o} = \frac{\Delta I_L}{8F_s\Delta V_o} = \frac{I_{o,min}}{4F_s} \tag{3.3}$$

Here, L is the value of the inductance used, ΔV_o the desired output voltage ripple, and ΔI_L the inductor current ripple. In CCM, ΔI_L is independent of the load and depends on the inductance and bus voltage used. Thus, for a larger inductance and fixed bus voltage, ΔI_L reduces and the required output capacitance reduces. On the other hand, for a fixed inductance and larger bus voltage, ΔI_L increases thus increasing the capacitance. When the BCM mode inductance from (3.1) is used, the resulting capacitance depends on the value used for $I_{o,min}$ only.

$$C_{o,min} > \frac{I_{o,min}}{4F_s} \tag{3.4}$$

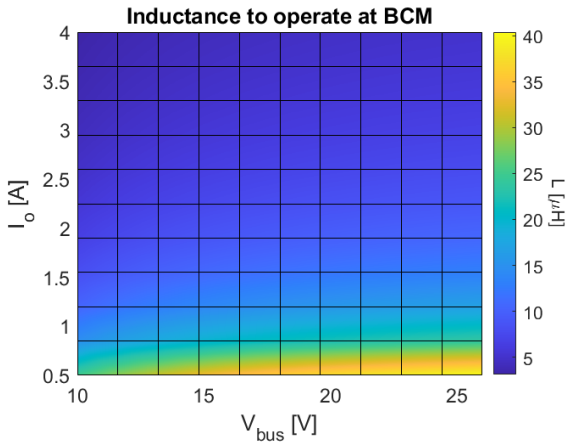


Figure 3.3: The inductance that results in BCM for the 5 V buck converter.

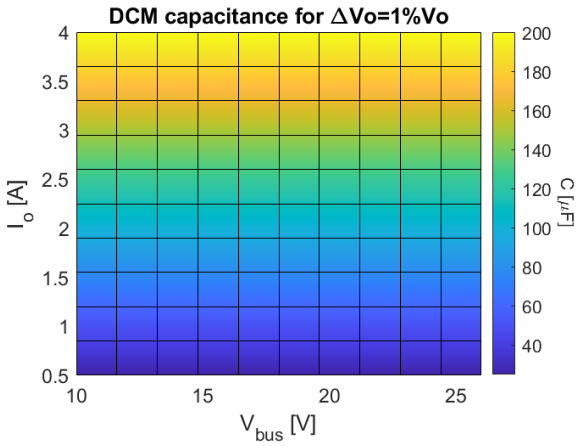


Figure 3.4: Required capacitance in DCM for the 5 V buck converter.

3.2.2 Buck Converter DCM

To operate in DCM, the inductance must be smaller than the BCM value from (3.1). The influence of the bus voltage and output current on the inductance in DCM is also shown by Figure 3.3. However, this figure now shows the maximum inductance required to operate in DCM. Thus, to operate in DCM for the complete output power range, the inductance is calculated at the maximum output current $I_{o,max}$=4 A for all three buck converters.

The minimum output capacitor required is calculated using (3.5).

$$C_{o,min} > \left(\frac{\Delta I_L - I_o}{2\Delta V_o}\right)\left(\frac{L(\Delta I_L - I_o)}{V_o} + D_{DCM}T_s - \frac{LI_o}{V_{bus} - V_o}\right) \tag{3.5}$$

Here, ΔI_L is the inductor current ripple, I_o the output current, L the value of the inductance used for DCM, and T_s the switching time. Finally, D_{DCM} is the duty cycle in DCM, which is calculated using (3.6).

$$D_{\text{DCM}} = \sqrt{\frac{2LP_{\text{o}}F_{\text{s}}}{V_{\text{bus}}(V_{\text{bus}} - V_{\text{o}})}} \tag{3.6}$$

In DCM, the capacitance required depends on the load current. Figure 3.4 shows the output capacitance required for ΔV_{o}=1%V_{o} as a function of the output current and bus voltage. The inductance for BCM is used for each bus voltage and output current. Therefore, the capacitance does not depend on the input voltage. The largest voltage ripple occurs at maximum load, hence (3.5) must be evaluated at I_{o}=4 A.

3.2.3 Boost Converter CCM

For the boost converter, the inductance value depends on the input current. The inductance that results in BCM is given by (3.7).

$$L_{\text{BCM}} = \frac{DV_{\text{pv}}}{2I_{\text{in,min}}F_{\text{s}}} \tag{3.7}$$

The input current and duty cycle are calculated using (3.8) and (3.9), respectively.

$$I_{\text{in}} = \frac{I_{\text{o}}}{1 - D} \tag{3.8}$$

$$D = 1 - \frac{V_{\text{pv}}}{V_{\text{bus}}} \tag{3.9}$$

For the boost converter, the input voltage is the voltage that is applied at the PV panel, and the output voltage is the bus voltage. The input voltage that results in the minimum required inductance for CCM operation is found from solving (3.10) for V_{pv}, which results in $V_{\text{pv}} = \frac{1}{2}V_{\text{bus}}$. This can also be seen in Figure 3.5, which shows the inductance that results in BCM as a function of the input voltage and current using V_{bus}=24 V. The inductance that results in BCM is maximum at V_{pv}=12 V. Figure 3.6 shows the inductance that results in BCM as a function of the input current and bus voltage, using $V_{\text{pv}} = \frac{1}{2}V_{\text{bus}}$. Similar to the buck converter, the larger the bus voltage, the larger the inductance required to operate in CCM. Furthermore, the inductance required is maximum at minimum load current as well. The current ripple is set at 20% of $I_{\text{in,max}}$ to limit the inductance required, which results in BCM mode at an input current of $I_{\text{in}} \approx 239$ mA.

$$\frac{dL_{\text{CCM}}}{dV_{\text{pv}}} = 0 \tag{3.10}$$

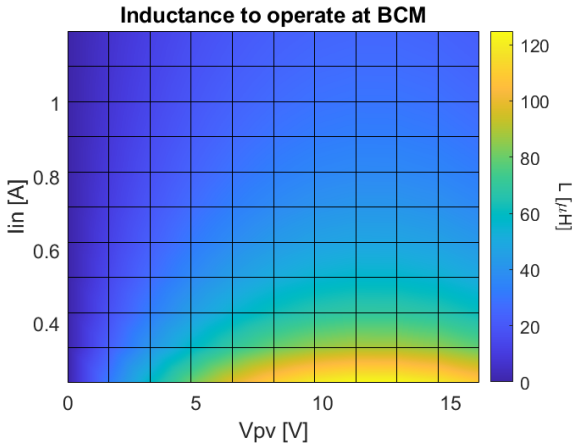


Figure 3.5: The inductance that results in BCM for the PV boost converter using V_{bus}=24 V.

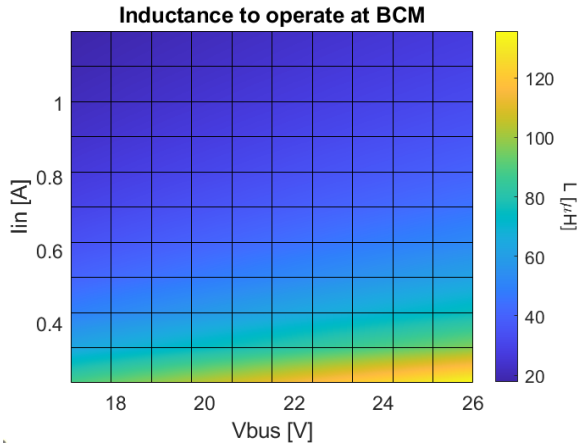


Figure 3.6: The inductance that results in BCM for the PV boost converter using V_{pv}=$\frac{1}{2}V_{bus}$.

The minimum output capacitance required is calculated using (3.11).

$$C_{\text{o,min}} > \frac{DI_{\text{o}}}{\Delta V_{\text{bus}} F_{\text{s}}} \tag{3.11}$$

For the boost converter, the output capacitance required depends on the load current, input voltage, and output voltage. Figure 3.7 shows the output capacitance required for a 1% voltage ripple as a function of the input voltage and current. Similar to the inductance, the capacitance required is maximum for $V_{\text{pv}} = \frac{1}{2}V_{\text{bus}}$. Further, the capacitance required is maximum for maximum load current. The influence of the bus voltage on the output capacitance required for a 1% voltage ripple is shown in Figure 3.8. Increasing the bus voltage results in a lower capacitance required.

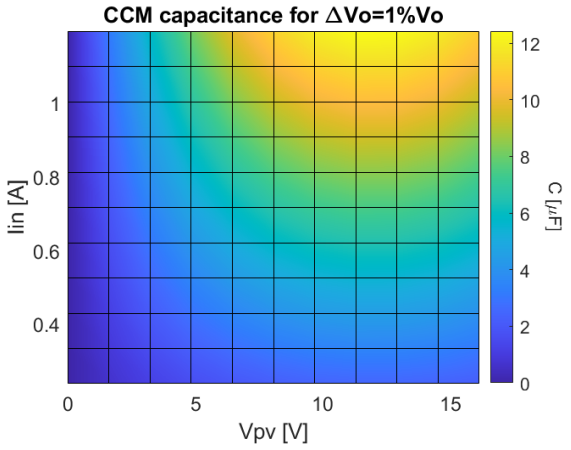


Figure 3.7: Capacitance for the PV boost converter in CCM using V_{bus}=24 V.

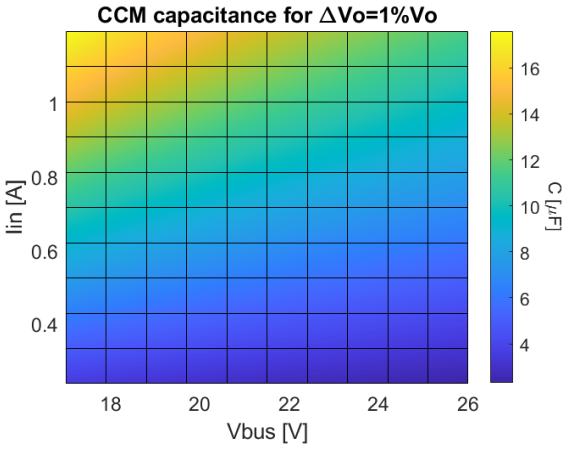


Figure 3.8: Capacitance for the PV boost converter in CCM using V_{pv}=$\frac{1}{2}V_{bus}$.

3.2.4 Boost Converter DCM

The influence of the input current and input voltage on the inductance for DCM is also shown by Figure 3.5. However, this figure now shows the maximum inductance required to operate in DCM. Thus, the inductance should be calculated at the maximum load current to ensure DCM for all input currents. The inductance reduces for smaller PV panel voltages until it becomes 0 μH. This implies that a limit must be set for the PV panel voltage for the converter to start operating in DCM. This limit is set at 20% of $P_{\text{pv,max}}$, so at $V_{\text{pv}} \approx 3$ V. Thus, the converter operates in CCM when the PV panel generates less than 20% of $P_{\text{pv,max}}$, and in DCM when generating more than 20% of $P_{\text{pv,max}}$. The influence of the bus voltage on the inductance required follows the same trend as in Figure 3.6. Thus, a lower bus voltage results in a lower inductance.

The minimum output capacitance required in DCM is calculated using (3.12)-(3.14).

$$C_{\text{o,min}} > \frac{L(\Delta I_{\text{L}} - I_{\text{o}})^2}{2\Delta V_{\text{bus}}(V_{\text{bus}} - V_{\text{pv}})} \tag{3.12}$$

$$\Delta I_{\text{L}} = \frac{D_{\text{DCM}} V_{\text{pv}}}{L F_{\text{s}}} \tag{3.13}$$

$$D_{DCM} = \sqrt{\frac{2P_{\text{o}} L F_{\text{s}}}{V_{\text{bus}} V_{\text{pv}}^2}(V_{\text{bus}} - V_{\text{pv}})} \tag{3.14}$$

Figure 3.9 shows the influence of the PV panel voltage and input current on the output capacitance required, using a bus voltage of 24 V. The output capacitance required is maximum when the PV panel generates maximum power. In Figure 3.10, the influence of the bus voltage is shown. Similar to CCM, by increasing the bus voltage, the output capacitance required is decreased.

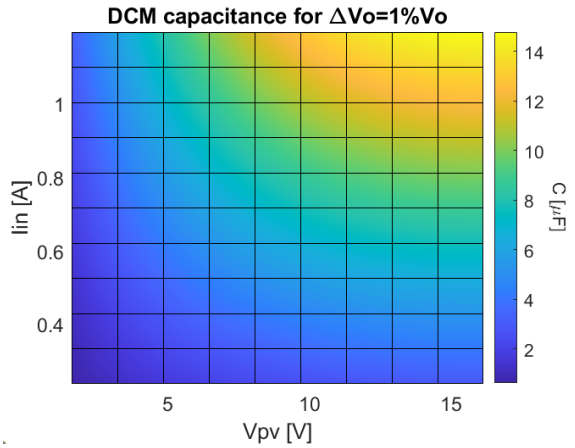


Figure 3.9: Capacitance for ΔV_o=1%V_o for the PV boost converter in DCM using V_{bus}=24 V.

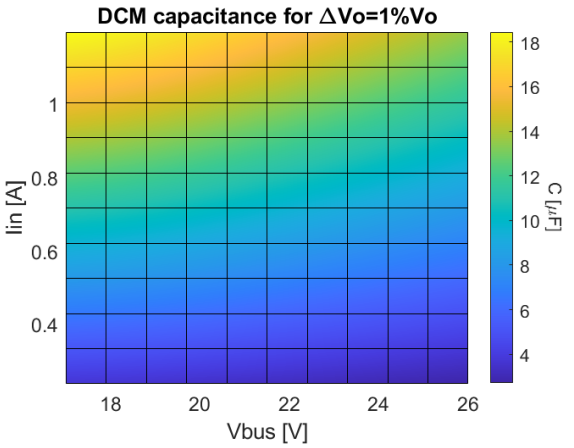


Figure 3.10: Capacitance for ΔV_o=1%V_o for the PV boost converter in DCM using V_{pv}=16.14 V.

3.2.5 Buck-Boost Converter CCM

The inductance that results in BCM is given by (3.15).

$$L_{\text{BCM}} = \frac{V_{\text{pv}} D(1-D)}{2I_{\text{o,min}} F_{\text{s}}} \tag{3.15}$$

The duty cycle of the buck-boost converter is calculated using (3.16).

$$D = \frac{V_{\text{bus}}}{V_{\text{bus}} + V_{\text{pv}}} \tag{3.16}$$

Using (3.15) in (3.10), the input voltage that results in the minimum required inductance for CCM is found at $V_{\text{pv}} = V_{\text{bus}}$. This can be seen from Figure 3.11, which shows the influence of the input voltage and current on the inductance that results in BCM. A bus voltage of 12 V is used in this figure, and the maximum BCM inductance is at V_{pv}=12 V. Figure 3.12 shows the effect of the bus voltage and input current on the inductance required for BCM. Here, $V_{\text{pv}} = V_{\text{bus}}$ is used to obtain the largest inductance. Again, the inductance required to operate in CCM increases for an increasing bus voltage and decreasing input current. The current ripple is set at 20% of $I_{\text{in,max}}$ to limit the inductance required.

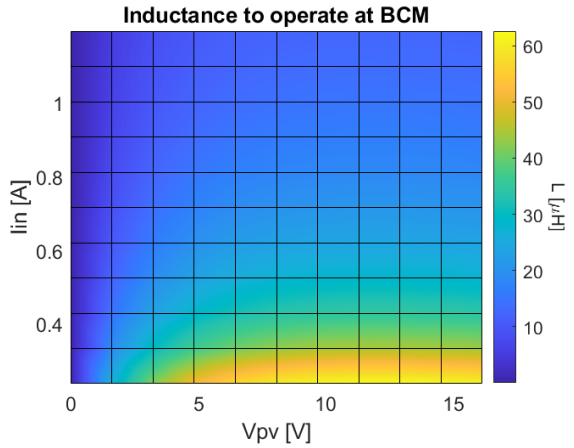


Figure 3.11: The inductance that results in BCM for the PV buck-boost converter using V_{bus}=12 V.

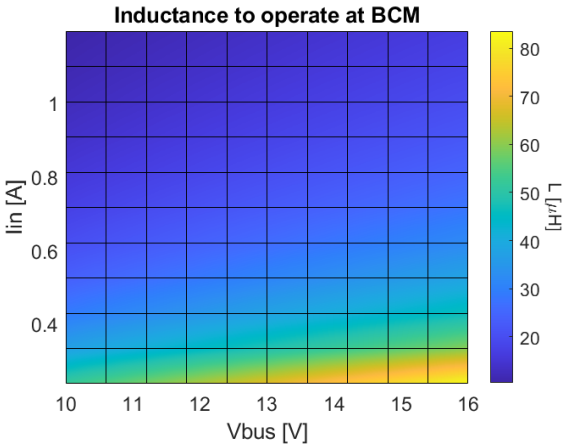


Figure 3.12: The inductance that results in BCM for the PV buck-boost converter using V_{pv}=V_{bus}.

The minimum output capacitance required is calculated using (3.17).

$$C_{\text{o,min}} > \frac{DI_{\text{o}}}{\Delta V_{\text{bus}} F_{\text{s}}} \tag{3.17}$$

Figures 3.13 and 3.14 show the capacitance required as a function of the input current and voltage, and input current and bus voltage, respectively. Similar observations for the boost converter can be made. The capacitance required is maximum at maximum input current and voltage. Furthermore, the capacitance required reduces when the bus voltage is increased as well.

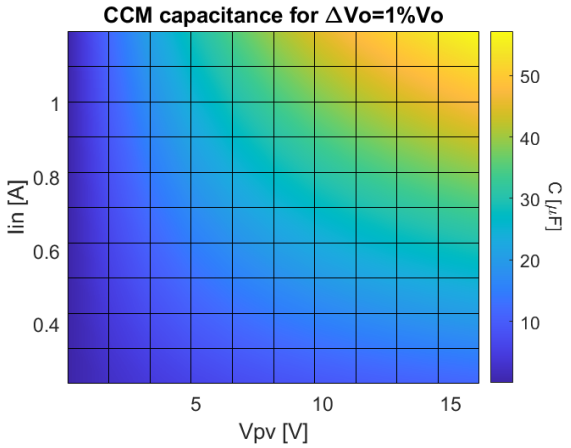


Figure 3.13: Capacitance for ΔV_{o}=1%V_{o} for the PV buck-boost converter in CCM using V_{bus}=12 V.

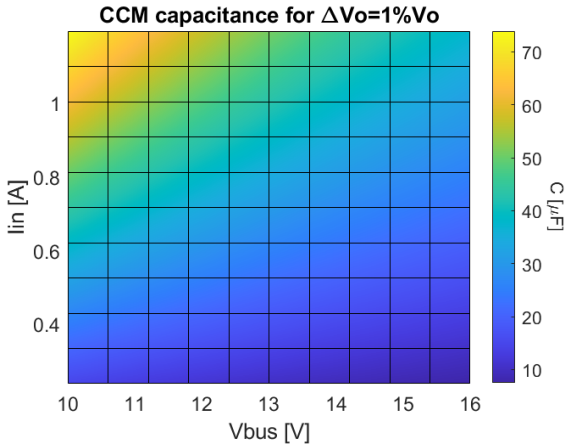


Figure 3.14: Capacitance for ΔV_{o}=1%V_{o} for the PV buck-boost converter in CCM using V_{pv}=16.14 V.

Comparing the inductance required for the PV converter to operate in CCM for a 12 V and 24 V bus from Figures 3.6 and 3.12, a 24 V bus results in a larger inductance. However, by comparing Figures 3.8 and 3.14, the output capacitance required for a 24 V bus is smaller than for a 12 V bus. Therefore, more energy is stored in PV converter using a 12 V bus when the converter is in standby. This is preferred because this energy can be used during transients in the system.

3.2.6 Buck-Boost Converter DCM

For the buck-boost converter in DCM, the influence of the input current and input voltage on the inductance for DCM is also shown by Figure 3.11. However, this figure now shows the maximum inductance required to operate in DCM. Thus, the inductance should be calculated at the maximum input current to ensure DCM for all input currents, and at $V_{\text{pv}} = 0$ to ensure DCM for all PV voltages. However, from (3.16), V_{pv}=0 V results in $D = 1$, which is not realistic. Therefore, similar to the boost converter in DCM, V_{pv}=3 V is used to calculate the inductance. Thus, the converter starts operating in DCM from 20% of maximum power.

The minimum output capacitance is calculated using (3.18).

$$C_{\text{o,min}} > \frac{L(\Delta I_{\text{L}} - I_{\text{o}})^2}{2V_{\text{bus}} \Delta V_{\text{bus}}} \tag{3.18}$$

The current ripple ΔI_{L} is calculated using (3.19).

$$\Delta I_{\text{L}} = \frac{V_{\text{pv}} D_{\text{DCM}}}{L F_{\text{s}}} \tag{3.19}$$

The DCM duty cycle D_{DCM} is calculated using (3.20).

$$D_{\text{DCM}} = \sqrt{\frac{2V_{\text{bus}} I_{\text{o}} L F_{\text{s}}}{V_{\text{pv}}^2}} \tag{3.20}$$

Figures 3.15 and 3.16 show the capacitance required for a 1% output voltage ripple in DCM as a function of the input current and voltage, and input current and bus voltage, respectively. The inductance used in (3.18)

is the value that results in BCM for each input voltage and current in Figure 3.15, and for each input current and bus voltage in Figure 3.16. Similar to CCM, the output capacitance required is maximum at maximum PV voltage. Further, by increasing the bus voltage, the output capacitance required is reduced.

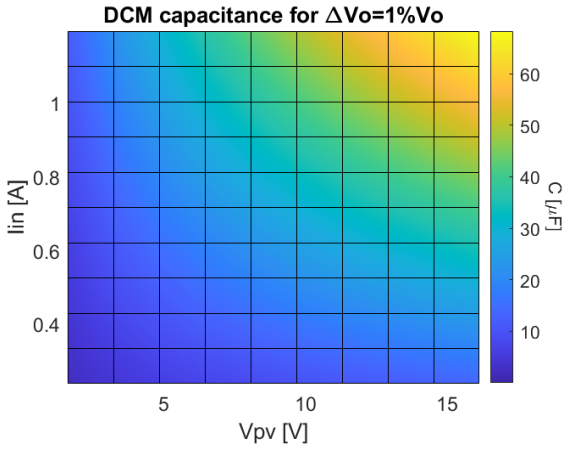


Figure 3.15: Capacitance for ΔV_o=1%V_o for the PV buck-boost converter in DCM using V_{bus}=12 V.

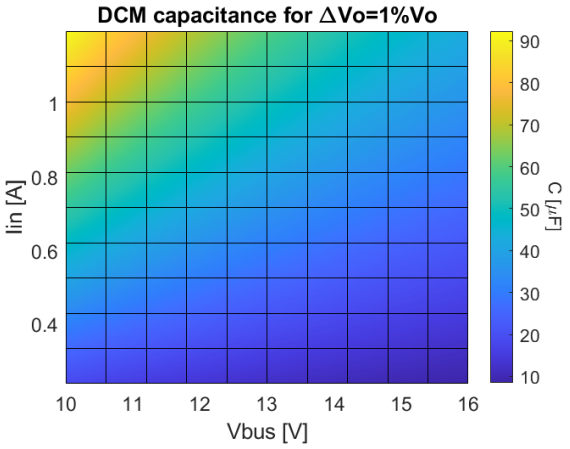


Figure 3.16: Capacitance for ΔV_o=1%V_o for the PV buck-boost converter in DCM using V_{pv}=16.14 V.

3.2.7 Bidirectional Converter

The mode of operation that results in the largest power should determine the design of the bidirectional converter. The maximum power generated by the PV panel is 18 W, while the maximum total power drawn by the outputs is 81 W. Thus, the design should be based on discharging mode. For the 12 V bus, the bidirectional converter always operates in buck mode when discharging the batteries. Therefore, the inductance and capacitance required are given by (3.1)-(3.6). The worst-case condition occurs at maximum battery voltage because then the voltage across the inductance is maximum. Hence, this voltage must be used when evaluating the equations. For the 24 V bus, the bidirectional converter always operates in boost mode when discharging the batteries. Hence, the inductance and capacitance required are given by (3.7)-(3.12). In this case, the worst-case condition occurs at minimum battery voltage. Because this converter has the largest power rating, $I_{o,min}$=10%$I_{o,max}$ to limit the current ripple.

3.3 Specifications and Component Values Single-Phase Converters

The specifications of each converter for a 12 V and 24 V bus are shown in Table 3.1. The resulting values of inductance and capacitance calculated and used are shown in Table 3.2. The power rating of the bidirectional converter is determined from the sum of the power ratings of the three outputs having an assumed efficiency of 90%. The power rating of the PV panel is derived in Appendix D.1.

The choice of inductors is based on the SGIHLP series from Vishay. The capacitors are selected from the Kyocera AVX high reliability tantalum capacitors series. These inductors and capacitors are available in space-grade and non-space-grade variants. For the bidirectional converter, the EPC2014C GaN switches are used. For the other converters, the EPC8004 GaN switches are used. Various Si Schottky diodes are used for the converters.

3.4 Losses in the Single-Phase DC/DC Converters

The losses in the switch, diode, inductor, and output capacitor are considered to determine which bus voltage and mode of operation results in the highest efficiency of each converter.

Table 3.1: Specifications of the single-phase DC/DC converters for a 12 V and 24 V bus.

	P_o [W]	V_{in} [V]	V_o [V]	$I_{o,max}$ [A]	$I_{o,min}$ [A]	ΔV_o [V]
Bus	*Bidirectional*					
12V	90.22	13.5 to 21	12	7.519	0.752	0.12
24V	90.22	13.5 to 21	24	3.759	0.376	0.24
	PV converter					
12V	20.90	0 to 16.14	12	1.74	0.348	0.12
24V	20.90	0 to 16.14	24	0.871	0.174	0.24
	3.3V buck					
12V	13.20	12	3.3	4	0.5	0.033
24V	13.20	24	3.3	4	0.5	0.033
	5V buck					
12V	20	12	5	4	0.5	0.05
24V	20	24	5	4	0.5	0.05
	12V buck					
24V	48	24	12	4	0.5	0.12

Table 3.2: Calculated and used inductor and capacitor values for a 12 V and 24 V bus in CCM and DCM.

		L calc [μH]	L used [μH]	C calc [μF]	C used [μF]
Bus		*Bidirectional*			
12V	**CCM**	34.2	47	11.4	15
	DCM	0.887	0.47	415.81	594
24V	**CCM**	44.19	47	68.53	99
	DCM	3.06	2.2	100.64	132
		PV converter			
12V	**CCM**	54.35	75	64.15	68
	DCM	6.96	6.8	74.02	100
24V	**CCM**	108.70	120	18.14	22
	DCM	9.51	8.2	23.17	33
		3.3V buck			
12V	**CCM**	23.93	33	27.46	33
	DCM	2.99	2.2	395.42	400
24V	**CCM**	28.46	33	32.67	47
	DCM	3.56	3.3	325.81	400
		5V buck			
12V	**CCM**	29.17	33	22.10	33
	DCM	3.65	3.3	219.9	220
24V	**CCM**	39.58	47	21.05	33
	DCM	4.95	4.7	210.28	220
		12V buck			
24V	**CCM**	60	75	8.33	15
	DCM	7.5	6.8	91.49	100

3.4.1 Losses in the Switch

The losses in the switch consist of conduction losses and switching losses. The conduction losses are calculated in (3.21).

$$P_{\text{sw,cl}} = I_{\text{sw,rms}}^2 R_{\text{DS}} \tag{3.21}$$

Here, $I_{\text{sw,rms}}$ is the RMS current in the switch, and R_{DS} the drain-source on-resistance. The switching losses are calculated in (3.22).

$$P_{\text{sw,fs}} = (E_{\text{on}} + E_{\text{off}}) F_{\text{s}} \tag{3.22}$$

Here, F_{s} is the switching frequency, and E_{on} and E_{off} the turn-on and turn-off switching energy loss, respectively. These are calculated using (3.23) and (3.24).

$$E_{\text{on}} = \frac{1}{2} V_{\text{sw,off}} I_{\text{sw,on}} t_{\text{on}} \tag{3.23}$$

$$E_{\text{off}} = \frac{1}{2} V_{\text{sw,off}} I_{\text{sw,off}} t_{\text{off}} \tag{3.24}$$

Here, $V_{\text{sw,off}}$ is the voltage the switch blocks when turned off, $I_{\text{sw,on}}$ and $I_{\text{sw,off}}$ the current that the switch must switch when turned on and off, respectively. Because $I_{\text{sw,on}} = 0$ in DCM, only turn-off losses occur in DCM. Finally, t_{on} and t_{off} are the turn-on and turn-off times of the switch.

3.4.2 Losses in the Diode

The losses in the diode consist of conduction losses and switching losses as well. The conduction losses are due to the forward voltage drop and on-resistance of the diode and is calculated using (3.25).

$$P_{\text{D,cl}} = V_{\text{f}} I_{\text{D,av}} + I_{\text{D,rms}}^2 R_{\text{D,on}} \tag{3.25}$$

Here, V_{f} is the forward voltage drop of the diode, $I_{\text{D,av}}$ the average diode current, $I_{\text{D,rms}}$ the RMS diode current, and $R_{\text{D,on}}$ the on-resistance of the diode. The switching losses are due to the junction capacitance and due to reverse recovery current. However, since Schottky diodes are used, the reverse recovery current can be neglected. Thus, the switching losses in the diode are calculated using (3.26).

$$P_{\text{D,fs}} = \frac{1}{2} C_{\text{j}} V_{\text{R}}^2 F_{\text{s}} \tag{3.26}$$

Here, C_{j} is the junction capacitance, V_{R} the reverse voltage blocked, and F_{s} the switching frequency.

3.4.3 Losses in the Inductor

The losses in the inductor considered are the DC conduction losses and core losses, neglecting the AC winding losses. The DC conduction losses are calculated using (3.27).

$$P_{\text{L,DC}} = I_{\text{L,rms}}^2 R_{\text{DC}} \tag{3.27}$$

Here, $I_{\text{L,rms}}$ is the RMS inductor current, and R_{DC} the DC resistance of the inductor. The core losses in CCM are evaluated using the core loss calculator provided by Vishay [97]. This tool calculates the core losses for CCM only. For DCM, the core losses are calculated using the generalised Steinmetz equation, shown in (3.28).

$$P_{\text{v}} = V_{\text{e}} \frac{k_{\text{i}} \left(\Delta B\right)^{\beta-\alpha}}{T_{\text{s}}} \cdot \left(\left| \frac{\Delta B}{D T_{\text{s}}} \right|^{\alpha} D T_{\text{s}} + \left| \frac{\Delta B}{(1-D)\, T_{\text{s}}} \right|^{\alpha} (1-\text{D})\, T_{\text{s}} \right) \tag{3.28}$$

The Steinmetz coefficients α, β, and k are obtained from curve fitting the core losses in CCM using the core loss tool from Vishay. The exact method is elaborated in Appendix B. Further, V_{e} is the effective core volume, and ΔB the change in flux density, shown in (3.29).

$$\Delta B = L \frac{\Delta I_{\text{L}}}{N A_{\text{c}}} \tag{3.29}$$

Here, N is the number of turns of the inductor, A_c is the area of the cross-section of the bobbin of the magnetic core, and ΔI_{L} is the current ripple in the inductor.

3.4.4 Losses in the Output Capacitor

The losses in the output capacitor considered are conduction losses only. They are calculated in (3.30).

$$P_{\text{Co}} = I_{\text{Co,rms}}^2 R_{\text{ESR}} \tag{3.30}$$

Here, $I_{\text{Co,rms}}$ is the RMS current in the capacitor, and R_{ESR} the equivalent series resistance of the output capacitor.

3.4.5 Currents in the Components

The calculation of the RMS currents of the components, as well as the average diode current in CCM and DCM are shown in Tables 3.3 and 3.4, respectively. Note that the equations for the buck-boost converter and boost converter are equal.

Table 3.3: RMS and average currents of the components required for the loss calculation in CCM.

CCM	**Buck**	**Boost**	**Buck-boost**
$\mathbf{I_{L,rms}}$	$\sqrt{I_o^2 + \frac{\Delta I_L^2}{12}}$	$\sqrt{\left(\frac{I_o}{1-D}\right)^2 + \frac{\Delta I_L^2}{12}}$	$\sqrt{\left(\frac{I_o}{1-D}\right)^2 + \frac{\Delta I_L^2}{12}}$
$\mathbf{I_{sw,rms}}$	$\sqrt{D\left(I_o^2 + \frac{\Delta I_L^2}{12}\right)}$	$\sqrt{D\left(\left(\frac{I_o}{1-D}\right)^2 + \frac{\Delta I_L^2}{12}\right)}$	$\sqrt{D\left(\left(\frac{I_o}{1-D}\right)^2 + \frac{\Delta I_L^2}{12}\right)}$
$\mathbf{I_{D,rms}}$	$\sqrt{(1-D)\left(I_o^2 + \frac{\Delta I_L^2}{12}\right)}$	$\sqrt{(1-D)\left(\left(\frac{I_o}{1-D}\right)^2 + \frac{\Delta I_L^2}{12}\right)}$	$\sqrt{(1-D)\left(\left(\frac{I_o}{1-D}\right)^2 + \frac{\Delta I_L^2}{12}\right)}$
$\mathbf{I_{Co,rms}}$	$\sqrt{\frac{\Delta I_L^2}{12}}$	$\sqrt{\frac{DI_o^2}{1-D} + \frac{(1-D)\Delta I_L^2}{12}}$	$\sqrt{\frac{DI_o^2}{1-D} + \frac{(1-D)\Delta I_L^2}{12}}$
$\mathbf{I_{D,av}}$	$(1-D)I_o$	I_o	I_o

Table 3.4: RMS and average currents of the components required for the loss calculation in DCM.

DCM	**Buck**	**Boost**	**Buck-boost**
$\mathbf{I_{L,rms}}$	$\sqrt{(D+\Delta_1)\frac{\Delta I_L^2}{3}}$	$\sqrt{(D+\Delta_1)\frac{\Delta I_L^2}{3}}$	$\sqrt{(D+\Delta_1)\frac{\Delta I_L^2}{3}}$
$\mathbf{I_{sw,rms}}$	$\sqrt{D\frac{\Delta I_L^2}{3}}$	$\sqrt{D\frac{\Delta I_L^2}{3}}$	$\sqrt{D\frac{\Delta I_L^2}{3}}$
$\mathbf{I_{D,rms}}$	$\sqrt{\Delta_1\frac{\Delta I_L^2}{3}}$	$\sqrt{\Delta_1\frac{\Delta I_L^2}{3}}$	$\sqrt{\Delta_1\frac{\Delta I_L^2}{3}}$
$\mathbf{I_{Co,rms}}$	$\sqrt{(D+\Delta_1)\left(\frac{\Delta I_L^2}{3} - \Delta I_L I_o\right) + I_o^2}$	$\sqrt{\Delta I_L^2\left(\frac{\Delta_1}{3} - \frac{\Delta_1^2}{4}\right)}$	$\sqrt{\Delta I_L^2\left(\frac{\Delta_1}{3} - \frac{\Delta_1^2}{4}\right)}$
$\mathbf{I_{D,av}}$	$\Delta_1\frac{\Delta I_L}{2}$	$\Delta_1\frac{\Delta I_L}{2}$	$\Delta_1\frac{\Delta I_L}{2}$

3.4.6 Results

The losses in each component for the converters operating in CCM and DCM for the 12 V and 24 V bus are shown as a stacked bar graph in Figure 3.17. The losses are shown as a percentage of the power rating of the corresponding converter. For all converters holds that operating in CCM results in higher efficiency than operating in DCM. This is mainly due to the decrease of the losses in the inductor. The losses in the inductor are significantly larger for DCM as compared to CCM, which is caused by the significant increase in the core losses. In [14] it is shown that the core losses in DCM can reduce the efficiency by 10% relative to CCM.

For the bidirectional converter, only for DCM operation the 24 V bus results in a notably increased efficiency compared to the 12 V bus. The 24 V bus in DCM results in a 2.57% increase in efficiency compared to the 12 V bus in DCM. From Figure 3.17, the losses in the switch and output capacitor in DCM are reduced significantly for the 24 V bus compared to the 12 V bus. This is caused by the reduction of the currents due to the increased bus voltage. Note that the capacitor losses for the 12 V bus in CCM are 0.0 For operation in CCM, the efficiency using the 24 V bus is increased by 0.02% compared to the 12 V bus.

Similarly, the PV converter is more efficient for a 24 V bus than for a 12 V bus. This is expected because the PV converter is a boost converter for the 24 V bus, which is in general more efficient than the buck-boost converter used for the 12 V bus [98, 99]. Furthermore, DCM operation is less efficient than CCM operation. For CCM operation, the efficiency for the 24 V bus is increased by 1.15% compared to the 12 V bus. For DCM operation, the efficiency using the 24 V bus is increased by 6.72% compared to the 12 V bus.

On the other hand, for the 5 V and 3.3 V buck converters, operating at a 12 V bus results in higher efficiency than at a 24 V bus. This is mainly due to the reduced losses in the diode. The duty cycle is higher for the 12 V bus, so the diode conducts for a shorter amount of time while the switch conducts longer compared to the 24 V bus. The conduction losses in the diode are usually larger than the conduction losses in the switch due to the contribution of the forward voltage drop in the diode [11]. To improve the efficiency, synchronous rectification can be implemented [100]. As expected, the losses in the switch of the 12 V bus are increased compared to the 24 V bus because the duty cycle is larger for the 12 V bus.

The 3.3 V buck converter has remarkably low efficiencies, mainly in DCM. This can be accounted for by the fact that the power rating is low (13.2 W) while the current is relatively large (4 A). Therefore, the conduction losses make up a significant part of the total power. Furthermore, the core losses of the inductor in DCM are 1.81 W and 1.85 W for the 12 V and 24 V bus, respectively. This corresponds to a 13.7% and 14.0% drop

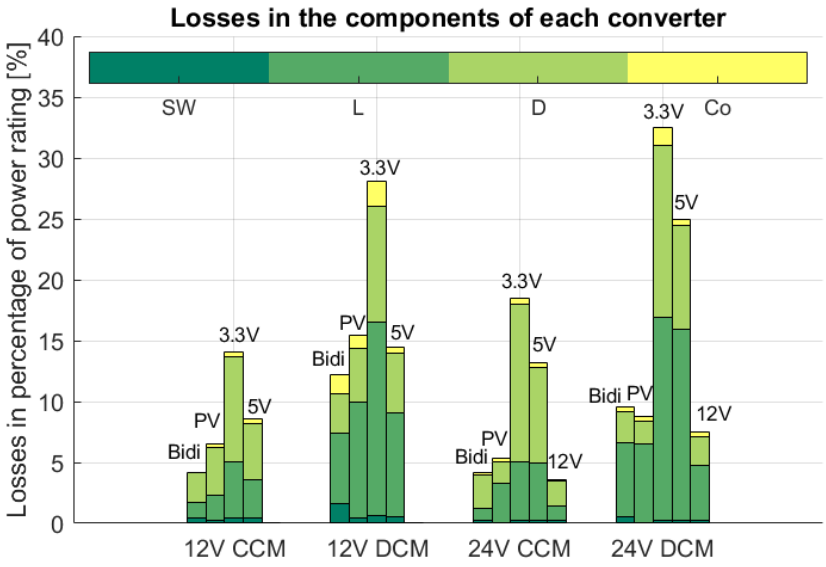


Figure 3.17: Losses in the switch (SW), inductor (L), diode (D), and output capacitor (Co) of the bidirectional (Bidi), PV buck or buck-boost converter (PV), 3.3 V buck (3.3V), 5 V buck (5V), and 12 V buck (12V) converters.

in efficiency. From Figure 3.18 can be seen that the losses in the 3.3 V, 5 V, and 12 V buck converters differ by less than 1 W. This small difference is because different inductors and capacitors are used. Therefore, the low efficiency of the 3.3 V buck converter is acceptable.

In [101], a synchronous buck converter operating in CCM at 1.2 V and 6 A output has a measured efficiency of 95%. It is found that approximately 80% of the losses in the diodes of the 5 V and 3.3 V buck converters are due to the forward voltage drop. Thus, it is expected that these converters in CCM approach a 90% efficiency when operated in synchronous topology, which is in good agreement with [101].

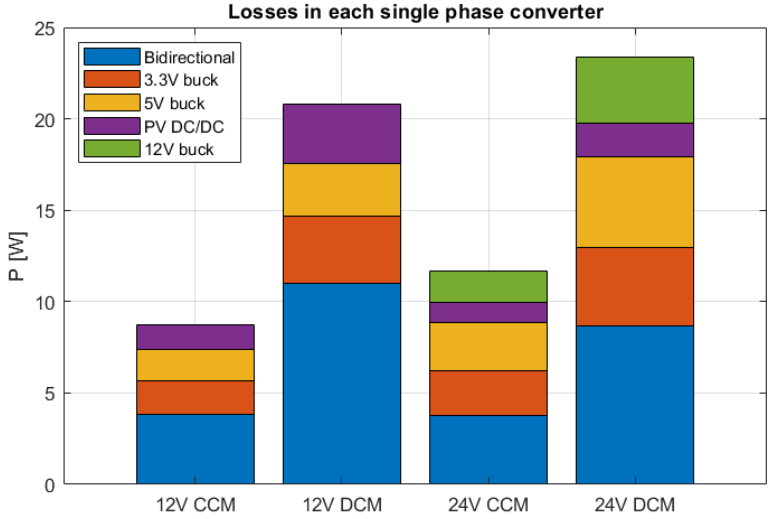


Figure 3.18: Losses in the single-phase converters for a 12 V bus and 24 V bus operating in CCM and DCM.

The losses are summed up to determine which bus voltage and mode of operation results in minimal total losses. This is shown in Figure 3.18. Operating in CCM with a 12 V bus results in an increase of 33.78% of efficiency compared to the 24 V bus in CCM. Similarly, operating in DCM with a 12 V bus results in a 12.34% improvement in efficiency compared to DCM operation with a 24 V bus. Notably, for both the 12 V and 24 V bus configurations, operating in CCM is more efficient than operating in DCM and consequently results in the lowest total losses. When utilising the 12 V bus, operating in CCM results in a 138.45% increase in efficiency compared to operating in DCM, whereas the 24 V bus demonstrates a 100.22% increase. Therefore,

it can be concluded that operating the DC/DC converters in CCM results in a higher efficiency than DCM. Furthermore, for a given mode of operation, a 12 V bus is more efficient than a 24 V bus.

3.5 Losses Based on Usage Profile

The previous analysis was done for the converters operating at maximum load. However, a more realistic estimation of the losses is made based on the usage profile of the rover. This is done by calculating the average power loss during one operational cycle. One operational cycle means that the fully charged batteries are first fully discharged at constant load without energy generated from the PV panel, after which they are completely charged from the PV panel at maximum power point without any loads. This is a realistic usage scenario for the rover because during charging operation the rover does not walk or carry out non-critical tasks. The influence of adding the 12 V buck converter but having a more efficient boost converter for the 24 V DC bus topology will be compared to the 12 V DC bus topology, where a less efficient buck-boost converter is used but no 12 V buck converter is required. This is done for the DC/DC converters operating in CCM because it was found to be more efficient than operating in DCM. The following assumptions are made:

- The average output current drawn by the 12 V, 5 V, and 3.3 V outputs is 1 A.
- The efficiencies of the converters operating at 1 A are equal to the efficiencies calculated in Section 3.4.6, so these efficiencies are used in the analysis.
- The efficiency of the bidirectional converter is the same during charging and discharging.

The average power loss during one operational cycle is calculated using (3.31).

$$P_{\text{L,av}} = \frac{E_{\text{L,w}} + E_{\text{L,ch}}}{t_{\text{cycle}}} = \frac{P_{\text{L,w}} t_{\text{w}} + P_{\text{L,ch}} t_{\text{ch}}}{t_{\text{w}} + t_{\text{ch}}} \tag{3.31}$$

Here, $E_{\text{L,w}}$ is the total energy loss in the 12 V buck converter during walking, and $E_{\text{L,ch}}$ is the total energy loss in the DC/DC converter of the PV panel during charging. Similarly, $P_{\text{L,w}}$ and $P_{\text{L,ch}}$ are the power losses during walking and charging in the corresponding DC/DC converters, and t_{w} and t_{ch} are the times the rover walks and charges, respectively. Using (3.32) $P_{\text{L,w}}$ is calculated

$$P_{\text{L,w}} = P_{\text{L,12V,w}} + P_{\text{L,5V,w}} + P_{\text{L,3V3,w}} + P_{\text{L,bi,w}} \tag{3.32}$$

Here, $P_{\text{L,12V,w}}$, $P_{\text{L,5V,w}}$, and $P_{\text{L,3V3,w}}$ are the losses in the 12 V, 5 V, and 3.3 V buck converters during walking, and $P_{\text{L,bi,w}}$ the losses in the bidirectional converter during walking. These are calculated using (3.33), where $P_{\text{o,conv}}$ is the output power of the corresponding converter and η_{conv} the corresponding efficiency.

$$P_{\text{L,conv,w}} = P_{\text{o,conv}} \left(\frac{1}{\eta_{\text{conv}}} - 1 \right) \tag{3.33}$$

Further, $P_{\text{L,ch}}$ from (3.31) is calculated using (3.34).

$$P_{\text{L,ch}} = P_{\text{L,pv,ch}} + P_{\text{L,bi,ch}} \tag{3.34}$$

Here, $P_{\text{L,pv,ch}}$ and $P_{\text{L,bi,ch}}$ are the losses in the PV DC/DC converter and bidirectional converter during charging. These are calculated using (3.35).

$$P_{\text{L,conv,ch}} = P_{\text{in,conv}} \left(1 - \eta_{\text{conv}}\right) \tag{3.35}$$

Here, $P_{\text{in,conv}}$ is the input power of the corresponding converter, and η_{conv} the corresponding efficiency. Further, P_{PV}=20.90 W is the maximum power generated from the PV panel. The time in seconds the rover can walk and needs to charge is calculated using (3.36) and (3.37).

$$t_{\text{w}} = \frac{E_{\text{bp}}\eta_{\text{bi}}}{P_{\text{o,bi}}} \cdot 3600 \tag{3.36}$$

$$t_{\text{ch}} = \frac{E_{\text{bp}}}{P_{\text{PV}}\eta_{\text{pv}}\eta_{\text{bi}}} \cdot 3600 \tag{3.37}$$

Here, E_{bp} = 57.60 Wh is the capacity of the battery pack and $P_{\text{o,bi}}$ the output power of the bidirectional converter, calculated from (3.38).

$$P_{\text{o,bi}} = \frac{P_{\text{o,12V}}}{\eta_{\text{12V}}} + \frac{P_{\text{o,5V}}}{\eta_{\text{5V}}} + \frac{P_{\text{o,3V3}}}{\eta_{\text{3V3}}} \tag{3.38}$$

Here, $P_{\text{o,12V}}$, $P_{\text{o,5V}}$, and $P_{\text{o,3V3}}$ are the average output power of the 12 V, 5 V, and 3.3 V outputs, respectively. The resulting energy losses during walking and charging, the time the rover can walk and needs to charge, and the resulting average power loss for the 12 V and 24 V bus are summarised in Table 3.5.

Table 3.5: Resulting energy loss and time for walking and charging, and average power loss.

	$\mathbf{E_{L,w}}$	$\mathbf{t_w}$	$\mathbf{E_{L,ch}}$	$\mathbf{t_{ch}}$	$\mathbf{P_{av}}$
12 V bus	18.07 kJ	2.59 h	24.16 kJ	3.08 h	2.07 W
24 V bus	26.09 kJ	2.48 h	21.25 kJ	3.04 h	2.38 W

For the 12 V bus, the losses during walking are reduced by 30.51% compared to the 24 V bus, while the losses during charging are increased by 13.46%. As a result, the 12 V bus has 310 mW less losses on average compared to the 24 V bus, which is a reduction of 13.02%. Therefore, from an operational point of view, the 12 V bus results in an PES with a higher efficiency.

3.6 DC Bus Selection

It was found that the combined losses in the DC/DC converters are lower for a 12 V bus than for a 24 V bus. The least amount of losses is obtained using a 12 V bus operating in CCM, with a total power loss of 8.72 W. Furthermore, it was found that the 12 V bus results in the least amount of average power loss during operation as well, where a reduction of 13.02% was observed compared to the 24 V bus. Thus, it can be concluded that a bus voltage of 12 V results in a more efficient PES, and therefore this bus voltage will be used. The mode of operation that results in the highest efficiency in the interleaved converters for the 12 V bus will be explored in more detail in Chapter 5.

Besides the increased efficiency, the 12 V bus has as advantage that no additional 12 V buck converter is required, reducing the size and weight of the system. Moreover, the 12 V bus results in lower inductance required for a specified current ripple than the 24 V bus. In Section 5.5.3 is shown that the inductors take up most space in the design. Thus, the size and weight are even further reduced using the 12 V bus compared to the 24 V bus. The only disadvantage is that the capacitance required for a specified voltage ripple is larger. However, the increase in size of the capacitors is insignificant compared to the reduction of inductor sizes. Furthermore, larger capacitance has more energy stored when the system is idle. In contrast, larger inductance has more energy stored only when current is flowing. Thus, the 12 V bus increases the energy available when the PES transits from idle to operation.

Chapter 4

Redundancy in the Power Electronic System

The Power Electronic System (PES) is the most critical system in the rover. When a DC/DC converter fails, the rover loses all functionalities that are powered by that converter. By implementing redundancy, the system reliability is increased [8]. In Section 2.2 was proposed to use interleaved converters. They provide redundancy and have better performance than the single-phase variants. Therefore, the goal of this chapter is to explore different redundancy methods and compare the resulting footprint and component count with the non-redundant single-phase converters. Finally, the optimal redundancy method is selected to implement in the PES.

4.1 Redundant Systems

In a redundant system, relaying, backup components, and tripping circuits are incorporated to reduce the probability that failure of a single component results in the failure of the system. Common metrics to evaluate system reliability are failure rate, mean time between failures, and availability [102]. However, a precise mathematical model is required based on empirical and physics-of-failure models. Since this is not the focus of this thesis, only an objective analysis is made to come to a fault-tolerant system.

Electrolytic capacitors and power switching devices are the main components that put the reliability of the system in jeopardy [102, 103]. From Chapter 2.1, a capacitor and switch can fail as either an open circuit or a short circuit. When an open circuit occurs, a redundant component should be there to take over the functionality. For a short circuit, the short should first be isolated from the system before the redundant component takes over. Since space-grade tantalum capacitors are used, no redundancy measures are required for short-circuit faults of the capacitors.

There are four categories for hardware redundancy: switch level, leg level, module level, and system level [102]. For the switch level, parallel or series redundant switches are employed. Parallel redundant switches result in higher redundancy since they account for both open and short circuit failure of a switch, while series only account for short circuit failure. Parallel switches can operate in online or offline mode. In online mode, the redundant switch is used during normal operation. In offline mode, the redundant switch is not used during normal operation but only when the main switch fails. The leg level includes an additional redundant leg in the system. For online mode, this results in the interleaved converters covered in Chapter 2.2.3. It is shown that for full fault-tolerant design, the redundant leg is the best tradeoff between cost, performance, and reliability [102]. Multilevel modular converters are an example of module-level redundancy. Finally, the system level incorporates a redundant converter. Similar to switch level, connecting the redundant system in parallel connection results in higher reliability than cascaded [102].

When a fault occurs, the first step is to isolate the fault from the system. GaN switches can handle short pulses of high currents and fast-blow fuses are available. Therefore, simple isolation with the aid of a fuse is possible with as only drawback the added series inductance [102]. Other methods include adding a triac or switch to reconfigure from the faulty switch to the backup switch [104, 105]. The drawback is that additional fault diagnostics and control are required.

Only leg-level and system-level redundancy are considered. To implement the switch level redundancy for a single-phase converter, an additional switch and gate driver are required. The only difference between the resulting topology and an interleaved converter is an additional inductor and diode. From Chapter 2.2,

the interleaved converter has many advantages over the single-phase converter. Hence, the switch level redundancy is not considered.

4.2 System Level Redundancy

At system level, N denotes the minimum amount of DC/DC converters required to operate. Different levels of redundancy can be included. The minimum amount to achieve redundancy is N+1, where a single DC/DC converter is redundant. When a redundant converter is present for each DC/DC converter, 2N redundancy is achieved. Both options are explored in more detail. Figures 4.1 and 4.2 show the topology of the PES for N+1 and 2N redundancy, respectively. A fuse is placed in series with each converter. This fuse should blow when a fault occurs in the converter, effectively isolating the faulty converter from the system.

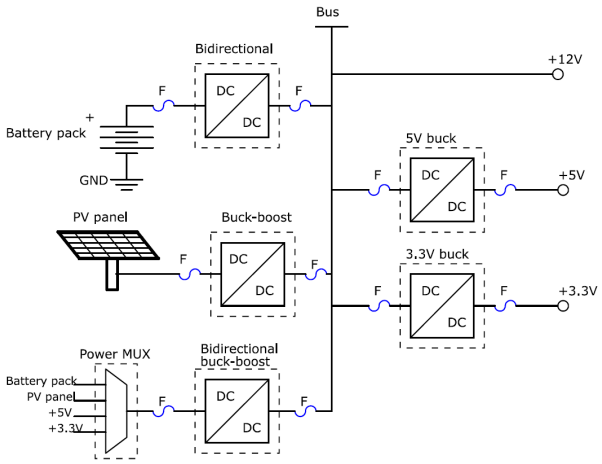


Figure 4.1: PES topology for N+1 system level redundancy.

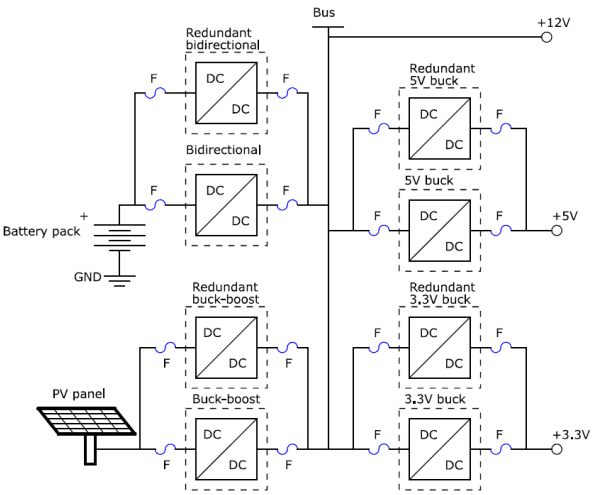


Figure 4.2: PES topology for 2N system level redundancy.

4.2.1 N+1 Redundancy

In N+1 redundancy, a single redundant DC/DC converter is added to the system. This redundant converter must be able to replace each of the DC/DC converters of the PES. It must support bidirectional power flow to be able to replace the bidirectional converter connected to the battery and must support buck-boost operation to be able to replace the buck-boost converter at the PV converter. Therefore, this converter must be a bidirectional buck-boost converter. It can then inherently also function as the 5 V and 3.3 V buck converter.

The main advantage of this topology is that minimum amount of components are added to the system. This reduces the size, weight and cost of the system. However, this topology has several disadvantages. First of all, it can replace only one faulty converter. Secondly, the redundant converter has a buck-boost topology. This results in more losses than a buck or boost converter [96]. Finally, additional hardware and control are required to reconfigure the correct input to the redundant converter. This can be done using a power multiplexer or a relay. Electromechanical relays are not considered since they are very sensitive to mechanical shocks and vibrations. Furthermore, only a few space-grade variants are commercially available and are bulky (e.g. the footprint of EV250 from Kilovac is 5.72x6.99 cm).

Power Multiplexer

The power multiplexer is responsible for selecting the correct input for the redundant bidirectional buck-boost converter. This should be based on which converter has a fault and needs to be replaced. The power multiplexer can be implemented using discrete switches, or using a fully-integrated Integrated Circuit (IC). The multiplexer can be controlled manually, automatically, or both. When controlled manually, a control signal from the microcontroller selects what input to supply to the output of the multiplexer. When con-

trolled automatically, it will determine which input to supply to the output based on a set threshold, for example, the voltage of the first input [106]. The power multiplexer has the following requirements:

- It should have bidirectional power flow to charge and discharge the batteries when it replaces the bidirectional converter.
- It should have automatic control. During a fault in the 3.3 V line, the power to the microcontroller is interrupted. Therefore, it should not rely on manual control from the microcontroller.
- It should have a current rating of at least 6.7 A. The current rating is determined from the DC/DC converter with the highest current rating, which is the bidirectional converter.
- It should have a voltage rating larger than 21 V, determined by the maximum battery voltage.

No integrated IC multiplexer is available that can handle the current rating. Furthermore, no IC multiplexer with more than two inputs is available that has both the required voltage rating and significant current rating. The TPS2121 from Texas Instruments is one of the few ICs that has both a large current rating (4.5 A) and a voltage rating higher than the maximum battery voltage. Furthermore, it supports bidirectional current flow. It has two inputs and one output. Therefore, at least four are required to implement the power multiplexer from Figure 4.1.

In Figure 4.3, the power multiplexer implemented using four of the TPS2121 from Texas Instruments is shown. Each of the multiplexers M1-M4 can be controlled using low-power discrete logic gates. They should select their input based on the status of the corresponding converters. For example, when a fault occurs in the 5 V buck converter, M1 should select input 1, M2 should select input 1, and M3 and M4 should select input 2. Two multiplexers, M3 and M4, are required in parallel to handle the current of the bidirectional converter.

Figure 4.4 shows a two-input one-output automatic multiplexer implemented using discrete switches. The comparator is set to connect input supply 1 to the output V_{MUX_OUT} when input 1 is present, else it connects input supply 2 to the output. The four-input one-output multiplexer from Figure 4.1 can be realised by adding two more parallel circuits and modifying the control circuit. The control circuit consists of comparators to drive the switches, and low-power discrete logic gates to determine which switch to drive. Because this method is significantly more complex to design, only the method using the TPS2121 multiplexer from Texas Instruments is considered.

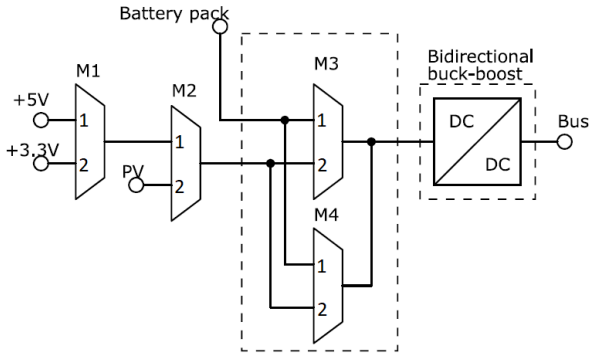


Figure 4.3: Power multiplexer from Figure 4.1 implemented using the TPS2121 from Texas Instruments.

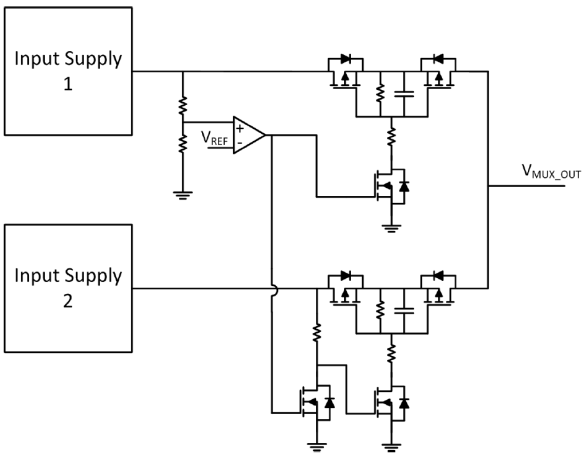


Figure 4.4: Automatic 2-input 1-output power multiplexer implemented using discrete switches [106].

4.2.2 2N Redundancy

With 2N redundancy, every DC/DC converter has a backup. Figure 4.2 shows the simplest case, where each converter has a copy of itself connected in parallel. When a failure occurs in the main converter, the redundant converter takes over. In case a short circuit occurs, the fuse in series with the DC/DC converter should trip.

The main advantage of this topology is the amount of redundancy added. Each converter can be replaced, independently from the type of fault in the converter. Furthermore, the control required is simple. The controller should know which converter has a fault, and send gate signals to the backup converter instead of the main converter. The main drawback of this topology is the amount of components required is doubled compared to the single-phase topology without redundancy.

4.3 Leg-Level Redundancy

Leg-level redundancy for the single-phase converters results in interleaved converters. By increasing the number of phases N, the input and output current ripples are reduced, as well as the RMS currents in each phase [107, 108]. However, increasing the number of phases from two to more does not necessarily increase the efficiency of the converter [88]. Therefore, only one redundant leg is considered. In this way, the additional amount of components is minimised, while still benefiting from the improved performance and reliability compared to a single-phase converter. To create redundancy in the interleaved converters from Chapter 2.2.3, small adjustments need to be made. This is achieved by placing redundant capacitors, and by placing fuses in series with the input and output of each phase leg. Figure 4.5 shows the interleaved buck-boost including these redundancy measures.

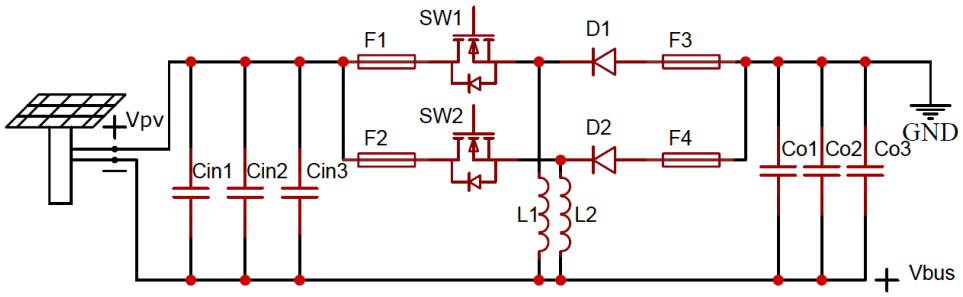


Figure 4.5: Interleaved buck-boost including redundancy measures.

When one of the switches fails as open circuit, no measures need to be taken and the other phase leg can take over. When the switch fails as short circuit, the fault needs to be isolated from the converter before the other switch can take over. Therefore, a fuse in series with each switch should be placed. When the switch shorts, the fuse trips, effectively isolating the fault from the converter [104, 105]. This is done for the interleaved bidirectional, buck-boost, and both buck converters. Similarly, when the diode fails as a short circuit, the fuse in series with the diode should trip effectively isolating the short from the output. Finally, when a capacitor fails as open circuit, no measures need to be taken. A second capacitor should be present to create redundancy. To comply with the RMS current rating two capacitors are required at the input and output, hence three input and output capacitors are used in total. In Appendix C, the schematics of the interleaved bidirectional and both buck converters including the redundancy measures are shown.

4.4 Comparison Redundancy Methods

The total footprint area of the single-phase converters and interleaved converters without redundancy are compared with the total footprint of the aforementioned redundancy methods. This is shown in Figure 4.6, together with the total number of components required. The components considered are those of the converter, including the switch, diode, inductor, output capacitor, input capacitor (if applicable), and fuses. Furthermore, the components for the gate driver are considered, including the bootstrap and startup circuit, as well as the isolated DC/DC converter for the buck-boost converter. Finally, the snubber network is considered, as well as the power multiplexer from Figure 4.3. The design of the interleaved converters, gate driver, and snubber network is covered in Chapter 5.

As expected, the number of components as well as the footprint area of the single-phase converters increase for N+1 and 2N redundancy. The number of components required for interleaved converters is almost twice as large as for single-phase converters without redundancy. However, the total resulting footprint area is approximately equal to that of the single-phase converters. This is due to the decrease

of inductance required for interleaved converters, resulting in significantly smaller inductors. Finally, the most number of components are required for interleaved converters including redundancy, however, the increase in footprint area is small compared to the interleaved converters without redundancy.

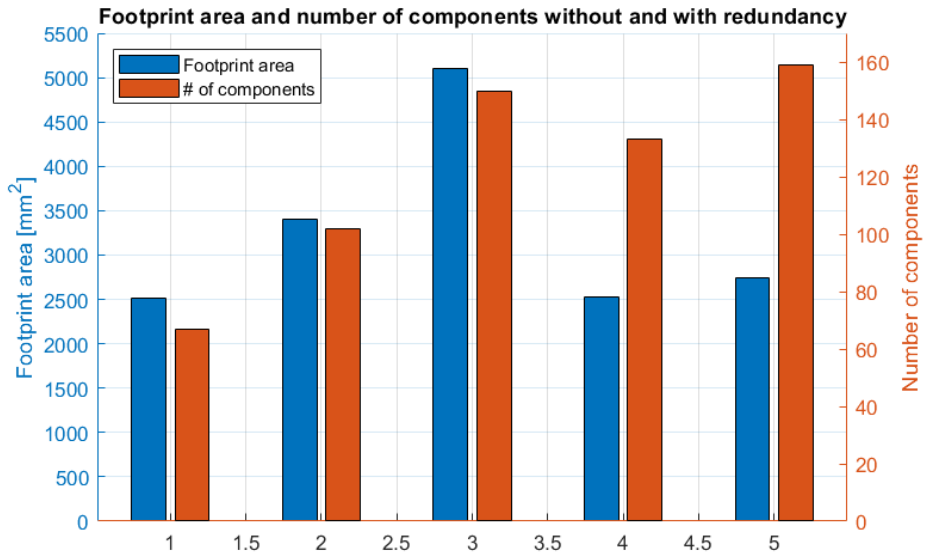


Figure 4.6: Comparison of the resulting total footprint and number of components of the single-phase converters without redundancy (1ph), N+1 redundancy, 2N redundancy, and interleaved converters without redundancy measures (int) and including redundancy measures (int+red).

It can be concluded that leg-level redundancy has the best tradeoff between redundancy added and footprint area added. Compared to the single-phase converters without redundancy (1ph), the interleaved converters including redundancy (int+red) increase the footprint area by 8.59%. For N+1 redundancy, an increase of 35.3% is observed, while for 2N redundancy, an increase of 103.3% is observed.

Compared to N+1 redundancy, leg-level redundancy has as advantage that redundancy for each converter is included instead of only one converter. Furthermore, the leg-level redundancy can account for a short or open circuit failure in the switch and diode, and an open circuit failure of both an output capacitor and input capacitor of each converter. For both N+1 and 2N redundancy, failure in only one of these components results in failure of the entire converter and the redundant converter should take over operation. Therefore, though no mathematical proof is given, it is expected that the leg-level redundancy results in the most amount of redundancy thus the highest reliability of the PES. Furthermore, the interleaved converters have improved efficiency and performance compared to the single-phase converters [87, 90].

Chapter 5

Power Electronic System Design Using Interleaved Converters

In this chapter, the designs of the two-phase interleaved DC/DC converters are presented. In Chapter 3 was found that a 12 V bus is more efficient than a 24 V bus for the single-phase converters. Therefore, the interleaved converters are designed for a 12 V bus voltage only. In addition, CCM operation was found to be more efficient than DCM operation. However, the interleaved converters are designed for both CCM and DCM. For two-phase interleaved converters the power is shared between the two channels. Therefore, the RMS currents are reduced significantly. Hence, the effect on the efficiency for both modes of operations is investigated to see if CCM is also more efficient than DCM for the interleaved converters.

First, in Section 5.1, the design of the interleaved converters in CCM and DCM is elaborated. Second, the specifications of the converters and resulting component values are presented in Section 5.2. Third, in Section 5.3, the models derived of the interleaved converters in CCM and DCM are verified using simulations in Matlab Simulink. Next, Section 5.4 compares the theoretical losses in the interleaved converters with those of the single-phase converters from Chapter 3. Section 5.5 presents the results of the loss calculations and compares them to the losses in the single-phase converters. Finally, Sections 5.6-5.8 cover implementation challenges, where the designs of the gate drivers, snubber networks, and startup circuit are presented, respectively.

5.1 Design Two-Phase Interleaved Converters

The design equations of the inductance and capacitances required are given for CCM and DCM. These are derived from the waveforms of the currents in the converters. In addition, the current waveforms are used to calculate the losses in each component in Chapter 5.4. To simplify the design, the following assumptions are made:

- The switches, diodes, inductors, and capacitors are ideal.
- The output and input capacitors are large enough to maintain a constant voltage.

5.1.1 Buck Converter CCM

For a two-phase interleaved buck converter, the inductance required for each phase is halved compared to that of a single-phase converter [109]. The inductance is calculated using (5.1).

$$L_{\text{CCM}} > \frac{D(V_{\text{in}} - V_{\text{o}})}{2I_{\text{o,min}}F_{\text{s}}N} \tag{5.1}$$

Here, V_{in} and V_{o} are the input and output voltages, respectively, $I_{\text{o,min}}$ the minimum output current to operate in CCM, F_{s} the switching frequency, and N the number of phases. Note that the phases operate at DCM at $I_{\text{o,min}}$, while the output phase current $i_{\text{ph,o}}$ is CCM. This holds when $D_{\text{DCM}} + \Delta_1 > 0.5$. The phases start operating in CCM when $I_{\text{o}} = 2I_{\text{o,min}}$. The duty cycle D is equal to the single-phase buck converter, given in (3.2).

The output capacitance required is calculated using the output phase current $i_{\text{ph,o}}(t)$, which is given by (5.2).

$$i_{\text{ph,o}}(t) = i_{\text{L,ph1}}(t) + i_{\text{L,ph2}}(t) \tag{5.2}$$

Here, $i_{\text{L,ph1}}$ and $i_{\text{L,ph2}}$ are the inductor phase currents. For both the 5 V and 3.3 V interleaved buck, $D < 0.5$. When D<0.5, $i_{\text{ph,o}}$ is described by (5.3).

$$i_{\text{ph,o}}(t) = \begin{cases} \frac{V_{\text{in}}-2V_{\text{o}}}{L}t + I_{\text{o}} - \frac{V_{\text{o}}T_{\text{s}}}{2L} + \frac{V_{\text{o}}DT_{\text{s}}}{L}, & \text{for } 0 \leq \text{t} < \text{D}T_{\text{s}} \\ -\frac{2V_{\text{o}}}{L}t + I_{\text{o}} + \frac{V_{\text{o}}T_{\text{s}}}{2L} + \frac{V_{\text{o}}DT_{\text{s}}}{L}, & \text{for D}T_{\text{s}} \leq \text{t} < \frac{T_{\text{s}}}{2} \end{cases} \tag{5.3}$$

The current in the output capacitor $i_{\text{Co}}(t)$ can be expressed by (5.4).

$$i_{\text{Co}}(t) = i_{\text{ph,o}}(t) - I_{\text{o}} \tag{5.4}$$

Here, I_{o} is the average output current. In Figure 5.1, the topology of the two-phase interleaved buck converter is shown, together with the aforementioned currents.

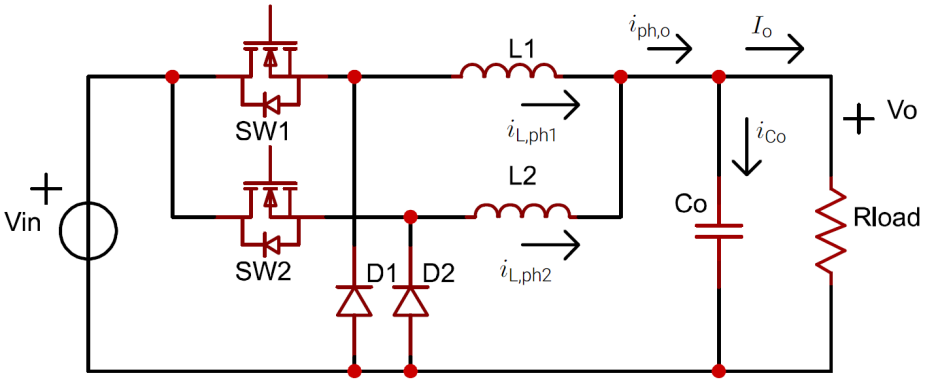


Figure 5.1: Currents used for the capacitance derivation of the two-phase interleaved buck converter.

Figure 5.2a shows the inductor phase currents, phase output current, and output capacitor current for the 5 V buck converter operating in CCM at maximum load (I_{o}=4 A). This is done for two switching cycles, using a switching frequency of 100 kHz. The inductor phase current ripple is $\Delta_{\text{L,ph1}}$=1.33 A, while the output phase current ripple is $\Delta I_{\text{L,pho}}$=0.38 A. Thus, the output current ripple is reduced by a factor 3.5. Furthermore, the frequency of the output phase current ripple is doubled compared to the inductor phase current ripple. Using (5.5), the output capacitance is calculated.

$$C_{\text{o}} = \frac{\Delta Q}{\Delta V_{\text{o}}} = \frac{1}{2\Delta V_{\text{o}}}(t_2 - t_1)i_{\text{Co,max}} \tag{5.5}$$

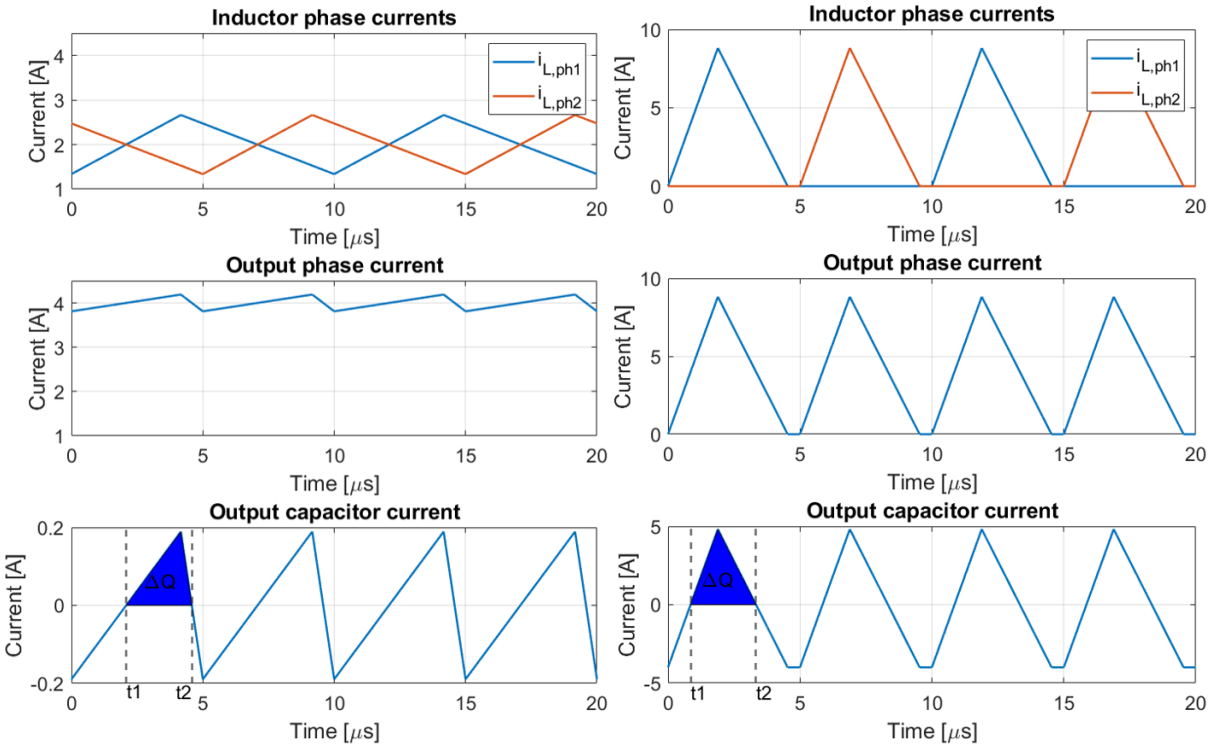
Here ΔQ is the change in charge stored in the capacitor and ΔV_{o} the corresponding change in voltage, $i_{\text{Co,max}}$ is the peak capacitor current, and t_1 and t_2 are found using (5.6) and solving for t.

$$i_{\text{ph,o}}(t) = 0 \tag{5.6}$$

In the plot of the output capacitor current in Figure 5.2a, the value of ΔQ, t_1, and t_2 are graphically shown. Solving for C_{o} using (5.3)-(5.6), the output capacitance is given by (5.7). The current ripple ΔI_{L} is calculated using (5.8).

$$C_{\text{o}} = \frac{1}{2\Delta V_{\text{o}}}\left(\frac{T_{\text{s}}}{2}\left(D + \frac{1}{2}\right) + \frac{V_{\text{o}}T_{\text{s}}}{V_{\text{in}} - 2V_{\text{o}}}(D - \frac{1}{2})\right)\left(\Delta I_{\text{L}} - \frac{V_{\text{o}}T_{\text{s}}}{2L}\right) \tag{5.7}$$

$$\Delta I_{\text{L}} = \frac{D(V_{\text{in}} - V_{\text{o}})}{LF_{\text{s}}} \tag{5.8}$$



(a) CCM operation. *(b) DCM operation.*

Figure 5.2: Waveforms of the currents in the interleaved 5 V buck converter corresponding to the output capacitance calculation, shown for two switching cycles.

5.1.2 Buck Converter DCM

The inductance to operate in DCM is shown in (5.9). Similar to the single-phase buck converter, the inductance should be evaluated at maximum load current to ensure DCM operation for the complete load current.

$$L_{\text{DCM}} < \frac{D(V_{\text{in}} - V_{\text{o}})}{2I_{\text{o,max}}F_{\text{s}}N} \tag{5.9}$$

The output phase current $i_{\text{ph,o}}$ becomes CCM for $I_{\text{o}} > I_{\text{o,max}}$. However, the individual phases remain in DCM until $I_{\text{o}} > 2I_{\text{o,max}}$. For the output capacitance, the same approach as for CCM is used. For both the 5 V and 3.3 V buck converter, $D + \Delta_1 \leq 0.5$, so $i_{\text{ph,o}}$ is described by (5.10).

$$i_{\text{ph,o}}(t) = \begin{cases} \frac{V_{\text{in}} - V_{\text{o}}}{L}t, & \text{for } 0 \leq \text{t} < D_{\text{DCM}}T_{\text{s}} \\ -\frac{V_{\text{o}}}{L}t + \Delta I_{\text{L}} + \frac{V_{\text{o}}}{L}D_{\text{DCM}}T_{\text{s}}, & \text{for } D_{\text{DCM}}T_{\text{s}} \leq \text{t} < (D_{\text{DCM}} + \Delta_1)T_{\text{s}} \\ 0, & \text{for } (D_{\text{DCM}} + \Delta_1)T_{\text{s}} \leq \text{t} < \frac{T_{\text{s}}}{2} \end{cases} \tag{5.10}$$

The DCM duty cycle D_{DCM} is calculated using (5.11). Because the power is divided by the number of phases N, the duty cycle is reduced by a factor $1/\sqrt{N}$ compared to a single-phase buck converter.

$$D_{\text{DCM}} = \sqrt{\frac{2LP_{\text{o}}}{V_{\text{in}}(V_{\text{in}} - V_{\text{o}})N}} \tag{5.11}$$

Further, the inductor current ripple ΔI_{L} is calculated using D_{DCM} in (5.8). Finally, Δ_1 is calculated using (5.12).

$$\Delta_1 = D_{\text{DCM}} \left(\frac{V_{\text{in}}}{V_{\text{o}}} - 1 \right) \tag{5.12}$$

The inductor phase currents $i_{\text{L,ph1}}$ and $i_{\text{L,ph2}}$, output phase current $i_{\text{ph,o}}$, and output capacitor current i_{Co} are shown in Figure 5.2b for the 5 V buck converter operating in DCM at maximum load. In this case, the output current phase current ripple is not reduced from the sum of the inductor phase currents. This happens when $D + \Delta_1 > 0.5$, which is not the case. The frequency of the ripple is again doubled.

The output capacitance required is calculated using (5.10) in (5.4)-(5.6). Further, ΔQ, t_1, and t_2 are graphically shown in the bottom plot of Figure 5.2b. The resulting equation of the output capacitance is given by (5.13). Note that this is the same equation as for the single-phase buck converter.

$$Co = \frac{\Delta I_{\text{L}} - I_{\text{o}}}{2\Delta V_{\text{o}}} \left(\frac{L(\Delta I_{\text{L}} - I_{\text{o}})}{V_{\text{o}}} + D_{\text{DCM}} T_{\text{s}} - \frac{L I_{\text{o}}}{V_{\text{in}} - V_{\text{o}}} \right) \tag{5.13}$$

5.1.3 Buck-Boost Converter CCM

The inductance that results in CCM is given by (5.14). Again, the inductance is divided by the number of phases N.

$$L_{\text{CCM}} > \frac{V_{\text{in}} D(1-D)}{2 I_{\text{o,min}} F_{\text{s}} N} \tag{5.14}$$

The duty cycle D of the buck-boost converter is equal to the single-phase duty cycle, given in (3.16). It was found in Section 3.2.5 that the maximum inductance is found when $V_{\text{in}} = V_{\text{o}}$. Similar to the buck converter, the phases operate in DCM at $I_{\text{o,min}}$. However, the output phase current becomes CCM when $\Delta_1 \geq 0.5$, so

$$I_{\text{o}} \geq \frac{N V_{\text{o}}}{8 L F_{\text{s}}}$$

For the output capacitance, the maximum value occurs at maximum load and input voltage, thus at MPP. For the interleaved buck-boost converter, the output capacitance is calculated from the output phase current, given by (5.15).

$$i_{\text{ph,o}}(t) = i_{\text{D,ph1}}(t) + i_{\text{D,ph2}}(t) \tag{5.15}$$

Here, $i_{\text{D,ph1}}$ and $i_{\text{D,ph2}}$ are the diode phase currents through $D1$ and $D2$, respectively. At MPP, $D \approx 0.44$. When $D < 0.5$, the output phase current is given by (5.16).

$$i_{\text{ph,o}}(t) = \begin{cases} -\frac{V_{\text{o}}}{L} t + \frac{V_{\text{o}} T_{\text{s}}}{L} (D - \frac{1}{2}) + \frac{I_{\text{o}}}{2(1-D)} + \frac{1}{2} \Delta I_{\text{L}}, & \text{for } 0 \leq \text{t} < \text{D} T_{\text{s}} \\ -\frac{2V_{\text{o}}}{L} t + \frac{V_{\text{o}} T_{\text{s}}}{L} (2D - \frac{1}{2}) + \frac{I_{\text{o}}}{1-D} + \Delta I_{\text{L}}, & \text{for D} T_{\text{s}} \leq \text{t} < \frac{T_{\text{s}}}{2} \end{cases} \tag{5.16}$$

The current ripple ΔI_{L} is calculated from (5.17).

$$\Delta I_{\text{L}} = \frac{V_{\text{in}} D}{L F_{\text{s}}} = \frac{V_{\text{o}}(1-D)}{L F_{\text{s}}} \tag{5.17}$$

Finally, the current in the output capacitor can be expressed by (5.18).

$$i_{\text{Co}}(t) = i_{\text{ph,o}}(t) - I_{\text{o}} \tag{5.18}$$

In Figure 5.3, the schematic of the interleaved buck-boost converter is shown, together with the aforementioned currents.

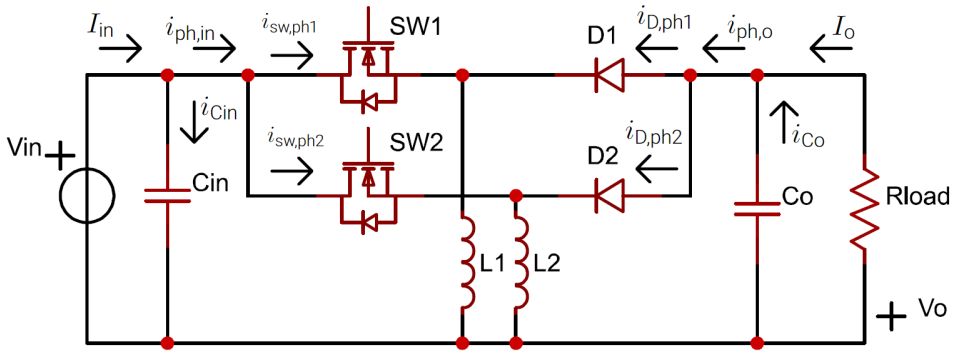


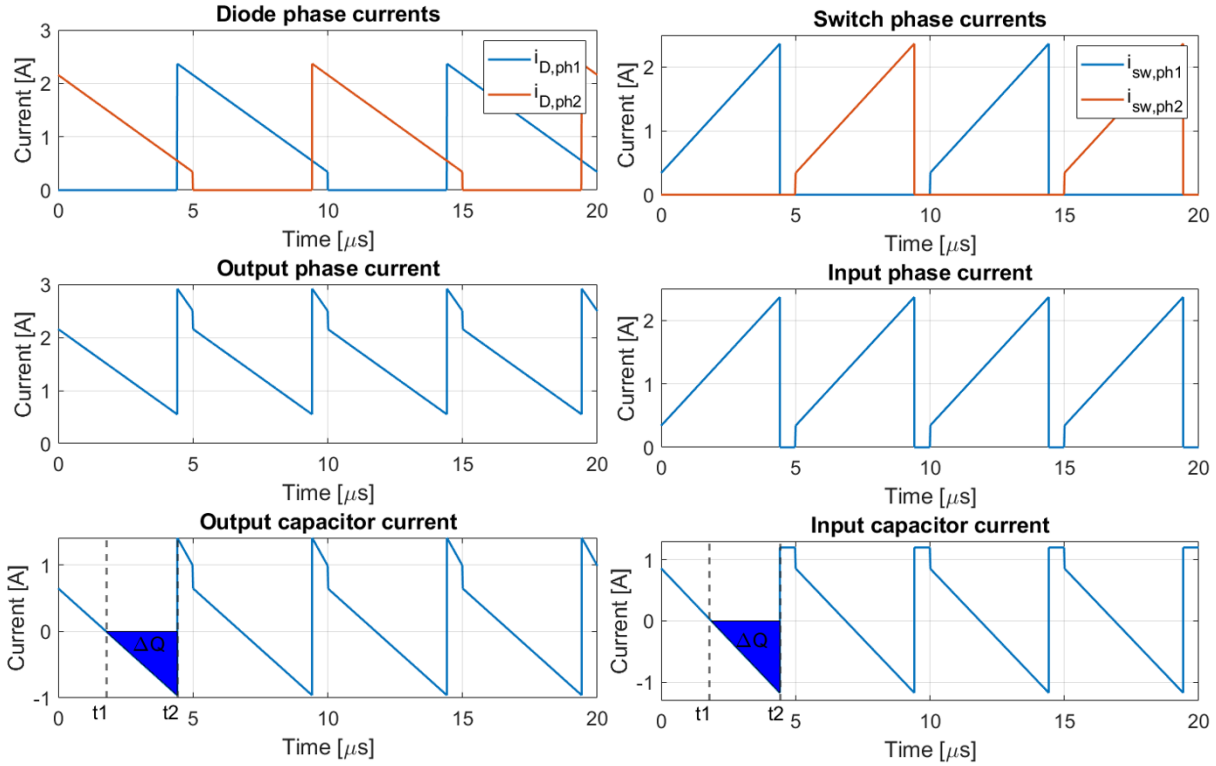
Figure 5.3: Currents used for the capacitance derivation of the two-phase interleaved buck-boost converter.

In Figure 5.4a, the diode phase currents $i_{D,ph1}$ and $i_{D,ph2}$, phase output current $i_{ph,o}$, and output capacitor current i_{Co} are shown for the interleaved buck-boost converter for two switching cycles. It operates at MPP at 100 kHz in CCM. Further, it shows the values of ΔQ, t_1, and t_2 in the bottom plot. Note that $t_2 = DT_s$. The value of the output capacitance is calculated using (5.19).

$$C_o = \frac{\Delta Q}{\Delta V_o} = \frac{1}{2\Delta V_o}(t_2 - t_1)|i_{Co,min}| \tag{5.19}$$

This results in (5.20).

$$Co = \frac{1}{2\Delta V_o}\left(\frac{Ts}{2} - \frac{LI_o}{2V_o(1-D)} - \frac{L\Delta I_L}{2V_o} + \frac{LI_o}{V_o}\right)\left|\frac{I_o}{2(1-D)} + \frac{\Delta I_L}{2} - \frac{V_o T_s}{2L} - I_o\right| \tag{5.20}$$



(a) Waveforms used for output capacitance calculations. *(b) Waveforms used for input capacitance calculations.*

Figure 5.4: Currents in the interleaved buck-boost converter in CCM shown for two switching cycles.

The input capacitance required is also calculated at MPP, using the input phase current shown in (5.21).

$$i_{\text{ph,in}}(t) = i_{\text{sw,ph1}}(t) + i_{\text{sw,ph2}}(t) \tag{5.21}$$

Here, $i_{\text{sw,ph1}}$ and $i_{\text{sw,ph2}}$ are the currents through the switches of phase 1 and 2, respectively. When D < 0.5, the input phase current is given by (5.22).

$$i_{\text{ph,in}}(t) = \begin{cases} \frac{V_{\text{in}}}{L}t + \frac{I_{\text{in}}+I_{\text{o}}}{2} - \frac{\Delta I_{\text{L}}}{2}, & \text{for } 0 \leq \text{t} < \text{D}T_{\text{s}} \\ 0, & \text{for D}T_{\text{s}} \leq \frac{T_{\text{s}}}{2} \end{cases} \tag{5.22}$$

Finally, the current in the input capacitor is given by (5.23).

$$i_{\text{Cin}}(t) = I_{\text{in}} - i_{\text{ph,in}}(t) \tag{5.23}$$

In Figure 5.4b, the switch phase currents $i_{\text{sw,ph1}}$ and $i_{\text{sw,ph2}}$, input phase current $i_{\text{ph,in}}$, and input capacitor current i_{Cin} are shown for two switching cycles. It operates at MPP at 100 kHz in CCM. When D < 0.5, the input phase current is DCM. Further, it shows the values of ΔQ, t_1, and t_2 graphically. Note that t_2 = DT_{s}. The value of the input capacitance is calculated using (5.24).

$$C_{\text{in}} = \frac{1}{2\Delta V_{\text{o}}}(t_2 - t_1)|i_{\text{Cin,min}}| \tag{5.24}$$

The resulting expression of the input capacitance is given in (5.25).

$$C_{\text{in}} = \frac{1}{2\Delta V_{\text{in}}}\left(DT_{\text{s}} - \frac{L}{2V_{\text{in}}}\left(I_{\text{in}} - I_{\text{o}} + \Delta I_{\text{L}}\right)\right)\left|\frac{I_{\text{in}} - I_{\text{o}} - \Delta I_{\text{L}}}{2}\right| \tag{5.25}$$

5.1.4 Buck-Boost Converter DCM

The inductance to operate in DCM is shown in (5.26). To always operate in DCM, the inductance should be evaluated at MPP.

$$L_{\text{DCM}} < \frac{V_{\text{in}}D(1-D)}{2I_{\text{o,max}}F_{\text{s}}N} \tag{5.26}$$

The expression of the output capacitance is the same as for the single-phase buck-boost converter in DCM, shown in (3.18). The reason is that the currents in the diodes of the two phases do not overlap, because $\Delta_1 < 0.5$. However, the duty cycle D_{DCM} is now calculated using (5.27). Just as for the interleaved buck converter, the duty cycle is reduced by a factor $1/\sqrt{N}$ compared to a single-phase buck-boost converter.

$$D_{\text{DCM}} = \sqrt{\frac{2V_{\text{o}}I_{\text{o}}L}{V_{\text{in}}^2 T_{\text{s}}N}} \tag{5.27}$$

The expression for the input capacitance required is derived in the same way as for the input capacitance in CCM. At MPP, $D < 0.5$ and the input phase current is described by (5.28).

$$i_{\text{ph,in}}(t) = \begin{cases} \frac{V_{\text{in}}}{L}t, & \text{for } 0 \leq \text{t} < D_{\text{DCM}}T_{\text{s}} \\ 0, & \text{for } D_{\text{DCM}}T_{\text{s}} \leq \text{t} < \frac{T_{\text{s}}}{2} \end{cases} \tag{5.28}$$

Thus, the waveforms look similar to the CCM case, shown in Figure 5.4b. The difference is that the switch phase currents start from 0 A. From (5.23) and (5.24), the input capacitance is expressed by (5.29)

$$C_{\text{in}} = \frac{1}{2\Delta V_{\text{in}}}\left(D_{\text{DCM}}T_{\text{s}} - \frac{LI_{\text{in}}}{V_{\text{in}}}\right)|I_{\text{in}} - \Delta I_{\text{L}}| \tag{5.29}$$

The current ripple ΔI_{L} is calculated from (5.17) using (5.27).

5.1.5 Bidirectional Converter CCM

Similar to the single-phase bidirectional converter, the design of the two-phase interleaved bidirectional converter is made for buck mode and maximum battery voltage. Therefore, the expression of the inductance that results in CCM is equal to that of the interleaved buck converter, given in (5.1).

The expression of output capacitance required differs from the interleaved buck converter because D > 0.5 for all battery voltages for the bidirectional converter. Now, $i_{\text{ph,o}}$ is described by (5.30).

$$i_{\text{ph,o}}(t) = \begin{cases} \frac{2(V_{\text{in}}-V_{\text{o}})}{L}t + I_{\text{o}} - \Delta I_{\text{L}} + \frac{(V_{\text{in}}-V_{\text{o}})T_{\text{s}}}{2L}, & \text{for } 0 \leq \text{t} < (\text{D-}\frac{1}{2})T_{\text{s}} \\ \frac{V_{\text{in}}-2V_{\text{o}}}{L}t + I_{\text{o}} - \Delta I_{\text{L}} + \frac{V_{\text{o}}T_{\text{s}}}{2L}, & \text{for } (\text{D-}\frac{1}{2})T_{\text{s}} \leq t < \frac{T_{\text{s}}}{2} \end{cases} \tag{5.30}$$

The current in the output capacitor is expressed the same as for the interleaved buck converter, given by (5.4). In Figure 5.5 the schematic of the interleaved bidirectional converter is shown, together with the currents required for the input and output capacitance derivation.

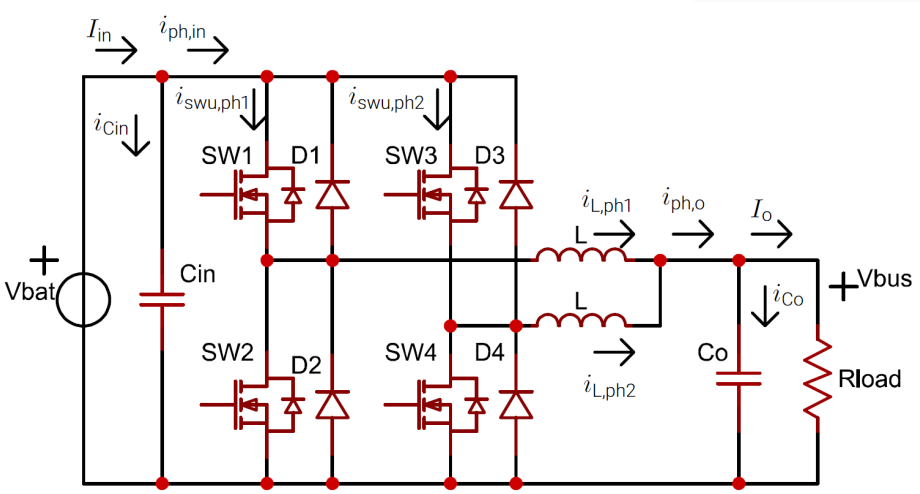


Figure 5.5: Currents used for the capacitance derivation of the two-phase interleaved bidirectional converter.

In Figure 5.6, the inductor phase currents $i_{\text{L,ph1}}$ and $i_{\text{L,ph2}}$, output phase current $i_{\text{ph,o}}$, and output capacitor current i_{Co} are shown for two switching cycles. The converter operates at maximum load (7.52 A), maximum battery voltage (21 V), and at 100 kHz in CCM. Further, it shows the values of ΔQ, t_1, and t_2. Similar to the interleaved buck converter, the output capacitance is calculated using (5.5). The resulting expression of the output capacitance is given in (5.31). The capacitance should be calculated at maximum load.

$$C_{\text{o}} = \frac{1}{2\Delta V_{\text{o}}}\left(\frac{\Delta I_{\text{L}}L - \frac{V_{\text{o}}T_{\text{s}}}{2}}{V_{\text{in}} - 2V_{\text{o}}} - \frac{\Delta I_{\text{L}}L}{2(V_{\text{in}} - V_{\text{o}})} - \frac{T_{\text{s}}}{4}\right)\left(\frac{V_{\text{in}} - 2V_{\text{o}}}{L}\left(D - \frac{1}{2}\right)T_{\text{s}} - \Delta I_{\text{L}} + \frac{V_{\text{o}}T_{\text{s}}}{2L}\right) \tag{5.31}$$

The input capacitance is calculated at maximum load from the input phase current, given by (5.32).

$$i_{\text{ph,in}}(t) = i_{\text{swu,ph1}}(t) + i_{\text{swu,ph2}}(t) \tag{5.32}$$

Here, $i_{\text{swu,ph1}}$ and $i_{\text{swu,ph2}}$ are the currents in the upper switch of phase 1 and 2, respectively. When $D > 0.5$, the input phase current is given by (5.33).

$$i_{\text{ph,in}}(t) = \begin{cases} \frac{2(V_{\text{in}}-V_{\text{o}})}{L}t + I_{\text{o}} - \Delta I_{\text{L}} + \frac{(V_{\text{in}}-V_{\text{o}})T_{\text{s}}}{2L}, & \text{for } 0 \leq \text{t} < (D - \frac{1}{2})T_{\text{s}} \\ \frac{(V_{\text{in}}-V_{\text{o}})}{L}t + \frac{I_{\text{o}}-\Delta I_{\text{L}}}{2}, & \text{for } (D - \frac{1}{2})T_{\text{s}} \leq \text{t} < \frac{T_{\text{s}}}{2} \end{cases} \tag{5.33}$$

Finally, the input capacitor current is given by (5.34).

$$i_{\text{Cin}}(t) = I_{\text{in}} - i_{\text{ph,in}}(t) \tag{5.34}$$

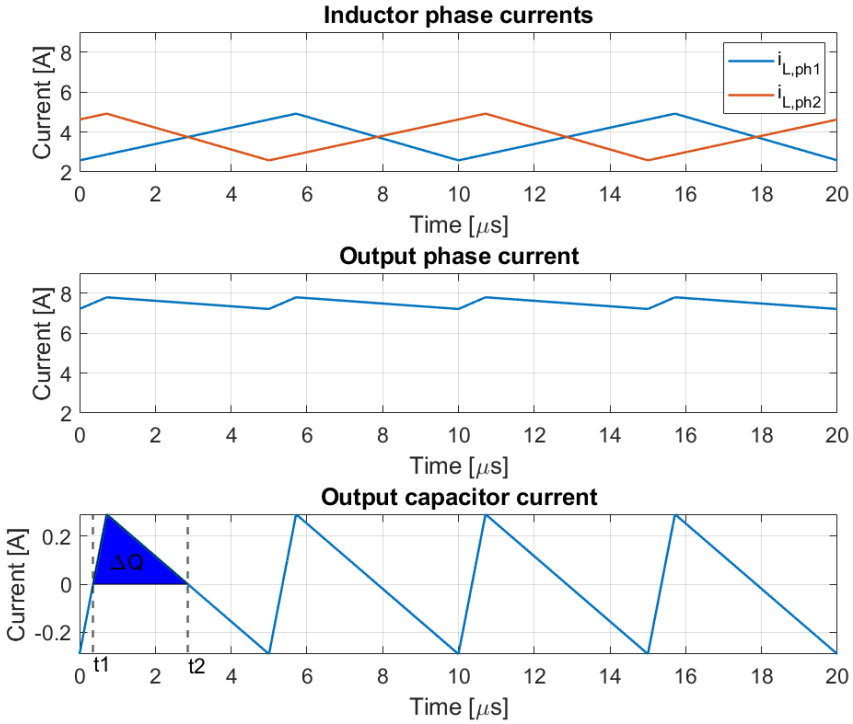


Figure 5.6: Waveforms of the currents in the bidirectional converter corresponding to the output capacitance calculations for CCM, shown for two switching cycles.

Figure 5.7a shows the upper switch phase currents $i_{\text{swu,ph1}}$ and $i_{\text{swu,ph2}}$, input phase current $i_{\text{ph,in}}$, and input capacitor current i_{Cin} for two switching cycles. Further, it shows the values of ΔQ, t_1, and t_2 in the bottom plot. The input capacitance is calculated using (5.24). This results in (5.35).

$$C_{\text{in}} = \frac{1}{2\Delta V_{\text{in}}} \left(\frac{L}{V_{\text{in}} - V_{\text{o}}} \left(I_{\text{in}} + \frac{\Delta I_{\text{L}} - I_{\text{o}}}{2} \right) - \left(D - \frac{1}{2} \right) T_{\text{s}} \right) \left(I_{\text{in}} - \frac{(V_{\text{in}} - V_{\text{o}})}{L} \left(D - \frac{1}{2} \right) T_{\text{s}} + \frac{\Delta I_{\text{L}} - I_{\text{o}}}{2} \right) \tag{5.35}$$

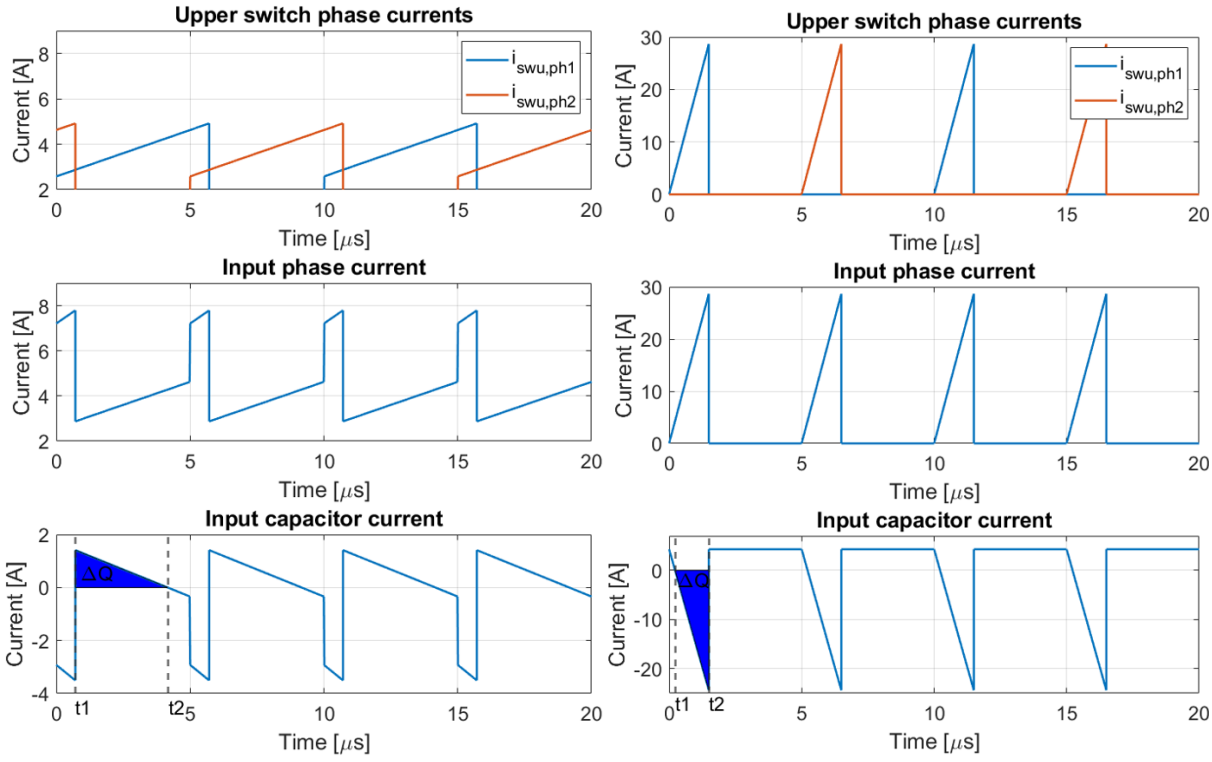
5.1.6 Bidirectional Converter DCM

The inductance that results in DCM is equal to the expression of the interleaved buck converter in DCM, given in (5.9). Further, because $D_{\text{DCM}} + \Delta_1 \leq 0.5$ for the complete operating region, the expression of the output capacitance is also equal to the interleaved buck converter in DCM, given in (5.13). The derivation of the input capacitance is equal to that of the interleaved buck-boost. The input phase current is given by (5.36).

$$i_{\text{ph,in}}(t) = \begin{cases} \frac{V_{\text{in}} - V_{\text{o}}}{L} t, & \text{for } 0 \leq t < D_{\text{DCM}} T_{\text{s}} \\ 0, & \text{for } D_{\text{DCM}} T_{\text{s}} \leq t < \frac{T_{\text{s}}}{2} \end{cases} \tag{5.36}$$

The duty cycle D_{DCM} is calculated using (5.11) from the interleaved buck converter. The input capacitor current is calculated from (5.23). The plot of the currents in the upper switch phases $i_{\text{swu,ph1}}$ and $i_{\text{swu,ph2}}$, the input phase current $i_{\text{ph,in}}$, and input capacitor i_{Cin} are shown in Figure 5.7b for two switching cycles. Finally, from (5.24), the input capacitance is calculated from (5.37).

$$C_{\text{in}} = \frac{1}{2\Delta V_{\text{in}}} \left(D_{\text{DCM}} T_{\text{s}} - \frac{I_{\text{in}} L}{V_{\text{in}} - V_{\text{o}}} \right) |I_{\text{in}} - \Delta I_{\text{L}}| \tag{5.37}$$



(a) CCM operation. *(b) DCM operation.*

Figure 5.7: Switch phase currents (top), input phase current (mid), and input capacitor current (bottom) of the interleaved bidirectional converter, operating in discharge (buck) mode at maximum load (7.5 A) with maximum battery voltage (21 V) at 100 kHz for two switching cycles.

5.2 Specifications and Component Values Interleaved Converters

The requirements of the interleaved converters are shown in Table 5.1. When a fault has occurred in one of the phases of an interleaved converter, it operates in single-phase mode. This results in a significant increase in the output voltage ripple. Therefore, the output capacitance is calculated from the single-phase mode using the inductance calculated from the interleaved mode. In this way, the output voltage ripple always is <1%. The calculation of the output capacitance required for interleaved converters is still useful for several reasons. First, the difference in output capacitance required for an interleaved converter and single-phase converter is shown. Second, the expected output voltage ripple during interleaved operation is calculated from the output capacitance equations. Finally, the losses in the capacitors during interleaved operation can be calculated using the model of the capacitor currents. The same holds for the input capacitance calculations.

Table 5.1: Specifications of the interleaved converters.

	Bidirectional	**Buck-boost**	**3.3V buck**	**5V buck**
$\mathbf{P_o}$ **[W]**	90.22	20.90	13.20	20
$\mathbf{V_{in}}$ **[V]**	13.5 to 21	0 to 16.14	12	12
$\mathbf{V_o}$ **[V]**	12	12	3.3	5
$\mathbf{I_{o,max}}$ **[A]**	7.52	1.74	4	4
$\mathbf{I_{o,min}}$ **[A]**	0.752	0.348	0.5	0.5
$\mathbf{\Delta V_o}$ **[V]**	0.12 (1%V_o)	0.12 (1%V_o)	0.033 (1%V_o)	0.05 (1%V_o)
$\mathbf{\Delta V_{in}}$ **[V]**	1.05 (5%V_{in})	0.76 (5%V_{in})	-	-

5.2.1 Interleaved Bidirectional Converter

The calculated and used values for the inductance, input capacitance, and output capacitance are shown in Table 5.2 for both CCM and DCM. For CCM, the worst-case conditions for the inductance and capacitors are at maximum battery voltage. This was found in Chapter 3.2. Two input capacitors are required to handle the current rating, and an additional capacitor is used as redundant capacitor. Note that a slightly larger inductance is used than is calculated for DCM. The reason is that the smaller inductors available at Vishay do not have a saturation current large enough to handle the current ripple. The inductance calculations are done at minimum battery voltage, while the capacitor calculations are done at maximum battery voltage. These are the worst-case operating conditions for DCM. In DCM, three input and output capacitors are required to handle the current rating, and an additional capacitor is used as redundant capacitor.

Table 5.2: Component values calculated and used for the interleaved bidirectional converter.

	CCM		**DCM**	
	Interleaved	**Single phase**	**Interleaved**	**Single phase**
L calc [μH]	17.10	34.20	0.443	0.887
L used [μH]	22		0.47	
Co calc [μF]	3.04	24.35	170.56	415.81
Co used [μF]	15		198	
Num Co used	2 + 1 redundant		3 + 1 redundant	
Total Co [μF]	45		792	
Cin calc [μF]	2.33	17.54	14.78	32.71
Cin used [μF]	22		28.2	
Num Cin used	2 + 1 redundant		3 + 1 redundant	
Total Cin [μF]	66		112.8	

5.2.2 Interleaved Buck-Boost Converter

Table 5.3 shows the calculated and used inductance and capacitance values. Note that though the calculated input capacitance required for CCM is smaller than for DCM, the actual capacitance used is larger. The reason is that from the available capacitors from Kyocera, a capacitor of 22 μF had the right current and voltage rating such that only one capacitor is required.

Table 5.3: Component values calculated and used for the interleaved buck-boost converter.

	CCM		**DCM**	
	Interleaved	**Single phase**	**Interleaved**	**Single phase**
L calc [μH]	31.33	62.66	6.18	12.32
L used [μH]	33		5.6	
Co calc [μF]	10.71	55.65	33.95	83.04
Co used [μF]	33		47	
Num Co used	2 + 1 redundant		2 + 1 redundant	
Total Co [μF]	99		141	
Cin calc [μF]	1.97	8.82	4.93	11.46
Cin used [μF]	22		10	
Num Cin used	1 + 1 redundant		1 + 1 redundant	
Total Cin [μF]	44		30	

5.2.3 Interleaved 5 V and 3.3 V Buck Converters

The calculated values and values used for the inductance and capacitance of the 5 V buck converter are shown in Table 5.4, while those of the 3.3 V buck converter in Table 5.5.

Table 5.4: Component values calculated and used for the interleaved 5 V buck converter.

	CCM		DCM	
	Interleaved	**Single phase**	**Interleaved**	**Single phase**
L calc [μH]	14.58	29.16	1.82	3.64
L used [μH]	22		1.5	
Co calc [μF]	4.73	33.14	119.44	369.14
Co used [μF]	22		220	
Num Co used	2 + 1 reduntant		2 + 1 reduntant	
Total Co [μF]	66		660	

Table 5.5: Component values calculated and used for the interleaved 3.3 V buck converter.

	CCM		DCM	
	Interleaved	**Single phase**	**Interleaved**	**Single phase**
L calc [μH]	11.96	23.92	1.50	3.00
L used [μH]	15		1.00	
Co calc [μF]	18.75	60.42	211.77	612.53
Co used [μF]	33		330	
Num Co used	2 + 1 reduntant		2 + 1 reduntant	
Total Co [μF]	99		990	

5.3 Verification of Calculations and Waveforms

The expected waveforms from Chapter 5.1 are verified using simulations in Simulink. The calculated RMS currents and voltage ripples are verified using these simulations as well. This is done for both interleaved and single-phase modes of operation. In the simulations, the redundant capacitors are included and the converters operate at maximum power. The simulation models are discussed in Appendix D.2.1.

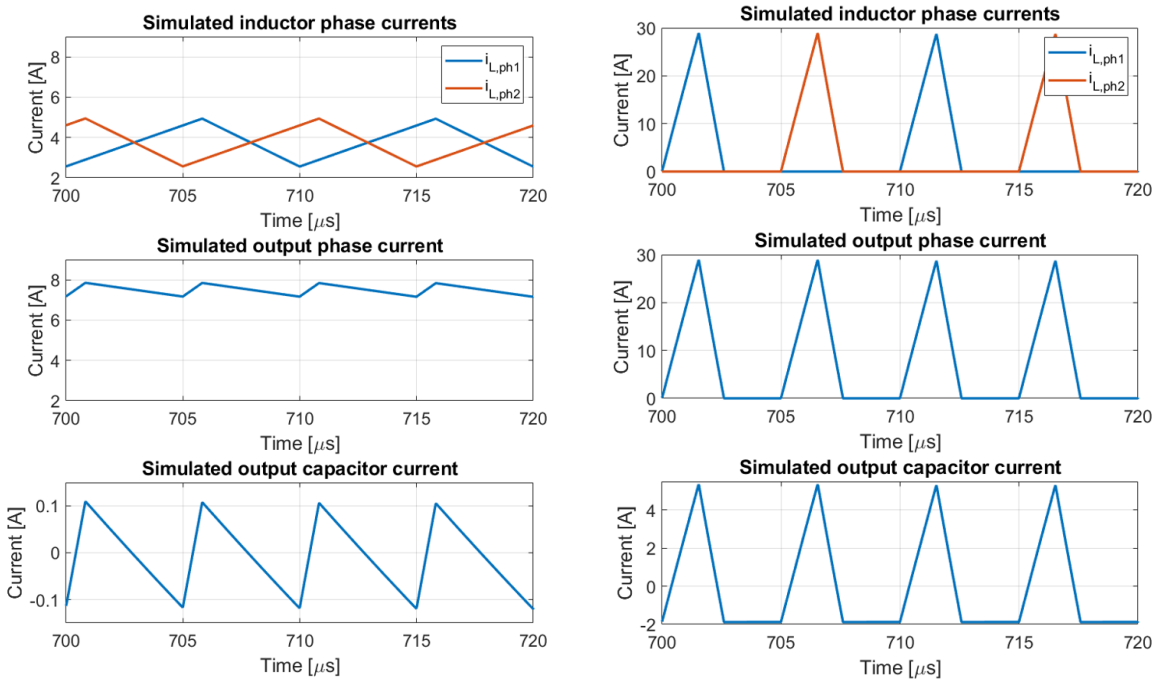
5.3.1 Interleaved Bidirectional Converter

Output Capacitance

The currents corresponding to the output capacitance calculations in CCM are shown in Figure 5.8a. The CCM simulated waveforms look similar to the expected waveforms from Figure 5.6. The only difference that can be observed is that the peak of the output capacitor current is reduced by approximately a factor of three. This is expected because three output capacitors are used in the simulation while only one output capacitor is used in the expected waveform. The simulated waveforms for DCM are shown in Figure 5.8b. For DCM was expected that the waveforms would look like the buck converter in DCM, shown in Figure 5.2b. Comparing these waveforms with the simulated waveforms, it can be confirmed that the bidirectional converter in DCM has the same waveform as the buck converter in DCM. The differences are the amplitudes, as well as the value of D and Δ_1. Thus, for $D + \Delta_1 \leq 0.5$, the model for the output capacitance of the 5 V buck converter and bidirectional converter in DCM are equal. Thus, it can be concluded that the models derived for the output phase current and output capacitance required are correct for CCM and DCM.

Input Capacitance

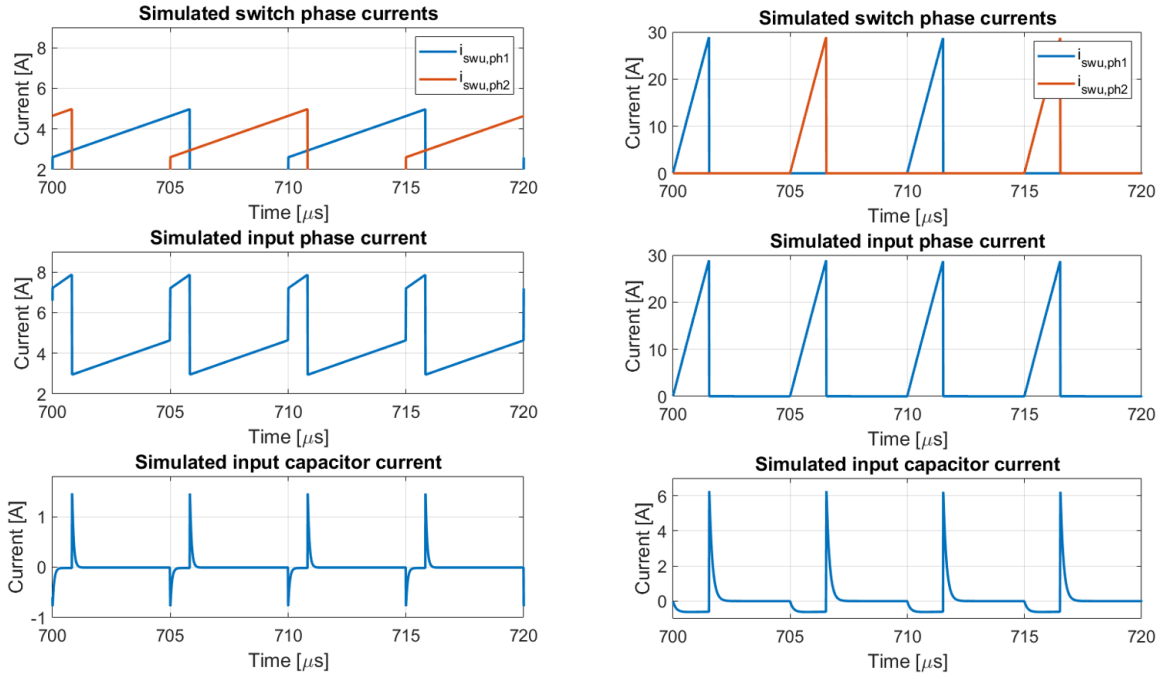
The simulated switch phase and input phase current corresponding to the input capacitance calculation, shown in Figure 5.9, match the expected waveforms of CCM from Figure 5.7a and DCM from Figure 5.7b. However, the simulated input capacitor current differs from the expected waveforms for both CCM and DCM. In the derivations was assumed that the input capacitance is large enough to maintain a constant voltage, resulting in an input current $i_{\text{Cin}} = I_{\text{in}} - i_{\text{ph,in}}$ for CCM and constant $i_{\text{Cin}} = I_{\text{in}}$ for DCM when $DT_{\text{s}} \leq t < T_{\text{s}}/2$. However, in the simulation i_{Cin} = 0 A in less than 1 μs indicating that the capacitors are completely charged after this time. Thus, the assumption that the input current is constant due to the input capacitance being large enough is incorrect. It is shown that the simulated waveforms match the expected waveforms when the input capacitance is increased by a factor of 100. This is shown in Figure



(a) CCM operation. *(b) DCM operation.*

Figure 5.8: Simulated inductor phase currents (top), output phase current (mid), and output capacitor currents (bottom) of the interleaved bidirectional converter.

5.10, which provides the simulation using the increased C_{in}. Comparing these with the expected waveforms in Figures 5.7a and 5.7b, there are only minor differences. The simulated waveforms exhibit some charge and discharge behaviour, while the expected waveforms do not have this property. Additionally, the magnitude of the input capacitor currents is reduced by a factor of 4 since there are four input capacitors in the simulation while only one is in the derivation.



(a) CCM operation. *(b) DCM operation.*

Figure 5.9: Simulated switch phase currents (top), input phase current (mid), and input capacitor currents (bottom) of the interleaved bidirectional converter.

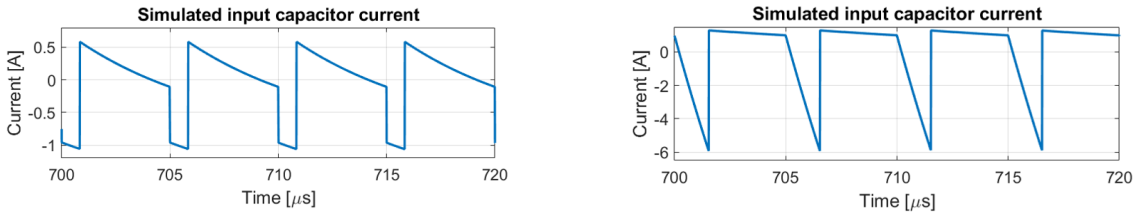


Figure 5.10: Simulation of the input capacitor currents of the interleaved bidirectional converter with a 100x increase of input capacitance for CCM (left) and DCM (right).

Currents and Ripples

The calculated and simulated currents and ripples in the inductor, switch, diode, output capacitor, and input capacitor are shown in Table 5.6. This is shown for CCM and DCM, both for operating in interleaved mode and single-phase mode. Note that the converter is operated in non-synchronous operation. For both CCM and DCM, the RMS currents in all components, the output voltage ripple, and the input voltage ripple are smaller for interleaved operation. This confirms the advantage of interleaving in terms of current sharing and ripple reduction.

Table 5.6: Comparison of the calculated and simulated currents and ripples in the inductor, switch, diode, and input and output capacitor of the interleaved bidirectional converter operating in CCM and DCM.

	CCM				DCM			
	Interleaved		Single phase		Interleaved		Single phase	
	Calc	Sim	Calc	Sim	Calc	Sim	Calc	Sim
D	0.571	0.583	0.571	0.586	0.150	0.154	0.212	0.219
ΔI_L [A]	2.34	2.37	2.34	2.37	28.68	28.87	40.56	40.84
$I_{L,max}$ [A]	4.93	4.96	8.69	8.72	28.68	28.87	40.56	40.84
$I_{L,rms}$ [A]	3.82	3.82	7.55	7.55	8.48	8.51	14.26	14.32
$I_{sw,rms}$ [A]	2.89	2.94	5.71	5.81	6.41	6.60	10.78	11.17
$I_{D,rms}$ [A]	2.50	2.45	4.94	4.84	5.55	5.38	9.33	8.97
$I_{D,av}$ [A]	1.61	1.54	3.22	3.09	1.61	1.51	3.22	2.97
$I_{Co,rms}$ [A]	0.056	0.066	0.225	0.229	2.34	2.35	3.03	3.05
ΔV_o	0.068%	0.095%	0.54%	0.54%	0.22%	0.22%	0.53%	0.53%
$I_{Cin,rms}$ [A]	0.466	0.150	1.25	0.205	2.00	0.82	2.47	0.83
ΔV_{in}	0.176%	0.023%	1.33%	0.041%	0.656%	0.13%	1.45%	0.18%

In general, the calculated RMS and average diode current is slightly larger than the simulated value. On the other hand, the calculated RMS switch current is slightly lower than the simulated value. This difference between the calculation and simulation is due to the non-zero switch on-resistance, and non-zero diode on-resistance and forward forward drop that are simulated. In the calculations, they were assumed to be zero. Due to the losses created by these non-ideal components, the duty cycle is slightly larger in the simulation. Thus, the switch conducts longer in the simulation, increasing the RMS current in the switch. The diode conducts shorter, thus reducing the average and RMS current in the diode. Additionally, the simulated inductor current ripple and the maximum inductor current are slightly larger than calculated. Again, this is caused by the slightly increased duty cycle. Therefore, it can be concluded that the calculations of the RMS currents in the switch, diode, and inductor are correct.

Further, the difference between the calculated and simulated output voltage ripples is very small. Thus, the model of the output phase current is correct, as well as the output capacitance calculation. However, the difference between the calculated and simulated input capacitor current and input voltage ripple is significant. It was already shown that the assumption that the input capacitance is large enough to maintain a constant voltage is incorrect by comparing the expected waveforms with the simulated waveforms. This can also be confirmed from the calculated and simulated $I_{\text{Cin,rms}}$ and ΔV_{in} when C_{in} is increased by 100, shown in Table 5.7. In general, the simulated input capacitor RMS current and input voltage ripple is slightly larger than calculated. Thus, it can be concluded that the model for the input phase current is correct and, for C_{in} large enough, the calculation of the input voltage ripple is correct as well.

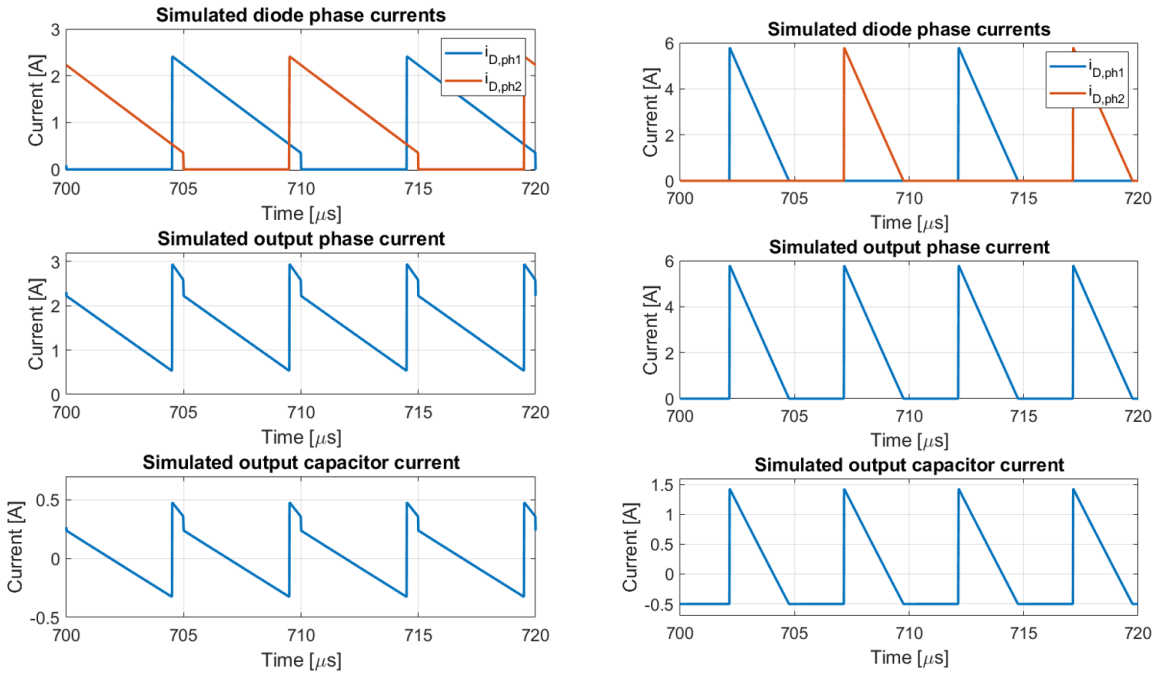
Table 5.7: Input capacitor RMS current and input voltage ripple when C_{in} is increased by 100.

	CCM				DCM			
	Interleaved		Single phase		Interleaved		Single phase	
	Calc	Sim	Calc	Sim	Calc	Sim	Calc	Sim
$I_{Cin,rms}$ [A]	0.466	0.488	1.22	1.25	2.00	2.04	2.47	2.52
ΔV_{in}	0.0018%	0.0019%	0.0133%	0.0128%	0.0066%	0.0068%	0.0145%	0.0155%

5.3.2 Interleaved Buck-boost

Output Capacitance

The simulated waveforms of the interleaved buck-boost converter that correspond to the output capacitance calculation are shown in Figure 5.11. The expected waveforms for CCM, shown in Figure 5.4a, are similar to the simulated waveforms in Figure 5.11a. Again, since three output capacitors are used in the simulation, the simulated output capacitor current is reduced by three compared to the expected waveform. For DCM was expected that the diode currents would not overlap and look like those in CCM, but starting from 0 A. This can be confirmed by the simulated waveform from Figure 5.11b. Therefore, the calculation of the output capacitance required in DCM is equal to the single-phase buck-boost converter.



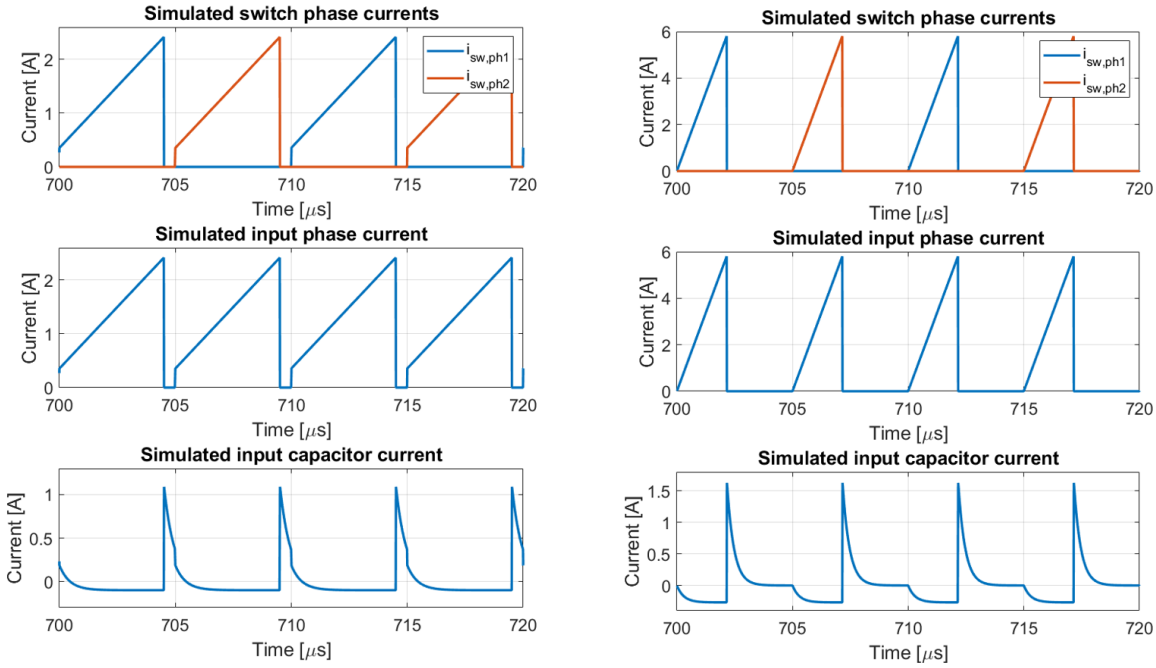
(a) CCM operation.

(b) DCM operation.

Figure 5.11: Simulated diode phase currents (top), output phase current (mid), and output capacitor currents (bottom) of the interleaved buck-boost converter operating at MPP.

Input Capacitance

The simulated waveforms corresponding to the input capacitance calculation are shown in Figure 5.12. Similar observations as for the bidirectional are made. The switch phase currents and input phase currents do match with the expected waveforms. The input capacitor current shows strong charge and discharge behaviour. Therefore, the calculated input capacitor RMS current input voltage ripple is larger than the simulated value. When the input capacitance is increased by 100, the simulated waveforms do match the expected waveforms. This is shown in Figure 5.13.



(a) CCM operation. *(b) DCM operation.*

Figure 5.12: Simulated switch phase currents (top), input phase current (mid), and input capacitor currents (bottom) of the interleaved buck-boost converter operating at MPP.

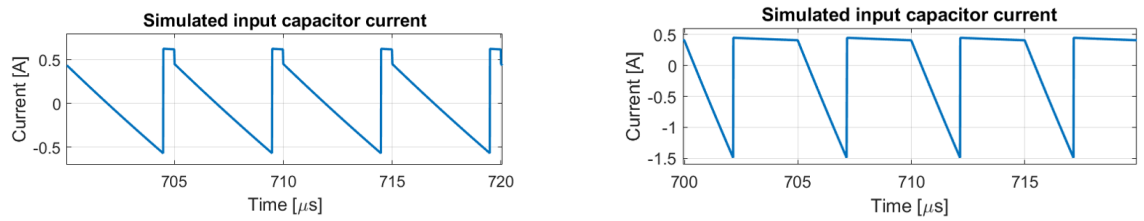


Figure 5.13: Simulated input capacitor currents of the interleaved buck-boost converter, operating at MPP in CCM (left) and DCM (right) with a 100x increase of input capacitance.

Currents and Ripples

The calculated and simulated currents and ripples in the inductor, switch, diode, output capacitor, and input capacitor are shown in Table 5.8. This is shown for CCM and DCM, both for operating in interleaved mode and single-phase mode. Similar observations as for the interleaved bidirectional converter are made. The RMS currents are smaller for the interleaved operation, as well as the output and input voltage ripples. The duty cycle in the simulation is slightly larger due to the non-ideal components. Thus, the simulated currents in the inductor and switch are slightly larger than calculated. However, for the buck-boost converter, the RMS diode current is also slightly larger. Thus, it can be concluded that the calculations of the RMS currents in the switch, diode, and inductor are correct.

The simulated output capacitor RMS current and output voltage ripple is slightly larger than calculated due to the increased duty cycle. Therefore, it can be concluded that the model of the output phase current is correct, as well as the calculation of the output capacitance. However, similar to the bidirectional converter, the calculated input capacitor RMS current and input voltage ripple are larger than the simulated values. When the input capacitor is increased by 100, the calculations and simulations do match. This is shown in Table 5.9. Thus, it can be concluded that the input phase current model is correct and that for large C_{in} the calculation of the input voltage ripple is correct as well.

Table 5.8: Comparison of the calculated and simulated currents and ripples in the inductor, switch, diode, and output capacitor of the interleaved buck-boost converter operating in CCM and DCM.

	CCM				DCM			
	Interleaved		Single phase		Interleaved		Single phase	
	Calc	Sim	Calc	Sim	Calc	Sim	Calc	Sim
D	0.442	0.451	0.442	0.452	0.210	0.261	0.298	0.307
ΔI_L **[A]**	2.03	2.07	2.03	2.07	5.69	5.83	8.05	8.23
$I_{L,max}$ **[A]**	2.37	2.45	3.72	3.87	5.69	5.83	8.05	8.23
$I_{L,rms}$ **[A]**	1.47	1.53	2.77	2.84	2.27	2.33	3.81	3.93
$I_{sw,rms}$ **[A]**	0.98	1.05	1.82	1.93	1.51	1.58	2.53	2.66
$I_{D,rms}$ **[A]**	1.10	1.13	2.07	2.10	1.69	1.72	2.85	2.90
$I_{D,av}$ **[A]**	0.76	0.76	1.51	1.51	0.76	0.76	1.51	1.52
$I_{Co,rms}$ **[A]**	0.205	0.211	0.471	0.489	0.619	0.640	0.804	0.824
ΔV_o	0.061%	0.111%	0.562%	0.604%	0.241%	0.250%	0.589%	0.600%
$I_{Cin,rms}$ **[A]**	0.350	0.240	0.700	0.313	0.588	0.332	0.744	0.336
ΔV_{in}	0.22%	0.110%	1.00%	0.24%	0.822%	0.334%	1.851%	0.492%

Table 5.9: Calculated and simulated input capacitor RMS current and input voltage ripple of the interleaved buck-boost converter when C_{in} is increased by 100.

	CCM				DCM			
	Interleaved		Single phase		Interleaved		Single phase	
	Calc	Sim	Calc	Sim	Calc	Sim	Calc	Sim
$I_{Cin,rms}$ **[A]**	0.350	0.349	0.700	0.716	0.588	0.606	0.744	0.777
ΔV_{in}	0.0022%	0.0024%	0.0100%	0.0104%	0.0082%	0.0085%	0.0185%	0.0202%

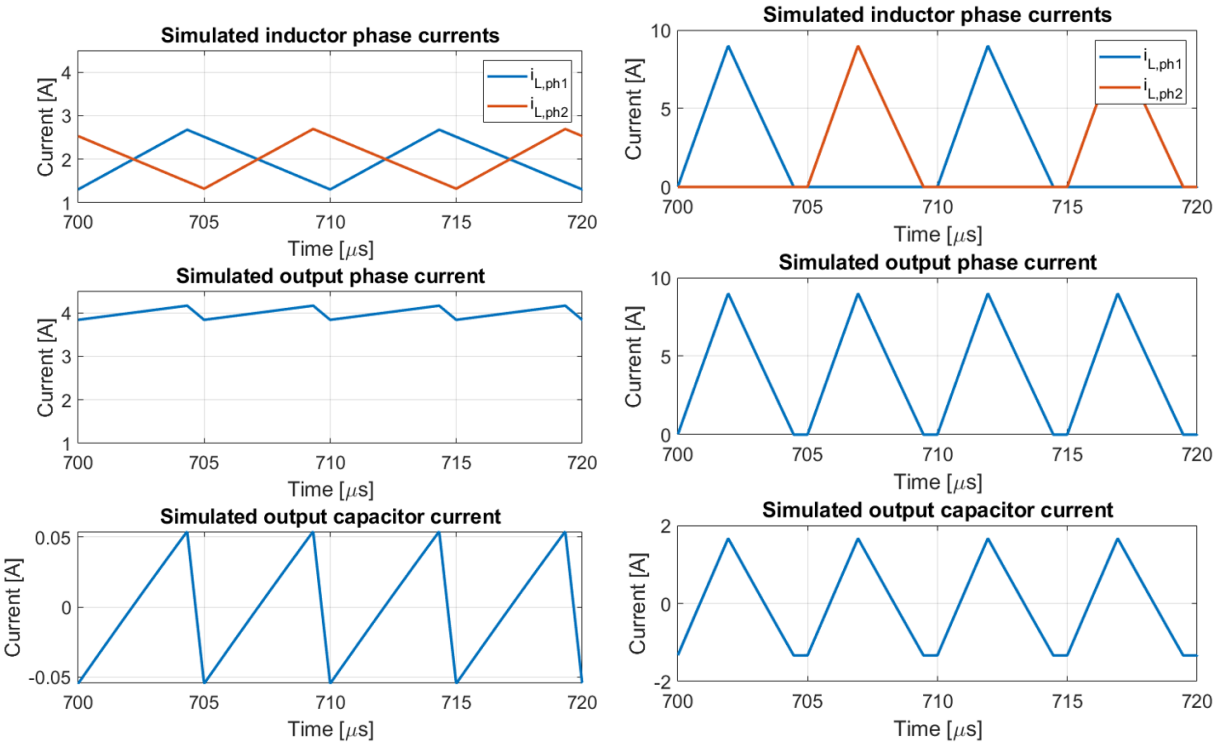
5.3.3 Interleaved 5 V Buck Converter

Output Capacitance

The simulated waveforms of the interleaved 5 V buck converter operating in CCM are shown in 5.14a, and for DCM in Figure 5.14b. They are shown for two switching cycles. The only difference that can be observed from the expected waveforms from Figures 5.2a and 5.2b is that the amplitude of the output capacitor current is reduced by a factor three. Again, three capacitors are used in the simulation while only one in the derivation. Therefore, it can be concluded that the model derived of the output phase current and capacitance required is correct.

Current and Ripples

The calculated and simulated currents and ripples in the inductor, switch, diode, and output capacitor are shown in Table 5.10. This is shown for both CCM and DCM. Similar observations for the interleaved bidirectional and buck-boost converters are made. The RMS currents are smaller for the interleaved operation, as well as the output voltage ripple. The duty cycle in the simulation is slightly larger due to the non-ideal components. Thus, the simulated currents in the inductor and switch are slightly larger than calculated, while the simulated currents in the diode are slightly smaller than calculated. Finally, the difference in output voltage ripple is really small. This confirms that the output capacitance calculation is correct.



(a) CCM operation. *(b) DCM operation.*

Figure 5.14: Simulated inductor phase currents (top), output phase current (mid), and output capacitor currents (bottom) of the 5 V interleaved buck converter.

Table 5.10: Comparison of the calculated and simulated currents and ripples in the inductor, switch, diode, and output capacitor of the 5 V interleaved buck converter operating in CCM and DCM.

	CCM				DCM			
	Interleaved		Single phase		Interleaved		Single phase	
	Calc	Sim	Calc	Sim	Calc	Sim	Calc	Sim
D	0.417	0.432	0.417	0.432	0.189	0.193	0.267	0.274
ΔI_L [A]	1.33	1.37	1.33	1.37	8.82	8.94	12.47	12.71
$I_{L,max}$ [A]	2.66	2.68	4.66	4.72	8.82	8.94	12.47	12.71
$I_{L,rms}$ [A]	2.04	2.05	4.02	4.03	3.43	3.46	5.77	5.82
$I_{sw,rms}$ [A]	1.31	1.35	2.59	2.66	2.21	2.29	3.72	3.87
$I_{D,rms}$ [A]	1.56	1.54	3.07	3.02	2.62	2.59	4.41	4.36
$I_{D,av}$ [A]	1.17	1.13	2.33	2.25	1.17	1.12	2.33	2.24
$I_{Co,rms}$ [mA]	36.5	31.4	127.6	132.5	914.0	939.9	1384	1411
ΔV_o	0.072%	0.062%	0.50%	0.53%	0.18%	0.19%	0.56%	0.57%

5.3.4 Interleaved 3.3 V Buck Converter

The current waveforms of the inductor phase currents, output phase current, and output capacitor current are similar to the 5 V buck converter. Hence, only the calculated and simulated currents and ripples are compared. This is shown in Table 5.11 for operating in CCM and DCM, and for interleaved and single-phase modes of operation. Similar observations as for the interleaved 5 V buck converter are made. The simulated duty cycle is slightly larger than calculated due to simulating non-ideal components. This, in turn, increases the simulated inductor and switch currents slightly, while reducing the simulated diode currents slightly. Additionally, this increases the simulated voltage ripples slightly as well compared to the calculations. Thus, it can be concluded that the models of the interleaved and single-phase 3.3 V buck converter is correct and equal to those of the 5 V buck converter.

Table 5.11: Comparison of the calculated and simulated currents and ripples in the inductor, switch, diode, and output capacitor of the 3.3 V interleaved buck converter operating in CCM and DCM.

	CCM				DCM			
	Interleaved		Single phase		Interleaved		Single phase	
	Calc	Sim	Calc	Sim	Calc	Sim	Calc	Sim
D	0.275	0.294	0.275	0.296	0.112	0.117	0.159	0.167
$\mathbf{\Delta I_L}$ **[A]**	1.60	1.70	1.60	1.71	9.78	10.15	13.83	14.42
$\mathbf{I_{L,max}}$ **[A]**	2.80	2.87	4.80	4.86	9.78	10.15	13.83	14.42
$\mathbf{I_{L,rms}}$ **[A]**	2.05	2.06	4.03	4.03	3.61	3.68	6.07	6.19
$\mathbf{I_{sw,rms}}$ **[A]**	1.08	1.13	2.11	2.20	1.89	2.02	3.19	3.42
$\mathbf{I_{D,rms}}$ **[A]**	1.75	1.73	3.43	3.38	3.08	3.08	5.17	5.16
$\mathbf{I_{D,av}}$ **[A]**	1.45	1.41	2.90	2.81	1.45	1.40	2.90	2.79
$\mathbf{I_{Co,rms}}$ **[A]**	0.0953	0.0960	0.154	0.165	1.06	1.11	1.52	1.58
$\mathbf{\Delta V_o}$	0.19%	0.22%	0.61%	0.66%	0.21%	0.23%	0.62%	0.64%

5.4 Losses Interleaved Converters

The losses in the switch, diode, inductor, and output capacitor are considered, similar to the single-phase converters. The losses in the input capacitor losses of the bidirectional and buck-boost converter are not considered to have a fair comparison between the losses in the single-phase and interleaved converters. In general, due to current sharing, the current in the switch, diode, and inductor of a phase of an N-phase interleaved converter is reduced by a factor N compared to a single-phase converter. This is shown in (5.38).

$$I_{\text{x,int}} = \frac{I_{\text{x,1ph}}}{N} \tag{5.38}$$

The subscript x denotes the component (inductor, switch, or diode), the subscript int that it corresponds to a phase of the interleaved converter, and the subscript $1ph$ that it corresponds to a single-phase converter. The equations of the RMS currents for the single-phase converters were shown in Tables 3.3 and 3.4. In the analysis, the following assumptions are made:

- The current is shared equally among the phases of the interleaved converter.
- The same components are used for the interleaved and single-phase converters.

5.4.1 Losses in the switch

The conduction losses in the switch of an N-phase interleaved converter are reduced by N, shown in (5.39).

$$P_{\text{sw,cl,int}} = \left(\frac{I_{\text{sw,1ph,rms}}}{N}\right)^2 R_{\text{DS}} N = \frac{P_{\text{sw,cl,1ph}}}{N} \tag{5.39}$$

Here, $I_{\text{sw,int,rms}}$ is the RMS current in the switch of a phase of the interleaved converter, $I_{\text{sw,1ph,rms}}$ the RMS current in the switch of a single-phase converter, R_{DS} the drain-source on-resistance.

The total switching losses of the switches in the interleaved converter are not reduced compared to a single-phase converter. This is shown in (5.40).

$$P_{\text{sw,fs,int}} = \frac{1}{2} V_{\text{sw,off}} \left(\frac{I_{\text{sw,on,1ph}}}{N} t_{\text{on}} + \frac{I_{\text{sw,off,1ph}}}{N} t_{\text{off}}\right) F_{\text{s}} N = P_{\text{sw,fs,1ph}} \tag{5.40}$$

Here, F_{s} is the switching frequency, $V_{\text{sw,off}}$ is the voltage the switch blocks when turned off, t_{on} and t_{off} are the turn-on and turn-off time of the switch, and $I_{\text{sw,on,1ph}}$ and $I_{\text{sw,off,1ph}}$ the current that the switch of a single-phase converter must switch when turned on and off.

5.4.2 Losses in the diode

The total conduction losses of the diodes in the interleaved converter are reduced compared to a single-phase converter, but not by a factor N. The reason is the losses due to the forward voltage drop of the diode are not reduced by N. This is shown in (5.41).

$$P_{\text{D,cl,int}} = \left(V_{\text{f}} \frac{I_{\text{D,av,1ph}}}{N} + \left(\frac{I_{\text{D,rms,1ph}}}{N} \right)^2 R_{\text{D,on}} \right) N = V_{\text{f}} I_{\text{D,av,1ph}} + \frac{I^2_{\text{D,rms,1ph}}}{N} R_{\text{D,on}} \tag{5.41}$$

Here, V_{f} is the forward voltage drop of the diode, $I_{\text{D,av,1ph}}$ the average diode current of the single-phase converter, $I_{\text{D,rms,1ph}}$ the RMS diode current of the single-phase converter, and $R_{\text{D,on}}$ the on-resistance of the diode. Compared to a single-phase converter, the total switching losses in the diodes of the interleaved converter are increased by a factor N, shown in (5.42). Here, C_{j} is the junction capacitance, V_{R} the reverse voltage blocked, and F_{s} the switching frequency.

$$P_{\text{D,fs,int}} = \frac{1}{2} C_{\text{j}} V_{\text{R}}^2 F_{\text{s}} N = P_{\text{D,fs,1ph}} N \tag{5.42}$$

5.4.3 Losses in the inductor

The total DC conduction losses in the inductors of an interleaved converter are calculated using (5.43). Here, $I_{\text{L,rms}}$ is the RMS inductor current, and R_{DC} the DC resistance of the inductor. Thus, the total conduction losses of the inductors are reduced by a factor N compared to a single-phase converter.

$$P_{\text{L,DC,int}} = \left(\frac{I_{\text{L,rms,1ph}}}{N} \right)^2 R_{\text{DC}} N = \frac{P_{\text{L,DC,int}}}{N} \tag{5.43}$$

Similar as for the single-phase converters, the core losses in CCM are evaluated using the core loss calculator provided by Vishay, and for DCM by using this tool to obtain the Steinmetz coefficients [97]. The total core loss for an interleaved converter is shown in (5.44), which shows the generalised Steinmetz equation.

$$P_{\text{v,int}} = V_{\text{e}} \frac{k_{\text{i}} \left(\Delta B \right)^{\beta - \alpha}}{T_{\text{s}}} \cdot \left(\left| \frac{\Delta B}{D T_{\text{s}}} \right|^{\alpha} D T_{\text{s}} + \left| \frac{\Delta B}{(1-D)\, T_{\text{s}}} \right|^{\alpha} (1 - \text{D})\, T_{\text{s}} \right) N \tag{5.44}$$

In CCM, the duty cycle is the same for an interleaved converter and a single-phase converter. Thus, for the same inductor, $\Delta I_{\text{L,int}} = \Delta I_{\text{L,1ph}}$. Therefore, the total core losses in an interleaved converter are increased by a factor of N compared to a single-phase converter when the same inductor is used. For DCM, the duty cycle decreases by a factor $1/\sqrt{N}$ compared to a single-phase converter. Thus, ΔB is decreased by a factor $1/\sqrt{N}$. Since the core loss depends non-linearly on ΔB, the exact change can not be predicted. However, the combined losses will be larger than for the single-phase converter but less than a factor of N as for CCM operation.

5.4.4 Losses in the output capacitor

The losses in the output capacitor considered are conduction losses only. They are calculated in (5.45).

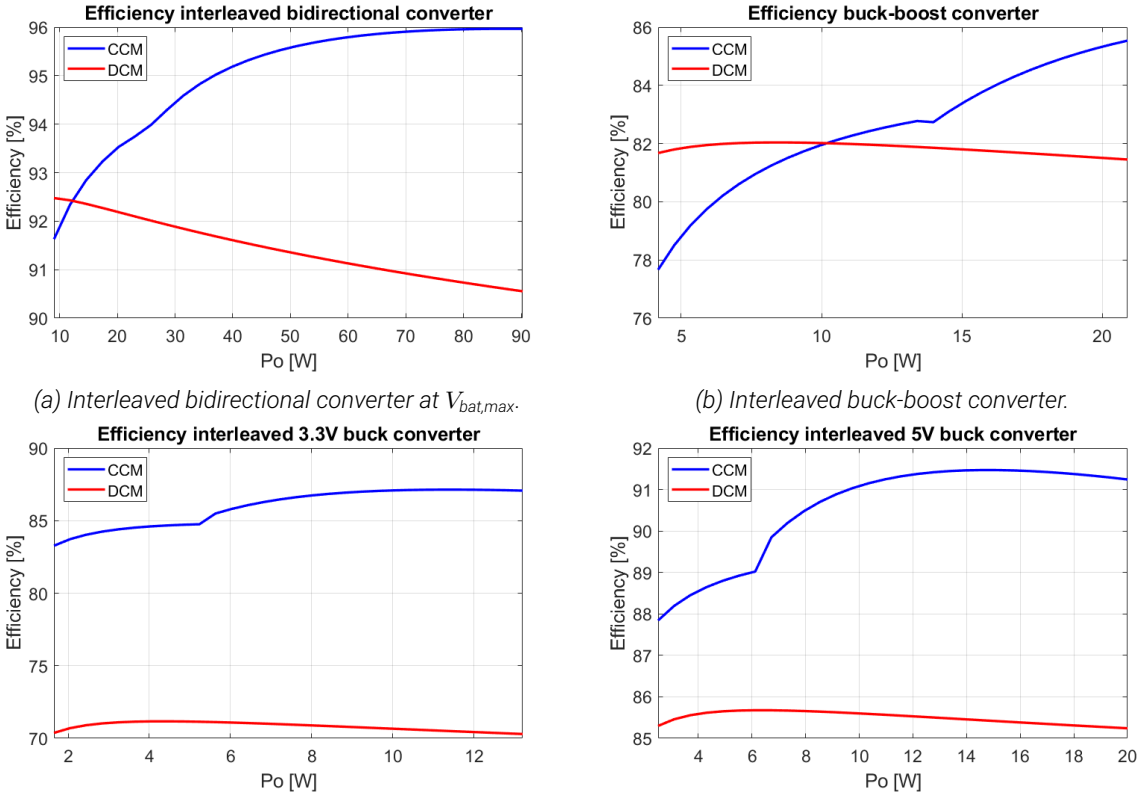
$$P_{\text{Co,int}} = I^2_{\text{Co,rms,int}} R_{\text{ESR}} \tag{5.45}$$

Here, $I_{\text{Co,rms}}$ is the RMS current in the capacitor, and R_{ESR} the equivalent series resistance of the output capacitor. In Chapter 5.3 was shown that the RMS current in the output capacitor of the interleaved converters is reduced compared to a single-phase converter. Therefore, the conduction losses in the output capacitors are reduced compared to a single-phase converter.

5.5 Results of Loss Calculations

5.5.1 Efficiency Curves

The efficiency of the interleaved converters for the CCM and DCM design as a function of the output power is shown in Figure 5.15. From Chapter 5.1, the output phase current of the interleaved converters operates in CCM before the phase currents become CCM. Table 5.12 summarises the conditions and corresponding values. Thus, when the phase current is DCM, the model for the DCM currents of the inductor, switch, and diode are used in the analysis. Similarly, the core loss in DCM is used. The crossover point from operating in DCM to CCM phase current of the CCM design is visible in Figure 5.15, for example at P_o = 6 W for the 5 V buck converter in Figure 5.15d.



(a) Interleaved bidirectional converter at $V_{bat,max}$.

(b) Interleaved buck-boost converter.

(c) Interleaved 3.3 V buck converter.

(d) Interleaved 5 V buck converter.

Figure 5.15: Efficiency curves of the interleaved converters for CCM and DCM.

Table 5.12: Condition and value of the output current for the output phase current and phase inductor current to operate in CCM of the interleaved converters.

	$I_{ph,o}$ is CCM		$I_{L,ph}$ is CCM	
	Condition	**Value**	**Condition**	**Value**
5 V Buck	$I_o > \frac{D(V_{in}-V_o)}{2LF_sN}$	0.331 A	$I_o > \frac{D(V_{in}-V_o)}{LF_s}$	1.33 A
3.3 V Buck	$I_o > \frac{D(V_{in}-V_o)}{2LF_sN}$	0.399 A	$I_o > \frac{D(V_{in}-V_o)}{LF_s}$	1.60 A
Bidirectional	$I_o > \frac{D(V_{in}-V_o)}{2LF_sN}$	0.152 A at $V_{bat,min}$ 0.584 A at $V_{bat,max}$	$I_o > \frac{D(V_{in}-V_o)}{LF_s}$	0.606 A at $V_{bat,min}$ 2.34 A at $V_{bat,max}$
Buck-Boost	$I_o > \frac{V_o}{4LF_s}$	0.909 A	$I_o > \frac{V_{in}D(1-D)}{LF_s}$	1.13 A

For the 3.3 V and 5 V interleaved buck converters, the CCM design is more efficient than the DCM design for the complete power range. However, for the interleaved bidirectional and buck-boost converter the DCM design is more efficient at low power than the CCM design. At low power, the core losses are low due to the low current ripple for both the CCM and DCM design. However, the inductor conduction losses are significantly larger for the CCM design due to the increased winding resistance. Hence, at low power, the DCM design is more efficient. At increasing power, the core losses for the DCM design increase sig-

nificantly. The core losses for the CCM design remain constant when the phase inductor current reaches CCM. Therefore, the efficiency at large power is larger for the CCM design than for the DCM design.

5.5.2 Losses in Components

Figure 5.16 shows the losses in each component of the interleaved converters operating at maximum power. The losses are shown as a percentage of the power rating of the corresponding converter. Similar observations as for the single-phase converters in Section 3.4 can be made. The converters operating in CCM have a higher efficiency than the converters operating in DCM. This is caused by the significant increase of inductor core losses in DCM [14].

For the CCM design, the losses in the output capacitor are sufficiently small that they are barely visible. The capacitor losses are increased significantly for the DCM design. The losses in the diode are a significant part of the losses. The main contribution of the diode losses is due to the forward voltage drop [11]. It is found that the losses due to the forward voltage drop of the diode contribute to 90% of the total diode losses for the 5 V and 3.3 V interleaved buck converters, 75% for the interleaved bidirectional converter, and 65% for the interleaved buck-boost converter. Therefore, the efficiency of these converters can be improved by implementing synchronous operation [100]. Though the same diode is used, the losses in the diode of the 3.3 V buck are larger than for the 5 V buck. This is because the duty cycle for the 3.3 V buck is lower, hence the diode conducts longer. It can be concluded that the CCM design results in a significantly more efficient system than the DCM design. Therefore, the interleaved converters will be operated in CCM.

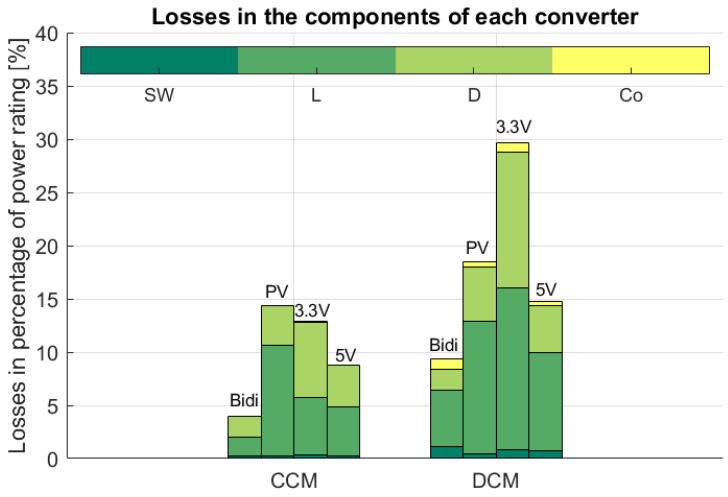


Figure 5.16: Losses in the switch (SW), inductor (L), diode (D), and output capacitor (Co) of the interleaved bidirectional (Bidi), PV buck-boost (PV), 3.3 V buck (3.3V), and 5 V buck (5V) converters at maximum power.

5.5.3 Comparison Interleaved and Single-Phase Converters

The losses in the interleaved converters are compared to the losses in the single-phase converters from Chapter 3.4.6 to verify if the interleaved converters are more efficient. In Figure 5.17, the total losses in each converter are shown for the interleaved and single-phase converters operating in CCM and DCM. For DCM, the combined losses in the interleaved converters are 19.27 W while in the single-phase converters 20.86 W. Thus, a reduction of 7.62% is achieved. For CCM, the sum of the losses of the interleaved converters is increased by 12.74% compared to those of the single-phase converters. Though the losses in the interleaved bidirectional and 3.3 V buck converters are lower than the single-phase converters, the losses in the buck-boost converter are increased significantly. This causes the total losses for the interleaved converters to be larger than the single-phase converters in CCM.

Further, it can be concluded that the losses in CCM are lower than in DCM for the interleaved converters, similar to the single-phase converters. The efficiency is improved by 90.42% when operating in CCM compared to DCM. Therefore the interleaved converters are operated in CCM. A more thorough analysis is made for the losses in CCM to see what causes the increase in combined losses for the interleaved

converters compared to the single-phase converters. The losses in each component for every converter operating in CCM are shown in 5.18. For all converters hold that the losses in the switch, diode, and output capacitor of the interleaved converters are reduced compared to the single-phase converters. On the contrary, the losses in the inductors are increased. The combined losses in the interleaved bidirectional converter are reduced by 5.37% compared to the single-phase converter, while for the interleaved 3.3 V buck converter by 9.00%. However, the combined losses in the interleaved buck-boost are increased by 118.54% compared to the single-phase converter, and for the interleaved 5 V buck converter by 1.26%.

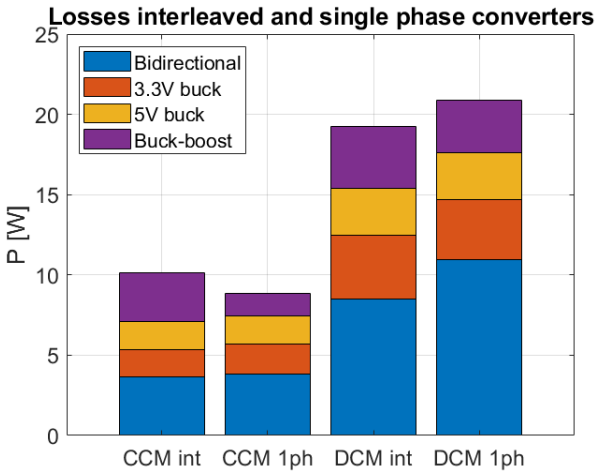


Figure 5.17: Comparing the combined losses for interleaved (int) and single-phase (1ph) converters operating in CCM and DCM.

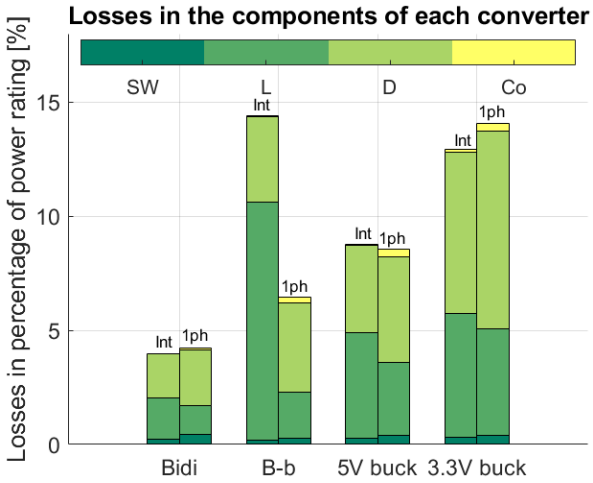


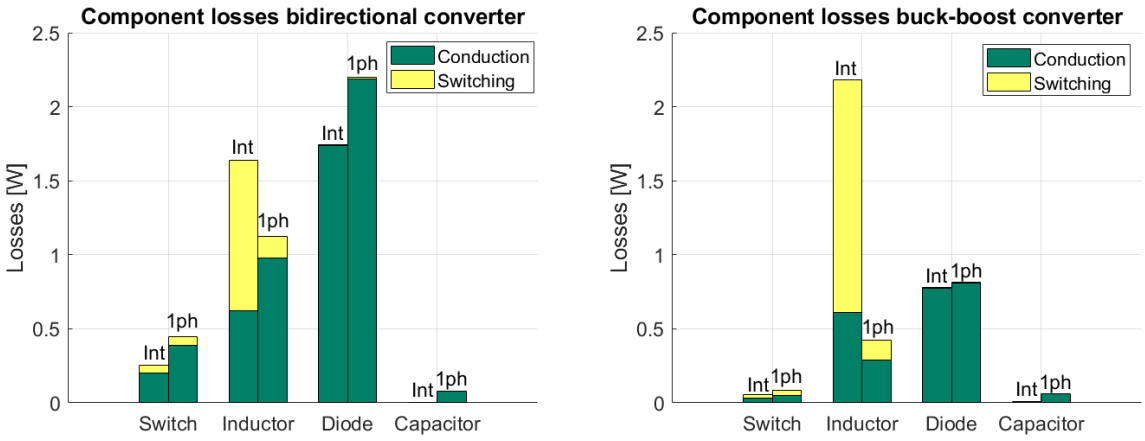
Figure 5.18: Comparing the losses in each component of the interleaved (int) and single-phase (1ph) converters operating in CCM.

From Chapter 5.4, when a two-phase interleaved converter is compared to a single-phase converter with the same components, the following is expected:

- E1. The total conduction losses in the switches are reduced by a factor of two.
- E2. The total conduction losses in the diodes are reduced by less than two.
- E3. The total switching losses in the switches and diodes remain the same.
- E4. The total conduction losses in the inductors are reduced by a factor of two.
- E5. The total core losses are increased by a factor of two.
- E6. The losses in the output capacitor are reduced significantly.

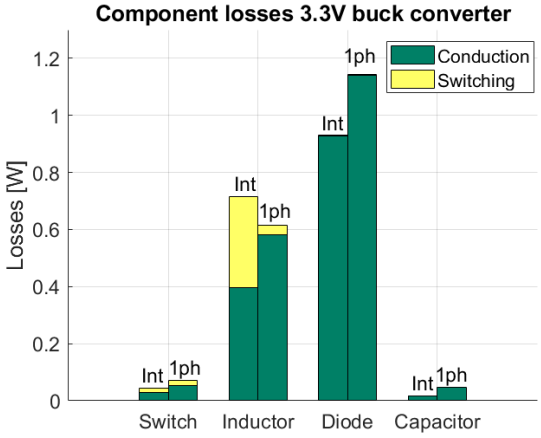
However, the inductors used for the interleaved converters are different than for the single-phase converters. Their inductance is approximately halved, increasing the current ripple. This increases the conduction losses slightly in the switch, diode, and output capacitor compared to E1, E2, and E6. However, it is difficult to predict the change in conduction and core losses of the inductors compared to E4 and E5 since they depend on the properties of the inductors used. The choice of inductors is based on the available inductors from the SGIHLP series of Vishay, which offers the inductors in space-grade and non-space-grade variants. Therefore, the effect on the conduction and core losses as a result of the reduced inductance for the interleaved converters is investigated further. The contribution of the switching losses and conduction losses in each component of the interleaved converters is shown in Figure 5.19. Note that the core losses in the inductor are categorised under switching losses.

The expected reduction in the conduction losses in the switch, diode, and output capacitor of the interleaved converters can be confirmed for each converter in Figure 5.19. The losses in the switches of the interleaved converters are reduced by slightly less than two, the losses in the diodes are reduced by less than two, and the losses in the capacitors are reduced significantly. The difference between the losses in the inductor for the converters is not consistent, however. This can be explained by the choice of inductors used. The properties of the inductors used for the interleaved and single-phase converters are provided in Table 5.13. For the single-phase converters, only inductors with an oversized DC current rating I_{DC} have the required saturation current. Therefore, though their inductance is larger, their DC resistance R_{DC} is

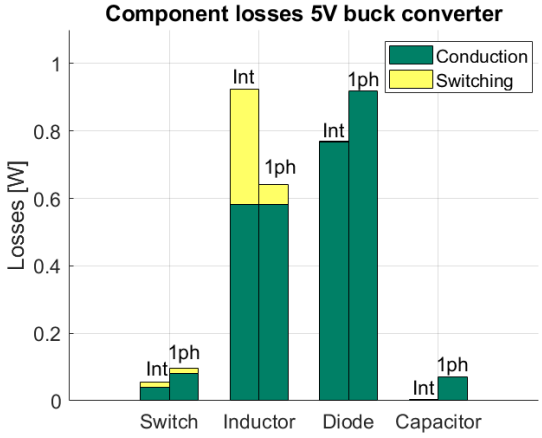


(a) Bidirectional converter at $V_{bat,max}$.

(b) Buck-boost converter.



(c) 3.3 V buck converter.



(d) 5 V buck converter.

Figure 5.19: Comparison of the switching and conduction losses in each component of the interleaved converters and single-phase converters operating in CCM.

lower than for the interleaved converters. Note the significant increase in footprint area and volume of the inductors of the single-phase converters.

Table 5.13: Comparison of the properties of the inductors used for interleaved and single-phase converters.

	Bidirectional		**Buck-boost**		**5 V buck**		**3.3 V buck**	
	Int	**1ph**	**Int**	**1ph**	**Int**	**1ph**	**Int**	**1ph**
L [μH]	22	47	33	75	22	33	15	33
I_{DC} [A]	11.7	13.5	3.7	12	4.1	7.25	5.1	7.25
R_{DC} [mΩ]	21.28	17.31	110	29.77	70.5	36.2	47	36.2
Footprint [mm^2]	360.4	673.2	157.9	673.2	157.9	360.4	157.9	360.4
Volume [mm^3]	3157.3	10260.3	981.9	10260.3	981.9	3157.3	981.9	3157.3

For the interleaved bidirectional and 3.3 V buck converters, the combined conduction losses in the inductors are reduced compared to the inductor of the single-phase converters. This is because the difference between R_{DC} of the inductors for the single-phase and interleaved converters is small. For the interleaved 5 V buck converter, R_{DC} is approximately twice as large as for the single-phase converter. Therefore, the combined conduction losses in the inductors are approximately equal to the losses in the inductor of the single-phase converter. For the interleaved buck-boost converter, however, R_{DC} is almost four times as large as for the single-phase converter. Thus, the resulting combined conduction losses are nearly two times larger than for the inductor of the single-phase converter.

The core losses of the interleaved converters are increased significantly compared to the single-phase converters. The core loss of the interleaved bidirectional converter is increased by a factor of 7.15 compared

to the single-phase converter. Similarly, the core loss for the interleaved buck-boost converter is increased by 12.06, for the 5 V buck by 5.76, and for the 3.3 V buck by 9.35. Two changes are made in the inductors of the interleaved converters compared to the single-phase converters. The inductance is reduced and the core volume is decreased for the interleaved converters. The former increases the change in flux density ΔB, increasing the core losses. The influence of the latter is determined from the core loss tool from Vishay [97]. It is found that the core losses are increased for an inductor with the same inductance but a smaller core volume when operated in the same conditions. From the generalised Steinmetz equation in (5.44), ΔB is increased when a smaller core volume is used due to the decrease of the core area A_c, increasing the core losses. However, the core loss P_V is directly proportional to the core volume V_e, thus reducing the core losses. Therefore, it can be concluded that the increase in ΔB increases the core loss more than the decrease in V_e reduces the core loss. Because both the inductance and core volume are reduced for the interleaved converters, the core losses are increased significantly.

It can be concluded that the conduction losses in the switch, diode, and output capacitor are reduced in the interleaved converters compared to the single-phase converters. The switching losses in the switch and diode remain unaffected. However, the inductor losses are increased due to a significant increase in the core losses. Because the inductor losses in the interleaved buck-boost converter are increased significantly, the combined losses of the interleaved converters are higher than those of the single-phase converters. However, without the buck-boost converter, the losses are lower for the interleaved converters. Thus, the rover can operate for a longer time before the batteries need to be charged using the interleaved topology, but charging takes more time.

To improve the efficiency, the inductor losses can be reduced. The inductance can be increased, reducing ΔB and therefore the core losses. Second, the core size can be increased because it was found that the core losses are reduced when increasing the core size for the SGIHLP inductors from Vishay. This also results in lower R_DC for these inductors, so the conduction losses are reduced as well. However, both improvements come at the cost of increased size and weight of the inductors. Another improvement for the efficiency is implementing synchronous operation where the diode is replaced by a switch. It is found that the losses in the diodes are a significant part of the losses in the converters.

5.6 Gate Driver

The Infineon 1EDN7146U EiceDRIVER is used as gate driver for the GaN switches. This section covers the design of the gate resistor and bootstrap circuit used with the gate driver to drive the switches.

5.6.1 Gate Resistor

One of the advantages of GaN switches is their fast switching speed. However, fast switching also results in a large voltage overshoot that can exceed the maximum voltage rating of the switch which can destroy the device. Additionally, from Chapter 2.1, larger applied voltages increase the chance on SEBs. Thus, the vulnerability to SEBs is increased during the voltage overshoot as well. The voltage overshoot is caused by stray inductance when switching off. The voltage induced due to the stray inductance is given by (5.46).

$$V_\mathrm{L,stray} = L_\mathrm{stray} \frac{di_\mathrm{L}}{dt} \tag{5.46}$$

Thus, the induced voltage can be reduced by reducing the stray inductance L_stray, or by limiting the current slope di_L/dt during turn-off. Furthermore, high frequency oscillations occur due to LC resonance with the parasitic inductances and capacitances of the device [110, 111]. This negatively affects the EMI emitted. In addition, false triggering oscillations can occur where the gate voltage oscillates such that the device is turned on and off repeatedly [112].

The aforementioned phenomena can be reduced by increasing the gate resistor [111]. The gate resistor controls the switching speed of the GaN switches. The value of the gate resistor is calculated by (5.47) [113].

$$R_\mathrm{G} = \frac{V_\mathrm{dd} - V_\mathrm{GS,th}}{\frac{dV_\mathrm{DS}}{dt} C_\mathrm{GD}} \tag{5.47}$$

Here, V_{dd} is the gate driver supply voltage, $V_{GS,th}$ the worst-case threshold voltage of the GaN switch, dV_{DS}/dt the slope of the drain-source voltage during switching, and C_{GD} the gate-drain capacitance. Low voltage switches do not have a recommended dV_{DS}/dt in their datasheet. In real applications, $dV_{DS}/dt <$ 40 V/ ns [114]. Therefore, a worst-case value of 40 V/ ns is used for the gate resistance calculation. Table 5.14 provides the values of the gate resistors used.

Table 5.14: Gate resistor values used for the interleaved converters.

	5 V and 3.3 V buck	**Bidirectional**	**Buck-boost**
$\mathbf{R}_G$	7 Ω	9.09 Ω	10 Ω

Figures 5.20 and 5.21 show the drain-source voltage and drain current, and gate-source voltage and gate current, respectively, of the 5 V interleaved buck converter. In these figures, the influence of the gate resistor is shown on the ringing and overshoot of the drain and gate voltage and current. The double pulse test simulation used is discussed in Appendix E.1. From Figure 5.20, adding a gate resistance reduces the drain-source voltage overshoot from 51.0 V to 47.5 V. Furthermore, the ringing in the drain-source voltage and drain current is reduced, but only slightly. From Figure 5.21, there is no ringing present in the gate voltage. The ringing of the gate current is reduced by adding the gate resistance.

The reduction in drain-source voltage overshoot is insufficient. The maximum voltage rating of the switch is exceeded. Furthermore, the reduction in ringing and oscillations is inadequate. Similar observations are made for the other interleaved converters. Therefore, a snubber network is added to mitigate these effects further. The design is presented in Chapter 5.7.

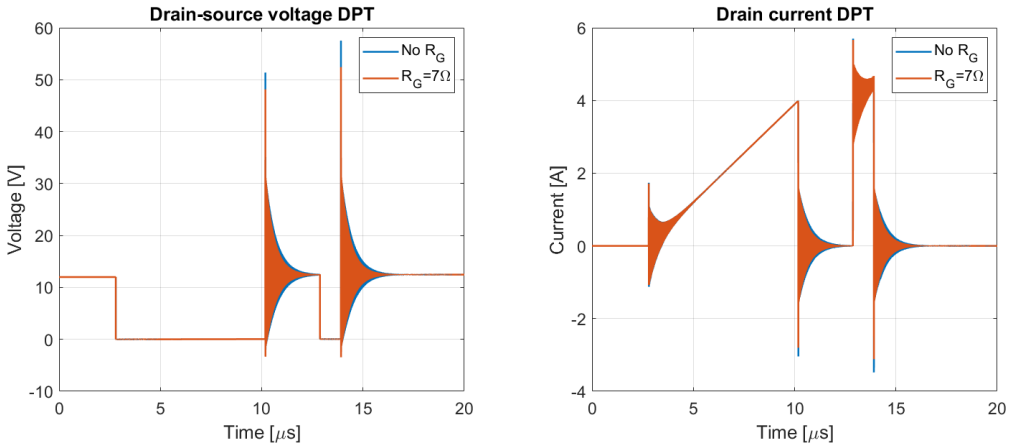


Figure 5.20: Influence of the gate resistor on the overshoot and ringing of V_{DS} and I_D of the 5 V buck converter.

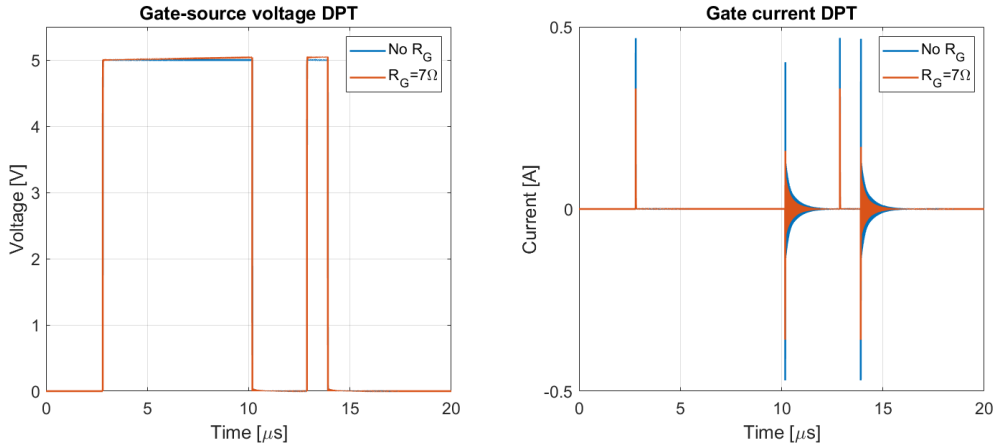


Figure 5.21: Influence of the gate resistor on the overshoot and ringing of V_{GS} and I_G of the 5 V buck converter.

5.6.2 Bootstrapping High Side Switches

For the GaN switches to be driven in full enhancement, the gate voltage should be 5 V above the source voltage. This poses no problems for low-side switches where the load is connected to the drain and the source is at ground potential. However, for high-side switches, the load is connected to the source of the switch. Thus, the voltage of the gate would have to be above the rail voltage. The gate voltage is controlled using low-voltage logic referenced to ground. Therefore, the control signals need to be shifted to the source potential. One of the most common methods for driving high-side switches is the bootstrap circuit [113]. Its advantages are simple implementation and low cost. However, the drawback is that the on-time is limited by the requirement to refresh the charge of the bootstrap capacitor [115].

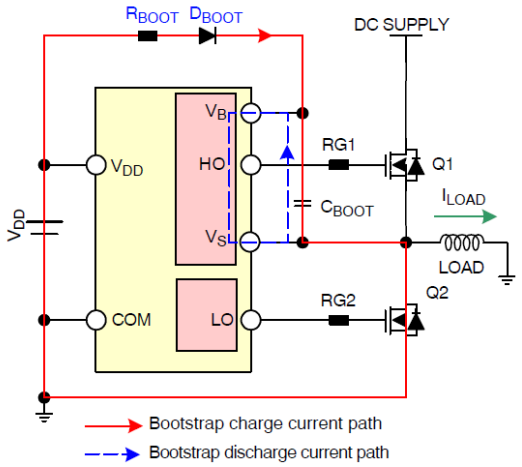


Figure 5.22: Bootstrap circuit of a half-bridge gate driver [113].

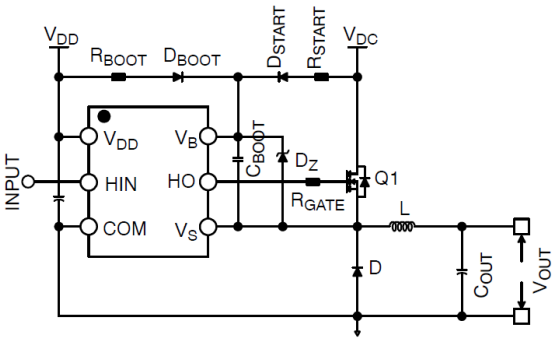


Figure 5.23: Bootstrap circuit including startup circuit for buck converters [113].

The bootstrap circuit consists of a resistor, diode, and capacitor. Figure 5.22 shows a common circuit consisting of a gate driver for a half-bridge including bootstrapping circuitry. This is representative for the interleaved bidirectional converter. When the high side switch Q_1 is turned off, the low side switch Q_2 conducts and the source of Q_1 is at ground potential. During this time, the bootstrap capacitor is charged to V_{DD} by the gate driver supply voltage V_{DD} through R_{boot} and D_{boot}. When Q_1 is turned on, C_{boot} is connected between the gate and source of Q_1 by the gate driver. This creates a floating voltage equal to the voltage of V_{Cboot}=V_{DD}. In this way, a gate-source voltage of 5 V is created. The bootstrap diode is reversed biased and blocks the bootstrap capacitor voltage from the lower gate driver supply voltage V_{DD}. The gate charge of Q_1 is supplied by C_{boot}. This creates a limitation regarding the on-time of the high-side switch. If C_{boot} is not charged enough during the off-time of Q_1, its voltage drops until Q_1 can not be turned on any more.

For the interleaved buck converters, the low-side switch is replaced by a diode. The C_{boot} charge path is through the load to ground, instead of through the low-side switch to ground. This introduces a problem when there is an output voltage present but zero load current. The diode is in blocking state so the source of Q_1 can not be pulled down to ground potential. Instead, it sits at the output voltage. Furthermore, there is no current to charge C_{boot}. Thus, the bootstrap capacitor can not be charged at all [116]. To mitigate this problem, a startup circuit consisting of a zener diode D_z and an additional diode D_{start} and resistor R_{start} is included. This is shown in Figure 5.23. The bootstrap capacitor is charged through D_{start} and R_{start} to zener voltage V_z. The zener voltage should be larger than V_{DD} and, to prevent damage to the gate of the GaN, switch below 6 V. Note that this method works when $V_{DC} > V_o + V_{Dstart} + V_{Rstart}$ only. The drawback is that the current through D_{start} and R_{start} is permanent. Therefore, R_{start} should be as large as possible.

The bootstrapping method does not work for the buck-boost converter. Due to the inverted output voltage, the C_{boot} is charged to $V_{DD} + V_o$ instead of V_{DD}. This is larger than the maximum voltage rating of the GaN switch. Therefore, an isolated DC/DC converter is used for each switch. The drawback of this method is a significant increase in the component count compared to the bootstrap method.

The value of the bootstrap components is calculated from the datasheet of the gate driver [117]. The value of the start resistor R_{start} is determined from simulations in LTspice, where the largest value of R_{start} is found such that the gate driver can operate during startup. The resulting values for each converter are

similar, hence the same components are used. These are summarised in Table 5.15. Operation of the bootstrap and startup circuits for each converter are verified using LTspice simulations.

Table 5.15: Overview of the bootstrap components used.

$\mathbf{C}_{\text{boot}}$	$\mathbf{R}_{\text{boot}}$	$\mathbf{C}_{\text{Vdd}}$	$\mathbf{R}_{\text{start}}$	$\mathbf{D}_{\text{z}}$	$\mathbf{D}_{\text{start}}$
220 nF	4.7 Ω	470 nF	20 kΩ	DFLS130L	DFLS130L

5.7 Snubber Design

In Chapter 5.6.1 was found that adding the gate resistor results in insufficient reduction of the drain voltage overshoot and oscillations. An RC snubber network in parallel to the switch is used to mitigate the voltage overshoot and oscillations further. However, designing the optimal values of the snubber network is non-trivial [118]. In [119], it is shown that the power loss in the snubber network is determined by the capacitance. Thus, the capacitance must be as low as possible to limit the losses in the snubber network. In [120], a simulation study has been performed to find the optimal snubber component values. The influence of the snubber resistance is investigated to see the effect on the V_{DS} overshoot and losses in the snubber resistance. This is done by changing the snubber resistance while keeping the snubber capacitance constant. The same is done for the snubber capacitance.

The simulation study of [120] is adopted to find the optimal snubber component values for the interleaved converters. This is done for the worst-case operating conditions to ensure the voltage overshoot remains within the maximum rated voltage of the switch at all times. The worst-case conditions are at the maximum voltage seen by the switch and at the maximum current that the switch must switch during turn-off. The latter occurs in single-phase mode. The double pulse test simulation used is discussed in Appendix E.1. Because the simulation study is repetitive for each converter, only the buck converters are covered in this section. The bidirectional and buck-boost converters are covered in Appendix E.2.

5.7.1 Snubber Interleaved Buck Converters

The same switch (EPC2014C) is used for the 5 V and 3.3 V interleaved buck converter. Furthermore, they share the same bus voltage so the voltage seen by the switch is the same for the two converters. Finally, their current rating is the same. Therefore, the same snubber component values can be used, and only one simulation study has to be performed for both converters.

Figure 5.24 shows the drain-source voltage when switching off for different values of R_s when C_s = 1 nF. For $R_s = 1\Omega$, significant ringing is observed. By increasing the resistance, the ringing is more damped. The overshoot is reduced when increasing the resistance from 1 Ω to 5 Ω. However, increasing the resistor further increases the overshoot and ringing observed. This is in accordance with the results obtained in [119], where it is shown that increasing the resistance beyond a certain value increases the overshoot. The losses in the snubber resistance for turn-off and turn-on are shown in Figure 5.25. When R_s > 5 Ω, the losses are barely affected by the snubber resistance value.

The drain-source voltage when switching off using different values of C_s while keeping the resistance fixed is shown in Figure 5.26. By increasing the capacitance, the ringing is more damped. Furthermore, the overshoot is also reduced for increasing C_s. Figure 5.27 shows the energy losses in the snubber resistance for turn-off and turn-on using different values for C_s. The losses increase exponentially for an increasing capacitance. Thus, to minimise the losses in the snubber, the capacitance should be minimised. This is in accordance with the results from [119] as well.

Because the losses increase rapidly for C_s > 1 nF, a capacitance of 1 nF is chosen. Furthermore, the resistance of 5 Ω resulted in the lowest overshoot while still providing a significant amount of damping. Therefore, the snubber values used are C_s = 1 nF and R_s = 5 Ω. From Figure 5.25, the energy loss is 205.00 nJ. This results in an average power loss of $P_{\text{sn}} = E_{\text{sn}} F_{\text{s}}$ = 20.5 mW. At maximum load, this reduces the efficiency by 0.103% and 0.124% for the 5 V and 3.3 V interleaved buck converter, respectively. Therefore, these losses are negligible.

The drain-source voltage and drain current are provided in Figure 5.28. In this figure, the influence of adding the snubber is shown on the ringing and overshoot of the voltage and current of the drain. The voltage

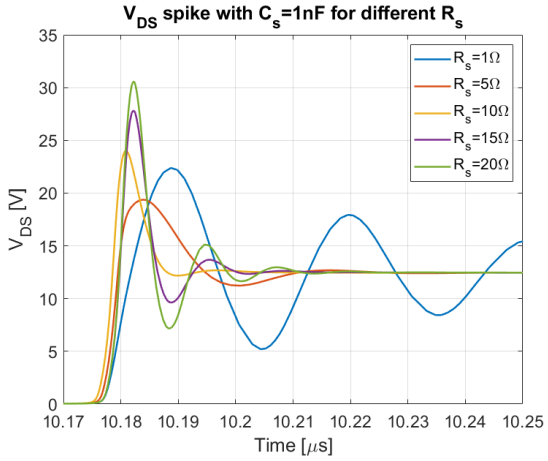


Figure 5.24: Simulated drain-source voltage overshoot of buck converter for different resistance values.

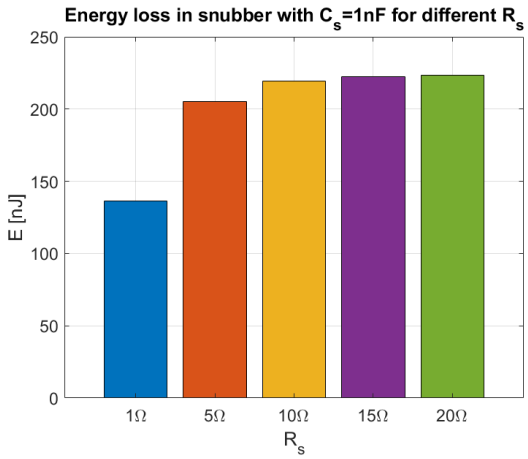


Figure 5.25: Simulated energy loss in snubber for different resistance values.

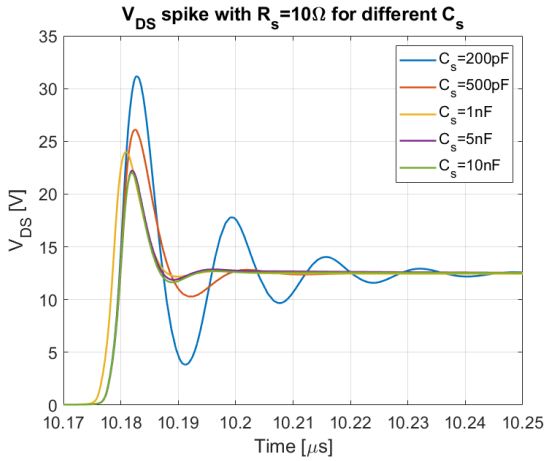


Figure 5.26: Simulated drain-source voltage overshoot of buck converter for different capacitances.

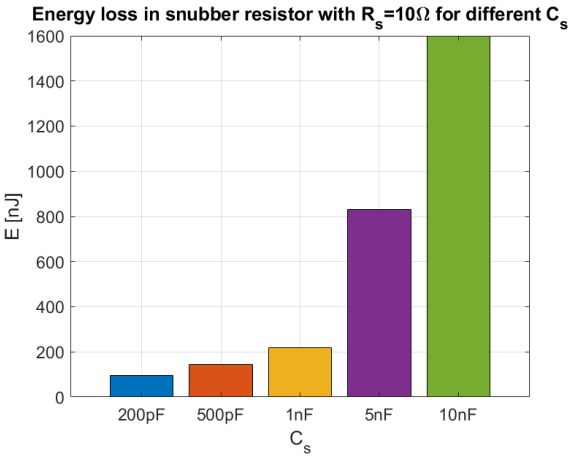


Figure 5.27: Simulated energy loss in snubber of buck converter for different capacitor values.

overshoot is reduced from 47.5 V to 19.1 V. Furthermore, the ringing of the drain-source voltage is almost completely damped. Similarly, the negative overshoot of the drain current is reduced significantly at turn-off, and the ringing is almost completely damped. Because a turn-off snubber is used, no reduction of oscillation of the drain current at turn-on is visible. Thus, it can be concluded that the addition of the snubber network mitigates the overshoot and oscillations sufficiently, which was not achieved by the gate resistor alone. Table 5.16 provides the resulting snubber values of each converter.

Table 5.16: Snubber component values.

	Bidirectional	**Buck-boost**	**5 V buck**	**3.3 V buck**
$\mathbf{C_S}$	2 nF	500 pF	1 nF	1 nF
$\mathbf{R_S}$	4 Ω	15 Ω	5 Ω	5 Ω

5.8 Startup Circuit PES

The moment the batteries are connected to the system, no energy is available at the gate drivers and microcontroller and all output voltages are at 0 V. Thus, no Pulse Width Modulation (PWM) signals can be generated and the switches can not be driven by the gate drivers. Hence, a startup system consisting of two Low-Dropout Regulators (LDOs) is made. The startup circuit is shown in Figure 5.29. When the

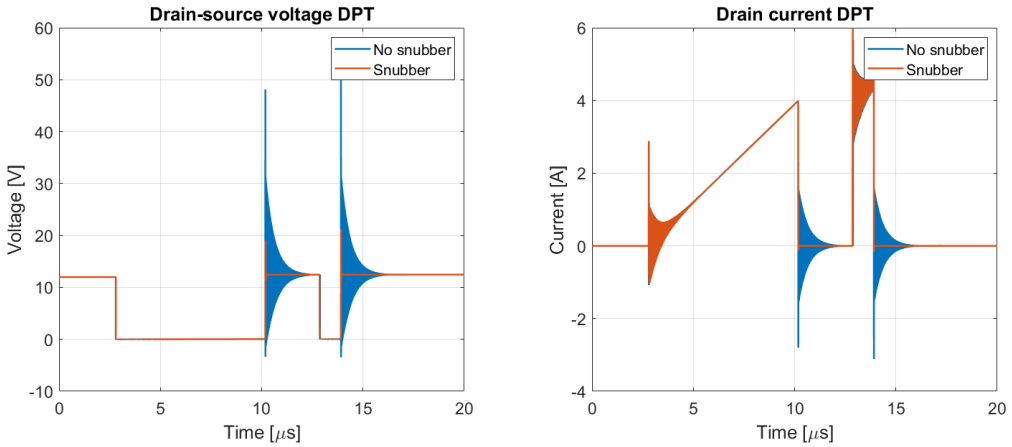


Figure 5.28: Drain-source voltage and current of the interleaved 5 V buck converter without and with snubber.

batteries are connected to the system, the microcontroller is off and hence Q_1 is open. Thus, the enable pin of the LDOs is pulled high to the battery voltage and the LDOs are enabled. When the bidirectional converter has regulated the bus voltage to 12 V, the startup of the PES has completed. The microcontroller pulls the shutoff pin high, enabling Q_1 and pulling the enable pins to ground so the LDOs are disabled. The microcontroller and gate drivers are then powered by the 3.3 V and 5 V interleaved buck converters, respectively.

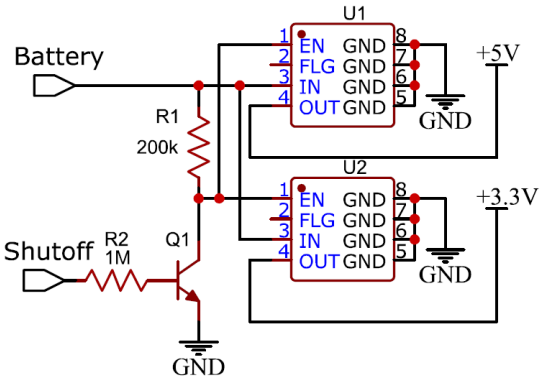


Figure 5.29: Startup circuit for powering the microcontroller and gate drivers.

Chapter 6

Control Implementation of the Interleaved Converters

The design of the hardware of the PES was presented in Chapter 5. However, to test the prototype of the PES, control of the hardware is required. This chapter focuses on the implementation of the control for each converter. First, in Section 6.1, the design of the controller for the bidirectional and buck converters using voltage control is discussed. Next, the digitisation of the controllers and program flow on the microcontroller is discussed in Section 6.2. Finally, Section 6.3 discusses the MPPT algorithm implemented for the buck-boost converter.

6.1 Voltage Control of DC/DC Converters

When the load is constant and without external disturbances, open loop control suffices to regulate the output of a DC/DC converter. However, the current drawn by the subsystems of the rover will change continuously. Therefore, closed-loop control is required to regulate the output voltage of each DC/DC converter. The output voltage can be regulated using voltage control or current control. Current control can achieve higher bandwidths than voltage control, hence has better transient response [121]. However, current control requires two control loops. This increases the complexity of tuning the controllers for stable operation. Voltage control requires only one control loop, hence this method is adopted.

Voltage control can be easily implemented using a Proportional Integral (PI) controller. The transfer function of the parallel PI controller in Laplace domain is given by (6.1).

$$G_{\mathrm{PI}}(s) = \frac{D(s)}{e(s)} = K_{\mathrm{p}} + \frac{K_{\mathrm{i}}}{s} \tag{6.1}$$

Here, K_{p} and K_{i} are the proportional and integral gains, respectively. Figure 6.1 shows the closed-loop control block diagram for voltage control. The output voltage is subtracted from the reference voltage. This error is the input of the PI controller. The output of the PI controller is the reference of the duty cycle for the PWM generator. The PWM generator in turn provides the PWM signal for the switch of the DC/DC converter.

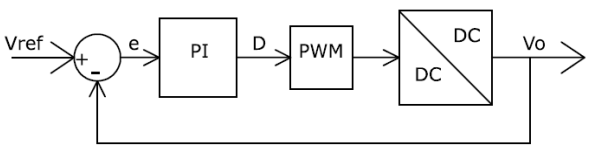


Figure 6.1: Voltage control block diagram.

	Bidirectional	5V buck	3.3V buck
$\mathbf{K}_{\mathrm{u}}$	0.967	1.033	0.670
$\mathbf{T}_{\mathrm{u}}$	71 μs	80 μs	77.5 μs
$\mathbf{K}_{\mathrm{p}}$	0.0870	0.0930	0.0603
$\mathbf{K}_{\mathrm{i}}$	738.16	700.28	468.71

Table 6.1: PI controller parameters.

Tuning the PI controller can be done based on the small-signal transfer function of the plant it controls or using heuristic methods. The Ziegler-Nichols closed-loop tuning method is an often used heuristic method for tuning PI controllers of DC/DC converters [122, 123]. In this method, K_{i} is set to zero and K_{p} is increased until the ultimate gain K_{u} is reached. At this gain, the system is marginally stable. The period T_{u} of the sustained oscillations is measured. Finally, the values of K_{p} and K_{i} are found from (6.2)-(6.3) [122].

$$K_{\mathrm{p}} = 0.45 K_{\mathrm{u}} \tag{6.2}$$

$$K_\mathrm{i} = \frac{K_\mathrm{p}}{0.83 T_\mathrm{u}} \tag{6.3}$$

However, during simulations was found that K_p and K_i require some downscaling for stable operation. The resulting values of K_u, T_u, K_p, and K_i are provided in Table 6.1. The voltage regulation capability of the PI controllers is elaborated in Appendix D.3.

6.2 Control Implementation on Microcontroller

6.2.1 Discretisation of the PI Controller

To implement the PI controller on the microcontroller, the transfer function of the PI controller must be transformed to the discrete domain. Discretisation of the integral action of the PI controller results in an approximation by a discrete summation. In [124] is shown that transforming (6.1) to the discrete domain using the bilinear transform, and by using a first-order hold approximation for the integral action, the resulting difference equation of the output D is given by (6.4). Here, $\omega_{\mathrm{PI}} = K_\mathrm{i}/K_\mathrm{p}$ is the bandwidth of the PI controller in rad/s, and T_{sample} the sampling time of the output voltage. In this case, the voltage is sampled once every time the control loop is executed. Hence, the sampling frequency is equal to the execution frequency of the control loop.

$$D[k+1] = K_\mathrm{p}\left(\frac{\omega_{\mathrm{PI}} T_{\mathrm{sample}}}{2} + 1\right) e[k+1] + K_\mathrm{p}\left(\frac{\omega_{\mathrm{PI}} T_{\mathrm{sample}}}{2} - 1\right) e[k] + D[k] \tag{6.4}$$

For first-order hold, $\omega_{\mathrm{sample}} \geq 10\omega_{\mathrm{PI}}$ to obtain less than 3% error between the continuous and discrete controller [124]. The ω_{PI} of the bidirectional converter is largest with 8.48 krad/s, thus $F_{\mathrm{samp}} > 13.5$ kHz. However, the microcontroller used is the MSP430FR5969 and is a design constraint. It is a low-performance microcontroller so its computation speed is limited, especially for floating-point operations. After optimising the code using fixed point representation, the control loop can run at approximately 35.7kHz for a single controller. Since one microcontroller is used, each converter can run at only 8.9kHz. Usually, the sampling frequency is chosen to be an integer of the switching period to avoid aliasing due to undersampling [125]. Thus, the sampling frequency for each converter is set to F_{samp} = 5 kHz.

6.2.2 Voltage Regulation Capability of Digital Controllers

The voltage regulation capability of the interleaved 5 V and 3.3 V buck converters and bidirectional converter is discussed next. In general, though $\omega_{\mathrm{sample}} < 10\omega_{\mathrm{PI}}$, the digital controllers behave similarly to the controllers in continuous domain, which is provided in Appendix D.3. The simulation models used for the voltage regulation capability of the interleaved bidirectional, and 5 V and 3.3 V buck converters are provided in Appendix D.2.

Buck Converters

The voltage regulation capability of the digital controller of the 5 V buck converter is shown in Figure 6.2. Initially, the converter operates in steady state at an output current of 1 A. At 3 ms, the output current starts increasing exponentially to 4 A in 10 ms. The output voltage drops by 1.8% to 4.91 V with minor oscillations. When the inductor phase currents become CCM at I_o=1.33 A, the output voltage increases with some oscillations to its reference voltage. From this moment, the controller can regulate the output to its reference with increasing load, showing only small drops and oscillations. When the output current reaches 4 A, some overshoot of the output voltage occurs due to the sudden stop of load increase. After a few oscillations, the output voltage is at its reference. However, some periodic steady-state oscillations are still visible caused by aliasing due to the low sampling frequency of 5 kHz.

Similar observations can be made for the voltage regulation capability of the digital controller of the 3.3 V buck converter, shown in Figure 6.3. The output voltage drops by 2.1% to 3.23 V. When the inductor phase currents reach CCM, the voltage increases to its reference. However, the controller suffers more from steady-state oscillations due to aliasing, both at steady-state at the start of the simulation and the end of the simulation. Due to aliasing, the voltage ripple frequency is folded to a lower frequency. This is shown

for the 3.3 V buck converter in steady state at maximum load in Figure 6.4. The sampled output voltage $V_{o,z}$ shows periodic oscillations at a frequency of 1.67 kHz. This results in an additional output voltage ripple in steady state at 1.67 kHz as well.

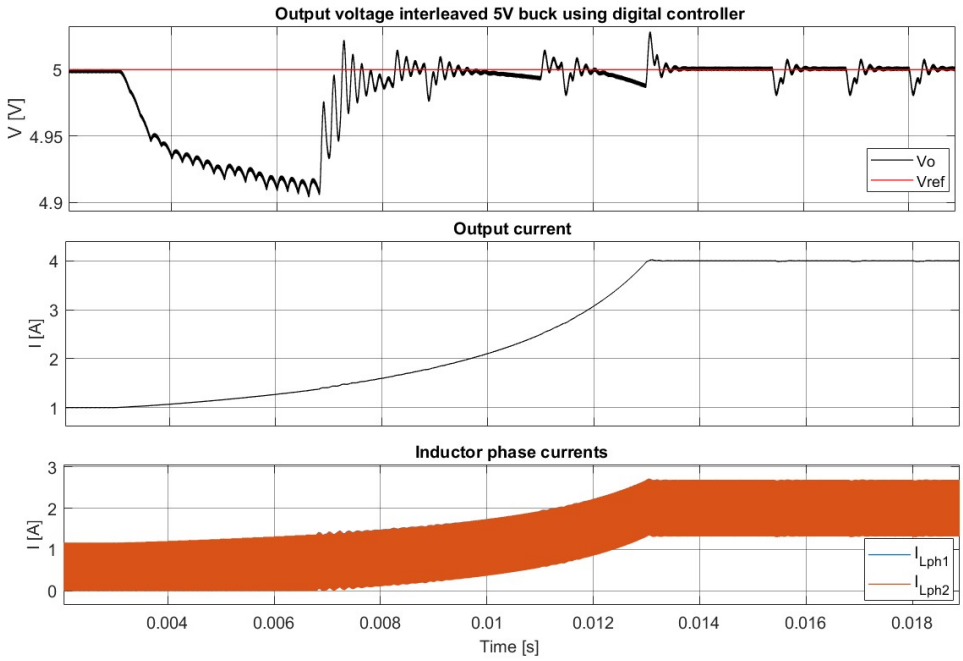


Figure 6.2: Simulation of the interleaved 5V buck converter using the digital PI controller under increasing load conditions.

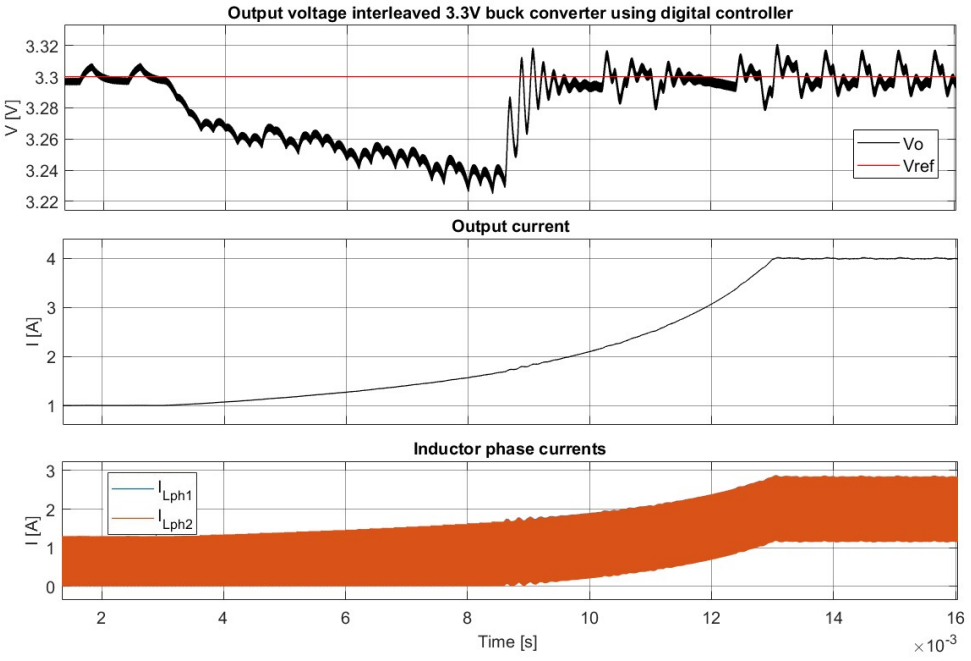


Figure 6.3: Simulation of the interleaved 3.3V buck converter using the digital PI controller under increasing load conditions.

Bidirectional Converter

The voltage regulation capability of the interleaved bidirectional converter is provided in Figure 6.5. Similar to the 3.3 V buck converter, steady state oscillations occur at the start and end of the simulation due to

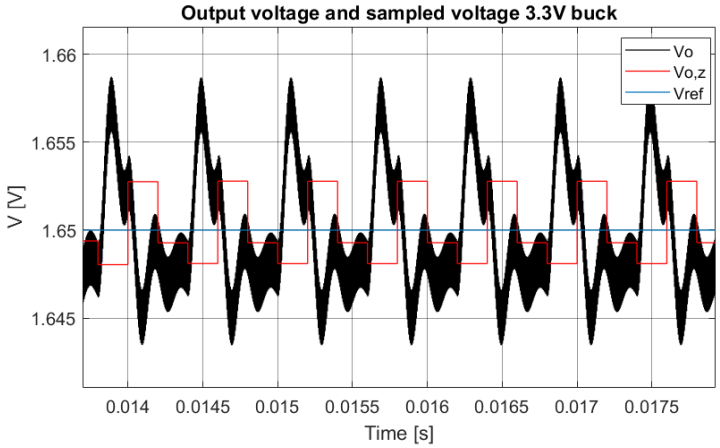


Figure 6.4: Output voltage oscillations at steady state of the 3.3 V interleaved buck converter.

aliasing. Initially, the load current is 2 A and the converter operates in forced CCM where the inductor current becomes negative. At 3 ms, the load is increased exponentially to its maximum of 7.51 A in 10 ms. Unlike the 5 V and 3.3 V buck converters, the output voltage remains regulated to its reference with some oscillations and small drops. For the 5 V and 3.3 V buck converters was found that the output voltage is regulated to its reference when the inductor currents become CCM. Therefore, it can be concluded that the bidirectional converter can keep its output voltage to its reference because the inductor currents are always CCM, even for DCM load conditions.

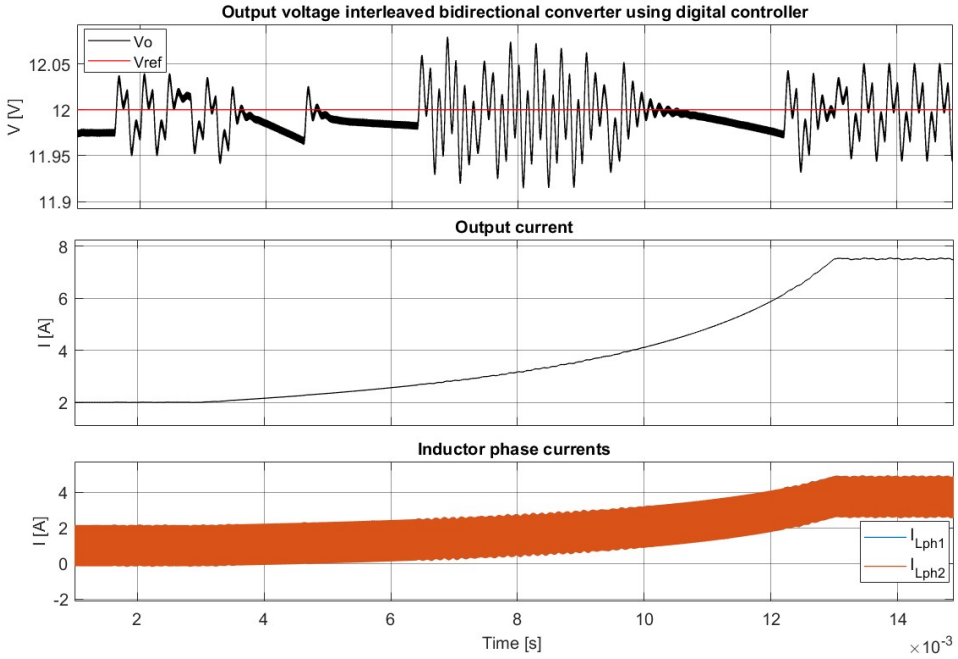


Figure 6.5: Simulation of the interleaved bidirectional converter using the digital PI controller under increasing load conditions.

6.2.3 Modulation Strategy

The PWM signals are generated using the MSP430FR5969 microcontroller. This microcontroller is capable of generating the ten PWM signals required for all converters. This is done using the internal timers TA0, TA1, and TB0 of the microcontroller [126]. The timers are set in up/down mode because symmetrical pulse generation is required for generating dead times in the bidirectional converter. Furthermore, creating the time shift of $T_S/2$ between the two phases of each converter is easily implemented. The timers are operated at their maximum frequency of 24 MHz. Thus, to obtain a switching frequency F_S = 100 kHz, the

timers must count to CCR0 = $\frac{F_{\text{clk}}}{2F_{\text{s}}}$ = 120.

PWM Generation for Buck and Buck-Boost Converters

For the interleaved buck and buck-boost converters, the PWM signal of phase 1 is generated using output mode 2: Toggle/Reset. The duty cycle D calculated by the PI controller is converted to a count value using equation (6.5) and written to the corresponding CCR1 register.

$$\text{CCR1} = D \cdot \text{CCR0} \tag{6.5}$$

The PWM signal of phase 2 is generated using output mode 6: Toggle/Set. The duty cycle in count number format is calculated using equation (6.6), and is written to the corresponding CCR2 register.

$$\text{CCR2} = \text{CCR0} - \text{CCR1} \tag{6.6}$$

Figure 6.6 shows the resulting waveforms. The timer counts up to CCR0, and the PWM signals of phases 1 and 2 are toggled when the timer reaches the value stored in the CCR1 or CCR2 register, respectively. The duty cycle of phase 2 is equal to that of phase 1. Finally, the PWM signal of phase 2 has a time shift of Ts/2 compared to the PWM signal of phase 1.

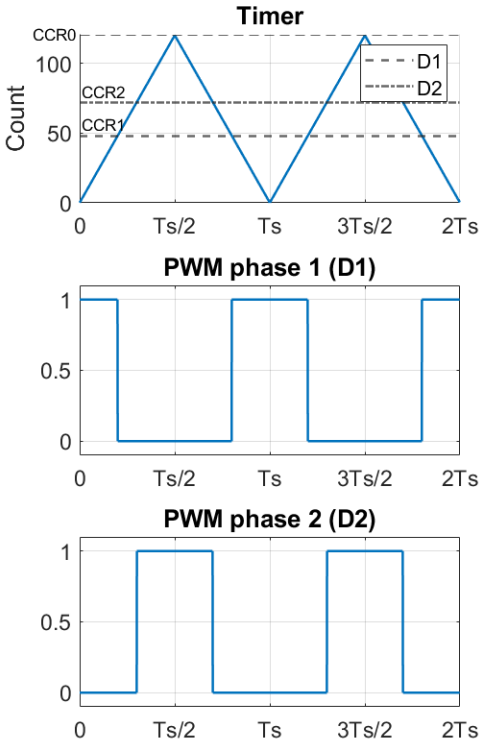


Figure 6.6: PWM modulation strategy for the two phases of the interleaved buck and buck-boost converters.

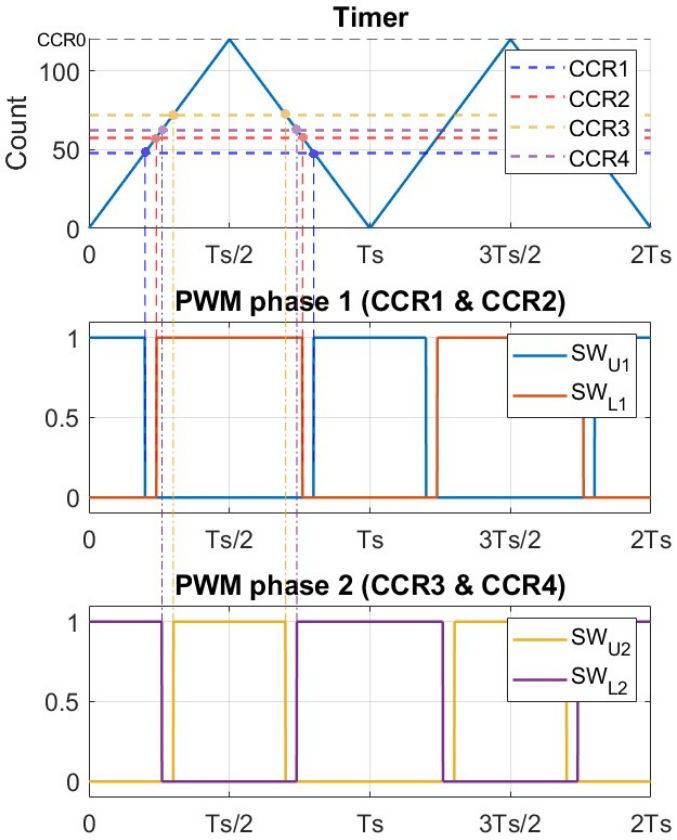


Figure 6.7: PWM modulation strategy for the two phases of the interleaved bidirectional converter.

PWM Generation for the Bidirectional Converter

The PWM generation of the interleaved bidirectional converter is more complex. The gate driver requires synchronous operation to charge the bootstrap capacitor. This can be achieved using complementary PWM generation. Ideally, when the converter is operating in DCM at light load, the synchronous switch should be turned off when the inductor current becomes zero. Then, the inductor current does not become

negative. However, as shown in [127], this introduces parasitic ringing of the inductor voltage and current during turn-off conditions. This is caused by the inductor and parasitic switch capacitance. The result is reduced efficiency and a significant increase of EMI. Therefore at light loads, the converter is operated at forced CCM. The synchronous switch remains on until T_s and the inductor current becomes negative. The drawback is increased losses in the inductor and switch.

In a practical half-bridge circuit, the switches have a finite turn-on and turn-off time. Furthermore, a finite delay exists between the PWM generated by the microcontroller and the output of the gate drivers. To prevent both switches from being on simultaneously, thus shorting the input voltage, a dead time must be implemented. In the datasheet of the gate driver a blanking time of 80 ns is specified [117]. The complementary PWM signals of the half-bridge of phase 1 are generated as follows. The output mode of the upper switch is toggle/reset, while the lower switch is toggle/set. The count values corresponding to the duty cycle of the upper and lower switch are calculated in (6.7)- (6.8), respectively. Here, t_dead is in number of clock cycles.

$$\mathrm{CCR1} = D \cdot \mathrm{CCR0} \tag{6.7}$$

$$\mathrm{CCR2} = \mathrm{CCR1} + t_\mathrm{dead} \tag{6.8}$$

Again, the PWM signals of phase 2 should have a time shift of $T_\mathrm{s}/2$ compared to phase 1. This is accomplished by setting the output mode of the upper switch to toggle/set and the lower switch to toggle/reset. The corresponding count values are calculated using (6.9)- (6.10).

$$\mathrm{CCR3} = \mathrm{CCR0} - \mathrm{CCR1} \tag{6.9}$$

$$\mathrm{CCR4} = \mathrm{CCR0} - \mathrm{CCR2} \tag{6.10}$$

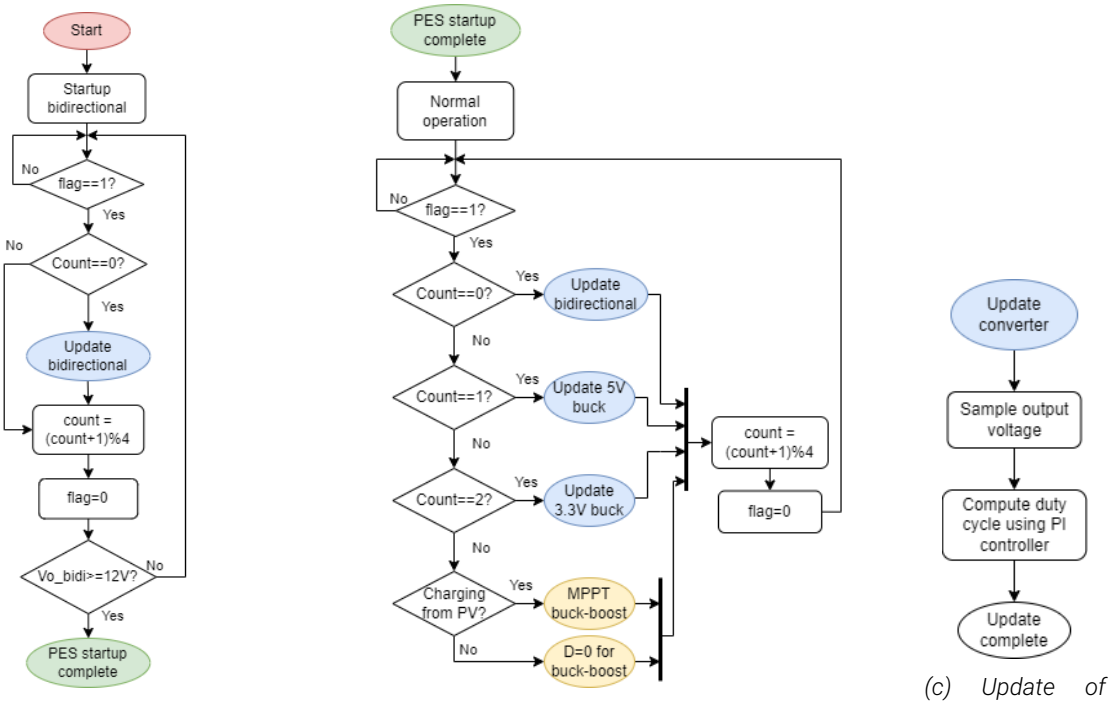
Figure 6.7 shows the resulting PWM signals of the half-bridge of phases 1 and 2. A dead time of 800 ns seconds is used for illustration purposes. The dead time between the upper and lower switches is maintained. Furthermore, a time delay of $T_\mathrm{s}/2$ is implemented between the switches of phase 1 and phase 2.

6.2.4 Program Flow

The flow chart of the microcontroller is shown in Figure 6.8. It consists of two main routines, startup and normal operation. First, when the batteries are connected, the PES needs to start up. The bidirectional converter needs to regulate the bus voltage to 12 V, while the 5 V and 3.3 V buck converter and the buck-boost converter remain off. This is shown in Figure 6.8a. After the bus voltage has been reached, the startup of the PES is completed and the LDOs are turned off. The controller goes to normal operation, given by the flowchart of Figure 6.8b. An interrupt service routine periodically sets the flag to 1 to update a converter. It runs at 32kHz to achieve an update frequency of 8kHz for each converter. Using the count variable, only one converter is updated each time. Finally, the program flow of updating the bidirectional and both buck converters is shown in Figure 6.8c. The output voltage is sampled, and the duty cycle is calculated using the PI controller of the corresponding converter. The MPPT algorithm is executed for the buck-boost converter if the rover is charging, else the converter is disabled by setting the duty cycle to zero. The MPPT algorithm flowchart is shown in Figure 6.9 and will be discussed in Section 6.3.

6.3 MPPT Algorithm Buck-Boost Converter

The power generated from the PV panel depends on the irradiance received and temperature of the PV panel. Thus, to generate maximum power under different conditions, a MPPT algorithm is needed. Two common used MPPT algorithms are Perturb & Observe (P&O) and hill climbing [128, 129]. The former introduces a perturbation in the operating voltage of the PV panel, while the latter introduces a perturbation in the duty cycle of the converter. They are known for their simple and low-cost implementation, especially the hill climbing algorithm. Their main disadvantage is that they oscillate around the MPP point. In [128]



(a) Startup PES. *(b) Normal operation.* *(c) Update of each converter.*

Figure 6.8: Flow charts of the startup, normal operation, and update of the converters of the PES.

is shown that (P&O) has a faster response time than hill climbing. A fast dynamic response is required for a grid-connected PV system. However, for a battery charging system, the dynamic response time can be slow. Furthermore, no change in irradiance is expected when charging the batteries since there is no atmosphere on the moon. Hence, hill climbing is adopted as the MPPT algorithm.

The hill climbing algorithm is shown in Figure 6.9. It introduces a perturbation in the duty cycle. Depending on the change in power and voltage, the controller determines if the duty cycle must be increased or decreased to locate the MPP operating point. For example, when both the change in power and voltage is positive, the controller must follow the trend of increasing the input voltage. Thus, from (6.11) follows that the duty cycle must be decreased. This equation shows the relation between the input voltage, output voltage, and duty cycle of the buck-boost converter.

$$V_{\text{in}} = \frac{(1-D)V_{\text{o}}}{D} \tag{6.11}$$

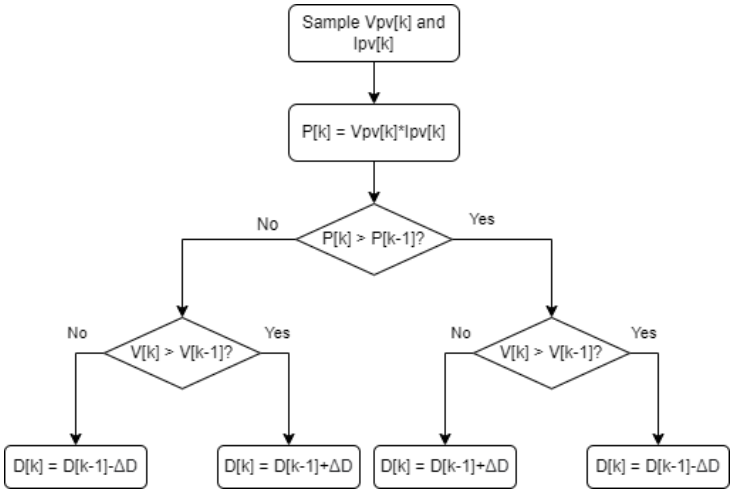


Figure 6.9: Hill climbing MPPT algorithm [129].

For the hill climbing algorithm the change in duty cycle ΔD is fixed. A tradeoff between fast dynamic response and low steady-state oscillations exists. By reducing ΔD, the dynamic response is slower but the controller exhibits lower oscillations in steady state. Since the dynamic response can be slow, a low perturbation value of ΔD=0.001 is used to obtain low steady-state oscillations.

The results of the MPPT simulation are provided in Figure 6.10. The simulation model used is elaborated in Appendix D.2.3. The initial irradiance of the PV panel is set to its maximum value of 1350 W/m^2, and is decreased to 500 W/m^2 at 0.03 s. Initially, the input capacitors connected to the PV panel are discharged, and the initial duty cycle is set to 0.35. At the start of the simulation the PV panel voltage increases because the input capacitors are charged from the current generated by the PV panel. The duty cycle decreases since both voltage and power increase. When the voltage has reached 16 V the MPP has been exceeded and the generated power drops to 10 W. The duty cycle starts to increase the moment the power starts to drop and keeps increasing until the MPP has been reached again after 0.022 s. Small oscillations of the duty cycle and PV voltage and current are visible. However, the power generated is almost constant with a ripple of 25 mW. Then, at 0.03 s, the irradiance is decreased to 500 W/m^2. After approximately 0.025 s, at t=0.055 s, the MPP has been reached again and a constant power of 7.16 W is generated. The ripple in the generated power is 1.8 mW. Thus, the MPPT algorithm can track the MPP under increasing and decreasing irradiances in a relatively fast time with a negligible power ripple.

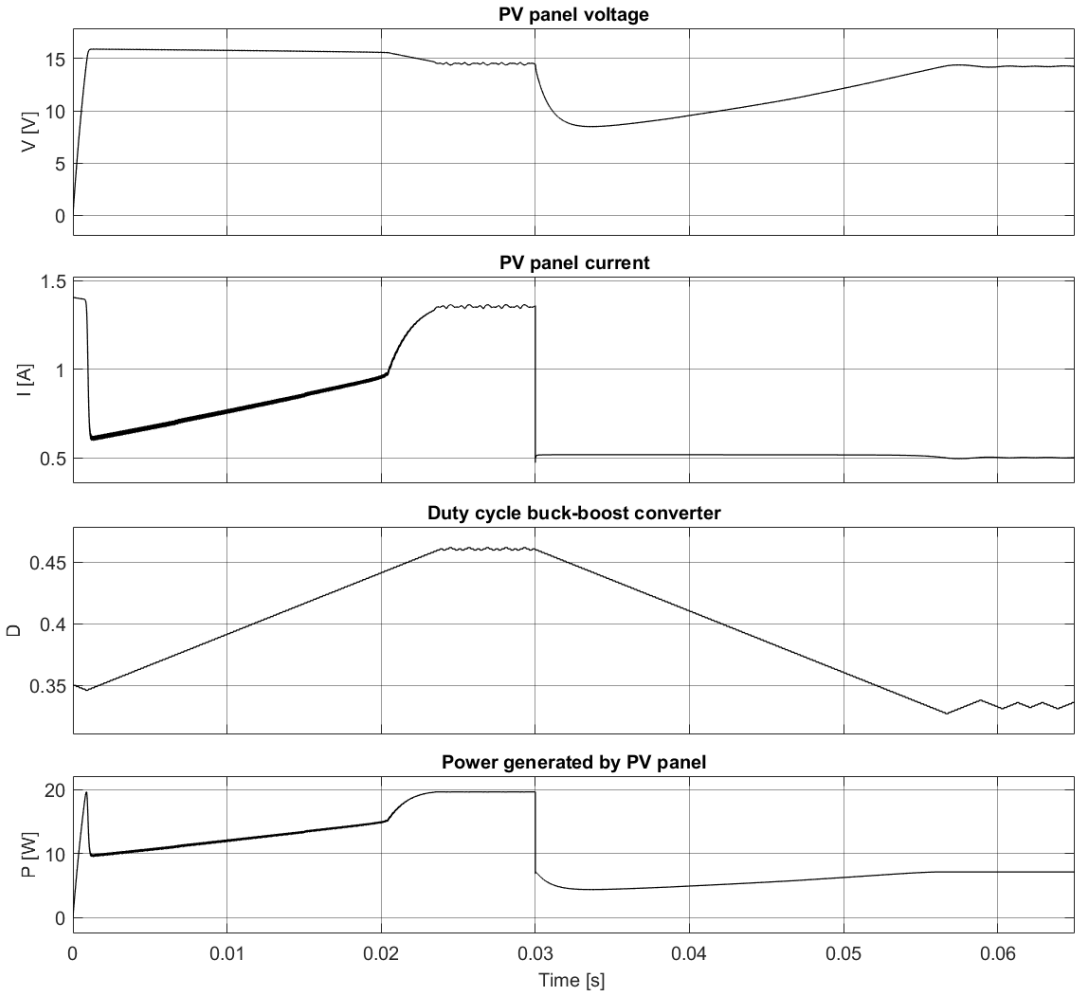


Figure 6.10: Simulation of the MPPT algorithm of the interleaved buck-boost converter.

Chapter 7

Simulations of the Complete Power Electronic System

In Chapters 5 and 6 each of the interleaved converters and their control are simulated individually. In the simulations of the interleaved buck and buck-boost converters, the DC bus was assumed to be an ideal voltage source having the DC bus voltage. However, the actual DC bus voltage fluctuates since it is regulated by the bidirectional converter. Further, the load of the bidirectional converter was assumed to be resistive while in reality, two buck converters are present as load as well. In this chapter simulations of the complete PES are done where all interleaved converters are connected to the DC bus. In this way is verified if the converters perform similarly to their individual simulations and if stability is retained. Three simulations are performed representing the three different scenarios for the PES. First, the PES during startup is simulated in Section 7.1. Next, in Section 7.2 the voltage regulation of the converters is simulated under changing load conditions. Finally, charging the batteries from the PV panel is simulated in Section 7.3. This simulation verifies the MPPT of the buck-boost converter and demonstrates the bidirectional power flow capability of the bidirectional converter.

7.1 Startup of the Power Electronic System

During startup of the PES the 5 V and 3.3 V outputs are regulated by the LDOs instead of the interleaved buck converters. When the bidirectional converter has regulated the bus voltage to 12 V, the LDOs are disabled and the buck converters are enabled. The load resistors are set as constant such that the output currents are 0.5 A at nominal voltages. Appendix D.4 gives a detailed description of the simulation model used. In Figure 7.1 the plot of the output voltages of the interleaved bidirectional converter, and the 5 V and 3.3 V interleaved buck converters are shown. Initially, all capacitors are discharged. However, the charging behaviour of the output capacitors of the buck converters is not shown. They charge almost instantaneously because they are connected to ideal voltage sources representing the LDOs. A small drop in output voltage for the 5 V buck converter occurs until t=0.33 ms. This is due to the output voltage being larger than the input bus voltage, therefore the body diode of the switch conducts. When the bus voltage has exceeded 5 V, the body diode stops conducting and the 5 V output voltage is constant. The same discussion holds for the small initial voltage drop at the 3.3 V buck converter.

The output voltage of the bidirectional converter increases to its reference without overshoot in 2.9 ms. At this moment the 5 V and 3.3 V bucks are enabled, where a small drop in output voltage is visible. This drop is due to a small mismatch between the calculated initial duty cycle with the actual duty cycle required. The outputs of the 5 V and 3.3 V buck converters are regulated to their reference value with small oscillations. Similarly, the bidirectional converter has only minor oscillations when it reaches its reference of 12 V, visible in the zoomed-in plot of the bidirectional output voltage.

Note that a feedforward scheme is used for the two buck converters when transiting power from the LDOs to the buck converters. The initial duty cycle is calculated based on the output current at the moment the converter is enabled. Without this feedforward scheme, a significant drop in output voltage occurs. If the output current of the corresponding converter is too large at the moment the converter is enabled, the drop in output voltage can exceed the minimum voltage of the microcontroller or gate drivers. Then, an endless loop occurs consisting of startup, enabling the buck converters, and shutdown of the microcontroller and/or gate drivers due to undervoltage.

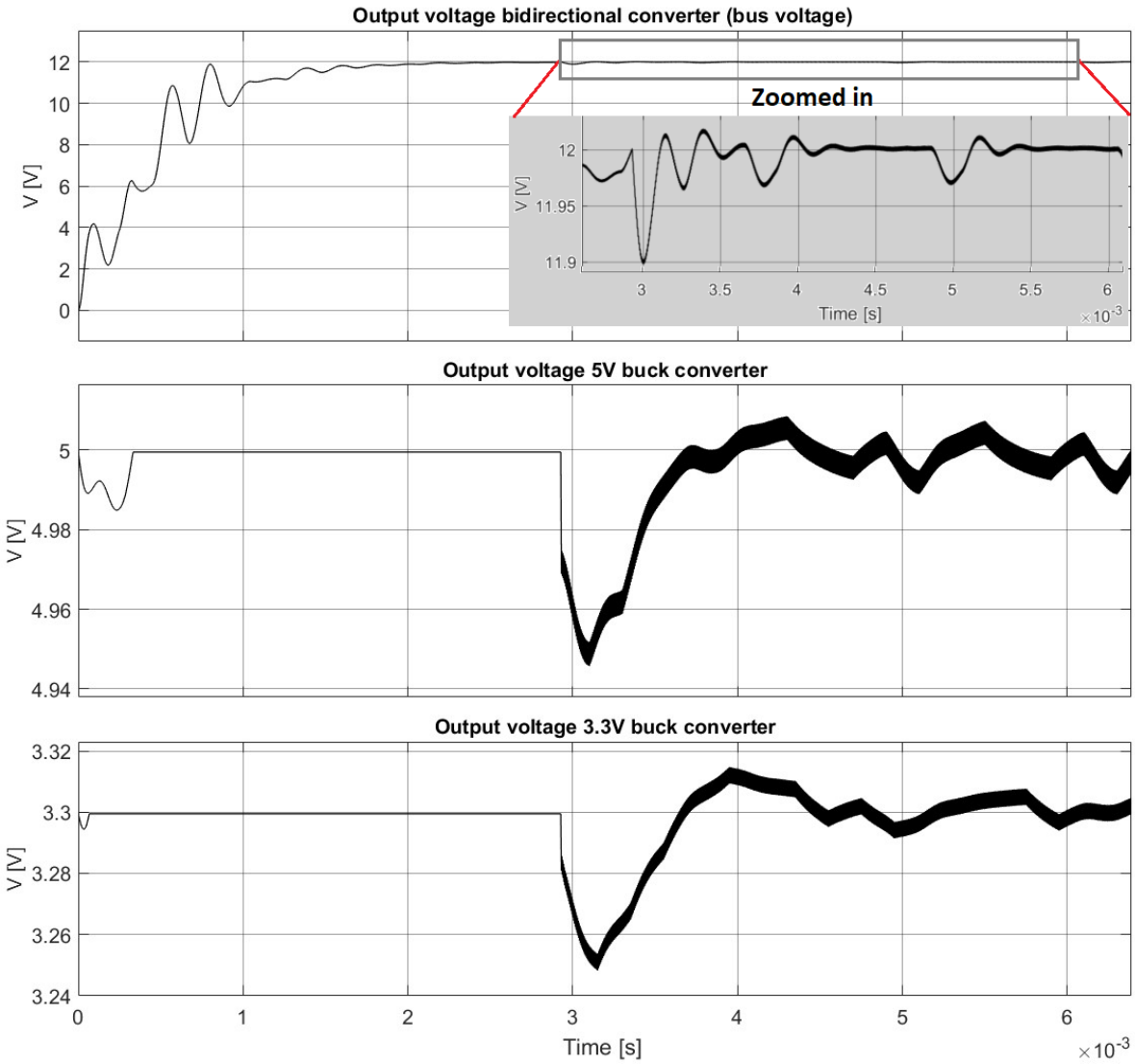


Figure 7.1: Output voltages of the interleaved bidirectional, 5 V buck, and 3.3 V buck converters during startup of the PES.

7.2 Voltage Regulation of the Interleaved Converters

In this simulation all simulations from Section 6.1 are combined. The output voltage regulation of the 5 V and 3.3 V buck converters and bidirectional converter under increasing load is simulated when they are connected to the DC bus. The load of the 12 V output, 5 V buck and 3.3 V buck converters are increased exponentially from 1 A to 4 A in 10 ms at t = 3 ms, see Figure D.10 for the exact waveform of each of the outputs. The resulting plot of the output voltages is shown in Figure 7.2. The bidirectional converter can keep its output to its reference of 12 V with small ripples, with a voltage ripple of approximately 0.625% in steady state. These ripples are more significant than in Section 6.1, caused by the buck converters connected to the bus in this simulation. Due to their nonlinear switching behaviour, the current drawn from the output of the bidirectional converter is not constant as opposed to the simulation in Section 6.1.

The 5 V buck converter has a similar transient response compared to the simulation in Section 6.1. The output voltage drops until 4.9 V, after which it is stabilised. However, more ripples occur, especially after the reference has been reached. This is due to the ripple present in the bus voltage. In steady state, the output voltage ripple is approximately 0.79%. The same discussion holds for the 3.3 V buck converter. Its output voltage drops to 3.23 V, after which it is stabilised and the ripple in steady state is 0.61%. Thus, it can be concluded that their voltage ripple is less than the intended 1%. Finally, it is observed that stability of each converter is maintained. Therefore it can be concluded that the voltage regulation of the output

voltages by the bidirectional, 5 V, and 3.3 V interleaved converters performs adequately and is similar to the simulations of the individual converters.

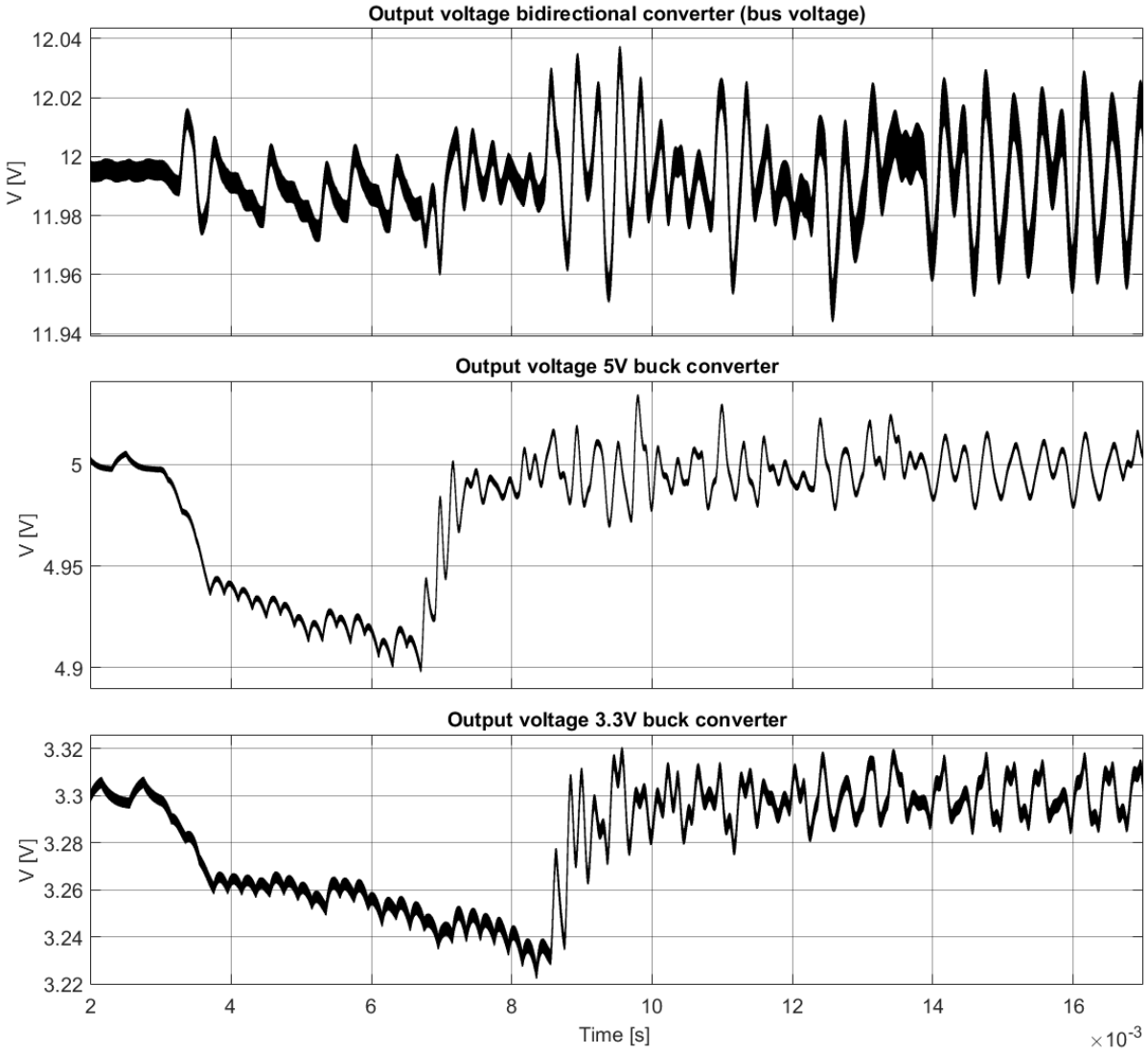


Figure 7.2: Output voltage regulation of the buck converters and bidirectional converter when connected.

7.3 Charging the Batteries From PV Panel

Similar to the MPPT simulation from Section 6.3, for this simulation the initial irradiance is 1350 W/m^2 and is decreased to 500 W/m^2 at t=0.25 s. Similarly, the initial input capacitors are discharged, and the initial voltage of the output capacitors is set at the bus voltage of 12 V. The output currents of the 12 V, 5 V, and 3.3 V outputs are 0.35 A, resulting in a total power dissipation of 7.11 W. Figure 7.3 shows the results of the simulation. The initial duty cycle is set at 0.35 and does not correspond to the MPP operating point. The MPPT algorithm finds the MPP after 0.022 s. After the irradiance drops to 500 W/m^2 at t=0.025 s, the MPPT algorithm again locates the MPP operating point. Therefore, it can be concluded that the MPPT algorithm works when all subsystems are connected. Further, the bus voltage remains regulated to its reference of 12 V with some oscillations.

When the irradiance is 1350 W/m^2, the average output current of the bidirectional converter is negative. This is expected, since the power generated by the PV panel P_{pv}>10 W while the total power at the loads is 7.11 W. Thus, power flows from the bus to the battery. When the irradiance drops to 500 W/m^2 the power generated by the PV panel drops to 4.5 W. At this point, the average output current of the bidirectional converter is positive. Thus, bidirectional power flow is achieved. The output current of the bidirectional

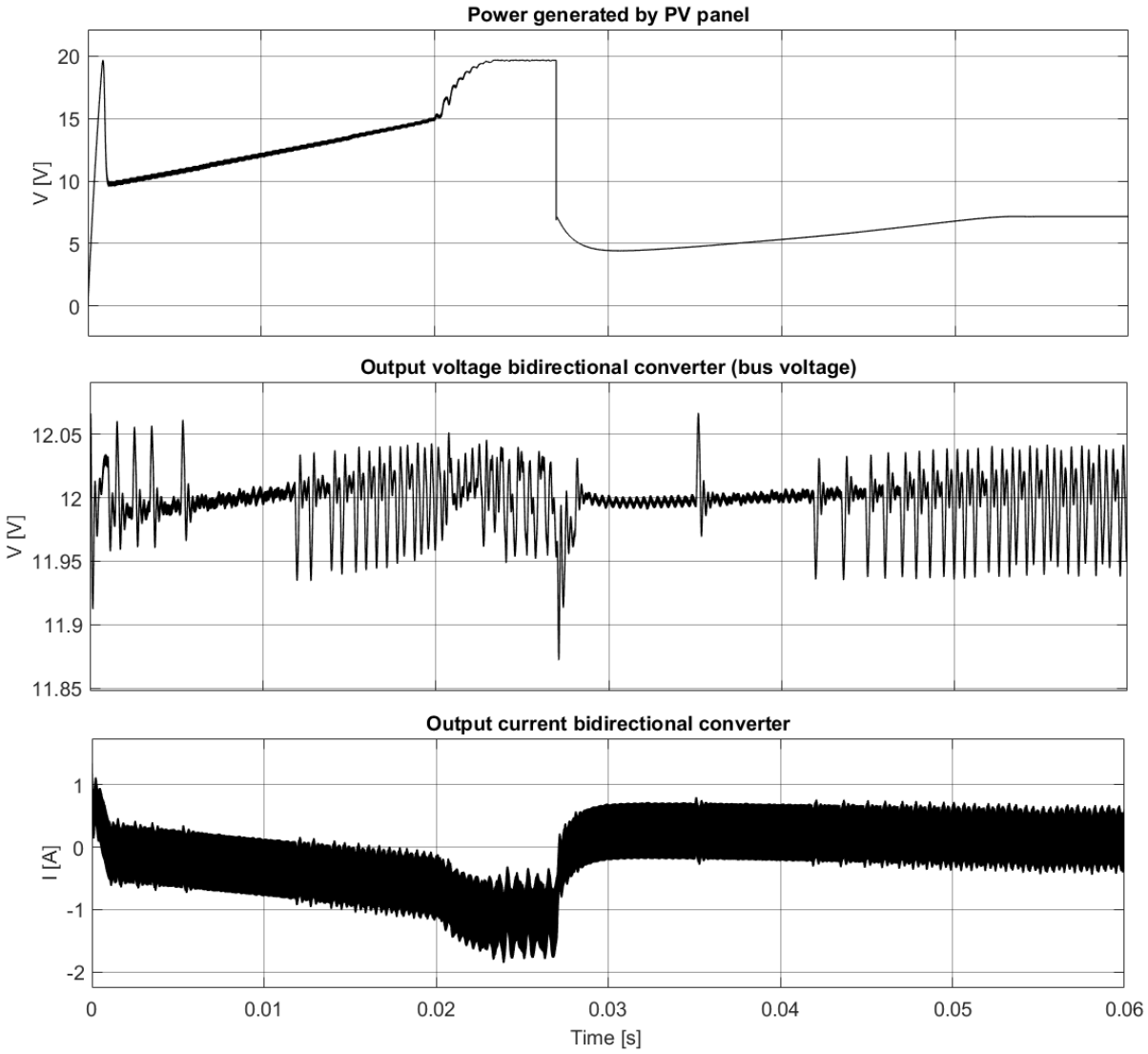


Figure 7.3: Simulation results of the MPPT algorithm and bidirectional power flow of the complete PES.

converter shows a relatively large ripple of 0.9 A. In the derivation of Chapter 5 was assumed that the output current of each converter is constant at constant load. Though the load is constant in this simulation, the load is not resistive only but consists of the buck converters as well. Only when a switch of the buck converters is closed current is drawn from the bidirectional converter. Therefore, a non-zero output current ripple of the bidirectional converter occurs due to the switching behaviour of the buck converters.

Chapter 8

Experimental Results Prototype

The design and efficiency of each interleaved converter were elaborated in Chapter 5, and their expected operation was verified through simulations. Furthermore, Chapter 6 provided the voltage control design and program flow on the microcontroller, together with the dynamic performance of each controller under changing load conditions. Finally, in Chapter 7 the complete PES was simulated where all converters are operated simultaneously. To verify the design of the PES and the simulations performed, a prototype of the PES has been developed. This chapter provides the measurements on the prototype to provide experimental verification of the PES design and the simulations conducted. First, in Section 8.1, the prototype and measurement setup are presented. Next, Section 8.2 provides the steady-state measurements. Finally, Section 8.3 provides the dynamic performance of the 5 V buck and bidirectional converter.

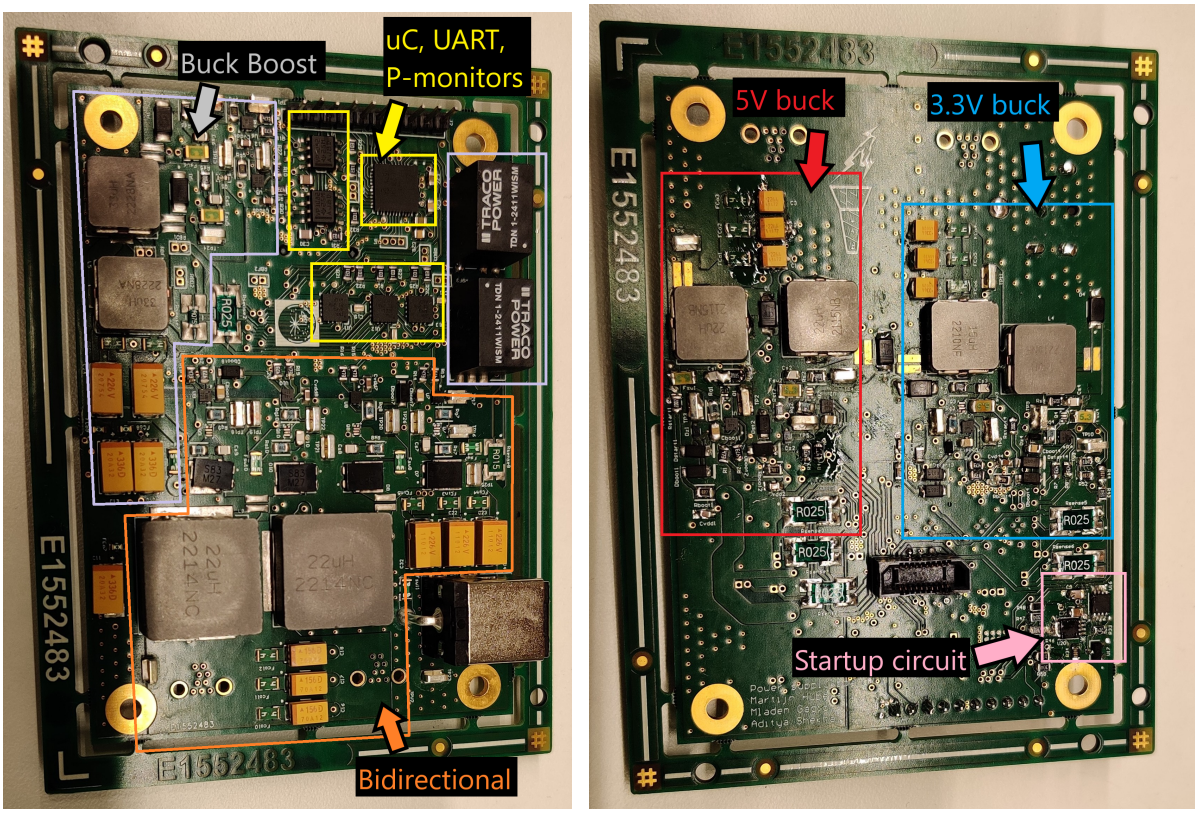
8.1 Prototype and Measurement Setup

A two-sided, six-layered Printed Circuit Board (PCB) has been developed for the prototype PES, having a size of 95 mm by 68 mm. In Figure 8.1a, the front side of the PCB is shown, which contains the interleaved buck-boost and bidirectional converters, microcontroller, UART chips, and INA3221 power monitors. The back side is shown in Figure 8.1b, which contains the interleaved 5 V and 3.3 V buck converters, and the startup circuit. The PES prototype functionalities are measured using the following sources, loads, and measurement equipment:

- DC power supply 1: Delta Elektronika EST 150 Series: Two outputs with [0 V, 20 V] and [0 A, 2.5 A], one output with [0 V, 10 V] and [0 A, 5 V]. This supply is used for supplying power to the 5 V and 3.3 V outputs when the corresponding converters are not operated, as well as the bus voltage when the bidirectional converter is not operated.
- DC power supply 2: Delta Elektronika ES030-10 Series: 1 output with [0 V - 30 V] and [0 A, 10 A]. This source is used for supplying the battery power at the input of the bidirectional converter.
- DC loads: 2x Elektro-Automatik EA-EL 3400-25 electronic load series. Resistance ranges from [0 Ω, 400 Ω] and has a power rating of 400 W. These are used as fixed loads for the steady state measurements of the converters and as the dynamic load for the dynamic load performance measurements.
- Oscilloscope: Yokogawa DLM3034.
- Voltage probe: Keysight Technologies N2791A differential probe.
- Current probes: Keysight Technologies N2782B snap-on probe.

8.2 Steady State Measurements

In this section, the measured steady-state performance of the converters at maximum load is presented. Each of the converters has been tested in interleaved mode and single-phase mode. The interleaved bidirectional and 5 V buck converter have been tested in closed-loop control using the digital voltage controller from Section 6.2, while the buck-boost converter and 3.3 V buck converter have been tested in open-loop control only. Due to time limitations, the 3.3 V buck has not been operated in closed-loop control and no measurements of the buck-boost converter utilising the PV panel have been carried out. In the steady-state measurements, only one converter is operated at a time.



(a) Front side. *(b) Back side.*

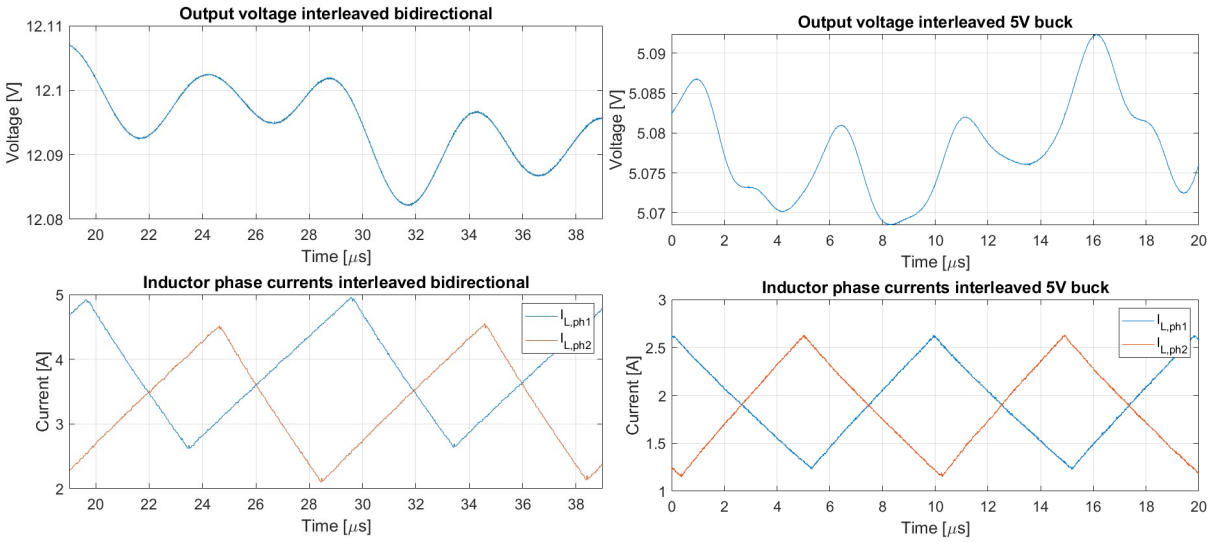
Figure 8.1: Prototype PCB of the Power Electronic System.

8.2.1 Interleaved Bidirectional and 5V Buck in Closed Loop Control

The measured voltage and inductor phase currents of the interleaved bidirectional converter are shown in Figure 8.2a. The ES030-10 is used as the input voltage source and is set at 21 V, and the EA-EL 3400-25 DC load is set at 1.59 Ω. Similarly, The measured output voltage and inductor phase currents of the interleaved 5 V buck converter are shown in Figure 8.2b. The DC load is set to 1.25 Ω. For both the bidirectional and 5 V buck converter, the output voltage is slightly higher than its reference. Further, it is observed that the frequency of the output voltage ripple is 200 kHz, which is twice the frequency of the switching frequency and hence the inductor current ripples. Thus, it is experimentally validated that the frequency of the output voltage ripple is increased by the number of phases N, which was stated in Section 2.2.3.

The average currents in the two inductors of the 5 V buck converter are almost equal. However, for the bidirectional converter, the average inductor current from phase one $I_{\text{L,ph1}}$ is 0.43 A larger than $I_{\text{L,ph2}}$. This shows the current sharing issue that arises with practical interleaved converters [130]. Due to a small mismatch between the phase inductances, the current between the two phases is shared unequally. The inductors used have a tolerance of ±20%. This problem can be circumvented by implementing current control, for example using average current control or by the duty cycle matching method [131, 132].

Table 8.1 provides the measured voltage ripples, current ripples, and power and efficiency measurements of the interleaved bidirectional and 5 V converter. These values are measured for interleaved operation and single-phase operation. Several differences are observed by comparing interleaved operation with single-phase operation. First of all, for the bidirectional converter, the average output voltage $V_{\text{o,av}}$ is 0.1 V above its reference for interleaved mode of operation. For single-phase mode, $V_{\text{o,av}}$ is 0.2 V above its reference. Thus, interleaved mode results in a regulated voltage that is closer to its reference. The same is observed for the 5 V buck converter. Interleaved operation results in a regulated voltage 0.1 V above its reference, while for single-phase operation 0.13 V above its reference. The small mismatch between the regulated voltage and reference is due to a small inaccuracy in the measured voltage. This is caused by the combination of quantisation error due to the 8-bit Analog-to-Digital Converter (ADC) and the conversion from floating point to fixed point representation in the control loop. The maximum quantisation error voltage $V_{\text{q,e}}$ of the



(a) Bidirectional converter. *(b) 5 V buck converter*

Figure 8.2: Measured steady state operation of the interleaved converters in closed-loop control.

ADC is defined as half of the Least Significant Bit (LSB), given by (8.1). Here, V_{ref} = 2.5 V is the reference voltage of the ADC, and n = 8 the number of bits.

$$V_{\text{q,e}} = \pm \frac{V_{\text{ref}}}{2^{n+1}} \tag{8.1}$$

Further, the resolution of the fixed point $V_{\text{fp,e}}$ is 7.81 mV. Because of the voltage divider attenuation R_{div}, the actual error in output voltage measured is increased by a factor R_{div}. The resulting error in measured voltage is calculated using (8.2). Thus, the observation that the voltage is regulated 100 mV higher than the reference is reasonable considering noise also deteriorates the accuracy of the voltage measurements.

$$V_{\text{o,e}} = (V_{\text{q,e}} + V_{\text{fp,e}})R_{\text{div}} = \begin{cases} (4.88 + 7.81) \cdot 10^{-3} \cdot 3.52 = \pm 44.67 \,\text{mV for the 5 V buck} \\ (4.88 + 7.81) \cdot 10^{-3} \cdot 6.67 = \pm 84.64 \,\text{mV for the bidirectional} \end{cases} \tag{8.2}$$

The second observation from Table 8.1 is that the duty cycle D for single-phase mode is larger than for interleaved mode. For the bidirectional converter, D is 0.005 higher in single phase mode, while 0.029 higher for the 5 V buck converter. As a result, the inductor current ripple ΔI_{L} is also larger for single-phase mode. For interleaved mode, $\Delta I_{\text{L,ph1}} \neq \Delta I_{\text{L,ph2}}$ due to a mismatch in the inductance of the two phases.

Third, the output voltage ripple ΔV_{o} for interleaved mode is decreased significantly compared to single-phase operation. The voltage ripple is measured at the largest transition from a peak to a valley during one switching period, or vice versa. This occurs, for example, at $t \approx 29\,\mu s$ and $t \approx 32\,\mu s$ for the bidirectional converter from Figure 8.2a. For the bidirectional converter, ΔV_{o} is decreased by a factor of 2.5, while for the 5 V by a factor of 8.54. Thus, it is experimentally verified that the interleaved converters have the advantage of decreased output voltage ripple compared to single-phase converters.

Finally, the efficiency for interleaved mode is higher than for single-phase mode. The efficiency of the bidirectional converter is only 0.05% larger in interleaved mode, while the efficiency of the 5 V buck converter is 2.90% higher in interleaved mode. Thus, this confirms the advantage of interleaved converters in terms of efficiency improvement compared to single-phase converters due to current sharing in the phases of the interleaved converters.

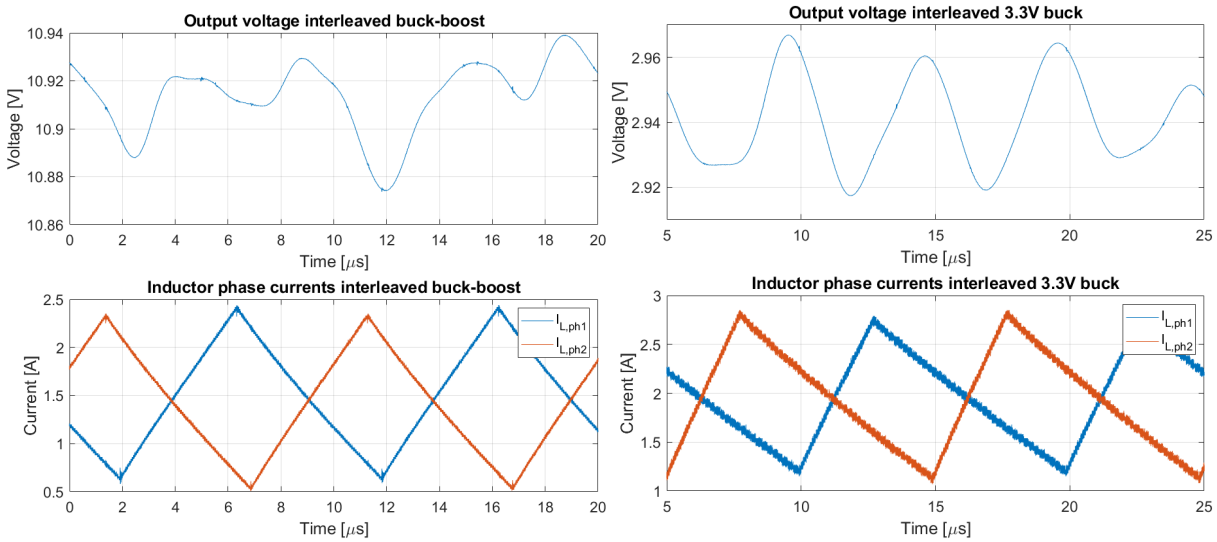
8.2.2 Interleaved Buck-Boost and 3.3V Buck in Open Loop Control

The measured steady-state output voltage and inductor phase currents of the interleaved buck-boost and 3.3 V buck converter operated in open-loop are shown in Figure 8.3a and 8.3b, respectively. For the buck-boost converter, the EST 150 is used as the input source at 15.1 V, and the EA-EL 3400-25 DC load is set at

Table 8.1: Measured steady-state characteristics of the interleaved bidirectional and 5 V buck converter.

		$V_{o,av}$	D	ΔI_L	ΔV_o	P_o	P_{in}	η
Bidirectional	**Int**	12.10 V	0.613	Ph1: 2.32 A Ph2: 2.42 A	0.54%	90.48 W	100.17 W	90.33%
	1ph	12.20 V	0.618	2.64 A	1.36%	84.18 W	93.24 W	90.28%
5V buck	**Int**	5.10 V	0.465	Ph1: 1.40 A Ph2: 1.46 A	0.39%	19.79 W	22.44 W	88.19%
	1ph	5.13 V	0.494	1.53 A	3.33%	20.06 W	23.52 W	85.29%

6.89 Ω.This mimics the MPP operation of the PV panel. For the 3.3 V buck, the DC load is set at 825 mΩ. Similar observations as for the interleaved bidirectional and 5 V buck converter are made: the frequency of the output voltage ripple is twice the frequency of the inductor current ripple, and the inductors show unequal current sharing. The main difference is that the average output voltage is lower than intended. The converters are operated in open loop using the ideal duty cycle calculated in Section 5.1. However, because the converters have losses, the actual output voltage is lower than the ideal input-to-output voltage ratio.



(a) Buck-boost converter. *(b) 3.3 V buck converter*

Figure 8.3: Measured steady state operation of the interleaved converters in open-loop control.

The measured voltage ripples, current ripples, and power and efficiency measurements of the interleaved buck-boost and 3.3 V buck converter are provided in Table 8.2. These values are measured for interleaved operation and single-phase operation. The following observations are made by comparing the two modes of operation. First of all, though the duty cycle is equal, the average output voltage $V_{o,av}$ for interleaved operation is higher than for single-phase operation. This indicates that the efficiency of interleaved operation is higher than for single-phase operation. This is confirmed by the efficiency measurements. The efficiency of the buck-boost converter is 3.56% higher in interleaved mode than in single-phase mode, while the efficiency of the 3.3 V buck is 4.28% higher in interleaved mode.

Second, the current ripple ΔI_L is larger for single-phase operation than for interleaved operation. The output voltage in single-phase operation is lower, increasing the voltage across the inductor. From (5.17) and (5.8), this increases the current ripple. Further, $\Delta I_{L,ph1} \neq \Delta I_{L,ph2}$ due to a mismatch in the inductance of the two phases, which is more prominent for the 3.3 V buck. Finally, the output voltage ripple ΔV_o is reduced significantly for interleaved operation. For the buck-boost converter, ΔV_o is reduced by a factor of 2.90 in interleaved operation compared to single-phase operation, while the 3.3 V buck a reduction of 2.31 is achieved. However, ΔV_o of the 3.3 V buck converter is 0.68% above the designed 1% ΔV_o.

8.2.3 Comparison Measurements With Calculations

In Section 5.3 was shown that the calculated output voltage ripples and RMS currents are close to the simulated values, both for interleaved and single-phase operation. Therefore, only the calculated output

Table 8.2: Measured steady-state characteristics of the interleaved buck-boost and 3.3 V buck converter.

		$V_{o,av}$	D	ΔI_L	ΔV_o	P_o	P_{in}	η
Buck-boost	**Int**	10.92V	0.446	Ph1: 1.78 A Ph2: 1.80 A	0.51%	17.25 W	21.14 W	81.60%
	1ph	10.28 V	0.446	1.89 A	1.48%	15.32 W	19.63 W	78.04%
3.3V buck	**Int**	2.94 V	0.277	Ph1: 1.54 A Ph2: 1.71 A	1.68%	11.50 W	13.68 W	84.06%
	1ph	2.74 V	0.277	1.68 A	3.88%	11.01 W	13.80 W	79.78%

voltage ripple and efficiency of each converter are compared to the measured values to provide experimental validation of the models derived and simulations performed for the output voltage ripples and converter efficiencies.

Output Voltage Ripple

The calculated and measured output voltage ripples of the converters operating in interleaved and single-phase mode are provided in Table 8.3. In general, the measured voltage ripples are larger than the calculated ripples, both for interleaved and single-phase operation. In the calculations, the assumption was made that the components are ideal. However, in the real converters, the components have a finite parasitic resistance and inductance. In [133] is shown that the Equivalent Series Resistance (ESR) of the output capacitors can increase the output voltage ripple significantly.

Table 8.3: Calculated and measured output voltage ripples.

	Bidirectional		**Buck-boost**		**5V buck**		**3.3V buck**	
	Int	**1ph**	**Int**	**1ph**	**Int**	**1ph**	**Int**	**1ph**
$\Delta V_{o,calc}$	0.07%	0.54%	0.06%	0.56%	0.07%	0.50%	0.19%	0.50%
$\Delta V_{o,meas}$	0.17%	1.36%	0.51%	1.48%	0.39%	3.33%	1.68%	3.88%

For the bidirectional converter, the measured voltage ripple is increased by a factor of approximately 3, both for single-phase and interleaved mode of operation. Similarly, the measured ripple for the 5 V buck converter is increased by approximately 6, and for the 3.3 V buck by approximately 8 both for interleaved and single-phase mode of operation. The difference in ripple of the buck-boost converter is larger, where the measured ripple in interleaved mode is increased by a factor of 9, while for single-phase by a factor of 3. Since this is still in the same order of magnitude, it can be concluded that the calculations and simulations of the voltage ripples are correct under the assumption that the components are ideal.

Efficiency Interleaved Operation

The calculated and measured efficiencies of the converters operating in interleaved mode are provided in Table 8.4. In general, the measured efficiency is slightly lower than the calculated efficiency. For all converters, there are several sources of additional losses that are not considered in the efficiency calculations. First of all, the losses in the snubber network are not considered. Second, the losses in the bootstrap startup resistor and diode are present during all efficiency measurements. Third, the power dissipation of the gate drivers is not considered, as well as the power dissipation of the microcontroller. Fourth, the resistor divider networks used for measuring the voltages using the microcontroller also draw a small amount of power. Finally, the PCB traces have finite resistance, introducing additional losses. In addition, the losses in the output capacitor are increased compared to the calculations. The RMS currents in the capacitors are larger than calculated because the measured voltage ripple is larger than calculated, hence the conduction losses due to the ESR are increased. These factors combined result in a reduction of 3.01% and 3.44% in the measured efficiency compared to the calculated efficiency for the 5 V and 3.3 V buck converters, respectively. Similarly, a reduction of 3.90% in measured efficiency is observed for the buck-boost converter.

The measured efficiency of the bidirectional converter is reduced by 5.57% compared to the calculated efficiency. In the efficiency measurement, the startup circuit is used to power the gate drivers and microcontroller. Since the LDOs of the startup circuit are very inefficient due to the large voltage drop (21 V to 5 V and 3.3 V) with an output current around 100 mA, a drop of 5% in efficiency can be expected. Further,

Table 8.4: Calculated and measured efficiencies of interleaved operation.

	Bidirectional	5V buck	3.3V buck	Buck-boost
η_{calc}	95.9%	91.20%	87.50%	85.50%
η_{meas}	90.33%	88.19%	84.06%	81.60%

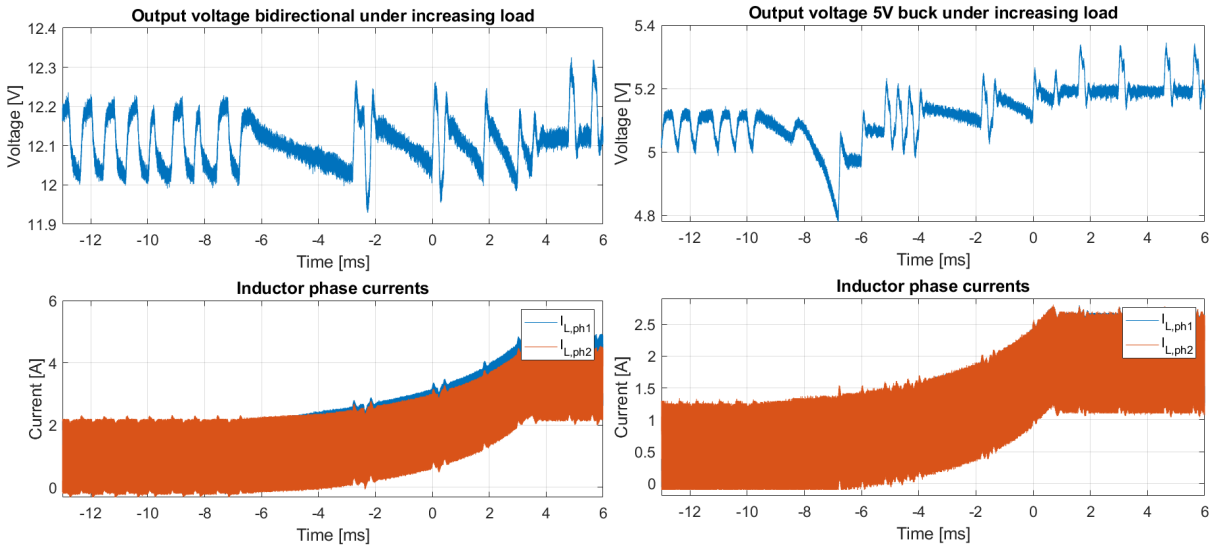
the isolated DC/DC converters for the gate drivers of the buck-boost converter are powered, increasing the power drawn from the 21 V input source. On the other hand, the bidirectional converter is operated in synchronous rectification while in the calculations the freewheeling diode was used. From Section 5.5, the losses in the diodes consist of 2% of the total losses, while the losses in the switch are negligible. Thus, this increases the measured efficiency by 2%. With all the aforementioned reasons, a reduction of 5% in efficiency can be expected. By disabling the startup circuit and powering the 5 V and 3.3 V by external voltage sources, a significant improvement in measured efficiency is expected.

8.3 Dynamic Load Performance

First, the voltage regulation capability of the interleaved 5 V and bidirectional converter with increasing load is elaborated when operated individually, corresponding to the simulations in Section 6.2.2. Next, their performance is evaluated when they are operated simultaneously with increasing load, which corresponds to the simulation of Section 7.2.

8.3.1 Standalone Operation

The measured voltage regulation of the interleaved bidirectional converter is shown in Figure 8.4a. Initially, the voltage is regulated to an average of 12.1, V and shows steady-state ripples similar to the simulation from Section 6.2.2. Furthermore, the inductor currents become negative, thus the converter operates at forced CCM. Then, at t = -7 ms, the load is changed from R_L = 6 Ω to $R_{L,max}$ = 1.59 Ω in Δt = 10 ms. Similar to the simulation in Figure 6.5, the output voltage is regulated close to its reference with only small drops and oscillations. When the load has reached its maximum, steady-state operation is maintained at a regulated voltage of 12.1 V, showing periodic oscillations similar to the simulation in Figure 6.5. However, the inductor currents show unequal current distribution where $I_{L,ph1} > I_{L,ph2}$, similar to the steady state measurements in Section 8.2. Thus, it can be concluded that the voltage controller of the bidirectional converter can regulate its output voltage for a load increasing from 26% to 100% of its rated value in 10 ms.



(a) Bidirectional converter. *(b) 5 V buck converter*

Figure 8.4: Measured voltage regulation capability under increasing load.

The voltage regulation of the 5 V buck converter, shown in Figure 8.4b, also resembles the simulation from Section 6.2.2, shown in Figure 6.2. The DC load is changed from R_L = 5 Ω to $R_{L,max}$ = 1.25 Ω in Δt = 10ṁs.

Three main differences between the simulation and measurements are observed. The first difference is in the initial steady-state, where oscillations are measured but not shown in the simulation. These oscillations are expected due to undersampling of the output voltage ripple. Second, the maximum measured drop in output voltage that occurs at t = -7 ms is 0.2 V larger than for the simulation, indicating that the transient response of the controller is slower for the implemented converter than for the simulated converter. Finally, the measured output voltage at maximum load is regulated 0.1 V higher than at the initial load.

8.3.2 Interleaved Bidirectional and 5V Buck Operated Simultaneously

The final experiment that is conducted is operating the interleaved bidirectional and 5 V buck converter in closed-loop control simultaneously under dynamic load. This corresponds to the simulation performed in Section 7.2 without the 3.3 V buck converter. The measured output voltages of the bidirectional and 5 V buck are shown in Figure 8.5. This figure also provides the inductor current of phase 2 of the 5 V buck converter to show the change in load profile. In this experiment, the DC load of the 12 V output is changed from 24 Ω to 3 Ω in Δt =6 ms, corresponding to I_o = 0.5 A and 4 A, respectively. Similarly, the load of the 5 V output is changed from 5 Ω to 1.25 Ω in Δt = 6 ms, corresponding to I_o = 1 A and 4 A, respectively.

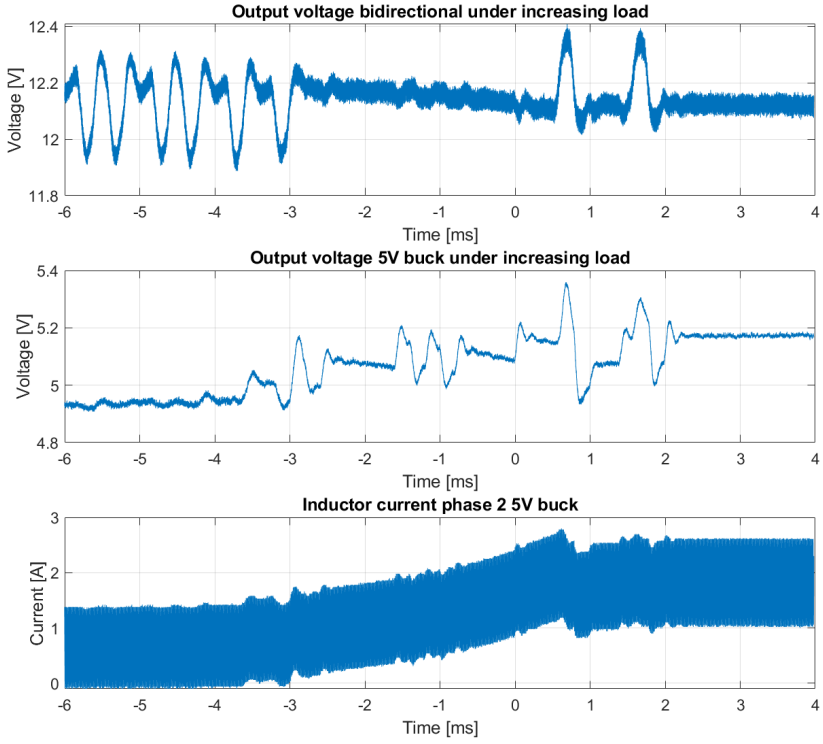


Figure 8.5: Measured voltage regulation capability of bidirectional and 5 V buck operated simultaneously.

Comparing the simulation in Figure 7.2 with the measured voltage regulation in Figure 8.5, the following observations are made. First of all, the measured output voltage ripples of the bidirectional converter are larger than the simulated ripples. Second, the measured output voltage of the bidirectional converter shows no steady-state oscillations at maximum load, which was shown in the simulation. Third, the output voltage of the 5 V buck converter shows no initial drop in output voltage and no oscillations in steady-state at maximum load, which were shown in both the simulation in Figure 7.2 and the stand-alone operation in Figure 8.4b. Further, the output voltage of the 5 V buck converter is regulated at 4.95 V initially, while at 5.19 V at maximum load. Finally, the output voltage of the bidirectional converter is regulated at 12.1 V. Thus, it can be concluded that the converters can regulate their output voltage slightly above their reference under dynamic load while remaining stable. Therefore, both the design and operation of the converters and their control are verified experimentally and are similar to the simulations with only minor deviations.

Chapter 9

Conclusion

In this thesis, the design of the Power Electronic System (PES) for the Lunar Zebro is developed. The primary objective of this design is to obtain a high level of efficiency, compactness, and the integration of redundancy methods. It is found that interleaved converters provide the best tradeoff between increase in size and redundancy added. In addition, the interleaved 3.3 V buck converter and bidirectional converter are more efficient than their single-phase counterpart. On the contrary, the interleaved 5 V buck and buck-boost converter are less efficient than their single-phase counterpart.

First, the effect of the bus voltage on the size and efficiency of single-phase DC/DC converters is explored. It is found that a 12 V bus results in more efficient DC/DC converters compared to a 24 V bus. An improvement of 33.78% is achieved when operated in CCM, whereas operation in DCM demonstrates a 12.34% improvement. Furthermore, the average power loss during operation is decreased by 13.02% using a 12 V bus compared to a 24 V bus, operating in CCM. Therefore, it is concluded that a 12 V bus voltage results in the most efficient system, hence this bus voltage is adopted. Moreover, it is concluded that the 12 V bus results in a more compact system. First, it requires a lower inductance for a specified current ripple than a 24 V bus. It is found that the size of the inductors contributes to 59.5% of the total footprint area. Therefore, opting for a reduced inductance results in a significant size reduction of the PES. Second, using a 12 V bus eliminates the need for an additional 12 V buck converter, further reducing the size of the system. Finally, it is concluded that operating the single-phase converters in CCM is more efficient than operating in DCM both for the 12 V and 24 V bus.

Subsequently, a comparative analysis of various redundancy methods is conducted to obtain the best tradeoff between redundancy added and the footprint required. The analysis revealed that a PES using interleaved converters including redundancy measures results in the lowest amount of footprint added, with only an 8.59% increase compared to single-phase converters without redundancy. Furthermore, for each converter short circuit or open circuit failure in a switch and diode, and open circuit failure of an output and input capacitor are accounted for. In contrast, the N+1 and 2N redundancy only account for failure in a single component for each converter. Therefore, interleaved converters including redundancy measures are used for the implementation of the PES.

The interleaved converters are designed using the 12 V bus configuration operating in both CCM and DCM. It is found that operating the interleaved converters in CCM is more efficient than DCM, similar to the single-phase converters. Operating the interleaved converters in CCM results in an improvement of 90.42% in efficiency compared to DCM operation. Therefore, it is concluded that operating in CCM results in the most efficient system.

The calculated efficiencies of the interleaved converters are compared to those of the single-phase converters. For DCM operation is found that the interleaved design is more efficient than the single-phase design in DCM, where the combined losses in the interleaved converters are reduced by 7.62% compared to the single-phase converters. On the contrary, when operated in CCM, the interleaved design is less efficient than the single-phase design. The combined losses in the interleaved converters in CCM are increased by 12.74% compared to the single-phase converters in CCM. It is concluded that this increase in losses is due to a significant reduction in efficiency for the interleaved buck-boost converter compared to the single-phase topology. The efficiency reduction is caused by the increase in core and winding losses for the inductors. The former arises from a reduction in inductance and smaller core size, while the latter is from an increase in DC resistance. Finally, it is concluded that the efficiency of the PES using interleaved converters is higher than the PES using single-phase converters during walking operation, but lower during charging operation.

A functional prototype of the PES has been developed. Measurements on this prototype have provided

experimental validation of the PES design. It is concluded that the measured steady-state operation of all interleaved converters is similar to the modelled and simulated operation, as well as the measured voltage regulation of the 5 V buck and bidirectional converters. Further, the models derived for the output capacitance and efficiency calculations are verified. The differences between the measured and calculated values are due to non-idealities of components that have not been modelled, such as the influence of the output capacitor ESR on the output voltage ripple. Finally, it is verified that the interleaved converters provide higher efficiency and lower voltage ripples than operating the same converter in single-phase mode.

9.1 Future Work

In Section 2.1 was found that GaN is the most radiation-hardened of all switches. This type of switch can handle switching speeds in the MHz range, however a switching frequency of only 100 kHz is used. Increasing the switching frequency results in smaller passive components. From Figure 4.6 and Table 5.13, the inductors of the interleaved converters including redundancy take up 59.5% of the total footprint area. Thus, the size and weight of the system can be significantly reduced by increasing the switching frequency. However, operating in the MHz range increases the effects of the parasitic capacitances and inductances. The PCB design of the PWM signals and high-frequency current path of the converters should be optimised to minimise these parasitics. Further, the parasitics should be modelled to verify they are not detrimental to the circuit operation. Finally, a significantly faster microcontroller should be used to generate the PWM signals at this frequency.

The second improvement involves the control. Currently, the converters are controlled using voltage control. In the measurements in Chapter 8 was shown that the inductor phases do not share the output current equally. By using current control, this problem can be alleviated [131, 132]. Current control provides several additional advantages over voltage control. First of all, it has a faster transient response since the output capacitor is removed from the feedback path. Second, it responds to input and output voltage changes immediately. Third, it has inherent cycle-by-cycle current limiting [134]. However, it requires two control loops instead of one increasing the complexity of tuning the PI controllers. Additionally, it requires more computation time of the microcontroller. The phase and gain margin of the system can be optimised by modelling the closed-loop transfer function of the converter and the controller. By inserting poles and zeros, the phase margin can be increased around the crossover frequency improving its transient response [127].

In Section 5.3 was found that the model of the input capacitor current of the interleaved bidirectional and buck-boost converter was incorrect. Hence, the calculated capacitance required and RMS current are too large. In the derivation was assumed that the capacitance is large enough such that the capacitor current shows no charge or discharge behaviour. However, in the simulations, it was observed that the capacitors show strong charge and discharge behaviour. Therefore, a more detailed model of the currents in these capacitors as a function of the converter parameters is needed to calculate the input capacitance required and RMS current in the capacitor.

In the loss evaluation of the interleaved converters in Section 5.5 was found that the inductor core losses are significantly larger for the interleaved converters compared to the single-phase converters. Additionally, it was found that the forward voltage drop of the diode accounts for a significant part of the total losses. Thus, a fourth improvement would be to reduce these losses to achieve higher efficiencies. The latter can be improved by implementing synchronous operation, where the diode is replaced with a switch. The disadvantage is that an additional gate driver circuit is required. Regarding the former, it was found that the core losses increase because the inductance is reduced by half and the core volume is reduced. The difference in core losses was the largest for the interleaved buck-boost converter where the core losses are increased by a factor of 12.06. As a result, the interleaved buck-boost converter is significantly less efficient than the single-phase variant. Similarly, the increase of core losses of the 5 V interleaved buck converter results in 109 mW more losses in the converter than in the single-phase variant. By increasing the inductance and core size, the core losses decrease. Thus, the efficiency can be improved by increasing the size of the inductors with the drawback of increased size and weight of the system.

Another improvement involves optimising the number of phases of the interleaved converters with respect to efficiency. In [88] is shown that the efficiency is not necessarily increased by increasing the number of phases but depends on the operating parameters of the converter. Furthermore, the value of the RMS

current in the input and output capacitor depends on the number of phases and duty cycle of the converter. For the output capacitor the RMS current can even become zero at certain conditions, for example using two phases at $D = 0.5$ [88].

A sixth improvement can be made by optimising the redundancy in the PES with respect to the size and weight of the system. In Chapter 4 was determined that the interleaved converters including redundancy methods resulted in the best tradeoff between the amount of redundancy added and the lowest amount of footprint added. However, no mathematical proof was given. By modelling the reliability of the PES using different redundancy methods, the best tradeoff between the reliability and the size and weight of the system can be obtained. One factor to consider involves optimising the number of phases of the interleaved converters with respect to the reliability and size of the converters.

The experiments conducted in Chapter 8 do not validate all functionalities of the PES. The closed-loop control of the 3.3 V interleaved buck converter is not verified, as well as operating it simultaneously with the rest of the PES under dynamic load. It is expected that this yields similar results as for the 5 V buck converter since the same topology and control are utilised. Further, the buck-boost converter utilising the PV panel has not been tested, and the MPPT algorithm has not been verified. Finally, the bidirectional power flow capabilities of the bidirectional converter should be verified as well.

The current design of the PES consists of the hardware and control required for supplying power to the subsystems in the rover. However, more systems need to be implemented for the PES to be complete for its mission. First of all, a Battery Management System (BMS) should be implemented to protect the batteries from over- and undercharging, implement cell balancing, control the charging of the batteries using a constant current and constant voltage mode scheme, and keep the batteries within the specified temperature range. The BMS should also interface with the rest of the rover to provide the health and status of the PES. Secondly, the gate drivers of the buck-boost converters are currently powered by COTS isolated DC/DC converters. Instead, these should be space-grade, or isolated gate drivers should be used. Finally, electrostatic discharge protection should be implemented to protect the system from the static electric-charged moon dust.

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Appendix A

Mechanisms of Radiation Damage on Power Electronics

A.1 Mechanism of Total Ionising Dose

The mechanism of TID is shown in Figure A.1, which shows the band diagram of a device with an SiO_2 dielectric where a positive gate voltage is applied. When radiation hits the dielectric, it creates electron-hole pairs inside this dielectric. Because of the applied gate voltage and because the mobility of electrons is high, the electrons that did not recombine are removed in picoseconds due to drift [17]. With the absence of electrons, recombination comes to a halt. The remaining holes that did not recombine have a much lower mobility, and hop from adjacent traps in the valence band to the SiO_2/Si interface. Deep hole trapping occurs near the SiO_2/Si interface, where naturally occurring defects are present where the holes are trapped. Hydrogen atoms are created due to the hopping and trapping of holes, which creates interface traps at the SiO_2/Si [27, 135]. These traps are negatively charged for N-channel Metal-Oxide-Semiconductor (NMOS) devices, thus compensating slightly for the positive charge build-up. The trapped holes can recombine with electrons that tunnel from the Si to the SiO_2, which increases with increasing temperature, but happens slowly [17]. This compensates for the positive charge build-up slightly as well.

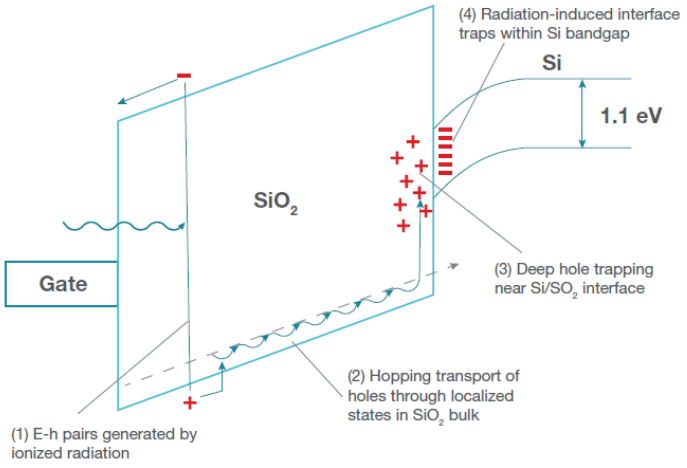

Figure A.1: Trapping mechanism of TID in an N-MOS SiO_2 with a positive gate voltage [17]

The interface traps and the trapped holes at the SiO_2/Si interface decrease the carrier mobility for both N-MOS and P-MOS devices. For an N-MOS device, the threshold voltage is shifted down. Because of the trapped holes in the oxide, the inversion layer in the channel is created more easily. However, the increase in the threshold voltage is slightly compensated due to the charge at the interface traps. Additionally, the drain-to-source leakage current is increased. For a P-MOS device, the opposite is true. The trapped holes increase the voltage required to create an inversion layer, increasing the absolute threshold voltage. Furthermore, the trapped holes reduce the leakage current. Thus, failure due to TID is less of a problem in P-MOS devices [17].

A.2 Mechanism of Single Event Burnout

A.2.1 IGBT

When incoming heavy ions travel through the high electric field region of the IGBT when it is in blocking state, the electric field strength is shifted from the n^-/p^- boundary to the n^-/n^+ boundary. This is shown in Figure A.2, which shows the electric field distribution at three times after radiation has hit. This shift is due to the local current created by the electron-hole pairs in the blocking region. The electric field at the n^-/n^+ boundary results in impact ionisation. Impact ionisation is explained in Appendix A.3.1. The carriers that are freed due to impact ionisation are injected into the n^- region (the base of the parasitic pnp transistor). This results in the parasitic npn transistor to turn on, and electrons are injected into the n^- region. With both parasitic transistors on, latch up of the parasitic thyristor has happened. Both the charges created from impact ionisation and thyristor latch up results in the SEB [52].

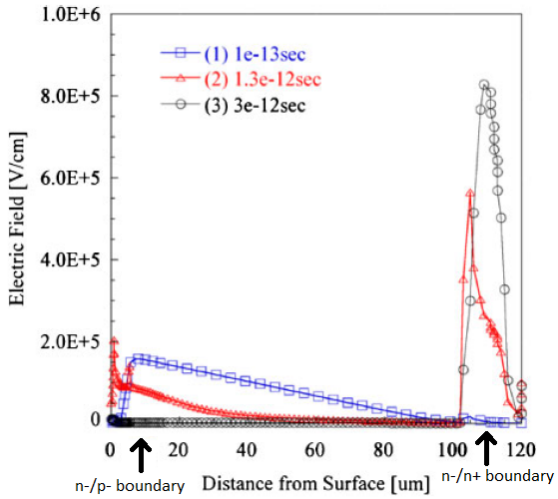

Figure A.2: Electric field distribution around the blocking region of an IGBT at different moments in time after radiation has hit the device [52].

A.2.2 MOSFETs

The mechanism of a SEB in Si MOSFETs is due to latch up or going into secondary breakdown. When heavy ions travel through the high electric field region of the MOSFET when it is in blocking state, the peak of the electric field strength is shifted from the p^-body/n^-drift junction to the n^-drift/n^+ junction and is increased in magnitude. This causes impact ionisation, where more carriers flow into the base of the parasitic transistor (the p-type body of the MOSFET), causing it to turn on locally. This results in more current flowing, resulting in a peak in the electric field at the drain. This results in more impact ionisation, which increases the current of the parasitic transistor and a positive feedback loop is created [23]. When a SEB occurs, this process continues until the device is destroyed.

The main mechanism of SEB in SiC MOSFETs is due to the shift in the electric field and the punch-through in the n+ source diffusion region, not due to the parasitic npn transistor action as is the case for a Si MOSFET [57]. This is similar to a SiC diode [20]. When heavy ions travels through the high electric field region of the MOSFET when it is in blocking-state, the peak of electric field strength is shifted from the p^-body/n^-drift junction to the n^-drift/n^+ junction and is increased in magnitude. This results in impact ionisation, and is shown in Figure A.3 from line t1 to line t3. The peak at $0\mu m$ shows that punch-through of the electric field happens at the n^+ source region. Both the impact ionisation and punch-through create highly localised currents that can result in a SEB. Note that the parasitic npn transistor can be turned on during the SEB, but has negligible effect on the destruction [20] [47].

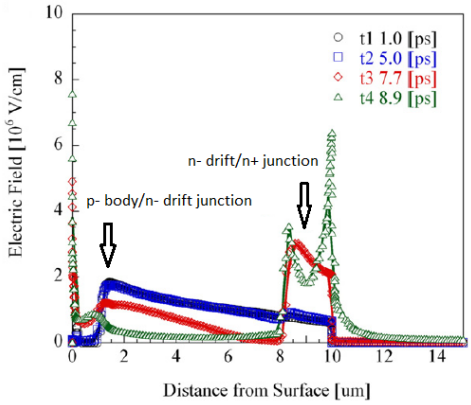

Figure A.3: Electric field distribution in a SiC MOSFET at different times after radiation hit the device [20].

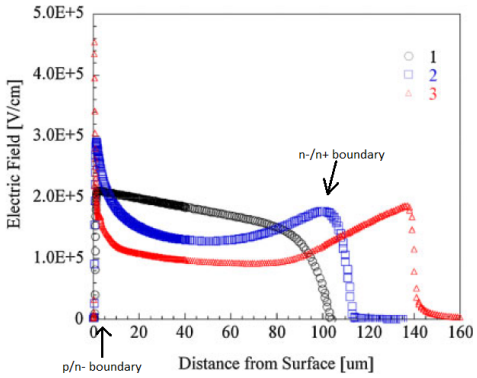

Figure A.4: Electric field distribution in a diode at different times after radiation has hit the device [52].

A.2.3 Diodes

When heavy ions create electron-hole pairs in the high electric field region when the diode is reversed biased, the electric field distribution transforms to a hammoc-like shape with two peaks at the p/n^- and n^-/n^+ boundary due to space charge effects [21]. This is shown in Figure A.4, where line 1 corresponds to normal voltage blocking operation at 1e-13s after radiation has hit. Line 2 and 3 correspond to two different times after radiation has hit the device and where the electric field is shifted. The two electric field spikes visible at line 2 cause double-sided impact ionisation. This creates highly localised currents with a negative differential resistance. The negative differential resistance causes an increase of the current while the voltage decreases, which is due to a decrease in the breakdown voltage [52]. Due to the double-sided impact ionisation the current increases locally, so the current density also increases locally resulting in a positive feedback loop. This is similar to the effect causing secondary breakdown [6]. At line 3, punch-through at the anode occurs and the diode acts locally as a resistor, because it has a positive differential resistance and has a linear increase of the electric field at the n^-/n^+ boundary [21]. Due to the high local currents, the device heats locally and can result in destruction [52].

A.3 Physics Power Electronics

A.3.1 Impact Ionisation

Impact ionisation is the process where the covalent bond of a silicon atom is broken and an electron is liberated when an electron hits the silicon atom, and this electron gained its kinetic energy from an electric field inside the semiconductor. This electric field is from the reverse voltage at the depletion region in case of blocking state of the device [73]. When the liberated electron gains enough kinetic energy from the electric field to again break a covalent bond and liberate an electron from a silicon atom, avalanche occurs. This process repeats quickly, resulting in a large current that can destroy the device. The voltage at which the electric field is large enough to produce avalanche is known as the avalanche breakdown voltage.

A.3.2 Secondary Breakdown

Secondary breakdown is the process where the device is destroyed due to a highly localised power dissipation. This localised power dissipation increases the temperature at this local spot to the degree that it destroys the device. It does not originate from impact ionisation [73]. Secondary breakdown happens due to thermal runaway. This process is defined as follows. Minority carriers have a negative temperature coefficient of resistivity, thus their resistivity decreases with increasing temperature. This results in an increase in the power dissipation for a constant voltage. If the temperature increase due to the increased power dissipation is larger than the rate of heat removal, then a positive feedback loop is created. If the current density is nonuniform, local thermal runaway can occur at places with a larger current density, resulting in local destruction of the device. This process is called secondary breakdown.

Appendix B

Calculation of core losses in DCM

In Chapters 3.4 and 5.4, the core losses for the DC/DC converters in DCM are presented. These are based on curve fitting the core losses in CCM using the core loss tool provided by Vishay [97]. Here, the method is presented.

The core losses in DCM can be calculated using the generalised Steinmetz equations. However, this requires knowledge of the Steinmetz coefficients α, β, and k_i, as well as the core volume V_e, core area A_c, and number of turns N of the inductor. These values are not provided by Vishay. Vishay provides a core loss calculator tool for operating in CCM, but not for DCM. Therefore, the unknown parameters are found by curve fitting the core losses in CCM using the core loss tool provided by Vishay using Matlab. This is done by writing the generalised Steinmetz equation as function of the input voltage. The input voltage is varied in the core loss tool and the resulting core loss is determined. In this way, all parameters are fixed except the input voltage. Since there are six unknown variables, the core loss at at least six input voltages need to be found using the core loss tool. The generalised Steinmetz equation is repeated in (B.1) for convenience.

$$P_\mathrm{v} = V_\mathrm{e} \frac{k_\mathrm{i} \left(\Delta B\right)^{\beta-\alpha}}{T_\mathrm{s}} \cdot \left(\left| \frac{\Delta B}{D T_\mathrm{s}} \right|^{\alpha} D T_\mathrm{s} + \left| \frac{\Delta B}{\left(1-D\right) T_\mathrm{s}} \right|^{\alpha} \left(1-\mathrm{D}\right) T_\mathrm{s} \right) \tag{B.1}$$

$$\Delta B = L \frac{\Delta I_\mathrm{L}}{N A_\mathrm{c}} \tag{B.2}$$

B.1 Buck Converters

For a buck converter, the duty cycle, current ripple, and flux density ripple as function of the input voltage are given by (B.3)-(B.5).

$$D = \frac{V_\mathrm{o}}{V_\mathrm{in}} \tag{B.3}$$

$$\Delta I_\mathrm{L} = \frac{V_\mathrm{o} \left(1 - \frac{V_\mathrm{o}}{V_\mathrm{in}}\right) T_\mathrm{s}}{L} \tag{B.4}$$

$$\Delta B = \frac{V_\mathrm{o} \left(1 - \frac{V_\mathrm{o}}{V_\mathrm{in}}\right) T_\mathrm{s}}{N A_\mathrm{c}} \tag{B.5}$$

Substituting in B.1 and simplifying, the resulting expression is given by (B.6).

$$P_\mathrm{v} = \frac{V_\mathrm{e} k_\mathrm{i}}{T_\mathrm{s}} \left(\frac{V_\mathrm{o} \left(1 - \frac{V_\mathrm{o}}{V_\mathrm{in}}\right) T_\mathrm{s}}{N A_\mathrm{c}} \right)^{\beta-\alpha} \left(\left| \frac{V_\mathrm{in} - V_\mathrm{o}}{N A_\mathrm{c}} \right|^{\alpha} \frac{V_\mathrm{o}}{V_\mathrm{in}} T_\mathrm{s} + \left| \frac{V_\mathrm{o}}{N A_\mathrm{c}} \right|^{\alpha} \left(1 - \frac{V_\mathrm{o}}{V_\mathrm{in}}\right) T_\mathrm{s} \right) \tag{B.6}$$

B.2 Boost Converter

For a boost converter, the duty cycle, current ripple, and flux density ripple as function of the input voltage are given by (B.7)-(B.9).

$$D = 1 - \frac{V_{\text{in}}}{V_{\text{o}}} \tag{B.7}$$

$$\Delta I_{\text{L}} = \frac{\left(1 - \frac{V_{\text{in}}}{V_{\text{o}}}\right) V_{\text{in}} T_{\text{s}}}{L} \tag{B.8}$$

$$\Delta B = \frac{\left(1 - \frac{V_{\text{in}}}{V_{\text{o}}}\right) V_{\text{in}} T_{\text{s}}}{N A_{\text{c}}} \tag{B.9}$$

Substituting in B.1 and simplifying, the resulting expression is given by (B.10).

$$P_{\text{v}} = \frac{V_{\text{e}} k_{\text{i}}}{T_{\text{s}}} \left(\frac{V_{\text{in}} \left(1 - \frac{V_{\text{in}}}{V_{\text{o}}}\right) T_{\text{s}}}{N A_{\text{c}}} \right)^{\beta - \alpha} \left(\left| \frac{V_{\text{in}}}{N A_{\text{c}}} \right|^{\alpha} \left(1 - \frac{V_{\text{in}}}{V_{\text{o}}}\right) T_{\text{s}} + \left| \frac{V_{\text{in}} - V_{\text{o}}}{N A_{\text{c}}} \right|^{\alpha} \frac{V_{\text{in}}}{V_{\text{o}}} T_{\text{s}} \right) \tag{B.10}$$

B.3 Buck-Boost Converter

For a buck-boost converter, the duty cycle, current ripple, and flux density ripple as function of the input voltage are given by (B.11)-(B.13).

$$D = \frac{V_{\text{o}}}{V_{\text{o}} + V_{\text{in}}} \tag{B.11}$$

$$\Delta I_{\text{L}} = \frac{\frac{V_{\text{o}}}{V_{\text{o}} + V_{\text{in}}} V_{\text{in}} T_{\text{s}}}{L} \tag{B.12}$$

$$\Delta B = \frac{\frac{V_{\text{o}}}{V_{\text{o}} + V_{\text{in}}} V_{\text{in}} T_{\text{s}}}{N A_{\text{c}}} \tag{B.13}$$

Substituting in (B.1) and simplifying, the resulting expression is given by (B.14).

$$P_{\text{v}} = \frac{V_{\text{e}} k_{\text{i}}}{T_{\text{s}}} \left(\frac{\frac{V_{\text{o}}}{V_{\text{o}} + V_{\text{in}}} V_{\text{in}} T_{\text{s}}}{N A_{\text{c}}} \right)^{\beta - \alpha} \left(\left| \frac{V_{\text{in}}}{N A_{\text{c}}} \right|^{\alpha} \frac{V_{\text{o}}}{V_{\text{o}} + V_{\text{in}}} T_{\text{s}} + \left| \frac{V_{\text{o}}}{N A_{\text{c}}} \right|^{\alpha} \left(1 - \frac{V_{\text{o}}}{V_{\text{o}} + V_{\text{in}}}\right) T_{\text{s}} \right) \tag{B.14}$$

Appendix C

Redundancy Interleaved Buck and Bidirectional Converter

In Chapter 4.3, the redundancy measures taken for the interleaved converters were explained to make them fault-tolerant. For the buck converter, two additional output capacitors are required. Furthermore, a fuse in series with the input and output of each phase leg is placed. The resulting topology is shown in Figure C.1. For the interleaved bidirectional converter, one additional input capacitor and two additional output capacitors are placed. Again, a fuse is placed in series with the input and output of each phase leg. The resulting topology is shown in Figure C.2.

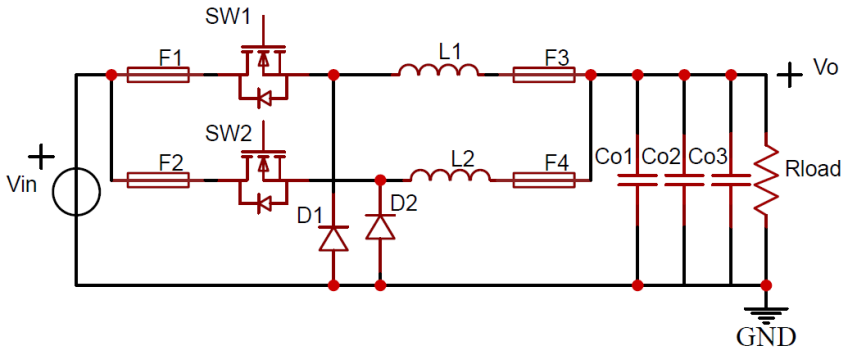

Figure C.1: Interleaved buck converter including redundancy measures.

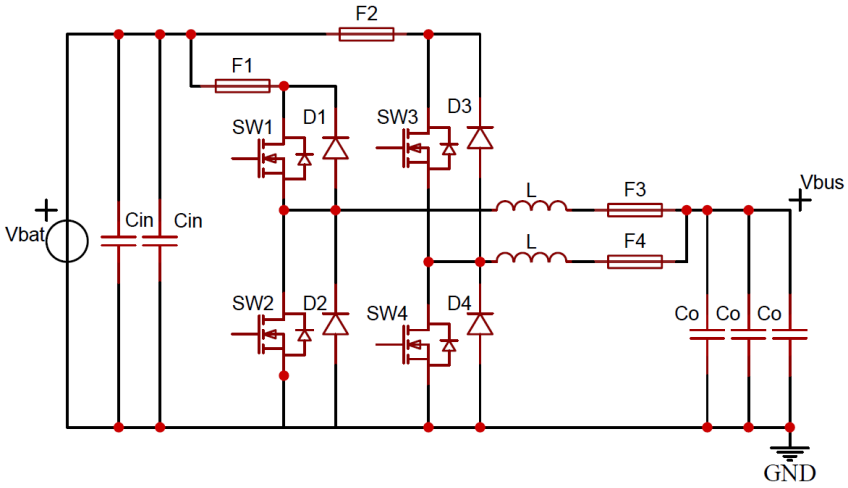

Figure C.2: Interleaved bidirectional converter including redundancy measures.

Appendix D

Simulink Simulation Models

D.1 Solar Panel Simulation

To find the power rating of the PV panel DC/DC converter, the MPP power must be known at the expected irradiance. The peak irradiance encountered on the moon is approximately 1350 W/m^2 [136]. The rover will operate between 60° and 90° longitude, while the solar panel is at 90° with the surface when charging. Thus, in worst-case conditions, the maximum angle of the solar irradiance is 30°, receiving $I_r = 1350sin(120°) \approx 1170\,W/m^2$. The MPP power in the datasheet is specified at 1000 W/m^2. Thus, to find the power generated at maximum and worst-case solar irradiance, a Simulink simulation is made, which is shown in Figure D.1.

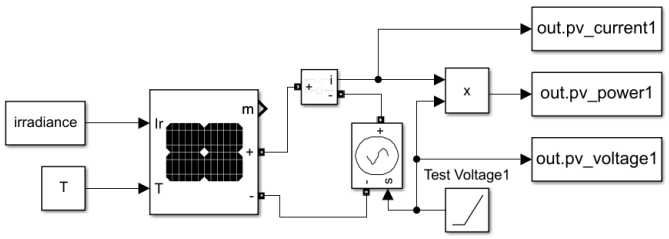

Figure D.1: Simulation model for determining the maximum power generated by the PV panel.

The solar cell is exposed at a constant irradiation, while the voltage at its terminals is ramped up. This is done for an irradiance of 1170 W/m^2, and 1350 W/m^2. The parameters used in the simulation for the PV cells used, the AzurSpace 3G30A cells, are based on the datasheet. Table D.1 provides the simulation parameters used. Table D.2 provides the resulting MPP voltage, current, and power under the worst-case and maximum irradiance.

Table D.1: Simulation parameters of the PV panel simulation

PV simulation parameters:		
Short circuit current cell	I_{sc}	0.5196 A
Open circuit voltage cell	V_{oc}	2.69 V
MPP voltage cell	V_{MPP}	2.409 V
MPP current cell	I_{MPP}	0.5029 A
Series connected cells	N_s	6
Parallel connected cells	N_p	2
Temperature coefficient V_{oc}	ΔV_{oc}	-0.1%/°C
Temperature coefficient I_{sc}	ΔI_{sc}	0.1%/°C
Temperature	T	25°C

Table D.2: MPP values of PV panel for worst-case and maximum irradiance.

	1170 W/m^2	**1350 W/m^2**
$\mathbf{V}_{MPP}$	15.12 V	15.14 V
$\mathbf{I}_{MPP}$	1.195 A	1.380 A
$\mathbf{P}_{MPP}$	18.07 W	20.90 W

D.2 Simulations of the Interleaved Converters

Throughout the thesis, multiple Simulink simulations of the interleaved converters are elaborated. In this appendix, the Simulink models used are presented together with the corresponding configuration parameters for each simulation. The Simulink models of the interleaved bidirectional converter, buck converters,

and buck-boost converter are shown in Appendix D.2.4, D.2.5, and D.2.6, respectively. The controllers of each converter are made as submodules and are presented in Appendix D.2.7. The general simulation parameters used for each converter are provided in Table D.3.

Table D.3: General simulation parameters of the interleaved converters.

General simulation parameters		**Bidirectional**	**5V buck**	**3.3V buck**	**Buck-boost**
Converter Parameters					
Rated power	P_{max}	90.22 W	20 W	13.2 W	20.95 W
Switching frequency	F_{s}	100 kHz	100 kHz	100 kHz	100 kHz
Inductance phase 1 and 2	L_1, L_2	22 μH	22 μH	15 μH	33 μH
Output capacitance	C_{o1}, C_{o2}, C_{o3}	15 μF	22 μF	33 μF	33 μF
Input capacitance	C_{in1}, C_{in2}, C_{in3}	22 μF	-	-	22 μF
Upper resistance of divider	R_1	1.02 MΩ	700 kΩ	300 kΩ	1.02 MΩ
Lower resistance of divider	R_2	180 kΩ	300 kΩ	300 kΩ	180 kΩ
On-resistance of switch	R_{sw}	12 mΩ	12 mΩ	12 mΩ	12 mΩ
On-resistance of diode	R_{D}	27.5 mΩ	14.3 mΩ	14.3 mΩ	65.3 mΩ
Forward voltage drop diode	V_{f}	433 mV	290 mV	290 mV	329 mV
Controller parameters					
Sampling frequency	F_{sample}	5 kHz	5 kHz	5 kHz	5 kHz
Proportional gain	K_{p}	0.087	0.093	0.0603	-
Integral gain	K_{i}	738.16	700.28	468.71	-
Anti windup limits	$[i_{\text{min}}, i_{\text{max}}]$	[-1, 1]	[-1, 1]	[-1, 1]	-

D.2.1 Steady State Simulations

In Chapter 5, the models derived of the interleaved converters are verified using simulations. A steady state simulation is done at maximum power of each converter, and the results were discussed in Section 5.3. For all four converters, the voltage controller in continuous domain from Figure D.5 is used. Note that for the bidirectional converter, no synchronous operation is used in this simulation. Hence, the gate signals *Gate1* and *Gate2* are for the upper switches *SW_U1* and *SW_U2*, while the gate signals of the lower switches are set to zero. For all converters, the output resistor R_{load} is set at the constant R_{resistor}. Note that for the buck-boost converter a DC source and resistor are used as input and output, respectively, just as for the bidirectional and buck converters. The initial conditions of the inductor currents for the buck converters and bidirectional converter in CCM are given by (D.1) and (D.2).

$$I_{\text{Lph1,0}} = \frac{I_{\text{o}}}{2} - \frac{\Delta I_{\text{L}}}{2} \tag{D.1}$$

$$I_{\text{Lph2,0}} = \frac{I_{\text{o}}}{2} + \frac{\Delta I_{\text{L}}}{2} - \frac{V_{\text{o}} T_{\text{s}} (0.5 - D)}{L} \tag{D.2}$$

The initial inductor currents of the buck-boost converter in CCM are given by (D.3) and (D.4).

$$I_{\text{Lph1,0}} = \frac{I_{\text{o}}}{2} - \frac{\Delta I_{\text{L}}}{2} \tag{D.3}$$

$$I_{\text{Lph2,0}} = \frac{V_{\text{o}} T_{\text{s}} (D - 0.5)}{L} + \frac{I_{\text{o}}}{2(1 - D)} + \frac{\Delta I_{\text{L}}}{2} \tag{D.4}$$

Finally, Table D.4 provides the operating conditions for the steady state simulations.

Table D.4: Simulation parameters used for the steady state simulations.

Steady state simulation parameters		**Bidirectional**	**5V buck**	**3.3V buck**	**Buck-boost**
Load resistance	R_{load}	1.60 Ω	1.25 Ω	825 mΩ	6.87 Ω
Output load current	I_{o}	7.52 A	4 A	4 A	1.75 A
Initial inductor current phase 1	$I_{\text{Lph1,0}}$	2.59 A	1.34 A	1.20 A	547.4 mA
Initial inductor current phase 2	$I_{\text{Lph2,0}}$	5.32 A	2.47 A	2.30 A	2.37 A
Input voltage	V_{in}	21 V	12 V	12 V	15.18 V
Output voltage	V_{o}	12 V	5 V	3.3 V	12 V

D.2.2 Changing Load Simulations

The performance of the PI controllers of the bidirectional, 5 V and 3.3 V buck converters was simulated in Section 6.1. In this simulation the ability to regulate the output voltage to its reference is tested under changing load conditions. The output resistance of the converters is ramped down until the converters operate at their rated power. The initial value of the load resistor is chosen such that the converters operate in DCM. In this way, the difference in tracking speed in DCM and CCM can be compared. The load resistor R_{load} is set at the ramp for all the simulations. Finally, the corresponding continuous voltage controllers are used. The same simulations were carried out for the digital controller in Section 6.2, where the corresponding digital controllers are used. Table D.5 provides the simulation parameters used.

Table D.5: Simulation configuration parameters for simulating a changing load for the voltage controllers.

Changing load simulation parameters		**Bidirectional**	**5V buck**	**3.3V buck**
Initial load resistance	$R_{\text{load,0}}$	6 Ω	5 Ω	3.3 Ω
Initial load current	$I_{\text{o,0}}$	2 A	1 A	1 A
Final load resistance	R_{load}	1.60 Ω	1.25 Ω	825 mΩ
Final load current	I_{o}	7.52 A	4 A	4 A
Ramp time from $R_{\text{load,0}}$ to R_{load}	t_{ramp}	10 ms	10 ms	10 ms

D.2.3 Maximum Power Point Tracking Simulation

The MPPT simulation of the interleaved buck-boost converter was carried out in Section 6.3. The Simulink model used is given in Figure D.4. In this simulation the capability of the MPPT algorithm of the buck-boost converter to find the MPP is tested for both increasing irradiance and decreasing irradiance. The implementation of the MPPT algorithm in Simulink is shown in Figure D.9. The initial irradiance is set at the maximum of 1350 W/m^2. The input capacitors are initially discharged to simulate that no power is generated earlier but that it starts generating at the start of the simulation. Hence, the capability to track an increase in the irradiance is simulated in this way. When the controller has reached the MPP, the irradiance is decreased to 500 W/m^2 to verify that the controller can track the MPP when the irradiance is decreased. Table D.6 provides the simulation parameters used.

Table D.6: Simulation configuration parameters used for the MPPT simulation.

MPPT simulation parameters		
Buck-boost converter:		
Initial input voltage	$V_{\text{in,0}}$	0 V
Initial output voltage	$V_{\text{o,0}}$	12 V
Initial duty cycle	D_0	0.35
PV panel:		
Temperature	T_{PV}	25 °C
Initial irradiance	I_{r0}	1350 W/m^2
Final irradiance	I_{r}	500 W/m^2

D.2.4 Interleaved Bidirectional Simulation Model

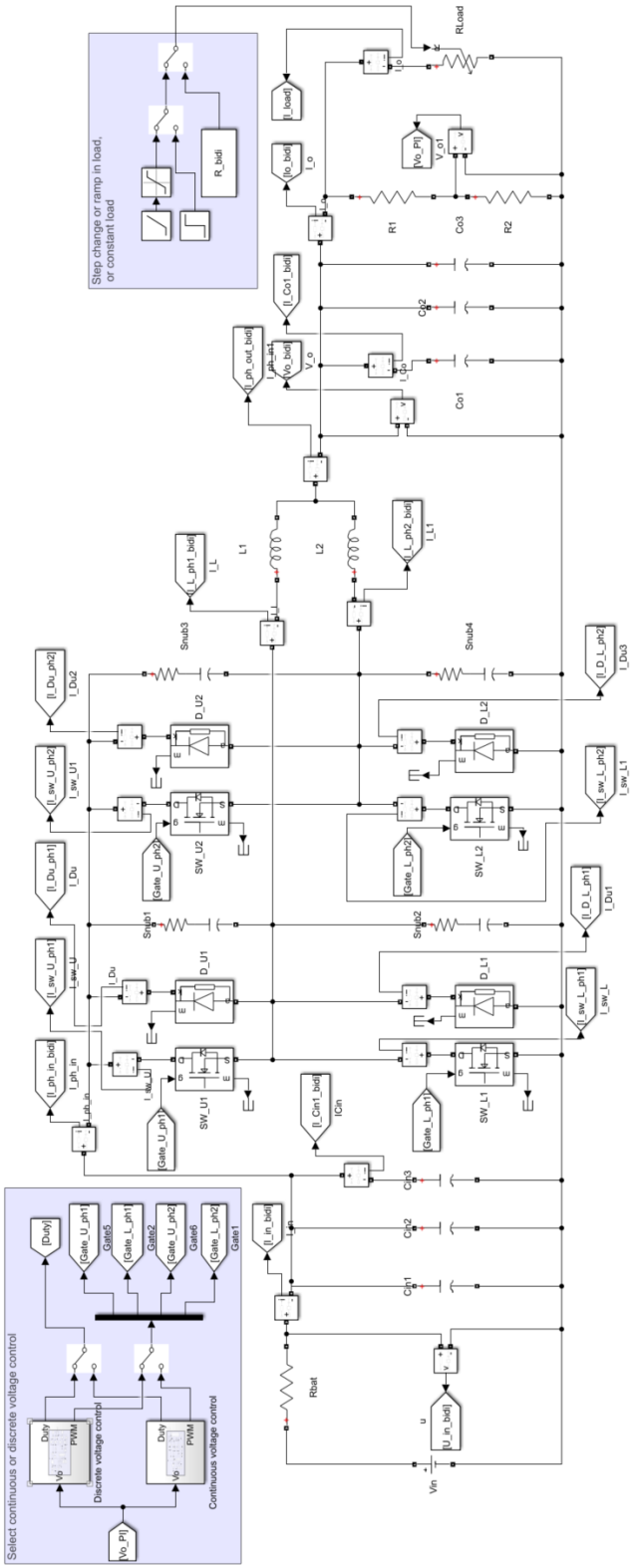

Figure D.2: Simulink model of the interleaved bidirectional converter.

D.2.5 Interleaved Buck Simulation

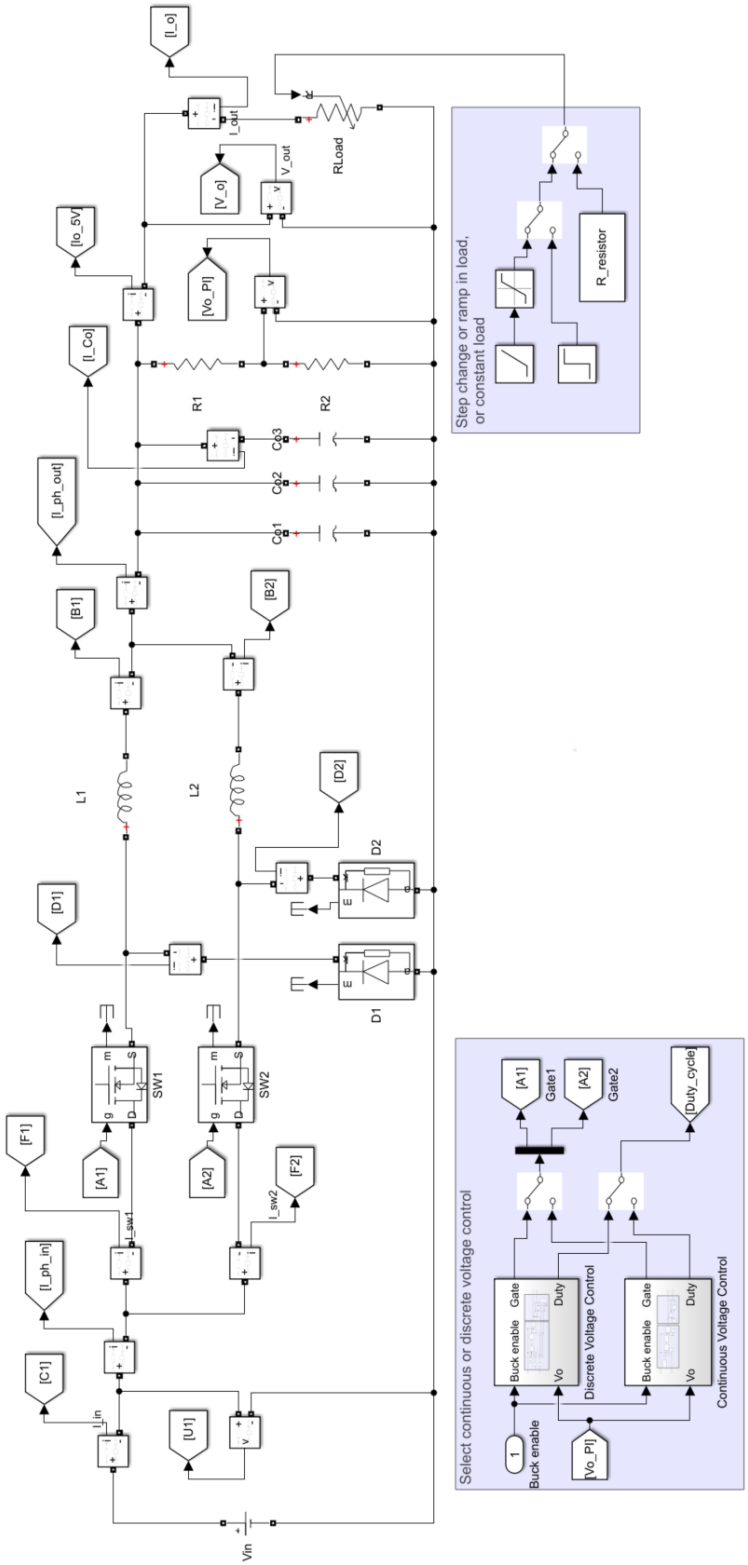

Figure D.3: Simulink model of the interleaved buck converters.

D.2.6 Interleaved Buck-Boost Simulation

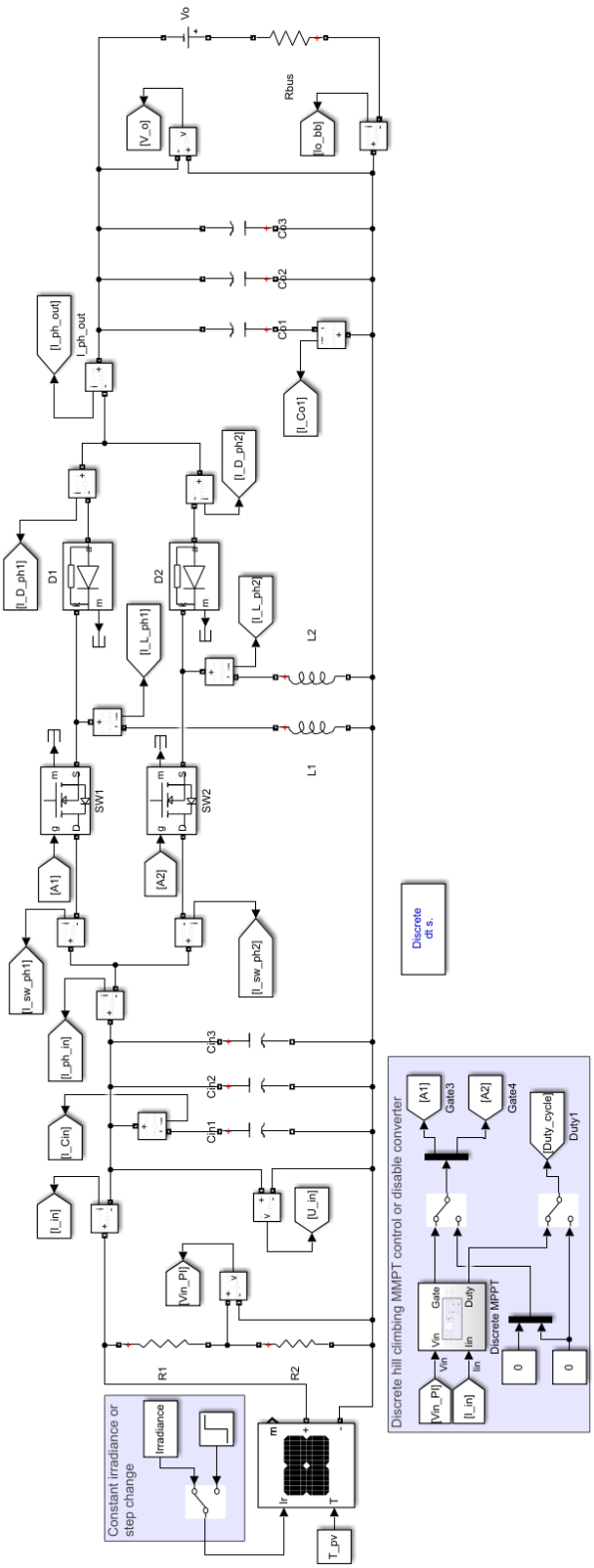

Figure D.4: Simulink model of the interleaved buck-boost converter.

D.2.7 Controllers

In Figure D.5 the controller for voltage control of the 5 V and 3.3 V buck converters in the Laplace domain is shown. It consists of the duty cycle calculation and the PWM generation. The error signal is fed into the PI controller which produces the duty cycle for the switches. Then, the PWM signal is generated from the duty cycle. A delay of $T_S/2$ is implemented with the delay block for the required phase shift of $T_S/2$ for the two switches of the interleaved converters. Finally, the controller can be disabled if the signal *Buck enable* is zero, which will be the case when startup of the PES is simulated.

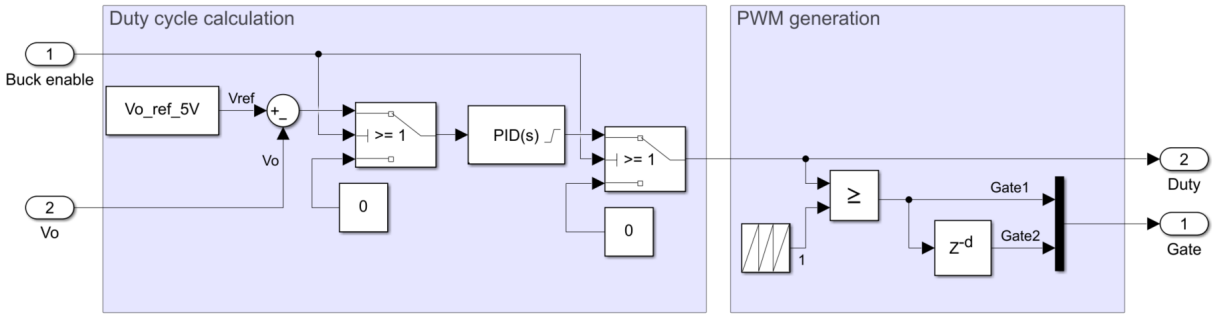

Figure D.5: Voltage control of buck converters in continuous domain.

The discrete implementation of the voltage controller is shown in Figure D.6. The difference between the continuous controller are the rate transmission blocks Fsample, Fsample1, and Fsample2. They are set to the sampling frequency of 5 kHz to mimic the control loop speed of the microcontroller. Additionally, instead of the PID block in s-domain, the discrete PI controller given by (6.4) is implemented using Simulink blocks. This is shown in Figure D.7. It includes anti-windup of the integrator, an configurable initial duty cycle, and saturation of the duty cycle. The PWM generation is the same as for the continuous domain.

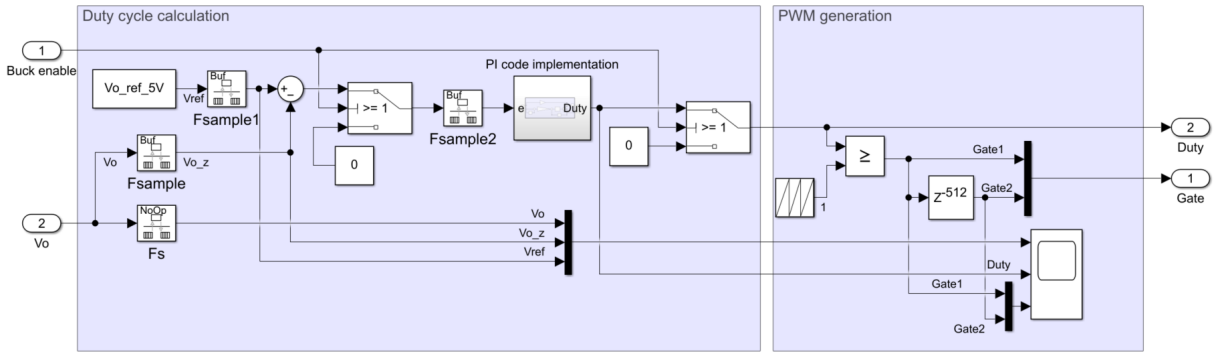

Figure D.6: Voltage control of buck converters in discrete domain representing the microcontroller.

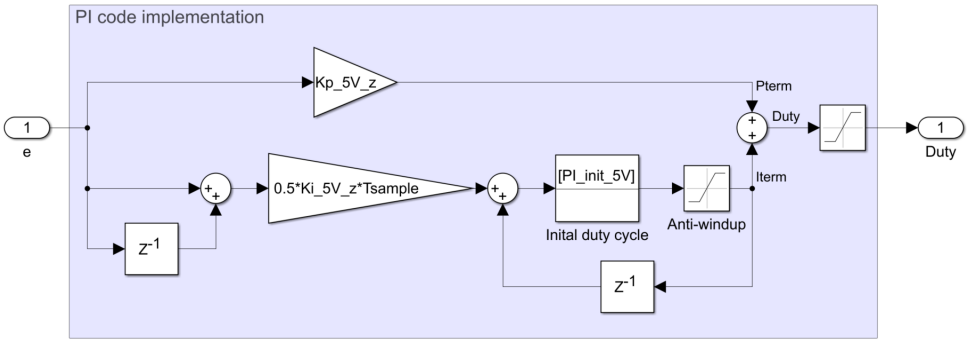

Figure D.7: PI controller of microcontroller implemented using Simulink blocks.

For the bidirectional converter, the duty cycle both in continuous domain and discrete domain is calculated the same way as for the buck converters. However, the PWM generation is done differently than for the buck converters. The PWM generation is the same for the continuous controller and digital controller. The discrete implementation of the voltage controller of the bidirectional converter is shown in Figure D.8. The dead time required is implemented by the logical AND operation between the gate signal and the time shifted version of the gate signal, where the time shift is equal to the dead time. Further, the lower switch has the logical NOT operation with respect to the upper switch to implement synchronous operation. Finally, the time shift of Ts/2 for phase two compared to phase one is implemented using the delay block, similar as for the buck converters.

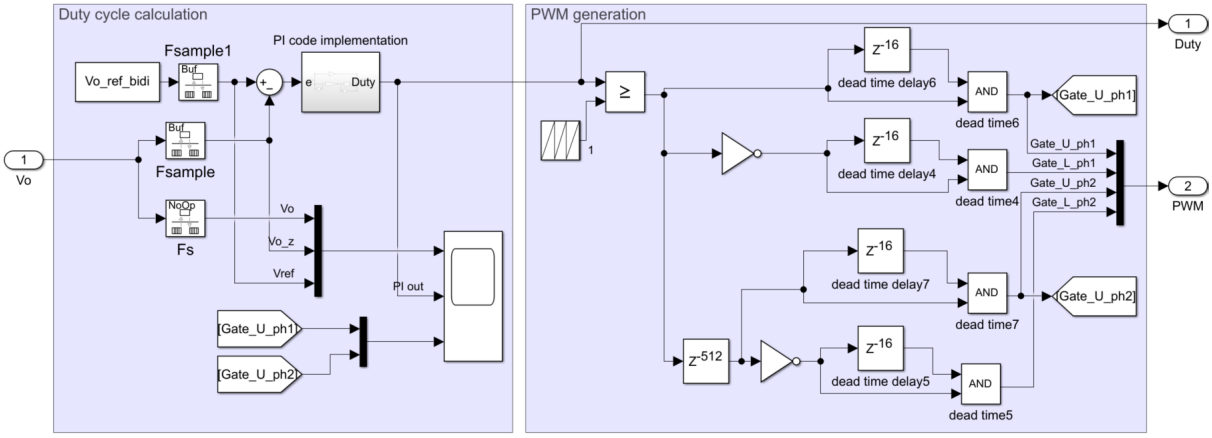

Figure D.8: Voltage control of bidirectional converter in discrete domain representing the microcontroller.

Finally, the discrete MPPT controller of the buck-boost converter is shown in Figure D.9. The increment or decrement of the duty cycle is a logical XOR between the power check 'P[k]>P[k-1]' and voltage check 'V[k]>V[k-1]' from Figure 6.9. This is implemented using the *V logic* and *P logic* blocks together with XOR port. Further, an initial duty cycle can be set using the *[D_init_bb]* block. The output of the MPPT algorithm is the duty cycle. The PWM generation is done in the same way as for the buck converters.

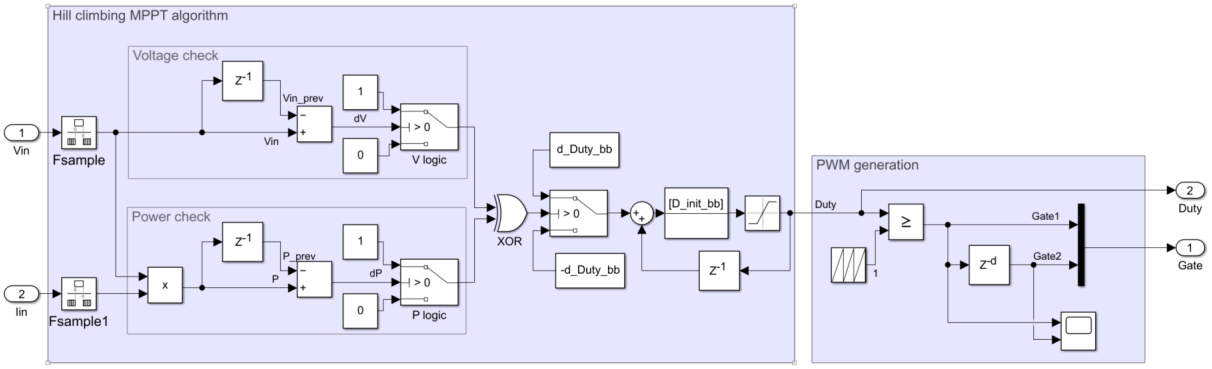

Figure D.9: Hill climbing algorithm and PWM generation in discrete domain for buck-boost converter.

D.3 Voltage Regulation of Continuous Controllers

In Section 6.1, the parameters K_p and K_i of the PI controllers for the interleaved bidirectional and buck converters are determined in the continuous domain. Here, the voltage regulation of these controllers for each converter is presented.

D.3.1 Bidirectional Converter

The performance of the PI controller of the bidirectional converter is shown in Figure D.10. The simulation model is elaborated in Appendix D.2.5. Initially, the load current is 2 A where it operates at forced CCM and the inductor currents become negative. At 3 ms, the load is increased exponentially to its maximum of 7.51 A in 10 ms. Because the converter operates at CCM at all times, it can keep its output voltage close to its reference. Only minor oscillations and drops in voltage are shown.

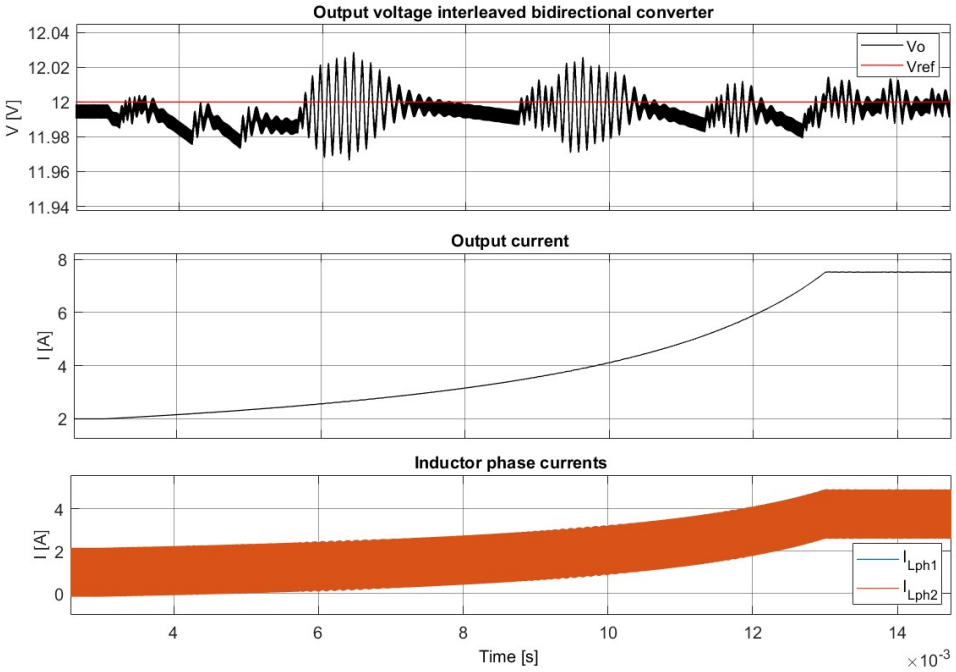

Figure D.10: Simulated voltage regulation of the interleaved bidirectional converter under increasing load.

D.3.2 Buck Converters

The performance of the PI controller of the interleaved 5 V buck converter is shown in Figure D.11. Initially, the converter operates in steady state at an output current of 1 A. At 3 ms, the current starts increasing exponentially to 4 A in 10 ms. The output voltage drops by 1.8% to 4.91 V. When the inductor phase currents become CCM at I_o=1.33 A, the output voltage increases until the reference voltage and shows damped oscillations. When the output current reaches 4 A, some overshoot of the output voltage occurs due to the sudden stop of load increase. After a few oscillations, the output voltage ripple is completely damped and the output voltage is at its reference.

Similar observations can be made for the interleaved 3.3 V buck converter, shown in Figure D.12. The output voltage drops by 2.1% to 3.23 V before increasing to the reference. However, fewer oscillations are visible than for the 5 V buck converter.

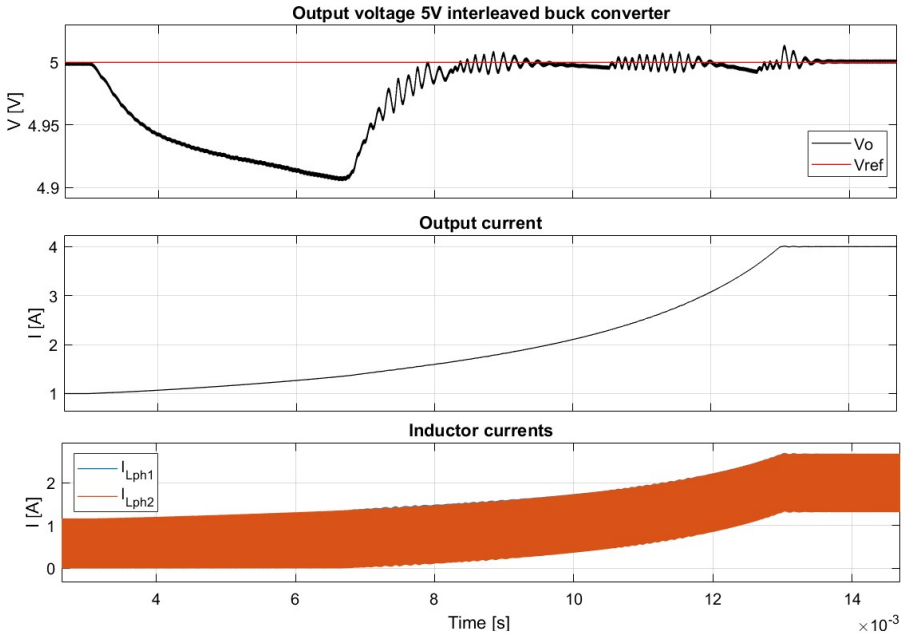

Figure D.11: Simulated voltage regulation of the interleaved 5 V buck converter under increasing load condition.

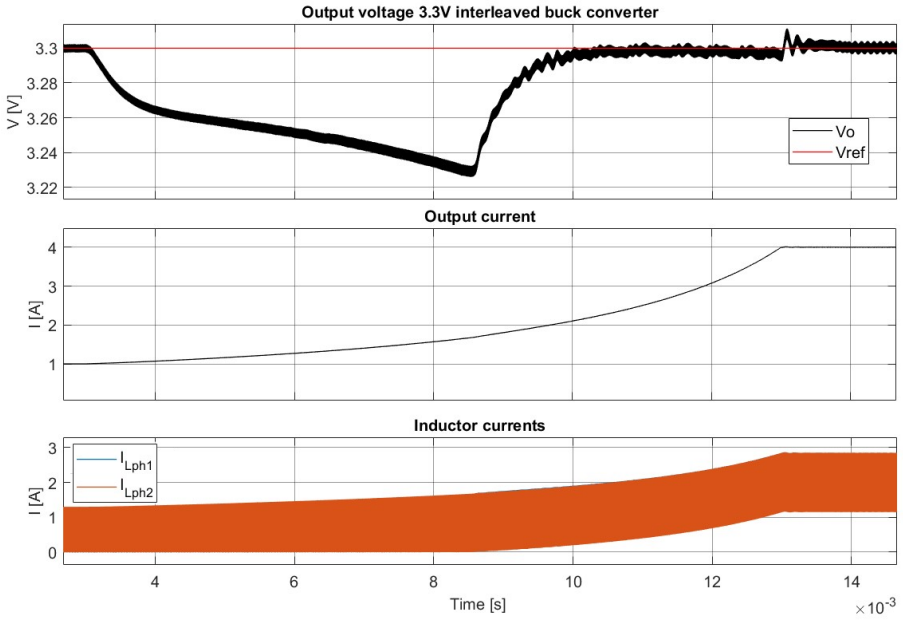

Figure D.12: Simulated voltage regulation of the interleaved 3.3 V buck converter under increasing load.

D.4 Complete PES Simulation Model

The simulation model of the complete PES from Chapter 7 is shown in Figure D.13. The model of the bidirectional, bucks, and buck-boost converters shown in Figures D.2, D.3, and D.4 are made as subsystems in the simulation. However, the input sources and output loads are removed for each converter. These are placed at the top level of the PES simulation. In addition, the duty cycle calculation part of the controllers of each converter is placed in the *Microcontroller* subsystem.

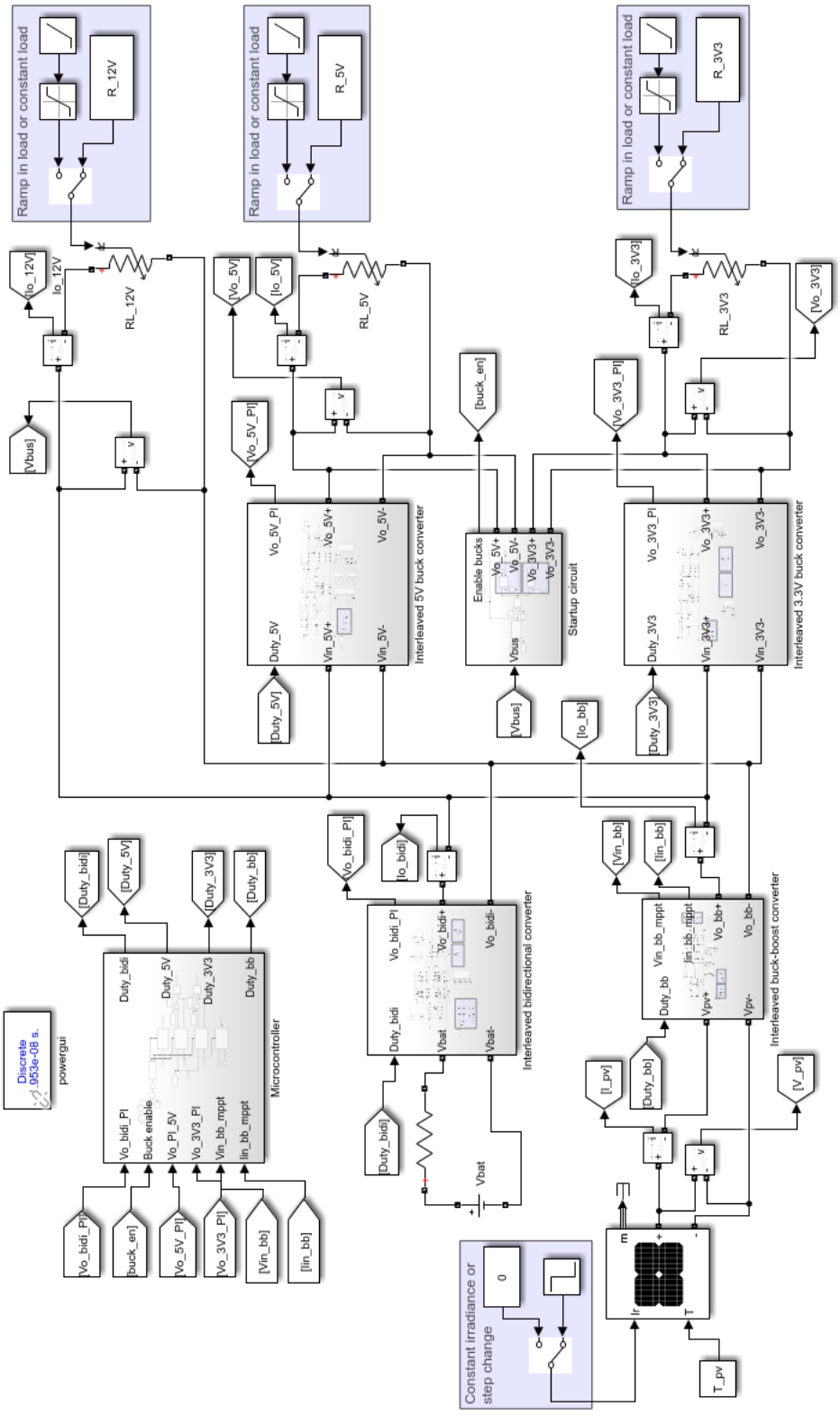

Figure D.13: Simulink model of the complete PES simulation.

The startup circuit is shown in Figure D.14. It mimics the two LDOs that power the gate drivers and microcontroller during startup. The startup circuit keeps the output voltages of the 5 V and 3.3 V bucks at their rated voltage during startup in the simulation while keeping the buck converters off. The Matlab function block sets the output *LDO_dis* to one when no startup is simulated. When startup is simulated, the output is set to zero and when the bus voltage has been reached the output is set to one. When the output is one, the sources representing the LDOs are disconnected from the outputs of the buck converters. The *Enable*

bucks output is the input of the controllers of the buck converters. When set to one, the voltage controllers of the buck converters from Figure D.6 are enabled.

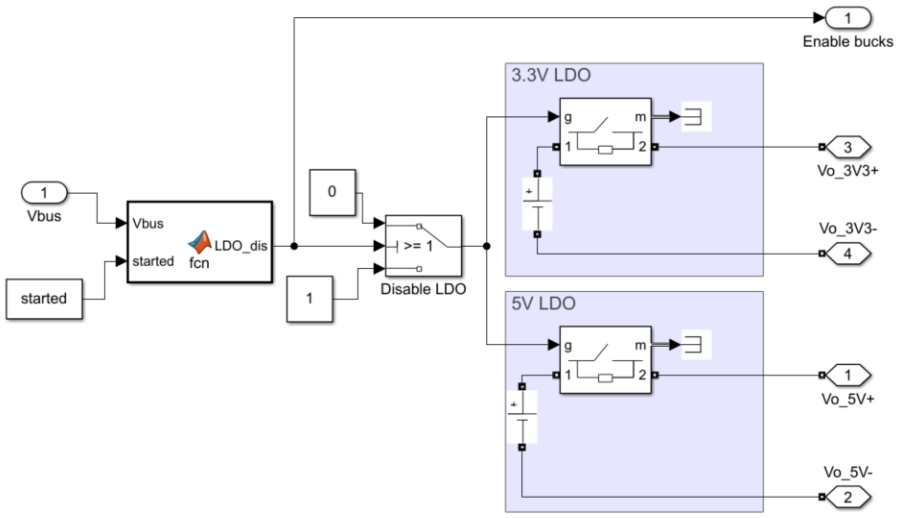

Figure D.14: Simulink model of the startup circuit.

Finally, the microcontroller implementation is shown in Figure D.15. It implements the switch-case structure of the software from Section 6.2.4, where each converter is updated periodically one by one at a rate of 5 kHz. The rate transition blocks *Fcontrol* are set at 20 kHz to achieve the 5 kHz update rate for each converter. The subsystems *Bidirectional update*, *5V buck update*, *3.3V buck update*, and *Buck-boost update* contain the duty cycle calculation part of each controller from Section D.2.7. The PWM generation part is put into subsystems of the converters since the PWM signals have to be generated continuously.

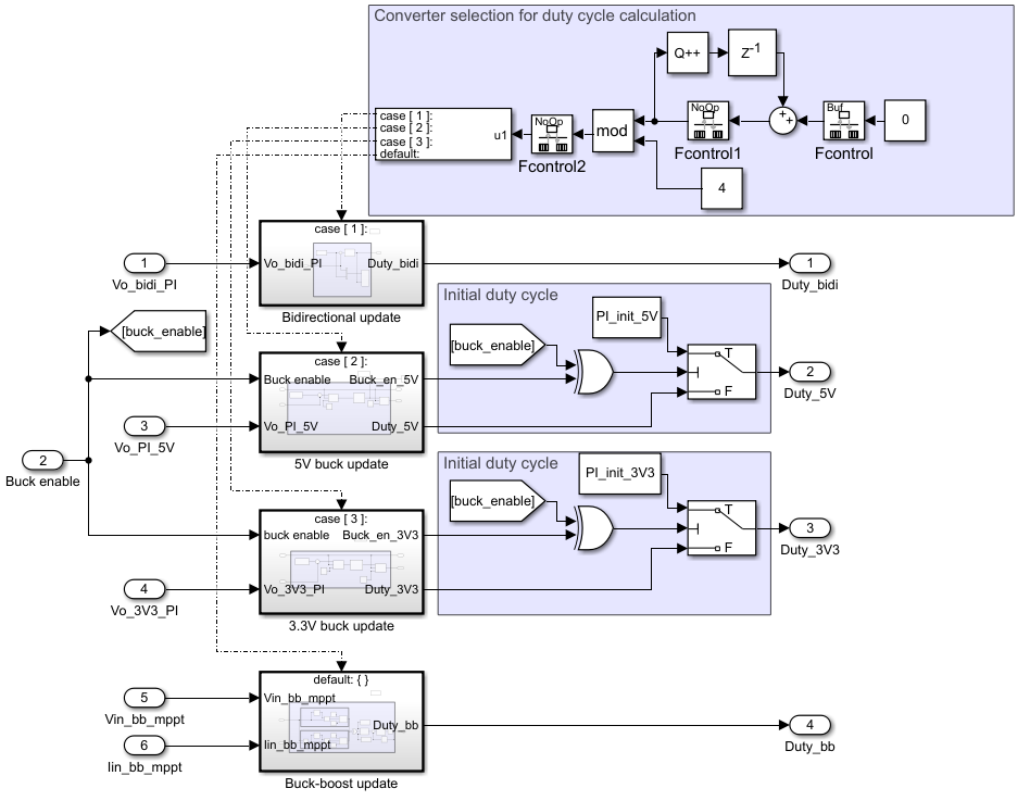

Figure D.15: Simulink model of the microcontroller control implementation.

Appendix E

LTSpice Simulations

E.1 Double Pulse Test

In Chapter 5.7, the snubber resistance R_s and capacitance C_s were found using double pulse test simulations in LTspice. In Figure E.1, the schematic of the double pulse test is shown. In a double pulse test, the switch is turned on and off twice. During the first pulse, the current in the inductor $L1$ is ramped up to the desired value I_{L1}. The pulse duration is determined from Equation E.1.

$$T_{\text{pulse1}} = \frac{L_1 I_{L1}}{V_1} \tag{E.1}$$

After T_{pulse1}, the switch is turned off at current I_{L1}. At this point, the turn-off characteristics of the switch are determined at worst-case conditions. When the switch has turned off, the diode D_1 acts as freewheeling diode and conducts I_{L1}. After T_{pulse2}, the switch is turned back on. It has to switch-on current I_{L1}, hence it operates under hard-switching conditions. At this point, the turn-on characteristics of the switch are determined at worst-case conditions.

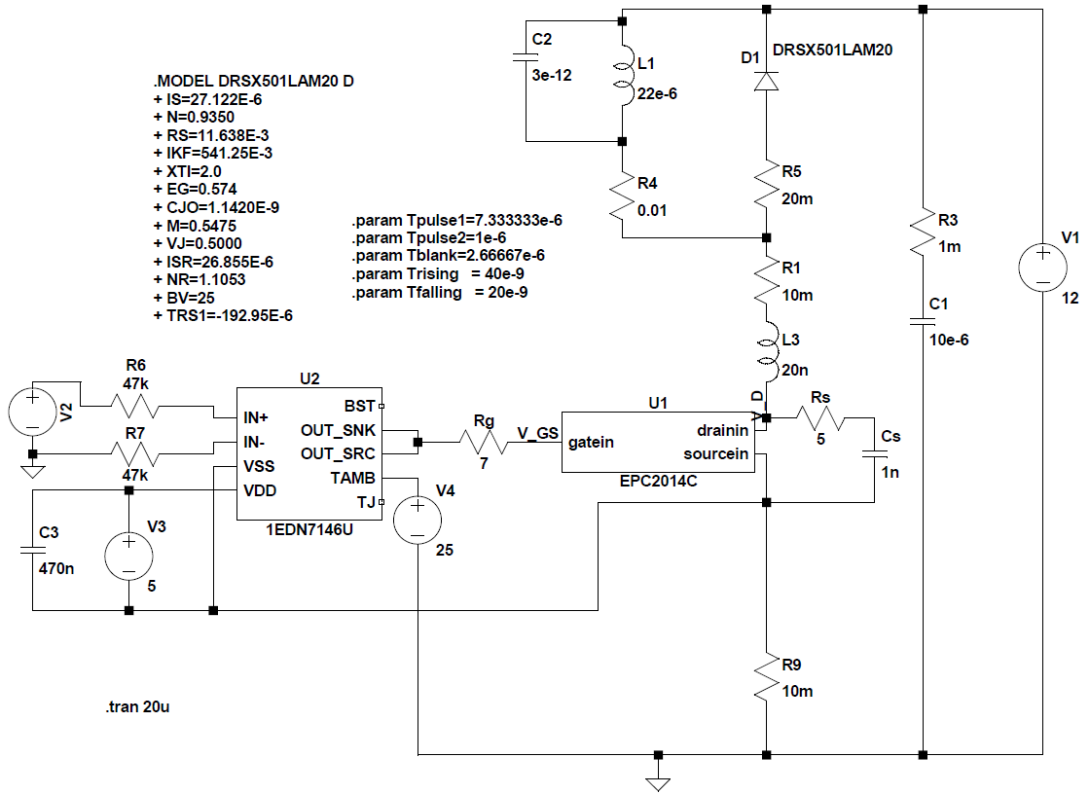

Figure E.1: Double pulse test simulation of the interleaved buck converters in LTspice.

In the simulations, a parasitic resistance is placed in series of each component. Additionally, a parasitic capacitance has been placed in parallel to the main inductance L_1. The stray inductance L_3 is modelled

as a single inductance at the drain, representing the total stray inductance seen by the drain and source of the switch. The exact value depends on the thickness and traces used in the PCB. A value of 10 nH seen at the drain and source is estimated, resulting in a total stray inductance of 20 nH. Table E.1 provides the simulation parameters of the DPT simulation for the interleaved bucks, buck-boost, and bidirectional converter.

Table E.1: Parameters of the DPT simulation

DPT simulation parameters:		**Bucks**	**Buck-boost**	**Bidirectional**
Double pulse circuit:				
Source voltage	V1	12 V	27 V	21 V
Diode	D1	RSX501LAM20TR	PMEG4050EP,115	SS8P3L-M3/86A
Inductor	L1	22 μH	33 μH	22 μH
Stray inductance	L3	20 nH	20 nH	20 nH
Gate driver:				
Supply voltage	V3	5 V	5 V	5 V
Gate resistor	Rg	7 Ω	10 Ω	9 Ω
Ambient temperature	V4	25°C	25°C	25°C
Supply capacitance	C3	470 nF	470 nF	470 nF
TDI input resistors	R6, R7	47 kΩ	47 kΩ	47 kΩ
On-time	Tpulse1	7.33 μs	4.547 μs	9.104 μs
Off-time	Tpulse2	1 μs	1 μs	1 μs

Figure E.2 shows the gate-source voltage, drain-source voltage, and drain current from the simulation shown in Figure E.1. The current ramps up to the maximum inductor current expected in the 5 V buck converter, after which the switch is turned-off. Some overshoot of V_{DS} is visible. The switch is turned on again, showing some oscillations in the drain current. Thus, it can be concluded that the simulation works as intended.

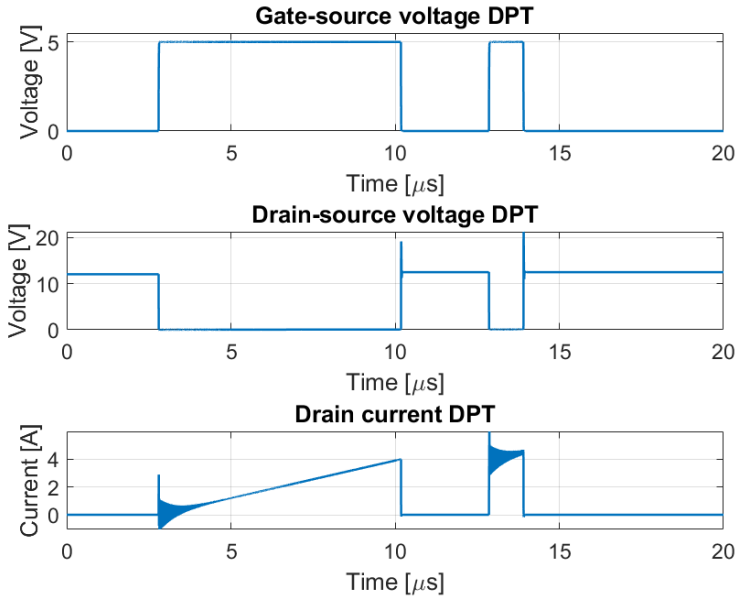

Figure E.2: Gate-source voltage (top), drain-source voltage (middle), and drain current (bottom), of the switch for the DPT of the interleaved buck converters from Figure E.1.

E.2 Snubber Design Bidirectional and Buck-Boost Converters

In Section 5.7.1 the design of the snubber network for the interleaved buck converters is discussed. Since the work is repetitive, the design of the snubber network of the interleaved buck-boost and bidirectional converter is presented here.

E.2.1 Snubber Interleaved Buck-Boost Converter

In Figures E.3 and E.4, the drain-source voltage and the losses in the snubber resistance are shown for constant C_s=1 nF and by changing R_s from 1 Ω to 20 Ω. Figures E.5 and E.6 show the same, but for constant R_s and changing C_s. The same observations as for the interleaved buck converter are made:

- By increasing the resistance, the voltage ringing is damped more and the overshoot is reduced.
- The ringing and overshoot is increased for R_s too large, in this case R_s >15 Ω.
- The energy loss in the snubber resistor is barely affected by the value of R_s for $R_s > 5\,\Omega$.
- By increasing C_s, the voltage ringing is damped more and the overshoot reduced.
- The energy losses increase exponentially by increasing C_s.

From Figure E.3, a snubber resistance value of R_s = 15 Ω results in the lowest amount of ringing and overshoot. From Figure E.5, a snubber capacitance of C_s = 1 nF results in the lowest overshoot while also keeping E_{sn} < 1 μJ. However, with C_s = 500 pF, the voltage spike increases by less than 2 V while decreasing the losses by a factor of two. Therefore, a snubber capacitance of 500 pF is used. The average power loss in the snubber network using R_s = 15 Ω and C_s = 500 pF is $P_{sn} = E_{sn}F_s$ = 35.55 mW. This reduces the efficiency by 0.170% at MPP. Thus, the power loss in the snubber resistance can be neglected.

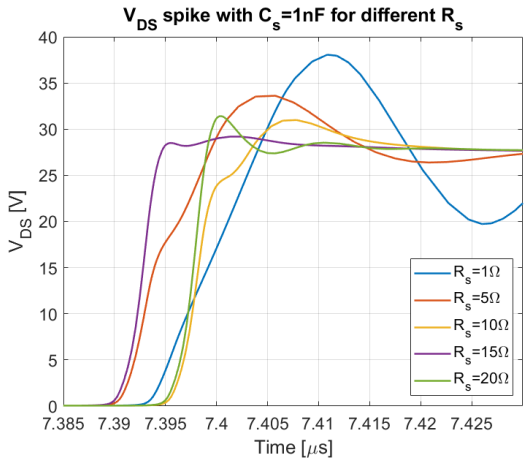

Figure E.3: Simulated waveform of drain-source voltage buck-boost for different resistor values.

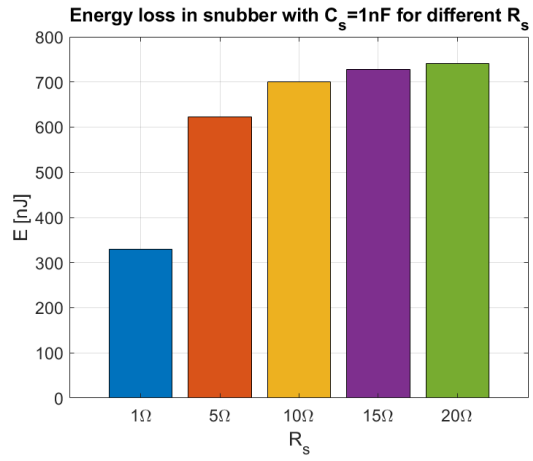

Figure E.4: Simulated energy loss in snubber of buck-boost for different resistor values.

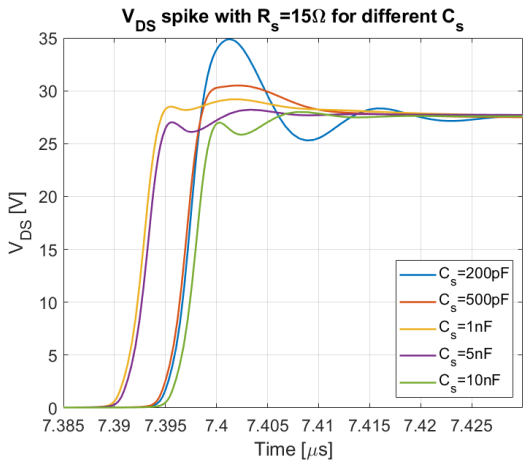

Figure E.5: Simulated waveform of drain-source voltage buck-boost for different capacitance values.

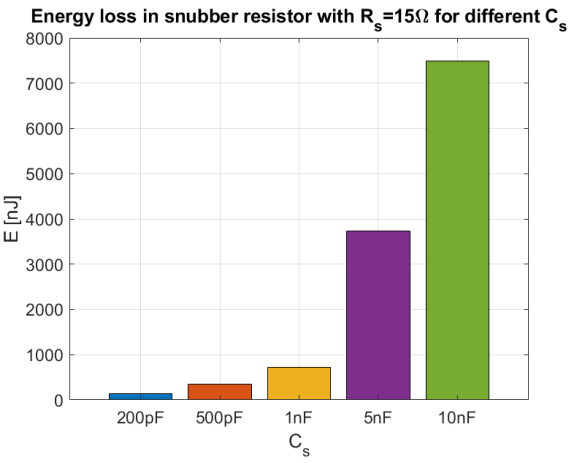

Figure E.6: Simulated energy loss in snubber of buck-boost for different capacitance values.

E.2.2 Snubber Interleaved Bidirectional Converter

The drain-source voltage and snubber losses of the interleaved bidirectional converter for a constant C_s = 1 nF and different R_s are shown in Figures E.7 and E.8, respectively. The same is shown in Figures E.9 and E.10, but for constant R_s = 4 Ω and varying C_s. Again, the same observations as for the buck and buck-boost converter are made and will not be repeated. However, the change in voltage overshoot is more sensitive to the values of R_s and C_s. Therefore, R_s is varied between 2 Ω and 8 Ω, and C_s between 200 pF and 5 nF.

From Figure E.7, a resistance of 4 Ω results in the lowest overshoot, but a small amount of ringing is present. A resistance of 5 Ω results in less ringing, but larger overshoot. By increasing the capacitance, both ringing and overshoot are reduced. Therefore, R_s = 4 Ω is preferred, because it has slightly lower losses. From Figure E.9, $C_s \geq 2$ nF to have sufficient overshoot reduction such that $V_{DS,peak}$ < 40 V. A capacitance of 2 nF is used. Compared to the 3 nF capacitance, the losses are reduced by 26.2% (1.76 µJ vs 1.30 µJ), while the overshoot is increased by 30.4% (9.45 V vs 12.32 V overshoot). The slightly larger overshoot is still acceptable because there is still a 6.68 V margin to the rated voltage of the switch. Using R_s = 4 Ω and C_s = 2 nF, the resulting average loss in the snubber resistance is $P_{sn} = E_{sn}F_s$ = 129.66 mW. At maximum load, this reduces the efficiency by 0.14%. Thus, the losses in the snubber resistance can be neglected.

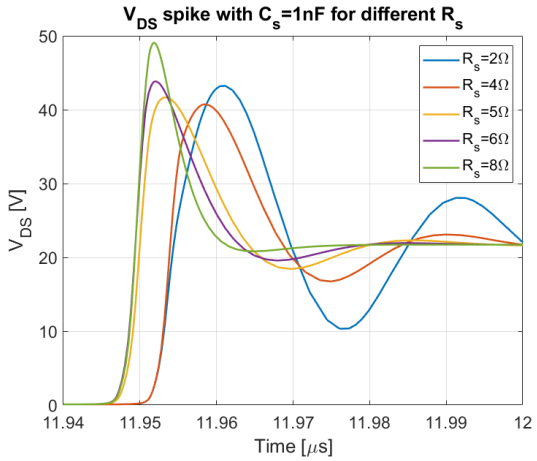

Figure E.7: Simulated waveform of drain-source voltage bidirectional for different resistor values.

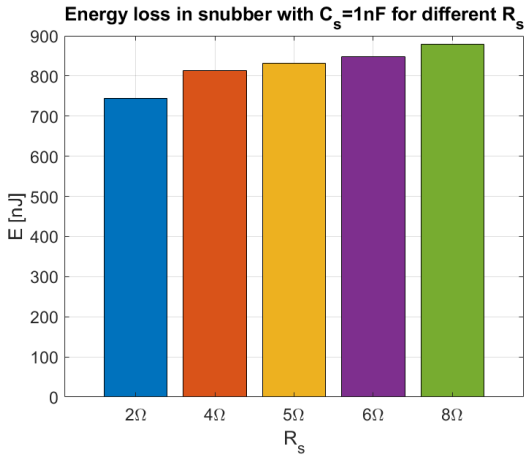

Figure E.8: Simulated energy loss in snubber of bidirectional for different resistor values.

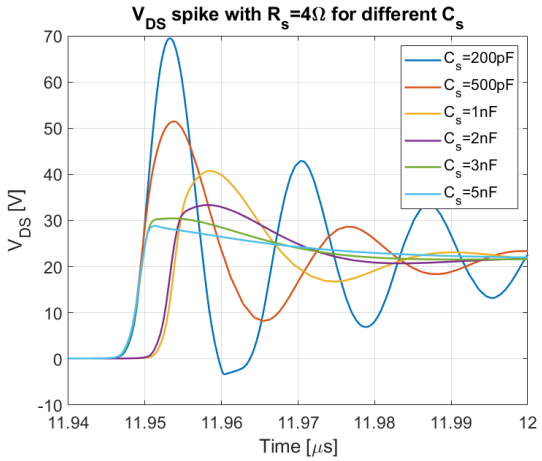

Figure E.9: Simulated waveform of drain-source voltage bidirectional for different capacitance values.

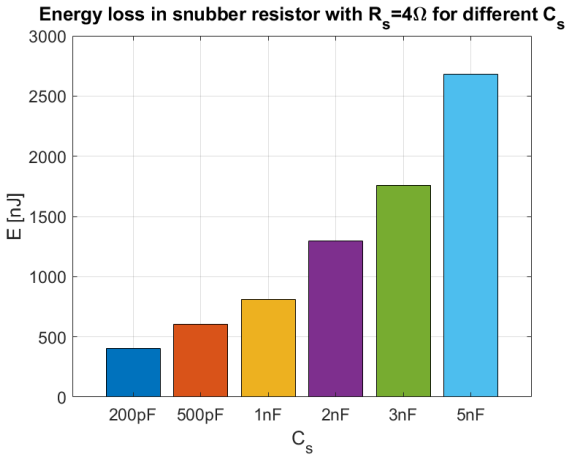

Figure E.10: Simulated energy loss in snubber of bidirectional for different capacitance values.