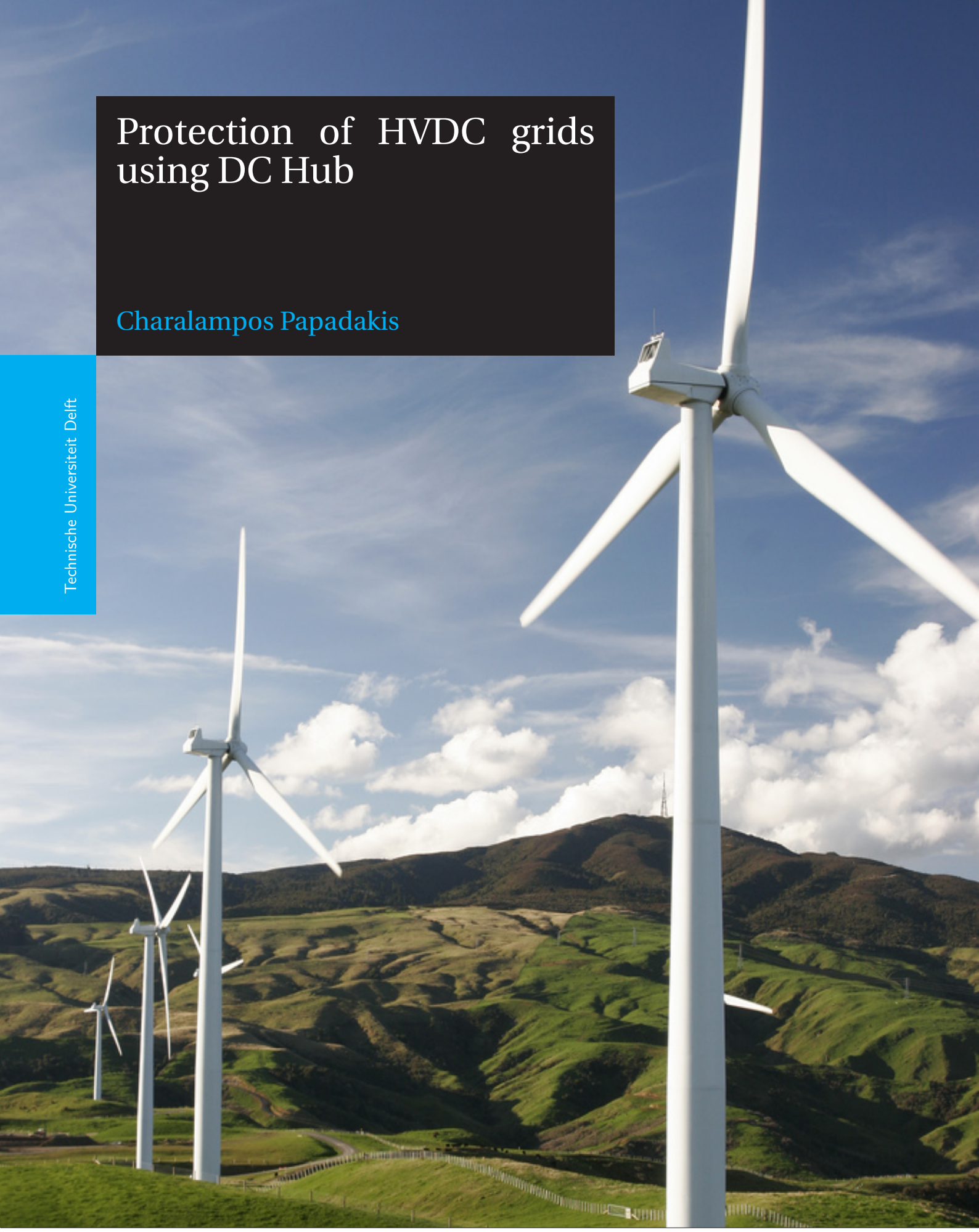
Protection of HVDC grids using DC Hub

Charalampos Papadakis

Technische Universiteit Delft



TU Delft Delft University of Technology

Challenge the future

PROTECTION OF HVDC GRIDS USING DC HUB

by

Charalampos Papadakis

in partial fulfillment of the requirements for the degree of

Master of Science
in Electrical Engineering

at the Delft University of Technology,
to be defended publicly on Thursday September 28, 2017 at 09:00 AM.

Supervisor:	Prof. dr. ir. Pavol Bauer	
Thesis committee:	Prof. dr. ir. Pavol Bauer,	TU Delft
	Dr. Zian Qin,	TU Delft
	Dr. Milos Cvetkovic,	TU Delft

TU Delft Delft University of Technology

ACKNOWLEDGEMENTS

This Master Thesis is my last big step towards obtaining the Master of Electrical Engineering at the Delft University of Technology. The project I have been working on for the last 10 months has been a great experience and many people have contributed to its successful completion.

First of all, I would like to thank Professor Pavol Bauer for giving me the opportunity to work on this project, for his support and guidance. I would like also to thank Epameinondas Kontos, my daily supervisor, for his enthusiasm, comprehension, and contribution to the project, his office door was always open whenever I ran into a trouble spot or had a question about my research.

To the friends I made during the last two years in the Netherlands, especially Anastasia, Kalliroi, Marina, Maya, Nadia, Aris, Alex, Dimitris, Dimitris, and Mike, thank you for the beautiful memories. The best is yet to come.

Finally, I must express my very profound gratitude to my parents Vasilis and Veta for providing me with unfailing support and continuous encouragement throughout my years of study and through the process of researching and writing this thesis. This accomplishment would not have been possible without them. Thank you.

Charalampos Papadakis
Delft, the Netherlands
September 2017

To my parents,

no one will ever know the strength of my love for you.

Haris

ABSTRACT

Nowadays there is a movement towards the creation of HVDC grids. The massive integration of renewable energy sources, the operation of the current grid close to its limits and the need to facilitate the power trade are some of the reasons driving the research on HVDC grids. Towards HVDC grids, there are still some obstacles and technical limitations to be confronted. To address these problems, the idea of a DC hub is introduced.

A DC hub is a multiport DC-DC converter, which serves as an actively controlled DC node. The basic parts of the DC hub are the ports, where AC/DC converters are used and the intermediate AC link. Until now there is no standardization of HVDC grids and thus, if different projects need to be interconnected a DC-DC conversion is necessary. A DC hub can offer solutions in the connection of HVDC lines with different voltage levels and different configurations. Moreover, it can facilitate the power exchange between any two HVDC lines connected in the DC hub. This thesis deals with the development of a DC hub model and its study under transient phenomena. More specifically, the ability of the DC hub to aid in the protection of HVDC grids is examined.

The first step to address this problem is to propose the most suitable multiport DC-DC converter topology. A literature review over different DC-DC converter topologies took place. The advantages, disadvantages and the ability to upgrade into a multiport DC-DC converter are examined. The most promising is the front-to-front topology where either a transformer or an LCL filter is used. In the current thesis, the front-to-front topology with an intermediate AC transformer is studied.

Before studying the DC fault response, the basic attributes of the DC hub must be acquired. A three-port DC-DC converter is designed where the state of the art modular multilevel converter is used in every port. The model operation is validated through step reference changes in the AC voltage, DC voltage, and active power. Moreover, the control role distribution is suggested, where the port with the higher power rating operates in AC voltage control mode. Being one of the main attributes, the connection/disconnection of a line without disturbing the operation of the DC grid is presented. For a smooth transition, the suggested steps are presented. The next step is to study the natural DC fault response of the DC hub. In the case of pole-to-ground faults, a design methodology is presented in order to acquire fault ride-through capability. Finally, the pole-to-pole fault contingency study leads to useful conclusions. A design methodology of adding large phase reactors between the converter and the transformer is suggested in order to limit the large fault currents.

The main contributions of this thesis are the following. First, a DC hub average model, using three modular multilevel converters in front-to-front configuration is provided. Moreover, the DC hub response to line connection/ disconnection is studied and steps are suggested for a smooth transition. Finally, after studying the natural DC fault response of the DC hub, the design requirements are provided in order to acquire a fault ride-through capability.

CONTENTS

List of Figures xi

List of Tables xv

1 Introduction 1
- 1.1 Motivation . . . 1
- 1.2 Objectives . . . 2
- 1.3 Main contributions . . . 3
- 1.4 Thesis structure . . . 3

2 DC-DC Converters 5
- 2.1 Different scenarios and parameters selection . . . 5
- 2.2 One Stage Converters . . . 6
- 2.3 Two-Stage Converters . . . 7
  - 2.3.1 Transformerless Topologies . . . 7
  - 2.3.2 Transformer Topologies . . . 8
- 2.4 DC Hub Literature . . . 10
  - 2.4.1 Two phase LCL DC Hub . . . 10
  - 2.4.2 Hybrid MMC-based DC Hub . . . 11
  - 2.4.3 Four-port DC Hub . . . 11
- 2.5 Conclusion . . . 12

3 Modular Multilevel Converter 15
- 3.1 General Overview . . . 15
  - 3.1.1 Submodules . . . 15
  - 3.1.2 MMC Components . . . 16
  - 3.1.3 Currents and Dynamics . . . 16
- 3.2 Averaging Principle . . . 17
- 3.3 Design Procedure . . . 18
- 3.4 MMC Control . . . 20
  - 3.4.1 Phase-Locked Loop . . . 20
  - 3.4.2 Higher-level control . . . 21
  - 3.4.3 Output-current control . . . 24
  - 3.4.4 Current Limiter . . . 25
  - 3.4.5 Arm-balancing control . . . 25
  - 3.4.6 Arm-level Average Model . . . 29
- 3.5 Summary . . . 30

4 DC HUB 33
- 4.1 Components Decision . . . 33
  - 4.1.1 Converter . . . 33
  - 4.1.2 Intermediate AC link . . . 34
  - 4.1.3 DC link configuration . . . 35
- 4.2 Port Design . . . 36
- 4.3 Control role distribution . . . 37
- 4.4 Model validation . . . 37
  - 4.4.1 Active power reference change . . . 38
  - 4.4.2 DC voltage reference change . . . 42
  - 4.4.3 AC voltage reference change . . . 44
- 4.5 Conclusions . . . 46

5 Port connection and disconnection **49**
5.1 Port Connection . . . 49
5.1.1 Case 1 connection of port operating in active power control mode . . . 49
5.1.2 Case 2 connection of port operating in DC voltage control mode . . . 52
5.2 Port Disconnection . . . 55
5.2.1 Case 1 Zero power in the DC hub . . . 56
5.2.2 Case 2 Full power in the DC hub . . . 57
5.2.3 Disconnection of port operating in AC voltage . . . 60
5.3 Conclusions . . . 66

6 DC Faults **67**
6.1 Introduction . . . 67
6.2 Protection system . . . 68
6.3 DC Faults causes and probability . . . 69
6.4 Pole-to-ground fault . . . 69
6.4.1 Pole-to-ground fault at port 1 . . . 70
6.4.2 Pole-to-ground fault at port 2 . . . 73
6.4.3 Pole-to-ground fault at port 3 . . . 74
6.5 Pole-to-pole fault . . . 76
6.5.1 Pole-to-pole fault at port 1 . . . 78
6.5.2 Pole-to-pole fault at port 2 . . . 84
6.5.3 Pole-to-pole fault at port 3 . . . 87
6.6 Conclusions . . . 88

7 Conclusions and Future Work **91**
7.1 Conclusions . . . 91
7.2 Future Work . . . 94

Bibliography **95**

LIST OF ACRONYMS

AC	Alternating Current
ALA	Arm-level Average
ALA-BLK	Arm-level Average Blocking
DAB	Dual Active Bridge
DC	Direct Current
F2F	Front-to-Front
HVDC	High Voltage Direct Current
MMC	Modular Multilevel Converter
PI	Proportional-Integral
PLL	Phase-Locked Loop
PR	Proportional-Resonant
PWM	Pulse Width Modulation
Q2L	Quasi 2-Level
SM	Submodule
VSC	Voltage-Source Converter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

List of Figures

1.1 Need to connect three different DC lines . . . 2
1.2 Two different approaches . . . 3

2.1 High power IGBT-based DC/DC converter . . . 8
2.2 MMC-based LCL DC-DC converter . . . 8
2.3 Two-phase LCL DC hub . . . 11
2.4 Hybrid MMC-based DC hub . . . 11
2.5 Four-port DC hub . . . 12

3.1 Single phase modular multilevel converter . . . 15
3.2 MMC control overview . . . 20
3.3 Phase-locked loop . . . 21
3.4 Active power controller . . . 22
3.5 Reactive power controller . . . 22
3.6 DC voltage controller . . . 23
3.7 AC voltage controller . . . 23
3.8 Phase reactor block . . . 25
3.9 Output-current controller . . . 26
3.10 Current limiter modes of operation . . . 26
3.11 Circulating-current controller . . . 28
3.12 Closed-loop voltage control . . . 28
3.13 Arm-level average model . . . 30
3.14 Arm-level average blocking model . . . 30
3.15 Port 1 and 2 control structure . . . 31
3.16 Port 3 control structure . . . 31

4.1 DC hub . . . 33
4.2 Symmetric monopole configuration . . . 35
4.3 Pi-equivalent line section model . . . 36
4.4 DC hub . . . 38
4.5 Values during changing active power reference . . . 39
4.6 AC currents in the intermediate link during changing active power reference . . . 40
4.7 Arm currents during changing active power reference . . . 40
4.8 DC voltages during changing active power reference . . . 41
4.9 Sum capacitor voltages during changing active power reference . . . 41
4.10 DC currents during changing active power reference . . . 41
4.11 Values during changing DC voltage reference . . . 42
4.12 DC voltages during changing DC voltage reference . . . 43
4.13 Sum capacitor voltages during changing DC voltage reference . . . 43
4.14 AC currents in the intermediate link during changing DC voltage reference . . . 44
4.15 Arm currents during changing DC voltage reference . . . 44
4.16 Values during changing AC voltage reference . . . 45
4.17 AC currents in the intermediate link during changing AC voltage reference . . . 45
4.18 Arm currents during changing AC voltage reference . . . 46
4.19 DC voltages during changing AC voltage reference . . . 46
4.20 Sum capacitor voltages during changing AC voltage reference . . . 46

5.1 AC breakers in the DC hub . . . 49
5.2 Connection of port 2 . . . 50

5.3 AC currents on the intermediate link . . . 51
5.4 DC link voltages at each port . . . 51
5.5 Active power at each port . . . 51
5.6 Comparison of values with insertion resistors . . . 52
5.7 Connection of port 1 . . . 53
5.8 AC currents of the intermediate link . . . 53
5.9 DC link voltages at each port . . . 53
5.10 Values during port 1 connection . . . 54
5.11 Comparison of values with insertion resistors . . . 55
5.12 Disconnection of port 2 with zero power . . . 56
5.13 AC currents of the intermediate link . . . 57
5.14 Values during disconnection of port 1 with full power . . . 58
5.15 AC currents during disconnection of port 1 with full power . . . 58
5.16 Arm currents during disconnection of port 1 with full power . . . 58
5.17 DC voltages during disconnection of port 1 with full power . . . 59
5.18 Active power . . . 59
5.19 AC currents during disconnection of port 2 with full power . . . 60
5.20 DC voltages during disconnection of port 2 with full power . . . 60
5.21 AC voltage during port 3 disconnection . . . 61
5.22 Disconnection of port 3 and AC voltage control change . . . 61
5.23 DC values of port 1 and 2 . . . 62
5.24 Active power during port 3 disconnection . . . 63
5.25 DC values of port 1 and 2 . . . 63
5.26 Current values at full power change . . . 64
5.27 DC currents of port 1 for different power levels of port 1 . . . 64
5.28 DC currents of port 2 for different power levels of port 1 . . . 65
5.29 DC voltages of port 2 for different power levels of port 1 . . . 65

6.1 DC hub in case of DC faults . . . 67
6.2 Protection system . . . 68
6.3 Pole-to-ground fault with two-level VSC . . . 70
6.4 Pole-to-ground fault with MMC . . . 70
6.5 Values during a pole-to-ground fault on port 1 . . . 71
6.6 AC voltages at the faulty port . . . 72
6.7 Comparison for different fault locations . . . 72
6.8 Comparison for different fault resistances . . . 73
6.9 Pole-to-ground fault at port 2 . . . 74
6.10 Sum capacitor voltages at port 2 . . . 75
6.11 AC voltages at the faulty port 3 without transformer . . . 75
6.12 Pole-to-ground fault at port 3 . . . 76
6.13 Equivalent circuit . . . 77
6.14 DC fault stages . . . 78
6.15 AC currents during pole-to-pole fault . . . 79
6.16 Arm currents during pole-to-pole fault at port 1 . . . 80
6.17 Port 2 DC values during pole-to-pole fault on port 1 . . . 80
6.18 Port 3 DC values during pole-to-pole fault on port 1 . . . 80
6.19 Sum capacitor voltages of port 3 . . . 81
6.20 AC voltage during fault pole-to-pole on port 1 . . . 81
6.21 Phase reactor effectiveness on limiting the arm current peaks at port 1 . . . 82
6.22 Arm currents of port 1 for different phase reactor values . . . 82
6.23 Values with phase reactor during pole-to-pole fault at port 1 . . . 83
6.24 Values with phase reactor during pole-to-pole fault at port 1 . . . 83
6.25 Values with phase reactor during pole-to-pole fault at port 1 . . . 84
6.26 Values with phase reactor during pole-to-pole fault at port 1 . . . 84
6.27 Values with phase reactor during pole-to-pole fault at port 1 . . . 84
6.28 Phase reactor effectiveness on limiting the arm current peaks at port 3 . . . 85

6.29 Values with phase reactor during pole-to-pole fault at port 2 86
6.30 Values with phase reactor during pole-to-pole fault at port 2 86
6.31 Values with phase reactor during pole-to-pole fault at port 2 87
6.32 Comparison of arm currents based on blocking times 88

List of Tables

3.1 Controller gains 29

4.1 DC line parameters 35
4.2 Port values 36
4.3 Component values 36
4.4 Different scenarios in control role distribution 37
4.5 DC hub parameters 38
4.6 Power reference steps 40
4.7 DC voltage reference steps 42
4.8 AC voltage reference steps 44

6.1 Port values and control modes 67
6.2 Protection threshold values 69
6.3 Fault location 71
6.4 Transformer configurations and fault ride-through capability 74
6.5 Phase reactor effect on pole-to-pole fault on port 1 82
6.6 Arm current values of port 3 85

1

INTRODUCTION

This chapter describes the background and motivation for the thesis. The objectives and the contributions, as well as the thesis outline are also presented.

1.1. MOTIVATION

HVDC TRENDS

Nowadays there is a movement towards the creation of HVDC grids.The research for HVDC grids is driven by the massive integration of renewable energy sources, while these energy sources are mainly located far from the load centers. Moreover, the current grid is operated close to its limits and there is a need for new lines construction. Also, there is a need to facilitate power exchange and trade between regional power systems. Finally, additional flexibility and security in the power systems are necessary. The most optimists can see a European Supergrid in the future, however, this project will require many years to be completed. To built such a meshed multiterminal grid, the VSC-HVDC technology is the most suitable for the reasons stated in [1]. Small steps of this big plan are today taken as more and more HVDC point–to–point lines are commissioned all over the world.

HVDC GRID OBSTACLES

Although HVDC grids have several advantages, there are still some obstacles and technical limitations to be confronted. One major obstacle in the DC systems is the protection which is more demanding comparing to the AC systems protection[2]. The DC cable resistance is lower, leading to high-short circuit current with a steep waveform. Additional reactors can be used in order to limit this current rise. Moreover, DC current does not pass through zero, and thus instantaneous switching is complicated while, the arc created is not easily extinguished. Also, the power electronic components of the converters being used are very sensitive to overloads and should be protected against overcurrents.

The operation of DC circuit breakers is more demanding and when a fault occurs is not acceptable to disconnect the entire DC backbone. That is why more research is needed. The basic requirements of the DC breaker can be distinguished as follows: [3]. First, an opposing voltage needs to be created to bring down the fault current to zero. Second, the energy stored in the inductance of the system needs to be dissipated. Third, after the current interruption, the circuit breaker needs to withstand the voltage response of the network. These three requirements cannot be met by a single element this is why different devices are connected in parallel. The three basic types of DC breakers are the mechanical, the semiconductor based and the hybrid DC circuit breaker.

CONTROL DEMANDS IN DC GRIDS

Additionally to the advanced protection requirements, DC grids need a demanding power flow control. Renewable energy power sources are essential components of the DC grid and their intermittent character requires a more complex and demanding control. Moreover, having a diversified portfolio of renewable energy sources, an effective control results in a power generation profile of lower variability while introducing additional flexibility to the power system. A basic difference with the conventional AC grids is the control inertia. In DC grids where power electronic converters are used and slow governors and generator exciters are absent,

the control time constants are much smaller. This requires a more complex control but also offers opportunities for optimization [4]. Another difference is that the frequency as global constant no longer exists, instead, the DC voltage should be monitored and controlled. Usually, a converter will be responsible for the DC voltage control while the others will control their local powers.

DIFFERENT STANDARDS

Today there is still an absence of common standards and there is not an established grid code for the DC grids. Also, there are different design approaches by the major manufacturers. Moreover, at each iteration of the technology, the cable ratings rise. As a result, DC lines will differ not only in magnitude but also in configuration. As a result, elements similar to AC transformers for AC grid are needed to connect different DC line configurations e.g. symmetric bipolar with symmetric monopolar.

NECESSITY OF DC HUB

In order to create a DC grid there is need to connect different point-to-point transmission lines. The obstacles towards a large DC grid are the needs for HVDC breakers, a reliable power flow control and the connection of regional systems with different characteristics. As can be seen in figure 1.1 there is a point in a DC grid where 3 different lines need to be connected. This DC node must have some special features. As the DC lines to be connected may have not only different voltages but also different configurations. Two different approaches are presented.

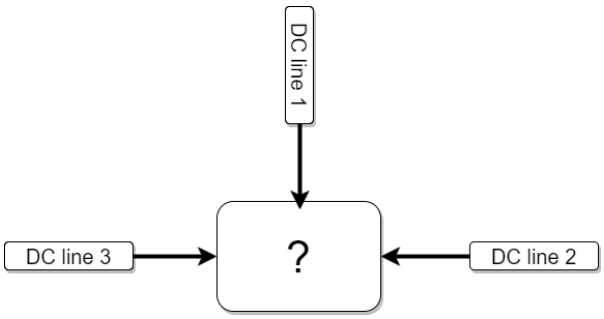


Figure 1.1: Need to connect three different DC lines

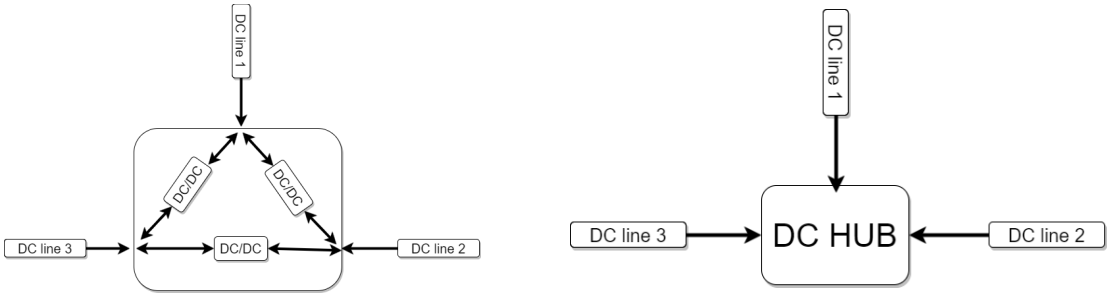
DC/DC converters approach This problem can be solved by using DC-DC converters for the interconnection of each DC line. In this case, three DC-DC converters are needed in total. However, there must be communication in order to control reliably the power flow. If an extra interconnection is to be made, an extra DC-DC converter will be needed for the connection of the new line to each of the existing ones. This increases the cost and makes the protection more complex. When there is need to interconnect more than three lines this approach is not flexible and reliable.

DC Hub approach The approach of using an element where all DC lines can be connected directly seems more viable. Such a solution is a DC node seen in the literature as DC hub. This is an expanded DC-DC converter topology into a multiport where the presence of an intermediate AC link can be of great benefit in the protection of the DC grid. AC circuit breaker located in the intermediate AC link can be used to interrupt DC faults instead of using DC breakers. In comparison with DC circuit breakers, AC circuit breakers is a more mature technology and less expensive. Moreover, the DC hub approach offers the advantages of reliability and expansion flexibility. This key element can be placed strategically in a DC grid while offering DC voltage transformation, fault ride-through capabilities and more control options.

1.2. OBJECTIVES

This thesis mainly focuses on the implementation of a modular multilevel converter to high power high voltage, multiport DC/DC converters. The objectives of the current thesis are:

- Design of a three-port DC-DC converter (DC Hub).
- Analysis of the DC hub response to a line connection/disconnection.



(a) DC-DC converters approach

(b) DC hub approach

Figure 1.2: Two different approaches

- Analysis of the natural fault response of the DC hub.
- Specify the design requirements in order to provide fault ride-through for different DC fault types.

1.3. MAIN CONTRIBUTIONS

The main purpose of this work is to study the operation of high voltage, high power multiport DC-DC converter during transient phenomena. The thesis contribution is to provide a DC hub average model using three modular multilevel converters in front-to-front configuration. The model is first verified for normal operation and the main attributes of a DC hub are acquired. Moreover, the created model is studied during line connection/disconnection. For a smooth transition, design and operation steps are suggested. Following, in comparison with DC hub studies already performed in the literature, the pole-to-ground fault is studied and the fault ride-through capability of the DC hub according to a specific design is presented. Finally, after studying the natural pole-to-pole fault response, a design methodology is proposed in order to limit the large fault currents.

1.4. THESIS STRUCTURE

In this first chapter, the motivation and the objectives of this thesis are explained. In order to meet the objectives, the thesis is structured as follows:

Chapter 2 presents the development of high power high voltage DC-DC converters. The different topologies are categorized and their ability to expand into multiport DC-DC converters is studied. Following, the different DC hub topologies studied so far in the literature are presented.

Chapter 3 presents the operation principles of MMC. Next, the design procedure of the converter is presented. The averaging principle is introduced, in which the control model of MMC is based. The different control levels of the MMC are presented and the Arm-level average model is discussed.

Chapter 4 explains the decisions made for the components of the DC hub. The choices for the converter, the intermediate AC link, and the DC link configuration are discussed. Moreover, the control role distribution is presented. Following, the created model is verified in normal simulation through step reference changes in the controlled values of AC voltage, DC voltage, and active power.

Chapter 5 studies the transient response in the DC hub during a connection and disconnection of a port. Steps for a smoother transition are suggested. In case of disconnecting the port responsible for AC voltage control, the capability of the system to maintain its operation is demonstrated. All the ports were studied for disconnection in two scenarios, the zero-power, and the full-power scenario.

Chapter 6 studies the natural fault response of the DC hub. Furthermore, a design methodology is proposed in order to acquire fault ride-through capability during a pole-to-ground fault. Next, after studying the response on the more severe pole-to-pole fault, a methodology is presented in order to limit the large fault currents and acquire a fault ride through capability.

Chapter 7 presents the summary of the thesis with conclusions and possible topics for future work.

2

DC-DC CONVERTERS

A DC-DC converter in a DC transmission system is related to the transformer in an AC transmission system. The basic functions of the DC-DC converter in a DC grid are the following. First, matching the different DC voltages. Currently, there is an absence of common standards and at each iteration of technology the cable ratings are rising, leading to different voltage level lines. Also, there is a difference in voltage levels between cables and overhead lines. Second, the power flow can be regulated. Third, another function that a DC-DC converter can have is to interrupt DC fault current. Finally, it has the ability to split a large DC grid into several protection zones.

2.1. DIFFERENT SCENARIOS AND PARAMETERS SELECTION

There are many DC-DC converters, where different applications will favor different topologies. As seen in [5] there are three different scenarios.

1. In the first scenario, DC/DC converter is used for the connection between a medium voltage collector grid and the HVDC transmission grid. The basic requirement for this topology is high voltage ratio. In this scenario the voltage level is medium.

2. These converters are used to connect HVDC and Ultra-HVDC, usually connecting load centers directly to higher voltage onshore connection points. The requirements are medium voltage ratio, high voltage level, DC fault protection and high efficiency.

3. Finally, there is a connection between different DC grids that requires low voltage ratio, high voltage level, and bidirectional power flow.

There are many applications where a DC-DC converter can be used. A variety of applications results in a variety of possible designs. The first classification of a DC-DC converter takes place in [6], where the basic parameters for selecting the desirable converter are presented

- Power rating
- Voltage Ratio
- Needs for galvanic separation
- Fault blocking capability
- Quadrants of operation

Other desired feature may be the ability to connect VSC and LCC technologies. Finally, one parameter for the selection of the DC-DC converter may be its ability to expand into the multiterminal topology. The decisive factors that determine the viability of a high-voltage DC-DC converter are the semiconductor losses, footprint, and initial cost. The performance under fault conditions is a secondary issue. The literature research will focus on different DC-DC converters for high voltages and look for their ability to upgrade into a DC hub.

Looking through the literature review a first categorization of the DC-DC converters is the number of conversion stages they have. There are two categories, the two-stage, where there is an intermediate AC link and

two AC/DC converters are used. The other category is the one-stage, which has no distinct intermediate AC link. The major advantage of the one stage topologies over the two-stage is that one converter is used instead of two resulting in a lower number of semiconductor devices leading to lower volume, weight, and cost. The two-stage topology or the front-to-front topology as it is alternatively named can be further classified based on the intermediate AC link to transformer and transformerless configurations.

The intermediate AC link of the F2F topology can have two phases or more. Usually, when more power is required in the AC link than the current cables can handle, more than three phases are used. Moreover, if the intermediate AC link is not connected to an AC grid, it can have higher frequencies resulting to lower dimensioning of the passive elements used. Also, the waveform of the AC link can have a different form than sinusoidal, for example, squared or trapezoidal.

2.2. ONE STAGE CONVERTERS

The one stage converters do not have a distinct AC link. The major advantage is the lower number of semiconductor devices resulting in lower volume, weight, and cost. However, the one-stage converters lack modularity and upgrading into a DC hub is more complex. The major representatives of DC-DC converters are following presented.

MODULAR MULTILEVEL DC CONVERTER

A first representative of the one stage topology is the multilevel modular DC converter presented by J.A. Ferreira in [7]. In this new topology, a secondary loop is introduced in the conventional topology of MMC in order to exchange power with the primary power loops at the input and output. The decoupling of active power at different frequencies is based on the principle of orthogonal power flow. In order for the average power in the capacitor to be zero, the primary and the secondary currents on the DC side of the converter need to be equal with opposite sign. The topology is not that promising for DC-DC conversion, as it requires large filter component.

In [8] a comparison between the modular multilevel converter and the dual-active bridge is presented. The results showed that the efficiency of M2DC for high voltage ratios is low while when the voltages diverge for a small percentage, the efficiency is really high. The push-pull version requires a similar amount of magnetic component for its filtering as the DAB converter, which makes it noncompetitive for high voltage applications.

BIDIRECTIONAL DC POWER FLOW CONTROLLER

Another converter which can be categorized in the one stage DC-DC converters is a bidirectional power flow controller presented in [9]. The converter consists of interleaved strings. Each string has two arms and each arm is divided to an inner and an outer arm. The arm can have cascaded sets of HB or FB cells and an arm choke. There are inductors that link the strings together in order to establish AC circulating currents. There are input and output filters, where the output inductances are coupled with a large value. Also, capacitors are used to sink any high frequency currents. There are two modes of operation step-up and step-down. Circulating AC currents ensure power balance for the SMs capacitors, a technique similar to M2DC presented in [7]. Again a big disadvantage is the large value of the output filter inductance and capacitance in order to attenuate the fundamental AC voltage components from each phase voltage.

Concluding these one stage converters are not that competitive for DC-DC conversion as the conduction losses due to the secondary AC current are high and the filter requirements are increased. Also, these topologies may have difficulties in upgrading to a DC hub.

HVDC AUTOTRANSFORMER

Another single stage topology, different than the previous ones is the HVDC-DC autotransformer presented by Schon and Bakran in [10]. The proposed topology of the HVDC-DC Auto-Transformer is a single stage DC-DC converter resulting in a smaller footprint. Two MMC converters are connected in series creating the high voltage DC side. From the two subconverters, the lower one corresponds to the low voltage DC side. There is also an AC link connection between the upper and lower subconverter with an AC transformer. The conversion losses and the power rating of the installed transformer can be minimized thanks to the fact that only a fraction of the actual DC-DC power has to be converted.

A comparison takes place in [10] between the newly proposed topology and the F2F MMC. It is shown

that in all the cases the HVDC-AT has lower semiconductor effort and higher transferable DC power. In order to interrupt DC currents additional components are needed and depend on the transformation ratio. In the optimum transformation ratio of two, it can transfer twice the DC power of the conventional F2F topology. HVDC-AT is an efficient solution as the transformer used is smaller and has better switching utilization ratio, however, it exposes to high voltage stresses the transformer's windings and in order to prevent DC fault propagation needs the HB cells of the outer arms to be replaced by FB.

HYBRID CASCADED DC-DC CONVERTER

Following, a more recent concept of converters that can be classified as one-stage is the Hybrid Cascaded DC-DC converter presented in [11]. The proposed converter is a polyphase structure, where each phase consists of a controllable switch and an energy storage device. The controlled switch is a build up from IGBTs in series similar to a 2-Level converter switch, it has two switches in an arm. While the storage device is created by cascaded half-bridge submodules like an MMC arm. In order to avoid power flow interruption more than one phase is used. Through the converter operation, it is shown that it can realize soft-switching thanks to the highly controllable SMs. The energy variation of the SMs in one period should be zero in order to assure energy balancing of the SMs. Although the switching losses are low, there are many semiconductor devices in the conduction path and the RMS current is high, leading to higher conduction losses. Also in [11] a comparison with M2DC showed that parallel two-level (P2L) does not look promising to replace M2DC.

UN-ISOLATED MODULAR DC-DC CONVERTERS

The most recent attempts to reduce the footprint of the DC-DC converter by using single stage topology can be seen in [12, 13]. The proposed method is to use the traditional DC/DC converters (buck, boost, buck-boost) and replace the 2 complementary semiconductor switches with 2 chains of submodules (chainlinks). Their operating principle and control strategies are similar to the conventional DC/DC converters. In order to decrease the stresses of the derivative of voltages during transitions, the stepped 2-level modulation is introduced. The transition time must be much lower than the switching period in order not to affect the basic operation principle of the converter. Also with the stepped 2 level modulation, the SM capacitor voltages can be balanced using the same sorting method as in the conventional MMC. In comparison with the M2DC [7, 9] seen previously having sinusoidal modulation, where the amplitude of the AC circulating current is lower, decreasing the switching and conduction losses. Moreover, as the required capacitance of the SMs is decreased, the volume and cost of the SMs also decrease.

2.3. TWO-STAGE CONVERTERS

The following large category of DC-DC converters are the two-stage converters. In this topology, two AC/DC converters are connected front-to-front, having an intermediate AC link. The first to introduce this concept was De Doncker in [14, 15] based on the dual active bridge converter. These converters can be further classified according to their intermediate AC link:

- No use of transformer, use of simple L filter or LCL filter
- Use of transformer

2.3.1. TRANSFORMERLESS TOPOLOGIES

Transformerless topologies with a simple inductance as an intermediate AC link can be used in low transformation ratios while in medium and higher ratios the use of a transformer is inevitable. The only advantage of the simple L filter is that the huge AC transformer is avoided, however, there are many disadvantages. First of all, there is no galvanic separation to act as a firewall stopping a fault on one DC system to propagate to the other DC system. Moreover, the use of a transformer offers better switching utilization and minimizes the circulating reactive power in the AC link. The main representatives of transformerless topologies are presented next.

BIDIRECTIONAL, HIGH-POWER DC TRANSFORMER

An LCL filter in the intermediate AC link was first introduced by Jovcic in [16]. The bidirectional, high-power DC transformer presented is a first representative of the resonant based transformerless topologies. Two topologies are presented, the bidirectional converter with voltage polarity change ($V_1 < V_2$) and the bidirectional with current polarity change. In both topologies, there is a common energy storage capacitor which is

centrally grounded. Consideration should be taken when choosing the capacitor as its peak voltage should be 20 – 30% higher than the high side voltage. Furthermore, the thyristor-based resonant converter is a frequency controlled element and the passive parameters are difficult to be designed.

HIGH POWER IGBT-BASED DC/DC CONVERTER WITH DC FAULT TOLERANCE

Continuing, in[17] the thyristors of the resonant converter are replaced with IGBTs as can be seen in figure 2.1. Compared to the previous thyristor-based converter higher efficiencies can be achieved with lower size and weight. The following benefits of a well-designed LCL circuit are mentioned: 1) inherent power reduction which does not depend on protection circuits, 2) considerably lower cost of LCL components compared with semiconductors, 3) the capability to maintain converter control even during the worst case faults. Thanks to the internal voltage stepping by the LCL filter the voltage stresses on the switches is low and comparable to the converter with the internal transformer. However, being single phase leads to large DC current ripple and lowers the ability to transfer high levels of power. Also, it has no electrical isolation and it steps DC voltage symmetrically around the central point and therefore it cannot be used with asymmetric monopole HVDC.

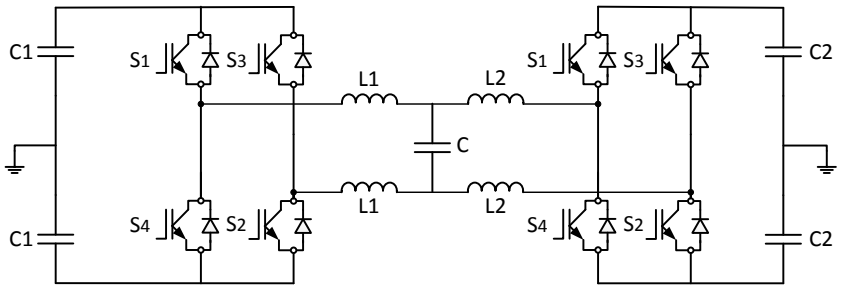


Figure 2.1: High power IGBT-based DC/DC converter

MMC-BASED LCL DC-DC CONVERTER

As being state of the art, offering higher reliability, higher power quality, lower power losses and having a modular structure, the modular multilevel converter was also introduced in resonant topologies, as shown in figure 2.2. MMC aided these resonant topologies to have higher efficiencies for all the transformation ratios. In [18] is presented a MMC-based LCL DC-DC converter having unity transformation ratio, fault-tolerant capability, and high efficiencies.

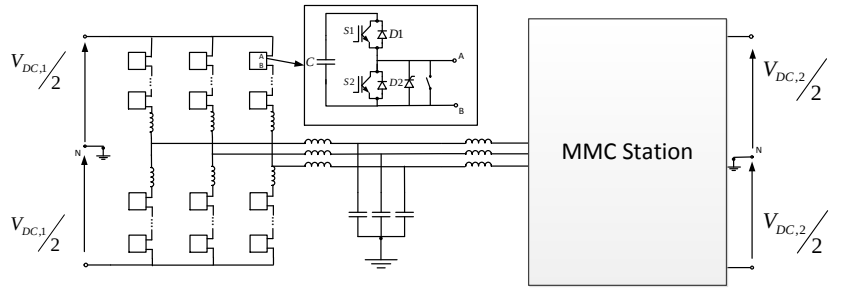


Figure 2.2: MMC-based LCL DC-DC converter

2.3.2. TRANSFORMER TOPOLOGIES

The DC-DC converter topologies found in bibliography where a transformer is used are next presented.

TWO-LEVEL DUAL ACTIVE BRIDGE CONVERTER

The two-level DAB converter is presented in [15]. The basic advantages of DAB are the lower dc-link currents and decreased turn-off losses. It is composed of two three-phase bridges with IGBTs and antiparallel diodes and an intermediate three-phase transformer. It has the ability to transfer power bidirectional between the

two bridges by controlling the load angle φ. The two-level DAB is usually operated in a square wave mode where each arm conducts for 180^o creating a six-step voltage waveform to the transformer. Thanks to ZVS and ZCS the turn-on losses of the switches and the turn-off losses of the diodes are basically zero. Furthermore, the switching losses can be reduced by using snubbers. In order to minimize the circulating reactive power in the AC link instead of using pulse width modulation resulting in higher switching losses, low-frequency modulation schemes like selective harmonic elimination (SHE) are used. The major problem of this topology is that in higher operating voltages, the rate of change of voltage stressing the intermediate transformer is too high. These high voltages impressed to the transformer request a more challenging design.

MULTI-MODULE DC-DC CONVERTERS

Another category is the Multi-module DC-DC converter. This topology has a modular structure comprising of DC-DC converter cells. There can be used bidirectional or unidirectional power flow DC-DC converter depending on the application. Some of the bidirectional converters are the dual active bridge, the dual half bridge, and the series resonant converter where each has its advantages and disadvantages [19]. The control philosophy of each module is individual and as a result, different technologies of power production and storage systems can be connected to the input. Usually, the cells of one input are connected in series while in the other in parallel. Higher fundamental frequencies can be used and soft-switching operation will result in low component volume without significantly reducing the efficiency. The dominant disadvantage of this topology is the high number of low power transformers with increased isolation requirements, increasing the volume and cost of the total system.

ISOLATED MODULAR DC-DC CONVERTER

The great advantages of the modular multilevel converter (MMC) over the conventional two-level VSC are discussed and since MMC has a high efficiency it was next to be used in a front-to-front DC-DC converter topology. This converter can be seen in [20] and its main features are the low switching losses and low voltage stresses on the isolation transformer compared to the two-level DAB. Also, during DC faults and during black-start the full modulation index range is available for voltage control in the AC link.

QUASI-TWO-LEVEL OPERATION OF MMC

As mentioned earlier, the intermediate AC link can have higher frequencies in order to reduce the volume and cost of the passive components but can also have a different waveform from the traditional sinusoidal or square waveforms. An obstacle in increasing the DC link voltages is that the derivative of voltages on the intermediate AC transformer is destructive, requiring special isolation design. A solution to this problem can be seen in [21] where an MMC with trapezoidal waveform is used. A new design of DC-DC converter is the Quasi-Two-Level operation of two modular multilevel converters (MMC) in F2F configuration. With this modulation technique, the semiconductor losses are decreased and the footprint is smaller. A disadvantage of the Q2L mode is that the modulation index control range gets narrower.

FRONT-TO-FRONT TOPOLOGIES WITH NEWLY PROPOSED AC/DC CONVERTERS

So far the basic topologies of DC-DC converters were discussed. More recent concepts replace the AC/DC converters seen in the F2F configuration with new innovative hybrid concepts. The VSC-HVDC converters can be classified into two categories:

1. The low-pulse number converters with PWM (two-level VSC).

2. The very high pulse number, multilevel converters (MMC).

Each category has advantages and disadvantages and an effort of combining the desired characteristics of the two can be seen in [22]. The MMC converter can achieve better harmonic distortion, eliminating the need for AC filters. Also, the switching losses are lower thanks to reduced switching frequencies. However, the number of IGBTs is doubled compared to the 2-level converter. Another disadvantage is that the total stored energy of DC capacitors is larger in the MMC compared to the 2-level. The building blocks of these new hybrid converters are the series switch, half-bridge cells, and full-bridge cells. The technique of relatively small MMC as active filters or wave-shaping circuit is used. The different combinations of these elements in series or in parallel lead to new innovative designs.

- **Hybrid cascaded two-level converter.** The wave-shaping circuit is located on the AC side [23]. The use of full-bridge modules offers reverse blocking capability during DC fault. However, the large number of switching devices in conduction path leading to increased conduction losses makes this converter not prominent for DC-DC high-voltage converters use.

- **Alternative Arm MMC.**Following, the wave-shaping circuit is on the DC side creating an alternative arm MMC as stated in the bibliography [24]. There is no path for circulating currents leading to more efficient utilization of the devices. The efficiency is low due to a large number of switching devices in the conduction path. This configuration is less likely to be adopted in DC-DC high voltage converters.

- **Controlled Transition Bridge.**A recently proposed topology for AC-DC conversion is the controlled transition bridge presented in [25]. The CTB-DAB operating in Q2L is a good solution as it has low semiconductor losses, small footprint, and low initial cost. Still, further research is required for the implementation of this hybrid converter in F2F topologies.

- **Transition Arm Multilevel Converter operating in Q2L.** From a comparison taking place in [26] between Q2L TAMC and CTB, it is shown that TAMC has a smaller footprint, lower silicon area, and higher efficiency. An advantage is that IGCTs can be used in the bi-state arms, while a challenge remains the transformer design. These results show that TAMC is a promising design for a DC-DC converter in high voltages.

2.4. DC HUB LITERATURE

Similar to the AC substation in AC grids, the DC hub can be viewed as a DC substation in DC grids. The main objectives of the DC hub are the following [27]:

- It enables the interconnection of multiple HVDC lines at different voltage levels.

- Any HVDC line can controllably exchange power with any other line connected to the DC hub

- It offers connection points for expansion. Any number of new ports can be added to the DC hub.

- Any HVDC line can be easily connected or disconnected from the DC hub without disturbing the operation of the DC grid.

- It offers DC fault clearance using AC breakers on the AC lines of the DC hub.

The fact that the DC hub concept is very recent, results in very few studies seen in the bibliography. These studies of different approaches for the creation a DC hub are following presented.

2.4.1. TWO PHASE LCL DC HUB

The very first DC hub topology is presented in [27] and can be seen in figure 2.3. Two-level VSC converters with PWM modulation control are used, connecting DC lines with different DC voltage levels. Also, the LCL filter technique is used and each converter has its own inductance and capacitance. Mechanical AC circuit breakers are assumed to be used after the LCL filter of each converter. By controlling the d-q components of PWM modulated control signals the reactive and the active power of each port can be independently controlled respectively. With an optimal design of the inner LCL filter, the reactive power at the converter bridge of each port can be minimized only when maximum power is achieved. The frequency in the intermediate link is higher than 50Hz in order to decrease the passive components' size, however, this will lead to higher switching losses. It is important for the operating frequency to be chosen further away from the global and local resonance frequencies in order to avoid prolonged oscillations. Furthermore, it is shown that the voltage and power of each port depend only on its own L, C parameters. This gives the ability to connect or disconnect any DC line in the hub without affecting the others. Finally, the capability to ride through DC faults is presented in [27].

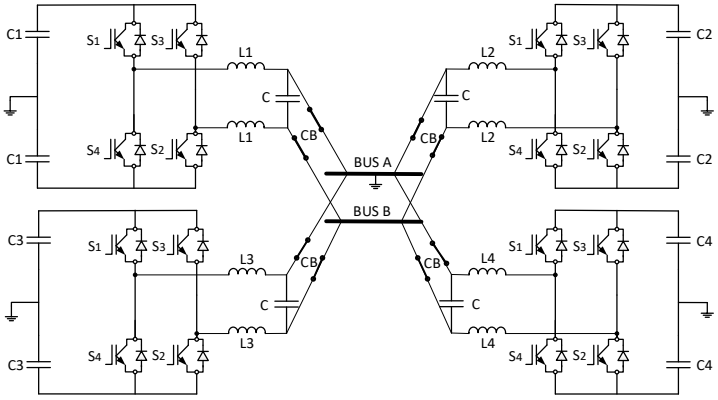


Figure 2.3: Two-phase LCL DC hub

2.4.2. HYBRID MMC-BASED DC HUB

Another topology seen in the bibliography and can be categorized as DC hub is presented in[28]. Three hybrid modular multilevel converters are connected to a three-phase three-winding AC transformer as shown in figure 2.4. The MMC converters have in each phase a chainlink of full-bridge submodules which will benefit in case of a fault. As it concerns the control method, each subconverter can operate in AC voltage, DC voltage or active power regulation modes. One of them must control the AC voltage of the intermediate AC link. A soft start is proposed which minimizes the oscillations and surge currents, improving the start-up performance. During a fault, the continuous operation capability of this topology can be seen. Only the faulted converters are blocked while the rest of them continue their operation without interruption.

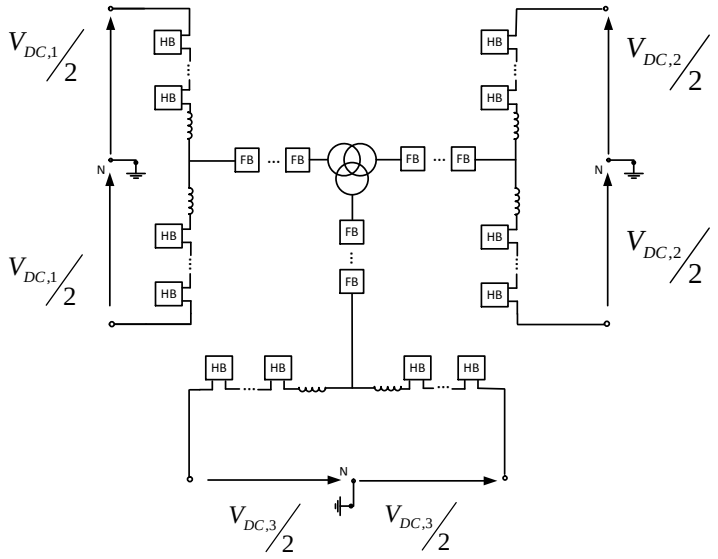


Figure 2.4: Hybrid MMC-based DC hub

The design of this three-winding three-phase transformer for high voltages will be demanding and occupy a lot of space increasing the system's footprint. Moreover, while the use of this transformer can reduce the total footprint instead of using three two-winding transformers, the addition of a new DC line seems difficult due to the presence of the three-winding transformer. Concluding, the full-bridge submodules are used instead of AC circuit breakers in order to connect or disconnect the line with the rest of the DC Hub.

2.4.3. FOUR-PORT DC HUB

Following, a four-port DC hub topology based on a multiport front-to-front type DC-DC converter is presented in [29].In figure 2.5 four ports can be seen, each of them having an MMC converter connected on a three-phase common AC bus. Each port may also have an AC transformer if necessary and an AC circuit

breaker for the disconnection of the port when necessary. The system has the capability to connect different types of DC line configurations with different voltage levels. A global voltage-controlled oscillator is used to provide the reference angle for the rotating dq frame. In order to solve the natural instability in the intermediate AC link, a control method of an inner balance loop and an external balance loop are presented. Each port has three modes, AC voltage control, DC voltage control or active power control mode. It is notable that DC fault ride through is achieved by using self-blocking submodules at 50% of the converters and half-bridge submodules for the other 50% leading to 25% higher semiconductor needs. Concluding, this topology offers galvanic isolation and the number of ports can be easily expanded.

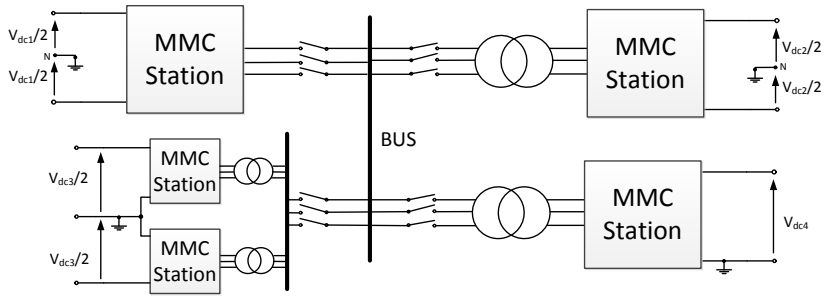


Figure 2.5: Four-port DC hub

2.5. CONCLUSION

Concluding, the main purpose of this literature review was to find DC-DC converter topologies able to upgrade to DC hub. From the discussed topologies the single-stage designs are not so prominent to be used in a DC hub as their upgrade may be complex, costly and not efficient. As a result, the most dominant design is the Front-to-Front topology using modular multilevel converters. MMC is state of the art, offering higher reliability, higher power quality, lower power losses, having a modular structure and starting to be a mature technology. Following, a decision should be made for the intermediate AC link, the two dominant options are the transformer and the LCL filter in order to adapt the voltage level. A transformer is used when there is a need for galvanic isolation and it offers the following basic advantages. First, it offers better switching device utilization of both converters and second, it minimizes the circulating reactive power in the AC link when there is a significant difference between the two DC link voltages. The big disadvantage of a transformer topology is the high volume, weight, and cost of the transformer. Moreover, in high voltages and in increasing frequencies the insulation design of the transformer can be really demanding. The resonant topology increases the current and voltage stresses on the switches, however when MMC converters are used it has shown high efficiencies. As a result, the most dominant option is front-to-front topology with LCL filter in the intermediate link as it combines small footprint, high efficiencies and an inherent fault ride through capability. Finally, the intermediate AC link can operate in higher frequencies where a trade-off between the system footprint and the total losses is presented. As it was discussed the operation mode can be sinusoidal or quasi-two level (trapezoidal), the last one offers the advantage of lower energy requirements for the cell capacitors. This leads to smaller footprint but the modulation index control range gets narrower.

From the mentioned DC hub topologies, different approaches for its design with fault blocking capabilities are observed. In the first approach, capacitors and inductors are used in the intermediate AC link in order to achieve the voltage step between the different DC lines. This approach, while it offers a smaller footprint by decreasing the inductor's and capacitor's dimensions, requires a complex control in order to keep stable the capacitor's voltage to a value higher than the ports' voltages. One major disadvantage is that all the ports should operate at full power in order to have zero reactive power transfer. Moreover, there is a central AC voltage which should always be the higher in the DC hub. This does not allow the connection of a DC line with higher voltage. The second approach uses an intermediate AC transformer. This three-phase three-winding transformer makes it impossible to expand the number of port and requires a demanding dimensioning. The third approach uses a transformer for each port in order to adapt to the central AC bus voltage. In comparison with the previous topology, the footprint is larger but there is the ability to expand the DC hub to a higher number of ports. Naturally, the addition of a new port with an AC transformer will increase even more the footprint making this topology not so prominent for offshore applications.

Overall, the LCL approach can lead to smaller footprint but has important disadvantages. In the case of

intermittent renewable energy sources, where power transfer levels change, the fact that in order to have zero reactive power transfer, the DC hub must operate in full power may lead to reactive power circulation inside the AC link of the DC hub. Moreover, the limitation of the central AC voltage needed to be higher than the port's voltage limits the expandability of the system. Finally, it cannot be used with asymmetric monopole HVDC topologies because it steps DC voltage symmetrically around the central AC voltage point. The above characteristics and the important aspects of the DC hub being easily expanded, connecting different DC line configurations and operating as efficiently as possible in any power level result in the decision of a transformer being used in the intermediate AC link of the DC hub.

3

MODULAR MULTILEVEL CONVERTER

In this chapter a general overview of the modular multilevel converter takes place. Moreover, the averaging principle is introduced in which the control design is based. The design procedure of an MMC is presented and finally, the MMC control is analytically presented. A big part of this chapter is based on the books [30],[31].

3.1. GENERAL OVERVIEW

Modular multilevel converter introduced by Prof. Marquardt in 2002 [32] belongs in the category of voltage source converters (VSC). Specifically, MMC is a cascaded multilevel converter and its fundamental block is a submodule. The submodules are also referred to as cells or chain links in the bibliography.

Following the three-phase modular multilevel converter is discussed. As it can be seen from figure 3.1 each phase leg has two arms. Each arm consists of a series connection of submodules and an arm reactor. The two basic categories of submodules are the half-bridge and full-bridge. In the current thesis, the half-bridge submodules are going to be used resulting in lower semiconductor switches count leading to lower cost, weight, and size.

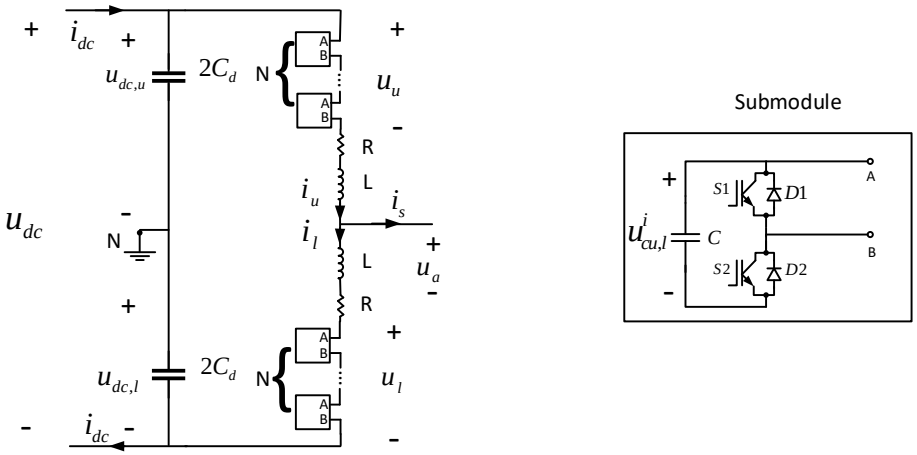


Figure 3.1: Single phase modular multilevel converter

3.1.1. SUBMODULES

The half bridge submodule is equipped with a capacitor and two switches. The switches are controllable power semiconductor devices with an antiparallel diode. A submodule can be seen in figure 3.1. There are three possible states for the submodule depending on the switching state of the semiconductor devices.

1. **Inserted:** When S1 is turned off and S2 is turned on. The submodule capacitor is inserted in the arm circuit. Depending on the direction of the arm current, the capacitor can either charge or discharge.

2. **Bypassed:** When S1 is turned on and S2 is turned off. The capacitor is bypassed. The capacitor voltage is constant disregarding the arm current direction.

3. **Blocked:** S1 and S2 are turned off. This operation mode is applied during the energization of the converter or for short time periods during faults. Depending on the current direction, the capacitor can charge through the antiparallel diode of S2 but cannot discharge.

3.1.2. MMC COMPONENTS

Arms As it can be seen from the figure 3.1, each arm consists of submodules connected in series with an inductor and a resistor. In the following analysis, the sum of the output voltage of the submodules in each arm can be studied as a variable voltage source, namely the inserted voltages $u_{u,l}$. Moreover, the inductor L represents the arm inductance. Finally, the resistor R represents the conduction losses of the arm inductor and the submodules. It is noted that because of the switching nature of the submodules, the resistor R will vary, but this variation depending on the operating conditions will be small.

DC side A lumped model is used to represent the pole-to-neutral capacitances of the positive and negative pole DC cables of an HVDC point-to-point transmission line. It is assumed that the DC bus has capacitive characteristics. A pole-to-pole capacitance C_d is used for the dynamic modeling. Moreover, the assumption of a balanced DC bus is made:

$$u_{dcu} = u_{dcl} = \frac{u_{dc}}{2}$$

AC side On the AC side, the converter is usually connected to an AC grid via a transformer. The transformer used for the voltage stepping also offers galvanic isolation and tap changer. The most common transformer configuration is star grounded on the grid side and delta ungrounded on the converter side offering a high zero sequence impedance. Furthermore, an AC circuit breaker is located on the point of common coupling and a pre-insertion resistor with parallel bypass breaker are used to prevent high inrush currents during the converters connection. Similar to the 2-level converter, the modulation index is determined by the magnitude of the AC side and DC side voltages. In the case of MMC, the AC side voltage is replaced by the inner emf u_s.

$$m_a = \frac{\hat{u}_s}{V_d/2}$$

3.1.3. CURRENTS AND DYNAMICS

The currents of the MMC are defined as follows. The currents flowing through the leg are divided to upper arm current i_u and lower arm current i_l. The sum of the mean values of the arm currents must equal the DC-bus current i_{dc} in order for the DC-bus voltage to be constant.

$$\sum_{k=1}^{M} \bar{i}_{u,l}^{k} = i_{dc}$$

Two other currents that are defined are the circulating i_c and the output current i_s. The following equations apply.

$$i_c = (i_u + i_l)/2 \tag{3.1}$$

$$i_s = (i_u - i_l) \tag{3.2}$$

Which following can be solved for the arm currents:

$$i_u = \frac{i_s}{2} + i_c \tag{3.3}$$

$$i_l = -\frac{i_s}{2} + i_c \tag{3.4}$$

By applying the Kirchoff's voltage law in the figure 3.1 for a single phase, the following relations are observed:

$$\frac{u_{dc}}{2} - u_u - Ri_u - L\frac{du_u}{dt} = u_a \tag{3.5}$$

$$-\frac{u_{dc}}{2} + u_l + Ri_l + L\frac{du_l}{dt} = u_a \tag{3.6}$$

Following, by manipulating the above equations:

$$\frac{L}{2}\frac{di_s}{dt} = \frac{-u_u + u_l}{2} + u_a + \frac{R}{2}i_s \tag{3.7}$$

$$L\frac{di_c}{dt} = -\frac{u_u + u_l}{2} + \frac{u_d}{2} - Ri_s \tag{3.8}$$

An important conclusion made from the above equations is the definition of the output voltage u_s driving the output current i_s and the internal voltage u_c driving the circulating current i_c :

$$u_s = \frac{-u_u + u_l}{2} \tag{3.9}$$

$$u_c = \frac{u_u + u_l}{2} \tag{3.10}$$

3.2. AVERAGING PRINCIPLE

An average dynamic model of the modular multilevel converter is used. This averaged model is the base for the control system design. This model is simple and as the name suggests is based on averaging. Only inserted and bypassed modes are considered for the submodules.

Two basic assumptions are used for the averaging. First, the submodule insertion indices have a discrete nature and can attain two values, 0 when a capacitor is bypassed and 1 when a capacitor is inserted. Following the per-arm insertion indices have $N+1$ discrete values. Assuming that the number of submodules in the arm is large enough, the per-arm insertion indices can be approximated as continuous on [0,1]. Following, by introducing the per arm insertion indices:

$$n_{u,l} = \frac{1}{N}\sum_{i=1}^{N} n_{u,l}^i \tag{3.11}$$

The second assumption concerns the submodule balancing. The insertion voltages can be expressed as:

$$u_{u,l} = \sum_{i=1}^{N} n_{u,l}^i u_{cu,l}^i \tag{3.12}$$

Submodule balancing can be very accurate leading to very small differences between the capacitor voltages that can be neglected. As a result, the individual capacitor voltage can be approximated by the average value of the arm voltage divided by the number of the submodules [33].

$$u_{u,l} = \sum_{i=1}^{N} n_{u,l}^i u_{cu,l}^i \approx \sum_{i=1}^{N} n_{u,l}^i \frac{u_{cu,l}^{\Sigma}}{N} = \frac{u_{cu,l}^{\Sigma}}{N}\sum_{i=1}^{N} n_{u,l}^i \tag{3.13}$$

Equation 3.13 can be simplified by using the per arm insertion indices:

$$u_{u,l} = n_{u,l} u_{cu,l}^{\Sigma} \tag{3.14}$$

This simplified equation is the product of two continuous values. Using the averaging principle it is implied that the switched-mode operation of the MMC is disregarded.

The averaging principle is also used in the capacitor voltages. The equation for each capacitor voltage follows:

$$C\frac{du_{cu,l}^i}{dt} = \sum_{i=1}^{N} n_{u,l}^i i_{u,l} \tag{3.15}$$

By summing over all the capacitor voltages and introducing the per arm insertion indices, equation 3.15 is simplified to:

$$\frac{C}{N}\frac{du^{\Sigma}_{cu,l}}{dt} = n_{u,l}\, i_{u,l} \tag{3.16}$$

It can be seen that the effective arm capacitance is equivalent to C/N.

Finally, the averaged dynamic model for the currents can be found by substituting 3.14 in equations 3.7,3.8.

$$\frac{L}{2}\frac{di_s}{dt} = \frac{-n_u u^{\Sigma}_{cu} + n_l u^{\Sigma}_{cl}}{2} + u_a + \frac{R}{2} i_s \tag{3.17}$$

$$L\frac{di_c}{dt} = -\frac{-n_u u^{\Sigma}_{cu} + n_l u^{\Sigma}_{cl}}{2} + \frac{u_d}{2} - R i_s \tag{3.18}$$

Moreover by introducing the equations 3.3, 3.4 in 3.16, the averaged dynamic model equations for the MMC are complete.

$$\frac{C}{N}\frac{du^{\Sigma}_{cu}}{dt} = n_u\left(\frac{i_s}{2} + i_c\right) \tag{3.19}$$

$$\frac{C}{N}\frac{du^{\Sigma}_{cl}}{dt} = n_l\left(-\frac{i_s}{2} + i_c\right) \tag{3.20}$$

3.3. DESIGN PROCEDURE

In every port of the DC Hub, a modular multilevel converter is used. The design of an MMC is a complex and not straightforward procedure. The design begins with the required power and voltage ratings and continues with the initial values of the converter components. In order to tune the main-circuit parameters, various calculations and simulations are performed. As a result, the whole process presents an iterative character.

Main inputs First of all the main parameters that characterize the converter are the rated power and voltage of the port. In an HVDC project, a certain amount of power is transmitted. As a result, the converter is dimensioned according to the transferred power of the DC link. Following, the DC link voltage is chosen. High-voltage extruded cross-bound polyethylene (XLPE) cables are mostly used for power transmission involving MMCs. Based on the different manufacturers, the DC cables are available on standardized voltage levels.The chosen values for the DC side voltage level of the MMC are based on these available voltage levels.

Semiconductor Devices The next component to be decided is the power semiconductor switch that is going to be used in the submodule. In comparison to the 2-level VSC operating in high frequencies with PWM, MMC operates in lower frequencies. As a result, devices operating in lower frequencies with low voltage drops and high voltage ratings are preferably used. Half-bridge submodules are chosen, the submodule technology also affects the current ratings. The current ratings of the semiconductor devices are determined not only by the normal operation but also from the fault operation. In normal operation the arm current flows through the submodules and the peak value of the current that should be handled equals:

$$I_{arm,r} = \frac{I_{dc,r}}{3} + \frac{\hat{I}_{s,r}}{2}$$

where $I_{dc,r}$ is the rated current on the DC-side(absolute value), $\hat{I}_{s,r}$ is the peak value of the AC-side current at the rated operation.

The fault currents during DC side short-circuits need to be studied in order to make a decision for the semiconductor switches current ratings. In case of a DC-side fault, which is studied in the next chapters, the controlled power semiconductor switches are blocked and the current flows through the antiparallel diodes. Following, the circuit breakers on the AC side will interrupt the fault current. In this case, the antiparallel diodes should be dimensioned in order to handle the fault current. There are other cases where special measures are taken. Like the use of large thyristors in parallel with the submodule conducting only in the fault situation instead of the antiparallel diode or when a DC side circuit breaker is used.

Number of submodules At this point still, important data which will enable the designer to make some choices is missing. The important parameter of the submodule capacitance is still unknown being an obstacle to the decision of the submodules total number. A rule of thumb [34] is used for the total energy storage of the converter which has to be between $30-40kJ/MVA$.

Following, the average sum capacitor voltage per arm $u^{\Sigma}_{cu,l}$ and the average submodule capacitor voltage V_c need to be calculated. The average sum capacitor voltage per arm $u^{\Sigma}_{cu,l}$ can be taken equal to the rated DC side pole-to-pole voltage V_{dc}

$$u^{\Sigma}_{cu,l} = V_{dc}$$

In case of modulation index higher than one, when using full-bridge submodules, the $u^{\Sigma}_{cu,l}$ can get a higher value.

Moreover, the average capacitor voltage V_c choice should be made by considering 5 main quantities:

- the average submodule capacitor voltage with respect to reliability due to cosmic ray
- the submodule capacitor voltage ripple in the operation where this ripple is maximum
- the overvoltage due to the stray inductance of the submodule when switching the maximum arm current
- the maximum submodule capacitor voltage during ac-side faults
- the maximum submodule capacitor voltage during dc-side faults

The first factor is chosen based on experience. For the second, an assumption for a 10% ripple can be made or the rule of thumb for the total converter energy storage requirement can be used. In the third, the value of the stray inductance of the commutation path of the submodule should be known, which can be found through numerical methods. The last two should be confirmed through simulations. Concluding an initial value for the number of submodules can be given by:

$$N = \frac{u^{\Sigma}_{cu,l}}{V_c}$$

At this point, it is noted that more submodules can be used in order to have redundancy in the system and this value can be chosen based on estimations on the system reliability.

Submodule capacitance The submodule capacitor is probably the most important part of the converter. The capacitors comprise a big part of the total system's size, weight, and cost. The capacitor size is connected to the capacitor voltage ripple. While a large capacitor value will lead to a small voltage ripple, it will also lead to bigger total size and higher cost for the converter. Moreover, there is a trade-off between the cost of the capacitor and the cost of the semiconductor devices in a submodule. Again real-time or time-domain simulation can be performed in order to optimize this value. As mentioned earlier, in order to get a first value for the submodule capacitance, the rule of thumb where the total stored energy in the system is between $30-40kJ/MVA$ is used.

Arm inductance There are three main aspects in order to choose the arm inductance [35].

1. Part of the link inductor
2. Prevention of circulating current resonance
3. Suppressing the fault current

Part of the link inductor The arm inductance L_{arm} in the MMC is part of the link inductor, in the way of connecting the MMC with the rest of the system. When looking from the AC side the two arm inductors are seen in parallel, as a result, the half of the inductance is counted $L_{arm}/2$. Other parts of the link inductor can be the inductance of the link transformer L_{Tr} or the inductance of phase filters L_f.

A bigger link inductance X_{link}, corresponds to slower changes for the output current when following a reference value. Moreover, the bigger the X_{link}, the higher the reactive power consumption. One advantage of a big X_{link} is that it can suppress the negative-sequence current better.

Circulating current resonance The value of the arm inductance should be chosen appropriately for the series resonance angle frequency to be far away from the circulating current resonance angle frequency.

Suppress the fault current The value of the arm inductance depends on the way the short-circuit faults are handled. In the current thesis, the DC fault is studied so the arm inductance is chosen for the worst case of DC pole-to-pole short-circuit.

First of all, before the submodules are blocked, the arm inductor should protect the power transistors from a high inrush current rise. The following equation should be satisfied:

$$L_{arm} = \frac{V_{DC}}{2\alpha} \tag{3.21}$$

where $\alpha[kA/s]$ is the maximum current rise rate.

After blocking the submodules, the antiparallel diodes will conduct. There is the case where special equipment is used to conduct the current during the fault instead of the antiparallel diodes. In the other case, the antiparallel diodes of the submodule conduct during the fault. In this case, the arm inductor will be dimensioned in order to protect them from high currents.

3.4. MMC CONTROL

The control of modular multilevel converter is cascaded and is more complex compared to the 2-level voltage source converter. An overview of a typical control system can be seen in figure 3.2.First, the higher-level control, where the inputs of this stage can be the AC voltage, DC voltage, active and reactive power. While the output is the output-current reference entering the next control stage of output-current control. Also, in this stage, the measured output current is the other input, while the output of this stage is the output-voltage reference. So far the control system is similar to the 2-level converter. Because of the higher complexity of MMC, a new stage is added, the arm-balancing control. This stage comprises the circulating current control and the sum capacitor voltage control. The output is the insertion indices entering the next stage of modulation and submodule balancing. In this stage, the measured capacitor voltages are the inputs Finally, based on the insertion indices and the submodule capacitor voltages the gate signals for all the submodules are generated.

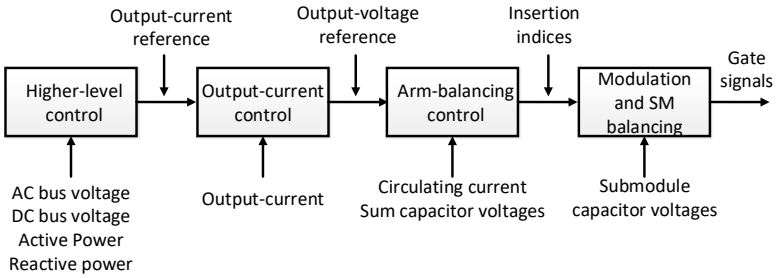


Figure 3.2: MMC control overview

As far as it concerns the choice of the two-dimensional frame, there are two main classes for representing a space-vector: the alpha-beta frame and the dq-frame. The stationary dq-frame is chosen in this thesis. In the dq-frame, the signals can be seen as DC values under stable operation. This results in DC command tracking problem instead of a sinusoidal tracking problem. Following, simpler proportional integral controllers can be used instead of proportional resonant controllers.

3.4.1. PHASE-LOCKED LOOP

The converter control is synchronized with the line voltage through the phase-locked loop (PLL). The PLL calculates the grid's phase synchronous angle required for the dq transformation. The role of the PLL is to align the grid voltage with one axis in the dq-frame. This is succeeded via a closed-loop control with three main components, a compensator, a saturation block and a voltage-controlled oscillator (VCO) as can be seen in figure 3.3.

The input of the PLL is the three-phase grid voltage $V_{G,abc}$ which is then transformed to the dq-frame $V_{G,dq}$. In this thesis, the d coordinate is chosen to be regulated to zero in the steady state. The compensator is designed to establish a zero steady-state error. The poles and zeros of the compensator's transfer function are regulated on the basis of the needed phase and gain margins and the PLL's closed-loop bandwidth.

The output of the compensator is the rotational speed ω of the dq-frame. It is needed to be defined in a narrow range in order to avoid large variations via a saturation block. Lastly, the acquired rotational speed of the dq-frame ω is integrated via a voltage-controlled oscillator. The output of this integration is the grid's phase synchronous angle θ. Whenever θ reaches 2π is reset to zero. The control loop closes using this value for the new dq-transformation of the grid voltage.

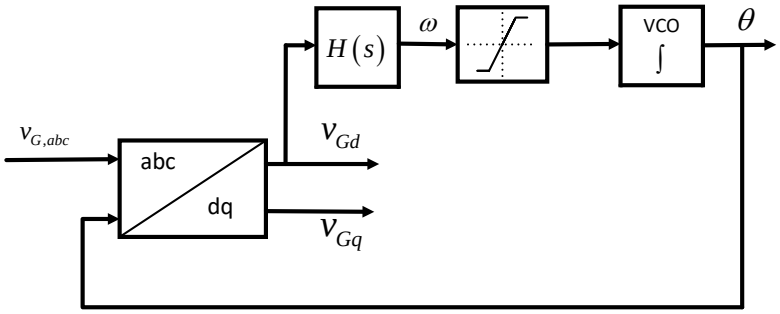


Figure 3.3: Phase-locked loop

3.4.2. HIGHER-LEVEL CONTROL

On this stage, the reference of the output-current is generated. The inputs depend on the control mode of the converter which can be active or reactive power control mode, AC voltage control mode and DC voltage control mode.

It is known that the active and reactive power control can be decoupled in d and q components. As a result, the controllers are divided into two main categories. First, the active power channel including active power controller and DC voltage controller. Second, the reactive power channel consisting of the reactive power controller and the AC voltage controller.

Depending on the systems specifications and network configurations only one controller from each channel can be used. Proportional-integral controllers are employed in order to achieve a zero steady-state error.

The values of the active and reactive power in a three-phase abc-frame are the following[30]:

$$p_{ac} = \frac{3}{2}(u_a i_a + u_b i_b + u_c i_c) \tag{3.22}$$

$$q_{ac} = \frac{1}{\sqrt{3}}(u_a b i_a + u_b c i_b + u_c a i_c) \tag{3.23}$$

These equations can be transformed into dq-frame using the Park transformation and preserving the magnitude of the phase quantities the following equations are derived:

$$p_{ac} = \frac{3}{2}(v_d i_d + v_q i_q) \tag{3.24}$$

$$q_{ac} = \frac{3}{2}(v_q i_d + v_d i_q) \tag{3.25}$$

As mentioned earlier, by implementing the PLL control, the q-axis of the dq-frame is alligned to the AC network voltage, resulting in $u_d = 0$ and :

$$p_{ac} = \frac{3}{2} v_q i_q \tag{3.26}$$

$$q_{ac} = \frac{3}{2} v_q i_d \tag{3.27}$$

From the above equation, it is clear that active power is controlled through i_q and reactive power is controlled through i_d. As a result, independent control of active and reactive power is achieved.

The input of the PI regulators is the error between the power reference and the measured power. The power error is transformed into a current reference and it is saturated before forwarded to the output-current control stage. A current limiter is used to maintain the current references within the converter's current limits. The analytical equations of the implemented controllers are seen next and the block diagrams are presented in figures 3.4 and 3.5.

$$i^*_{Cq} = (p^*_{ac} - p_{ac}) \cdot \left(K_{p,p} + \frac{K_{i,p}}{s} \right) \tag{3.28}$$

$$i^*_{Cd} = (q^*_{ac} - q_{ac}) \cdot \left(K_{p,q} + \frac{K_{i,q}}{s} \right) \tag{3.29}$$

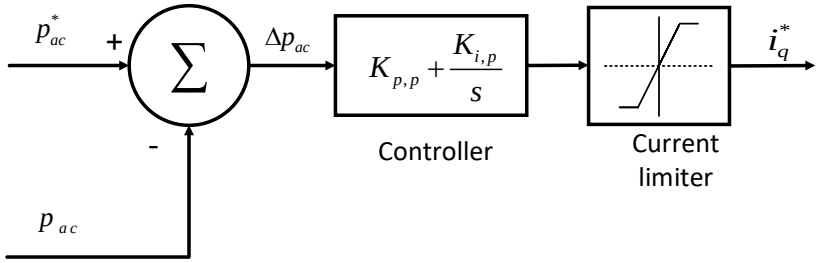


Figure 3.4: Active power controller

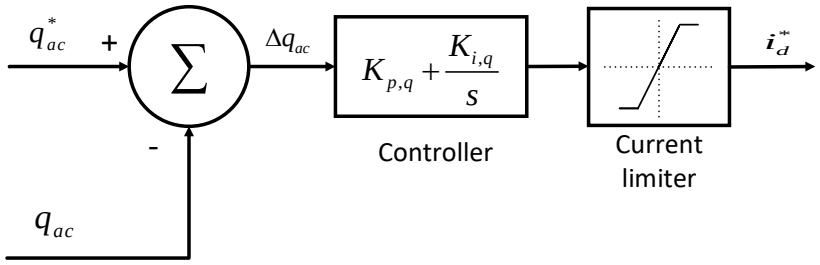


Figure 3.5: Reactive power controller

DC voltage controller The DC voltage controller is very important in a VSC HVDC transmission system. By controlling the q-component of current and adjusting the amount of active power flowing in or out of the network, the DC voltage is controlled at a certain level. A possible approach is for the controller to work on the error of DC voltage. However, in this case, the closed loop dynamics depend on the operating point since I_{DC} is inversely proportional to V_{DC}. The control approach followed is to work on the energy error avoiding nonlinearity problems. The energy W_c stored in the DC capacitor is proportional to V^2_{DC} and given by:

$$W_c = \frac{1}{2} C V^2_{DC} \tag{3.30}$$

The analytical equation of the implemented controller is seen next and the block diagrams are presented in figures 3.6.

$$i_{Cq}^{*} = (W_c^{*} - W_c) \cdot \left(K_{p,DC} + \frac{K_{i,DC}}{s} \right) \tag{3.31}$$

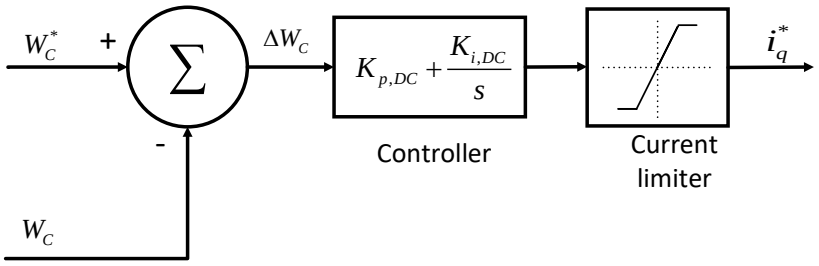


Figure 3.6: DC voltage controller

AC voltage controller There are two different approaches to control a VSC system. The first one is the current-mode which is used in the previous controllers. In this approach, there is a dedicated control loop which regulates the VSC line current. There are also saturation blocks limiting the current references. In this way, the converter is protected from overloads. This approach is the most commonly used as it offers superior dynamic performance, higher control precision, and robustness[30].

The second approach is the voltage-mode control which is simpler with a lower number of control loops. However, due to the absence of the VSC line current loop, the converter is not protected against overcurrents.This approach is implemented on the AC voltage controller and can be following seen in figure 3.7. In this case both d,q components are used in order to control the AC voltage. The $V_{AC,d}^{*}$ is given equal to zero while $V_{AC,d}^{*}$ is given according to the modulation index we want to achieve.

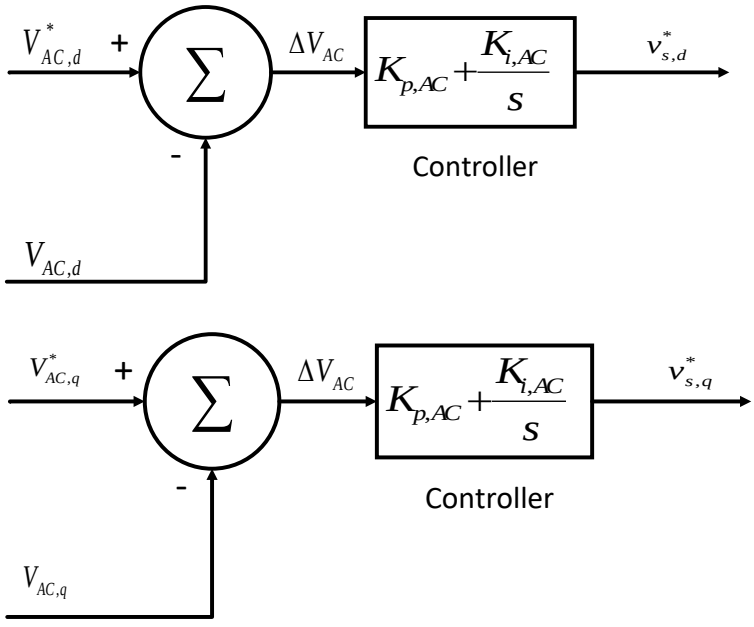


Figure 3.7: AC voltage controller

F2F connection of three MMCs In the front-to-front topology, three MMC connect their AC sides in an intermediate AC link. Current-mode control approach is commonly used for MMC. In this approach, the line current of the converter is controlled to a specific reference. By changing the command references of active or reactive power channels the reference of the output current changes and the output current adapt

to this new value on steady state. The connection of three MMC in front-to-front configuration can be seen as three current sources connected to a node. Consequently, Kirchhoff's current law should be followed. In a system where one converter is operating in power control mode while the other in AC voltage control mode and the third one in DC voltage control mode that is not the case. There exists a natural instability in the intermediate AC link in the way that the algebraic sum of the AC line currents in the central AC node is not zero. As the Kirchhoff's law is always followed, the control approach need to be adapted.

A way to solve this problem is to change the control approach in one port from current-mode to voltage-mode. With this approach the current of one line is uncontrolled, giving the freedom to stabilize the system. The Kirchhoff's current law can be applied, as a result, the current of this line is going to be the sum of the other two. The same conclusion can be reached for an N-port DC hub, where N-1 ports operate in current-control mode while the one in voltage-control mode.

Effective DC bus capacitance In the modular multilevel converter, the distributed arm capacitances are operating as a voltage source and are responsible to maintain the DC-link voltage at a specific level. The DC capacitors correspond to the main inertia source of the system and their size influences the power flow control and the controller's bandwidth. For that reason, their size is carefully calculated based on both steady-state operation and desired transient behavior. In [31] the DC bus dynamics are studied and the submodule capacitors were included. The contribution from the submodule capacitors results in a larger effective DC-bus capacitance C_{eff} according to :

$$C_{eff} = C_d + \frac{2MC}{N} \tag{3.32}$$

where M is the number of phases, N the number of the submodules, C_d the DC cable capacitance, C the submodule capacitance.

3.4.3. OUTPUT-CURRENT CONTROL

In a VSC independent control of active and reactive power power is achieved by regulating the voltage drop across an inductance and by controlling the current flowing though it. The following equation applies:

$$v_f - u_c = R_T i_c + L_T \frac{d}{dt}(i_c) \tag{3.33}$$

Which in the dq-frame results in the following state-space equations:

$$v_{fd} - u_{cd} = R_T i_{cd} + L_T \frac{d}{dt}(i_c d) - \omega L_T (i_{cq}) \tag{3.34}$$

$$v_{fq} - u_{cq} = R_T i_{cq} + L_T \frac{d}{dt}(i_c q) - \omega L_T (i_{cd}) \tag{3.35}$$

where;
i_c is the converter current in the rotating frame [A];
v_f is the AC network voltage in the rotating frame [V];
u_c is the converter voltage in the rotating frame [V];
R_T is the total resistance between the VSC and the AC grid [W];
L_T is the total inductance between the VSC and the AC grid [H] and

Using Laplace transformation in the above equations, the equivalent block model can be derived as seen in figure 3.8.

The current reference provided from the higher control level is compared to the measured current through the inductance. In order to have a zero steady-state error, a compensator is used. The proportional integral (PI) controller transforms the current error into a voltage error. This voltage error is next subtracted from the converter voltage resulting in a reference voltage value. The block diagram of the output-current controller (OCC) is presented in figure 3.9.

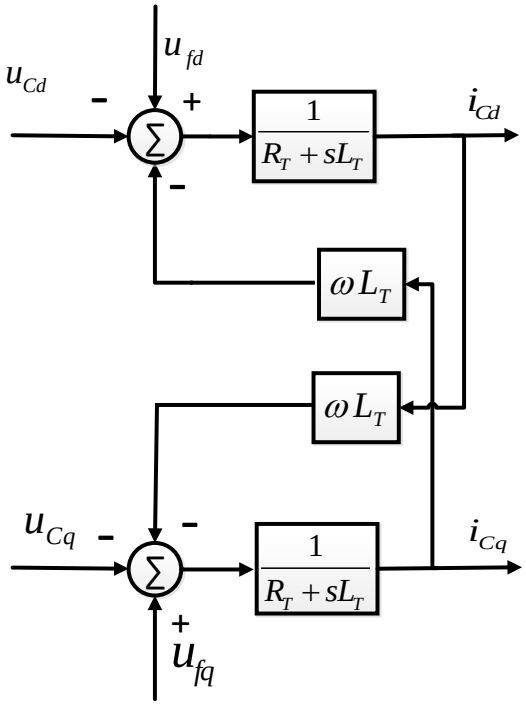


Figure 3.8: Phase reactor block

3.4.4. CURRENT LIMITER

In order to maintain the current at the converter within limits, a current limiter is needed. The output current controller provides the reference current value. This value is following compared to a maximum allowable value. If the current is higher than the limit then has to be limited. The magnitude of the current vector is given:

$$|i^*| = \sqrt{i_d^{*2} + i_q^{*2}} \tag{3.36}$$

Depending on the converter, there are three limitation modes that can be applied. These three possible modes are shown in figure 3.10 and are the following:

1. **d-axis priority:** reactive power is prioritized to help voltage restoration. In this case, d-axis current remains stable and q-axis is reduced. This strategy is mostly applicable in case of weak grid connections.
2. **q-axis priority:** active power is considered more important and therefore only d-axis current is limited, while q-axis current is preserved.
3. **proportional limitation:**both d-, q-currents are decreased proportionally.

3.4.5. ARM-BALANCING CONTROL

The internal dynamic equations of an MMC were derived in section 3.2 and are presented again in the following equations:

$$L\frac{d}{di_c} = \frac{u_d}{2} - u_c - Ri_c \tag{3.37}$$

$$\frac{C}{N}\frac{du_{cu}^{\Sigma}}{dt} = n_u\left(\frac{i_s}{2} + i_c\right) \tag{3.38}$$

$$\frac{C}{N}\frac{du_{cl}^{\Sigma}}{dt} = n_l\left(\frac{-i_s}{2} + i_c\right) \tag{3.39}$$

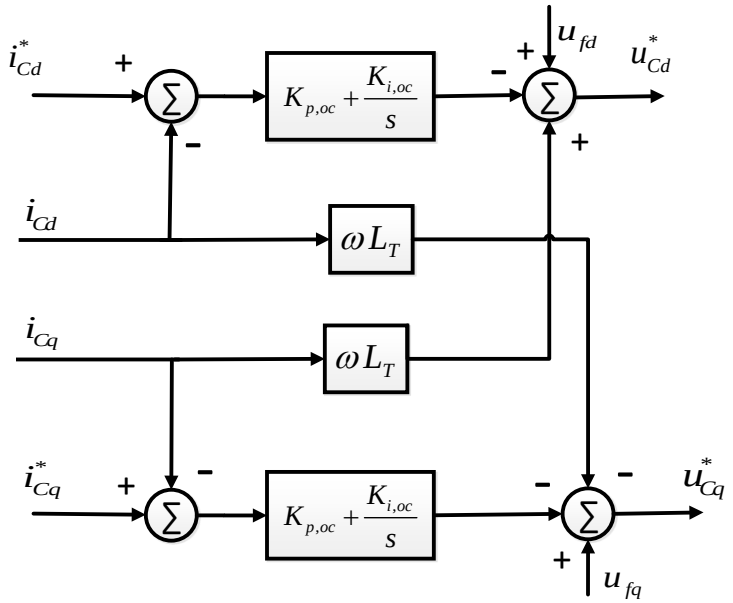


Figure 3.9: Output-current controller

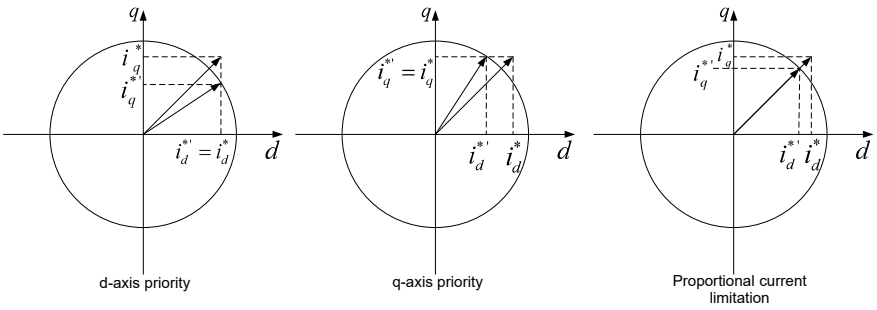


Figure 3.10: Current limiter modes of operation

From the equations, it can be seen that the output current is not available in the arm-balancing control. As a result, by controlling the circulating current, energy is transferred in and out of the arms by charging and discharging the SM capacitors.

The arm-balancing or internal control is divided into two tasks. First, the control of the circulating current in order to converge to a DC component given by:

$$i_c^* = \frac{I_d}{3} \tag{3.40}$$

Second, the mean values of the sum capacitor voltages in each arm should converge to the DC pole-to-pole voltage.

$$u_{cu,l}^{\Sigma} = V_{dc} \tag{3.41}$$

Circulating current control So far, the dq-frame has been used for the design of the controllers for the higher and output-current levels, however, for the circulating-current controller, the abc-frame is going to be used. The reasons for this decision are the following [36]:

1. In case of additional harmonics, additional park's transformations are needed, increasing the complexity of the controller.

2. dq-frame does not provide direct and explicit control of the circulating current independently by phase.

In comparison with the previous control levels, where dq-frame and proportional integral controllers are used, for the circulating current controller proportional resonant controllers (PR) are implemented.

The differences in the arm voltages in the MMC legs lead to the creation of a circulating current flowing within the MMC. This circulating current does not affect the output current and voltage. However, it increases the RMS value of the arm current, resulting in bigger power electronic components and higher losses. For that reason, there is a need to mitigate the circulating current within the converter.

According to [33], it is observed that the stored energy in each phase of an MMC has a double frequency component. The energy is stored in the submodule capacitors resulting in double frequency component for the submodule voltages. The inserted submodule output voltages $u_{u,l}$ drive the circulating current i_c. This results in a double frequency component in the circulating current. Moreover, there is a DC current equals $i_{dc}/3$. Also, during the transients, there is a quadruple harmonic component in the circulating current [37]. In order to mitigate both double and quadruple harmonic component, two proportional resonant (PR) controllers are connected in parallel. Each of them achieves high bandwidth in the corresponding resonant frequency.

The circulating current dynamics are given by the equation 3.42.

$$L\frac{d}{di_c} = \frac{u_d}{2} - u_c - Ri_c \Rightarrow i_c = \frac{1}{sL+R}\left(\frac{u_d}{2} - u_c\right) \tag{3.42}$$

Taking the above equation and adding the feedforward term $\frac{u_d}{2} - Ri_c^*$ to compensate for the half DC pole-to-pole voltage term and the resistive voltage drop, the control law for obtaining the reference for the voltage driving the circulating current:

$$u_c^* = \frac{u_d}{2} - Ri_c^* - R_a\left(1 + \frac{2\alpha_2 s}{s^2 + (2\omega_1)^2}\right)(i_c^* - i_c) \tag{3.43}$$

The biggest contribution in the above equation comes from the $\frac{u_d}{2}$. As a result, the contribution of the PR controller is small.

The proportional gain of the PR controller equals to R_a. The circulating current controller does not need to be as aggressive as the output current controller, for this reason, it is chosen[31]:

$$R \ll R_a \leq K_p$$

K_p is the gain of the output-current controller.

The bandwidth α_2 is chosen to be smaller than the angular frequency ω_1.

The circulating current reference i_c^* is taken by passing the circulating current i_c through a Butterworth filter.

A per phase equivalent of the circulating current control can be seen in figure 3.11.

Closed-loop voltage control In this control stage, the basic inputs are the reference for the voltage driving the circulating current v_c^*, the output voltage reference u_s^* and the sum capacitor voltages for the upper and the lower arm $u_{cu}^{\Sigma}, u_{cl}^{\Sigma}$. The main role of this stage is to calculate the insertion indices and forward these signals to the modulation and submodule balancing stage.

$$n_u = \frac{u_c^* - u_s^*}{u_{cu}^{\Sigma}} \tag{3.44}$$

$$n_l = \frac{u_c^* + u_s^*}{u_{cl}^{\Sigma}} \tag{3.45}$$

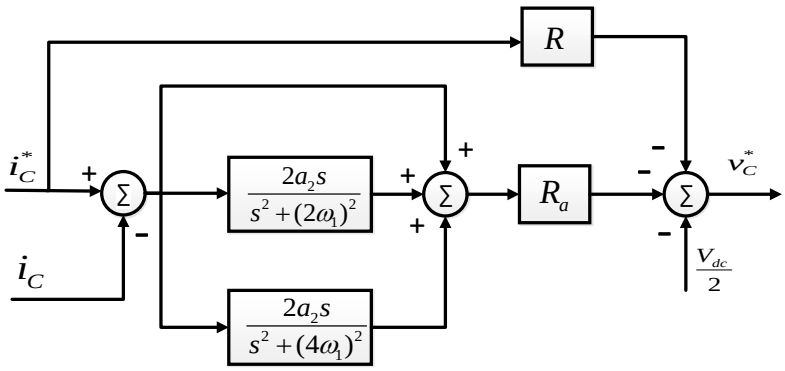


Figure 3.11: Circulating-current controller

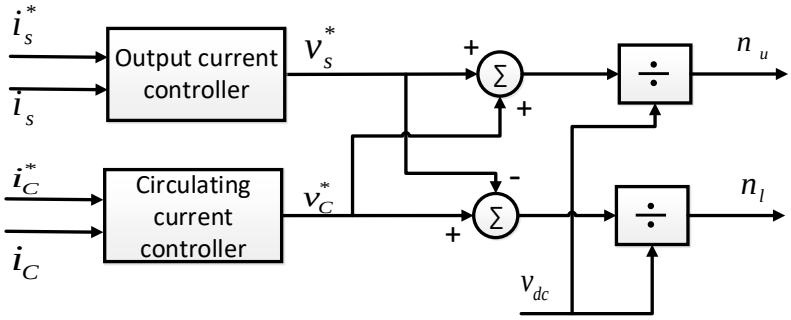


Figure 3.12: Closed-loop voltage control

Bandwidth In order for the closed-loop system to remain stable, there is an upper limit for the closed-loop bandwidth α_c. According to a rule of thumb [38] it should be at least 10 times lower than the angular sampling frequency ω_s.

$$\alpha_c \leq \frac{\omega_s}{10} \tag{3.46}$$

In the current thesis the switching frequency is selected at $600Hz$. The maximum closed-loop bandwidth is $\alpha_c = 377krad/s$. The output-current controller is the "heart" of the system, as a result it should be faster than the outer controllers. Based on the analysis of the DC voltage controller closed-loop transfer function in [39] :

$$K_{p,DC} \leq \frac{1}{8}\alpha_c C \Rightarrow \alpha_{dc} \leq 0.125\alpha_c \tag{3.47}$$

As it is advisable to keep an extra safe margin [40]. The simplifications included neglect the PLL influence, the crosscoupling of d,q axes, the converter switching behaviour etc. Following, in order to guarantee a sufficient gain to damp voltage oscillations :

$$\frac{K_{i,DC}}{K_{p,DC}} \ll \frac{\alpha_c}{4}, if \frac{K_{i,DC}}{K_{p,DC}} \leq \frac{\alpha_c}{8} = \alpha_{dc} \Rightarrow K_{i,DC} \leq \alpha_{dc}^2 C \tag{3.48}$$

The bandwidth of the active and reactive power controller should not be larger than the DC voltage controller. The dynamics of the reactive power channel depend on the impedance of the AC grid and as a result, it can be tuned only by trial and error.

The gains of the controllers are calculated in the SI based on the equations shown in table 3.1. The quantities V_{bc}, I_{bc}, S_{bc} are the base AC voltage, AC current, and power values of the converter respectively, while V_{dcr} is the voltage base of the DC grid.

Table 3.1: Controller gains

Controllers	K_p	K_i
OCC	$a_{c_{pu}} L_p \omega$	$a_{c_{pu}} R_p \omega$
Active power	$a_{dc_{pu}} C_{dc_{pu}} I_{bc} / S_{bc}$	$a^2_{dc_{pu}} C_{dc_{pu}} \omega I_{bc} / S_{bc}$
Reactive power	$a_{dc_{pu}} C_{dc_{pu}} I_{bc} / S_{bc}$	$a^2_{dc_{pu}} C_{dc_{pu}} \omega I_{bc} / S_{bc}$
DC votlage	$a_{dc_{pu}} C_{dc_{pu}} 2 I_{bc} / (C V^2_{dcr})$	$a^2_{dc_{pu}} C_{dc_{pu}} 2\omega I_{bc} / (C V^2_{dcr})$
AC votlage	$a_{dc_{pu}} C_{dc_{pu}}$	$a^2_{dc_{pu}} C_{dc_{pu}} \omega$

3.4.6. ARM-LEVEL AVERAGE MODEL

For the model simulations, MATLAB/Simulink is used. Simulink is a time-domain circuit simulator. Its advantages are that the control circuit and the power circuit can be defined separately, which is conceptually closer to the real converter system.

The modeling of the MMC is inseparably connected to the control. There are many modeling approaches for the MMC with different degrees of detail. There are very detailed models like the switch-level average (SLA) presented in [41]. In such a model, the level of detail goes down to the semiconductor switches of the submodule in an MMC. This level of detail allows studies concerning semiconductor device losses, switching transients, harmonic analysis and internal fault and protection design. Unfortunately, such detailed models having many switching elements lead to excessive computational efforts and long simulation times.

The focus of this thesis is on the power system level. The transient stability and faults response on the DC-side link are studied. For this reason, a less-detailed model is used, resulting in shorter simulation times. The arm-level-average model is based on the leg-level average model first introduced in [42]. Following, the arm-level average model and its integration into the control part are presented.

The block of the arm-level average model is shown in figure 3.13. As it can be seen, the ALA block is part of the power circuit of the MMC model. The ALA model presented in [31] is based on the the internal dynamic equations provided by equations 3.18, 3.19 and 3.20. This model represents the dynamics of the sum capacitors' voltage in each arm and it is seen as a controlled voltage source. The block contains both power and control circuits.

The control signals are:

1. The insertion indices $n_{u,l}$ from the voltage control balancing represent the one signal input.
2. The arm current $i_{u,l}$ is the second input
3. The sum capacitor voltages $u^{\Sigma}_{u,l}$ of each arm is the main output of this block

The insertion indices $n_{u,l}$ represent continuous values in the range $[0,1]$. The multiplication of the $n_{u,l}$ with the $u^{\Sigma}_{u,l}$ results in the inserted voltages $v_{u,l}$ of each arm. This controlled voltage source is incorporated to the main circuit of the MMC along with the arm inductance L_{arm} and arm resistance R_{arm}.

Furthermore, a second power circuit is present inside the ALA block. The multiplication of the $n_{u,l}$ with the $i_{u,l}$ results on the equivalent current through the capacitors $i_{cu,l}$. This is represented by a controlled current source which is connected in series with the equivalent arm capacitance C/N. Also there is a voltage measurement for the $u^{\Sigma}_{u,l}$.

This model offers low computational times but ignores the PWM dynamics aspects, the discrete nature of the insertion indices and the capacitor voltage unbalance within the arm. Moreover, the situations where in case of a fault, the submodules should be blocked cannot be represented by the ALA model. In the current thesis, fault contingencies are studied, for that reason, the ALA model should be enhanced to the arm-level average model with blocking capability.

ALA-BLK

The understanding of ALA-BLK model is easy after the simple ALA model is studied. In this model, the blocking state of the submodule is represented, where both switches of the half-bridge circuit are turned-off based on a solution presented on [43].As it can be seen from the figure 3.14 the following circuit elements are added:

1. A normally closed switch S_{blk}. The switch opens in case of fault with a signal produced by the protection circuit.

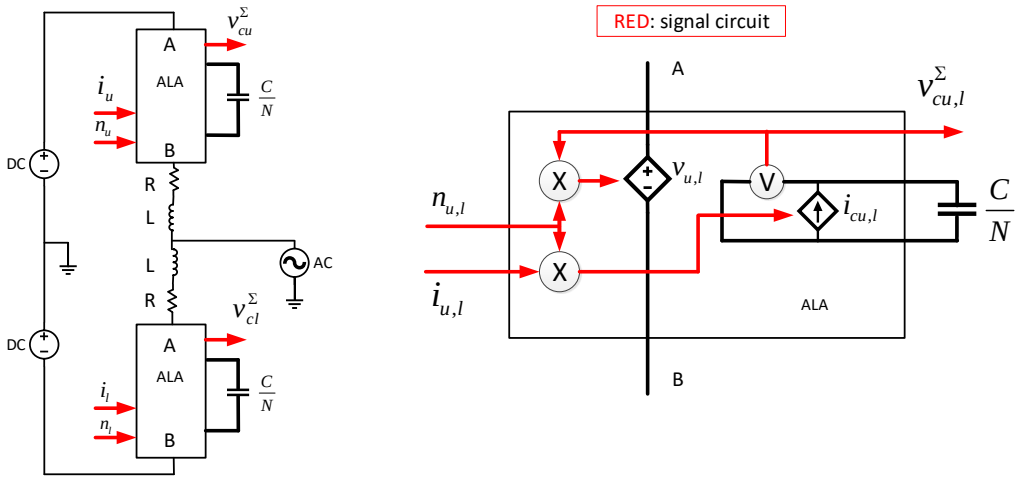


Figure 3.13: Arm-level average model

2. A bypass diode D_{bp1} representing the upper switch antiparrallel diode of the submdodule as presented in figure 3.1.
3. A bypass diode D_{bp2} representing the lower switch antiparrallel diode.

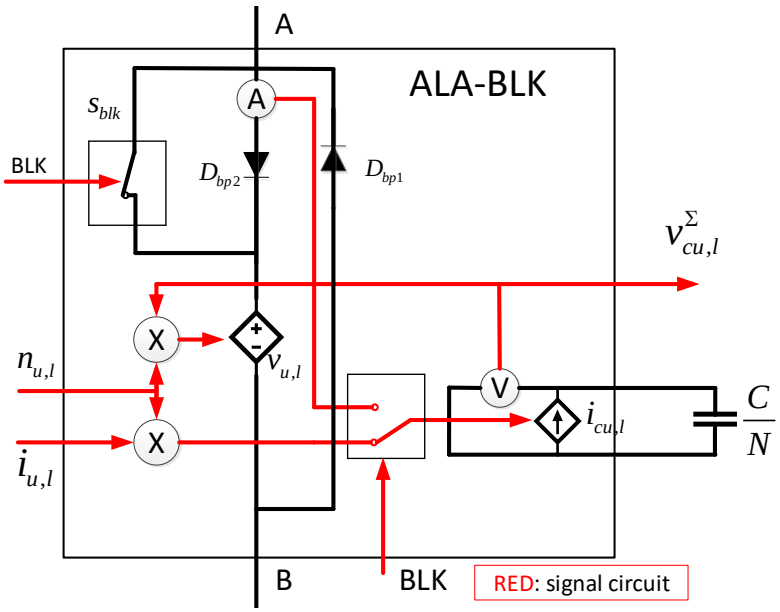


Figure 3.14: Arm-level average blocking model

In normal operation S_{blk} switch is closed. The bypass diode D_{bp1} is reverse biased. In case of a fault where the current reaches a specified threshold, a signal is sent from the protection circuit to open S_{blk}. In this way, the semiconductor controlled switches are protected from overcurrent. In case of a positive arm current, the D_{bp2} conducts and the capacitors are charged. In case of a negative arm current, the D_{bp1} conducts and the capacitors are bypassed.

3.5. SUMMARY

For the creation of a DC hub, the MMC is the most basic and important component. For that reason, a general overview of the MMC topology and operation is presented. The averaging principle introducing the arm insertion indices and assuming a very accurate submodule balancing is next presented. Moreover, based

on the averaging principle, the control levels of the MMC are presented. The higher-level, output current controller, and arm-balancing controller are presented. The control structure of port 1 and 2 are presented in figure 3.15, and the control structure of port 3 is presented in figure 3.16 Finally, the arm-level-average model and the enhanced arm-level-average blocked model for the fault contingencies are presented.

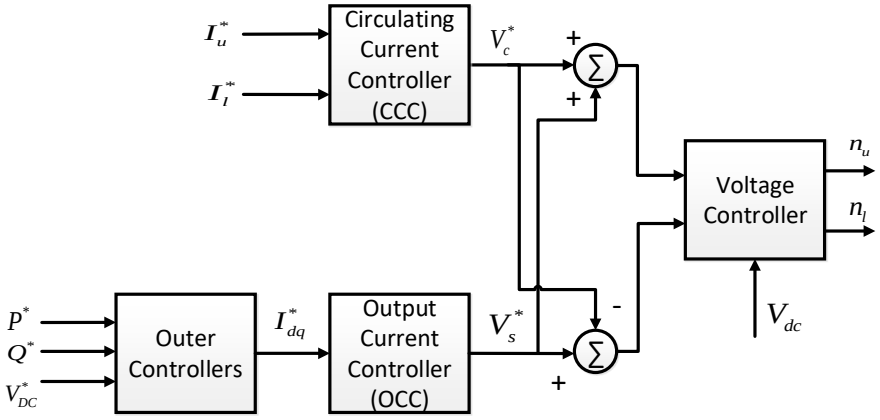


Figure 3.15: Port 1 and 2 control structure

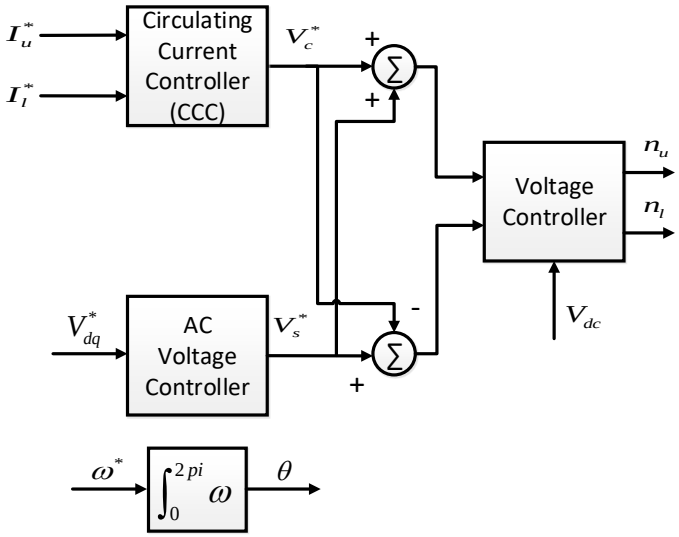


Figure 3.16: Port 3 control structure

4

DC HUB

In this chapter, the decisions made over the different components of the DC hub are discussed. Specifically, the choices for the intermediate link, whether a transformer is going to be used or not, the frequency and waveform of the intermediate AC link are made. Moreover, a first design procedure of the converter and the intermediate link is presented. A discussion for the control role distribution takes place and finally, the model is validated throughout simulations.

4.1. Components Decision

A DC hub consists of two basic parts. The ports, where AC/DC converters convert the direct current to alternative and vice versa and the intermediate AC link, where different components are located. An overview of the system can be seen in figure 4.1. Point-to-point transmission lines are also present, connecting the terminals to the DC hub ports. When referring to a point-to-point connection the following abbreviations will be used: $pxpy$, where x is the number of the port and y the number of the outer terminal.

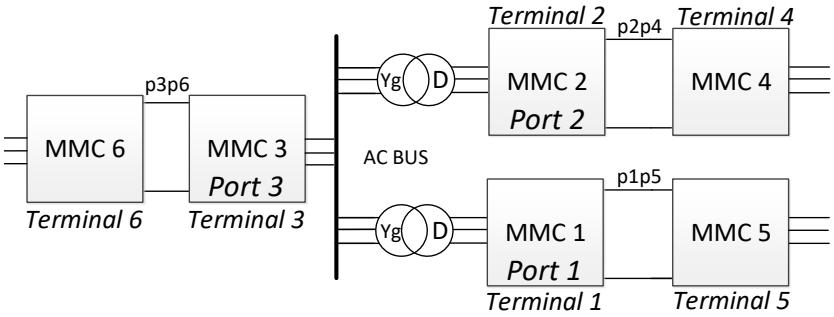


Figure 4.1: DC hub

4.1.1. Converter

After its introduction by Prof. Marquardt in 2002 MMC became very popular in a very brief time period. This is achieved thanks to the benefits that this converter offers. The main advantages of MMC are briefly presented.

1. modularity, scalability
2. high-quality output voltage
3. lower filter need due to the low harmonic distortion
4. redundancy

This popularity of MMC has led to excessive research from both academia and industry resulting in important developments. Nowadays, there are many HVDC projects based on MMC topology. MMC is now a mature technology with clear advantages over the 2-level VSC technology. Moreover, in the bibliography [22],new topologies are presented combining the favorable characteristics of both MMC and 2-level VSC technologies. These state of the art technologies can combine higher efficiencies and smaller volume, however,

these technologies are not as mature as MMC and further research is required. For the reasons above, the MMC is chosen as the desirable converter for being used in the ports of the DC Hub. A first design of the converter components is later shown.

4.1.2. INTERMEDIATE AC LINK

The intermediate AC link of the DC Hub can be independent of the AC grid. There is the possibility of connecting the intermediate AC part with an AC grid or the AC link of a wind farm, but this option is not going to be studied in the current thesis. Being independent of an AC grid offers some advantages. First of all, the decisions of a frequency higher than 50Hz or a waveform different than sinusoidal (i.e. square or trapezoidal) can be made. Moreover, the established AC grid codes can be disregarded as there is no connection to an AC grid. Furthermore, in order to adapt to the different voltage levels, a transformer can be used. Finally, there is the possibility of adding phase reactors in order to suppress the fault current.

OPERATING FREQUENCY

The AC grid frequency is 50 Hz, while in the intermediate AC link of the DC hub this frequency can be higher. The operating frequency is connected to the size of the passive components as well as to the losses. With a higher frequency, the size of the inductors and the capacitors in the converter arms can be decreased. Also, the AC transformer or LCL filters being used in the intermediate AC link can have a smaller size. All these result in a total design with lower volume, weight, and lower initial investment. However, this increase in frequency results in higher switching losses in the converter and increases the iron power losses of an AC transformer. The study of losses in a front-to-front topology with MMC in [44] confirms that increasing the frequency the total system losses also increase. Concluding, a trade-off exists between the footprint and the total losses. In offshore projects where the footprint is the basic factor, a higher frequency can be chosen. However, as the most important factor in the current thesis is the system efficiency, a frequency of 50 Hz is chosen leading to lower total losses.

NUMBER OF PHASES

Three phases are usually used but more can be used for two reasons. Firstly, more phases will increase the power handling capability of the intermediate AC link of the DC hub. Secondly, the reliability of the system can be improved by having a redundant phase readily to connect in case of an internal fault or hub maintenance.

WAVEFORM

Apart from the sinusoidal waveform, different techniques have been seen in the literature where squared or trapezoidal waveform is used in the intermediate AC link. Especially, the trapezoidal waveform seen in [21] can lower the energy requirements of the converter cell capacitances leading to smaller footprints. However, the modulation range of the converter gets lower and the stresses on the AC transformer will increase and still these solutions are not as mature as the common sinusoidal waveform. The square waveform seen in the DAB converter results in high stresses on the AC transformer, leading to special transformer design. As a result, the sinusoidal waveform is chosen, offering the full range modulation.

AC TRANSFORMER

First of all, a transformer provides galvanic isolation in the circuit. A transformer is used in the intermediate AC link in order to increase the voltage conversion ratio by allowing the AC voltage magnitude seen by each MMC to be optimal, depending on its DC bus voltage. In a transformerless configuration due to the significantly different AC voltages, there will be circulating reactive power leading to high losses. In order to avoid this scenario, a common AC voltage for the intermediate AC link should be chosen. This decision can lead to some converters operating in undermodulation while others in overmodulation. In case of overmodulation in a port with lower DC-link voltage, full-bridge submodules should be used in order to get a modulation index higher than one ($m > 1$). As a result, the cost, size, and losses of the particular port will increase. In the case of undermodulation, there is no need of full-bridge submodules. However, the undermodulation results in poor device utilization for the port connected to the higher DC-link voltage. Moreover, in order to get the same amount of power, while operating in lower voltage, the current will increase. The presence of higher currents leads to a larger footprint and higher losses. Moreover, transformer topologies offer more advantageous solutions under large transients. It is stated in [45] that: " DC/DC can be developed for optimal loss and weight using non-isolated topologies, but isolated DAB possess advantages in terms of grounding and

under large transients ". Furthermore, except ports with different voltage, also different configurations can be connected with the presence of a transformer.

The MMC side of the transformer usually adopts the delta (D) connection, while the AC network side adopts the star grounded (Yg). In this way, the filtering of the harmonic and of the DC component in the windings is achieved. Moreover, the zero-sequence component caused by unsymmetrical faults is avoided by pouring into the AC system. Also, with this configuration, a zero-sequence component can be added in the output voltage resulting in a higher maximum nominal peak.

As a result, a transformer is used to adapt the different voltage levels in the AC link with a (D-Yg) configuration. Moreover, the following criterion is used. In case of N different voltage levels, N-1 transformers are needed to be used. In this way, every port operates in the optimal AC voltage.

4.1.3. DC LINK CONFIGURATION

There are different ways in which the HVDC system can be configured. The first division into monopolar and bipolar configurations can be done based on the number of the converters used at each terminal.

The monopolar HVDC system requires only one converter on each side for the power transmission and can be further divided into:

- Asymmetric monopolar with metallic return
- Asymmetric monopolar with ground return
- Symmetric monopole

The bipolar HVDC system uses two converters at each terminal. In comparison with the cost-effective monopolar configurations, bipolar can increase the power rating and the reliability of the system with the expense of increasing the cost and footprint of the system. They can be divided further into:

- Bipole with metallic return
- Bipole with ground return

The most commonly used configuration is the symmetric monopolar [46]. In this system, there are two high voltage cables connected to the positive and negative pole. Each of them carries half the rated power and it is subjected to full rated current and half the rated voltage.

In this configuration, there is no grounding on the DC side. As it will be shown in the DC fault study cases, the DC side is not fed by AC grids in case of a DC pole-to-ground fault. Also, the coupling transformer on the AC side is not subjected to any DC voltage. Nevertheless, in comparison to the other monopolar configurations two fully insulated conductors are needed.

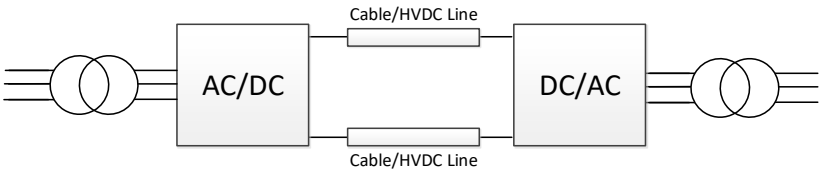


Figure 4.2: Symmetric monopole configuration

DC line modeling The pi-equivalent model is used for the DC line modeling. The uniformly distributed characteristics of an HVDC transmission line are represented by cascading identical pi-sections. The pi-equivalent model consists of lumped RLC elements as can be seen in figure 4.3.

The DC line parameters can be seen in the table 4.1.

Table 4.1: DC line parameters

DC line parameters	Unit	Value
Length (l)	km	80
Resistance (R)	Ω/km	0.0195
Inductance (L)	mH/km	0.18
Capacitance (C)	nF/km	250

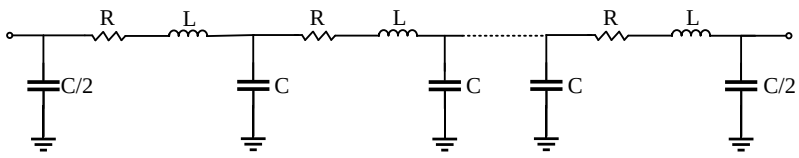


Figure 4.3: Pi-equivalent line section model

4.2. PORT DESIGN

In every port of the DC Hub, a modular multilevel converter is used. The design of an MMC is a complex and not straightforward procedure as seen in section 3.3. The design begins with the required power and voltage ratings and continues with the initial values of the converter components. In order to tune the main-circuit parameters, various calculations and simulations are performed. As a result, the whole process presents an iterative character.

The connection of ports with different DC link voltages and different power levels is studied. The values for the DC voltage and power level were chosen according to the latest trends [47]. These different values lead to different component values. In table 4.2 the different values for each port are presented.

Table 4.2: Port values

Ports	Port 1	Port 2	Port3
Power	300 MW	500 MW	800 MW
DC Voltage	$\pm 150kV$	$\pm 250kV$	± 320 kV

The design procedure shown in section 3.3 can calculate the submodule capacitance C_{sm}. However, in our average model the important parameter needed is the arm capacitance C_{arm}. The relation between the two is:

$$C_{arm} = \frac{C_{sm}}{N}$$

Where N is the number of SMs in the arm. The equivalent arm capacitance can be calculated based on the rule of thumb [34].

The total energy stored in the converter is given by the equation:

$$E = \frac{\frac{1}{2}C_{sm}}{N} \cdot V_d \cdot 6 \tag{4.1}$$

Where V_d is the pole-to-pole voltage and the energy requirements are

$$\frac{E}{P} = \frac{30kJ}{1MVA}$$

Based on the above, the equivalent arm capacitances can be calculated.

As far as it concerns the arm inductance, it is chosen equal to $0.07pu$ and the arm resistance is taken equal to 10% of the arm reactance.

The calculated values for each port are presented in the table 4.3.

Table 4.3: Component values

Ports	Port 1	Port 2	Port3
C_{arm}	$34\mu F$	$20\mu F$	$19\mu F$
L_{arm}	$25mH$	$41mH$	$43mH$
R_{arm}	0.75Ω	1.25Ω	1.28Ω

4.3. CONTROL ROLE DISTRIBUTION

The DC hub under study has three ports, where each port will operate in a different control mode. There are three possible control modes:

- AC voltage control
- DC voltage control
- Active power control

Moreover, each of the three ports will have a different power and a different DC link voltage level.The fact that there are three different control modes and three different rated powers for each port gives a variety of combinations. The different combinations are presented in table 4.4

Each port is connected in a point-to-point connection with another terminal. In a point-to-point connection, there must be one terminal operating in DC voltage control in order to maintain the DC link voltage of the transmission line stable. This leads to the fact that the terminal operating in AC voltage control mode will not be able to control its power directly. The power will be controlled indirectly through the other two ports.

Table 4.4: Different scenarios in control role distribution

Scenario	Port 1	Port 2	Port 3
1	Power	AC Voltage	DC Voltage
2	Power	DC Voltage	AC Voltage
3	DC Voltage	Power	AC Voltage
4	DC Voltage	AC Voltage	Power
5	AC Voltage	DC Voltage	Power
6	AC Voltage	Power	DC Voltage

For all the above combinations, a basic understanding of the power flow inside the DC hub can be gained. First of all, there is a port controlling its active power according to a given reference. Secondly, the port operating in DC voltage control has its active power controlled via the other terminal of the point-to-point connection. Finally, the converter operating in AC voltage control has its power indirectly controlled as the sum of powers in the DC hub is constant. This can be proven as the AC voltage in the intermediate AC link is constant and the Kirchoff's current law is valid.

The simulation results of the different scenarios show the following response during changing the active power and DC voltage references. During the transient phenomena triggered by ports operating in DC voltage or active power control mode, changes are observed only in the values of the triggered port and the port operating in AC voltage control mode. As a result, the AC voltage port takes part in the different transitions while the third port is uninvolved. Moreover, it has been observed that the larger the rated power of the port operating in AC voltage, the less the impact on its operation. Moreover, as it will be presented in section 4.4 in a DC voltage step, the charging or discharging energy of the submodule capacitors is provided or absorbed by the port operating in AC voltage control mode. In the worst case 6, a large change in the DC voltage will lead to larger energy changes on the port operating in AC voltage resulting in high arm currents and affecting more the port operation in comparison with case 3.

The AC voltage in the intermediate AC link is an important factor for the stability of the DC hub. For that reason, the port operating in AC voltage is chosen to have the highest rated power resulting in a more stable system. Following, the port operating in DC voltage is chosen to have the lowest rated power. Case 3 is chosen to be studied next on line connection/disconnection and DC fault responses.

4.4. MODEL VALIDATION

In order to gain a better understanding of the transient phenomena in the DC hub, point-to-point connections are added on each port. In this way, the fault response can be studied. Also in comparison with other studies where the DC link is modeled with an ideal DC voltage source, the system is now closer to the real case. The transients on the DC link of each port can now be studied through changes in the DC hub. The system that is going to be studied can be seen in figure 4.4. Two transformers are located in the AC link in order

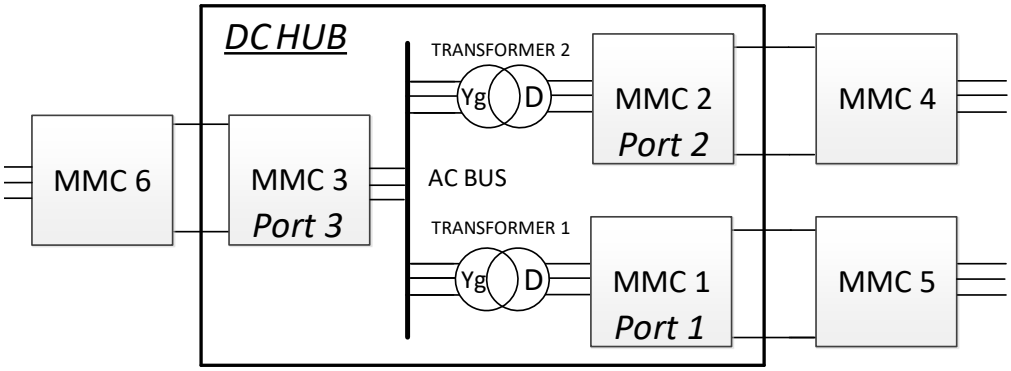


Figure 4.4: DC hub

to step-up the AC voltage at the level of port 3. Three point-to-point connections can be seen, where port 1 is connected to terminal 5, terminal 2 is connected to terminal 4 and terminal 3 is connected to terminal 6.

The port with the higher power rating operates in AC voltage control mode. This leads to a more stable system as transient phenomena observed in the other two ports will affect less the operation of the highest power port. The port with the lower power operates in DC voltage control mode. It is observed that the energy needs for charging/discharging the submodule capacitors in order to follow the DC voltage step reference are provided by the port operating in AC voltage control mode. For this reason, it is advantageous to choose the highest power rated port to operate in AC voltage control and the lower power port to operate in DC voltage control. The third one operates in active power control mode. The power flows from port 3 towards port 1,2 via the intermediate AC link of the DC hub. The active power in port 1 is controlled through terminal 5, while port 2 controls its own power. The active power of port 3 is the sum of the active power flowing through the other ports.

Table 4.5: DC hub parameters

System parameters	Unit	Value
Rated power (MMC1/MMC2/MMC3)	MVA	300/500/800
DC voltage(MMC1/MMC2/MMC3)	kV	±150/ ± 250/ ± 320
Transformer rated power(1/2)	MVA	300/500
Transformer voltage ratio (MMC1/MMC3)	kV	150/320 (D-Yg)
Transformer voltage ratio (MMC2/MMC3)	kV	250/320 (D-Yg)
Transformer leakage inductance	pu	0.1

In order to validate the model, its operation is studied under changes on control references. From the six possible combinations the case 3 is chosen to be studied more in depth as it is the most advantageous. Three different cases are studied:

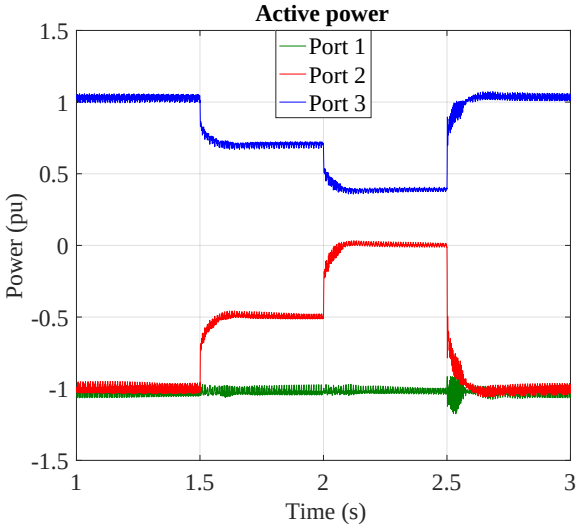
1. Active power reference step change
2. DC voltage reference step change
3. AC voltage reference step change

Per unit base In the following chapters, the figures of the most important values are presented. The per-unit system is chosen for the representation of the different values. Each port uses its own base values according to its rated power and DC voltage. For the representation of the sinusoidal values, the peak value is used as a base, in order to gain a better understanding of the overvoltages and overcurrents that can be present in the system.

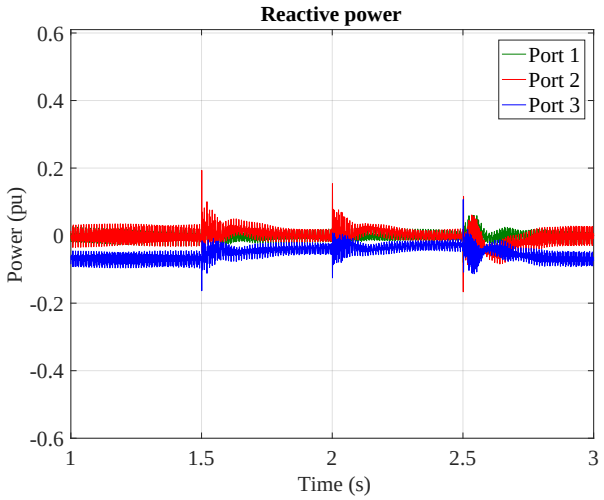
4.4.1. ACTIVE POWER REFERENCE CHANGE

Port 2 operating in active power control mode changes its reference according to the table 4.6. The following changes on the active power on every port are seen in figure 4.5a. The negative sign (-) denotes the port

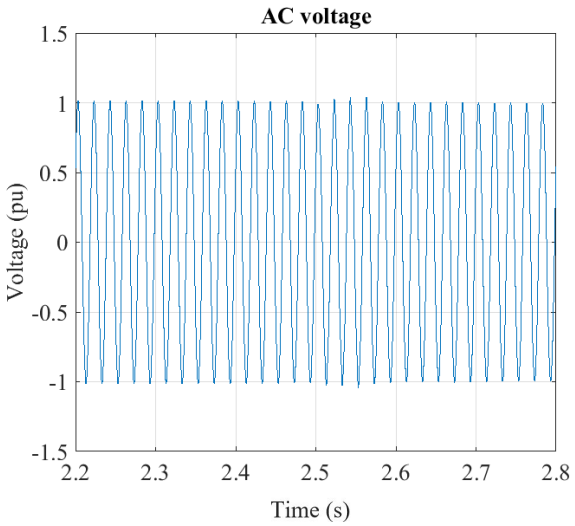
is absorbing power from the DC hub and the positive sign (+) denotes that the port is feeding power. It is important to see that the step references are followed. The power of port 1 operating in DC voltage control is controlled from terminal 5 via the point-to-point connection. As a result, its power is controlled to 1 pu and stays unaffected from the power changes in the rest of the DC hub. In contrast, port 3 responsible for the AC voltage control follows the power steps of port 2. The reactive power is shown in figure 4.5b. Port 1 and 2 have reactive power control and their values are controlled to the zero reference. Port 3 does not have a reactive power control, however, due to the reactive power control of port 1 and 2, its reactive power value is close to zero. Moreover, the results in figure 4.5c indicate that the AC voltage of the DC hub remains stable during the power changes. It can be seen that at $t = 2.5$ when $P_2 : 0 \rightarrow -1pu$ a small decrease in AC voltage is observed. This decrease is a result of the decrease in port's 3 DC voltage.



(a) Active power at each port



(b) Reactive power at each port



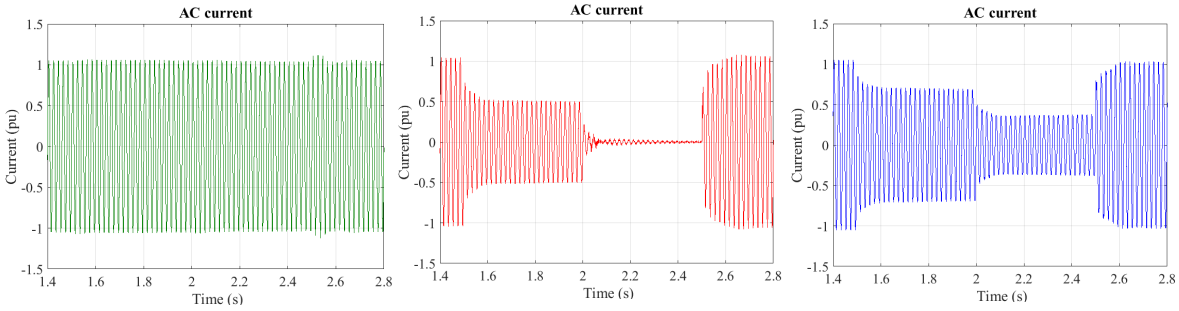
(c) AC voltage

Figure 4.5: Values during changing active power reference

Figure 4.6 presents the AC currents in the intermediate AC link of each port. According to the power steps in each port, while the AC voltage is maintained stable the presented current results were expected. The same current changes are also observed on the arms of the converters as shown in figure 4.7.

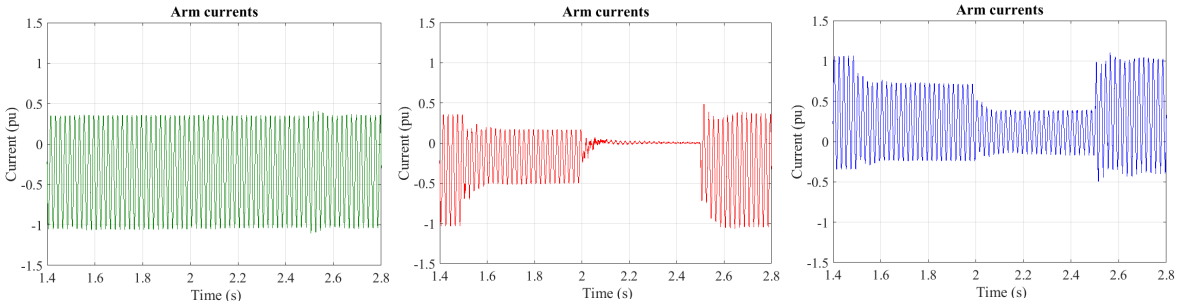
Table 4.6: Power reference steps

Time (s)	Power (pu)
0	-1
1.5	-0.5
2	0
2.5	-1



(a) Port 1 (b) Port 2 (c) Port 3

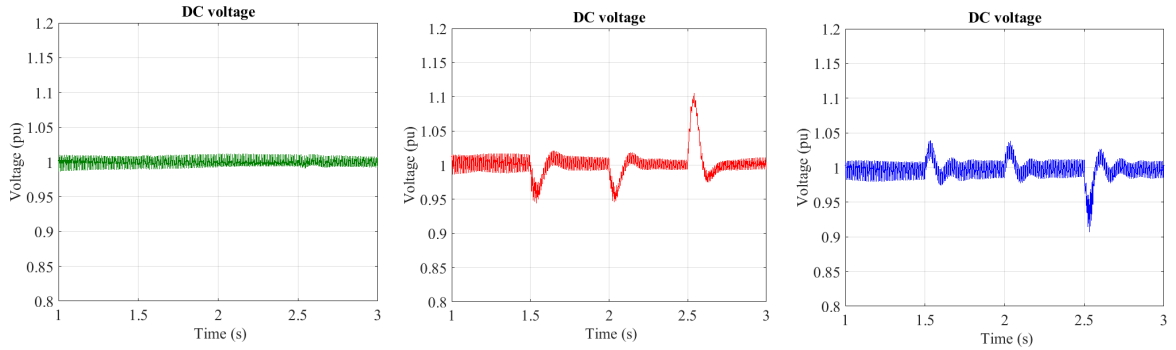
Figure 4.6: AC currents in the intermediate link during changing active power reference



(a) Port 1 (b) Port 2 (c) Port 3

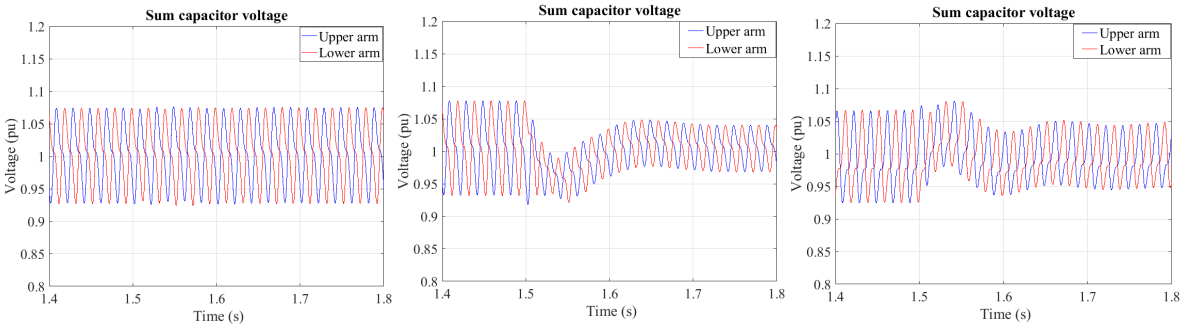
Figure 4.7: Arm currents during changing active power reference

Figure 4.8 provides the results of the DC voltage values of each DC link during the changes in power references. A power decrease of $0.5pu$ leads to a DC voltage decrease of $0.05pu$. This small undervoltage lasts for $t = 100ms$ caused by a power step of $0.5pu$. This can be explained by observing the sum capacitor voltages of port 2 in figure 4.9b. After the power decrease step, the AC current in the intermediate link decreases. Instantly, this current decrease leads to a lower V_{cap2} by discharging the capacitors. Moreover, it can be observed that in a lower power the voltage ripple of the capacitors is now smaller. The terminal 4 responsible for DC voltage control drives the V_{dc2} to its nominal value. In comparison with port 2, in port 3 an increase of DC voltage is observed for the same power step. This increase can also be seen in the sum capacitor voltages in figure 4.9c and can be following explained. Port 3 provides with power the port 2. As the power needs are now lower, the submodule capacitors will absorb the extra power not taken by port 2. This corresponds to a small increase as the port 3 changes its power according to the needs of port 2. Terminal 6 restores the DC link voltage of the point-to-point connection between port 3 and terminal 6.



(a) Port 1 (b) Port 2 (c) Port 3

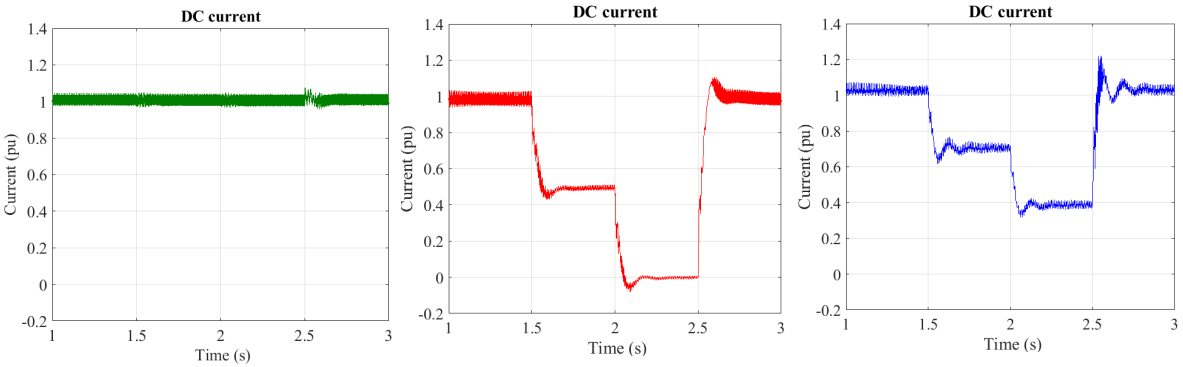
Figure 4.8: DC voltages during changing active power reference



(a) Port 1 (b) Port 2 (c) Port 3

Figure 4.9: Sum capacitor voltages during changing active power reference

By controlling the DC link voltage to its nominal value, the power steps on each port result in DC current steps as seen in figure 4.10.



(a) Port 1 (b) Port 2 (c) Port 3

Figure 4.10: DC currents during changing active power reference

It is apparent from these results that port 1 is uninvolved during the power changes of port 2. A very small observation can be made when the AC voltage drops for a small amount. In order to maintain the power at $1pu$ port 1 increase its current needs. This small current increase is observed in the intermediate AC, arm and DC currents of port 1.

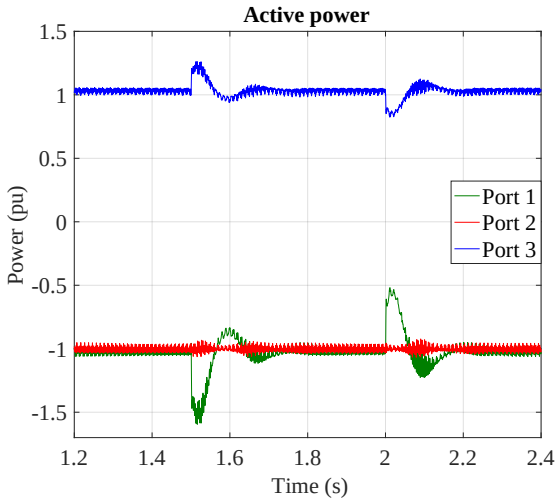
Overall, these results indicate that even large power steps (1pu) can be performed and the system maintains its stability. After the performed step, the active power reaches the reference value in less than $200ms$.

4.4.2. DC VOLTAGE REFERENCE CHANGE

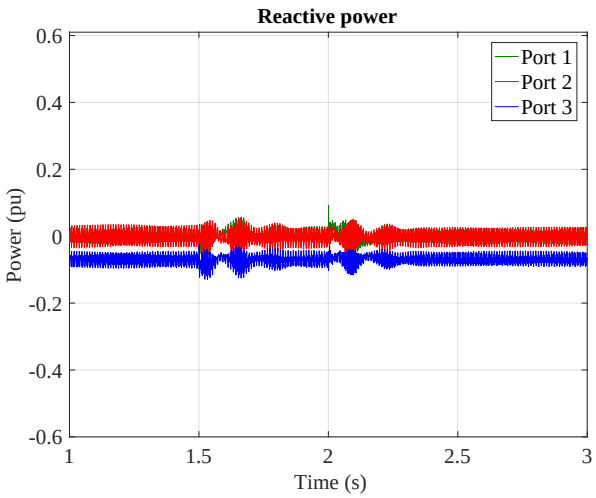
Port 1 operating in DC voltage control mode changes its reference according to the table 4.7. These steps represent a worst case scenario as voltage steps of $0.1pu$ are rarely performed. The following changes on the active power on every port are seen in figure 4.11a. During these DC voltage steps, the AC voltage of the intermediate link is controlled to its nominal value.

Table 4.7: DC voltage reference steps

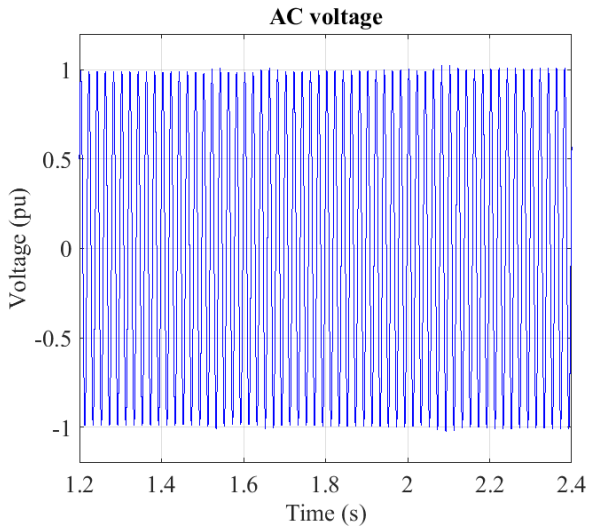
Time (s)	DC voltage (pu)
0	1
1.5	1.1
2	1



(a) Active power at each port



(b) Reactive power at each port

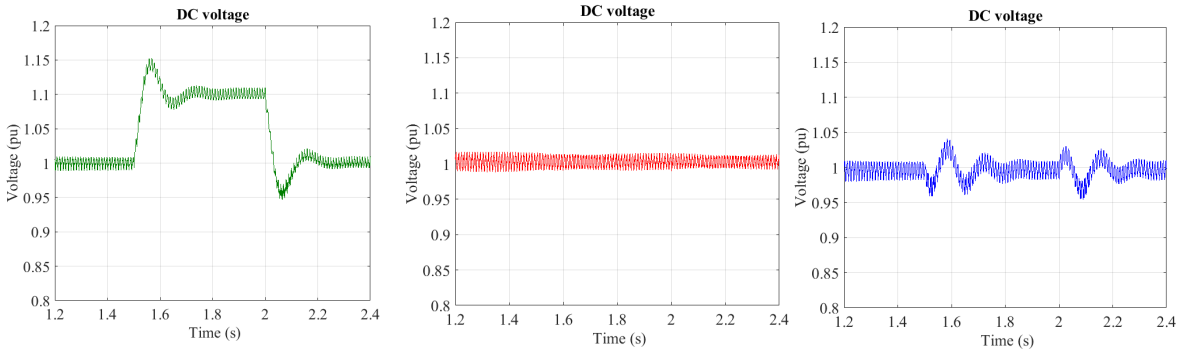


(c) AC voltage

Figure 4.11: Values during changing DC voltage reference

Figure 4.12 presents the voltage steps in the DC links. It can be observed that the DC voltage reference steps are followed by port 1. The reference value is reached after $200ms$. In order to acquire a higher voltage level, the sum capacitors of port 1 need to charge. The energy needs for this charging are provided by port 3. As a result, as the AC voltage is kept constant, larger currents are observed on the AC link and the arms of port

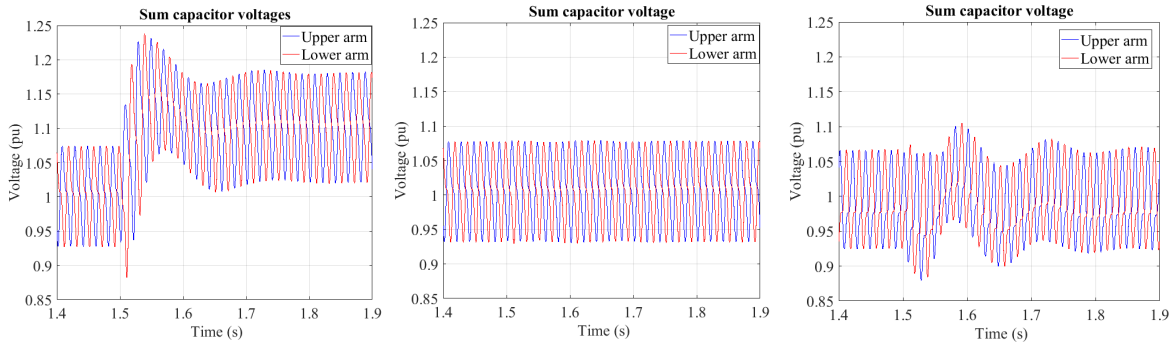
1 and 3 as seen in figures 4.14 and 4.15. This results in power increase as seen in figure 4.11. Correspondingly, the opposite changes are observed during a decrease in DC voltage, where submodule capacitors now need to discharge. In figure 4.11b the reactive power at each port can be seen. The reactive power is controlled at the reference value.



(a) Port 1 (b) Port 2 (c) Port 3

Figure 4.12: DC voltages during changing DC voltage reference

The performed voltage step can be also seen in the sum capacitor voltages in figure 4.13. It is observed that the mean value increases from $1pu$ to $1.1pu$ while the capacitor ripple remains the same as the power level remains stable at $1pu$ controlled by terminal 5. Also, the voltage ripple of the rest of the ports remains the same as there is no active power change.



(a) Port 1 (b) Port 2 (c) Port 3

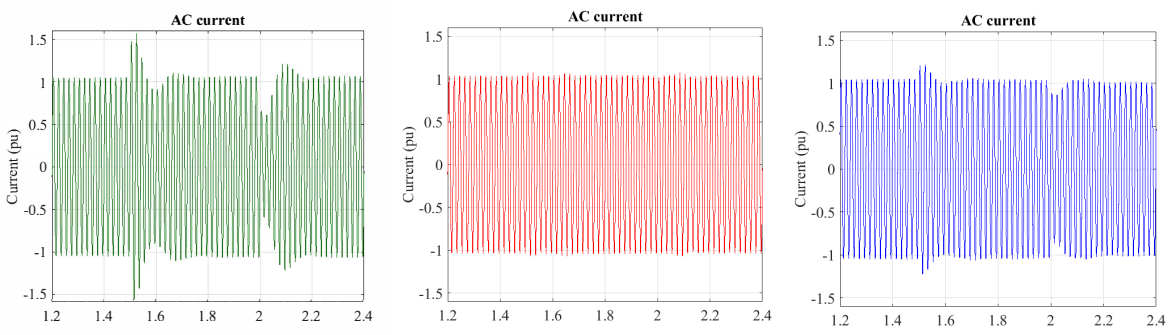
Figure 4.13: Sum capacitor voltages during changing DC voltage reference

From the figure 4.14, we can see that after some transients the AC currents return to their nominal values in order to maintain their reference power values given a stable AC voltage value. Furthermore, the observed arm current peaks stay between the predefined limits as seen in figure 4.15. It is observed that as the V_{dc1} increases, the I_{dc1} decreases in order to maintain the active power flowing through the point-to-point connection constant to 1 pu.

Concluding, when DC voltage of port 1 changes, no significant changes are observed in the values of port 2 operating in active power control mode. Contrariwise, port 3 is responsible to cover the power needs of port 1. What is interesting in these simulation results is the fact that port 2 is not influenced from the DC voltage steps of port 1 and continues its normal operation as can be seen from the presented figures.

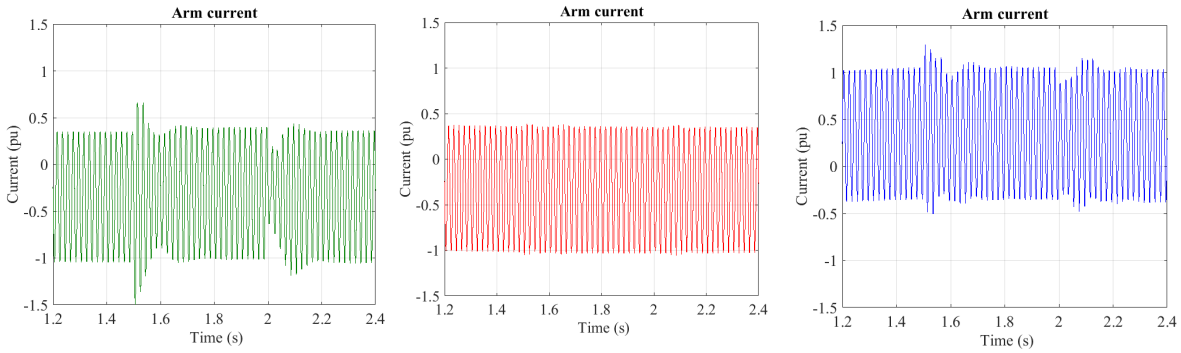
The results of this case together with the previous case of power reference changes show that the operation of port 1,2 is unaffected during step reference changes of port 2,1 correspondingly. Port 3 is responsible to cover the energy needs of port 1 and 2 and at the same time to maintain the AC voltage of the intermediate AC link stable at $1pu$.

It is noticed that the values of each port are expressed in per-unit according to their base. For this reason, as port 3 is the port with the highest power rating, the per-unit changes in its value are seen smaller in comparison to ports 1 and 2. This can lead us to the conclusion that if port 3 was not the port with the high-



(a) Port 1 (b) Port 2 (c) Port 3

Figure 4.14: AC currents in the intermediate link during changing DC voltage reference



(a) Port 1 (b) Port 2 (c) Port 3

Figure 4.15: Arm currents during changing DC voltage reference

est power rating, the transient phenomena observed in its values could be larger and more influential to its stability. This fact due to the importance of a stable AC voltage would not be acceptable.

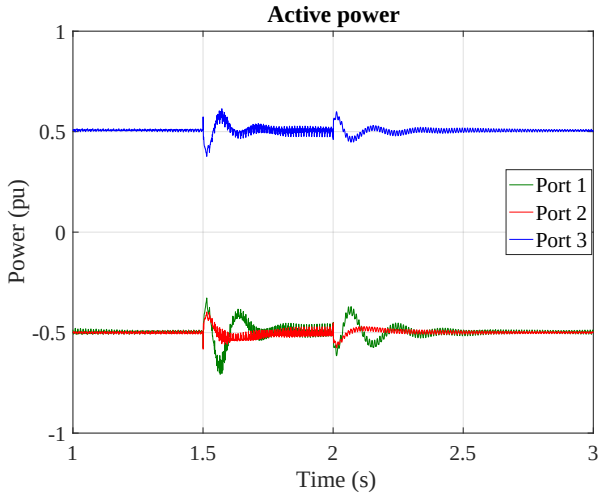
4.4.3. AC VOLTAGE REFERENCE CHANGE

Port 3 operating in AC voltage control mode changes its reference according to the table 4.8. For the following voltage steps, all the ports are chosen to operate in lower power as the decrease in the AC voltage leads to undermodulation of the converters resulting in higher currents. Figure 4.16c presents the AC voltage following the reference steps. The active power is presented in figure 4.16a. The values are controlled at its reference. In figure 4.16b the transients observed in the reactive power at each port are presented. After the AC voltage step, both active and reactive power maintain their reference values after some transients.

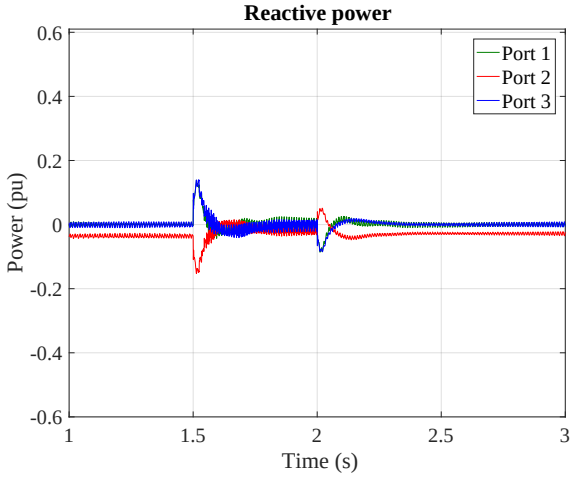
Table 4.8: AC voltage reference steps

Time (s)	AC voltage (pu)
0	0.7
1.5	1
2	0.8

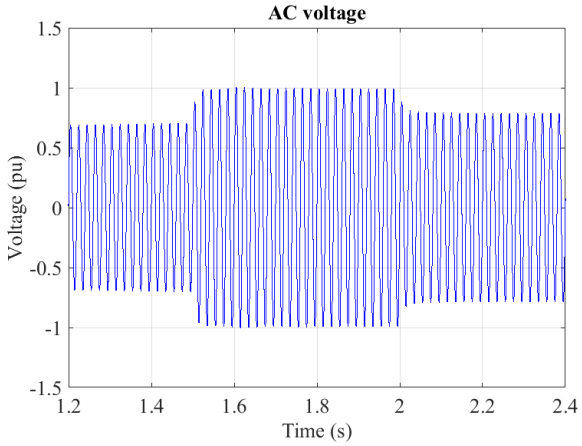
The results obtained from the simulations are following presented. It is observed in figure 4.17 that the AC currents decrease their values as the AC voltage increases in order to achieve a constant power level. Following, the arm current values decrease as seen in figure 4.18. The decrease in the arm currents leads to smaller sum capacitor voltage ripples as shown in figure 4.20. Finally, the DC voltages of all the ports are controlled to their nominal value as presented in figure 4.19. The small transients observed in the DC voltages originate from the current changes. Respectively, same conclusions can be made for the AC voltage decrease.



(a) Active power at each port



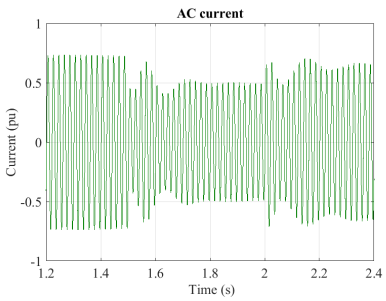
(b) Reactive power at each port



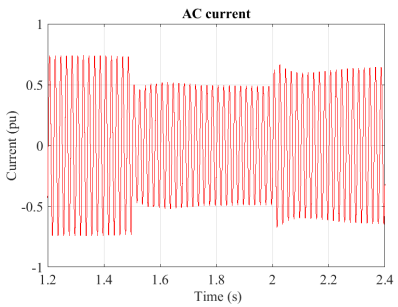
(c) AC voltage

Figure 4.16: Values during changing AC voltage reference

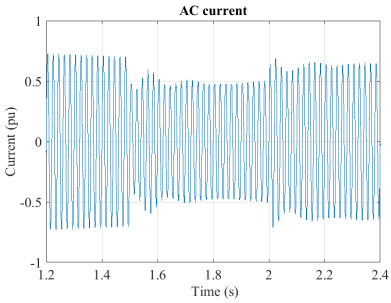
In comparison with the previous cases, the AC voltage changes lead to transients with larger duration. However, step reference changes will be rarely performed as the objective of the port 3 is to maintain the AC voltage in the reference value. Overall, The reference values are followed and the system maintains its operability without any large currents or voltages present on the system.



(a) Port 1

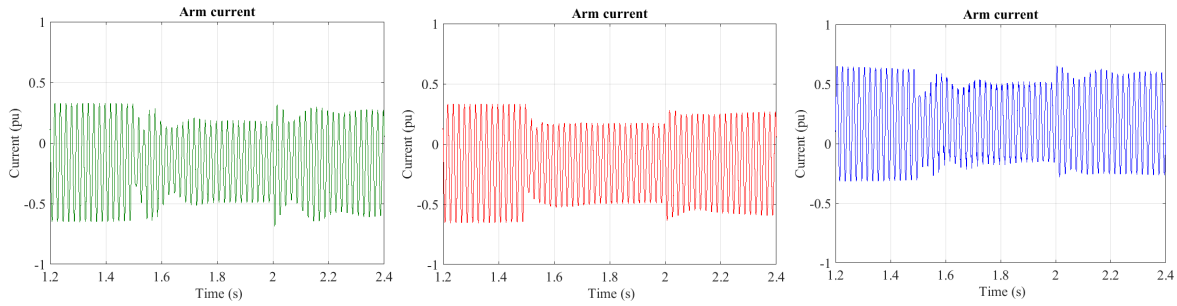


(b) Port 2



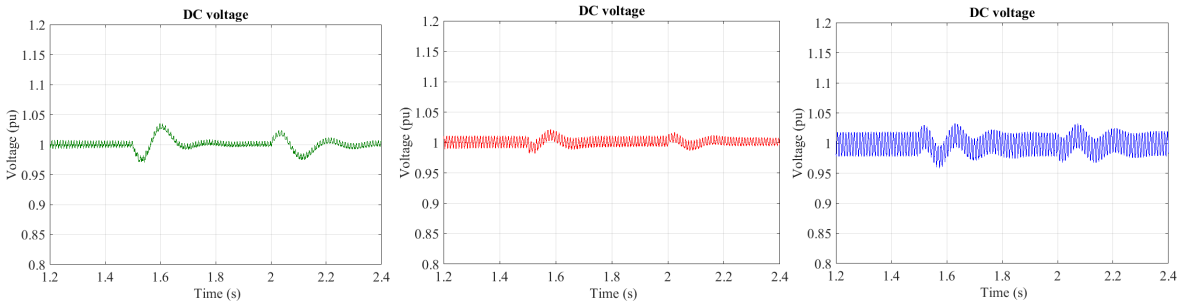
(c) Port 3

Figure 4.17: AC currents in the intermediate link during changing AC voltage reference



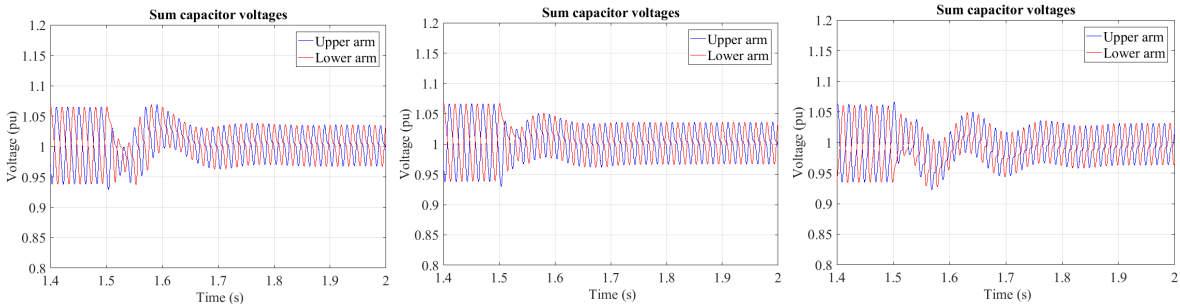
(a) Port 1 (b) Port 2 (c) Port 3

Figure 4.18: Arm currents during changing AC voltage reference



(a) Port 1 (b) Port 2 (c) Port 3

Figure 4.19: DC voltages during changing AC voltage reference



(a) Port 1 (b) Port 2 (c) Port 3

Figure 4.20: Sum capacitor voltages during changing AC voltage reference

4.5. CONCLUSIONS

In this chapter, the values of the different components in the system were presented. Through the early design, basic objectives of the DC hub are fulfilled. The transformers in the intermediate AC link provide the voltage stepping required between the different DC lines. Moreover, the modular design of the DC hub offers connection points for expansion. Any number of ports can be added by connecting to the intermediate AC link via a transformer. The DC hub connecting to three other terminals via point-to-point connections is presented in figure 4.4.

A discussion and a suggestion for the control role distribution took place next. The port with the higher power rating is chosen to operate in AC voltage control while the less powerful in DC voltage control. Finally, the model was validated through simulations in Matlab/Simulink.

Overall, the simulation results suggest that in normal operation the system maintains its stability as is was

shown through different step changes on the controlled values. Moreover, as seen from the performed reference steps in the controlled values of active power, DC and AC voltage, the real values follow the references.

The results provide important insights as far as it concerns the control role distribution. The converter with the higher power rating is chosen to operate in AC voltage control. Apart from the voltage control it is responsible to provide (absorb) power to(from) the other two ports (1,2) and has the capability to absorb or provide the transient currents which due to the higher power rating have less impact on its operation. In this way, it is proven that with the suggested control scheme a stable operation of the DC hub can be achieved. In this chapter, the controllable power exchange of any HVDC line with any other line connected to the hub was acquired. This is one of the main objectives of the DC hub. In the next chapter, the DC hub response to a line connection/disconnection is studied

.

5

PORT CONNECTION AND DISCONNECTION

A DC hub must have the capability to connect and disconnect a DC line without affecting the operation of the rest of the system. A DC hub can be seen as a central node where new HVDC point-to-point links can be connected. In order to connect or disconnect a new line, some first steps should be identified.

5.1. PORT CONNECTION

The first part to be studied is the connection of a new DC line with the DC Hub. The connection takes place by closing the AC circuit breakers in the intermediate AC link of the terminal to be connected, achieving a connection with the intermediate AC link of the DC Hub. It is assumed that the port responsible for the AC voltage control is already connected. There are two different scenarios in the connection of a new port. The two different cases depend on the chosen control mode of the converter to be connected. In a point-to-point connection, one terminal is responsible for the active power control while the other is responsible for controlling the voltage of the DC link.

In the first case, in the point-to-point connection, a terminal is already connected to an AC network operating in DC voltage control mode, while the other terminal to be connected to the DC Hub will operate in active power control mode. In the second case, first, the connection of the port with the DC hub will take place. The port needs to operate in DC voltage control in order to establish and maintain a stable DC voltage on the point-to-point connection. Following, the other terminal operating in active power control mode will connect again via AC circuit breakers with an AC network.

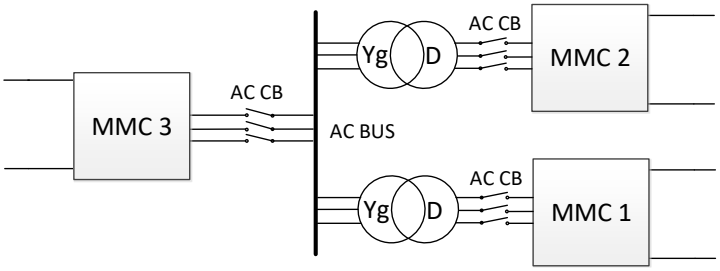


Figure 5.1: AC breakers in the DC hub

5.1.1. CASE 1 CONNECTION OF PORT OPERATING IN ACTIVE POWER CONTROL MODE

In the first case, terminal 4 is already connected to an outer AC grid and port 2 is connected to the DC hub as can be seen in figure 5.2. The steps to be followed are:

1. First, the new line to be connected should be energized. The converter responsible for the DC voltage control should be in operation resulting in a DC line having the nominal value.
2. After the energization process, the point-to-point connection has achieved to reach the nominal DC voltage value. In order to effectively connect the line, there should not be any power transfer from the

outer system to the DC hub. In that way, a smooth connection limiting transient phenomena will be achieved.

3. The next step is to close the AC circuit breakers and connect the AC part of the new port with the intermediate AC link of the DC Hub.
4. After the successful connection, the new port controlling the power can start the power exchange between the DC Hub and the point-to-point connection.

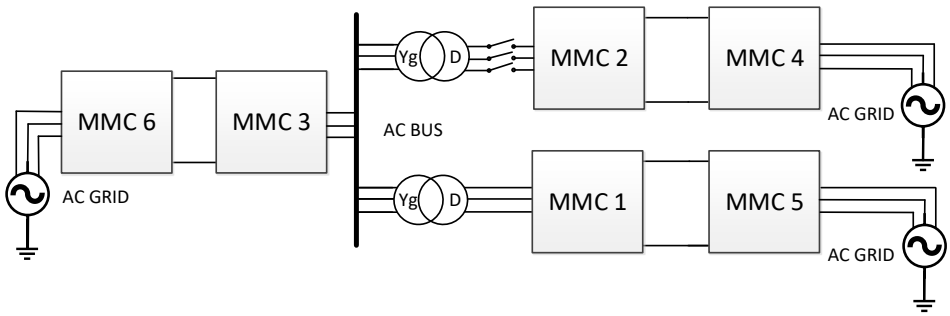
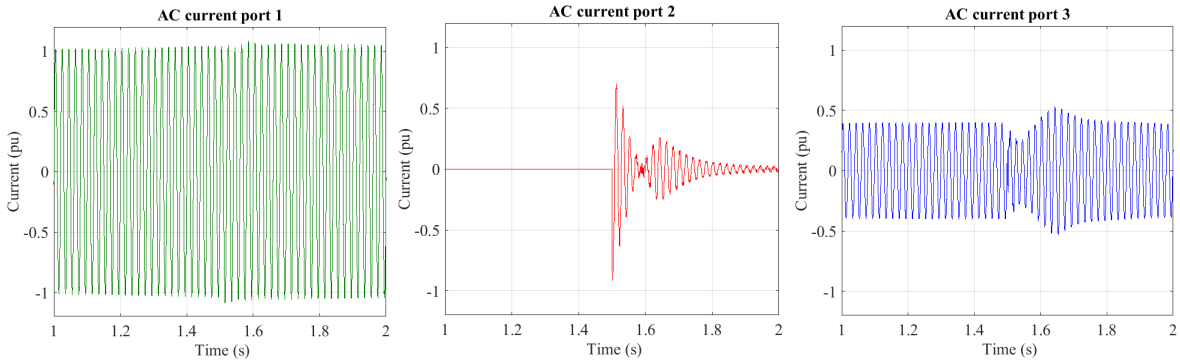


Figure 5.2: Connection of port 2

The case of connecting port 2 is studied. Port 2 operates in active power control mode. Terminal 4 operates in DC voltage mode and is responsible to maintain the DC link voltage to its reference value. After the connection of the port 2, an inrush current is observed from the port 2 towards the inner of the DC hub as shown in figure 5.3b. It is observed that the submodule capacitors of the connected port discharge. This can be also seen in figure 5.4b, where the DC voltage drops. Port 1 is operating in DC voltage control and terminal 5 is responsible for the active power control of the point-to-point transmission line $p1p5$. As a result, the power and current of port 1 remain at their rated values during the connection. While port 3 absorbs the connection current. The inrush current towards port 3 charges the submodule capacitors. This leads to DC voltage increase in port 3 as seen in figure 5.4c.

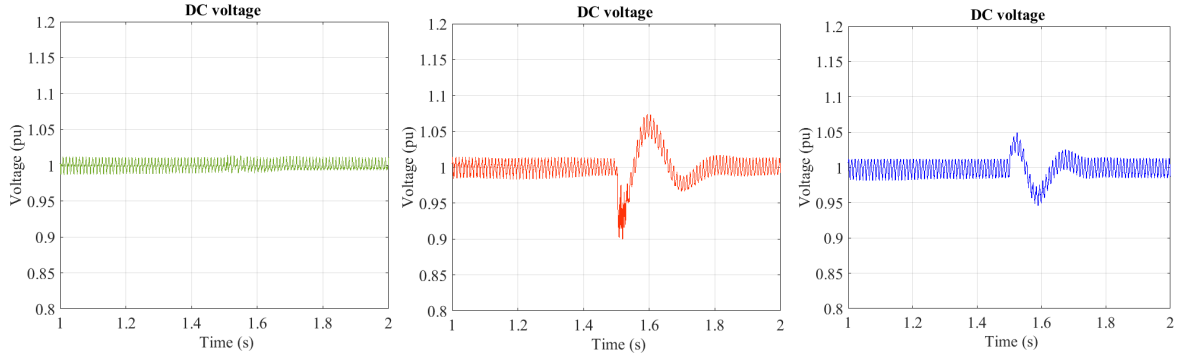
The total power of port 3 is now lower. It is the sum of the power needed to cover the needs of $p1p5$ and the power absorbed from the connection of port 2. Terminal 4 is responsible for controlling the DC link voltage of the $p2p4$. Current (energy) is needed in order to charge the submodule capacitors and return the DC voltage to its nominal value. This extra energy is given by the DC hub through port 3. After some transients, DC link voltage returns to its nominal value.The power exchange of the DC hub with the point-to-point transmission line $p1p5$ is controlled by the terminal 5. In contrast in the $p3p6$ there is no direct power control, as the power of this port is the sum of ports 1 and 2. As a result, the current change caused by the new port connection will only be seen by the port 3 while port 1 maintains a stable current. Port 3 provides power to port 1. The change of active power in the DC hub can be seen in figure 5.5.

The AC currents in the intermediate AC link of each port are shown in figure 5.3. It can be observed that the AC current of port 1 maintain the same value during the port connection. Port 2 and 3 do not present any large currents in their AC side. The arm currents of port 2 and 3 are shown in figure 5.6 for $R = 0\Omega$. A large current with a value higher than 1pu is observed in the connected port.



(a) Port 1 (b) Port 2 (c) Port 3

Figure 5.3: AC currents on the intermediate link



(a) Port 1 (b) Port 2 (c) Port 3

Figure 5.4: DC link voltages at each port

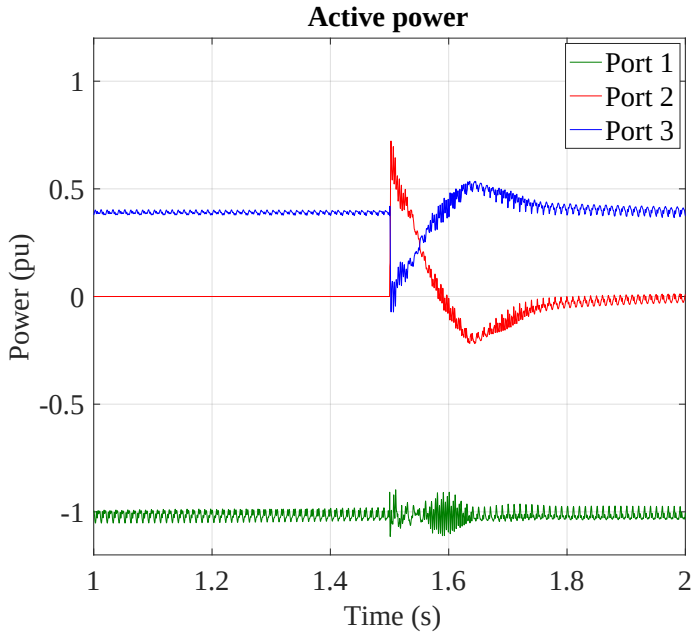


Figure 5.5: Active power at each port

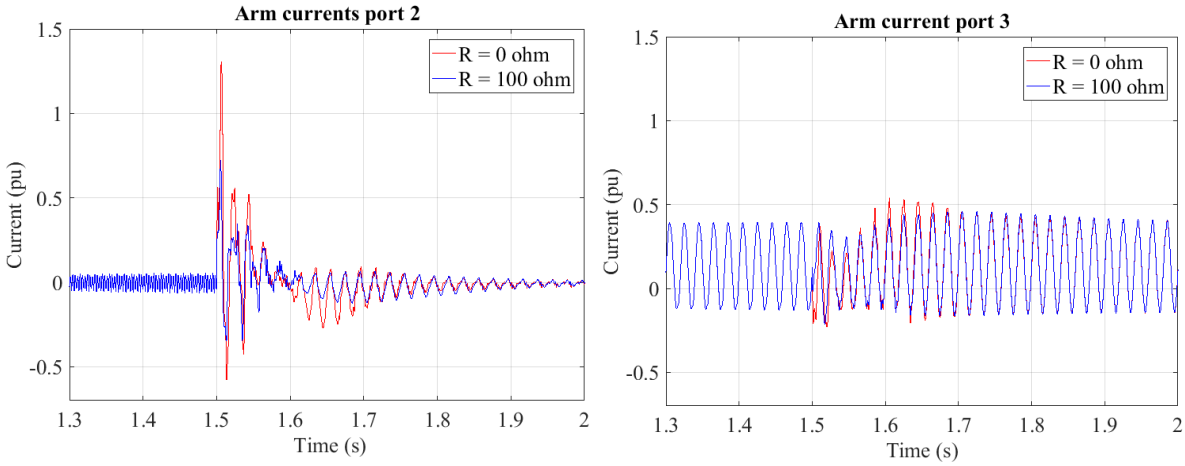
At the moment of the connection, an inrush current from the port 2 towards the inner of the DC hub is observed, resulting in changes in the inner AC current of each port. Following, these currents flowing through

the arms of the converter will lead to DC voltage changes. These changes can be seen in figure 5.4. As there are no current or power changes on port 1, the DC voltage will also remain stable. However, in ports 2 and 3 a small oscillation is observed on the DC voltages before they return to their nominal values as seen in figure 5.4. It is observed that the DC voltage ripple for the connected port 2 is below 0.1 pu while for the port 3 is below 0.05 pu. Moreover, port 2 returns to the nominal value after 300ms while port 3 after 150ms.

Port 3 has the highest power rating in the DC hub with $P_{2base} = 500MW$ while $P_{3base} = 800MW$. All the results are presented in the per-unit system. It can be observed that the changes in the values of port 3 correspond to larger changes for port 2 in the per-unit system.

INSERTION RESISTORS

In this case of connection, the AC currents in the intermediate AC link are kept bellow 1pu as shown in figure 5.3. Furthermore, the arm currents of the connected port reach a value of 1.3pu while in port 3 remain below 0.52 pu. In order to achieve an even smoother connection, insertion resistors can be added during the connection. By inserting resistors, the peak currents on the arms are smaller compared with the previous case as shown in figures 5.6a and 5.6b. Also, the current peaks observed in the intermediate AC link are lower. In this way, the components of the system can be protected and a more stable operation can be achieved.



(a) Arm currents in port 2

(b) Arm currents in port 3

Figure 5.6: Comparison of values with insertion resistors

5.1.2. CASE 2 CONNECTION OF PORT OPERATING IN DC VOLTAGE CONTROL MODE

A different case of connection is studied as can be seen in figure 5.7. Port 1 is operating in DC voltage control mode. The steps to be followed are now different. In this case, the DC hub will be first connected to port 1. The hub will energize the DC transmission line $p1p5$ via port 1. After reaching a steady state, the terminal 5 can be connected to the AC grid. Before the connection, port 2 operates in active power control mode and port 3 in AC voltage control mode. Power is injected to the hub, through port 3 in order to cover the needs of the point-to-point transmission line $p2p4$. For the simulation purposes, the submodule capacitors are charged to their nominal value. This leads to the DC line being charged to its nominal value before the connection with the DC hub.

After the connection, an inrush current is observed flowing towards the inner of the DC hub. The submodule capacitors of port 1 are discharging. Port 2 continues its normal operation without being affected by this inrush current. However, port 3 is the converter operating without a direct power control, as a result, all the transient currents flow through this converter. In figure 5.8 the AC currents of each port are shown. The inrush current is absorbed by port 3. At this point, this extra power is subtracted from the power injected to cover the needs of port 2 leading to a lower total active power for port 3 shown in figure 5.10a.

Port 1 starts its operation on DC voltage control mode. In order to reach the nominal value of the DC line voltage, the capacitors need to be charged again. The current and consequently the energy to charge the capacitors is given by port 3. At this point the active power injected through port 3 to the DC hub is higher than the rated. It is the sum of the power towards port 2 to cover its needs and the power flowing to port 1 in order to charge the capacitors. Port 1 after some oscillations reaches its reference value.

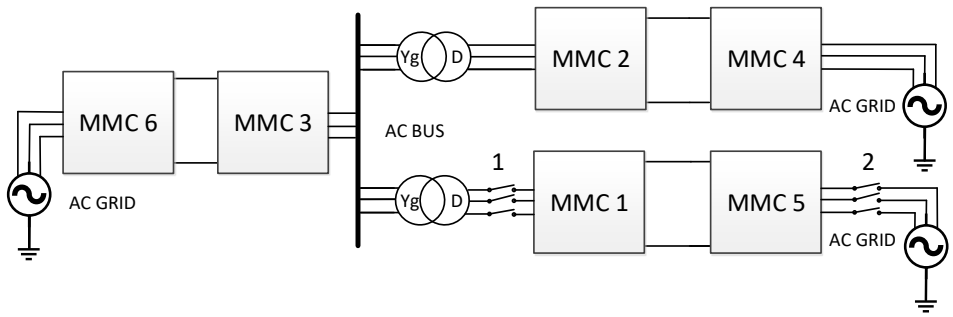
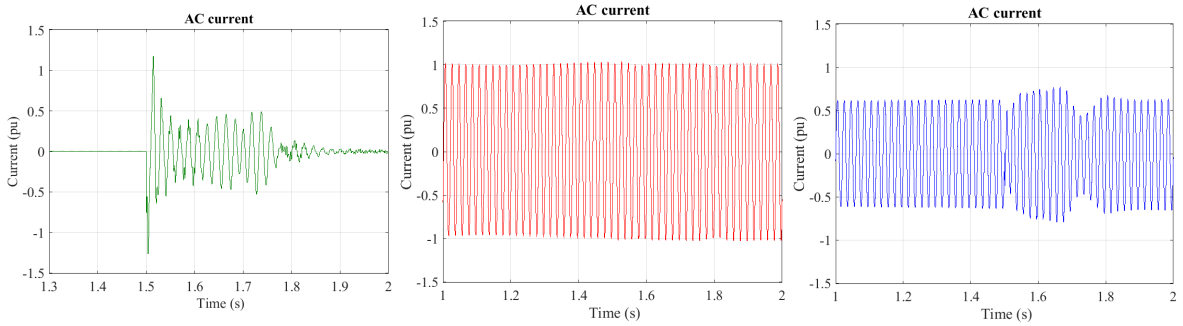


Figure 5.7: Connection of port 1

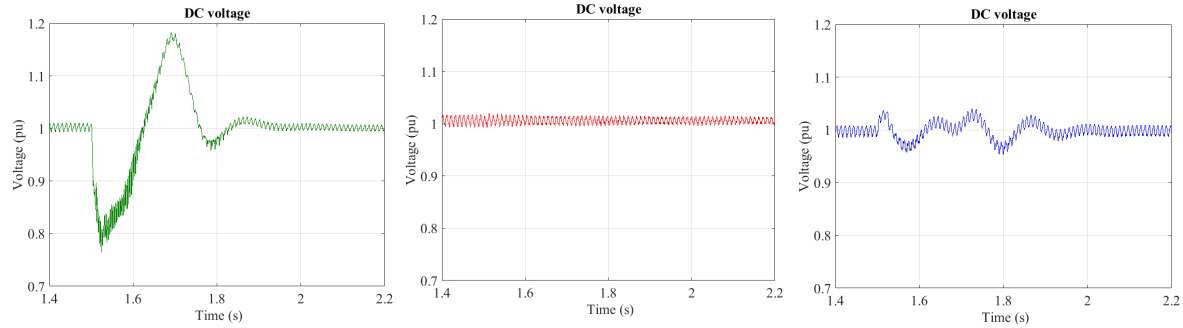
Throughout these events, port 2 continues its normal operation without being affected by the changes taking place in the rest of the DC hub. Also, the operation point of port 2 does not affect the connection of the new line. The changes in the power of port 3 lead to power changes at terminal 6 in the other point of the point-to-point connection. Terminal 6 is responsible for keeping DC voltage stable. Some small oscillations are present in the DC voltage of port 3 throughout this period.



(a) Port 1 (b) Port 2 (c) Port 3

Figure 5.8: AC currents of the intermediate link

The submodule capacitors' discharge leading to voltage drop in the DC link of port 1 can be seen in figure 5.9. Also, small oscillations are observed in port 3. After 500ms the V_{DC2} andV_{DC3} return to their nominal value. At that point, the terminal 5 can be connected via AC breakers to the outer AC grid in order to complete the connection of the point-to-point transmission line.



(a) Port 1 (b) Port 2 (c) Port 3

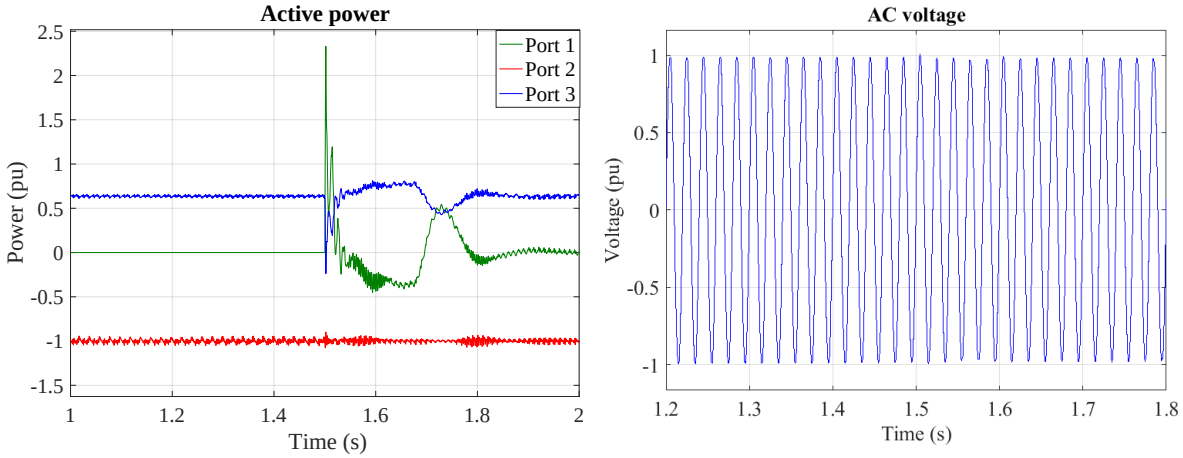
Figure 5.9: DC link voltages at each port

Concluding, the stable operation of the DC hub is maintained and the AC voltage of the intermediate link is shown in figure 5.10b. In comparison with the previous case, the discharge of the submodule capacitors is

now larger leading to larger voltage drop in the DC line voltage. Moreover, the peak currents of the AC and DC values are now higher. Reasons for that can be:

1. In comparison with the previous case, the other terminal of the point-to-point connection is not connected to an external AC grid.

2. Before the connection, there is no terminal operating in DC voltage control. The new port will start operating in DC voltage control at moment of the connection.



(a) Active power of each port

(b) AC voltage

Figure 5.10: Values during port 1 connection

INSERTION RESISTORS

On the AC side, in series with the AC breakers, a set of charging resistors in order to limit the inrush current can be added.

The addition of an insertion resistor $R_{ins} = 50\Omega$ leads to the following:

- The peaks of the AC intermediate link and arm currents are now lower. In figure 5.11a it can be seen that while the arm current peak was $1.3pu$, with the insertion resistors has a lower value of $0.6pu$
- In figure 5.11b is observed that the undervoltage observed in the connected port has a value of 0.88 in comparison with the previous case where was $0.79pu$. Finally, in port 3 the DC voltage oscillations have a value of ± 0.04.

Overall a smoother transition with lower peak values is achieved.In figure 5.11 a comparison for the arm currents and DC voltage values is presented.

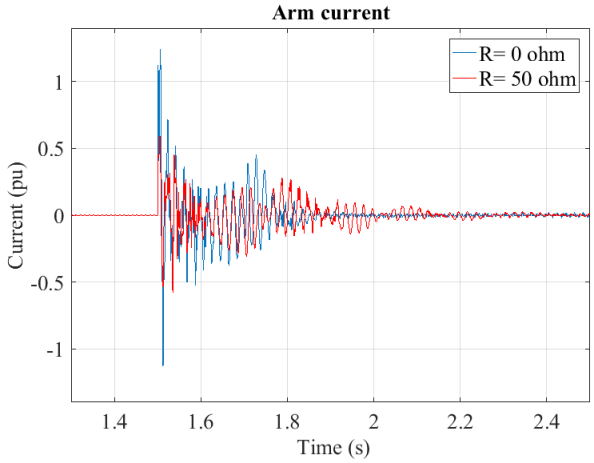
A high inrush current at the time of connection is observed in both connection cases. This inrush current can be following interpreted. At the time of connection the connected port, having a nominal AC voltage, "sees" through the DC hub a very small resistance. For this reason, the inrush current is high.

$$I_{con} = V/R$$

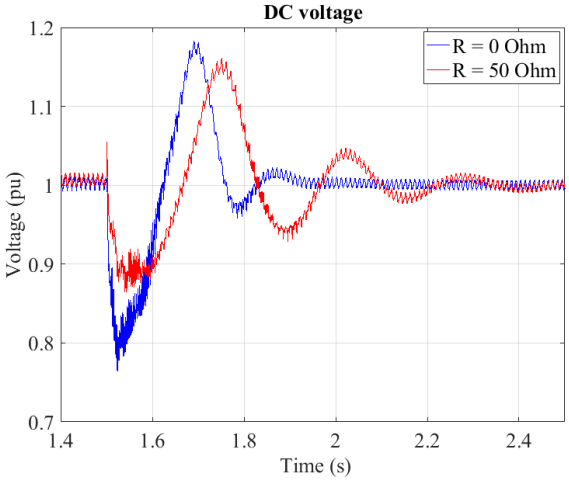
This conclusion is further confirmed with the addition of insertion resistors in the AC intermediate link resulting in lower current peaks during the transients. Overall the following observations were made:

- During the connection only port 3 is affected by the transient events.
- The operation of the port 1 or 2 prior, during or after the connection does not affect or be affected directly by the connection of port 2 or 1 correspondingly.
- Insertion resistors can be added for a smoother connection and lower inrush current.

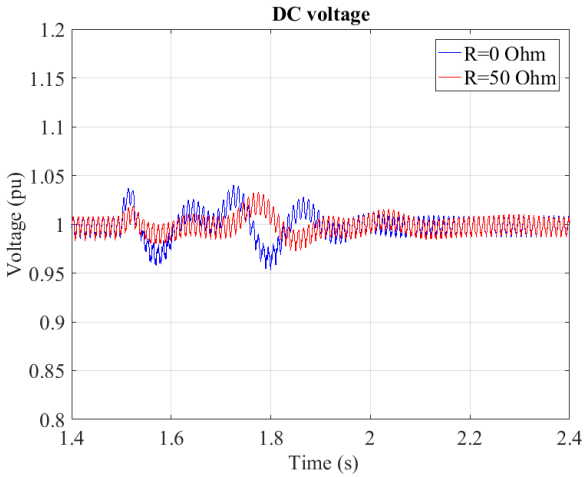
An important difference between the two cases is the connection of the point-to-point transmission line with an outer AC grid. In the first case, the transmission line is already connected to an outer AC grid and next is connected to the DC hub. In the other case, the transmission line is first connected to the DC hub and then



(a) Arm currents



(b) DC voltage at port 1



(c) DC voltage at port 3

Figure 5.11: Comparison of values with insertion resistors

to the outer AC grid. As a result, in the first case, after the discharge of the capacitors during the connection, the energy needed for the DC link to reach again the nominal value is given by both the DC hub through port 3 and the AC grid connected to the terminal 4. In the other case, as there is no connection to an AC grid, all the energy needs are covered from the DC hub.

5.2. PORT DISCONNECTION

A line can be disconnected for maintenance reasons or after a fault contingency in order to protect the rest of the system. In this section, the case of a normal situation will be studied. Like in the connection, there are also some suggested steps for the disconnection of a port in order to succeed a smoother operation of the system. The suggested steps are:

1. The first step is to control the power exchange of the DC hub with the line to be disconnected to zero. In this way, a smoother transition can be succeeded.

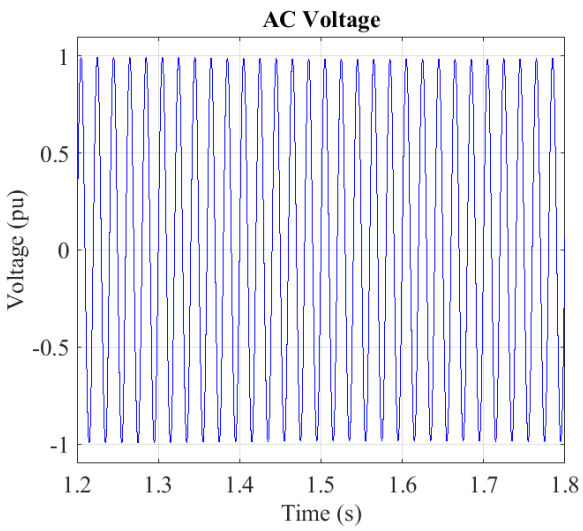
2. Following the AC breakers will open, and disconnect the AC part of the port with the intermediate AC link of the DC Hub.

The ideal case is when the power exchange between the DC Hub and the port to be disconnected equals to zero. However, that will not always be the case, as for example in case of a system malfunctioning or an emergency disconnection, the transferred power can be different from zero at the moment of disconnection.

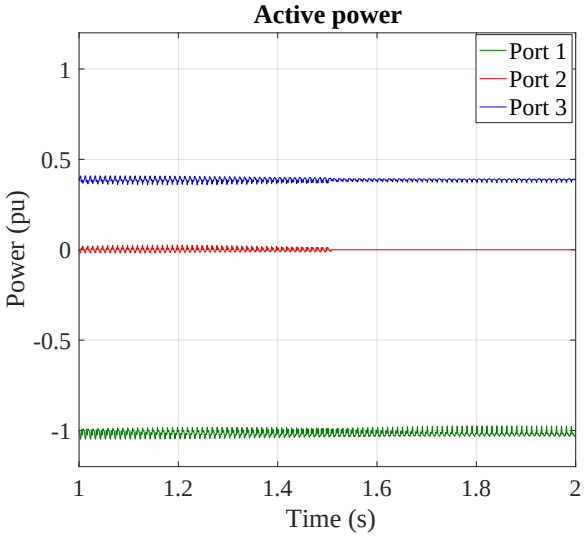
5.2.1. CASE 1 ZERO POWER IN THE DC HUB

PORT OPERATING IN ACTIVE POWER CONTROL MODE

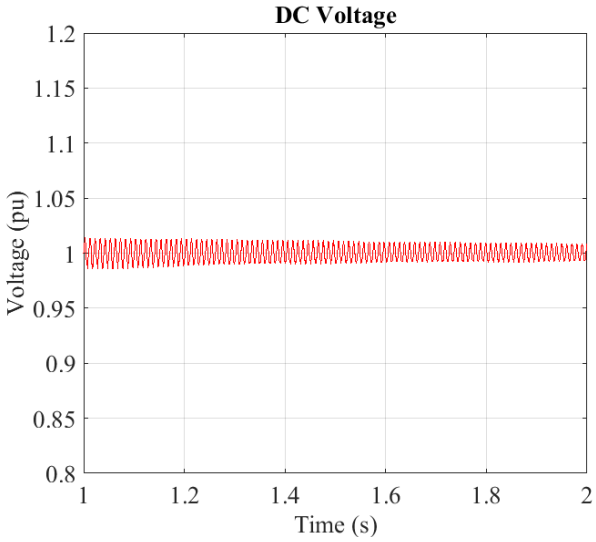
In this first case, Port 2 operating in power control mode is disconnected. The steps for a smooth disconnection are followed. The power transferring between the DC hub and the DC link is zero.



(a) AC voltage



(b) Active power



(c) DC voltage of port 2

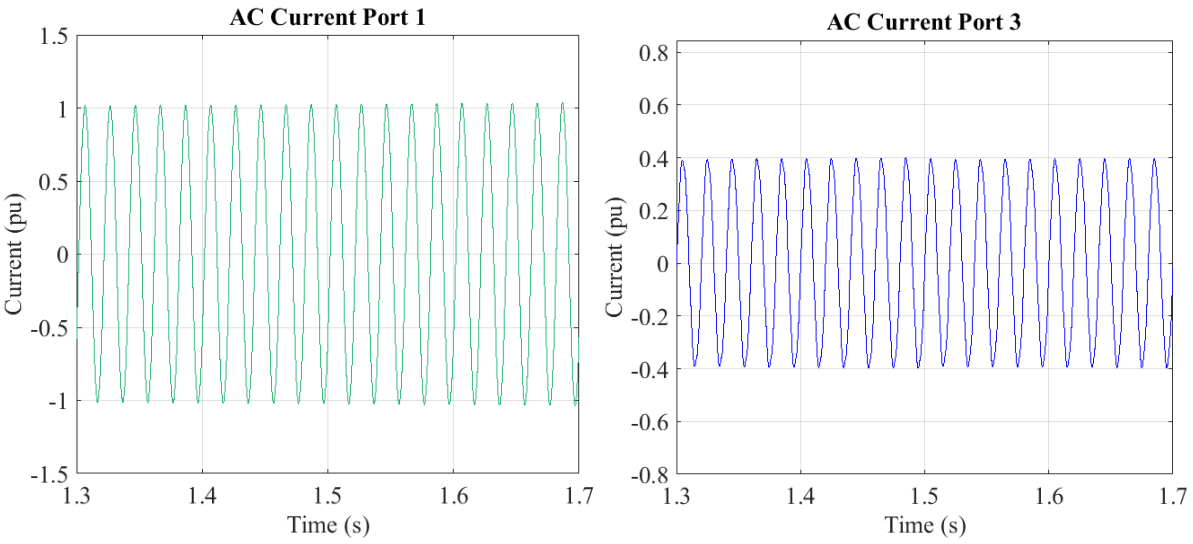
Figure 5.12: Disconnection of port 2 with zero power

It is observed that after the port is disconnected, the DC hub continues its normal operation with the AC voltage of the intermediate AC link shown in figure 5.12a. There are no overvoltages or overcurrents during this disconnection. Moreover, the active power of each port can be seen in figure 5.12b. As mentioned previously there is no current flowing between the DC hub and the port 2, it is observed that the AC currents in the intermediate link and following the arm current in the converters remain stable as shown in figure 5.13.

It is important to notice that the point-to-point transmission line maintains its voltage stable as the terminal responsible for keeping the voltage stable in a reference value is connected to the grid and continues its normal operation as shown in figure 5.12c.

PORT OPERATING IN DC VOLTAGE CONTROL MODE

In this case, Port 1 operating in DC voltage control mode is disconnected. The steps for a smooth disconnection are followed. The power transferring between the DC hub and the port to be disconnected is zero. It is



(a) Port 1

(b) Port 3

Figure 5.13: AC currents of the intermediate link

observed that after the port is disconnected, the DC hub continues its normal operation. There are no overvoltages or overcurrents during this disconnection. It is observed that the AC currents in the intermediate link and following the arm current in the converters remain stable. It is important to notice that the point-to-point transmission line maintains stable. The port 1 is disconnected from the DC hub but it is still connected to the terminal 5 from which absorbs energy in order to maintain the DC link voltage at the reference value.

The same observations are made like the previous case. Consequently, if the steps for smooth disconnection are followed, the control mode of the port does not affect the disconnection.

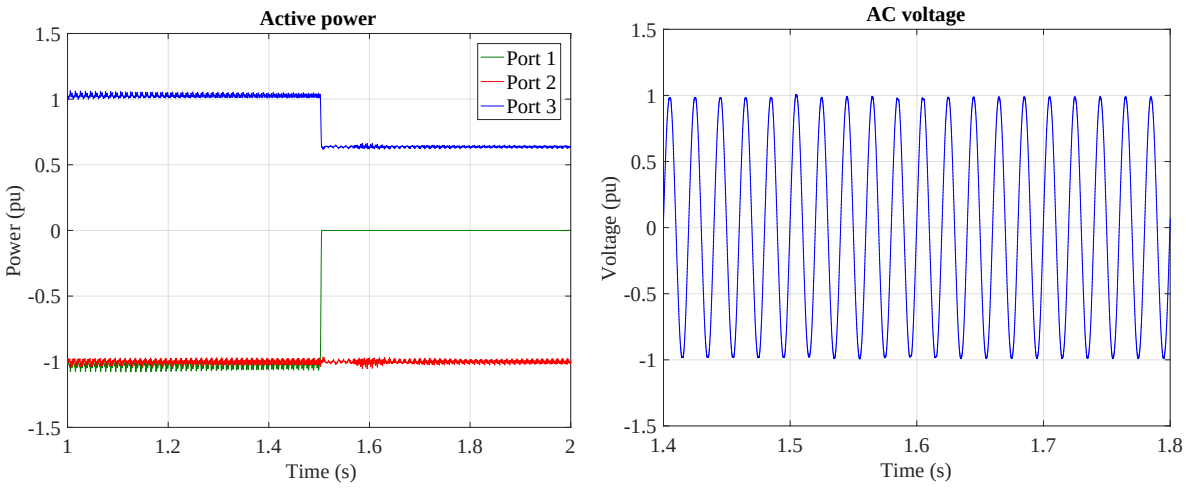
5.2.2. CASE 2 FULL POWER IN THE DC HUB

In this second case, the operation of the system is studied when the steps for smooth operation are not followed. The worst case is examined when all the ports operate in full power. The disconnection of port 1 and 2 are following studied.

PORT OPERATING IN DC VOLTAGE CONTROL MODE

In this case, terminal 5 absorbs 1 pu power from the DC hub through Port 1. At $t = 1.5s$ the port 1 is disconnected. Terminal 5 continuous to ask for power from port 1 and the submodule capacitors will discharge in order to cover its needs. This results in the collapse of the DC link voltage. Detecting this undervoltage, converters on both sides of this DC link will be blocked. In figure 5.14 the active power on each port and the AC voltage of the DC hub is presented. It is observed a jump in the power of port 1, $P_1 = -1 \Rightarrow 0$. Port 3 responsible to cover the power needs also lowers its power while port 2 continues its operation in full power. Observing the AC voltage can be concluded that the AC voltage control is unaffected from the step in power and continues its normal operation.

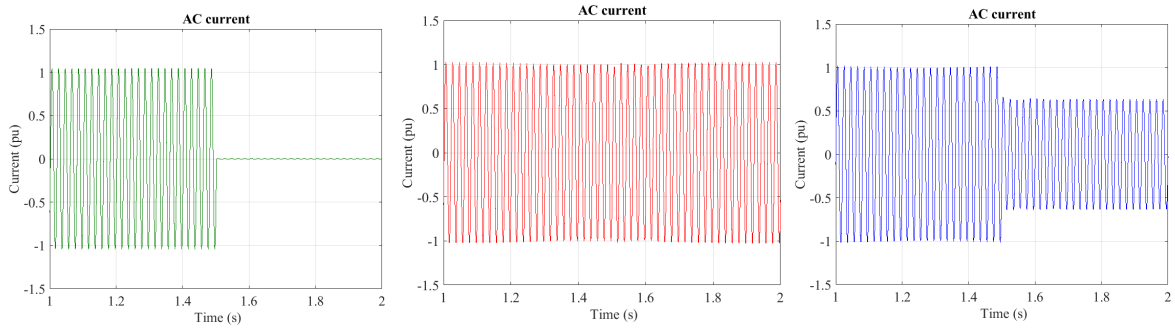
Following the AC currents in the intermediate AC link and the arm currents of each port are presented in figure 5.15 and 5.16. At the time of disconnection, the current of port 1 from the full power value goes to zero. I_{ac3} follows this change while I_{ac2} stays constant. Same transitions are observed in the arm currents. It is interesting to observe the arm current of port 3. After the disconnection, both the AC and DC current of port 3 are now lower. The arm current consists of a DC and AC component. As a result not only the peak of the AC part is lower but also the average value is displaced now closer to zero. The lower values of AC and DC component are a result of the lower value of transferred power.



(a) Active power

(b) AC voltage

Figure 5.14: Values during disconnection of port 1 with full power

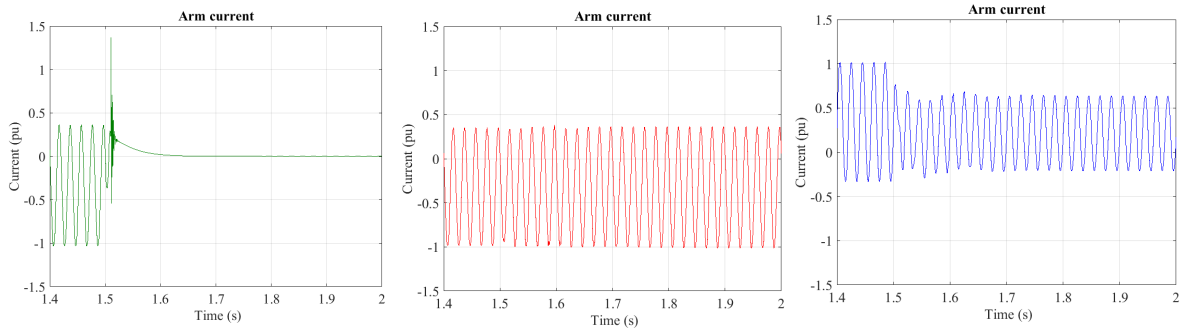


(a) Port 1

(b) Port 2

(c) Port 3

Figure 5.15: AC currents during disconnection of port 1 with full power



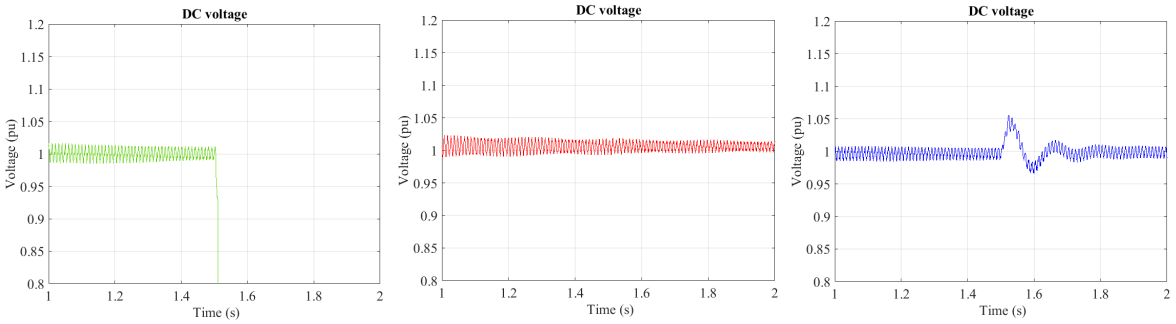
(a) Port 1

(b) Port 2

(c) Port 3

Figure 5.16: Arm currents during disconnection of port 1 with full power

By observing figure 5.17 small oscillations are presented in the DC voltage of port 3. The maximum peak is $0.05pu$ and the duration less than $200ms$. The operability of the system is maintained. Overall, the currents observed in the arms do not take large values after the disconnection and there are no overvoltages or overcurrents observed in the system. The DC hub continues its normal operation after the disconnection of port 1 operating at full power in DC voltage control mode.



(a) Port 1 (b) Port 2 (c) Port 3

Figure 5.17: DC voltages during disconnection of port 1 with full power

PORT OPERATING IN ACTIVE POWER CONTROL MODE

In this case, port 2 operating in active power control mode disconnects at $t = 1.5s$. As port 2 disconnects, the DC current of the point-to-point transmission line from 1 pu jumps to 0 pu as there is no power flowing from the DC hub to terminal 4. The power of port 2 goes to zero while port 3 has a new value covering only the power needs of port 1. The steps in active power of port 2 and 3 are shown in figure 5.18. The power step results in very small oscillation ($\pm 0.03pu$) in the AC voltage. The AC currents of each port can be seen in figure 5.19. The current of port 1 remains stable, while the current of port 3 decreases by the amount of current subtracted by the disconnection of port 2.

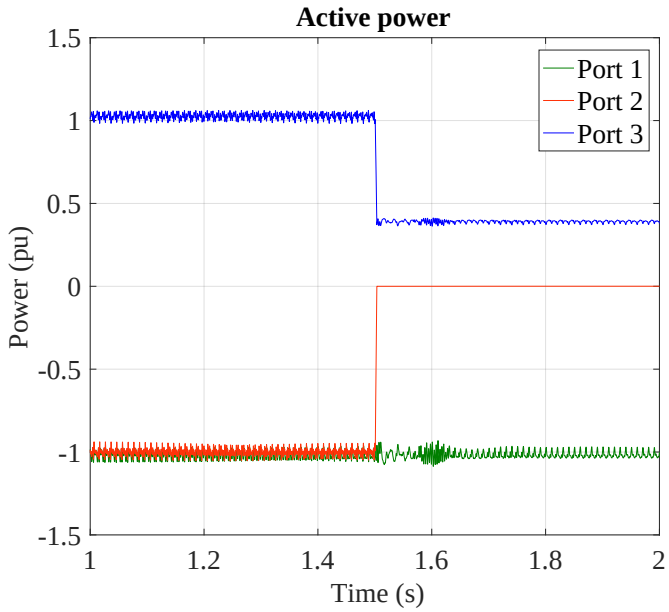
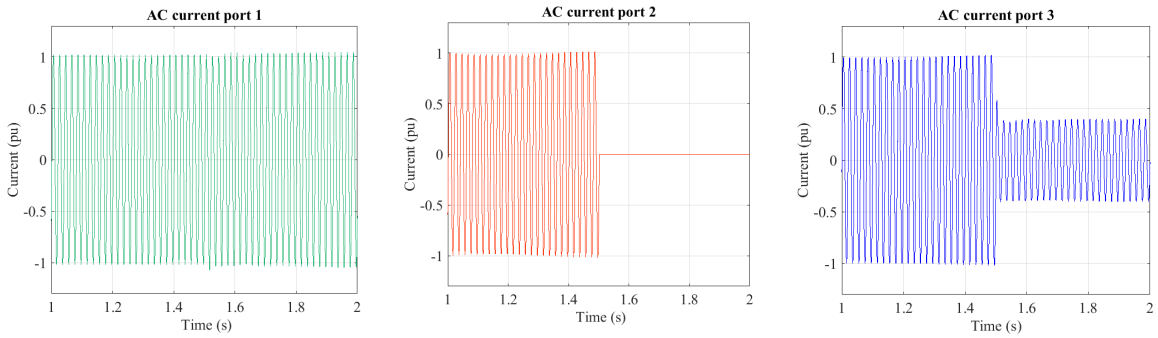
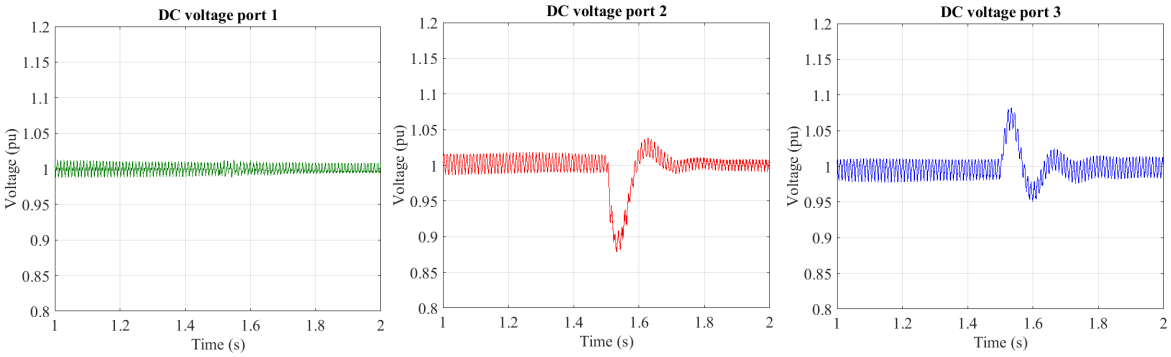


Figure 5.18: Active power



(a) Port 1 (b) Port 2 (c) Port 3

Figure 5.19: AC currents during disconnection of port 2 with full power



(a) Port 1 (b) Port 2 (c) Port 3

Figure 5.20: DC voltages during disconnection of port 2 with full power

Port 1 continues its normal operation without any overvoltages or overcurrents observed as shown in figure 5.20a. The power through p3p6 is not controlled and as a result, this instantaneous power loss will be detected in terminal 6. As a result, there are small transients observed on the DC link voltage lower than $0.1 pu$ as can be seen in figure 5.20c. This transient on DC link voltage affects the AC voltage control of port 3.

5.2.3. DISCONNECTION OF PORT OPERATING IN AC VOLTAGE

The disconnection of the port operating in AC voltage is a special case, for that reason, it is studied separately in this section. It has been observed that the disconnection of a port while following the appropriate steps can take place smoothly without affecting the operation of the rest of the DC hub. In order for the DC hub to continue its normal operation, another port must change its control operation to AC voltage mode.

This port should fulfill the following:

- have the highest power rating
- operate in active power control mode
- be bidirectional
- can cover the power needs of the remaining ports

VAC CHANGE AT ZERO POWER

Following the same rules for choosing the port operating in AC voltage mode, the second in power rating converter is now chosen. Moreover, the port should operate in active power mode. Otherwise, this change in control will lead to losing the DC voltage control in the point-to-point connection. For example in a scheduled maintenance of DC link $P3-P6$, the port 3 is disconnected. In order for the port 3 to operate in zero power, the power on ports 1 and 2 should be zero.

The AC circuit breaker of port 3 opens at $t = 1.5s$. The control mode of port 2 changes from active power to AC voltage control mode instantly at $t = 1.5s$. It is observed in this case that the voltage of the AC link is maintained stable after a voltage drop. In figure 5.21 the AC voltage of the intermediate link is presented.

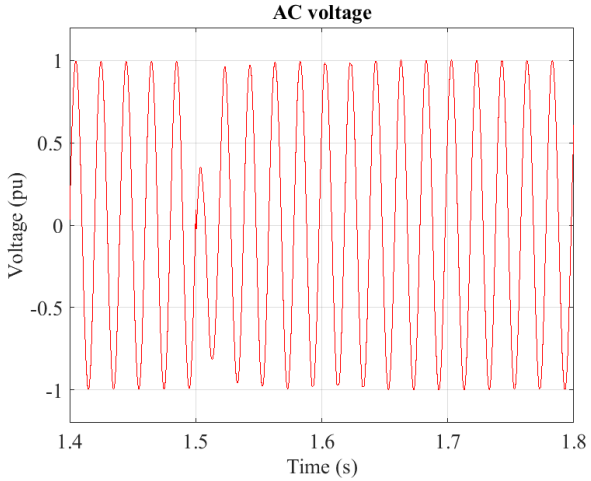


Figure 5.21: AC voltage during port 3 disconnection

The DC voltage at port 2 also decrease. The submodule capacitors in the arms of each phase discharge. This discharge current flows through the arms of port 2 and via the AC link reaches port 1. As a result higher currents are observed throughout the DC hub. However,the arm overcurrents observed in figure 5.22 stay between the predefined values. Next, the submodule capacitors of port 1 are charged from this inrush current and the DC link voltage of port 1 increase. Following, port 1 operating in DC voltage control mode restores the DC voltage to its reference value. In order to achieve that, the capacitors discharge and the discharge current is absorbed from the port 2 operating now in AC voltage control. After some small oscillations the DC voltage of both the transmission lines $p1p5, p2p4$ return to its nominal value. Notice that the discussed voltage ripples are bellow 0.05 pu as seen in figures 5.23d and 5.23b. Also the peak ripple in DC currents is kept bellow 0.5 pu as seen in figures 5.23c and 5.23a. Moreover, a current is observed from terminal 4 to terminal 2 in order to return the DC link to its reference value. After a small oscillation, the DC voltage stabilizes. Port 1 continues its normal operation, maintaining the DC link voltage stable at the reference value after a small transient with duration of $200ms$.

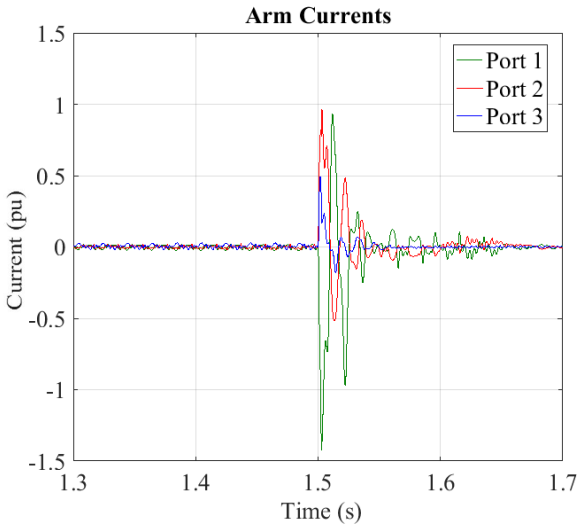
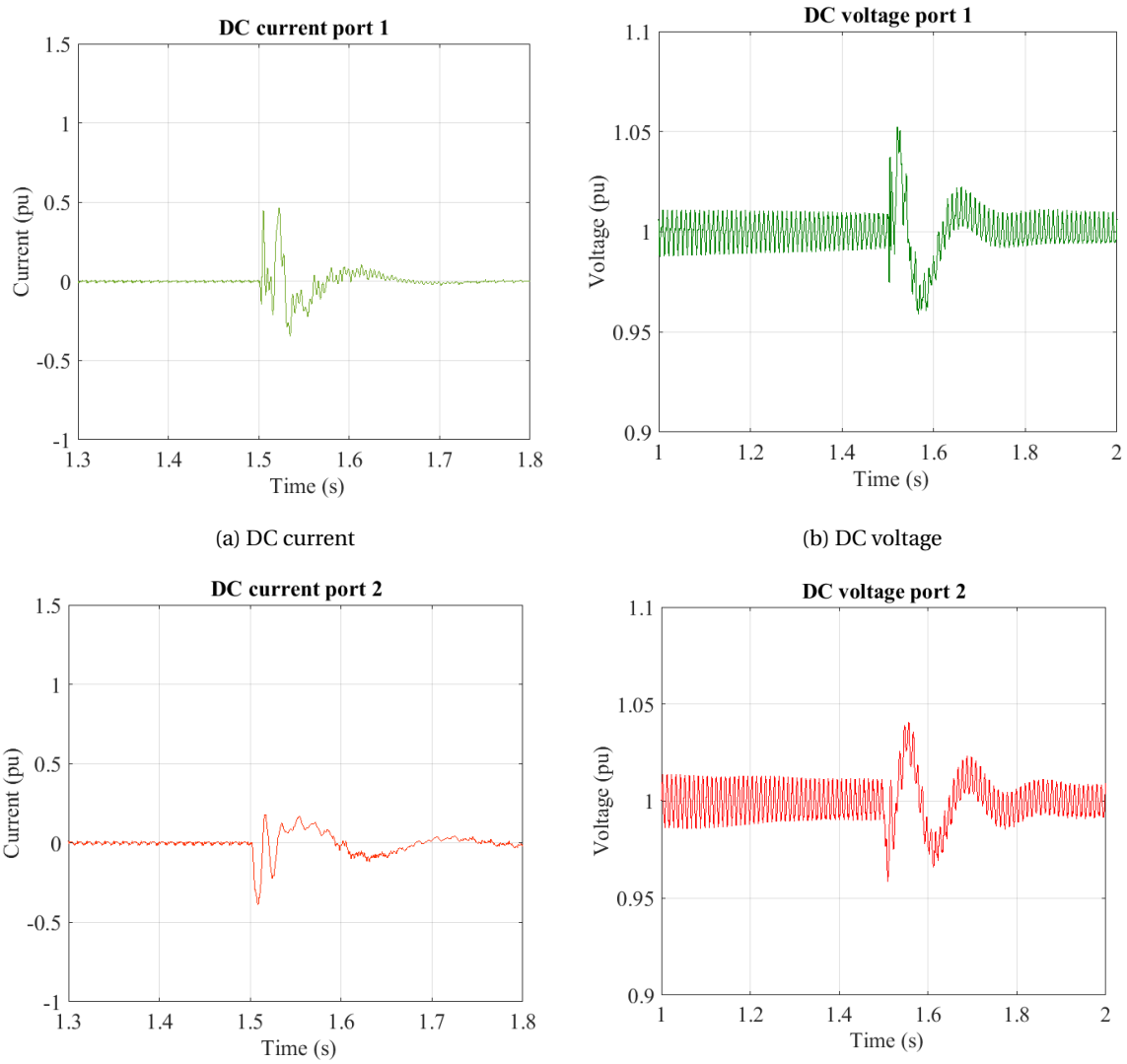


Figure 5.22: Disconnection of port 3 and AC voltage control change

VAC CHANGE AT FULL POWER

In case of an emergency or system malfunction, it is possible to open the AC circuit breakers of port 3 and change the control of port 2 while there is power flowing through the hub. Following, the worst case where



(a) DC current

(b) DC voltage

(c) DC current

(d) DC voltage

Figure 5.23: DC values of port 1 and 2

all ports operate in 1 pu active power is studied. At $t = 1.5s$ the AC CB of port 3 opens and the control mode of port 2 changes to AC voltage mode. The active power of port 3 jumps to zero and port 2 will now be responsible to cover the power needs of port 1. The full power reversal change is shown in figure 5.24. Port 2 now changes its mode operating in voltage mode, resulting in not having control of the line currents as previously. Moreover, it is observed that the undervoltage of the transmission line p2p4 has a longer duration around 80 ms and is kept above 0.77pu. The DC current peaks do not pass the 1.5 pu as seen in figure 5.25c. Figure 5.26 presents the AC and arm currents of ports 1,2. The larger discharge of the submodule capacitors results in larger current peaks for the arm currents of port 2, the intermediate AC currents and finally for the arm currents of port 1. The DC current starts oscillating at the time of the disconnection and after a period of 100ms returns to the reference value. It is observed that the peaks obtain values larger than 2 pu but for a very small period of time as shown in figure 5.25a. This is not expected to affect the insulation of the DC cable.

Overall, in this case, larger currents are observed in the DC hub components. It is important to notice that due to the large arm currents, the fault detection system will be enabled. This peak in the arm currents can be limited by increasing either the arm inductance or adding a phase reactor. Else, the submodules can be dimensioned for higher currents by adding more semiconductor switches in parallel.

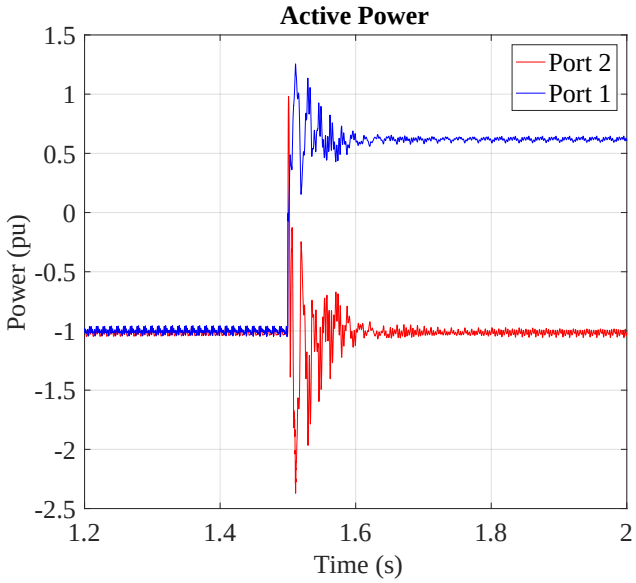
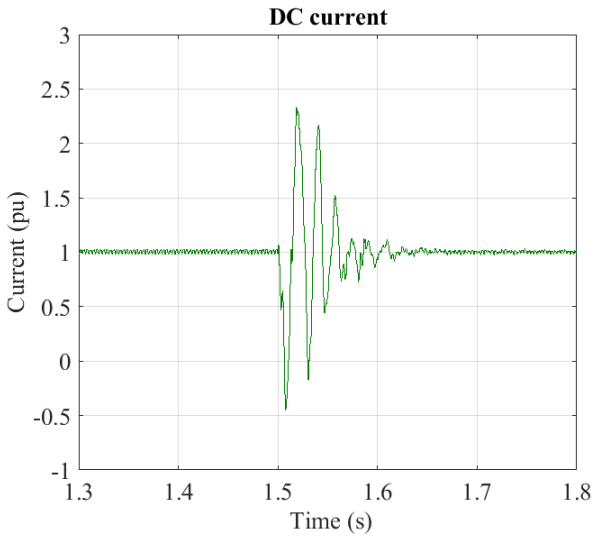
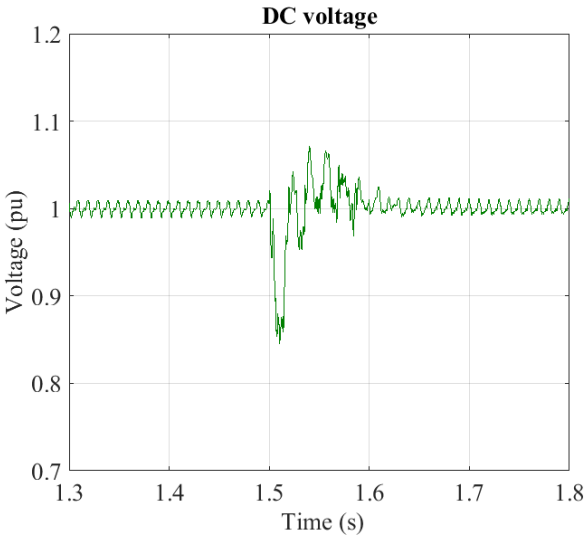


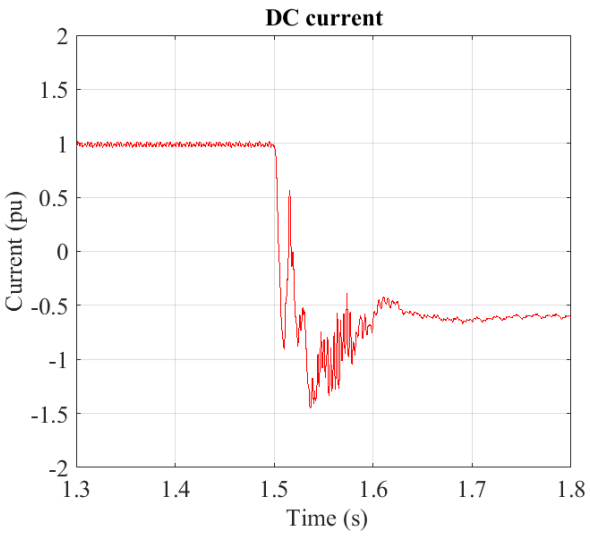
Figure 5.24: Active power during port 3 disconnection



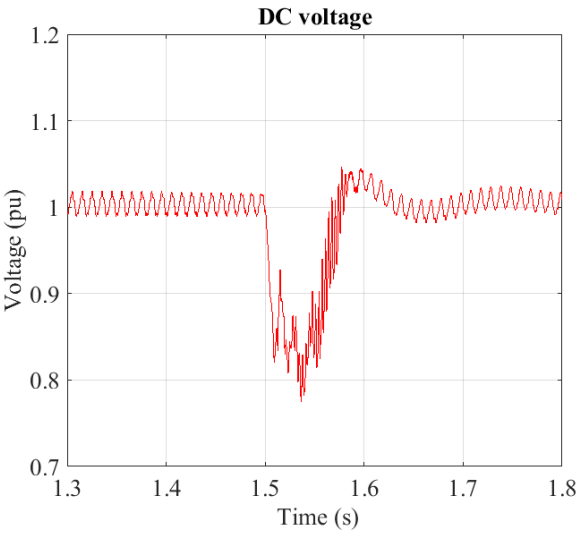
(a) DC current port 1



(b) DC voltage port 1

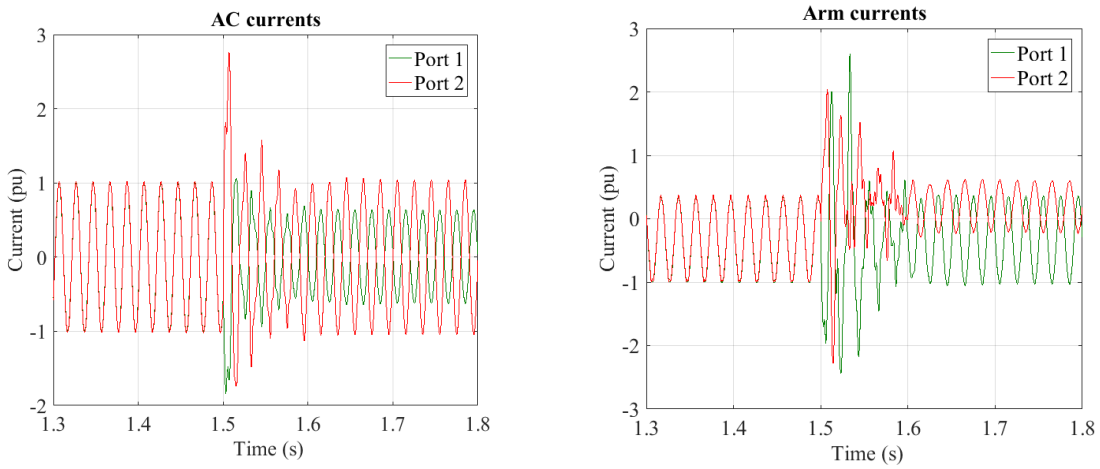


(c) DC current port 2



(d) DC voltage port 2

Figure 5.25: DC values of port 1 and 2



(a) AC currents

(b) Arm currents

Figure 5.26: Current values at full power change

COMPARISON

Following, simulations were executed for the port 3 disconnection case where port 2 operates in full power and port 1 operates in $P_1 = 0.1-1pu$. In this way a better understanding of the system response after changing the port operating in AC voltage control can be achieved. From the following figures 5.27, 5.28 and 5.29 useful conclusions can be made. It is observed that when port 2 is operating at full power, the higher the power of port 1, meaning the bigger the power reversal, results in higher peaks for the DC current of port 2. Moreover, it results to lower DC voltages for port 2 for longer time periods. For the DC current of port 1, it is observed that the higher the power of port 1, the larger are the observed oscillations resulting in larger peaks before the I_{dc1} returns to its nominal value.

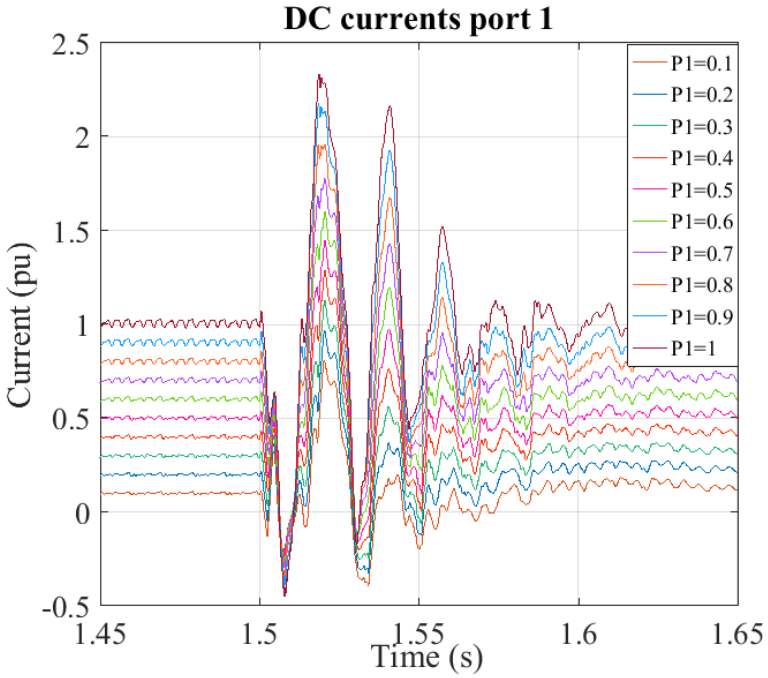


Figure 5.27: DC currents of port 1 for different power levels of port 1

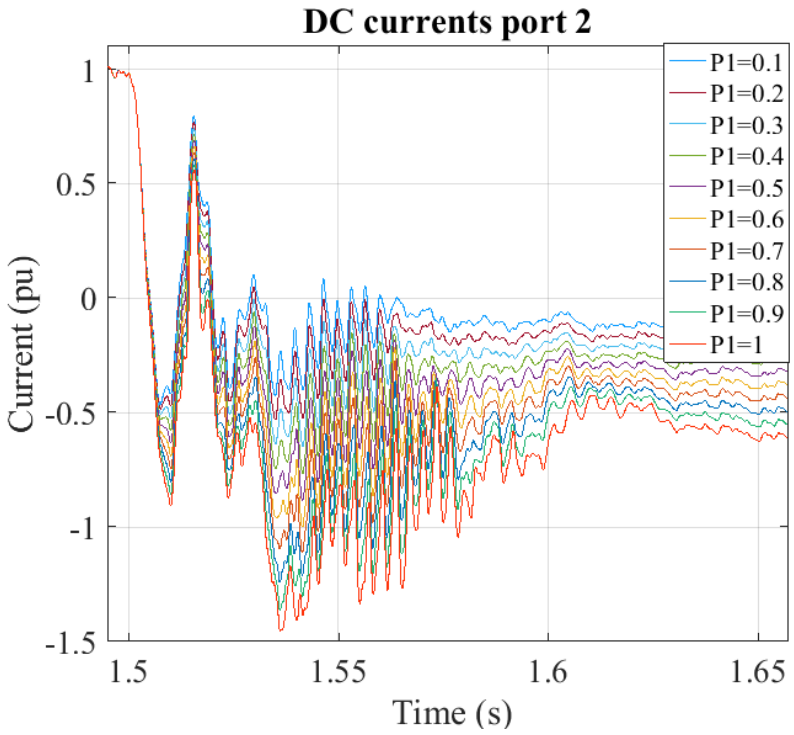


Figure 5.28: DC currents of port 2 for different power levels of port 1

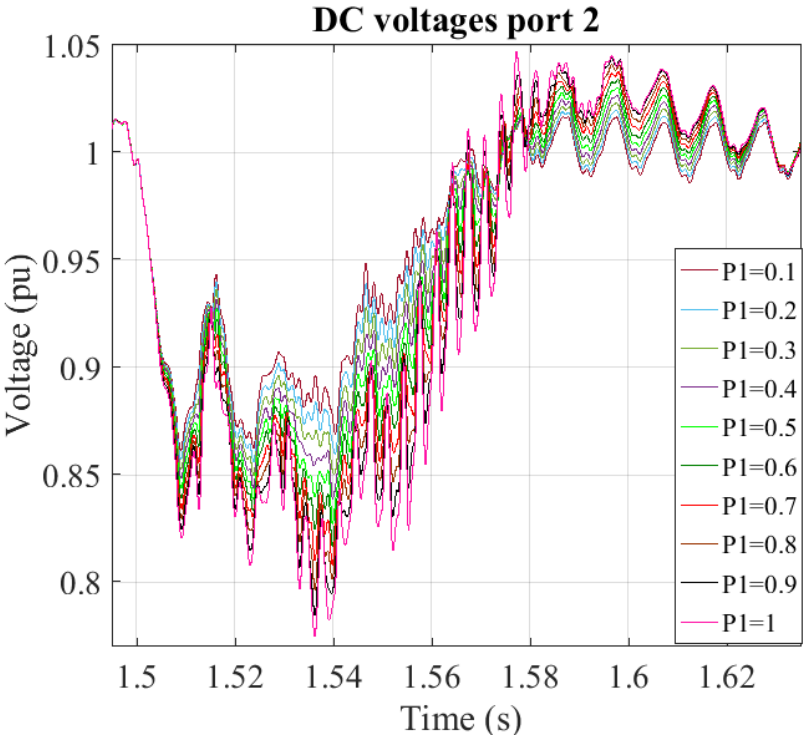


Figure 5.29: DC voltages of port 2 for different power levels of port 1

5.3. CONCLUSIONS

Concluding, the cases of a line connection/disconnection were studied under zero and full power condition. The results provide important insights into the DC hub response. The two different cases of connecting a port operating in DC voltage control mode and active power control mode were studied. In both cases, inrush currents were observed due to the submodule capacitors discharge. However, it has been shown that using insertion resistors can limit this current and lead to a smooth connection. It is proposed to use insertion resistors for the first 0.5-1s after the connection in order to achieve a smoother transition. Overall, the system continues its normal operation without any large currents or voltages observed.

The port disconnection was next studied more in depth. For all the ports two cases, one in zero power and one in full power were presented. The results indicate that when the suggested steps for a line disconnection are followed, an excellent transition is achieved. However, in some cases, a port can be disconnected while operating at full power. The worst case of all the ports operating at full power was next studied. The results show that the DC hub continues its normal operation after this case.

The case of port operating in AC voltage disconnection was separately examined. In this special case, in order for the rest of the system to continue its operation, a different port must change its control mode and operate in AC voltage control mode. The new port is chosen according to some suggested criteria. From the results, it was observed the successful disconnection of port 3 when zero power transfers through the DC hub. Following, the full power case is studied. It is observed that the new AC voltage port perform a power reversal in order to cover the needs of the third port. In this case harsher transients were observed, however, the system maintains its controllability.

The results for the different levels of power reversal provided useful insights. The values of the DC link were observed and it was concluded that the bigger the power reversal, the larger the DC current peaks. For port 1, the higher DC current peak observed has a value of $2.4pu$ and a duration of $5ms$. In port 2 the highest peak observed is less than $1.5pu$. However, the peaks duration is small and it is not expected to affect the insulation of the cable. In port 2 the DC voltage has a lower value of $0.77pu$ for only $5ms$. The undervoltages effect on the fault detection system is project specific. In the above cases, the protection system is unabled in order to study the peaks of the different values during the transients.

In summary, the results in this Chapter 5 and the previous Chapter 4 indicate that the main attributes of a DC-DC multiport converter were successfully achieved. In the next chapter, the natural fault response of the DC hub is presented and the fault ride-through capability is studied.

6

DC FAULTS

In this chapter, the different faults in a DC line are studied. First, the protection system used on the DC side and the fault cause and probability are presented. Following, the natural fault response and the equivalent circuit during fault occasion is studied. Finally, the steps taken in order to block the fault are presented.

6.1. INTRODUCTION

The faults are simulated by using a single phase breaker from the library of $SimPowerSystems^{TM}$. In the case of a pole-to-ground fault, the breaker is used to connect one of the poles to the ground while in the pole-to-pole fault it is used to connect the two poles together.

The fault resistance is an important value that can change the transient response during a fault. In the pole-to-pole fault, the fault resistance is very small and for the simulation purposes, an $R_{fault} = 0.01\Omega$ is chosen. In the case of pole-to-ground fault, based on literature [48, 49] a fault resistance $R_{fault} = 7\Omega$ is chosen. This value corresponds to the ground resistance of a sparking ground connection in wet loamy sand.

The DC hub under study is again presented in figure 6.1. AC circuit breakers are used in order to isolate the DC faults. The power rating, the DC voltage values, and the control mode operation are presented in table 6.1.

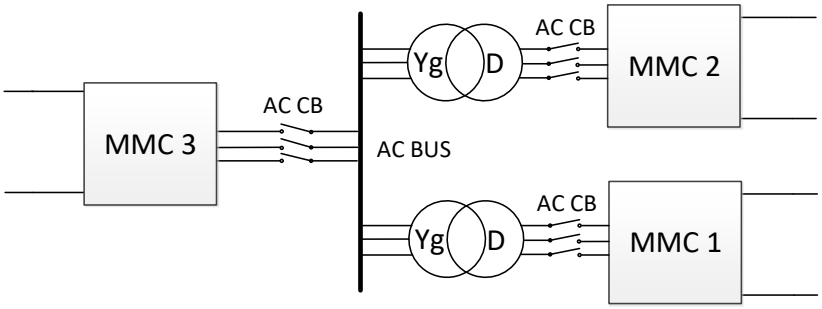


Figure 6.1: DC hub in case of DC faults

Table 6.1: Port values and control modes

Ports	Port 1	Port 2	Port3
Power	$300MW$	$500MW$	$800MW$
DC Voltage	$\pm 150kV$	$\pm 250kV$	± 320 kV
Control Mode	V_{DC}	P	V_{AC}

6.2. PROTECTION SYSTEM

The main objective of a protection system is to isolate the faulted subsystem or component in order to protect the rest of the system. In this section, the main protections of the DC side are presented. Namely: DC undervoltage, DC overvoltage, DC unbalance protection, DC overcurrent protection, DC differential protection. Also, the submodules on the arms should be protected [31].

DC undervoltage, overvoltage The DC voltage is monitored in the DC terminal. In case of a dc-bus voltage being measured below or above a threshold for a predefined time period then a signal is sent to block the converter.

DC differential voltage protection In this DC bus differential protection, the positive- and negative-pole voltages are monitored. A resistive voltage divider is used to measure the pole-to-ground voltage. When the difference between the two voltages is greater than a threshold level for a predefined time period, then the converter is blocked.

DC overcurrent protection The objective of this protection is to detect overcurrent and protect the converter components.If the current is greater than a threshold level for a predefined time period, then the converter is blocked.

DC differential protection In a transmission line, the currents entering and leaving the DC bus are measured. Following, these currents are compared keeping in mind the possible deviations in time due to communication delays between the two ends. A large deviation between the currents indicates a ground fault and the converter must be blocked.

Submodule protection The valve protection system can consist of overcurrent, overvoltage and undervoltage protection. Also, a thermal overload protection avoids overheating the valves. In case of an unnatural condition, a signal is sent to block the submodules and remove them from the circuit. Most commonly IGBT valves are used as the submodule switches. In order to select an appropriate threshold, both literature and industrial catalogs were used[50, 51]. Namely, the chosen threshold is $2pu$, when this value is surpassed, the IGBTs should be blocked.

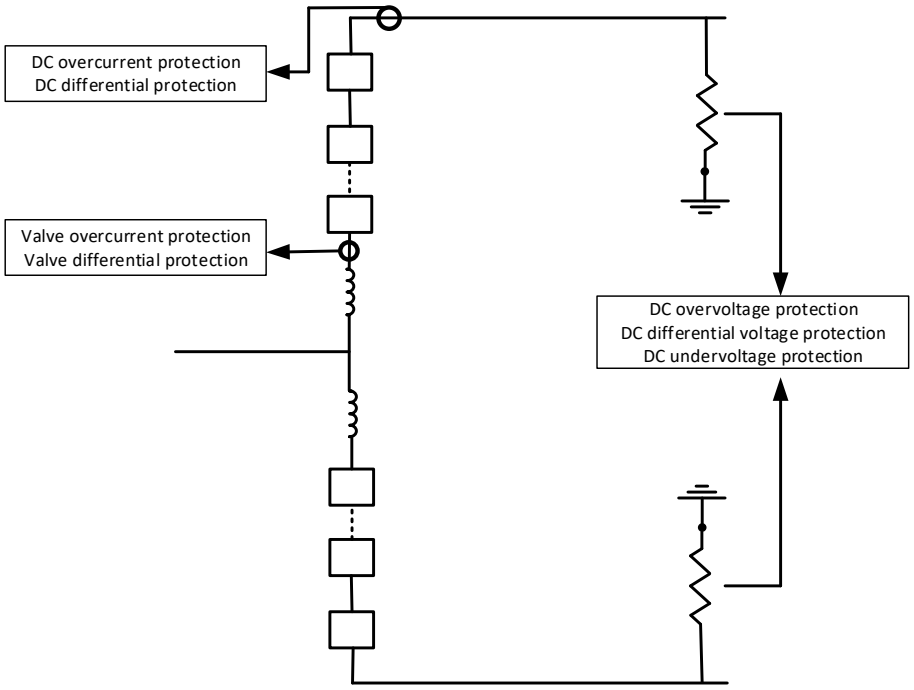


Figure 6.2: Protection system

In the current chapter, the thresholds used are presented in the table 6.2. The thresholds of the protective functions mentioned above are project-specific. They have to be defined based on the network characteristics and the ratings of the grid assets. As far as it concerns the submodule overcurrent the threshold of $2pu$ is chosen. However, the submodule overcurrent detection was unabled, because the arm current peaks are observed in order to achieve a proper dimensioning.

Table 6.2: Protection threshold values

Protection Function	Threshold (pu)
Pole overcurrent	2
Pole undervoltage	0.8
Pole overvoltage	1.2

6.3. DC FAULTS CAUSES AND PROBABILITY

In an HVDC transmission system, overhead transmission lines or cables (underground or submarine) can be used. Each of these transmission methods has its own advantages and disadvantages. Also, the fault causes and the fault probability are different.

In overhead lines, a line to ground faults takes place when one of the positive or negative lines is shorted to the ground. The most common cause is when a lightning strikes the line. This may result in breaking the line and short-circuiting it with the ground. In this case, the fault is permanent. Following, the fault must be located and the line must be isolated for repair. Another cause of a line to ground fault is an object falling on the line. In this case, either the line breaks leading in a permanent fault or the object can short-circuit the line with the ground. In this case, the system can be restored. The line to ground fault probability in overhead lines is reported to be $0.4 faults/100km/year$ where only 10% is permanent. This is described as high fault probability. The reasons for a line to line fault is again an object falling and short-circuiting the positive and negative line. In this case, the fault may be either permanent or temporary. By assuming again a 10% permanent to temporary fault rate, the probability of an overhead line to line fault is $0.03 faults/100km/year$. This probability can be classified as very low and this rate is 10 times smaller than the line to ground fault probability [52].

In cables, a pole-to-ground fault can be caused by breaking the cable insulation. This can be caused by improper installation, cable aging, very high voltages/currents and exposure to the environment [53]. The main threats to an underground cable are excavators and drilling, while for the submarine cables are anchoring, fishing activities and ocean dumping of dredged material. In comparison with the overhead lines, the cables can be protected better leading to lower fault probabilities. A research around the Norwegian coast shown a rate of $(2-5)\cdot 10^{-4} faults/100km/year$ for submarine cable faults due to anchoring. In the case of a pole-to-pole fault, the cables are separated by insulation, conduit and the soil resulting in a very low, almost zero probability. [54, 55]

6.4. POLE-TO-GROUND FAULT

In the current thesis, the symmetric monopole configuration for MMC-HVDC schemes is studied. In case of a pole-to-ground short-circuit fault, a fault ride-through capability is observed. In [56] the fault ride-through capability of a point-to-point transmission line is studied. It is shown that after the pole-to-ground fault, the voltage of the faulty pole decreases. This lower level depends on the fault resistance. On the other hand, the healthy pole increases its voltage. The increase can be up to two times the value of the pre-fault voltage. As a result a voltage displacement is observed between the poles, however, the pole-to-pole voltage remains constant.

As it can be seen in the figure 6.3, in the 2-level VSC-HVDC the neutral of the DC-link capacitors is grounded. In case of a pole-to-ground short-circuit, there is a large discharge current flow through the grounding loop due to the DC-link capacitors' discharge. In contrast, in the MMC-HVDC the potential reference on the DC side is given by two large clamped resistances as shown in figure 6.4. After the fault, the theoretical potential reference will change from point 1 to point 2. In this case, there is no charging path to the ground in order to discharge the capacitors. The DC cable should be designed having the necessary maximum insulation in order to sustain the temporary overvoltage. By clearing this fault as fast as possible, the overvoltage stress on the healthy pole is minimized.

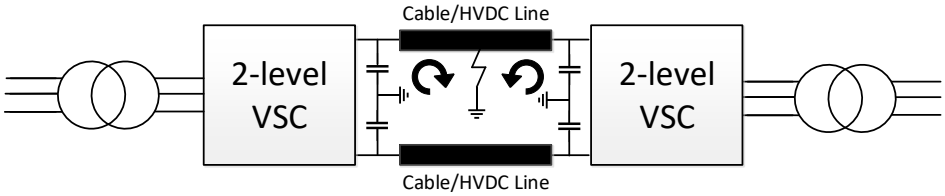


Figure 6.3: Pole-to-ground fault with two-level VSC

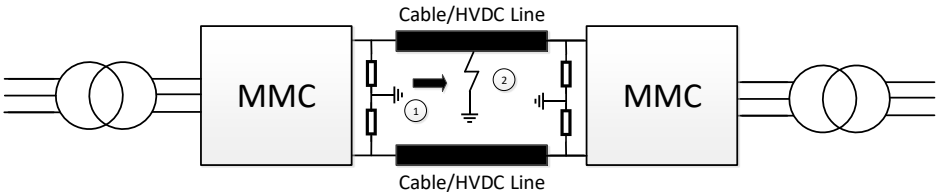


Figure 6.4: Pole-to-ground fault with MMC

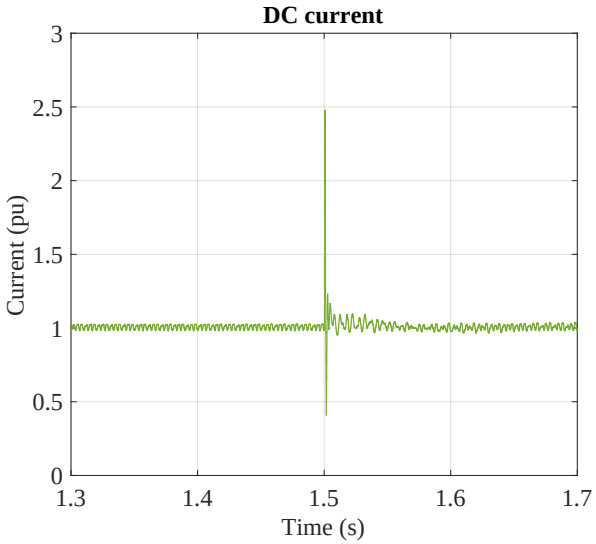
6.4.1. POLE-TO-GROUND FAULT AT PORT 1

In this section, the case where a pole-to-ground fault occurs at port 1 operating on DC voltage control is studied. At the moment of the fault $t = 1.5s$ there is observed an inrush current to the ground. This fault current is shown in figure 6.5a reaches a large peak value but for a very small period of time (2ms). The protection system will not be enabled by this change and the converters continue their normal operation. There is no overcurrent observed in the arm of the faulty port as seen in figure 6.5b. Also, there are no fault currents observed entering the intermediate AC link of the DC hub. Moreover, it is observed that the voltage of the faulty pole jumps to zero. The voltage of the healthy pole has a new value. This value is equal to two-times the pre-fault value. The pole-to-pole, positive and negative pole voltage of the faulty port 1 can be seen in figure 6.5c. The following equation stands for the DC pole-to-pole voltage:

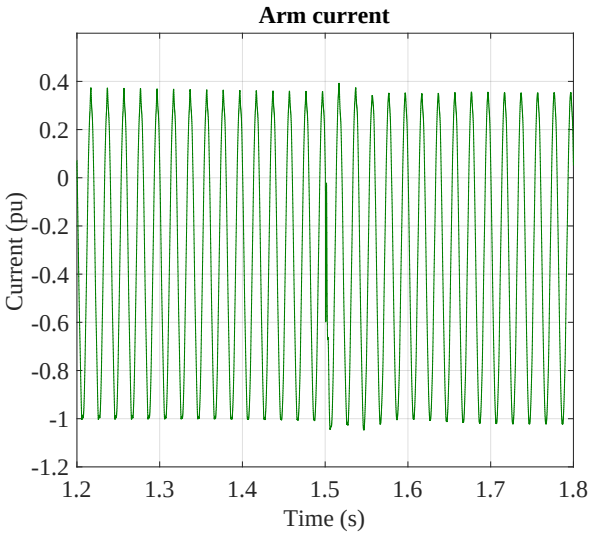
$$V_{dc} = V_p - V_n \tag{6.1}$$

where, V_{dc} is the pole-to-pole DC voltage, V_p is the positive pole DC voltage, V_n is the negative pole DC voltage.

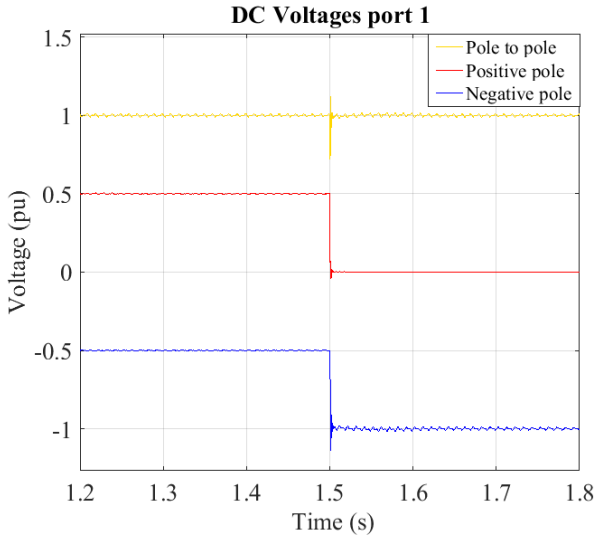
As a result, the pole-to-pole voltage remains constant but there is a displacement in the pole voltages. This voltage mutation is following seen in the phase voltage measured between the converter and the transformer. The phase-to-phase voltage remains the same as the two DC components cancel each other. These observations can be seen in figure 6.6. The transformer before the intermediate AC link does not allow for the DC component to pass. As a result, the phase voltage seen in the intermediate AC link remains the same.



(a) DC current of port 1



(b) Arm current of port 1



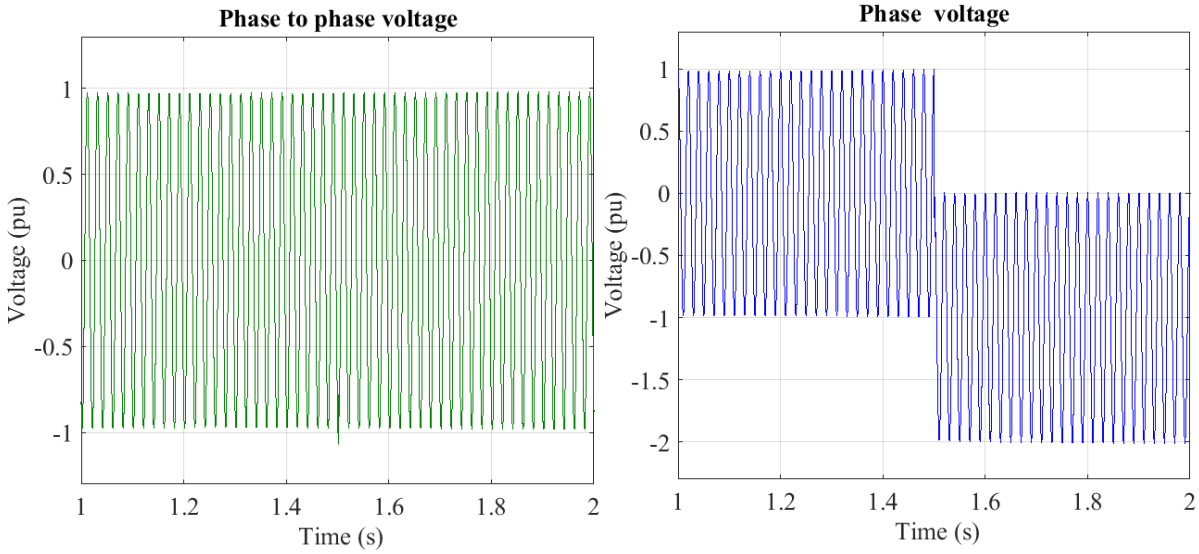
(c) Pole-to-pole, positive and negative pole voltage

Figure 6.5: Values during a pole-to-ground fault on port 1

Fault location Another parameter that affects the fault response is the location of the fault. Two different case seen in table 6.3. One fault was performed on the terminal next to the DC hub while the second one is performed closer to the other terminal of the point-to-point connection. The results show that the closer the fault to the hub the larger the DC voltage and DC current peaks, measured at port 1.

Table 6.3: Fault location

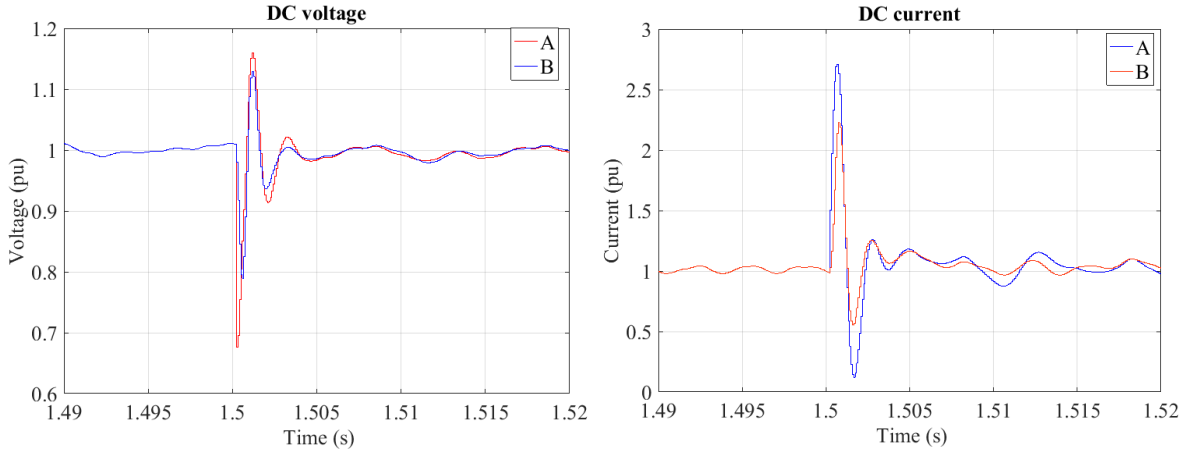
Case	Location
A	fault at terminal 1
B	fault at terminal 5



(a) Phase-to-phase voltage

(b) Phase voltage

Figure 6.6: AC voltages at the faulty port

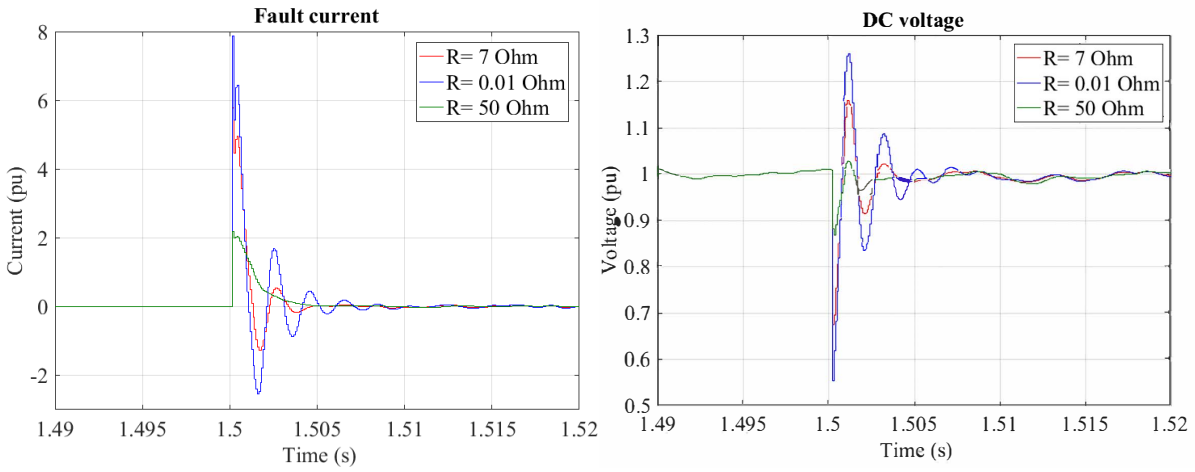


(a) Phase-to-phase voltage

(b) Phase voltage

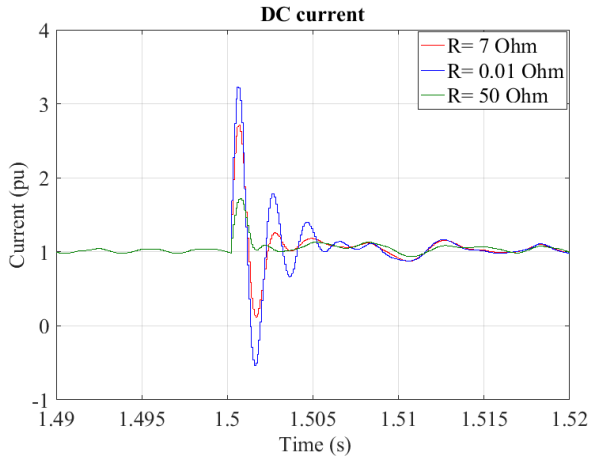
Figure 6.7: Comparison for different fault locations

Fault resistance The fault resistance is an important parameter that affects the peak and the damping rate of the fault current. In figure 6.8 the fault responses for different values of fault resistances can be seen. It is observed that the larger the resistance the lower the peak for the values of fault current, DC voltage and DC current of the faulty port.



(a) Fault current

(b) DC voltage



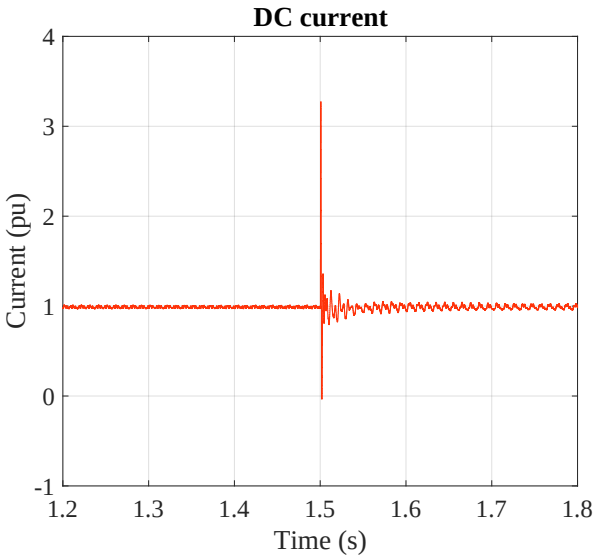
(c) DC current

Figure 6.8: Comparison for different fault resistances

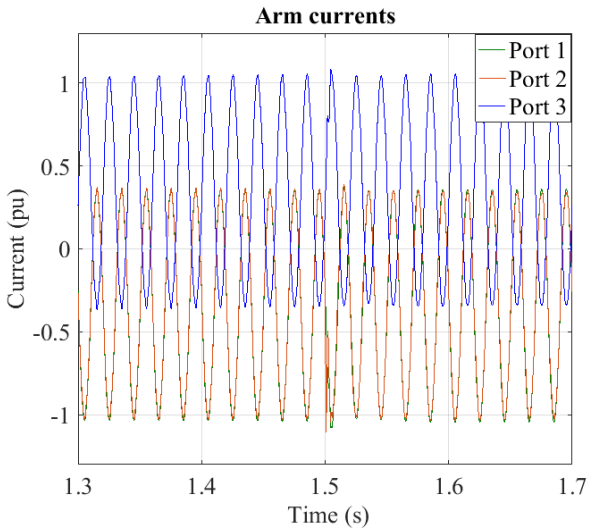
6.4.2. POLE-TO-GROUND FAULT AT PORT 2

Following, the case where a pole-to-ground short-circuit occurs at $t = 1.5s$ at port 2 operating on active power control is studied. At the moment of the fault, there is observed an inrush current to the ground similar to the previous case. The effect of the fault current can be seen in figure 6.9a. As in the previous case, the time period of the current peak is very small (2ms). However, the peak value is higher than 3 pu, larger than before. This can be explained by the fact that the power and DC voltage of port 2 are higher than port 1. The instantaneous (DC cable discharge) loss of DC current will lead to a small discharge of the submodule capacitors. As can be seen from the fig 6.10 the voltage decrease for less than $0.05pu$ but returns quickly to its nominal value.

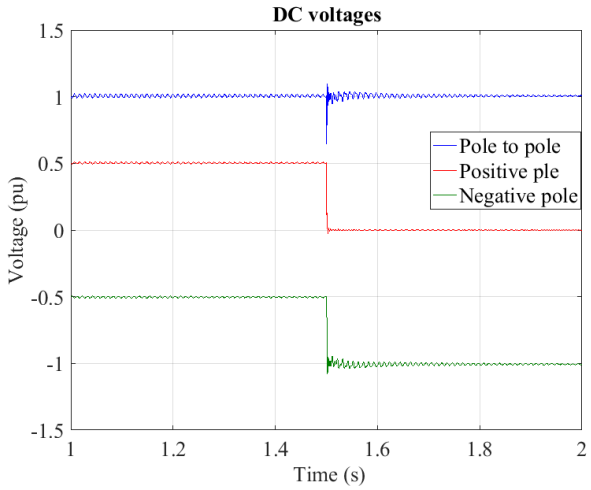
By observing the DC hub system, there are no high current or voltages observed and the system continues its normal operation. There is no overcurrent observed in the arms of the three ports as seen in figure 6.9b. Moreover, the same observations for the DC voltage are done as in the previous case. The voltage of the faulty pole jumps to zero while the voltage of the healthy pole has a new value equal to two times the pre-fault value. The pole-to-pole voltage remains stable as shown in figure 6.9c. This voltage mutation is following seen in the phase voltage on the AC part of the faulty port as presented in figure 6.9d.



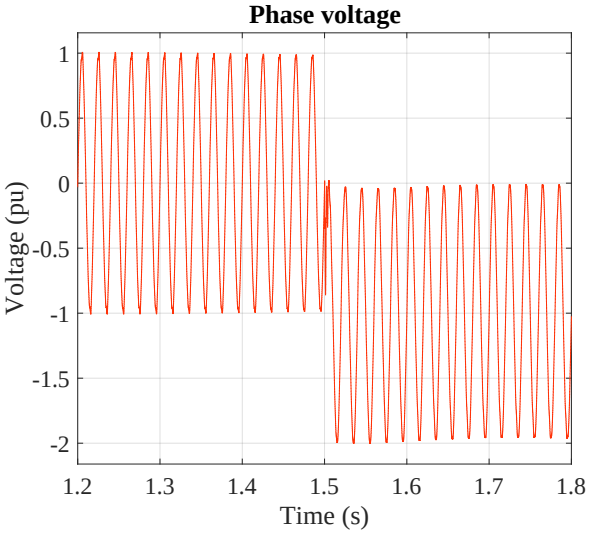
(a) DC current



(b) Arm currents port 2



(c) DC voltages



(d) Phase-to-phase

Figure 6.9: Pole-to-ground fault at port 2

6.4.3. POLE-TO-GROUND FAULT AT PORT 3

Finally, the case where a pole-to-ground short circuit occurs at $t = 1.5s$ at port 3 operating on AC voltage control is studied. In the first design of the DC hub, transformers were used only in the ports 1 and 2 in order to match the different voltage levels in the AC intermediate link. Simulating pole-to-ground fault at port 3 leads to instabilities and to the collapse of the DC hub. The different configurations of a three-phase transformer were tested in order to study the capability of aiding in the fault ride-through capability. The table 6.4 summarizes the results.

Table 6.4: Transformer configurations and fault ride-through capability

Configurations	FRT achieved
No transformer	NO
D-Yg	YES
Yg-Yg	NO
Y-Yg	YES

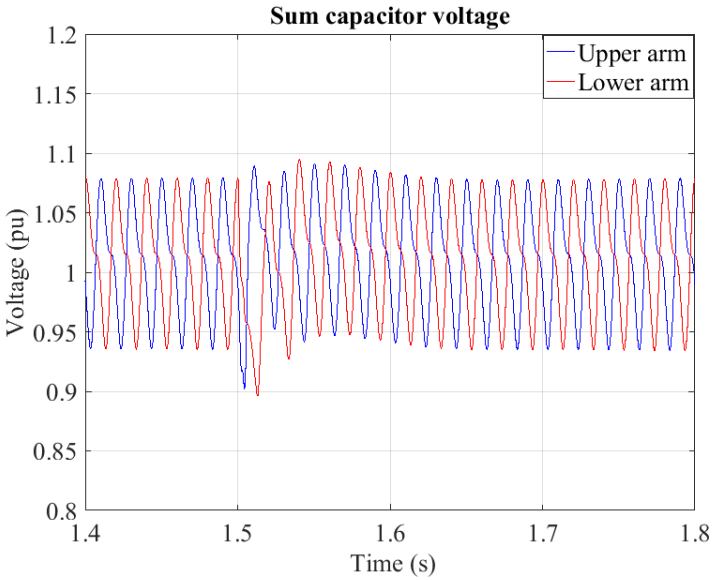
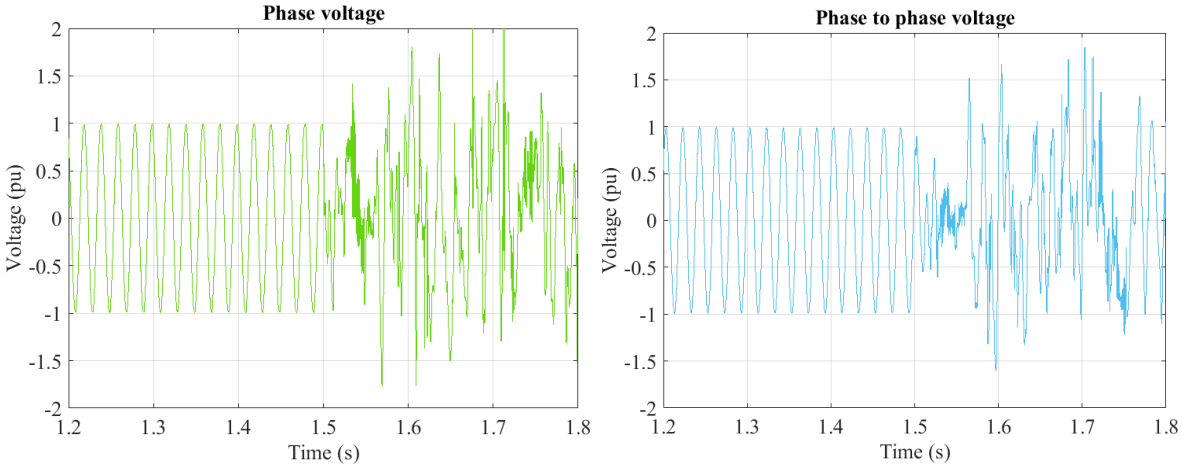


Figure 6.10: Sum capacitor voltages at port 2

From the results, it is observed that when the AC side of the faulty converter "sees" a grounding, the system is driven to instabilities after the fault occurrence and the collapse of the DC link voltage of the faulty port. This can be explained by the fact that in the presence of a grounding, the mutated voltage is driven to oscillate around the zero not being able to maintain a DC component. In figure 6.11 the phase voltage and phase-to-phase voltage are presented.



(a) Phase voltage

(b) Phase-to-phase voltage

Figure 6.11: AC voltages at the faulty port 3 without transformer

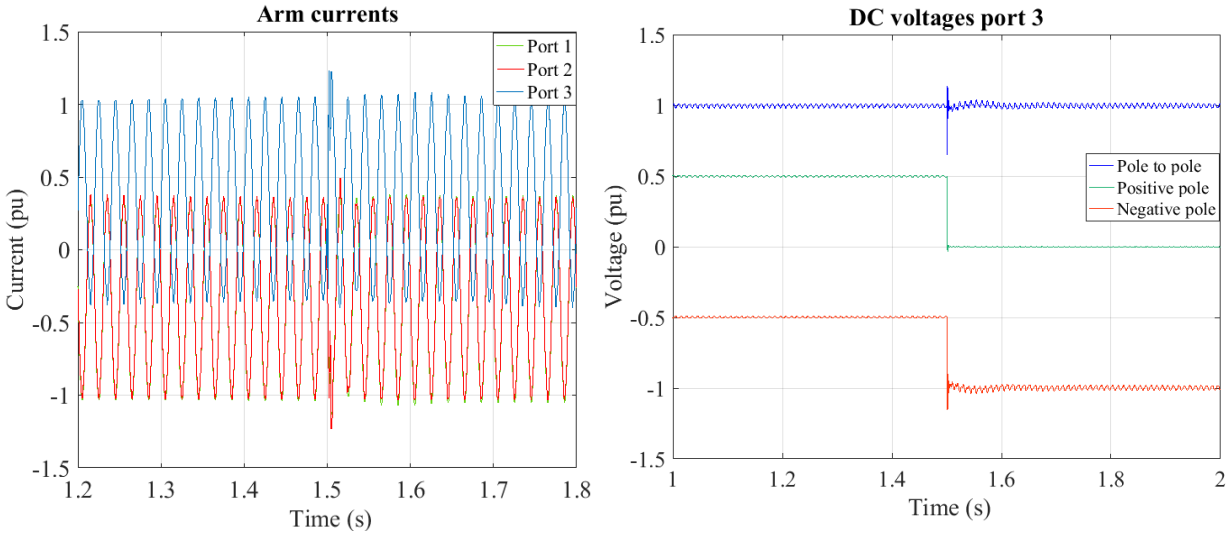
The produced phase voltage having a DC component discharges to zero through the grounding leading to large AC currents. This is observed in the case of the (Yg-Yg) configuration and in the case where no transformer is used on the AC side of port 3. However, in the other cases where no ground is encountered and the DC component of the mutated AC voltage is now filtered by the transformer, the DC pole-to-pole voltage remains stable and the DC hub continues its normal operation. In order to confirm these conclusions of port 3 similar analysis took place in the ports 1 and 2 resulting in the same observations.

TRANSFORMER ADDITION

As a result, a (D-Yg) transformer is added on the AC side of port 3, with the D on the converter side. Following the case where a short-circuit occurs at port 3 operating on AC voltage control is presented. At the moment

of the fault, an inrush current is observed to the ground similar to the previous cases. There is no overcurrent observed in the arms or in the intermediate AC link. Following, the arm currents of each port can be seen in figure 6.12a.

Moreover, it is observed that the voltage of the faulty pole jumps to zero. The voltage of the healthy pole has a new value while the pole-to-pole voltage remains the same. The new value of the healthy pole is equal to two times the pre-fault DC voltage value. The DC voltages are presented in figure 6.12b. This voltage mutation is following seen in the phase voltage on the AC side of port 3. The phase-to-phase voltage remains the same as the two DC components cancel each other. The DC component of the phase voltage is now filtered through the added transformer.



(a) Arm currents

(b) DC voltage

Figure 6.12: Pole-to-ground fault at port 3

The addition of a third transformer at port 3 leads to a more symmetrical system. The use of a (D-Yg) grounded transformer in every port results in the fault ride-through capability of all the ports during a pole-to-ground fault. The response of the system was observed to be similar in all the cases. It is observed that there are no currents flowing through the fault towards the intermediate AC link. As a result, all ports continue their normal operation. It is important to mention that due to this special response to a pole-to-ground fault, where the DC hub can continue its normal operation, the fault detection system has to be designed appropriately.

6.5. POLE-TO-POLE FAULT

A pole-to-pole DC fault can be analyzed into three distinct stages according to [57]:

1. DC cable and submodule capacitor discharge
2. AC transient infeed by the antiparallel diodes
3. AC steady state infeed and AC breakers activation

DC Cable and Submodule Capacitor Discharge At this stage, the cable and the capacitors of the inserted submodules at the time of the fault discharge and contribute to the steep increasing fault current. The lower control (capacitor balancing and circulating-current controller) continues its operation. As a result, capacitors can be bypassed or capacitors can be inserted and contribute to the fault during this stage depending on the gate signals references. The AC infeed during this stage is limited and can be assumed zero. In comparison to the 2-level VSC, the peak of the short-circuit current is foreseen to be much lower for the MMC due to the small amount of distributed DC capacitors that are inserted in the circuit.

The semiconductor switch turn off instant is a parameter depending on the converter internal protection. The time period between the initialization of the fault and the blocking of the switches is important. The later the semiconductor switches turn off, the higher the contribution from the capacitive discharge of the submodules.

For this stage, an equivalent RLC circuit for one leg can be used in order to model the capacitors discharge. In the following figure 6.13 the equivalent inductances, resistances and capacitances have the following values:

$$L_{eq} = 2L_{arm}, \quad R_{eq} = 2R_{arm}, \quad C_{eq} = C_{sm}/N$$

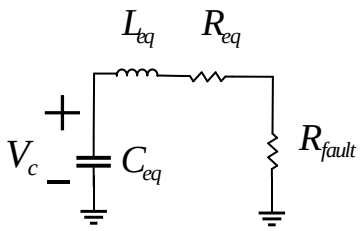


Figure 6.13: Equivalent circuit

The equivalent leg capacitance depends on the number of submodules inserted before the fault. It is shown in [57] that $C_{eq} = C_{sm}/N$ provides a better approximation for the fault current than the equivalent capacitance based on the energy stored in the capacitors $C_{eq} = 2C_{sm}/N$.

The above RLC circuit is characterized by the following second order equation

$$\frac{d^2 v_c}{dt^2} + 2\alpha \frac{dv_c}{dt} + \omega_0 v_c = 0 \tag{6.2}$$

where

$$\alpha = \frac{R}{2L}$$

$$\omega_0 = \sqrt{\frac{1}{LC}}$$

In the case of a pole-to-pole fault, the fault resistance is very small and is assumed zero. Following the cable inductance and resistance depend on the fault location in the DC line. In the worst case where the fault is located close to the converter, the $R_{cable} = 0 \quad and \quad L_{cable} = 0$

For the first stage of a pole-to-pole fault the leg contribution is given by:

$$i_{cap,dis} = \frac{V_{dc}}{\omega L_{eq}} e^{\frac{-Req}{2Leq}} sin(\omega t) \tag{6.3}$$

where

$$\omega = \frac{\sqrt{\frac{4L_{eq}}{C_{eq}} - R_{eq}^2}}{2L_{eq}}$$

AC transient Infeed by the antiparallel diodes This stage begins when the IGBTs are blocked and the antiparallel diodes come into conduction. Both AC and DC transient components are present on this stage. From the previous stage, the capacitors discharging energy was stored in the arm inductors. At this point, a decaying current is observed due to the release of this stored energy. The time constant of the RL circuit is given:

$$t_{dc} = L_{arm}/R_{arm} \quad where \quad R_{arm} = N_{Ron}$$

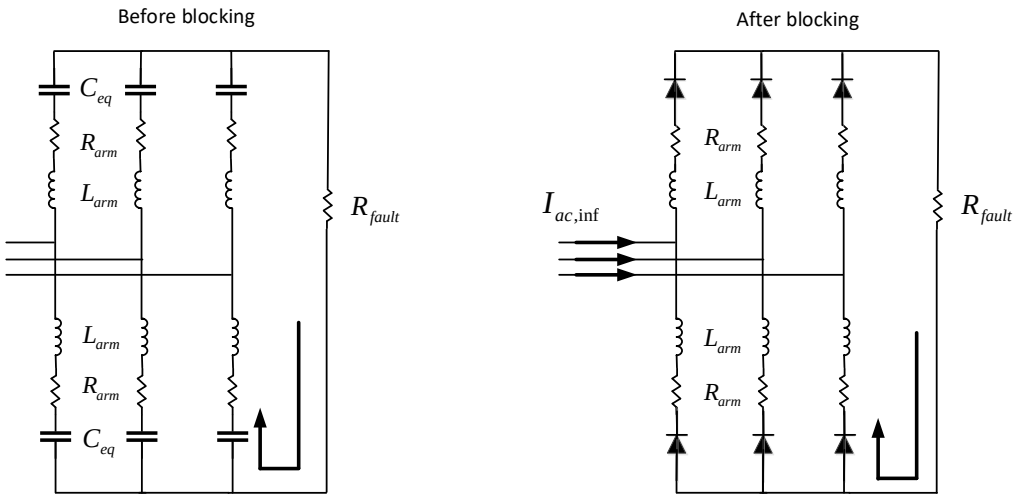


Figure 6.14: DC fault stages

AC steady state infeed and AC breakers Activation In this stage, the AC side feeds entirely the DC fault. The AC fault current is rectified through the antiparallel diodes, resulting in a six-pulse ripple in the DC fault current. The AC breakers are activated and the converter is disconnected from the AC network. This activation will take place after 2-3 fundamental AC cycles.

In the equivalent circuit for the MMC during fault contingencies, the response is affected by the power semiconductor switches turn-off instant, the fault resistance and the DC inductance.

- **Power semiconductor switch turn-off instant:** If the switches turn off immediately at the fault instant, the capacitors do not discharge and DC fault is directly fed by the AC side. The longer it takes to turn-off, the higher the current peak contribution from the capacitors discharge. This parameter affects only the first stage. This parameter is determined by the converter internal protection.

- **Fault resistance R_f:** It affects both the steady state and the transient fault current. The larger the R_f, the lower the peak and the steady state DC fault current. Also during stage 2, the transient DC component decays faster.

- **DC side inductance L_d:** The contribution in stage 1 is negligible. The greater the L_d the lower the rate of rising of the DC fault. The transient component in stage 2 decays slower.

6.5.1. POLE-TO-POLE FAULT AT PORT 1

The aim of this section is to study the overcurrents and overvoltages presented in the system components. The protection system is responsible to detect this non-healthy behavior and protect the system components. The most important and vulnerable to fault components are the power semiconductor switches of the submodules. For that reason, special attention should be paid to the arm current values. In this section, the ability of the rest of the ports to continue their normal operation after a pole-to-pole fault contingency is also studied. A port can continue its normal operation if it is not blocked by the protection system, meaning that all the values stay between the predefined limits and if the control operation of the port is maintained.

The two poles of the transmission line are short-circuited. The worst case where the fault occurs close to the port of the DC hub is studied. The submodules of the two terminal converters are blocked after the fault is detected. In this way, the power semiconductor switches are protected and the antiparallel diodes start to conduct. As a result, the fault current flows through the antiparallel diodes. In order to isolate the fault, AC circuit breakers are used. The activation of the circuit breakers takes place after 2-3 fundamental AC cycles. In the following fault studies, the worst case, where the AC circuit breakers are activated after 60ms is presented. In the following simulations, the value of the arm currents of the faulty and the two other healthy ports are calculated. In this way, the power semiconductor switches and the antiparallel diodes can be dimensioned appropriately for the pole-to-pole fault contingency.

NATURAL RESPONSE

A pole-to-pole fault at port 1 takes place at $t = 1.5s$. The fault resistance is assumed to be equal to 0.01 Ω. The fault detection system is in operation. The natural response of the DC hub is following studied, where on the intermediate AC link only the two transformers are present without any phase reactors.

The fault current presents a value of $8.8pu$ at the time of the fault. In the point-to-point transmission line $p1p5$, the overcurrent is detected immediately and the terminals 1 and 5 are blocked. This high fault current is conducted by the antiparallel diodes of the faulty port. The large fault current will flow in the intermediate AC link of the DC hub towards the other ports. The AC currents in the intermediate link are shown in figure 6.15. It can be observed that the currents of port 3 are much larger than port 2. The reason for that is the control mode operation of the two ports. The port 2 operates in active power control mode preserving the power and the current through the $p2p4$ stable to its reference values. While port 3 operates in AC voltage controlled mode. The power in the $p3p6$ is not directly controlled. As a result, all the transient currents flow through port 3.

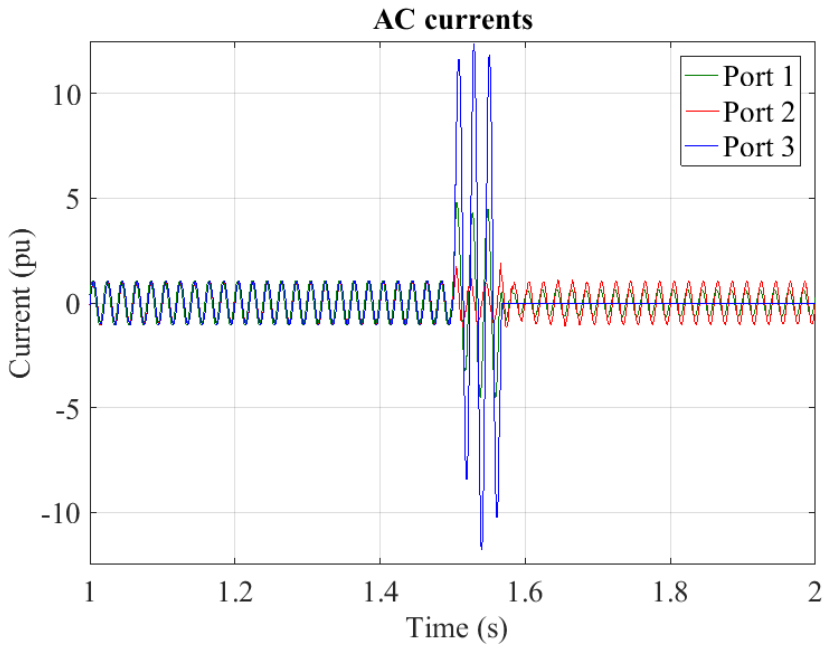
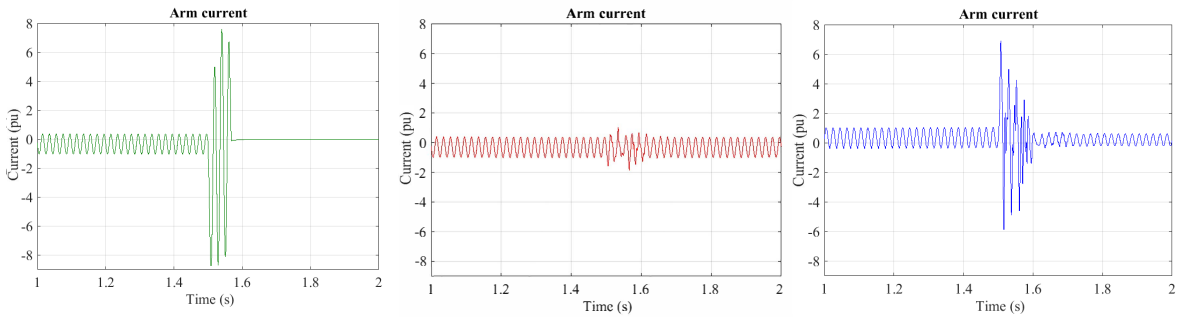


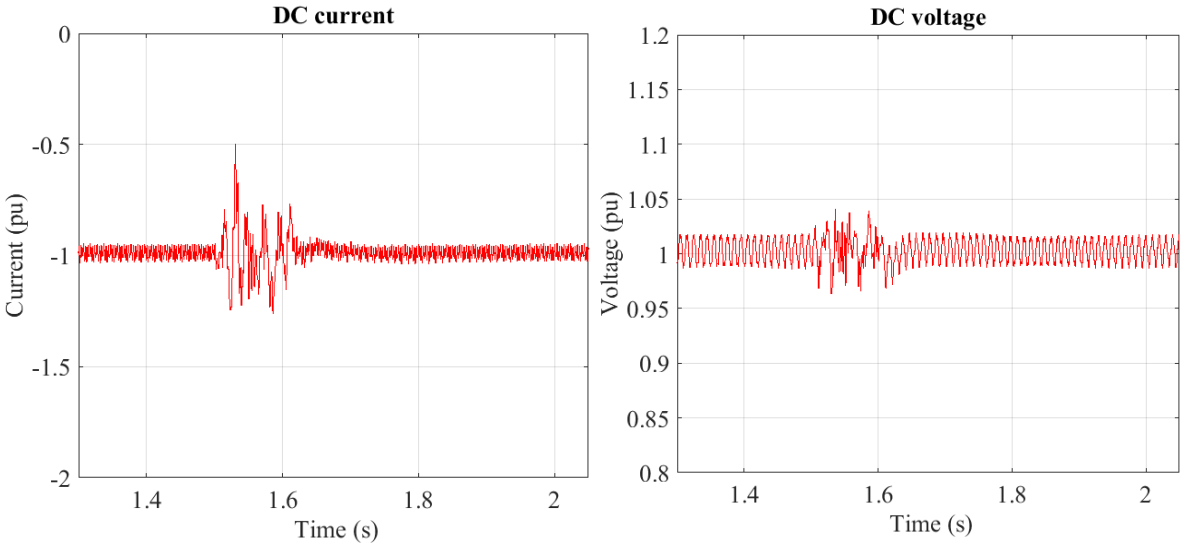
Figure 6.15: AC currents during pole-to-pole fault

Following, these high currents will flow through the arms of the converters and affect the operation of the rest of the ports. The arm currents shown in figure 6.16 follow the same pattern as the AC currents. The DC voltages and currents of ports 2 and 3 are shown in figures 6.17 and 6.18. It is observed that the port 2 preserves its normal operation with a very small ripple ($\pm 0.04pu$) in the DC voltage. While the DC voltage of port 3 presents a ripple of $\pm 0.17pu$. This DC voltage transient lasts for 250 ms. Moreover, the DC current reaches a peak of 3.3 pu but for a time period smaller than 1ms. It is assumed that such a high current for such short period does not affect the cable insulation or enables the protection system. The fault current flows inside the AC link increasing the values of the intermediate AC link currents of each port and finally reaches the arms of the other converters.The AC cables should be dimensioned for each port separately.



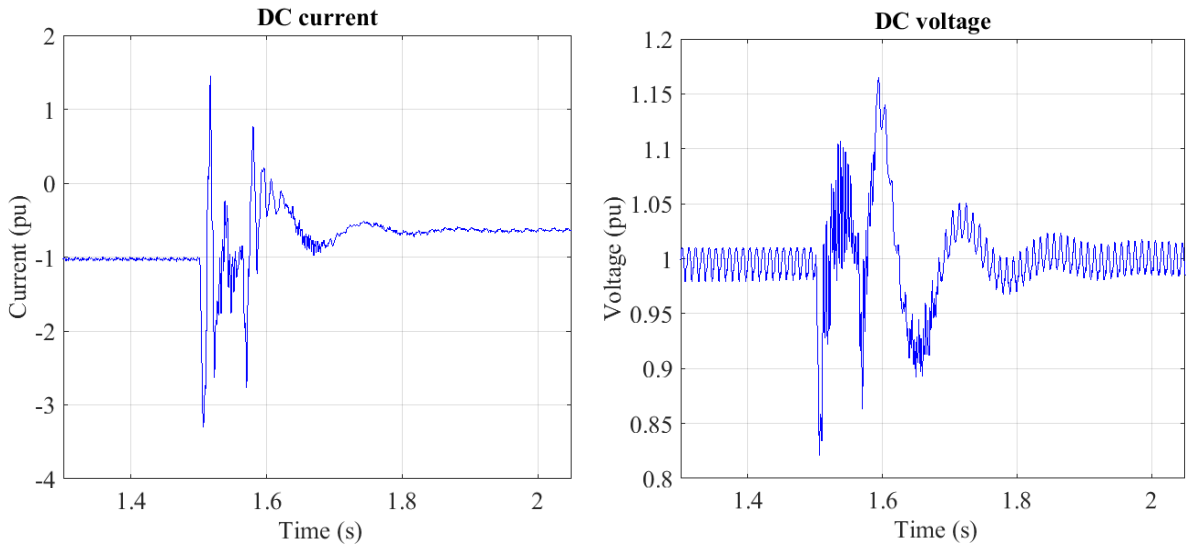
(a) Port 1 (b) Port 2 (c) Port 3

Figure 6.16: Arm currents during pole-to-pole fault at port 1



(a) DC current (b) DC voltage

Figure 6.17: Port 2 DC values during pole-to-pole fault on port 1



(a) DC current (b) DC voltage

Figure 6.18: Port 3 DC values during pole-to-pole fault on port 1

A similar observation made in the connection and disconnection can be also made in the pole-to-pole fault contingency. It is observed that the fault current flows through port 3. This leads to arm and DC line current ripples. Following, the DC voltage transients affect in a small percent the AC voltage control of port 3. Port 2 continues its normal operation throughout the fault contingency. It is only affected by the small changes of the AC hub voltage. Moreover, the high arm current is increasing the ripple of the sum capacitor voltages as seen in figure 6.19.

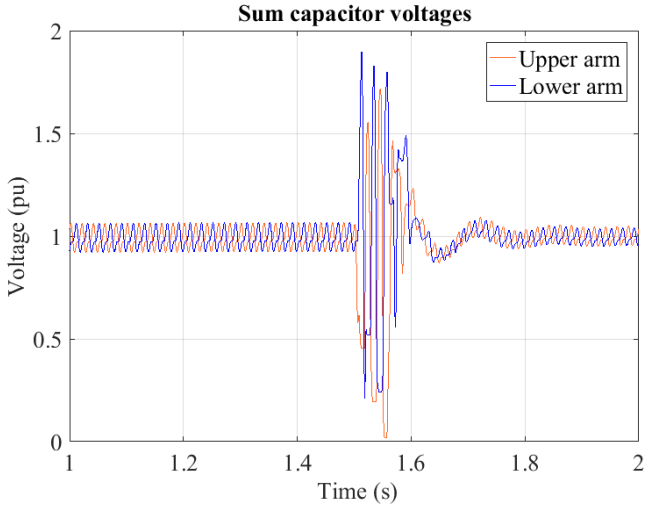


Figure 6.19: Sum capacitor voltages of port 3

The DC voltage and current of $p3p6$ are affected by the fault. This affects the AC voltage control leading to ripples. In figure 6.20 it can be observed a ripple in the AC voltage with a voltage drop at $0.75pu$ following by an increase at $1.15pu$ and continuing with some oscillations before returning to its nominal value after 200 ms. This voltage drop in the AC intermediate link is the reason for the increase of the AC current at port 2 in order to maintain the power transfer equal to 1 pu.

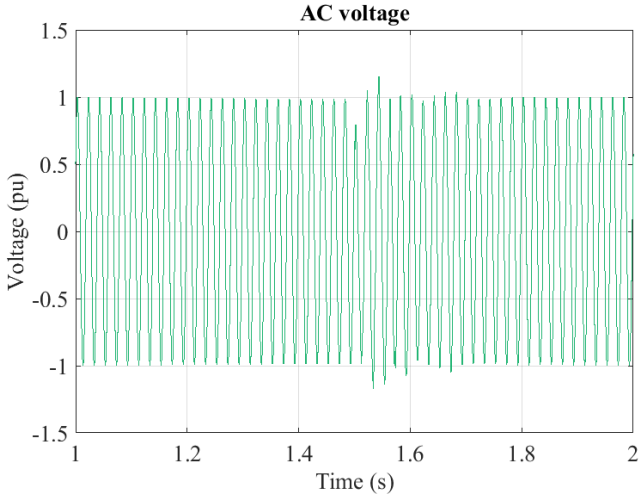


Figure 6.20: AC voltage during fault pole-to-pole on port 1

From studying the natural response for a pole-to-pole fault in port 1 it is observed that the currents flowing through the antiparallel diodes are very large, but also the arm currents of port 3 are large. Although the antiparallel diodes can be dimensioned for a higher current, the power semiconductor switches do not have that attribute. This leads us to take action in order to limit this overcurrent. A way to limit this high fault current is by inserting AC phase reactors in the intermediate AC link. At this point, the dimensioning of the

components for higher currents is not suggested as the currents observed are still very high. In order for the semiconductor switches to withstand the observed high currents, power semiconductor switches should be used in parallel increasing not only the cost due to higher semiconductor switch use but also the losses.

PHASE REACTORS

The effect of adding a phase reactor in the AC side of the faulty port can be observed in figure 6.22. The different values of inductance and the decrease in the arm current of the faulty port are presented in table 6.5. It can be observed that the larger the phase reactor, the lower the current peak. Also, it is observed that after some point increasing the phase reactor value is not that effective in reducing the current peak as seen in figure 6.21.

Table 6.5: Phase reactor effect on pole-to-pole fault on port 1

Case	Inductance (mH)	Inductance (pu)	Current peak (pu)
A	0	0	7.70
B	30	0.084	5.20
C	60	0.168	3.95
D	90	0.252	3.15
E	120	0.335	2.95

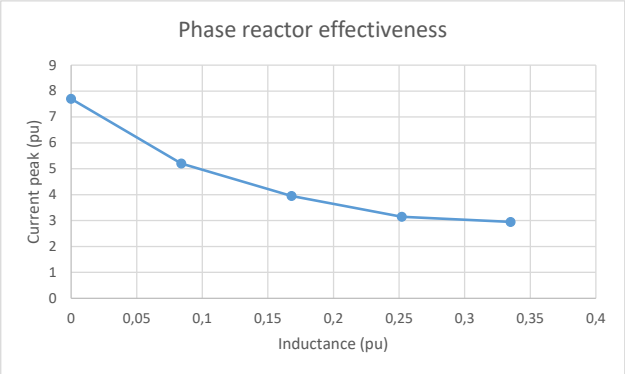


Figure 6.21: Phase reactor effectiveness on limiting the arm current peaks at port 1

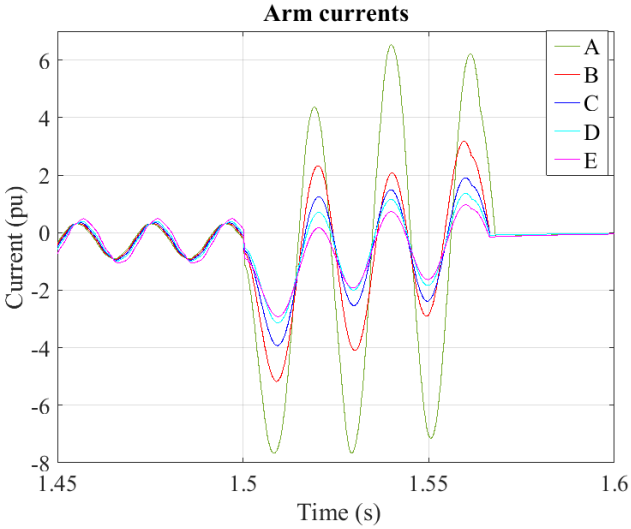
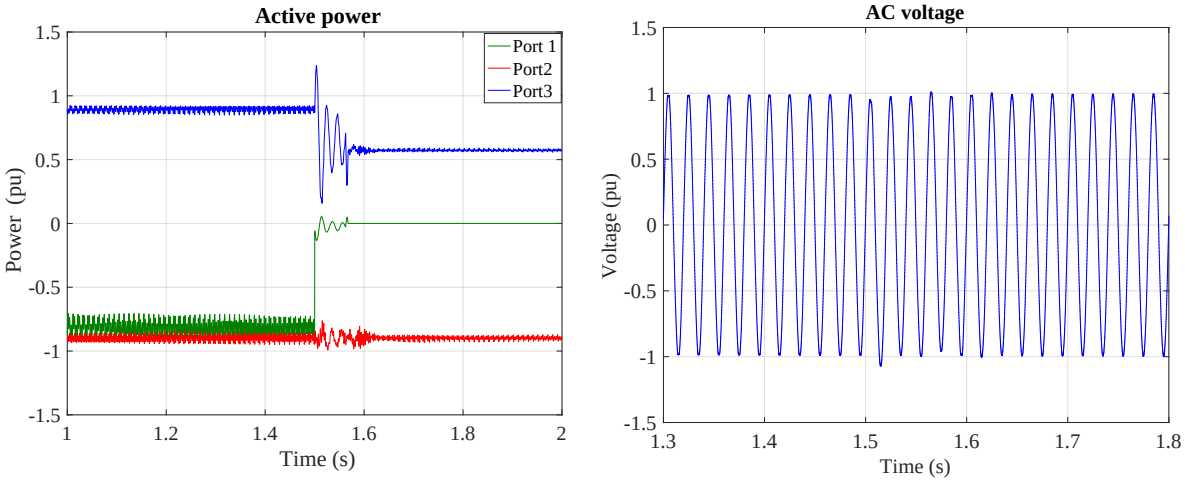


Figure 6.22: Arm currents of port 1 for different phase reactor values

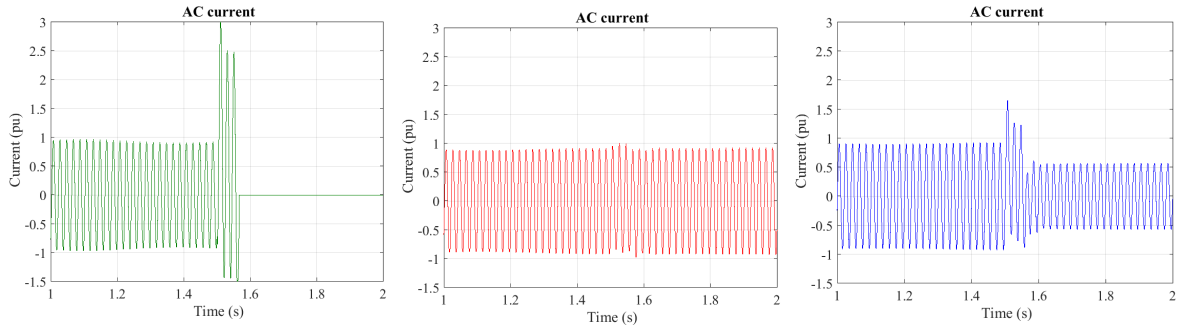
A phase reactor of $0.335pu$ equal to $120mH$ is added in every phase of port 1, between the transformer and the converter, in order to limit the fault current. The following case where $P_5 = 0.8pu$ and $P_2 = 0.9pu$ is presented. In figure 6.23a the active power of each port is presented. A step is observed on the power of port 3 after the disconnection of the faulty port 1, while port 2 maintains the same power level. The pole-to-pole fault affects the RMS value of the AC voltage in a small percentage of $\pm 0.04pu$. The AC voltage can be seen in figure 6.23b. The AC currents are presented in figure 6.24. In port 1, which is closer to the DC fault the highest currents are observed. In figure 6.25, the arm currents of every port are presented. In port 1 where the submodules are blocked, the larger than 2 pu arm current is conducted by the antiparallel diodes. Port 3 presents a peak lower than 2 pu, while port 2 is almost unaffected by the fault. In figures 6.26 and 6.27 the DC currents and DC voltages of all the ports are presented. The response of the DC link connected to the port 2 is similar to the cases of connection/disconnection. Port 2 is only affected by the small change in AC voltage leading to small ripples of its values. Port 3 is directly affected by the fault, however without presenting high values or losing its control. A ripple of $\pm 0.075pu$ is present on the DC voltage, while the DC current presents a ripple less than ± 0.5 before attaining a new value, which is smaller than the previous because of the power loss due to the faulty port's disconnection.



(a) Active power

(b) AC voltage

Figure 6.23: Values with phase reactor during pole-to-pole fault at port 1

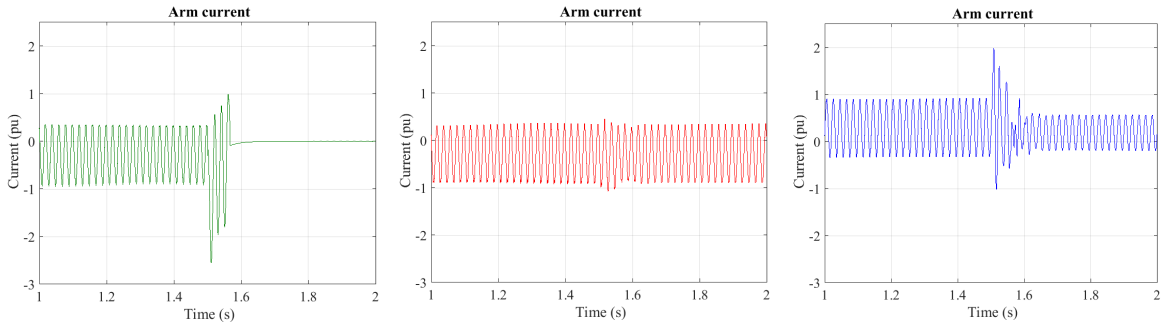


(a) Port 1

(b) Port 2

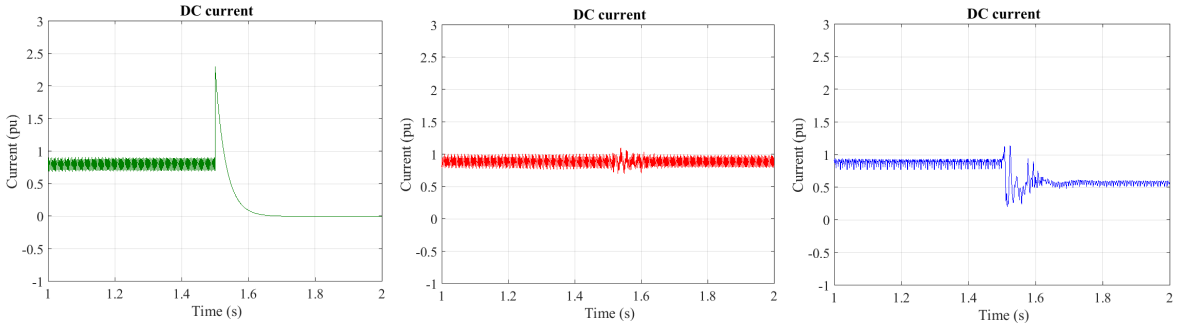
(c) Port 3

Figure 6.24: Values with phase reactor during pole-to-pole fault at port 1



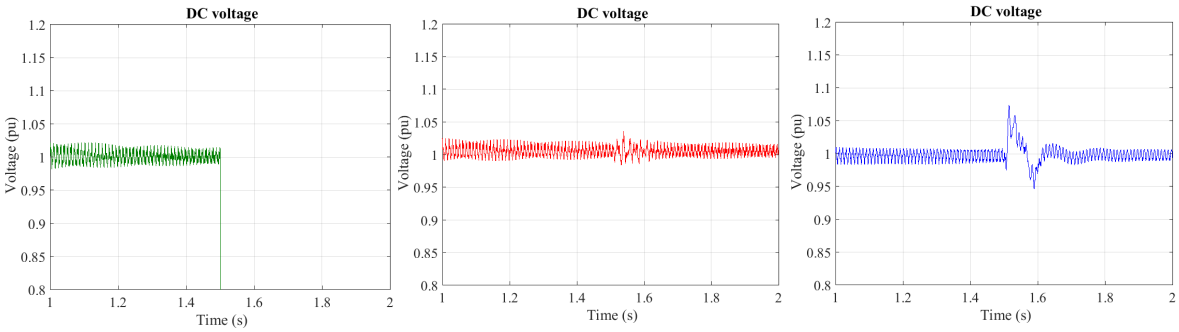
(a) Port 1 (b) Port 2 (c) Port 3

Figure 6.25: Values with phase reactor during pole-to-pole fault at port 1



(a) Port 1 (b) Port 2 (c) Port 3

Figure 6.26: Values with phase reactor during pole-to-pole fault at port 1



(a) Port 1 (b) Port 2 (c) Port 3

Figure 6.27: Values with phase reactor during pole-to-pole fault at port 1

Overall, the simulation results indicate that the DC hub maintains its controllability. The thresholds for the protection system can be adjusted accordingly based on the simulation results. The AC voltage control is maintained which is important for the stability of the DC hub. Finally, the observed arm currents have values under the predefined limits. A fault ride-through capability can be attained for port 1.

6.5.2. POLE-TO-POLE FAULT AT PORT 2

NATURAL RESPONSE

A pole-to-pole fault takes place at $t = 1.5s$ at port 2 operating in active power control mode. Port 2 has higher ratings compared to port 1 and as a result, the fault currents are higher. These large currents observed in the simulations, lead to ripples on the AC voltage. The DC current in port 3 is over the predefined allowed value and this result at the blocking of the converters. The results indicate that the operation of port 1 is not

affected from the fault overcurrents, however, it is affected from the loss of the AC voltage control. From the above, a useful conclusion can be made. It is important for the port operating in AC voltage control mode to maintain its stability, as a loss of the AC voltage can lead to instabilities in the other ports.

PHASE REACTORS

After studying the fault response, it was observed that the arm currents of port 3 reach large values. The power semiconductor switches are going to be damaged from these large fault currents. In order to limit the fault current, a phase reactor is added on the intermediate AC link between the faulty port and the transformer.The arm current peaks of port 3 are calculated for the different values of phase reactors. The results are shown in the table 6.6. Similar conclusions with the previous case can be made. The increase of the inductor value lowers the current peak but after a point, this increase is not so effective as seen in figure 6.28. It can be seen that even for a value of $0.35pu$ equal to $210mH$ the peak current takes values of $2.9pu$. Also, it was observed that the addition of large phase reactors affects the active power control, resulting in slower changes for the given references.

The study case of a pole-to-pole fault with the addition of a phase reactor equal to $0.225pu$ is presented. Port 2 responsible for the active power control operates in P=0.5 pu.

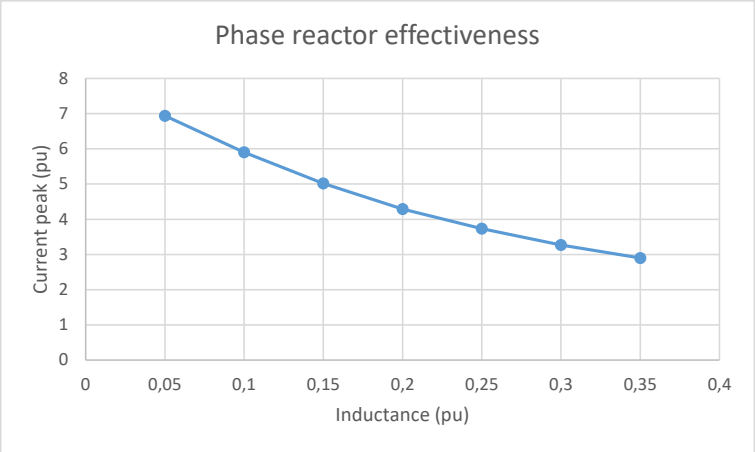


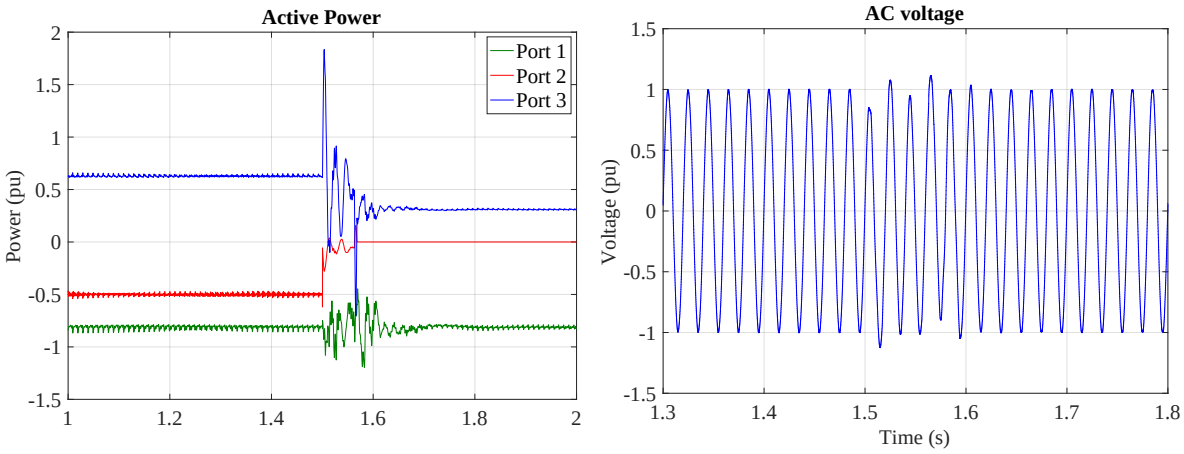
Figure 6.28: Phase reactor effectiveness on limiting the arm current peaks at port 3

Table 6.6: Arm current values of port 3

Inductance (pu)	Current peak (pu)
0.05	6.94
0.1	5.9
0.15	5.02
0.2	4.29
0.25	3.73
0.3	3.27
0.35	2.9

In figure 6.29, the active power of all the ports can be seen. Port 1 continues to operate in the same power reference after the fault, while port 3 lowers its active power due to the disconnection of the faulty port 2. Moreover, the RMS voltage of the intermediate AC link presents a ripple of $\pm 0.1pu$ and returns to the reference value after 120ms.

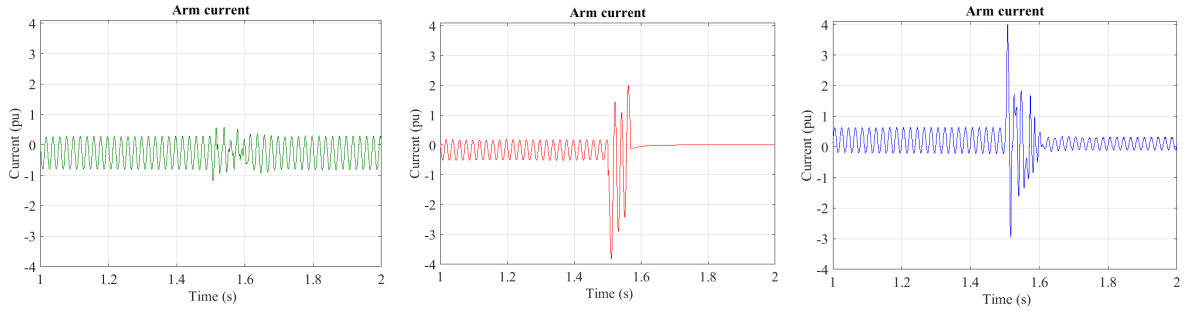
The proper dimensioning of the SM's power semiconductors can be done by observing the arm currents in figure 6.30. As it was expected, the arm current of port 1 is not affected by the fault. However, a small transient is observed due to the changes in AC voltage. Port 2 is blocked and the fault current flows through the antiparallel diodes. The peak current observed is 3.9 pu, as a result, the antiparallel diodes should be



(a) Active power (b) AC voltage

Figure 6.29: Values with phase reactor during pole-to-pole fault at port 2

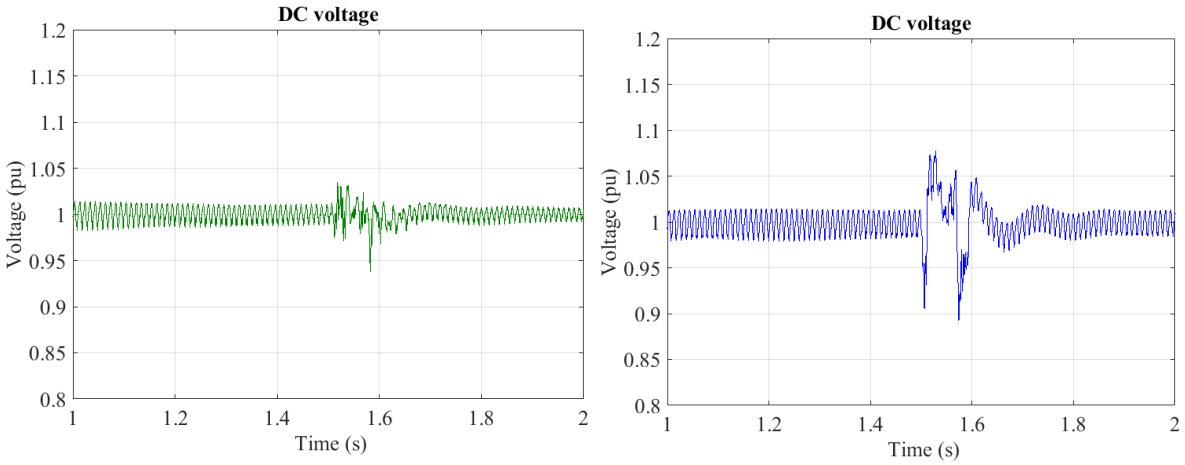
dimensioned accordingly. In port 3, the current is conducted by both the power semiconductor switches and the antiparallel diodes. The arm peak current observed is 3.95 pu.



(a) Port 1 (b) Port 2 (c) Port 3

Figure 6.30: Values with phase reactor during pole-to-pole fault at port 2

Next, the DC values of the two healthy point-to-point transmission lines are observed. The peak DC currents for port 1 and 3 are 1.12 pu and 2.2 pu. Also, the duration of these transients is 120 ms. The cables can withstand these values and the protection system is not enabled. In figure 6.31 the DC voltages of port 1 and 3 are observed. A maximum ripple of $\pm 0.06 pu$ pu is observed in port 1 while in port 3 the maximum ripple is $\pm 0.11 pu$. The transients observed in port 1 has a duration of 200 ms while in port 3 for 300 ms before they return to their nominal values.



(a) Port 1

(b) Port 2

Figure 6.31: Values with phase reactor during pole-to-pole fault at port 2

Overall, port 3 is directly affected by the fault, while the transients observed in port 1 are caused by the changes observed in the intermediate AC link voltage. The system continues its normal operation after the fault and all the reference values are maintained. In order to achieve a fault ride-through capability apart from the phase reactors addition, power semiconductor switches should be added in parallel in order to attain a maximum threshold of 4 pu.

6.5.3. POLE-TO-POLE FAULT AT PORT 3

The last port to be studied under pole-to-pole fault is port 3 operating in AC voltage control mode.

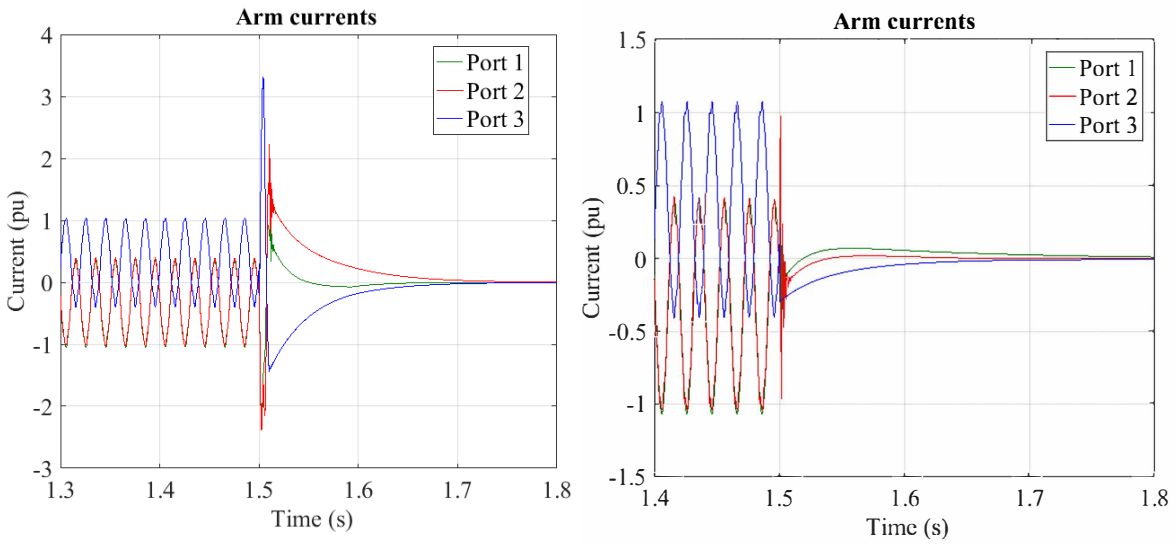
NATURAL RESPONSE

Firstly, the natural response of the DC hub is observed for the pole-to-pole fault contingency at $t = 1.5s$. The protection system of port 1,2 is disabled in order to observe the response of each port. After the fault occurrence, the AC voltage starts to collapse. Following, there are observed large DC currents from the outer terminals towards the fault location. These large currents pass through the arms of the converters and the cables of the AC intermediate link. Next, the fault detection system located on the DC link is enabled. As it was expected due to the high currents present on the DC line both the converters of the point-to-point transmission lines are blocked. The currents are above the predefined limit for the DC line. The AC voltage of port 3 collapses. As the other two ports maintain their AC voltage, an inrush current will be present from port 1,2 towards 3 due to the voltage difference. Port 1,2 feed the current until they are blocked. In the studied scenarios submodule fault detection system is disabled in order to study the overcurrents inside the arm. As seen in figure 6.32a port 2 absorbs higher current than 2 pu. In this case, the protection system located on the arms will act faster than the one on the DC link. The arm currents are shown in figure 6.32a. In this case, all the ports are blocked and the DC hub is not operational.

In the previous sections, in order to limit the large fault currents, phase reactors are inserted in the intermediate AC link. In this case, as the DC hub stops its operation and all the converters are blocked, the intermediate AC link does not feed the fault current. For that reason, the currents observed in the system are lower compared to the previous cases. This leads to the fact that no extra phase reactors are needed in order to limit the fault current.

After the fault occurrence, efforts were made in order to block only the faulty pole, while the rest of the ports to continue their normal operation. This case is similar to section5.2.3 where the port responsible for AC voltage control is disconnected and another port changes its control mode operation. In comparison with the simple disconnection, the same could not be achieved in a pole-to-pole fault contingency. The system control is lost leading to instabilities and finally, all the ports are blocked.

In order to limit the large currents present in the arm currents, the following solution is proposed. After the fault occurrence, the protection system does not only send a signal to block the faulty port but also sends signals to the other ports of the hub in order to get blocked. It can be assumed that as the ports are located very close, the block signals can be enabled almost instantly after the fault detection. This fast blocking



(a) Normal block

(b) Fast block

Figure 6.32: Comparison of arm currents based on blocking times

leads to lower values for the arm currents. In section 6.5 the three distinct stages of a pole-to-pole fault were presented. In the presented case only stage 1 takes place namely, the DC cable and submodule capacitor discharge. As a result, the AC infeed stage is skipped. In figure 6.32b , the arm currents are presented. Moreover, there are no overcurrents observed in the AC link. After the currents return to zero approximately in 300 ms, the restoration of the system can begin. In case of a permanent fault at port 3, port 3 remains blocked and port 2, fulfilling the attributes of being responsible for the AC voltage control, restarts its operation but now in AC voltage control mode.

6.6. CONCLUSIONS

The results in the section of the pole-to-ground fault indicate that the DC hub can obtain a fault ride-through capability following the proposed design methodology. This capability allows the faulty port to continue its operation with the condition that the healthy pole can stand twice the rated voltage. It is important to see that in this case, the transmission power and the DC-voltage are at the same level as in the pre-fault system. In case of a permanent fault, the pole-to-ground fault needs to be cleared as fast as possible. The results provide important insights for the transformer configuration used at the AC side of every port in the DC hub. A third transformer is added on (D-Yg) configuration in order for every port to have fault ride-through capability. This fact increases the dimensioning of the system by increasing the size, weight, and cost, however, it offers fault ride-through capability under pole-to-ground faults for the DC hub. Overall, the simulation results suggest that the DC hub continues its normal operation after the pole-to-ground fault contingency. The faulty port can also continue its normal operation. This is an advantage especially in the case where critical loads are connected to the faulty DC line. The system can withstand temporary overvoltages, providing the time in order to take the appropriate actions. Such actions can be the decrease of the power flow in the transmission line and the activation of the AC circuit breakers in order to disconnect the line.

In the second part of this chapter, the most severe pole-to-pole fault is studied. The natural response to the fault on every port is presented. Overall the results suggest that with the addition of phase reactors, a fault ride-through capability can be achieved for the rest of the DC hub while the faulty port is disconnected. This conclusion is valid for ports 1 and 2. In port 2 as the arm current peaks get higher than 2 pu, there is a need to parallel more than one semiconductor switches. As far as it concerns port 3 simulations showed that changing the port operating in AC voltage during a pole-to-pole fault contingency results in losing the AC voltage control. In the normal disconnection of a port operating in AC voltage control and the control change operation of another port was successful, as seen in the previous chapter. However, in the pole-to-pole fault contingency, the high current does not allow the control change, leading to instabilities. For this reason, the whole DC hub needs to shut down. The solution of blocking fast the healthy ports in order to limit the large currents is proposed. In case of a temporary fault, the DC hub restoration can take place after the fault is

isolated and all the currents have zero values. This time is calculated to be 300ms. In case of a permanent fault, after 300ms, a new port will be responsible for the AC voltage control.

7

CONCLUSIONS AND FUTURE WORK

7.1. CONCLUSIONS

Nowadays, there is a movement towards the creation of HVDC grids. The motivations for being attractive were mentioned in the introduction. Moreover, there are still some limitations and further research is needed for the creation of HVDC grids. Consequently, this thesis focused on the study of a new element which can offer solutions to the different limitations. A DC hub is presented, while its operation under transient phenomena and the ability to isolate DC faults was studied. The conclusions reached through answering the main objectives are presented hereby.

DESIGN OF A THREE-PORT DC-DC CONVERTER

The DC hub is a multiport high power high voltage DC-DC converter. In order to make a decision over the most appropriate topology for a DC hub, it is logical to study first the two-port DC-DC converter. A literature review took place, the advantages, disadvantages and most importantly, the ability of a two-port DC-DC converter to upgrade into a multiport were examined. The different topologies were categorized. It has been seen that although the one-stage topologies are more compact and have a smaller footprint, they are not so prominent to be used in a DC hub as their upgrade is complex, costly and not efficient. The most dominant design is the front-to-front topology. From the different VSC-converters, the modular multilevel converter being now a mature technology predominate the others. The state of the art MMC offers higher reliability, higher power quality, lower losses and has a modular structure. Also, it has advantages during fault contingencies compared to the two-level VSC. Furthermore, by studying the DC hub literature, there are two dominant approaches based on the components used on the intermediate AC link. The first approach uses LCL filters and based on the resonance, the different voltage levels are matched. It offers the advantages of a small footprint by only using capacitors and inductors in the AC link. Also, a great advantage is its fault response, achieving fault ride-through capability. However, some disadvantages are present. The fact that the new line to be connected must have a lower voltage than the central capacitor voltage and the symmetrical DC voltage stepping around a central point, not allowing the use of asymmetric monopole configuration, limits the expandability of the DC hub. Furthermore, in the resonant DC hub configuration, all the ports must operate in the rated full power in order to have zero reactive power circulation. This fact leads to lower efficiencies when the ports are not operating at full power. In fact this can happen very often due to the intermittent character of the renewable energy sources. These are parts of the basic attributes of a DC hub. The limits observed in the expandability and power flow efficiency lead to the decision of using an intermediate AC transformer instead of LCL filters.

The multiport DC-DC converter using MMCs in front-to-front configuration with AC transformers located in the intermediate AC link is chosen as the most prominent topology. It has the advantage of interconnecting multiple HVDC lines at different voltage levels and with different configurations. Moreover, the modular design of the DC hub offers connection points for expansion. Any number of ports can be added by connecting to the intermediate AC link via a transformer. After observing the natural instabilities inside the DC hub a different control approach is suggested. Based on this approach, all ports operate in current-control mode, except the port responsible for maintaining the AC voltage in the intermediate link, which operates in voltage-control mode. Moreover, the design of a three-port DC hub with different power and voltage levels

on every port and with different control modes was presented. A discussion and a suggestion for the control role distribution took place. The port with the highest power rating is chosen to operate in AC voltage control while the port with the lowest power rating in DC voltage control. These decisions were made after observing the operation of DC hub under step reference changes in the controlled values and were following confirmed through the line connection/disconnection and the DC fault studies. The basic characteristic of the designed DC hub is the fact that in the point-to-point transmission line where the port operates in AC voltage control, there is an absence of direct active power control. The active power of this port is equal to the sum of the two other ports. Apart from the AC voltage control, the port with the higher rating power is responsible to provide power to the other two ports and has the capability to absorb or provide the transient currents, which due to higher power rating have less impact on its operation. It was observed that the operation of the port operating in DC voltage control mode had no effect on the operation of the one operating in active power control mode and vice versa. However, the step reference changes performed on the values of DC voltage and active power affect the operation of the port responsible for the AC voltage control of the intermediate AC link.

ANALYSIS OF THE DC HUB RESPONSE TO A LINE CONNECTION/DISCONNECTION

In the study case of a line connection, an inrush current is observed in both scenarios of connecting a port operating in DC voltage and a port operating in active power control mode. The use of insertion resistors is proposed for the first 0.5-1s in order to limit this inrush current, leading to a smoother transition. Overall, it was shown that the system continues its normal operation without any large currents or voltages being present. The port disconnection was next studied more in depth. For all the ports two cases, one in zero power and one in full power were presented. The results indicate that when the suggested steps for a line disconnection are followed, an excellent transition is achieved. The suggestion is to keep the power flowing through the line to be disconnected at zero, in order to minimize the transient effects on the rest of the system. After reaching a point of zero power flow, then the AC breakers located in the intermediate AC link can open. However, in some cases, a port can be disconnected while operating at full power. The worst case of all the ports operating at full power was next studied. The results show that the DC hub continues its normal operation after this case. In both cases of connection and disconnection, the system maintains its operability and there are no high voltages or currents observed in the system.

To complete the line disconnection study, the special case of disconnecting the port responsible for controlling the AC voltage inside the DC hub was next studied. In this case, in order for the rest of the system to continue its operation, a different port must change its control mode and operate in AC voltage control mode. The new port is chosen according to the following suggested criteria. First, the port must have the higher power rating. Second, it should operate in active power control mode. Third, the power flow must be bidirectional. Finally, it can cover the power needs of the remaining ports. From the results, the successful disconnection of port 3 was observed, when zero power transfers through the DC hub. Furthermore, in case of a full power operation, such a change results in power reversal for the port operating now in AC voltage control. In this case harsher transients were observed, however, the system maintains its controllability. The following useful insights are provided from the simulation results for different levels of power reversal. A big power reversal, results in large DC current peaks and lower values for the DC voltage, for longer time periods. In order to observe the maximum and minimum values during the transient events, the protection system was disabled. The thresholds of the protection system are project specific.

ANALYSIS OF THE NATURAL FAULT RESPONSE OF THE DC HUB

It is stated that for the fault studies the symmetric monopole configuration is only examined as it is the most commonly used. The pole-to-ground fault was first studied. In the first design of the system, two transformers are present. This decision was based on the following criterion. In order to achieve the interconnection of N ports with different DC voltage levels, N-1 transformers should be used. Different three-phase transformer configurations were examined. During a pole-to-ground fault, the voltage of the faulty-pole was observed to reach a zero value, while the healthy pole reaches a new value equal to two times the pre-fault value. However, this pole displacement did not change the pole-to-pole voltage and the transmitted power according to the results. The voltage mutation observed in the poles was following seen in the phase voltage of the intermediate link. A DC component is now present on the AC voltage. Two different cases can be distinguished.

1. First, the three phases of the faulty port end up to a grounding. This can be seen in the examined case 6.4.3 of a pole-to-ground fault taking place in port 3. The results showed that the mutated AC voltage tries to oscillate around zero because of the grounding presence. This behaviour results in instabilities

and loss of the DC hub control.

2. Second, the three phases of the faulty port end up to transformer windings with no grounding. In this case, as no grounding is present, the DC component of the mutated AC voltage will not discharge to the ground. The results have shown that the DC component is now filtered through the transformer. As a result, the DC component does not pass through the transformer and is not affecting the system's operation.

The pole-to-pole fault has fewer probabilities to occur when compared to a pole-to-ground fault, but it is more severe. The stages of the fault were studied. The most expensive and vulnerable components in the MMC are the power semiconductor switches, thus they should be protected from large currents. When a fault is detected, a signal is sent to block the power semiconductor switches. As a result, the fault current flows through the antiparallel diodes. The submodule capacitor discharge stage duration is very small as the turn-off time of the power semiconductors is almost instant. The next stage is the AC transient infeed by the antiparallel diodes. After the fault, the DC link voltage has collapsed. The fault current flows through the arms of the faulty port and large currents are also observed in the intermediate AC link. Different DC hub fault responses were observed depending on the operation of the port. The two following cases can be distinguished:

1. **Port 1 and 2** The simulation results have shown, that when a fault occurs on port 1 or 2, the fault is fed only from port 3. Respectively, in port 1 or 2, high fault currents are not observed and these ports try to continue their normal operation. However, in port 3, who is responsible for the control of the AC voltage, large currents are observed. The fault current is observed to disturb the AC voltage control leading to instabilities. The port 1 and 2 are not affected directly by the fault. The loss of the AC voltage control in the intermediate AC link results in the control loss of all the remaining ports in the DC hub.

2. **Port 3** The second case is when a pole-to-pole fault takes place in port 3, which is responsible for the AC voltage control. The simulation results showed that the DC link of the faulty port collapses and the AC voltage goes to zero. Large DC currents are observed in the two healthy ports enabling the protection system. As a result, the remaining ports are also blocked. The DC hub is now out of operation.

After the pole-to-pole fault analysis, similar conclusions can be made with the previous cases of step reference changes and line connection/disconnection. Port 1 and port 2 operating in DC voltage and active power control had no connection and the operation of the one does not disturb the operation of the other. These two ports have a direct active power control, contrary to the port 3 which has no active power control. For that reason, port 3 feeds the fault. Moreover, the importance of the port responsible to maintain the AC voltage of the intermediate AC link in order to keep a stable operation is observed.

SPECIFY THE DESIGN REQUIREMENTS IN ORDER TO PROVIDE FAULT RIDE-THROUGH FOR DIFFERENT DC FAULT TYPES

After studying the natural fault response of the DC hub, an effort was made to provide fault ride-through for the different DC fault types. To begin with, AC circuit breakers are used to isolate the DC faults. The usual time of AC circuit breakers activation is 2-3 fundamental AC cycles. In the current thesis, the worst case is examined, where the faulty port is disconnected after $60ms$. In order to provide fault ride-through, the system should maintain its operability.

First, a design methodology is proposed to provide fault ride-through for the pole-to-ground faults. The importance of the transformer configuration in the AC link was presented. The use of a (D-Yg) configuration transformer in every port is proposed. The delta winding is located on the converter side. The simulation results have shown that the rest of the ports continue their normal operation without any large currents or voltages present on the system components. Moreover, it was observed that the faulty port also continues its normal operation. After the fault, a pole displacement is observed but the pole-to-pole voltage and the transmission power are maintained constant. The fact that no high arm currents are present and there is no need to block the converters is an important advantage of this topology. Apart from the transformer addition, the DC cables should be dimensioned in order to sustain the temporary overvoltage. The attribute of maintaining the operation of all the ports offers flexibility to the system. In case of a temporary fault, the fault occurrence does not affect the system and the operability is maintained. In case of a permanent fault, the system has time to react. The faulty port controls its power flow to the zero. Next, a smooth disconnection of the faulted line can take place. This is very important in the case where critical loads are supplied.

In the most severe case of a pole-to-pole fault, phase reactors are proposed to be used in order to limit the fault current. DC faults in all the ports were studied. The results showed that the addition of phase reactors between the transformer and the converter can lower the fault peak current. By increasing the size of the inductor, the observed current peak in the arms of the converter lowers. It can be observed that after a certain point the increase of the inductor is not that effective in limiting the fault current.

In the case of the port 1, a $120mH$ phase reactor, equal to $0.335pu$ is added. According to the results, the arm current peak of the port 1 is less than $2.5pu$. This current is conducted by the antiparallel diodes which can be dimensioned for higher than the $2pu$ limit. The arm current of port 2 is not affected by the fault. Observing the arm current of port 3, the peak is lower than $2pu$. The power semiconductor switches can handle this value and the protection scheme is not going to be enabled. Moreover, the AC voltage controlled by port 3 is only affected by a small percentage of $\pm 0.04pu$. This is important because the AC voltage of the intermediate link is stable after the fault and the remaining ports can continue their operation. As far as it concerns the DC currents and voltages of the healthy ports, their values are kept close to the reference values. Port 3 presents a DC voltage ripple of $\pm 0.075pu$ and a DC current ripple less than $\pm 0.5pu$. The duration of these transients is 200ms.

Port 2 presents the same behaviour as port 1. However, in this case, the DC voltage and the port power rating are higher. The design methodology of adding a phase reactor is again proposed. A phase reactor equal to $0.225pu$ is added, this value is equal to $135mH$. At port 3, the values of the arm currents are bellow $4pu$. For that reason, the solution of a phase inductor is not enough. Also, power semiconductor switches should be used in parallel in order to double their maximum current conduction limit. After completing these design requirements, the DC hub can attain a fault ride-through capability. It is observed that the system maintain its operability after the fault occurrence. The intermediate AC link voltage presents a ripple of $\pm 0.1pu$ and returns to the reference value after 120ms. At port 3 the DC voltage presents transients for 300ms, with a maximum ripple of $\pm 0.11pu$. The values of the DC currents stay between the predefined limits.

In the case of port 3, a pole-to-pole fault was seen to lead to the collapse of the intermediate AC voltage and the blocking of all the ports. Efforts were made to change the operation of another port to AC voltage control in order to maintain the AC voltage control of the DC hub. In comparison with the normal case of disconnection, in the fault case, this control change was unsuccessful. The solution of blocking fast not only the faulty but also the remaining ports is proposed. In this way, the arm fault current is limited. In case of a temporary fault, the DC hub restoration can take place after the fault is isolated and all the currents have zero values. This time is calculated to be 300ms. In case of a permanent fault, after 300ms, a new port will be responsible for the AC voltage control.

7.2. FUTURE WORK

Several aspects can be relevant for future study and investigate the other features of MMC based multiport DC-DC converters. Suggestions for future work include:

- The possibility of connecting an AC grid with generation and/or load to the intermediate AC link of the DC hub can be studied.
- In the current thesis, the half-bridge cell configuration is used. The full-bridge or other possible configurations can be a next step for modeling of a multiport DC-DC converter and study the different responses to DC faults.
- As the intermediate AC link is independent of the AC grid, higher frequencies can be used. In this way, a study can take place comparing the trade-off between decreasing the footprint and increasing the loses.
- The trapezoidal waveform can be used instead of the sinusoidal in the AC link. A study can take place comparing the footprint of the two systems.
- A different control approach can be followed in an effort to aid in the fault protection.
- A prototype for laboratory hardware realization should be constructed to test the control of MMC and verify the DC hub operation.

BIBLIOGRAPHY

[1] D. Van Hertem, M. Ghandhari, and M. Delimar, *Technical limitations towards a supergrid—a european prospective,* in *Energy Conference and Exhibition (EnergyCon), 2010 IEEE International* (IEEE, 2010) pp. 302–309.

[2] D. Van Hertem and M. Ghandhari, *Multi-terminal vsc hvdc for the european supergrid: Obstacles,* Renewable and sustainable energy reviews **14**, 3156 (2010).

[3] C. M. Franck, *Hvdc circuit breakers: A review identifying future research needs,* IEEE Transactions on Power Delivery **26**, 998 (2011).

[4] D. Jovcic, D. Van Hertem, K. Linden, J.-P. Taisne, and W. Grieshaber, *Feasibility of dc transmission networks,* in *Innovative Smart Grid Technologies (ISGT Europe), 2011 2nd IEEE PES International Conference and Exhibition on* (IEEE, 2011) pp. 1–8.

[5] Y. Zhang, S. Shi, R. Yang, *et al.*, *Comparison and review of dc transformer topologies for hvdc and dc grids,* in *Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), 2016 IEEE 8th International* (IEEE, 2016) pp. 3336–3343.

[6] C. Barker, C. Davidson, D. Trainer, and R. Whitehouse, *Requirements of dc-dc converters to facilitate large dc grids,* Cigre, SC B4 HVDC and Power Electronics (2012).

[7] J. A. Ferreira, *The multilevel modular dc converter,* in *IEEE Transactions on Power Electronics (Volume: 28, Issue: 10, Oct. 2013* (IEEE, 2013) pp. 4460 – 4465.

[8] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. De Doncker, *Comparison of the modular multilevel dc converter and the dual-active bridge converter for power conversion in hvdc and mvdc grids,* IEEE Transactions on Power Electronics **30**, 124 (2015).

[9] G. J. Kish and P. W. Lehn, *A modular bidirectional dc power flow controller with fault blocking capability for dc networks,* in *Control and Modeling for Power Electronics (COMPEL), 2013 IEEE 14th Workshop on* (IEEE, 2013) pp. 1–7.

[10] A. Schön and M.-M. Bakran, *A new hvdc-dc converter with inherent fault clearing capability,* in *Power Electronics and Applications (EPE), 2013 15th European Conference on* (IEEE, 2013) pp. 1–10.

[11] J. Yang, Z. He, H. Pang, and G. Tang, *The hybrid-cascaded dc–dc converters suitable for hvdc applications,* IEEE Transactions on Power Electronics **30**, 5358 (2015).

[12] H. You and X. Cai, *A family of un-isolated modular dc/dc converters,* in *Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), 2016 IEEE 8th International* (IEEE, 2016) pp. 696–702.

[13] Z. Xing, X. Ruan, H. Xie, and X. Wang, *A modular bidirectional buck/boost dc/dc converter suitable for interconnecting hvdc grids,* in *Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), 2016 IEEE 8th International* (IEEE, 2016) pp. 3348–3354.

[14] R. W. De Doncker, D. M. Divan, and M. H. Kheraluwala, *A three-phase soft-switched high-power-density dc/dc converter for high-power applications,* IEEE transactions on industry applications **27**, 63 (1991).

[15] N. Soltau, H. Stagge, R. W. De Doncker, and O. Apeldoorn, *Development and demonstration of a medium-voltage high-power dc-dc converter for dc distribution systems,* in *Power Electronics for Distributed Generation Systems (PEDG), 2014 IEEE 5th International Symposium on* (IEEE, 2014) pp. 1–8.

[16] D. Jovcic, *Bidirectional, high-power dc transformer,* IEEE transactions on Power Delivery **24**, 2276 (2009).

[17] D. Jovcic and J. Zhang, *High power igbt-based dc/dc converter with dc fault tolerance,* in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International* (IEEE, 2012) pp. DS3b–6.

[18] A. A. J. Far, M. Hajian, D. Jovcic, and Y. Audichya, *High-power modular multilevel converter optimal design for dc/dc converter applications,* IET Power Electronics **9**, 247 (2016).

[19] M. J. Carrizosa, A. Benchaib, P. Alou, and G. Damm, *Dc transformer for dc/dc connection in hvdc network,* in *Power Electronics and Applications (EPE), 2013 15th European Conference on* (IEEE, 2013) pp. 1–10.

[20] S. Kenzelmann, A. Rufer, M. Vasiladiotis, D. Dujic, F. Canales, and Y. R. De Novaes, *A versatile dc-dc converter for energy collection and distribution using the modular multilevel converter,* in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on* (Ieee, 2011) pp. 1–10.

[21] I. Gowaid, G. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. Williams, *Quasi two-level operation of modular multilevel converter for use in a high-power dc transformer with dc fault isolation capability,* IEEE Transactions on Power Electronics **30**, 108 (2015).

[22] C. Davidson and D. Trainer, *Innovative concepts for hybrid multi-level converters for hvdc power transmission,* (2010).

[23] G. P. Adam, S. Finney, B. Williams, D. Trainer, C. Oates, and D. Critchley, *Network fault tolerant voltage-source-converters for high-voltage applications,* (2010).

[24] M. M. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, R. Critchley, W. Crookes, and F. Hassan, *The alternate arm converter: A new hybrid multilevel converter with dc-fault blocking capability,* IEEE transactions on power delivery **29**, 310 (2014).

[25] C. Oates, K. Dyke, and D. Trainer, *The use of trapezoid waveforms within converters for hvdc,* in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on* (IEEE, 2014) pp. 1–10.

[26] I. Gowaid, G. Adam, B. Williams, A. Massoud, and S. Ahmed, *The transition arm multilevel converter—a concept for medium and high voltage dc-dc transformers,* in *Industrial Technology (ICIT), 2015 IEEE International Conference on* (IEEE, 2015) pp. 3099–3104.

[27] D. Jovcic and W. Lin, *Multiport high-power lcl dc hub for use in dc transmission grids,* IEEE Transactions on Power Delivery **29**, 760 (2014).

[28] R. Li, Z. Wang, D. Holliday, L. Yao, and B. Williams, *Dc transformer based on hybrid cascaded mmc in multi-terminal hvdc transmission system,* (2016).

[29] W. Xiang, W. Lin, L. Miao, and J. Wen, *Power balancing control of a multi-terminal dc constructed by multiport front-to-front dc–dc converters,* IET Generation, Transmission & Distribution **11**, 363 (2017).

[30] A. Yazdani and R. Iravani, *Voltage-sourced converters in power systems: modeling, control, and applications* (John Wiley & Sons, 2010).

[31] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems* (John Wiley & Sons, 2016).

[32] A. Lesnicar and R. Marquardt, *An innovative modular multilevel converter topology suitable for a wide power range,* in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, Vol. 3 (IEEE, 2003) pp. 6–pp.

[33] L. Harnefors, A. Antonopoulos, S. Norrga, L. Angquist, and H.-P. Nee, *Dynamic analysis of modular multilevel converters,* IEEE Transactions on Industrial Electronics **60**, 2526 (2013).

[34] J. Bjorn, K. Patrik, A. Gunnar, H. Lennart, J. Tomas, and A. Sweden, *Vsc-hvdc transmission with cascaded two-level converters,* (2011).

[35] Z. Xu, H. Xiao, and Z. Zhang, *Selection methods of main circuit parameters for modular multilevel converters,* IET Renewable Power Generation **10**, 788 (2016).

[36] G. Bergna Diaz, *Modular Multilevel Converter Control for HVDC Operation. Optimal Shaping of the Circulating Current Signal for Internal Energy Regulation,* , 239 (2015).

[37] Y. Ma, L. Fan, and Z. Miao, *Integrated control and switching strategy for a grid-connected modular multilevel converter,* in *Power & Energy Society General Meeting, 2015 IEEE* (IEEE, 2015) pp. 1–5.

[38] L. Harnefors and H.-P. Nee, *Model-based current control of ac machines using the internal model control method,* IEEE transactions on industry applications **34**, 133 (1998).

[39] R. T. Pinto, *Multi-terminal DC networks: System integration, dynamics and control,* Ph.D. thesis, CPI Koninklijke Wöhrmann (2014).

[40] L. Harnefors, M. Bongiorno, and S. Lundberg, *Input-admittance calculation and shaping for controlled voltage-source converters,* IEEE transactions on industrial electronics **54**, 3323 (2007).

[41] N. Ahmed, L. Ängquist, S. Mahmood, A. Antonopoulos, L. Harnefors, S. Norrga, and H.-P. Nee, *Efficient modeling of an mmc-based multiterminal dc system employing hybrid hvdc breakers,* IEEE Transactions on Power Delivery **30**, 1792 (2015).

[42] N. Ahmed, L. Ängquist, S. Norrga, A. Antonopoulos, L. Harnefors, and H.-P. Nee, *A computationally efficient continuous model for the modular multilevel converter,* IEEE Journal of Emerging and Selected Topics in Power Electronics **2**, 1139 (2014).

[43] W. Leterme, N. Ahmed, J. Beerten, L. Ängquist, D. Van Hertem, and S. Norrga, *A new hvdc grid test system for hvdc grid dynamics and protection studies in emt-type software,* (2015).

[44] T. Luth, *DC/DC converters for high voltage direct current transmission*, Ph.D. thesis, Imperial College London (2014).

[45] D. Jovcic and H. Zhang, *Optimal control and dc fault ride-through of transmission level, mmc-based, isolated dc/dc converter,* in *Power and Energy Society General Meeting (PESGM), 2016* (IEEE, 2016) pp. 1–5.

[46] O. Heyman and ABB, *HVDC Light ® It's time to connect,* (2012).

[47] S. Rodrigues, C. Restrepo, E. Kontos, R. T. Pinto, and P. Bauer, *Trends of offshore wind projects,* Renewable and Sustainable Energy Reviews **49**, 1114 (2015).

[48] J. Wang, A. C. Liew, and M. Darveniza, *Extension of dynamic model of impulse behavior of concentrated grounds at high currents,* IEEE Transactions on Power Delivery **20**, 2160 (2005).

[49] M. K. Bucher and C. M. Franck, *Contribution of fault current sources in multiterminal hvdc cable networks,* IEEE Transactions on Power Delivery **28**, 1796 (2013).

[50] J. Yang, J. E. Fletcher, and J. O'Reilly, *Short-circuit and ground fault analyses and location in vsc-based dc network cables,* IEEE transactions on Industrial Electronics **59**, 3827 (2012).

[51] L. Tang and B.-T. Ooi, *Locating and isolating dc faults in multi-terminal dc systems,* IEEE Transactions on Power Delivery **22**, 1877 (2007).

[52] K. Linden, B. Jacobson, M. Bollen, and J. Lundquist, *Reliability study methodology for hvdc grids,* in *CIGRE Sessions: 22/08/2010-27/08/2010* (2010).

[53] J. Yang, J. E. Fletcher, and J. O'Reilly, *Multiterminal dc wind farm collection grid internal fault analysis and protection design,* IEEE Transactions on Power Delivery **25**, 2308 (2010).

[54] *Export transmission cables for offshore renewable installations principles for cable routing and spacing.* Revision 1.0Ł (2012).

[55] *Third-party damage to underground and submarine cables,* Conseil international des grands reseaux electriques B1 (2009).

[56] X. Chen, C. Zhao, and C. Cao, *Research on the fault characteristics of hvdc based on modular multilevel converter,* in *Electrical Power and Energy Conference (EPEC), 2011 IEEE* (IEEE, 2011) pp. 91–96.

[57] W. Leterme, J. Beerten, and D. Van Hertem, *Equivalent circuit for half-bridge mmc dc fault current contribution,* in *Energy Conference (ENERGYCON), 2016 IEEE International* (IEEE, 2016) pp. 1–6.