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A 280 μW Dynamic Zoom ADC With 120 dB DR and 118 dB SNDR in 1 kHz BW

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***Abstract*— This paper presents a dynamic zoom analog-to-digital converter for use in low-bandwidth (<1 kHz) instrumentation applications. It employs a high-speed asynchronous successive approximation register (SAR) ADC that dynamically updates the references of a fully differential ΔΣ ADC. Compared to previous zoom ADCs, faster reference updates relax the loop filter requirements, thus allowing the adoption of energy-efficient amplifiers. Fabricated in a 0.16-μm CMOS process, the prototype occupies 0.26 mm^2 and achieves 119.1-dB peak signal-to-noise ratio (SNR), 118.1-dB peak signal-to-noise-and-distortion-ratio (SNDR), and 120.3-dB dynamic range (DR) in a 1-kHz bandwidth while consuming 280 μW. This results in a Schreier figure of merit (FoM) of 185.8 dB.**

***Index Terms*— A/D conversion, asynchronous successive approximation register analog-to-digital converter, battery-powered applications, delta–sigma ADC, dynamic zoom ADC, inverter-based operational transconductance amplifier (OTA), low-power circuits.**

I. Introduction

SLOWLY changing signals, with bandwidths below 1–2 kHz, are often encountered in several applications, such as sensor interfaces, biomedical signal processing, and industrial instrumentation. The amplitude of such signals may vary considerably, ranging from a few microvolts to a few volts, and so analog-to-digital converters (ADCs) are intended for such applications that require wide dynamic range (DR) (>above 120 dB, i.e., 20-bit resolution) and high linearity. Since many of these applications involve battery-powered systems, such as wearable medical devices and portable instruments, such ADCs should also be extremely energy efficient with a power consumption less than a milliwatt. Linearity requirements in such applications also necessitate an integral non-linearity (INL) within a few parts-per-million (ppm), translating into a signal-to-noise-and-distortion-ratio (SNDR) similar to the DR.

Successive approximation register (SAR) ADCs are well known for their excellent energy efficiency but their resolution is typically limited to about 12 bits unless extensive calibration and trimming are applied [1]–[3]. ΔΣ ADCs can achieve much higher resolution thanks to oversampling and noise shaping. However, high-order ΔΣ modulators (ΔΣMs) and multi-bit ΔΣMs, as typically employed to achieve high DR, are not energy efficient. This is due to the use of higher oversampling ratio (OSR) and multiple integrators in a single-bit high-order ΔΣM or a power-hungry flash quantizer in a multi-bit ΔΣM. Similarly, MASH architectures can achieve a high DR with a low OSR but often rely on the matching of internal analog and digital transfer functions and may require extensive calibration [4], [5]. Incremental ΔΣMs, in which the modulator is reset at the start of each conversion, have been widely used for high-DR applications, but they are typically limited to extremely low bandwidths [6], [7]. Energy-efficient designs such as multi-step incremental ΔΣMs rely on hardware reuse and extended counting to achieve a DR of around 100 dB within a 1-kHz BW [8], [9].

Hybrid ADCs attempt to optimally combine the strengths of various ADC architectures to obtain performance levels not achievable with a single architecture [10]–[14]. The zoom ADC [13], [14] is a hybrid ADC which combines a SAR ADC and a ΔΣM to achieve both high resolution and high energy efficiency. A SAR ADC is first used to make a low-resolution coarse conversion, which is then used to adjust the references of a ΔΣM, and thus zoom-in on the signal. The incremental zoom ADC in [13] performs these two operations sequentially and achieves a 119.8-dB DR for pseudo-dc input signals. However, due to its sequential operation, its bandwidth is limited to only 12.5 Hz. The dynamic zoom ADC in [14] overcomes this limitation by operating the SAR ADC and ΔΣM concurrently, allowing it to handle audio signals. Its use of a 5-bit synchronous SAR ADC, however, meant that the references of the ΔΣM are only updated once every five clock cycles. This makes it vulnerable to the fast out-of-band interferers, which can then overload the ΔΣM.

This paper describes a dynamic zoom ADC that uses an asynchronous SAR to update the ΔΣM references every clock cycle [15], thus improving its tracking capability and its robustness to the out-of-band interferers. This choice also relaxes the loop-filters input swing, thus allowing it to be realized in an energy-efficient manner.

This paper is organized as follows. Section II provides a brief introduction to the dynamic zoom ADC architecture. Section III highlights the advantages of using an asynchronous SAR ADC and describes the system design of the ADC. Sources of errors are discussed along with techniques

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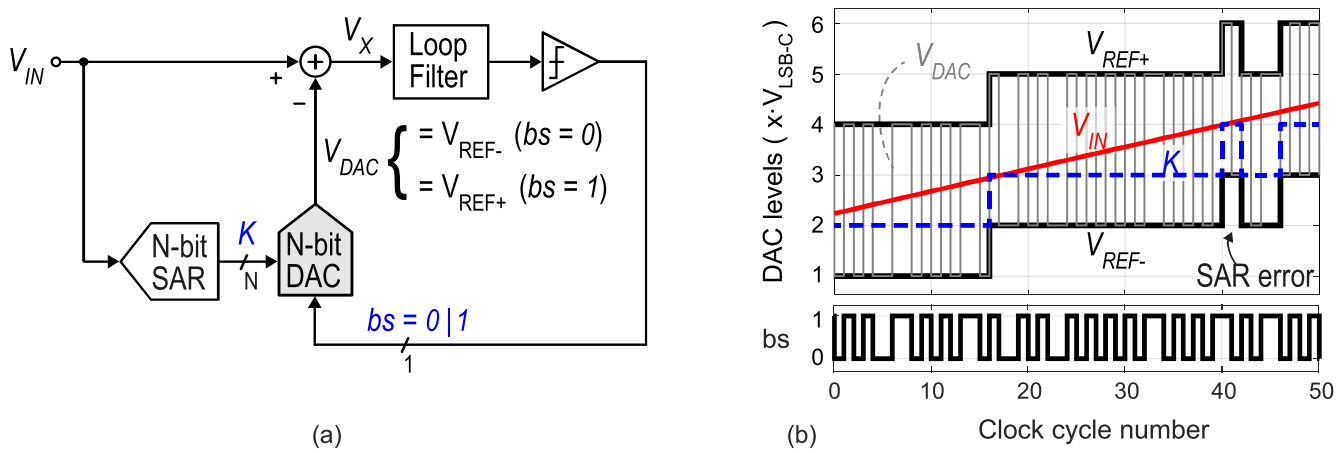

Fig. 1. (a) Simplified block diagram of the dynamic zoom ADC. (b) Time-domain waveforms of different signals in the zoom ADC with an over-ranging of $M = 1$.

to mitigate them. Section IV discusses the circuit implementation, and Section V is devoted to the experimental results. Finally, the conclusion is presented in Section VI.

II. Zoom ADC Architecture

A dynamic zoom ADC, as shown in Fig. 1(a), consists of an N-bit SAR ADC, which performs a coarse conversion and outputs an N-bit code K. This digital value K is used to determine the high and low references for the $\Delta\Sigma$M, respectively, as

$$V_{\mathrm{REF+}} = (K + 1 + M) \cdot V_{\mathrm{LSB},C} \tag{1}$$

$$V_{\mathrm{REF-}} = (K - M) \cdot V_{\mathrm{LSB},C} \tag{2}$$

where $V_{\mathrm{LSB},C}$ is the quantization step size corresponding to the N-bit SAR and M is the over-ranging factor. An N-bit digital-to-analog converter (DAC) is used to generate these fine references. The $\Delta\Sigma$M DAC toggles between these references depending on the bitstream output of the comparator bs, as in a conventional $\Delta\Sigma$M, essentially zooming-in on the signal and achieving a signal-to-quantization-noise ratio (SQNR) significantly higher than a conventional 1-bit $\Delta\Sigma$M. Fig. 1(b) shows the resulting signals in the case of $M = 1$.

If $M = 0$, no error can be tolerated in the coarse SAR conversion since a conversion error would lead to the $\Delta\Sigma$M references not straddling the input signal, thus leading to $\Delta\Sigma$M overload. Over-ranging, i.e., making $M > 0$, is used to reduce the accuracy requirements of the SAR ADC [14]. As the SAR ADC uses a separate capacitive DAC, its quantization levels will exhibit some mismatch with respect to those of the main DAC used by the $\Delta\Sigma$M to set the fine references. Any error made by the SAR ADC due to its noise, linearity, and offset will result in an error in the coarse code K. Without over-ranging, the overall accuracy of the zoom ADC would, therefore, be limited by both the SAR ADC and $\Delta\Sigma$M DAC. Over-ranging ensures that the fine references of the $\Delta\Sigma$M are still valid for a given input as long as the error in the SAR conversion is below M LSBs. Thus, the SAR ADC does not limit the overall accuracy. This is illustrated in Fig. 1(b), where despite the error in K, the input remains bounded by the fine references. It must be noted that although over-ranging relaxes the SAR ADC constraints, the main N-bit DAC must still be designed to achieve the intended resolution of 20 bits.

The relaxed requirements on the SAR ADC due to over-ranging greatly simplify its design. Furthermore, zooming reduces the swing at the input of the loop filter, relaxing the linearity and driving requirements of the $\Delta\Sigma$M integrators, thus allowing the use of simple energy-efficient inverter-based operational transconductance amplifiers (OTAs).

III. System-Level Analysis

A. Maximum Input Frequency and Over-Ranging

Over-ranging also plays a role in defining the maximum input signal frequency that a dynamic zoom ADC can tolerate. In [14], a conventional synchronous N-bit SAR ADC is constantly running in the background. Since it takes N cycles to calculate and update the coarse code K, and as this is then used for the next N cycles before it is updated again, an input signal is not allowed to swing beyond the fine references determined by K for $2N$ cycles. This is illustrated in Fig. 2(a) for a fast-changing input and a dynamic zoom ADC with $N = 5$ and an over-ranging $M = 2$. The N-cycle delay between every input sampled by the SAR ADC and the corresponding update in K (indicated by the red "×" and blue "dot" pairs) makes it difficult for the dynamic zoom ADC to track such signals. This inability to track high-frequency signals or interferers deteriorates its in-band performance, limiting its use to applications, where out-of-band inputs are not expected or requiring the use of a low-pass filter to attenuate them [14]. Tracking limitations can be improved by increasing the over-ranging. Higher M means that the input signal has more room to transition before reaching the limits set by the fine references, as illustrated in Fig. 2(b). To tackle an input signal as fast as the one shown in Fig. 2(a), the over-ranging could be increased from $M = 2$ to $M = 4$. However, a higher over-ranging also means an increased swing at the inputs of the $\Delta\Sigma$M loop filter [V_X in Fig. 1(a)], which can be expressed as

$$V_X = V_{\mathrm{IN}} - V_{\mathrm{DAC}} = K \cdot V_{\mathrm{LSB},C} + Q_E - V_{\mathrm{DAC}} \tag{3}$$

where Q_E is the coarse SAR ADC quantization error, and V_{DAC} is the output of the $\Delta\Sigma$M feedback DAC. As V_{DAC} can

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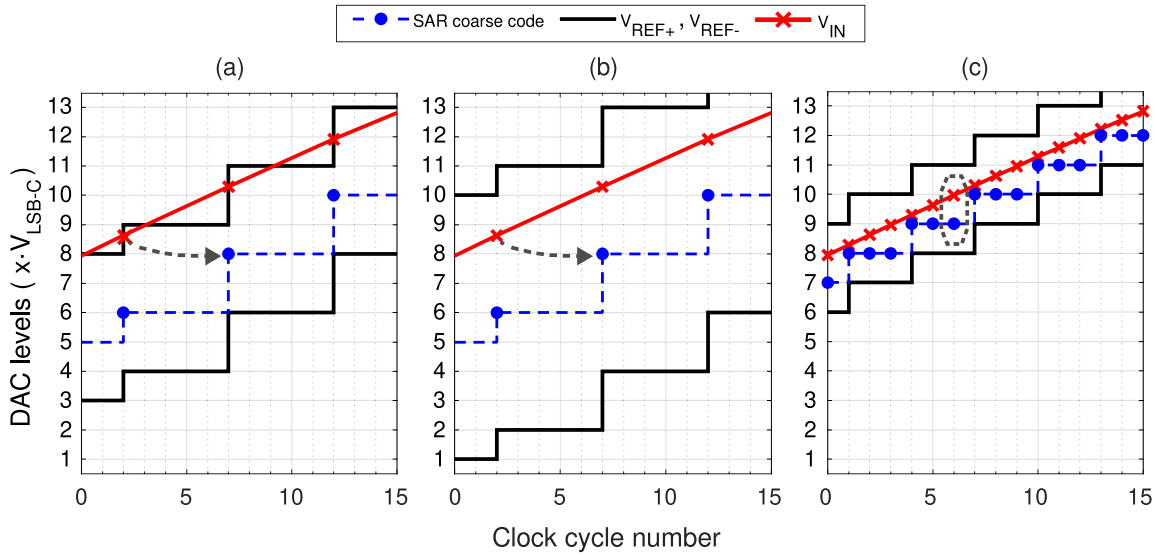

Fig. 2. Time-domain operation of the dynamic zoom ADC for a fast-changing input. (a) Coarse code (and corresponding fine reference) updated every N cycles by an N-bit SAR, for the case $N = 5$ and over-ranging $M = 2$. (b) Same conditions as in (a), but with an over-ranging of $M = 4$. (c) Coarse code (and corresponding fine reference) updated every cycle by an N-bit asynchronous SAR, with an over-ranging of $M = 1$.

be either $V_{\mathrm{REF+}}$ or $V_{\mathrm{REF-}}$ depending on the output of the comparator, V_X can have a maximum value $V_{X,\mathrm{MAX}}$, given as

$$V_{X,\mathrm{MAX}} = (1+M)\cdot V_{\mathrm{LSB},C} = (1+M)\cdot \frac{V_{\mathrm{REF,FS}}}{2^N-1} \tag{4}$$

where $V_{\mathrm{REF,FS}}$ is the full scale of the zoom ADC. This shows that the loop filter input increases for a larger over-ranging M and a lower coarse resolution N. In a switched-capacitor circuit, an amount of charge proportional to the swing V_X is transferred to the loop filter input capacitors. The OTAs used to implement the integrators in the loop filter must provide this charge with certain settling accuracy. If the swing at the loop filter input is smaller, this can be achieved with less current, hence with less total power consumption. For high energy efficiency, it is, therefore, necessary to keep the over-ranging as low as possible.

For a $\Delta\Sigma$M operating with the fine references defined in (1) and (2), its maximum stable input range may be defined as

$$V_{\Delta\Sigma,\mathrm{MAX}} < \alpha\cdot(V_{\mathrm{REF+}} - V_{\mathrm{REF-}}) \tag{5}$$

where $\alpha \leq 1$ is a modulator topology-dependent parameter defining its stable input range. The maximum input signal transition ΔV_{IN} for a sinusoidal input with frequency f_{IN}, within a certain period Δt (assuming $\Delta t \ll 1/f_{\mathrm{IN}}$) for a full-scale input amplitude occurs at their zero-crossings and can be approximated as

$$\Delta V_{\mathrm{IN}} \approx A_{\mathrm{MAX}}\cdot 2\pi f_{\mathrm{IN}}\Delta t = \frac{V_{\mathrm{REF,FS}}}{2}\cdot\left(2\pi f_{\mathrm{IN}}\frac{n}{f_S}\right) \tag{6}$$

where n represents Δt in terms of clock cycles. As the fine references are updated to ensure that a sampled input is centered between them, the above-mentioned input signal transition is constrained as

$$\Delta V_{\mathrm{IN}} < \left(\frac{V_{\Delta\Sigma,\mathrm{MAX}}}{2}\right). \tag{7}$$

In the case in [14], this constraint holds for $n = 2N$ cycles, which effectively translates into a maximum input frequency of $f_{\mathrm{IN,MAX}}$ of

$$f_{\mathrm{IN,\,MAX}} = \frac{\alpha\cdot(M+0.5)\cdot f_S}{2N\cdot\pi\cdot(2^N-1)}. \tag{8}$$

In this paper, the faster tracking of high-frequency interferers is achieved by increasing the update rate of the reference. This is accomplished by using an asynchronous SAR ADC instead of the conventional N-cycle SAR ADC. An asynchronous SAR ADC calculates the N-bit output code in a fraction of the clock period, as explained in Section IV-C, updating the fine references and allowing it to be used in the same cycle. This cycle-by-cycle update of the fine references implies that the input only has to stay within the bounds of the fine reference for the duration of one cycle. This increases the maximum tolerable input frequency in (8) as

$$f'_{\mathrm{IN,\,MAX}} = \frac{\alpha\cdot(M+0.5)\cdot f_S}{\pi\cdot(2^N-1)} \tag{9}$$

increasing the maximum tolerable input frequency by a factor of $2N$. This change also makes it possible to reduce M to the bare minimum required to tolerate the inaccuracies of the SAR ADC. Although the power required by an asynchronous SAR will be N times than that of a synchronous design, it is negligible compared to the power dissipated in the loop filter and the digital back end. Furthermore, the lower swing requirements on the integrators allow the use of simpler amplifiers, thus reducing the power consumption of the loop filter.

B. Loop Filter Order, Coarse Resolution, and OSR

To ensure a thermal noise-limited SNR, the target for SQNR is kept higher than 140 dB. Fig. 3 shows the variation of peak SQNR with different combinations of loop filter order and coarse resolution with an increasing sampling frequency.

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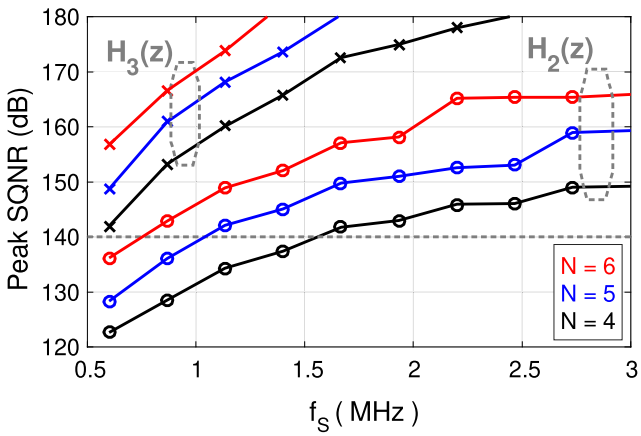

Fig. 3. SQNR versus sampling frequency f_S for a second- and third-order loop filters employing a 4-, 5-, or 6-bit asynchronous SAR ADC as the coarse quantizer with an over-ranging of $M = 1$ on the fine references.

Since this paper targets precision applications, a discrete-time loop filter is chosen over its continuous-time counterpart for the inherent advantages it offers, especially in terms of process spread and jitter immunity. However, a discrete-time loop filter suffers from the sampled thermal noise, mainly dominated by the input-stage sampling capacitors. The strict linearity requirement necessitates the use of metal capacitors that have the drawback of low density. Thus, they can be quite large at low OSRs. An OSR of 1000 ($f_S = 2$ MHz) is chosen to achieve a 120-dB DR while using reasonably sized capacitors. As seen in the plot, every configuration exceeds the target SQNR of 140 dB at $f_S = 2$ MHz, so that a third-order loop filter is unnecessary. With a second-order loop filter, coarse resolutions above $N = 4$ offer sufficient SQNR when an over-ranging of $M = 1$ is used. Using $M = 1$, the loop filter input swing for $N = 4$ is approximately twice than that of $N = 5$ [see (4)], leading to a proportional increase in the loop filter power consumption to maintain linearity. While the loop filter can achieve even lower swing for $N = 6$, the maximum tolerable input frequency of the zoom ADC decreases [see (9)] and the accuracy requirements of the SAR ADC increases [10], requiring an increase in over-ranging. Furthermore, since a dynamic element matching (DEM) algorithm is used in the digital back end for the DAC, as explained in Section III-E, its power consumption for $N = 6$ will be approximately double that for $N = 5$, which is quite significant in the chosen 160-nm technology. To prevent carry overflow while combining K and bs, K is constrained to lie between 1 and 29.

For the above-mentioned reasons, a coarse resolution of $N = 5$ is used in this design, for an optimum tradeoff between power consumption, tracking capability, and SAR ADC requirements.

C. Linearity Relaxation and Out-of-Band Fuzz

The zoom ADC can be modeled as shown in Fig. 4(a), where the SAR ADC serves as a direct input feed forward to the digital output. The feed-forward loop filter used in Section III-B is adopted here. The $\Delta\Sigma$M DAC can be split into two ideal DACs: one N-bit DAC that tracks the input using the coarse code K and another 1-bit DAC with levels $-1 \cdot V_{\mathrm{LSB},C}$ and $2 \cdot V_{\mathrm{LSB},C}$. Since the input to the loop filter $Q1(z)$ is basically the quantization error of the SAR ADC, the loop filter does not process the signal, as shown in the spectrum in Fig. 4(b), relaxing the linearity requirements of its integrators to a significant extent. It should be noted that splitting the N-bit DAC into two separate DACs is purely conceptual; the actual implementation consists of a single N-bit DAC.

Due to the way the digital logic processes the outputs of the SAR ADC and the $\Delta\Sigma$M, some residual out-of-band fuzz is visible in Fig. 4(b). Observing Fig. 4(a), one can write the outputs of the SAR ADC and the $\Delta\Sigma$M in the z-domain as

$$Y_{\mathrm{SAR}}(z) = X(z) - Q1(z) \tag{10}$$

$$Y_{\Delta\Sigma M}(z) = Q1(z) \cdot STF + Q2(z) \cdot \mathrm{NTF} \tag{11}$$

$$Y_{\mathrm{OUT}}(z) = X(z) + Q1(z) \cdot (\mathrm{STF\text{-}1}) + Q2(z) \cdot \mathrm{NTF} \tag{12}$$

where $Q1(z)$ is the quantization noise of the coarse SAR ADC, $Q2(z)$ is the quantization noise of the 1-bit comparator in the $\Delta\Sigma$M, and STF and NTF are the signal and noise transfer functions of the $\Delta\Sigma$M, respectively. Due to the feed-forward nature of the second-order loop filter, the STF exhibits some peaking and deviates from 1, which causes an imperfect cancellation of the SAR ADC quantization noise $Q1(z)$ out of band. The fuzz shown in Fig. 4(b) is a result of the imperfect cancellation of the SAR ADC's quantization error, which is characterized by the high-frequency tonal content. Since it depends only on the STF of the $\Delta\Sigma$M and the input signal amplitude, the fuzz is a time-independent signal processing artifact and can thus be compensated by a fixed filter.

As in MASH architectures, the fuzz can be tackled in the digital domain. Before combining it with the bitstream output, the SAR ADC's output code can be processed by a digital filter with a transfer function equal to the STF of the $\Delta\Sigma$M, as shown in Fig. 5(a). The combined output spectrum before and after digital processing to remove the fuzz is shown in Fig. 5(b).

D. SAR ADC Requirements

As explained earlier, over-ranging relaxes all the constraints on the SAR ADC, such as noise, offset, and linearity. Due to the use of $1 - V_{\mathrm{LSB\text{-}C}}$ over-ranging, the total errors of the SAR should be limited to 1 $V_{\mathrm{LSB\text{-}C}}$. A coarse quantization error, however, reduces the residual over-ranging and consequently lowers the maximum tolerable frequency. This changes (9) to

$$f''_{\mathrm{IN,\,MAX}} = \frac{\alpha \cdot (M + 0.5 - \epsilon) \cdot f_S}{\pi \cdot (2^N - 1)} \tag{13}$$

where $\epsilon = \sigma_{(\mathrm{LSB\text{-}C})}/V_{\mathrm{LSB\text{-}C}}$ is the standard deviation of the total combined error in the SAR ADC's quantization levels, when normalized to 1 $V_{\mathrm{LSB,C}}$. For a 5-bit converter, $\epsilon = 10\%$ translates roughly to an accuracy of 7 bit and decreases the maximum tolerable frequency by 10%. For this design, a 7-bit accurate SAR ADC is chosen so as to not deteriorate the overall performance of the zoom ADC while not requiring excessive power and area in the SAR ADC. The simulated offset of the SAR comparator is 0.1 $V_{\mathrm{LSB\text{-}C}}$ while the rest of

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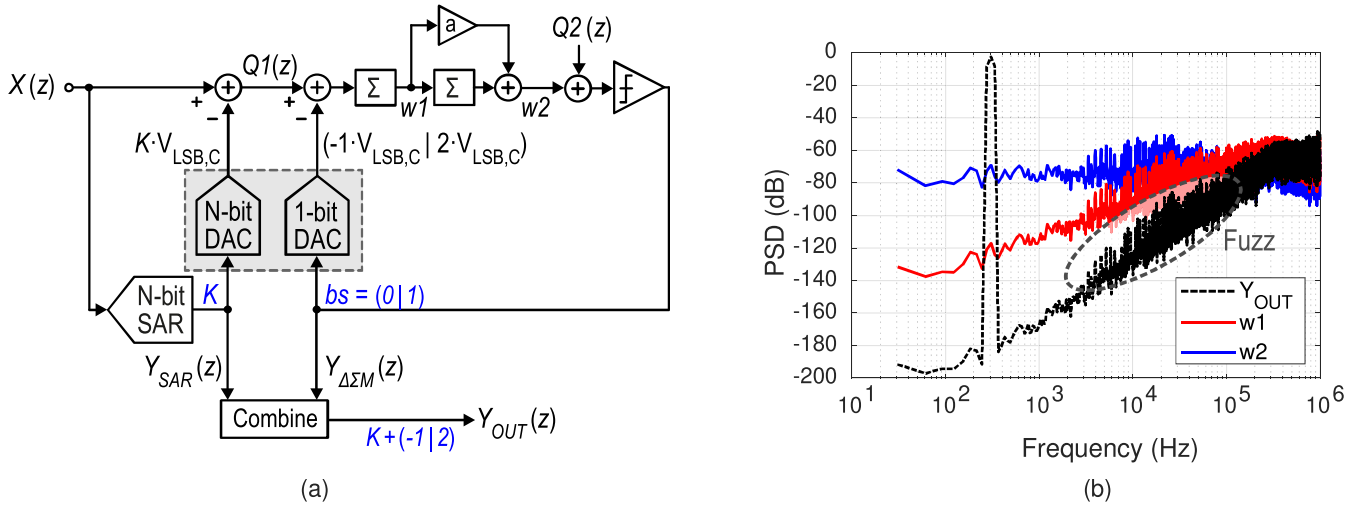

Fig. 4. (a) Intuitive block diagram of the coarse-fine operation of the N-bit DAC. (b) Spectrum at internal nodes of the loop filter and the output of zoom ADC when $N = 5$ and $M = 1$.

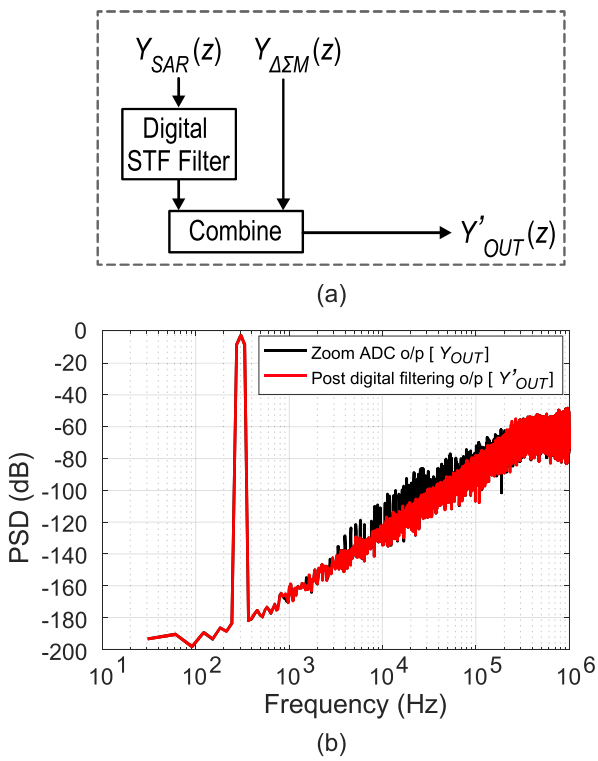

Fig. 5. (a) Fuzz filtering using a digitally matched STF filter. (b) Its effect on the zoom ADC output spectrum.

the error budget is used for noise and linearity. No calibration is used.

E. DAC

The SNDR of the zoom ADC needs to be above 120 dB and it is limited by the fine references generated by the N-bit DAC. While the unit capacitors used to implement the DAC are much larger than the SAR DACs, their mismatch limits the resolution to the 13-bit level. This issue is resolved using data-weighted averaging (DWA) [16]. For an expected spread of $\sigma_C/C = 0.3\%$ in the unit elements, simulations indicate that an OSR of 1000 provides a sufficiently low DWA noise.

IV. Implementation Details

Fig. 6 shows a simplified system-level diagram of the dynamic zoom ADC comprising a 5-bit asynchronous SAR, a 5-bit DAC, and a second-order feed-forward loop filter. The zoom ADC operates with an over-ranging of $M = 1$ and an OSR of 1000. A feed-forward loop filter is chosen to avoid the power consumption of a second DAC in the case of a feedback loop filter. The coefficients were optimized considering the stability of the loop filter, the output swing of the integrators, and corresponding capacitor sizes.

A. $\Delta\Sigma M$

Fig. 7(a) shows the circuit-level implementation of the fully differential discrete-time second-order $\Delta\Sigma$M. The input sampling capacitors also serve as the feedback DAC. It is built from 31 unit elements with a value $C_{\mathrm{DAC}}[\mathrm{J}] = 438$ fF to form an overall sampling capacitance $C_S = \sum C_{\mathrm{DAC}}[\mathrm{J}] = 13.6$ pF. This value, together with the OSR, determines the thermal noise level of the zoom ADC. Metal fringe capacitors have been used to implement the unit elements due to their high linearity and good matching. The integration capacitor of the first stage is sized to have a tolerable swing at that output of OTA1 and has a value $C_{\mathrm{INT},1} = 9$ pF. During sampling phase $\varphi 1$, all the units are shorted, and the input is effectively sampled on C_S; during $\varphi 2$, the digital back end converts the 5-bit DAC code to a 31-bit thermometer code, which is presented to the DAC switches after DWA to generate the appropriate feedback voltage.

A correlated-double-sampling (CDS) scheme is implemented to suppress the offset of OTA1 [17]. While the input is shorted to the outer plate of C_S during phase $\varphi 1$, OTA1 is connected in unity feedback and samples its own offset and $1/f$ noise on the other plate. During $\varphi 2$, this offset is effectively canceled while the input gets integrated. Due to the finite

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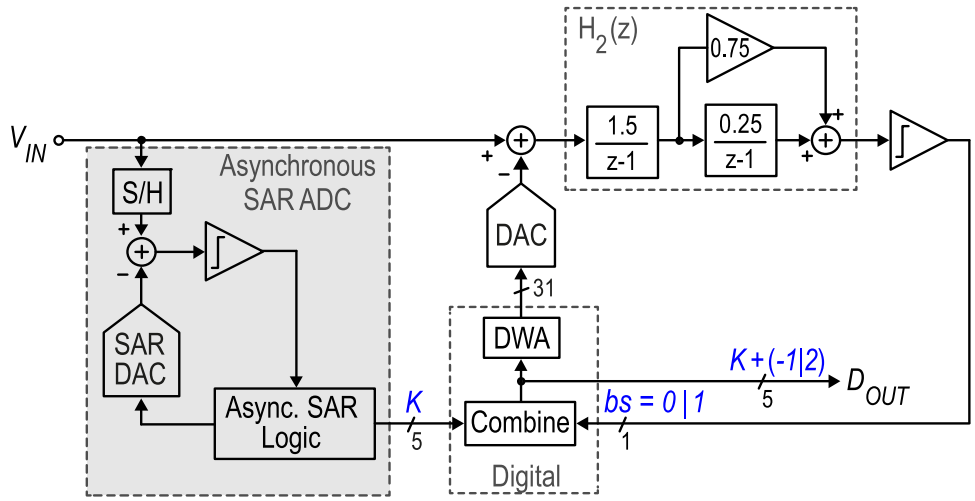

Fig. 6. Dynamic zoom ADC employing 1-bit second-order modulator with a coarse 5-bit asynchronous SAR quantizer.

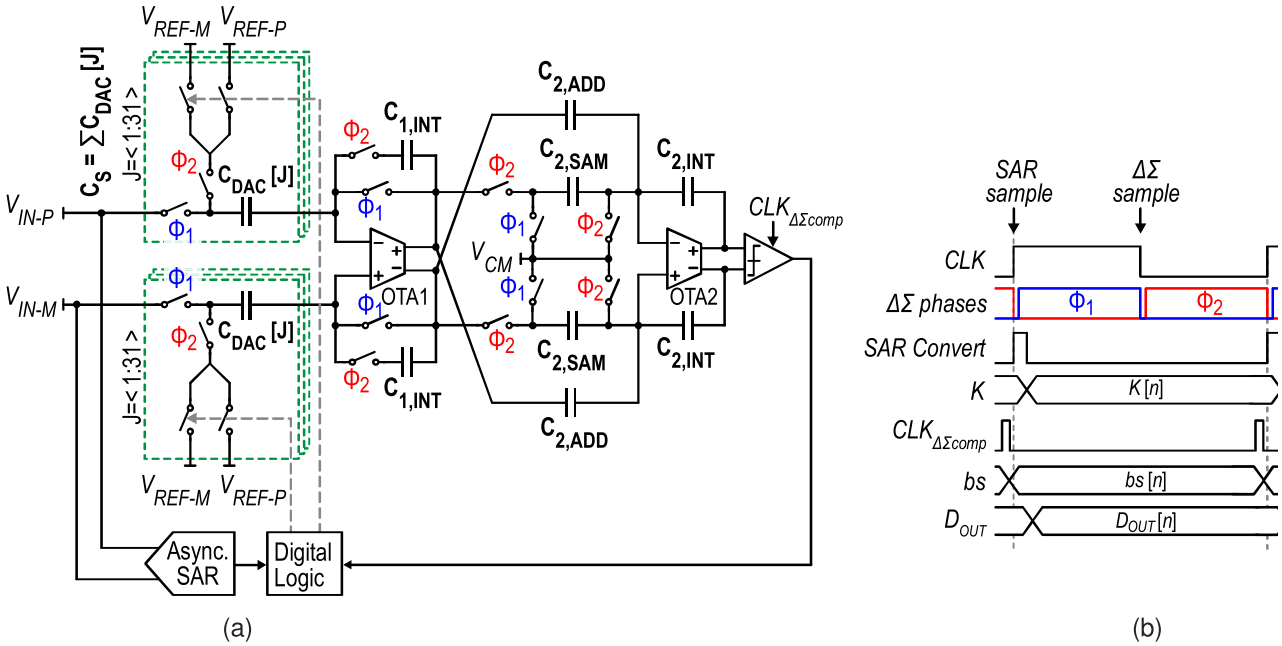

Fig. 7. (a) Simplified schematic of the dynamic zoomADC. (b) Timing diagram of the zoom ADC.

dc gain of OTA1, the offset sampled at the virtual ground node due to unity feedback is $V_{\mathrm{OFF}} \cdot A/(1+A)$. As a result, an input-referred offset of approximately V_{OFF}/A remains. A typical offset of a few millivolts gets suppressed to microvolts if the OTA gain is around 60 dB.

The size of the capacitors of the second stage can be very relaxed thanks to the high gain of the first stage. Hundred times smaller capacitors would mean that the corresponding thermal noise is 20-dB worse. However, thanks to the 60-dB gain of OTA1, the resulting input-referred noise floor is still 40 dB below the dominant thermal noise. In this case, the capacitance values are mainly limited by matching. $C_{\mathrm{SAM},2}$, $C_{\mathrm{ADD},2}$, and $C_{\mathrm{INT},2}$ are 150, 450, and 600 fF, respectively. On a similar note, the offset and $1/f$ noise of OTA2 and the comparator are also suppressed by the gain of their preceding stages. $C_{\mathrm{ADD},2}$ and $C_{\mathrm{INT},2}$ together form a continuous-time proportional path in parallel to the discrete-time integral path ($C_{\mathrm{SAM},2}$ and $C_{\mathrm{INT},2}$) and is used to implement the feed-forward coefficient without additional capacitors or switches.

Fig. 7(b) shows the timing diagram of the dynamic zoom ADC. The sampling instants of the SAR ADC and the $\Delta\Sigma$M are kept half clock cycle apart to minimize the coupling between them via the input terminal.

The digital logic consists of a binary-to-unary converter followed by the DWA logic to generate the signals for each of the 31 $\times$ 2 unit elements from a 5-bit binary value. These two blocks together make up the dominant source of power consumption in the digital back end.

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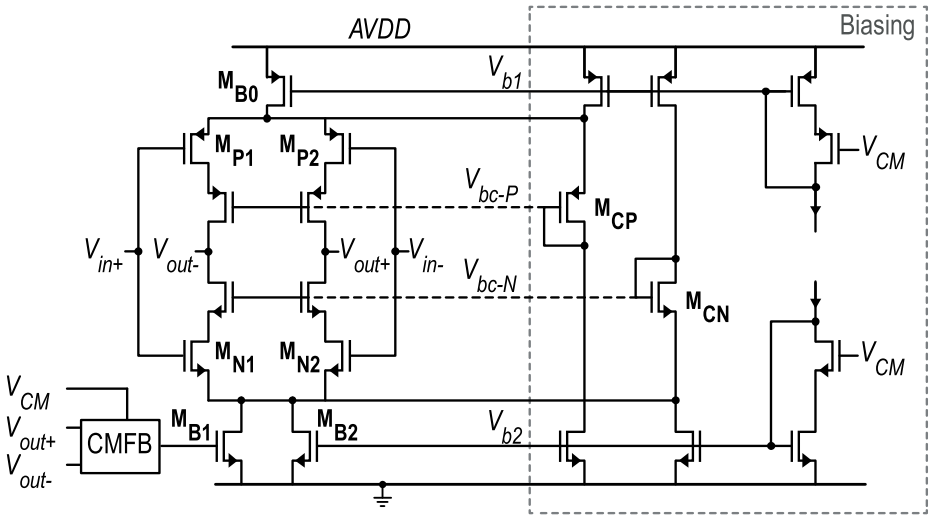

Fig. 8. Schematic of the current-starved inverter OTAs.

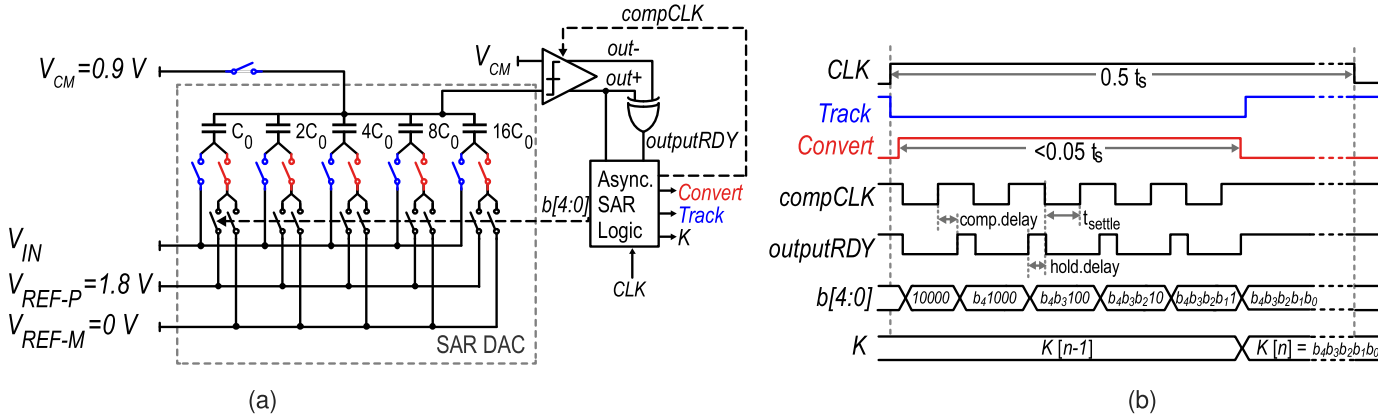

Fig. 9. (a) Simplified schematic of the asynchronous SAR ADC. (b) Timing diagram of the SAR ADC.

B. Current-Starved Inverter OTAs

Due to the reduced swing and current requirements, inverter-based OTAs are an ideal choice thanks to their high energy efficiency. The OTAs described in [13] and [14] are dynamically biased, resulting in switching losses, and hence degradation of their energy efficiency. The reduced output swing in this design allows the use of a simple class-A biasing scheme as shown in Fig. 8. The head and tail current sources M_{B0-2}, biased with 40 μA mirrored from a constant-gm reference, suppress unwanted signal and noise from the supply lines. Cascodes are used to achieve a 60-dB dc gain. Diode-configured transistors $M_{\mathrm{CP},N}$ are used to track the threshold voltage spread and bias the OTA cascode transistors, ensuring that both P/NMOS input pair remain in saturation across to PVT variations.

The CDS operation described earlier also samples the OTA's input-referred noise. In the case of inverter-based OTAs, assuming negligible noise contribution from the head and tail current sources and from the cascodes, both the transconductance and the noise are determined by the input PMOS and NMOS pairs, $M_{P1,2}$ and $M_{N1,2}$, respectively, and so unlike telescopic or folded-cascode OTAs, there is no excess-noise contribution. Therefore, the overall sampled noise is still kT/C_S, and C_S can be sized accordingly.

OTA2 is an 8× scaled down version of OTA1 consuming 6 μA. A conventional switched-capacitor common-mode feedback circuit [18], [19] is used to regulate the common-mode voltage of the OTA.

C. 5-bit Asynchronous SAR ADC

An asynchronous SAR ADC relies on internal states and logic to carry out the binary search algorithm [20], [21]. Fig. 9(a) shows the simplified schematic of the single-ended equivalent circuit of the asynchronous SAR ADC and Fig. 9(b) illustrates the timing of the logic signals associated with it. It consists of an asynchronous digital logic, a binary-weighted capacitor DAC (SAR DAC), and a comparator. Built as an asynchronous state machine, it uses the outputRDY signal to progress from one state to the next. The SAR ADC silently tracks the input to the rising edge of CLK, when it is sampled. Each bit conversion starts by setting the DAC inputs and then resetting the comparator with compCLK = 0. After a delay (t_{settle}) allows the DAC to settle, the comparator is clocked (compCLK = 1) to make a comparison. An XOR gate is used to monitor the comparator output and generate the outputRDY = 1 signal once a decision is made. The decision is saved in the SAR register and a new cycle is started after

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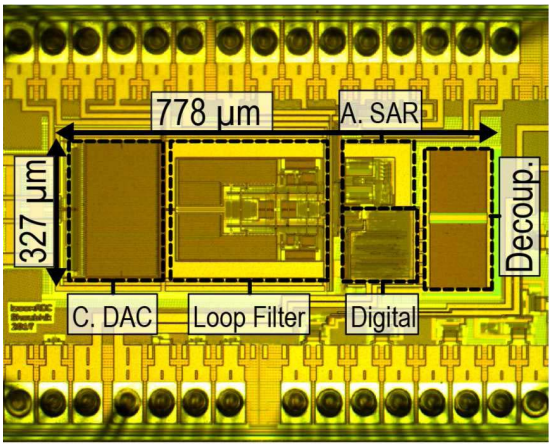

Fig. 10. Die micrograph of the prototype dynamic zoom ADC.

a hold delay for the digital logic. After five such asynchronous cycles, the SAR ADC returns to track the input.

The unit capacitors of the SAR DAC are around 5 fF and have more than 8-bit accuracy. The SAR ADC finishes the conversion in less than 5% of the zoom ADC sampling period (across PVT variations). To mitigate kick back on the small sampling capacitance due to the fast asynchronous operation, a dynamic comparator with a constant-current-biased preamplifier is used [22]. The power consumption of the preamplifier is minimized by keeping it off during the tracking phase.

V. Experimental Results

The prototype dynamic zoom ADC is realized in a standard 160-nm CMOS process and occupies an active area of 0.25 mm^2 as shown in Fig. 10. The input sampling capacitors, loop filter, SAR ADC, and digital logic occupy 22%, 39%, 4%, and 10% of the total area, respectively, with the remaining area taken up by secondary blocks such as bias and clock-phases generation, routing, and de-coupling capacitors.

The ADC is powered from off-chip 1.8-V regulators for the analog and digital supply domains, and a dedicated off-chip 1.8-V low-noise buffered voltage reference serves as the reference source for the ADC. The ADC draws 154.5 μA (88 μA for the analog section, 42 μA for the digital section, and 24.5 μA for the references).

The ADC achieves a peak SNDR of 118.1 dB with a −0.5-dB FS input signal, where 0-dB FS corresponds to a 3.6-$V_{PP,diff}$ input signal. The output spectrum is shown in Fig. 11. Off-chip buffers (OPA161x) are used to drive the ADC. An off-chip *RC* filter is used to limit the wideband noise of the buffers. Since the filter itself causes incomplete settling and hence some distortion, its cutoff (−3-dB BW of 2.3 MHz) is chosen such that the noise floor with an FS input signal is similar to the noise floor with the inputs shorted. The tone at $f_S/2$ and others at lower frequencies, when the inputs are shorted, are due to the lack of randomization in the DWA logic and $\Delta\Sigma$M. The $1/f$ noise corner is at 7 Hz and is measured by taking multiple (32×) averages of a 2^{23}-point FFT with the inputs shorted.

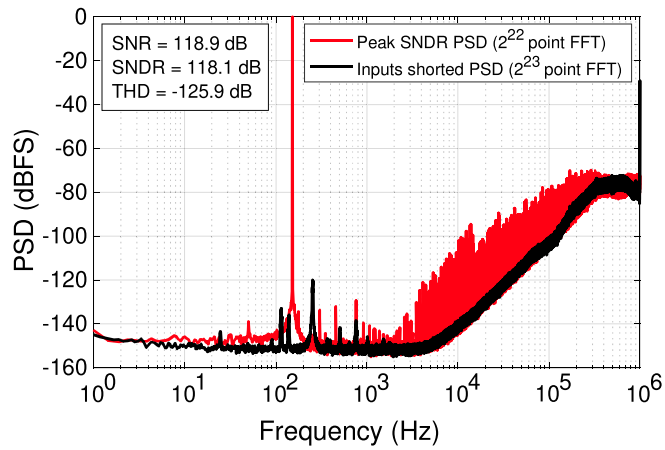

Fig. 11. Measured output spectrum of the zoom ADC at peak SNDR (with a −0.5-dB FS sine-wave input signal) and with inputs shorted.

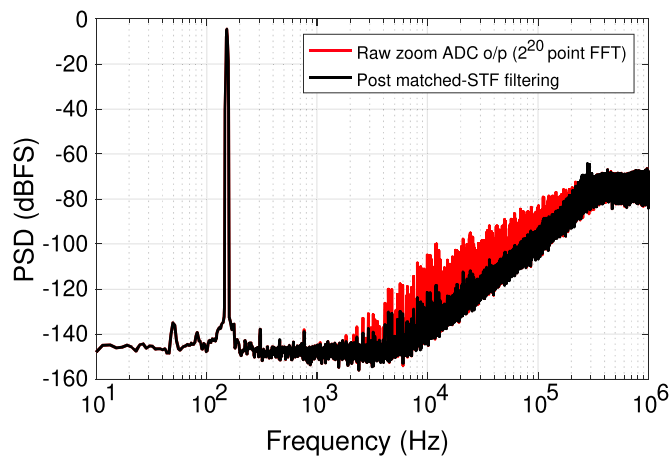

Fig. 12. Fuzz filtering of the output spectrum using a digital matched STF filter.

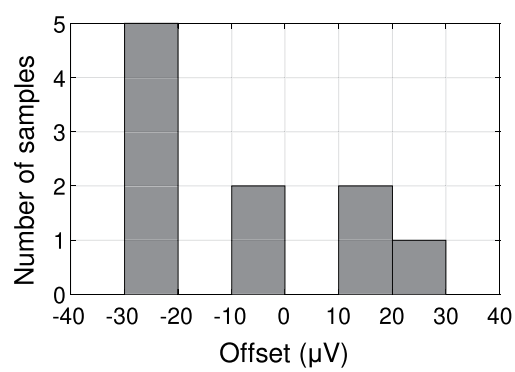

Fig. 13. Measured offset histogram (10 samples).

To demonstrate the efficacy of the out-of-band fuzz cancellation introduced in Section III-C, the off-chip digital post-processing filter has been implemented in MATLAB as an 8-tap finite-impulse-response (FIR) filter and used to process the measured output. Fig. 12 shows a comparison of the output spectrum before and after using the digital filter. The residual fuzz is indicative of a mismatch between the theoretical STF and the actual STF. A significant reduction in the out-of-band

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORKS

	This work	[1]	[7]	[11]	[12]	[13]	[14]	[23]
Year	**2018**	2018	2006	2016	2017	2013	2016	2016
Tech (nm)	**160**	180	600	55	180	160	160	350
Area (mm^2)	**0.25**	4	2.08	0.072	0.27	0.375	0.16	11.5
Supply (V)	**1.8**	1.8 / 5	3	1.2	1.5	1.8	1.8	5.4
Power (µW)	**280**	1970	300	15.7	33.2	6.3	1120	12700
Sampling Frequency (MHz)	**2**	1	0.03	1	0.64	0.05	11.29	0.64
Bandwidth (kHz)	**1**	500	0.0075	1	1.2	0.013	20	1
Offset (µV)	**30**	-	-	-	-	1	-	-
SNR_{MAX} (dB)	**119.1**	-	120	104	97.1	119.8	106	-
$SNDR_{MAX}$ (dB)	**118.1**	101.5	-	101	96.6	-	103	-
THD_{MAX} (dB)	**-125.9**	-	-	-	-	-	-	-116
DR (dB)	**120.3**	102.7	120	101.7	100.2	119.8	109	136.3
FoM_S $^+$ (dB)	**185.8**	176.7	164.0	179.7	175.8	182.7	181.5	185.3

$^+FoM_S = DR + 10 \cdot \log(BW/Power)$

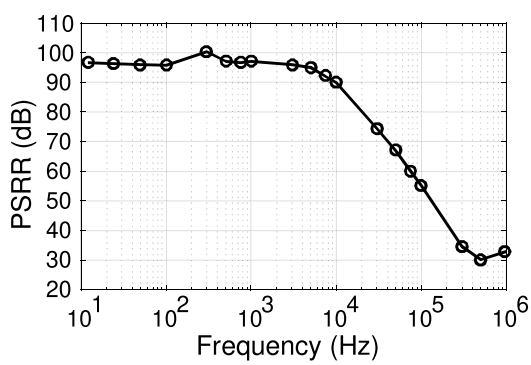

Fig. 14. PSRR of the dynamic zoom ADC.

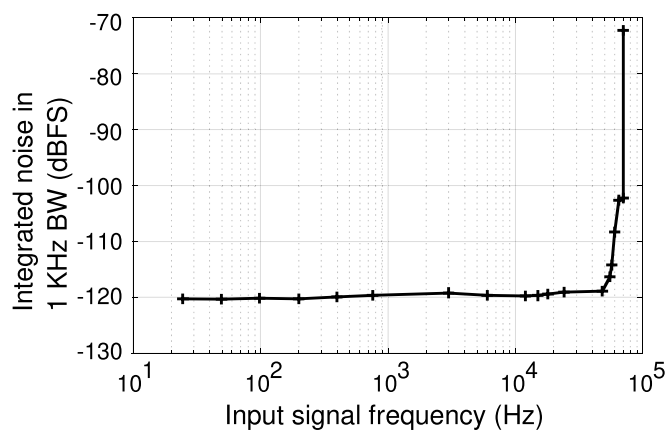

Fig. 15. Integrated noise floor across different input frequencies with a −1.5-dB FS amplitude.

fuzz is visible, and when implemented, this filter can be used to relax the decimation filter requirements or gain back the slight loss in BW due to the presence of the fuzz.

Fig. 13 shows the spread in the offset voltage from 10 different samples. A maximum value of 30 μV suggests that the CDS scheme is effective in suppressing the offset. Fig. 14 shows the power-supply rejection ratio (PSRR) of the ADC to be greater than 96 dB till 5 kHz, after which it has a second-order roll-off, demonstrating the current-starved OTA's ability to reject noise from the supply.

To assess the asynchronous SAR ADC's signal tracking capability, a −1.5-dB FS input signal is applied and its effect on the ADC's noise floor is monitored while varying the input signal frequency. Fig. 15 shows the integrated in-band noise power within a 1-kHz BW (0–1 kHz) across different input frequencies. The noise floor remains unperturbed for input frequencies as high as 48 kHz, making the dynamic zoom ADC immune to the out-of-band interferers. This advancement in the zoom ADC, to track signals 48× the signal bandwidth, is a drastic improvement over [14], which could only handle signals up to 1.5× its bandwidth before its in-band noise degrades.

Fig. 16 shows the measured INL of the dynamic zoom ADC. Without DWA, the linearity is limited by the mismatch of unit elements in the capacitive DAC and by asymmetry in the routing, resulting in an INL of 400 ppm. With DWA ON, the INL is within ±2 ppm.

Fig. 17 shows the measured SNR and SNDR of the dynamic zoom ADC across input amplitudes. The ADC achieves a peak

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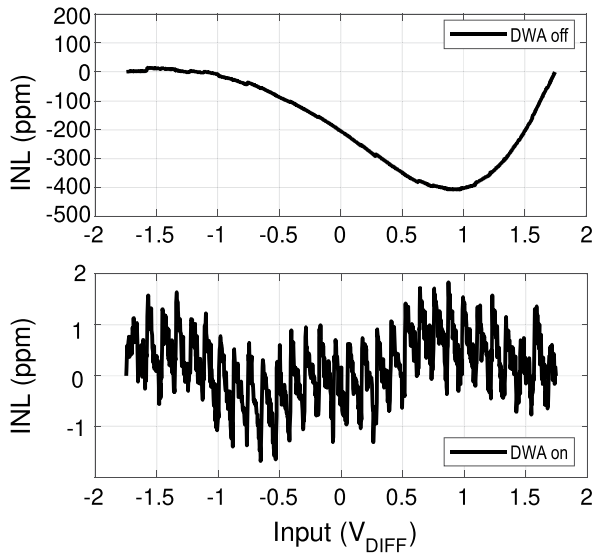

Fig. 16. Measured INL with and without DWA.

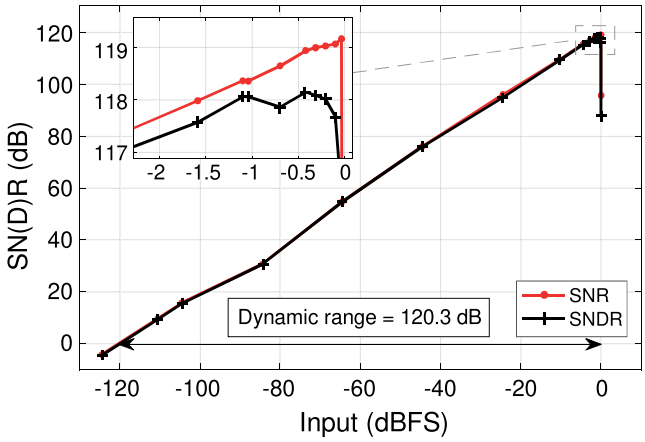

Fig. 17. Measured SN(D)R across input amplitude.

SNR, SNDR, and THD of 119.1, 118.1, and −125.9 dB, respectively. The measured DR of the ADC is 120.3 dB. Based on these results, the Schreier figure of merit (FoM) [24] is 185.8 dB. Table I summarizes the performance and compares it to other state-of-the-art ADCs with a similar resolution and bandwidth (SNDR > 95 dB and BW < 2 kHz). The proposed ADC outperforms all other designs in terms of peak SNDR and Schreier FoM while achieving a 120.3-dB DR.

VI. Conclusion

An energy-efficient dynamic zoom ADC to convert low-frequency signals with a high resolution is presented. By combining a fast asynchronous SAR with a high resolution high-linearity $\Delta\Sigma$M, the proposed ADC is able to track high-frequency signals, increasing the zoom ADC's immunity to the out-of-band interferers. Tight over-ranging relaxes the loop filter and simplifies the OTA's design resulting in an extremely low-power design and demonstrating the effectiveness of the zoom ADC to convert low-bandwidth signals with high resolution in an energy-efficient manner.

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