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A −109.1 dB/−98 dB THD/THD+N Chopper Class-D Amplifier with >83.7 dB PSRR Over the Entire Audio Band

Huajun Zhang[1], Nuriel Rozsa[1], Marco Berkhout[2], Qinwen Fan[1]
[1]Department of Microelectronics, Delft University of Technology, Delft, The Netherlands
[2]Goodix Technology, Nijmegen, The Netherlands
Email: h.zhang-13@tudelft.nl, n.n.m.rozsa@tudelft.nl, mberkhout@goodix.com, q.fan@tudelft.nl

***Abstract*—This paper reports a chopper Class-D audio amplifier that obtains high PSRR over the entire audio band. A chopping scheme is proposed to minimize intermodulation distortion between pulse-width modulation (PWM) and chopping in the audio band. A high-voltage chopper is developed to handle a 14.4 V PWM signal. Timing matching techniques are proposed to minimize chopping nonidealities which ensure good PSRR and THD. Fabricated in a 180nm BCD process, the prototype obtains a PSRR >109 dB at 217 Hz and >83.7 dB over the entire audio band. It also achieves −109.1 dB/−98 dB THD/THD+N and can deliver a maximum of 13 W to an 8-Ω load.**

Keywords—Class-D amplifier, chopping, PSRR, PWM, intermodulation

I. Introduction

Class-D amplifiers (CDAs) achieve high power efficiency because their output is switched between the supply and ground. To improve supply rejection and linearity, they often employ a closed-loop configuration with resistive feedback. However, the mismatch between feedback resistors causes common-mode-to-differential leakage and limits the overall PSRR. To achieve >100 dB PSRR, the mismatch between feedback resistors should be in the order of 10 ppm, which would require excessive die area or expensive trimming for high yield. The PSRR can also be improved by filtering the supply off-chip at the expense of increased system size. In [1, 2], an output common-mode regulation loop is employed to improve PSRR, but the PSRR drops significantly towards the edge of the audio band (20 kHz).

Alternatively, PSRR can be improved by removing feedback resistor mismatch using chopping. However, incorporating chopping into a pulse-width modulation (PWM) high-voltage (HV) CDA [2-5] is challenging. First, intermodulation between chopping and PWM in the audio band must be minimized. Second, an HV chopper capable of processing the HV fast-switching PWM signal at the CDA output is required. Third, chopping nonidealities such as duty cycle errors and glitches should be minimized to ensure good PSRR and THD.

This paper presents a 14.4 V chopper Class-D amplifier that addresses these challenges. Section II introduces the architecture of the CDA and explains the chopping scheme proposed to minimize the intermodulation between chopping and PWM in the audio band. Section III describes the implementation of the HV chopper and the timing alignment techniques to reduce chopping artifacts. Measurement results are reported in Section IV, followed by conclusions drawn in Section V.

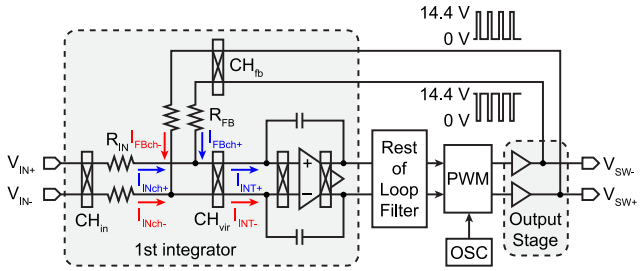

Fig. 1. Architecture of the proposed chopper CDA.

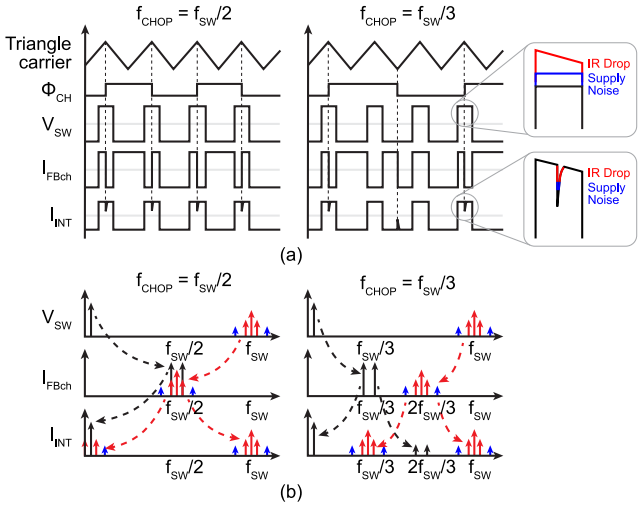

Fig. 2. (a) Time and (b) frequency domain behavior of chopping a PWM signal.

II. Architecture

A. Overview

Fig. 1 shows the architecture of the chopper CDA. It consists of a 3rd order loop filter and a PWM modulator in the 1.8-V domain, a fully differential HV output stage, and a resistive feedback network defining a closed-loop gain of 8. The input and feedback signals are modulated by the choppers CH_{in} and CH_{fb}, respectively, and then demodulated by CH_{vir}. The OTA of the 1st integrator is also chopped, which removes its 1/*f* noise and increases its CMRR, which rejects the HV supply-induced common-mode (CM) variations at its virtual ground.

B. Choice of Chopping Frequency

To minimize intermodulation between PWM and chopping in the audio band, the chopping scheme must be carefully chosen. In this work, the chopping clock and the

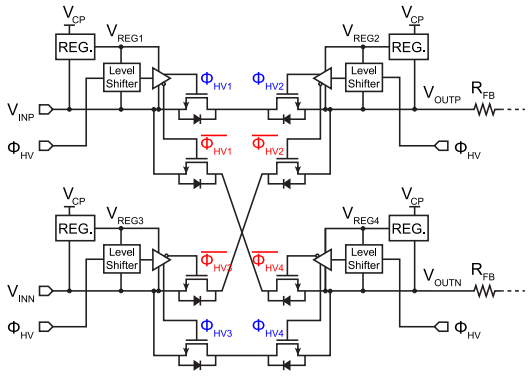

Fig. 3. Schematic of the HV chopper.

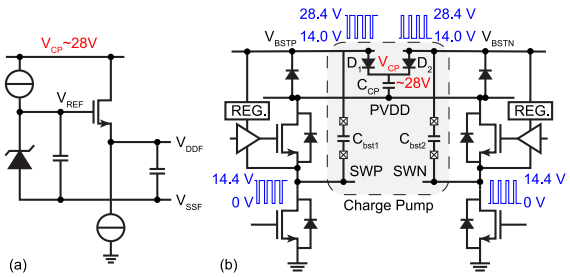

Fig. 4. (a) Regulator used in HV chopper, and (b) CDA output stage and the charge pump that supplies the regulators in the HV chopper.

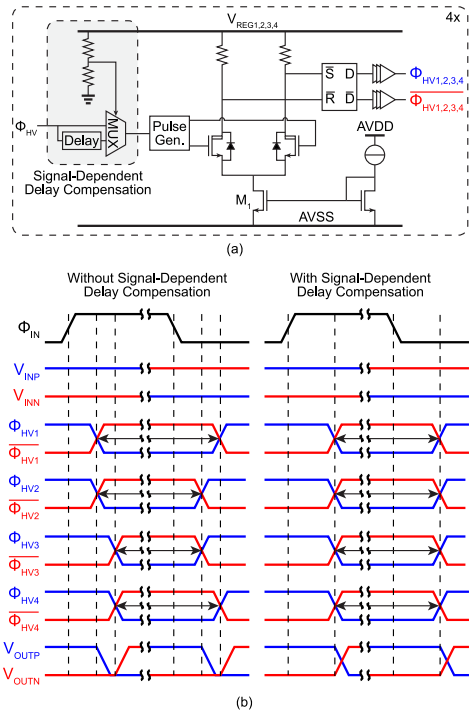

Fig. 5. (a) Level shifter [7] with added signal-dependent delay compensation circuit, and (b) input, output, and switch control signals in the HV chopper with and without compensation for the signal-dependent delay.

triangle wave carrier for PWM generation are synchronized such that the chopping transitions always occur at the center of a PWM pulse, as shown in Fig. 2(a). This avoids having very narrow pulses in I_{FBch}, which can be easily filtered by parasitic capacitances, leading to distortion. Moreover, chopping produces glitches at the switching transitions, which introduce two signal-dependent error sources and can degrade both PSRR and THD. The first error source is the supply noise (shown in blue). The second error source is the IR drop across the output stage power transistors (shown in red). When the class D amplifier drives a speaker, which can be electrically modeled as an inductor in series with a resistor, a signal-dependent ripple current is produced, which in turn creates a ripple voltage across the finite on-resistance of the output power transistors. The IR drop, therefore, contains PWM signal content that exhibits sideband around multiples of the PWM switching frequency f_{PWM} as shown in Fig. 2b [6]. To minimize degradation in both PSRR and THD due to intermodulation, the chopping frequency f_{CH} is chosen to be an odd subharmonic rather than an even subharmonic of f_{SW}. The two scenarios are compared in Fig. 2 in both the time and frequency domains. When the ratio f_{SW}/f_{CH} is even (e.g., equal to 2), the chopping glitch errors appear in the baseband, degrading both PSRR and THD. In contrast, when the ratio f_{SW}/f_{CH} is odd (e.g., equal to 3), the glitch errors are modulated to the chopping frequency. Choosing f_{CH} to be higher than the audio band edge (20 kHz) with a sufficient margin guarantees that the demodulated PWM sideband around f_{CHOP} is kept out of the audio band. In this work, an f_{CH} of 100 kHz (=f_{SW}/21) is chosen. It should be pointed out that the IR drop also contains components around even multiples of f_{SW}, which will be modulated to the baseband. To minimize this intermodulation, the total energy of the glitches should be reduced, which can be done by choosing a low f_{CH} and using circuit techniques to reduce the size of the individual glitch, as described in Section III.

III. Circuit Implementation

A. High-Voltage Chopper

To handle the 14.4 V PWM signal, a bootstrapped HV chopper (CH_{fb}) is proposed, as shown in Fig. 3. Back-to-back LDMOS transistors are used to block the conduction path through the body diodes when the switches are turned off. The chopper clocks are transferred from the LV digital domain (1.8 V) to the HV domain by level shifters [7], each powered by a local regulator. All regulators are sourced by a charge pump that provides a ~28 V supply.

Each open-loop regulator, shown in Fig. 4a, employs a Zener reference and a source follower output stage. The charge pump, shown in Fig. 4b, consists of 2 Schottky diodes (D_1 and D_2), an on-chip capacitor C_{CP}, and reuses two off-chip bootstrap capacitors C_{bst1} and C_{bst2} that are already required in the floating gate driver circuits of the power transistors [5]. C_{CP} is charged by C_{bst1} and C_{bst2} in an alternating fashion in each PWM cycle, holding V_{CP} up to ~28 V. The level shifter is shown in Fig. 5a [7]. Depending on the PWM signal and the chopping phase, $V_{REG1,2,3,4}$ are either ~5 V or ~19.4 V. This introduces a signal-dependent delay in the level shifter since, in the former case, the bias current source M_1 operates in the triode region for part of the transition. Therefore, the chopping signals experience a longer delay when switching from 0 V to 14.4 V and a shorter delay vice versa. As a result, two distinct switching transitions occur, as illustrated in Fig. 5b, which causes a duty cycle error that degrades PSRR. To mitigate this issue, a delay compensation block is employed in the HV chopper drivers. A simple 10:1 resistor divider detects the voltage level of V_{REG} and either enables a delay if $V_{REG} \approx 19.4$ V or disables the delay if $V_{REG} \approx 5$ V (Fig. 5a) before the next transition. As a result, all HV chopper switching transitions are aligned.

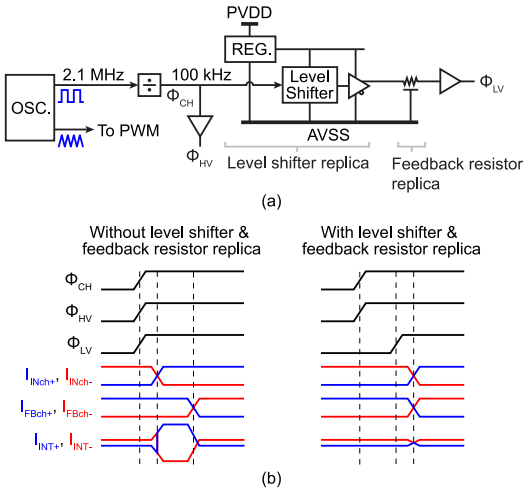

Fig. 6. (a) Replica delay circuit to align chopping transitions of HV and LV choppers, and (b) HV and LV chopper clock signals and resulting input, feedback, and integrator current with and without the replica delay circuit.

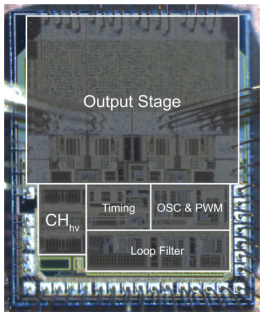

Fig. 7. Die photo.

B. HV and LV Chopper Timing Matching

Apart from CH_{fb}, all the other choppers are implemented in the 1.8 V domain. Timing skew between the HV and LV choppers due to different driving circuitries results in large chopping glitches that can degrade THD and PSRR. Moreover, the parasitic capacitance in the feedback resistors adds a delay between CH_{fb} and CH_{vir}, which again causes large chopping glitches. Replicas for the level shifter and feedback resistor, shown in Fig. 6a, are added in the LV chopper driving path to mitigate these issues across PVT variations. Fig. 6b illustrates the chopped input current $I_{INch+/-}$, chopped feedback current $I_{FBch+/-}$, and the current going into the 1st integrator $I_{INT+/-}$ (indicated in Fig. 1) with and without the delay replicas. As shown, the replicas can significantly remove the timing skew and therefore minimize the chopping glitches in the current flowing into the 1st integrator.

C. LV Circuitry

To ensure linearity with a full-scale input signal, the input choppers are bootstrapped to maintain a constant on-V_{GS} for the switches [8]. A PWM modulator driven by an on-chip oscillator runs at 2.1 MHz, which allows a relatively high loop gain for high linearity. A 3rd order loop filter [5, 7] is employed, which provides >80 dB loop gain within the audio band to suppress the distortion of the output power stage. The input stage of the 1st integrator's OTA is sized such that its 1/*f* noise corner frequency is below f_{CHOP}.

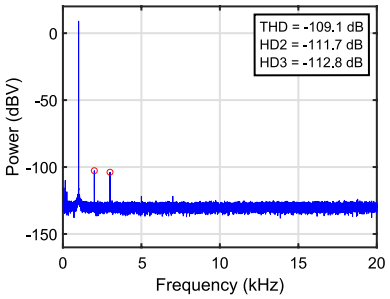

Fig. 8. Output spectrum for 1 kHz input at 1 W output power.

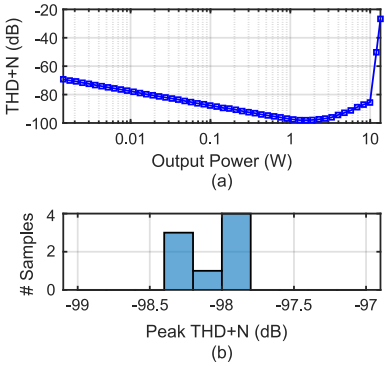

Fig. 9. (a) THD+N across output power, and (b) peak THD+N for 8 samples.

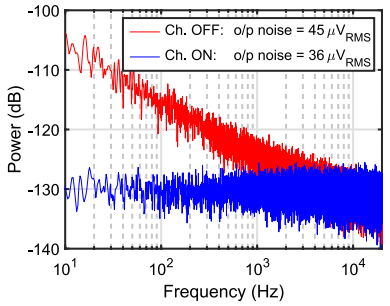

Fig. 10. Output spectra with and without chopping with a zero input.

IV. Measurement Results

The design is prototyped in a 180nm BCD process and occupies 5 mm^2 (Fig. 7). The HV chopper, its driving circuit (the level shifters and regulators), and the timing replica circuits occupy 7% of the total chip area. For all measurements, the CDA is loaded with (44 µH + 8 Ω), which mimics a real speaker, and the output is measured using an Audio Precision APx555 Analyzer.

The measured output spectrum for a 1 kHz sine wave input is shown in Fig. 8. The CDA achieves a THD of −109.1 dB when delivering 1 W into the load. The THD+N performance across output power is plotted in Fig. 9. The CDA achieves a peak THD+N of −98 dB (0.0013%). Fig. 10 compares the output spectra with a zero input when chopping is turned ON and OFF. With chopping ON, flicker noise is clearly suppressed, and the integrated output noise (A-weighted) improves from 45 μV_{RMS} to 36 μV_{RMS}. Fig. 11 plots the PSRR across the entire audio band for 8 samples measured by superimposing a 2 V_{PP} sinewave onto the 14.4 V supply. When chopping is turned OFF, the PSRR spreads widely

TABLE I. PERFORMANCE SUMMARY AND COMPARISON.

	This Work	D. Schinkel [2]	[3]	E. Cope [4]	S. Karmakar [5]
Area (mm^2)	5	-	-	4.3	4.8
Supply (V)	14.4	25	14.4	8~20	14.4
f_{SW} (kHz)	2100	500	2100	400	2000
Quiescent Current (mA)	21	-	180	20.5	17
Idle Power (mW)	302	-	-	-	245
Output Power (W)	13	80	75	20	28
Efficiency	92%	>90%	86%	90%	91%
Peak THD+N @ 1kHz	0.0013%	0.004%	0.02%	0.0013%	0.0008%
SNR (A-weighted)	108 dB	-	-	116 dB	-
DR (A-weighted)	110.3 dB	115 dB	-	115.5 dB	109 dB
PSRR (Frequency Range)	109 dB~83 dB (20 Hz~20 kHz)	88 dB~60 dB (100Hz~20kHz)	75 dB~57 dB (20 Hz~20 kHz)	80 dB~50 dB (20 Hz~20 kHz)	70 dB ~ 62 dB (20 Hz~20 kHz)
# Samples	8	-	-	-	-

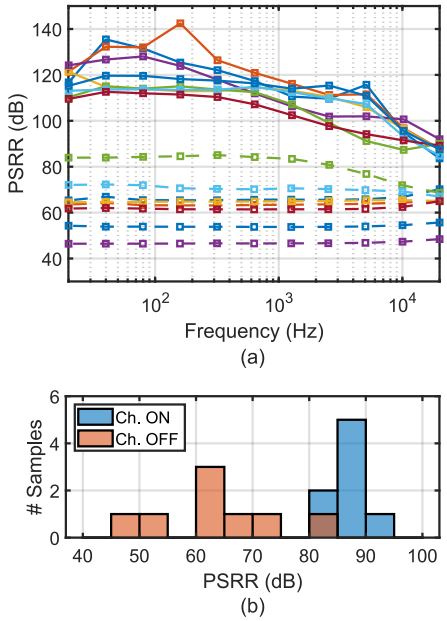

Fig. 11. (a) PSRR across the audio band with chopping ON (solid) and OFF (dashed), and (b) Comparison of PSRR at 20 kHz between chopping ON and OFF.

between 46 dB and 84 dB due to random resistor mismatch. With chopping enabled, the PSRR is improved to >109 dB at low frequencies for all samples and remains > 83 dB across the entire audio band. Fig. 12 shows the efficiency across output power. The CDA achieves a peak efficiency of 91.8%. It draws a quiescent current of 22 mA from the 14.4 V supply.

Table I summarizes the performance of this CDA and compares it with other state-of-the-art HV (>10 V) CDAs. This work achieves over 20 dB higher PSRR both at low frequencies and 20 kHz while attaining competitive THD+N, SNR, and power efficiency.

V. CONCLUSION

This paper proposes the use of chopping to improve the PSRR of CDAs. The chopping frequency is carefully chosen to be an odd subharmonic of the PWM switching frequency to minimize intermodulation between chopping and PWM in the audio band. An HV chopper capable of processing the 14.4V CDA output is presented. Timing alignment techniques are proposed to reduce chopping duty cycle errors and glitches to ensure good THD and PSRR. Measurement results across multiple samples show a >20 dB improvement in PSRR over

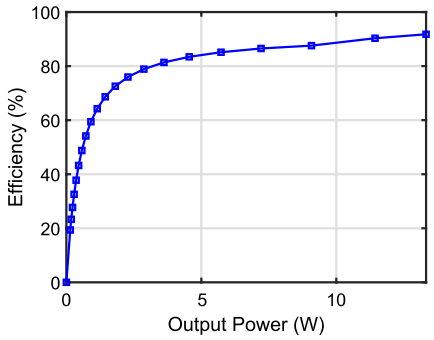

Fig. 12. Power efficiency across output power.

the entire audio band while achieving competitive THD+N performance compared to other state-of-the-art designs.

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