Delft University of Technology

Lifecycle Management of Emerging Memories

Fieback, Moritz; Poehls, Leticia Bolzani

DOI
10.1109/ETS61313.2024.10567697

Publication date
2024

Document Version
Final published version

Published in
Proceedings - 2024 29th IEEE European Test Symposium, ETS 2024

Citation (APA)
Fieback, M., & Poehls, L. B. (2024). Lifecycle Management of Emerging Memories. In *Proceedings - 2024 29th IEEE European Test Symposium, ETS 2024* (Proceedings of the European Test Workshop). IEEE. https://doi.org/10.1109/ETS61313.2024.10567697

Important note
To cite this publication, please use the final published version (if applicable).
Please check the document version above.

Copyright
Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

Takedown policy
Please contact us and provide details if you believe this document breaches copyrights.
We will remove access to the work immediately and investigate your claim.

This work is downloaded from Delft University of Technology.
For technical reasons the number of authors shown on this cover page is limited to a maximum of 10.

Green Open Access added to TU Delft Institutional Repository

'You share, we take care!' - Taverne project

https://www.openaccess.nl/en/you-share-we-take-care

Otherwise as indicated in the copyright section: the publisher
is the copyright holder of this work and the author uses the
Dutch legislation to make this work public.

2024 29th IEEE European Test Symposium (ETS)
- Embedded Tutorial Paper -

Lifecycle Management of Emerging Memories

Moritz Fieback* Letícia Maria Bolzani Pöhls†
* QCE Department, Faculty EEMCS, Delft University of Technology, The Netherlands
† Group of Test & Reliability of Emerging Applications, Chair of Integrated Digital Systems and Circuit Design, RWTH Aachen University, Germany
m.c.r.fieback@tudelft.nl poehls@ids.rwth-aachen.de

2024 IEEE European Test Symposium (ETS) | 979-8-3503-4932-0/24/$31.00 ©2024 IEEE | DOI: 10.1109/ETS61313.2024.10567697

***Abstract*—Traditional charge-based memories such as dynamic RAM (DRAM) and flash are facing more and more manufacturing, reliability, energy, and speed issues. A growing group of emerging memory technologies, such resistive RAM (RRAM), spin-transfer torque magnetic RAM (STT-MRAM), phase change memory (PCM), and Ferroelectric (Fe) devices (e.g., FeFET, FeRAM), address these problems. Nonetheless, these technologies are also not perfect, and thus special care must be taken to ensure that the lifecycle management, from design to obsolescence, of these memories is as optimal as possible. Lifecycle management is being developed for traditional technologies, but these are not optimized for emerging memories yet. In this paper, we present the first steps of lifecycle management for emerging memories. We analyze the different lifecycle phases that exist for two case studies on RRAM and FeFET-based memories. In this analysis, we identify how the phases affect each other and which optimizations are possible by analyzing the complete lifecycle. Finally, we compare the lifecycle phases of these two emerging memories to see how a unified approach can be developed.**

***Index Terms*—lifecycle management, emerging memory, RRAM, STT-MRAM, PCM, FeFET**

I. Introduction

Traditional charge-based memory technologies, such as dynamic RAM (DRAM) and Flash are facing more and more issues, that relate to their difficult manufacturing process, energy consumption, and speed [1–3]. Emerging memory technologies, such as resistive RAM (RRAM), spin-transfer torque magnetic RAM (STT-MRAM), phase change memory (PCM), and memories based on ferroelectric (Fe) devices (e.g., FeRAM, FeFET), address these problems. For example, RRAMs and PCMs are faster than Flash, STT-MRAM is faster than DRAM and non-volatile, and FeFETs are more energy efficient than Flash [4–6]. Furthermore, it is generally true that electronics, both traditional and emerging technologies, are used increasingly in critical applications that are more demanding than in the past, e.g., autonomous driving or edge AI in healthcare [7]. As such, it becomes more and more important that the quality of these electronics can be guaranteed over longer periods of time. To provide these guarantees, it is needed that the complete lifecycles of these devices are understood and optimized together in an effective and efficient manner, a process called lifecycle management. Lifecycle management aims to optimize the complete lifecycle of a device, from design to its obsolescence.

Existing research in this field can be divided into two directions: general silicon lifecycle management tools, and research related to individual emerging technology lifecycle phases. EDA companies have started providing lifecycle management tools for general digital logic semiconductors, but these tools are not yet dedicated and optimized for emerging memories [8–10]. For instance, they severely lack optimized Design-For-Test (DFT) circuits that can be used for emerging memories. Research for individual emerging memory technologies focuses mainly on single aspects, such as circuit design [11, 12], manufacturing optimization [13], production testing [14, 15], or in-field security [16, 17]. Nonetheless, some research relates to more than one lifecycle phase, e.g., by combining test and reliability systems [18, 19], but this is not yet suitable or complete enough to allow for full lifecycle management of emerging devices. For example, there is limited feedback to other lifecycle phases, nor is a complete analysis method available.

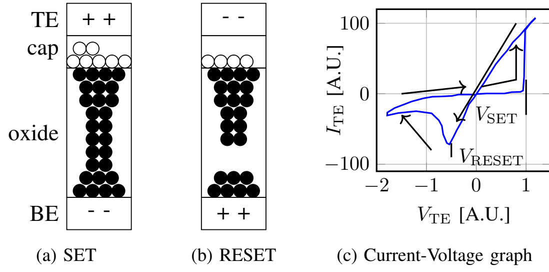
In this paper, we present the first steps towards a complete lifecycle management concept for emerging devices. We do this by analyzing what the different lifecycle phases for these circuits are, how they interact with each other, and how these interactions can be leveraged to optimize their overall quality. Furthermore, by comparing the lifecycles of different emerging memory technologies, we are able to identify overlapping factors between the different technologies. This also allows for more optimized lifecycle management development. In short, this paper:

- Introduces lifecycle management for emerging memory technologies;
- Analyzes the different phases in an emerging memory's lifecycle;
- Applies this analysis to two emerging memory technologies: RRAM and FeFET;
- Discusses optimizations that can be made based on this analysis for single technologies, as well as for multiple technologies at once.

The remainder of this paper is structured as follows. Section II presents background information on four emerging memory technologies: RRAM, and FeFET-based memories. Section III describes the different lifecycle phases of an emerging memory. Section IV analyzes the lifecyle of an RRAM. Section V analyzes the lifecycle of a FeFET-based memory. Finally, Section VI discusses the differences and overlaps and concludes this paper.

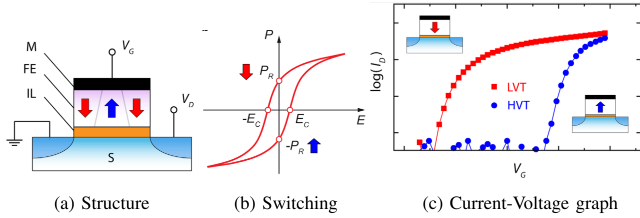
979-8-3503-4932-0/24/$31.00 ©2024 IEEE

Authorized licensed use limited to: TU Delft Library. Downloaded on July 15,2024 at 14:57:29 UTC from IEEE Xplore. Restrictions apply.



(a) SET (b) RESET (c) Current-Voltage graph

Fig. 1: RRAM CF and switching [18]



(a) Structure (b) Switching (c) Current-Voltage graph

Fig. 2: FeFET structure and switching [5]

II. Background on Emerging Devices

This section provides background information on the two emerging technologies that will be part of the later case study: RRAM and FeFET-based memories.

A. Resistive RAM

An RRAM device is a stacked structure of an oxide (OxRAM) between two metallic electrodes (bottom (BE) and top (TE)), or between an electrode and a capping (cap) layer, as shown in Fig. 1a. When a positive voltage is applied to the TE with respect to the BE, the bond between the oxygen and metal ions can break [20–22]. The oxygen ions are then attracted towards the TE into the capping layer and leave a conducting chain of oxygen vacancies behind, called the conductive filament. When a negative voltage is applied to the TE, the oxygen ions move back from the capping layer into the oxide and break the CF, as shown in Fig. 1b. In this case, the resistance of the device increases again. This switching process is illustrated in Fig. 1c. The figure shows that when $V_{\mathrm{TE}} > V_{\mathrm{SET}}$, the CF forms and the resistance of the device decreases, while when $V_{\mathrm{TE}} < V_{\mathrm{RESET}}$, the CF is dissolved and the resistance increases again. To ensure reliable writing and reading from the cell, the SET and RESET resistance should be far apart from each other (at least 2 to 3 times).

The CF will have a different shape every time that it is grown or dissolved, leading to cycle-to-cycle variations [23]. Further, the CFs will also be different in every manufactured device, thus leading to device-device variations. The CF also suffers from wear-out phenomena when the device is written frequently; it will tend to get stuck in the RESET or SET state (more frequently) [24]. Finally, the CF may dissolve as well under high storage temperatures or long storage times, limiting the retention of the device [24].

B. FeFET

Ferroelectric FETs have a structure that is shown in Fig. 2a [5]. It resembles a regular FET, except that an additional ferroelectric (FE) layer is added between the metal (M) gate and the interfacial layer (IL). The crystalline FE layer has a natural polarization (indicated by the arrows per crystal) that affects the threshold voltage of the FET. The polarization can be changed by applying an electrical field through the layer, as shown in Fig. 2b. By changing the polarization of the FE layer, the threshold voltage can be changed, as shown in Fig. 2c, and thus data can be stored on the device. The voltage difference between the two resulting threshold voltages is called the memory window. the wider this window is, the easier it is to read out the device.

FeFETs also suffer from reliability issues such as endurance, retention, and variability [25]. These are caused by the non-perfect polarization switching of the individual crystals. For example, after a certain number of switching cycles, not all crystals may switch, thus reducing the memory window. If the memory window falls below a threshold, the device cannot be read out anymore. Similarly, under high temperature or long storage conditions, the polarization may also switch and thus lead to data loss. Variability is caused by the fact that the switching of the crystals in the FE layer is stochastic, and also by the fact that these layers differ from device to device.

III. Lifecycle Phases

The lifecycle of emerging devices can be described in five phases, as shown in Fig. 3: design, post-silicon validation and yield learning, manufacturing and production test, deployment, and end of life. In each of these phases, choices are made that affect the later phases, but they also have an impact on earlier phases. For example, during the manufacturing phase monitoring processes can be included that give insights into the device's performance during deployment as well. Similarly, the measurements from these monitors can be used to optimize the manufacturing process, as they indicate weaknesses.

In this section, we will discuss the different lifecycle phases in more detail. In Sections IV–V, we demonstrate how these phases are interconnected for all the RRAMs and FeFETs.

A. Design

In this phase, two goals need to be achieved: the design is made to adhere to its functional requirements and to adhere to its lifecycle requirements. The functional requirements can be, for example, memory sizing, operating frequencies, and interfaces. Lifecycle requirements can be, e.g., defectivity, endurance, security, and lifetime. To meet the lifecycle requirements, changes need to be made to the functional design, thus resulting in trade-offs in the finalized design. To illustrate, to obtain a high endurance, it might be needed to include specialized monitors in the circuit that measure the degradation of the chip during deployment. In the design phase, it is decided which design modifications are made and included to facilitate achieving the lifetime requirements.

Authorized licensed use limited to: TU Delft Library. Downloaded on July 15,2024 at 14:57:29 UTC from IEEE Xplore. Restrictions apply.

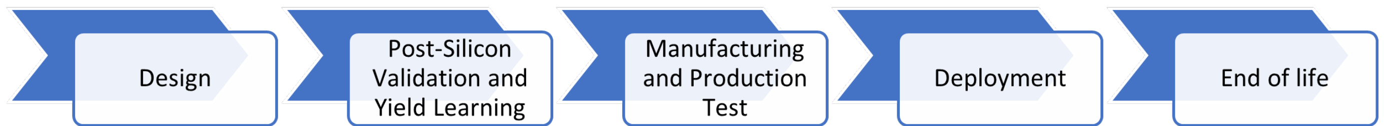


Fig. 3: Different lifecycle phases of emerging devices

B. Post-Silicon Validation and Yield Learning

In this phase, the post-silicon design is validated and made ready for mass production through yield learning. The validation ensures that the design is meeting its requirements, both functional and lifecycle-related. Here, bugs are identified and extensive characterization of the design takes place to see how the yield of the production process can be improved, which is called yield learning. As an illustration, from the characterization it may follow that the design cannot meet its endurance requirements due to a defect. To combat this, the manufacturing process needs to be improved so that the occurrence probability of the defect is reduced, but also the production and in-field tests need to be improved to detect these defects in a better manner. For example, additional DFT can be included, or a test algorithm can be optimized for a frequently observed defect, which means that the design has to be adapted.

C. Manufacturing and Production Test

In this phase, mass production has started and the lifecycle management processes focus on monitoring the production process and applying production tests to every device. The aim is to minimize the cost of both these procedures without losing quality. The production process is monitored through monitoring structures on the wafer that measure, e.g., threshold voltages, switching frequencies, and resistances. This monitoring ensures that the devices operate within the specified margins. Production tests are run on every device and result in a pass/fail decision. Hence, these tests need to be time-efficient, while detecting as many defects as possible. This might require the design of dedicated test algorithms, or the inclusion of DFT, e.g., BIST, or schemes that detect certain defects. For memories, a single failing cell renders a complete chip useless and thus is detrimental for the yield. To prevent this, repair mechanisms are included that can replace the row or column in which the broken cell is present based on the production test result.

D. Deployment

In this phase, the chip is deployed in its intended working environment and the lifecycle management focuses on ensuring that the device operates reliably, functionally safe, and securely. These requirements are closely related, but not the same. The reliability of a circuit details how well the circuit can perform its function during its intended lifetime. To ensure reliability, online or in-field self-testing, parameter monitoring, and error-correcting circuits are used. The aim of these is to detect failures that arise from aging and mitigate their impact. To illustrate, running an in-field test during the startup of the device could detect broken bits due to aging and perform an in-field repair. To minimize costs, this test can use the same hardware that was used to perform the production test. The functional safety of a circuit details how the circuit will respond due to upsets, such as radiation or aging of the circuit. For example, due to aging, a certain bit is stuck at a single value. To prevent critical data loss, error-correcting codes (ECCs) can be used to restore the data word in which the bit is present, thus mitigating an unsafe situation. Finally, security details how well the chip is protected against damage and theft of its function and data. For example, an attacker might gain access to the data stored in a memory by increasing the chip's clocking frequency. Now, an on-chip frequency sensor can detect this sudden increase and take precautions to prevent data loss.

E. End of Life

In this phase, the circuit has reached the end of its functional life and needs to be decommissioned appropriately. This process entails the shutdown of the device and proper recycling. When the device reaches its obsolescence it is shut down. This needs to be done safely and securely, i.e., the shutdown will not lead to functional unsafe situations, nor will it lead to a data loss. For example, aging monitors might be used to determine that the device cannot operate to its functional requirements anymore, and bring the system into a safe shutdown state in which all data on the chip is deleted or securely encrypted. After this, the chip needs to be recycled in a proper manner so that it is not sold again by malicious vendors, or that it poses harm to the environment. This can be done, for example, by ensuring that the shutdown chip is sent back to its manufacturer through legal means.

IV. Case Study: RRAM

The lifecycle management of RRAMs will be discussed in this section. Details about every lifecycle phase are going to be provided.

A. Design

In the design phase, there are several choices that affect the lifetime performance of an RRAM. These relate to the cell structure, read and write circuitry, and operating frequencies. The cell structure is defined by the material properties of the RRAM stack and the architecture of a bit cell. To

Authorized licensed use limited to: TU Delft Library. Downloaded on July 15,2024 at 14:57:29 UTC from IEEE Xplore. Restrictions apply.

illustrate, hafnium-based RRAM devices are easier to integrate in existing manufacturing processes but suffer from a smaller resistance window than other more exotic materials [26], which makes it harder to read out these cells and thus forms a manufacturing and reliability risk The architecture of bit cell is determined by the number of RRAM devices and access transistors. Single RRAM devices offer dense crossbar structures but suffer from sneak-paths that make reading the cell more difficult [20, 27]. Adding an access transistor solves these problems at the cost of increased area consumption [20]. Besides, due to the stochastic growth of the filament, RRAM devices suffer from large resistive variations between different devices, and even within different write cycles of a device itself [28]. This can be addressed by incorporating more elaborate write schemes, that ensure that the cell is written properly, but this introduces an additional area or time overhead [29].

B. Post-Silicon Validation and Yield Learning

The most important metrics for RRAMs during post-silicon validation and yield learning are the endurance of a cell, the variability, the retention, and the defects that can be present after manufacturing. The cycle endurance describes how many write cycles the RRAM can withstand without failing. If this number is too low, the write operation, material stack, or usage of error-correcting circuits can be adapted. The first has the benefit that it might not require a redesign of the circuit at the cost of power or time, but that this might affect the reliability of the circuit later. The other two will require (significant) design changes but can give better results. As described in the design phase, the variability needs to be small enough that the readout circuit can reliably read the cell's contents. As such, if the variation is too large, design changes have to be made. Retention describes how long the data remains stored on the devices when it is turned off. Again, if this value is too low, design changes need to be made.

Finally, during validation and yield learning, the defects that can occur in the production process are identified through extensive testing and diagnosis [30, 31]. This information is used to optimize the manufacturing process and might affect the design of the device, but it is also used to develop efficient test solutions that can be used in the production phase [32]. To illustrate, in [33] the existence of the intermittent undefined state fault is shown, in which the underlying defect mechanisms are caused by a poor production process or too severe operating conditions. For the former, either test solutions are required that detect the defect, i.e., in this case, extensive march algorithms, or mitigation of the faulty effects is needed, e.g., by adding appropriate ECC. For the latter, design modifications are needed that ensure that the devices are not over-stressed. Similar to the other requirements, these choices can affect the design as well as further lifecycle phases.

C. Manufacturing and Production Test

In this phase, the lifecycle management focuses mainly on production testing of RRAM, rather than monitoring, as there are no dedicated RRAM manufacturing monitoring circuits. Production tests need to ensure a high defect coverage that can be obtained in a short test time. Test time can be reduced by optimizing the march algorithms that are used [30], or by the inclusion of DFTs that reduce test time, e.g., through sneak-path testing [34], or in-memory computing [35]. However, due to the analog behavior of the RRAM device, march testing alone is not enough to achieve a high defect coverage [32]. If this coverage is not high enough, the reliability of the device later in the lifecycle might be too low. Instead, additional DFTs are needed that are able to detect certain defects and faults in RRAMs that cannot be detected using regular memory operations, e.g., by adding multiple comparisons [18, 19], or by modifying the write time [36]. Some of these tests can also work directly on the chip itself as a self-test, which is also useful during the deployment phase of the device.

D. Deployment

When RRAM devices are deployed in the field, the main concerns are related to reliability and security. As mentioned before, RRAM cells have a limited cycle endurance, for both writing and reading operations. After a certain number of cycles, frequently around 10^{6-7} cycles [26], the RRAM cells cannot be written properly anymore and become unable to store data. To address these aspects, self-tests can be run at regular intervals to detect loss of storage capabilities. Ideally, these tests make use of (parts of) the same on-chip hardware that was used during the manufacturing testing of the devices, such as [18]. Frequent reading of an RRAM cell also deteriorates the data stored and can lead to read-disturbance faults. To prevent data loss from this, solutions such as ECC or dedicated read disturb monitors can be included [28]. Security risks for RRAMs are mainly related to data theft or loss. It is shown that thermal coupling between different cells allows for row hammer attacks [16] that might leak or lose data. Furthermore, because the data in an RRAM are fundamentally stored as a filament in the oxide, the data can be read out by physically reading out the shape of the filament using x-rays [37].

E. End of Life

At the end of an RRAM's lifecycle, it is important that the device is securely decommissioned, as data will remain stored in the memory. For example, the x-ray-based methods from [37] can still be used to obtain the data in the device. To prevent this data theft, the device can be reset when its aging sensors detect the end of its life by applying a long pulse that will bring all the devices in the same state, preferably the SET state. Finally, the device needs to be recycled, to prevent environmental damage.

V. Case Study: FeFET-based Memories

This section will discuss the lifecycle management of FeFET-based memories.

Authorized licensed use limited to: TU Delft Library. Downloaded on July 15,2024 at 14:57:29 UTC from IEEE Xplore. Restrictions apply.

A. Design

Similar to RRAM, many design choices will affect the lifecycle of a FeFET-based memory, such as materials, and read and write circuitry. The usage of different materials has a strong effect on the write voltages that are required in the circuit, e.g., polyvinylidene fluoride-based FeFETs require a much higher gate voltage than hafnium-based ones [38]. Furthermore, higher write voltages affect neighboring cells and can lead to write failures [39]. Applying a higher voltage will result in more degradation of peripheral circuitry, e.g., read and write circuits, and thus reduce the expected quality of the memory.

B. Post-Silicon Validation and Yield Learning

The most important metrics for FeFETs during post-silicon validation are similar to RRAM: endurance, retention, variability, and defects present. Again, if these metrics are not up to the required specifications, the design can be modified to optimize them, or additional features can be included that can deal with these problems, such as error correction. Research has also started on the topic of understanding and modeling defects in FeFETs [40], but this field is far from being fully developed.

C. Manufacturing and Production Test

For FeFETs, to this date, there exist no dedicated production test solutions. Nonetheless, it is clear that fast and dedicated test approaches are needed, similar to other emerging memory technologies. For example, it can be expected that there will be unique defects and faults in FeFET-based memories that need to be properly modeled, in order to develop an effective test method [32]. It can then subsequently be expected that these will need to ensure proper write verification can be used to quickly determine the stability of the cells, while it also is useful during in-field testing.

D. Deployment

During deployment, similar concerns as for RRAM are relevant: reliability, and security. For reliability, factors such as retention, variability, and endurance are the main concerns [5, 25]. Optimizing a design for high endurance will lower its retention and vice versa, and obtaining a larger memory window will also decrease the endurance. [25], which is similar to what happens in RRAMs. As such, similar architectures that have been used in RRAMs to guarantee a certain reliability could be used for FeFET-based memories as well. These circuits can range from ECC, to onboard sensors, to in-field testing. Again, care should be taken to ensure that these features are useful also in earlier and later lifecycle phases. For security, it is shown that FeFETs are susceptible to side-channel attacks that reveal the data that is stored [17]. As such, special care needs to be taken to protect the memory, e.g., by encrypting its contents [41].

E. End of Life

At the end of the FeFET's lifecycle, it needs to be securely decommissioned as well. When the device senses that it is reaching the end of its life using the reliability sensors, the stored data needs to be swept from the device to prevent data theft. Alternatively, encryption methods can be used to ensure that this is not needed [41]. Finally, the device needs to be recycled properly, so that environmental harm is minimized.

VI. Discussion and Conclusion

In this paper, we have presented the first steps towards a unified lifecycle management approach for emerging memories. We have analyzed how the the different lifecycle phases affect each other and how consideration of the full lifecycle can lead to products of better quality. Based on the analysis, we can observe the following about lifecycle management for emerging devices:

- *Overlapping considerations:* From the analysis, it followed that both RRAM and FeFETs show similarities in different phases, e.g., the most important metrics and their tradeoffs. Hence, it is realistic to assume that if solutions are found for one technology, e.g., efficient in-field tests, these might also apply to the other technologies.
- *Lack of full-stack approaches:* It also became clear that there are not many full-stack approaches that target the lifecycle management of emerging memories, which results in a lost opportunity to increase product quality.
- *Feedback and wide knowledge:* Although a complete lifecycle approach is necessary for better products, this is not easy to achieve, due to the required knowledge of the full lifecycle of a device. This can be addressed by ensuring that there is ample feedback between different phases, e.g., by quickly relaying reliability information back to test engineers and designers so that the scope of problems becomes more visible.

Acknowledgment

This work was supported by the Federal Ministry of Education and Research (BMBF, Germany) within the NEUROTEC project (project numbers 16ES1134 and 16ES1133K).

References

[1] IEEE, *IRDS Executive Summary*, 2022.
[2] S. Shiratake, "Scaling and Performance Challenges of Future DRAM," in *2020 IEEE International Memory Workshop (IMW)*, May 2020, pp. 1–3.
[3] U. Schroeder *et al.*, "The fundamentals and applications of ferroelectric HfO2," *Nature Reviews Materials 2022 7:8*, vol. 7, no. 8, pp. 653–669, Mar. 30, 2022.
[4] W. Banerjee *et al.*, "Engineering of defects in resistive random access memory devices," *Journal of Applied Physics*, vol. 127, no. 5, p. 51 101, Feb. 7, 2020.
[5] H. Mulaosmanovic *et al.*, "Ferroelectric field-effect transistors based on HfO2: A review," *Nanotechnology*, vol. 32, no. 50, p. 502 002, Sep. 2021.
[6] S. Yu *et al.*, "Emerging Memory Technologies: Recent Trends and Prospects," *IEEE Solid-State Circuits Magazine*, vol. 8, no. 2, pp. 43–56, 2016.

Authorized licensed use limited to: TU Delft Library. Downloaded on July 15,2024 at 14:57:29 UTC from IEEE Xplore. Restrictions apply.

[7] S. Hamdioui *et al.*, “Memristor for Computing: Myth or Reality?” In *Proceedings of the Conference on Design, Automation & Test in Europe*, European Design and Automation Association, 2017, pp. 722–731.

[8] J. Rajski *et al.*, “The Future of Design for Test and Silicon Lifecycle Management,” *IEEE Design & Test*, pp. 1–1, 2023.

[9] R. Kashyap, “Silicon lifecycle management (SLM) with in-chip monitoring,” in *2021 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2021, pp. 1–4.

[10] Y. Zorian, “Silicon Lifecycle Management: Trends, Challenges and Solutions : Tutorial 2,” in *2023 IEEE International Test Conference in Asia (ITC-Asia)*, Sep. 2023, pp. 1–1.

[11] C. Villa *et al.*, “A 45nm 1Gb 1.8V phase-change memory,” in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, IEEE, Feb. 2010, pp. 270–271.

[12] W. Gallagher *et al.*, “22nm STT-MRAM for Reflow and Automotive Uses with High Yield, Reliability, and Magnetic Immunity and with Performance and Shielding Options,” in *2019 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2019, pp. 2.7.1–2.7.4.

[13] L. M. Poehls *et al.*, “Review of Manufacturing Process Defects and Their Effects on Memristive Devices,” *Journal of Electronic Testing: Theory and Applications (JETTA)*, vol. 37, no. 4, pp. 427–437, Aug. 1, 2021.

[14] X. Cui *et al.*, “A snake addressing scheme for phase change memory testing,” *Science China Information Sciences*, vol. 59, no. 10, p. 102 401, Oct. 1, 2016.

[15] P. Liu *et al.*, “Defect Analysis and Parallel March Test Algorithm for 3D Hybrid CMOS-Memristor Memory,” in *2018 IEEE 27th Asian Test Symposium (ATS)*, IEEE, Oct. 2018, pp. 25–29.

[16] F. Staudigl *et al.*, “NeuroHammer: Inducing Bit-Flips in Memristive Crossbar Memories,” in *2022 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Mar. 2022, pp. 1181–1184.

[17] T. Li *et al.*, “ProtFe: Low-Cost Secure Power Side-Channel Protection for General and Custom FeFET-Based Memories,” *ACM Transactions on Design Automation of Electronic Systems*, vol. 29, no. 1, 3:1–3:18, Nov. 15, 2023.

[18] M. Fieback *et al.*, “Online Fault Detection and Diagnosis in RRAM,” in *2023 IEEE European Test Symposium (ETS)*, May 2023, pp. 1–6.

[19] T. S. Copetti *et al.*, “Evaluating a New RRAM Manufacturing Test Strategy,” in *2023 IEEE 24th Latin American Test Symposium (LATS)*, IEEE, Mar. 21, 2023, pp. 1–6.

[20] H.-Y. Chen *et al.*, *Resistive Random Access Memory (RRAM) Technology: From Material, Device, Selector, 3D Integration to Bottom-Up Fabrication*. Springer Nature Switzerland AG, 2022, 33-64.

[21] Z. Fang *et al.*, “The role of ti capping layer in HfOx-Based RRAM Devices,” *IEEE Electron Device Letters*, vol. 35, no. 9, pp. 912–914, 2014.

[22] Y. Zhang *et al.*, “Evolution of the conductive filament system in HfO2-based memristors observed by direct atomic-scale imaging,” *Nature Communications 2021 12:1*, vol. 12, no. 1, pp. 1–10, Dec. 13, 2021. pmid: 34903752.

[23] A. Grossi *et al.*, “Fundamental variability limits of filament-based RRAM,” in *2016 IEEE International Electron Devices Meeting (IEDM)*, IEEE, Dec. 2016, pp. 4.7.1–4.7.4.

[24] C. Peters *et al.*, “Reliability of 28nm embedded RRAM for consumer and industrial products,” in *2022 IEEE International Memory Workshop (IMW)*, IEEE, May 2022, pp. 1–3.

[25] N. Zagni *et al.*, “Reliability of HfO2-Based Ferroelectric FETs: A Critical Review of Current and Future Challenges,” *Proceedings of the IEEE*, vol. 111, no. 2, pp. 158–184, Feb. 2023.

[26] F. Zahoor *et al.*, “Resistive Random Access Memory (RRAM): An Overview of Materials, Switching Mechanism, Performance, Multilevel Cell (mlc) Storage, Modeling, and Applications,” *Nanoscale Research Letters*, vol. 15, no. 1, p. 90, Apr. 22, 2020.

[27] C.-M. Jung *et al.*, “Two-Step Write Scheme for Reducing Sneak-Path Leakage in Complementary Memristor Array,” *IEEE Transactions on Nanotechnology*, vol. 11, no. 3, pp. 611–618, May 2012.

[28] J.-H. Yoon *et al.*, “29.1 A 40nm 64Kb 56.67TOPS/W Read-Disturb-Tolerant Compute-in-Memory/Digital RRAM Macro with Active-Feedback-Based Read and In-Situ Write Verification,” in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 64, Feb. 2021, pp. 404–406.

[29] H. Aziza *et al.*, “An Energy-Efficient Current-Controlled Write and Read Scheme for Resistive RAMs (RRAMs),” *IEEE Access*, vol. 8, pp. 137 263–137 274, 2020.

[30] H. Xun *et al.*, “Device-aware diagnosis for yield learning in RRAMs,” in *DATE 2024*, IEEE, 2024, pp. 1–6.

[31] T. S. Copetti *et al.*, “Exploring an On-Chip Sensor to Detect Unique Faults in RRAMs,” in *LATS 2022*, Institute of Electrical and Electronics Engineers (IEEE), Nov. 14, 2022, pp. 1–6.

[32] M. Fieback *et al.*, “Device-Aware Test: A New test Approach Towards DPPB Level,” in *Proceedings of the 50th International Test Conference 2019 (ITC2019)*, 2019.

[33] M. Fieback *et al.*, “Intermittent Undefined State Fault in RRAMs,” in *European Test Symposium*, vol. 2021-May, IEEE, May 24, 2021.

[34] S. Kannan *et al.*, “Sneak-path Testing of Memristor-based Memories,” in *2013 26th International Conference on VLSI Design and 2013 12th International Conference on Embedded Systems*, IEEE, Jan. 2013, pp. 386–391.

[35] P. Liu *et al.*, “Logic operation-based Design for Testability method and parallel test algorithm for 1T1R crossbar,” *Electronics Letters*, vol. 53, no. 25, pp. 1631–1632, Dec. 7, 2017.

[36] S. Hamdioui *et al.*, “Testing Open Defects in Memristor-Based Memories,” *IEEE Transactions on Computers*, vol. 64, no. 1, pp. 247–259, Jan. 2015.

[37] N. Huynh *et al.*, “Hardware Security of Emerging Non-Volatile Memory Devices under Imaging Attacks,” in *2021 International Conference on Applied Electronics (AE)*, Sep. 2021, pp. 1–4.

[38] J. Y. Kim *et al.*, “Ferroelectric field effect transistors: Progress and perspective,” *APL Materials*, vol. 9, no. 2, p. 021 102, Feb. 2, 2021.

[39] P. R. Genssler *et al.*, “On the Reliability of FeFET On-Chip Memory,” *IEEE Transactions on Computers*, vol. 71, no. 4, pp. 947–958, Apr. 2022.

[40] D. Thapar *et al.*, “Analysis and Characterization of Defects in FeFETs,” in *2023 IEEE International Test Conference (ITC)*, Oct. 2023, pp. 256–265.

[41] Y. Xu *et al.*, “Embedding security into ferroelectric FET array via in situ memory operation,” *Nature Communications*, vol. 14, no. 1, p. 8287, Dec. 13, 2023.

Authorized licensed use limited to: TU Delft Library. Downloaded on July 15,2024 at 14:57:29 UTC from IEEE Xplore. Restrictions apply.