An FM Chirp Waveform Generator and Detector for Radar

Baseband, intermediate frequency, low noise and RF power amplifiers

by

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Abstract

This report describes the design of different amplifiers that are part of an FM transceiver. This is part of a larger project, which has the objective to design a complete FM transceiver from discrete components only, meaning that IC technology is not considered.

The circuits designed are two baseband amplifiers, an intermediate frequency amplifier, a low noise amplifier and an RF power amplifier. The baseband amplifiers are implemented with a Darlington pair in common-collector configuration to achieve a high input resistance, low output resistance, and unity gain transfer.

The intermediate frequency amplifier is centered at 9.95 MHz with a -3dB bandwidth of 2 MHz. The maximum gain is 40.5 dB and can be lowered with up to 39.7 dB using a potentiometer, based on the emitter degeneration principle.

The low noise amplifier has a maximum noise figure of 1.4 dB over the RF carrier band of 88 to 108 MHz. It has a gain of 33 dB, and reaches its 1 dB compression point for an input of -33 dBm. The total harmonic distortion is less than 0.3%.

A class E power amplifier is designed with an efficiency of 72.9%, a transmit power of 3.1 W, and a gain of 31.8 dB.

Furthermore, this reports also presents a systematic design approach for amplifiers, which illustrate the core principles on which all the designs are based.

Preface

To graduate from our bachelor in Electrical Engineering, at the TU Delft, we took part in the project to design an FM transceiver, from discrete components only. We were responsible for the design of the amplifiers. This project assignment was proposed by Leo de Vreede, Marco Pelk, Masoud Babaie and Morteza Alavi.

Overall, it has been a valuable experience for us, in which we tackled an assignment that seemed mighty and overwhelming at the start, but became manageable by using the skills, principles and knowledge we acquired during our bachelor. We started with the whole group by researching the complete FM transceiver, and later, in our case, the design of amplifiers.

We must say that we enjoyed this educational ride, where we learned a lot about conducting research and designing as part of a larger group. Unfortunately, as this project took place during the COVID-19 pandemic, we were not allowed to realize a physical prototype. This did allow us, however, to increase our focus on the theoretical background of our designs.

But this also meant that we had to work on the project from home. We have been physically separated from our friends, whom are our teammates, for the past 3 months. Despite the situation, we did feel a strong connection with all of them: Youri Blom, Filip Bradarić, Dimme de Groot and Roderick Tapia Barroso: thank you for this enjoyable experience! The daily interaction and assistance was pleasurable, and allowed us to flourish in our work.

We would like to thank our supervisors S. M. Alavi and M. Babaie. The weekly meetings we had together provided us with lots of useful feedback and insights. Their electronic doors were always wide open to answer all our questions, with great detail. They have been a great support during the course of the project.

In the end, we would like to thank our family and friends, especially our parents, whom are at the core of this academic achievement.

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Part I

System overview

1. Project Introduction

In this project, an FM chirp generator and detector for radar is developed [1].

RAdio Detection And Ranging (radar) is a technique used to determine range, angle and velocity of objects [2]. Currently, radar is mostly used to detect objects such as aircraft, ships and cars. It has applications in astronomy, geology, and weather forecasting amongst others [2], [3].

A schematic overview of a radar system can be seen in Figure 1.1. The principle on how radar operates is by radiating an Electromagnetic (EM) wave towards an object and measuring the reflected wave.

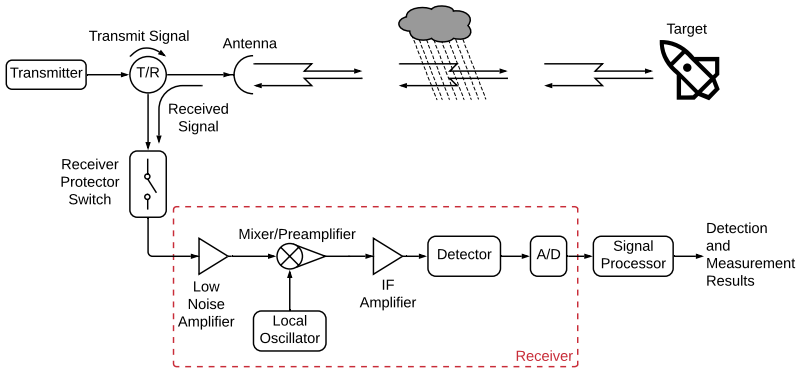

Fig. 1.1: Major elements of the radar transmission/reception concept (Based on [4]).

With the growing interest for autonomous vehicles, radar has come to play an important role in the automotive industry. Frequency-Modulated Continuous-Wave (FMCW) is often used in these radar systems [5]. State-of-the-art radar systems and a basic explanation on their operation can be found in Section 2.2.

The system designed in this thesis consists of two main parts, the first part is the transmitter (generally referred to as TX), which is used for generating and transmitting the chirp signal. The second part is the receiver (generally referred to as RX), which is used to receive and recover the sawtooth signal by demodulating the chirp signal. A top-level block-diagram of the two parts is given in Figure 1.2.

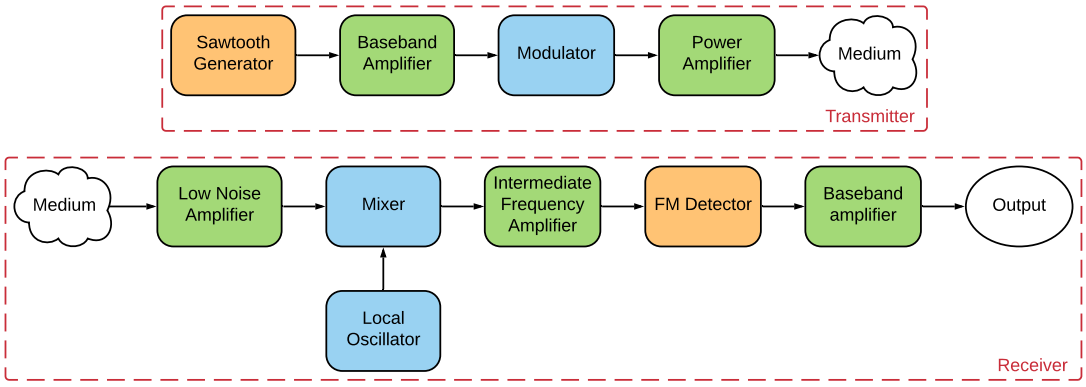

Fig. 1.2: A top level block-diagram of the receiver and transmitter architecture.

As can be seen, the system consists of many parts. These parts can be divided in a few subgroups, which are briefly described below.

- **The sawtooth generator** is formed by the sub-block depicted on the upper left of Figure

1.2. As the name states, it is used to generate a sawtooth waveform. The generated signal is also referred to as the baseband signal.

- **The amplifiers** are used to amplify the signal at different places in the system. In Figure 1.2, five amplifiers are depicted. The baseband and the Intermediate Frequency (IF) amplifier are used to amplify signals in the baseband frequency and in the IF, respectively. Both frequencies are lower than the transmit (or radio) frequency. A Power Amplifier (PA) is used to amplify the FM-signal and also forms the interface with the antenna. At the receiver side, a Low Noise Amplifier (LNA) is used to amplify the received signal. Both the PA and LNA operate at the Radio Frequency (RF). Finally, a baseband amplifier is used to buffer the signal at the output of the detector.
- **The modulator** and the **FM detector** are respectively used to modulate and demodulate the signal. The modulator oscillates at the RF, with the instantaneous frequency being determined by the amplitude of the baseband signal. This ultimately results in a chirp signal at the output. The detector is used to recover the original baseband signal. This is achieved by extracting the message signal from the phase of the IF signal to create a baseband signal.
- **The mixer** and the **Local Oscillator (LO)** are used to shift the frequency of the output of the LNA to an IF. This simplifies the design of subsequent stages in the receiver. It should be noted that, just like the modulator, the LO is a Voltage Controlled Oscillator (VCO).

1.1 Project Objective and Problem Definition

The rise of autonomous vehicles has sparked the interest in high-end radar sensors from industry. This project aims to introduce students to RF circuit design from an educational perspective by allowing them to design the needed subsystems for a basic FM chirp waveform transmitter and receiver.

As the attentive reader might have noticed, the proposed system architecture does not actually resemble a complete radar system. Because the development of a full radar system lies beyond the scope of a Bachelor thesis, this project constrains itself to the development of a separate receiver and transmitter part. Ultimately, the goal is to be able to modulate a sawtooth signal and transmit this over a range of at least five meters, after which the sawtooth signal should successfully be recovered at the output.

To facilitate designing the system in three subgroups, the previously described modules are split into three parts.

1. The amplifiers
2. The modulator, mixer and local oscillator
3. The FM detector and the sawtooth generator

This thesis focuses on the development and simulations of the amplifiers.

1.2 Methodology

In order to arrive at a working transceiver design, it is important to have the means to reliably simulate and validate the designed circuits. For this purpose, Advanced Design System (ADS) is used. ADS is a software package developed by Keysight technologies. Furthermore MATLAB is used for processing the data obtained from ADS. It is also used to generate figures of the data for aesthetic reasons. Finally, Scheme-it from DigiKey is used to draw the schematics.

Note that, under normal circumstances, the designed circuits would have been validated by physical prototyping. However, in light of the current COVID-19 pandemic, the circuit validation is also done in ADS.

1.3 Thesis synopsis

In this thesis, the design of the amplifiers required in the FM transceiver are discussed.

In Chapter 2, the basic theory of frequency modulation, as well as frequency-modulated continuous-wave signals are discussed. Some mathematical background is provided on the FMCW radar.

In Chapter 3, the program of requirements for the entire system is presented. These requirements are specified for the complete system, and more detailed requirements will be provided at the chapters discussing the specific amplifiers.

Before the amplifier designs will be discussed, a systematic approach to design is presented in Chapter 4. This includes some guidelines regarding the selection of the transistor.

In Chapter 5, the design of both baseband amplifiers is treated. The design of only one amplifiers is discussed in detail, due to the similarity between both. Finally, the results of both amplifiers are presented, and compared with the requirements.

The intermediate frequency amplifier will be discussed in Chapter 6. This amplifier is designed with the purpose to amplify only a specific, narrow, high frequency band. The filters of this amplifier are designed using the equations derived in Appendix E. The discussion of the simulation results also includes an integrated test with the FM detector, designed by another sub-group [6].

In Chapter 7, the design of the Low Noise Amplifier is discussed. The design procedure of the matching networks, at the input and output of the amplifier, is shown, and the trade-off between noise and gain is explained. Finally, the results for the LNA over the specified FM band are presented, including a verification on the stability of the amplifier.

In Chapter 8, the RF power amplifier is discussed. The power amplifier is responsible for providing the power over the transmit antenna. In this chapter, the relevant amplifier classes will be analysed, and a class E amplifier design will be realised. The chapter concludes with a discussion of the results, simulated for the RF band.

After all the amplifier designs are discussed individually, a final conclusion will be provided in Chapter 9. Along with this conclusion, some recommendations for future improvements on the system will be given.

Appendix A contains an analysis of the power, noise and gain regarding the complete system. The basics of using BJTs for amplifier design are discussed throughout Appendix B till D. Also, the derivations for the filter equations of the IF amplifier are given in Appendix E. Finally, the MATLAB scripts used during this project are provided in Appendix F.

2. Frequency Modulation

In radio technology, signals are typically modulated before transmissions using different modulation techniques. An advantage of using modulation techniques is that a specific bandwidth can be assigned to every user, such that there is little interference. One of the modulation techniques is Frequency Modulation (FM), which is used for this project. An advantage of FM is that the amplitude of the carrier is constant which means that the power is constant. Another advantage is that the information is not present in the amplitude of the signal meaning that it is less susceptible to noise [7]. This is not the case for Amplitude Modulation, where the information signal is incorporated in the amplitude of the carrier.

2.1 Mathematical theory

In FM, the instantaneous frequency of the transmitted signal is changed according to the information signal, as shown in Eq. (2.1) and Eq. (2.2) found in [8].

$$s(t) = A_c \cos\left[\omega_c t + \theta(t)\right] \tag{2.1}$$

where

$$\theta(t) = D_f \int_{-\infty}^{t} m(\tau) d\tau \tag{2.2}$$

where D_f is the frequency deviation constant, $m(t)$ is the information signal and ω_c is the carrier frequency.

The instantaneous frequency of the signal is $f_i(t) = f_c + \frac{1}{2\pi} D_f m(t)$. To make sure that the frequency range does not interfere with other neighbouring signals, the deviation of the frequency should not be too large. The frequency deviation can be determined by Eq. (2.3).

$$\Delta F = \frac{1}{2\pi} D_f V_p \tag{2.3}$$

where

$$V_p = \max\left[m(t)\right] \tag{2.4}$$

A practical example of FM can be seen in Fig. 2.1 where a carrier wave is being modulated by a sawtooth signal. The frequency range of the transmitted signal is centred around ω_c. At the receiver, this signal has to be demodulated to obtain the original signal.

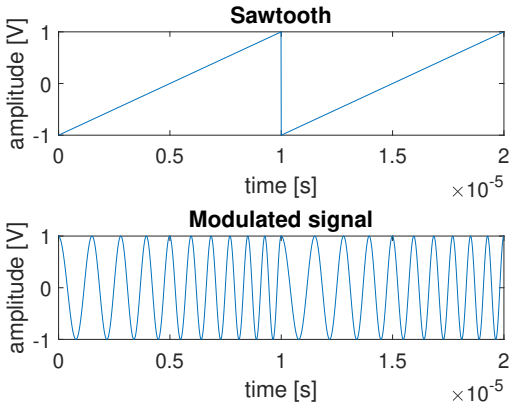

Fig. 2.1: The waveform of the sawtooth signal and the modulated signal.

2.2 Frequency-Modulated Continuous-Wave

Frequency-Modulated Continuous-Wave (FMCW) is a special type of FM where the modulation signal is a periodic wave. The reflected signal can be used to estimate the speed and distance to objects. The transmitter and receiver are placed at the same location and the receiver will receive the reflected signal that was sent by the transmitter. When comparing the difference between the received signal and the transmitted signal, the distance can be determined. A visualisation of the relevant parameters is shown in Fig. 2.2.

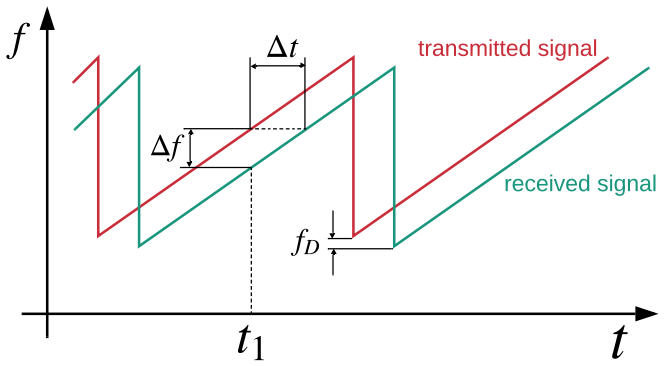

Fig. 2.2: The relevant parameters for determining the distance using FMCW.

From Fig. 2.2, it can be seen that the received signal has a phase shift compared to the transmitted signal caused by the propagation time. Since the signal is propagating with the speed of light c_0, the distance R can be determined using Eq. (2.5) [9].

$$R = \frac{c_0|\Delta t|}{2} = \frac{c_0|\Delta f|}{2\frac{df}{dt}} \tag{2.5}$$

There is a maximal distance that can be measured, given by Eq. (2.6), due to the fact that the signal is periodic. This equation is derived in [10, p. 17]. If the phase shift is larger than the period time T, it cannot be distinguished from which period the signal originated.

$$R_{max} = \frac{c_0 T}{2} \tag{2.6}$$

FMCW is not only limited to measuring the distance, but also the speed can be measured. Due to the Doppler effect [11], the frequency spectrum of a signal will shift by an amount of f_D. This frequency shift can be measured and therefore be used to determine the speed. For this project, a sawtooth is used as the modulation signal, for which the Doppler effect has a negligible influence [9] and cannot be distinguished from Δf. Therefore, the transceiver of this project cannot be used to accurately determine the distance of moving objects nor their speed.

3. Programme of Requirements

The goal of the project is to design an FM chirp generator and detector. The application in mind would be to integrate the design in cars for remote sensing applications. The complexity of the design for such an application lies outside the scope of this Bachelor project, since it requires the design to be in the GHz range (FMCW), using IC technology. For educational purposes, the requirements are simplified. The operational frequency must be in the FM radio band, and discrete components are allowed only. Needless to say, the end result of this project will not be near an applicable nor commercially competitive consumer product. The legal limit of power transmission in the FM radio band without a license will therefore also not be adhered to.

3.1 System requirements

The following specifications and requirements apply to the full transceiver system. The requirements are given by, or derived from, the specifications provided by the project supervisor [1]. Requirements governing the performance of the subsystem are discussed in the respective theses and chapters, and are based on the following:

Functional requirements:

- SYS0: The transceiver must be composed of discrete components only.
- SYS1: Frequency Modulation (FM) must be used.
- SYS2: The modulation signal must be a sawtooth waveform.
- SYS3: The sawtooth waveform must be recoverable over a minimum distance of 5 m.
- SYS4: The receiver must drive the recovered signal over a 50 Ω dummy load.

Non-Functional requirements:

- SYS5: The Radio Frequency (RF) carrier wave must be tuneable from 88 MHz to 108 MHz.
- SYS6: The FM modulation bandwidth must be between 180 kHz and 400 kHz.
- SYS7: The receiver noise figure must be lower than 5 dB.
- SYS8: The Signal-to-Noise Ratio (SNR) at the receiver output must be greater than 30 dB.
- SYS9: The transmitted power must be at least 100 mW.
- SYS10: The transmitter efficiency must be higher than 50%.
- SYS11: The total power consumption of the transceiver must be less than 10 W.
- SYS12: The transceiver must operate on a 12 V power supply.
- SYS13: The antennas provide a 50 Ω resistive load or source impedance.

3.2 Assumptions and disclaimers

- The detected waveform is only used to drive a 50 Ω dummy load. Processing the signals to perform distance measurements is outside the scope of the project.
- Antennas are assumed to be 50 Ω purely resistive: This simplifies the project to fit in the available timespan.
- The specified transmission power in the FM radio band is illegal [12]. However, the design will not be physically realized.
- The power consumption limit and supply voltage are chosen with the idea to be suitable for car applications.

4. Systematic Design Approach

To design all the different types of amplifiers, a systematic approach is needed. The first step is to evaluate the need of an amplifier. This step must be followed by a conceptual design of the required amplifier. Transforming this into an actual implementation requires an understanding of the core device, namely the transistor. For linear operations, contrary to switching applications, bipolar transistors are the preferred choice over MOSFETs [13, Ch.1].

This chapter starts with a focus on the most important characteristics of the transistor, followed by explanation on the need for clear interface requirements between other stages, which enhance the design orthogonality. In conclusion, a flowchart is presented that summarizes the design of an amplifier.

4.1 Transistor characteristics

When designing an amplifier, the characteristics of the transistor are important for achieving the required results. What follows is a non-exhaustive list of essential properties. A more detailed description of the BJT characteristics can be found in Appendix B.

Current gain

The current gain of the bipolar transistor is the essence of its amplification. It is defined as the ratio of the collector current to the the base current, denoted as β. What complicates the design, however, is that the current gain is typically specified for a wide range, e.g., 50 - 200. Furthermore, it is frequency-dependent and volatile to temperature. This implies that design principles must be applied to minimize the dependency on a critical value for β, making the design more robust.

Early voltage

The early voltage parameter describes the degree to which the bipolar transistor behaves as a non-ideal current source, by having a finite output resistance. Ideally, the early voltage is infinite, which means that the current remains constant in the active region. It is derived from the slope of the I-V curves. An ideal transistor has a zero slope, while a practical device has a positive slope (Fig. 4.1).

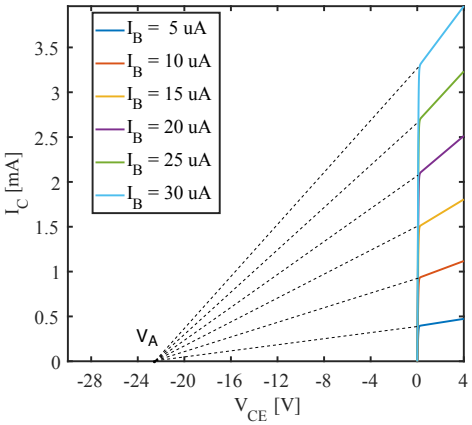

Fig. 4.1: Illustration of the early voltage of a BJT. The simulated device is the BFU630F [14].

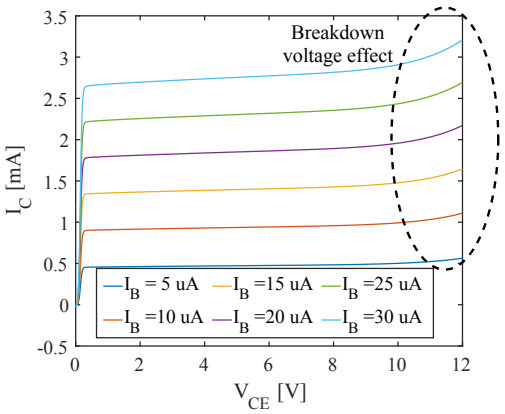

Fig. 4.2: Illustration of transistor breakdown effects. The simulated BJT is the BFU550 [15].

Breakdown voltage

Breakdown effects occur when the limitations on the device stress are approached. An increasing collector-emitter voltage can lead to a breakdown of the junction, where it starts conducting independent of the base voltage. It should be noted that by approaching the device's maximum ratings, the effects are already noticeable. This is illustrated in Fig. 4.2.

Transition frequency

The transition frequency is the current-gain-bandwidth product of a transistor. This metric implicitly states up to what frequency this transistor is suitable for amplification. This frequency is required to be much larger than the actual operational frequency.

Other important aspects of the transistor to consider are the parasitic capacitances such as the collector-base capacitance. These parasitics reduce the gain of the transistor for increasing frequencies.

The selection of the appropriate transistor is essential, but elaborating on the choice for every amplifier, designed in this thesis, is omitted to avoid repetition. The selection is always based on the above parameters. More on the BJT can be found in Appendix B.

4.2 Interfaces

What allows for the different stages to be designed orthogonally is an appropriate set of interface requirements. The information of the signal is presented in the voltage waveform, meaning that the amplifiers should behave as ideal voltage sensors at their input, and ideal voltage sources at their output. This is equivalent to having a 'high' input impedance and 'low' output impedance.

A matched output of the amplifier with the antenna is required to achieve maximum transmission power. Matching the antenna at the receiver side allows to extract maximum available power.

Voltage buffers, i.e., current amplifiers, are proven to be essential in making the design between stages orthogonally, and should therefore be considered to use.

4.3 Amplifier design approach

To design all the different amplifiers, a systematic approach is required. An overview of the applied approach is shown in the following figure:

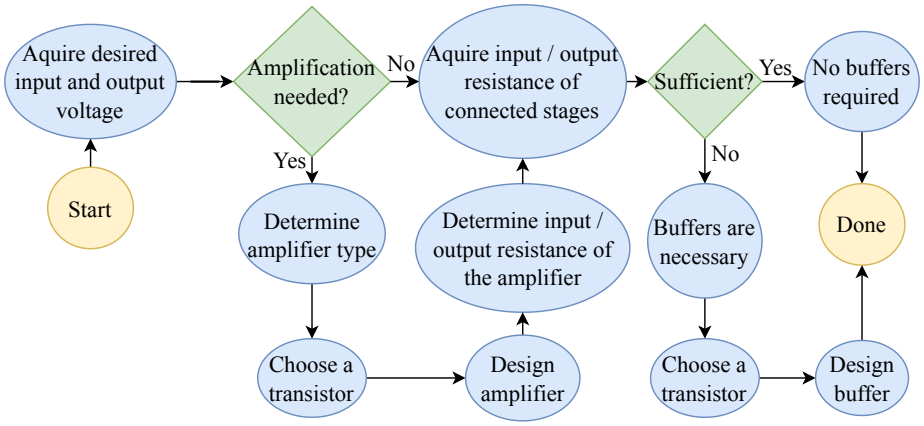

Fig. 4.3: Flowchart illustrating the process for amplifier design.

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Part II

Design

5. Baseband Amplifiers

Based on the drive capabilities of the different stages, it is found that two baseband amplifiers are required. They are referred to as BB1 and BB2:

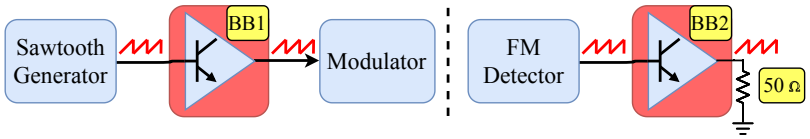

Fig. 5.1: The baseband amplifiers; residing in the transmitter and receiver.

5.1 Design requirements

Baseband amplifiers are required at both the transmitter and receiver, to increase the current drive capability of the sawtooth generator and FM detector, respectively. The following requirements follow from the output voltage of both stages, with their respective maximum deliverable current. Limits to the output resistances of the baseband amplifier are specified to constrain the internal voltage drop. The power consumption budget is derived from the total system calculations in Appendix A.

Table 5.1: Requirements and specifications for the baseband amplifiers

Category	**BB1**	**Tag**	**BB2**	**Tag**
Input/output voltage	3 V_{pp}	BB10	1 V_{pp}	BB20
Max input current	40 µA	BB10	330 µA	BB20
Max output current	1 mA	BB10	10 mA	BB20
Input resistance	$>$ 40 kΩ	BB11	$>$ 1.5 kΩ	BB21
Output resistance	$<$ 30 Ω	BB12	$<$ 5 Ω	BB22
Power consumption	$<$ 50 mW	BB13	200 mW	BB23

The baseband amplifiers must have unity voltage gain. Other important considerations are a linear phase response to preserve the shape of the wave. Note that these amplifiers will buffer a sawtooth waveform, wich has the power spread across many more harmonics than a pure sine wave. For simulation, the gain and phase shift are therefore considered up to the 10^{th} harmonic (100 kHz).

5.2 Proposed design

The baseband amplifiers are implemented as emitter followers, which have approximately unity voltage gain, and a current gain equal to β, which is in the order of 10^2. A basic schematic of an emitter follower is present in Fig. 5.2. The implementation with a Darlington pair has the advantage of a much higher current gain, or equivalently a much higher input resistance, at the cost of an extra transistor. Both transistors are biased using resistive divider biasing. Other biasing techniques could also be used, but this one has the advantage of being insensitive to fluctuations in β, if designed properly. A detailed description of common biasing techniques can be found in Appendix C.

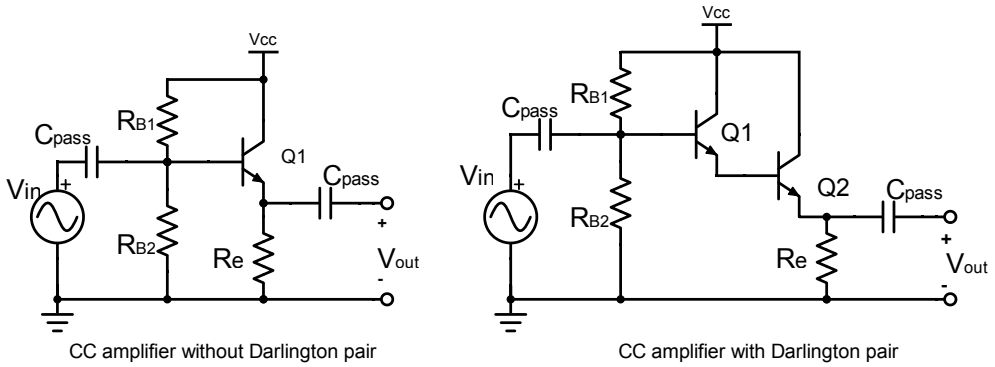

Fig. 5.2: Possible configurations for an emitter follower, known as the common-collector amplifier.

The input and output resistances are governed by Eqs. (5.1) and (5.2). The derivation for these formulas can be found in Appendix D. The Darlington pair can be viewed as a single transistor with much higher current gain, as discussed in Appendix B.

Note that these equations only hold for low frequencies, where the effect of parasitic capacitances and inductances can be ignored. This is a safe assumption for operation in the kHz range, but does not hold anymore in the MHz range, as will be illustrated in Ch. 6.

$$\text{No Darlington:} \quad R_{in} \approx R_{B1} \parallel R_{B2} \parallel [r_\pi + \beta(R_e \parallel R_{load})], \qquad R_{out} = g_m^{-1} \tag{5.1}$$

$$\text{With Darlington:} \quad R_{in} \approx R_{B1} \parallel R_{B2} \parallel \{r_{\pi_1} + \beta_1[\beta_2(R_e \parallel R_{load}) + r_{\pi_2}]\}, \qquad R_{out} = g_{m_2}^{-1} \tag{5.2}$$

where r_π equals β/g_m and the transconductance g_m is defined as

$$g_m = \frac{dI_C}{dV_{BE}} = \frac{d}{dV_{BE}}\left[I_S \exp\left(\frac{V_{BE}}{V_t}\right)\right] = \frac{I_C}{V_t}, \quad V_t \approx 26 \text{ mV for } T = 300 \text{ K} \tag{5.3}$$

where I_C is the collector current, V_{BE} the base-emitter voltage and V_t the thermal voltage.

The design of one baseband amplifier (BB1) will be discussed only, to avoid repetition because of the similarity.
First, assume that a Darlington pair is not needed, meaning that the circuit on the left of Fig. D.3 will be implemented: The output emitter node is biased at half the supply voltage, to allow for maximum voltage swing capability. The bias current is chosen to be 2.5 mA, which is more than the maximum current that should be supplied. The output resistance is also inversely proportional to the bias current, meaning that there is a trade-off between the output resistance, the power consumption and the drive capability. The calculation for the total consumption is stated in Eq. (5.4).

$$P = I_c \cdot V_{cc} + \frac{V_{cc}^2}{R_{B1} + R_{B2}} \approx I_c \cdot V_{cc} \tag{5.4}$$

The emitter resistor, R_e, is the ratio of the emitter voltage to the bias current (6V/2.5mA = 2.4 kΩ). The base voltage equals the base-emitter voltage (≈ 0.8 V) added to the emitter (6 V), and is therefore biased at 6.8 V with a resistive divider network.

To have a stable biasing network that has minimal dependency on variation in the current gain β, the current through the divider network must be much higher than the current drawn by the base of the transistor. This is equivalent to the requirement of having the biasing resistor from base

to ground, R_{B2}, being smaller than 10% of the effective input resistance of the base.

The typical value for the current gain is 90, according to the datasheet for the BFU550. Using this we find that $R_{B2} < 21.6$ kΩ. This implies that the input resistance of the baseband amplifier will be less than 21.6 kΩ, which does not comply to the minimum of 40 kΩ (BB11). This means that a new design must be used.

A Darlington pair could be used to increase the input resistance, or a single biasing resistor from the supply to the base can be used. Using a Darlington pair reduces the voltage swing capability at the output, but a fixed biasing resistor is less robust. Since the output swing requirement is relatively low (25% of the supply voltage), the suitable option is the use of a Darlington pair.

The Darlington pair raises the effective input resistance, see Eq. (5.2). This results in the requirement of $R_{B2} < 750$ kΩ. Selecting a large resistor for R_{B2} would intuitively add more thermal noise, but consider the transfer function regarding the noise contribution:

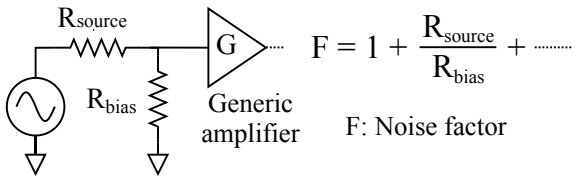

Fig. 5.3: A large (equivalent) biasing resistor counter-intuitively reduces the noise factor.

Selecting a large resistor reduces the noise factor, furthermore, the power consumption is also reduced. Also note that base should be biased at 7.6 V since it is 2 diode voltage drops higher than the emitter voltage. This fixes the ratio between R_{B1} and R_{B2}.

The final component selection for the final resistors can be seen in Table 5.2, together with the components of the second baseband amplifier.

Table 5.2: Component values for both baseband amplifiers.

Component	**Values for BB1**		**Values for BB2**	
R_{B1}	390 kΩ	± 1%	18 kΩ	± 1%
R_{B2}	680 kΩ	± 1%	32 kΩ	± 1%
R_e	2.4 kΩ	± 1%	400 Ω	± 1%
C_{pass}	47 µF	± 10%	47 µF	± 10%
Q_1 and Q_2	BFU550		BFU550	

5.3 Simulation results

As for every design, the first step in the proof-of-concept will be to simulate the operation to verify functional behaviour meeting the requirements. The final parameters of the design can be found in the following table:

Table 5.3: Comparing the requirements with the simulated results, R: Required, F: Final values

Category	**BB1 (F)**	**BB1 (R)**	**BB2 (F)**	**BB2 (R)**
Input resistance	240 kΩ	$>$ 40 kΩ	11.1 kΩ	$>$ 1.6 kΩ
Output resistance	15.4 Ω	$<$ 30 Ω	3.6 Ω	$<$ 5 Ω
Power consumption	31 mW	$<$ 50 mW	186 mW	$<$ 200 mW

The amplifiers are, amongst others, simulated with a sawtooth waveform to examine the frequency response. The input signal is composed of 10 harmonics, up to 100 kHz. Simulation results for both amplifiers are found next:

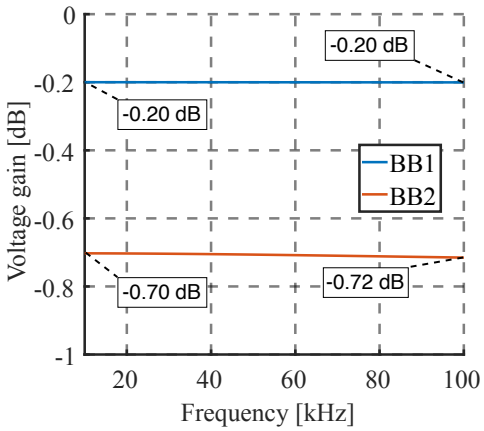

Fig. 5.4: Voltage gain of both the baseband amplifiers

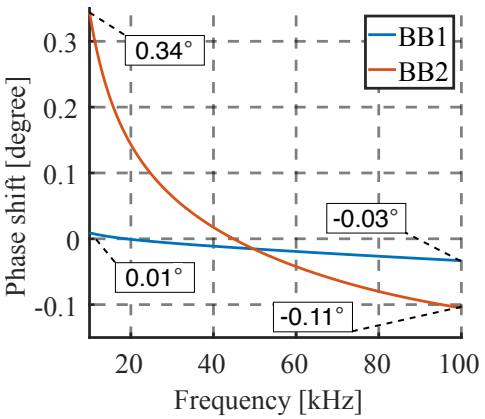

Fig. 5.5: Phase shift of both the baseband amplifiers

From Fig. 5.4 and 5.5, it can be seen that both baseband amplifiers meet all the specified requirements. The gain is not exactly unity, but stays constant up to the 10^{th} harmonic. And the phase response does not vary more than 0.5°.

6. Intermediate Frequency Amplifier

The mixer stage at the receiver, succeeding the low noise amplifier, shifts the carrier wave to a lower intermediate frequency (IF), which is higher than baseband. The signal is filtered and amplified at this new frequency, done by the IF amplifier. The use of an intermediate frequency is not a must to have a functional receiver, but using it brings several advantages [16, Ch.1], [17]:

- The FM detector does not require to be tuneable over the full FM band where the carrier wave resides. It can now be designed for a fixed and much lower frequency.
- IF filters require a lower quality factor than RF filters for the same bandwidth: in our case, this is the 400 kHz modulation bandwidth.

Using an IF stage does not only come with benefits, however. On of the main disadvantages is the need of an additional stage in the receiver, which consumes power, contributes noise, requires physical space and comes with a price.

Choosing the IF is a trade-off: The common standard for FM radio is 10.7 MHz, as this equals approximately half the full FM band of 20 MHz. A higher IF improves the separation from image frequencies, which is advantageous, but having a high IF defeats one of the main purposes of using an IF, namely, the need for filters less sharp. Considering these trade-offs and our RF bandwidth of 20 MHz, the IF is chosen to be 10 MHz.

6.1 Design requirements

The purpose of the intermediate frequency amplifier is to suppress all unwanted frequencies received or produced by the mixer and to amplify the frequency range of interest. The following requirements quantify this behaviour and are necessary to achieve the overall system requirements (Chapter 3). They are the result of many trade-offs between all receiver stages, mainly concerning gain, loading effects and drive capability.

Table 6.1: Requirements and specifications for the IF amplifier

Category		**Tag**	**Category**		**Tag**
Max voltage gain	> 40 dB	IF0	Voltage gain adjustability	> 40 dB	IF1
Max output voltage	5 V_{pp}	IF2	Max output current	2 mA	IF3
Input impedance	> 30 kΩ	IF4	Output impedance	< 30 Ω	IF5
Center frequency	10 MHz	IF6	Gain loss at 9.8, 10.2 MHz	< 0.25 dB	IF7
- 3dB bandwidth	< 2 MHz	IF8	Gain roll-off	> 40 dB/dec	IF9
Total harmonic distortion	$< 1\%$	IF10	1 dB gain compression input	> 1 V	IF11
Noise Figure IF stage	< 20 dB	IF12	Power consumption	< 200 mW	IF13

The details of the above requirements are explained as follows: IF0 accounts for the gain of the IF stage. It follows from the system calculations in Appendix A. The gain must be adjustable so that "large" signals can be received, without the output becoming saturated. The output voltage and current drive capability specs follow from the requirements of the FM detector, designed by [6].

Loading the mixer (preceding stage) affects its internal current to voltage conversion at its output, which takes place with a resistor of 3 kΩ. The input impedance of the amplifier must therefore be at least 30 kΩ (IF4). The internal voltage drop at the output is at max 2% due to the limit on the output impedance (IF5). This is considered to be acceptable.

The gain loss for the 400 kHz wide modulation bandwidth is limited to 0.25 dB. This limits the Amplitude Modulation (AM) produced by the IF amplifier. It would be ideal if the FM detector, which succeeds the IF amplifier, is insensitive to AM. This does of course not hold for a practical design. Some remaining specs quantify the performance of the amplifier as a bandpass filter. The

power consumption and noise performance follow from the link budget calculations in Appendix A.

6.2 Conceptual design

Many different topologies exist that implement the two core principles: amplification and filtering. They can be categorized on performance metrics such as gain, linearity, selectivity, stability etc. But the complexity of the design is another important detail. Furthermore, will the design be sensitive to board parasitics or electromagnetic interference? An extensive discussion of possible implementations is outside the scope of this thesis, interested readers are therefore kindly referred to [18] and [19].

The implemented topology is shown in Fig. 6.1: The amplifier must have a 40 dB/dec roll-off, for both increasing and decreasing frequencies (IF9). An obvious candidate would be a single 4th order bandpass filter (BPF). But having two, separate, 2nd order BPFs, could reduce design complexity. This can be realized with a BPF at the input, and a BPF at the output (Fig. 6.1). The premise of reduced design complexity does only hold when the two filters have minimal interference.

Also, asymmetric filtering, at either input or output, has been considered. But the interference between, e.g., a lowpass and bandpass filter at the input, increases the design complexity again.

The required voltage gain of 40 dB can be realized with a single common-emitter (CE) stage. Also, voltage buffers are necessary to improve the input and output impedance, but also to minimize interference from the other stages with the bandpass filters, enhancing orthogonal design.

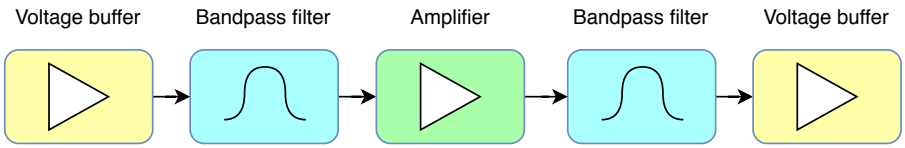

Fig. 6.1: Conceptual design of the intermediate frequency amplifier.

6.3 Proposed design

The final design of the IF amplifier is shown in Fig. 6.2. The circuit is an implementation of the topology discussed in the previous section. A qualitative explanation of the design will be provided in the next part. Afterwards, design equations will be presented and used to determine suitable component values.

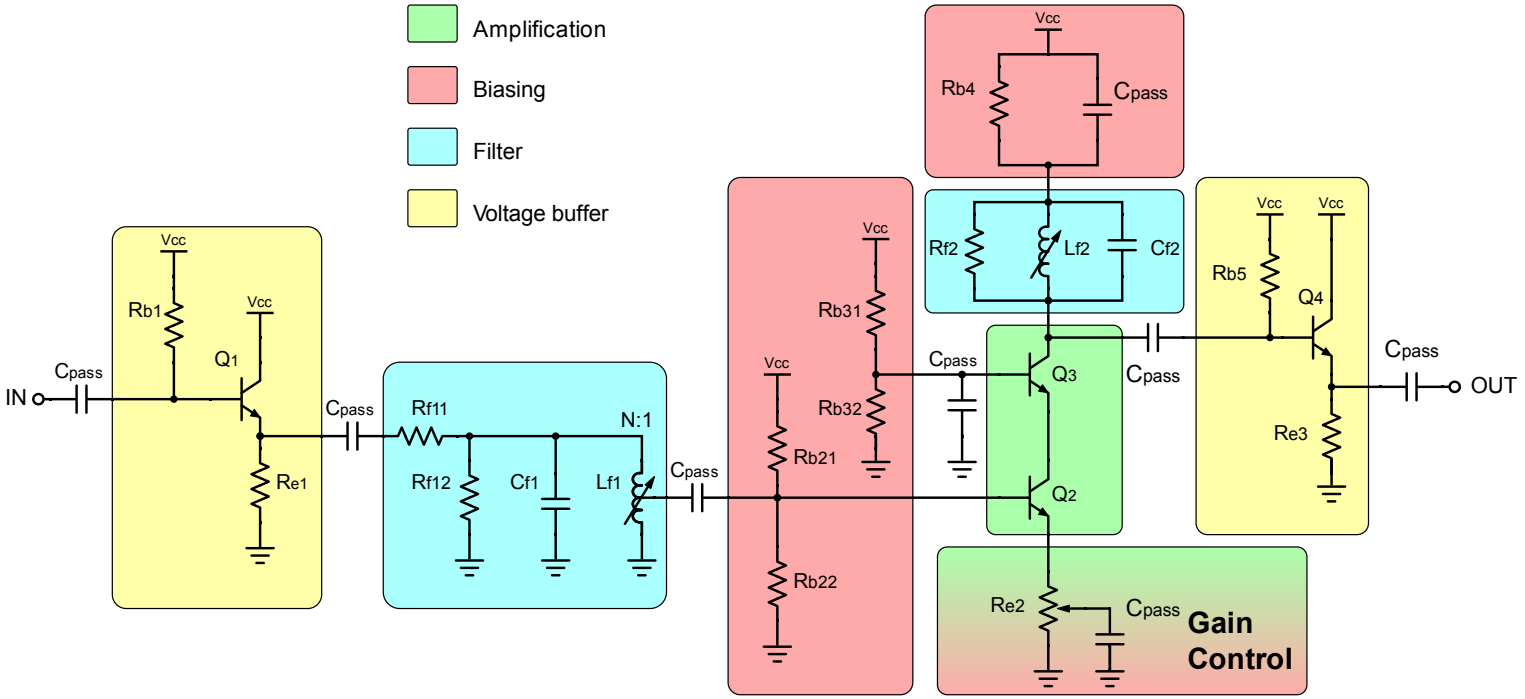

Fig. 6.2: The designed intermediate frequency amplifier: Voltage buffers improve the interface of the design. Two separate 2nd order BPFs are used. The tapped inductor L_{f1} reduces the loading from the amplification stage on the input filter. The inductors must be tuneable to center the sensitive narrowband filters. Q_2 and Q_3 form a cascode stage that achieves high gain while removing the Miller effect.

Table 6.2: Components of the complete IF amplifier. Unless otherwise stated, the components have a ± 1% tolerance.

V_{cc}	12 V	R_{b1}	100 kΩ	R_{b32}	6.2 kΩ	R_{e3}	3.9 kΩ	C_{pass}	100 nF	±10%	L_{f1}	1.05 µH	selfmade
Q_1		R_{b21}	6.2 kΩ	R_{b4}	300 Ω	R_{f11}	220 Ω	C_{f1}	240 pF	±2%	L_{f2}	6.8 (3.9 - 7.4) µH	Nr: BV-3.9-7.4
⋮	BFU550	R_{b22}	3.3 kΩ	R_{b5}	130 kΩ	R_{f12}	2 kΩ	C_{f2}	37 pF	±2%	R_{e2}	300 - 0 Ω	potentiometer
Q_4		R_{b31}	4.3 kΩ	R_{e1}	4.3 kΩ	R_{f2}	1.6 kΩ	N	4				

6.3.1 Qualitative explanation

The voltage buffer at the input stage reduces the loading of the IF amplifier on the mixer. The buffer can be seen from its input as an "ideal" voltage sensor. From its output, it is equivalent to an "ideal" voltage source with a low output resistance (few Ω). It minimizes interference from the previous stage on the filter. The filter is implemented as a parallel RLC tank in series with a resistor. At resonance, the input signal passes through a resistive voltage divider (signal gets damped). Out-of-band frequencies are pulled to ground by the LC tank, and a narrower band can be obtained by adding the series resistor R_{f11}. A higher resistance makes the band narrower. Resistor R_{f12} also limits the Q-factor of the LC tank (which is related to the bandwidth). Furthermore, the series resistance of the inductor can be modeled as parasitic parallel resistance, proportional to the finite Q-factor. To compensate for this non-ideality, R_{f12} should be selected higher than what is calculated.

The amplification stage (including its biasing network) has a finite input impedance and therefore loads the first BPF. A purely resistive input impedance could be compensated for by changing R_{f12}, but this is more difficult for the varying input capacitance of the transistor! A robust solution is to use an auto-transformer (tapped inductor). Since the number of turns on the side of the BPF is higher, the load resistance and capacitance on the secondary side, as seen from the primary side, are increased and decreased by the square of the turns ratio, respectively. This is also illustrated in Fig. 6.3. One notion about the autotransformer, however, it reduces the voltage amplitude. Choosing the turns ratio is therefore a trade-off between gain and filter performance.

Resistive divider biasing is usually preferred, as this is more stable for variations in the current gain, compared to a single biasing resistor. These variations result from manufacturing tolerances, temperature, humidity, etc., and are therefore out of control. The emitter resistance, R_{e2}, stabilizes the biasing with feedback, but also reduces the AC gain. Using a potentiometer, parallel to an AC bypass capacitor, the gain of the IF amplifier can be tuned over a wide range. Since the complete potentiometer is in series with the emitter, the biasing does not change.

A cascode structure is used instead of a single transistor, to minimize the impact of the Miller effect, which increases the collector-base capacitance by a factor of the voltage gain (see Appendix B.3. The cascode structure is formed by two transistors, Q_2 is in common-emitter configuration, and Q_3 is in common-base configuration. Other advantages of the cascode are that the Early effect is reduced and the device stress is decreased [19, p. 669-671].

The second BPF is located at the collector node. It is chosen to implement an RLC tank, instead of a capacitive BPF. Using capacitors only, has the advantage that it does not require an inductor, which is usually larger in size and more sensitive to parasitic coupling and interference. But the RLC tank is more suited to achieve the narrow-band filter response.

Since the inductor is a short for DC, the RLC tank can not bias the transistors Q_3 and Q_4. The biasing resistor R_{b4} is therefore added, but this resistor is bypassed for high frequencies, to design the biasing network and the filter independent of each other, enhancing design simplicity.

A voltage buffer, implemented as an emitter follower, is used at the output stage. This reduces the loading of the FM detector on the bandpass filter at the output, allowing the design to be done orthogonally.

6.3.2 Using design equations

Biasing the cascode: The first step is to design the biasing network of the amplification stage. The equivalent circuit under DC is as shown on the left in Fig. 6.3. The biasing current I_{Rb4} which flows through the collectors of Q_3 and Q_4 is chosen to be 10 mA. Decreasing the bias current reduces the maximum available gain.

Recall the supply voltage to be 12 V. Node V_{c3} is biased at 9 V. The maximum output swing is required to be 5 V_{pp} (IF2), meaning that this node oscillates between 11.5 V and 6.5 V. Having 11.5 V across a single transistor drives the device in its non-linear region (breakdown effects, discussed in Section 4.1). The cascode, however, has the advantage of reducing the device stress, since the voltage will be divided among Q_2 and Q_3. The maximum stress on Q_4 is also reduced by increasing the bias point. The emitter bias point of Q_4 follows by subtracting a diode voltage drop, of 0.8 V, from V_{c3}.

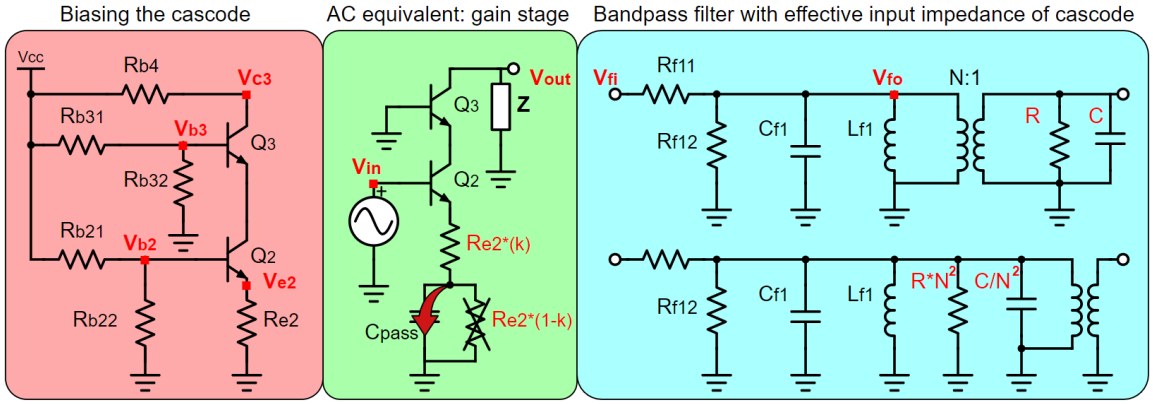

Fig. 6.3: Equivalent circuits obtained from different parts of the IF amplifier. Left: the amplification stage under DC conditions. Middle: The amplification stage, under AC conditions (ignoring the biasing resistors). Right: The input bandpass filter; the tapped inductor is equivalent to a single inductor, parallel to an ideal transformer, in case of perfect magnetic coupling.

Resistor R_{b4} is (12 V - 9 V)/10 mA = 300 Ω. The selection of R_{e2} is a trade-off. A large resistor, compared to R_{b4}, has a significant DC voltage drop. Since Q_2 and Q_3 therefore have less voltage "to share", their operating point shifts closer to saturation, which is undesired. But a large resistor gives more gain control under AC conditions. Furthermore, the input resistance increases by increasing the emitter resistor. To have a biasing network independent of the current gain β, the input resistance of the amplifier becomes roughly $\beta R_{e2}/20$ (see Appendix C). Considering all these trade-offs, a 300 Ω resistor is selected. This leaves, for DC, 6 V in total for both transistors.

Node V_{e2} is at 10 mA · 300 Ω = 3 V. Therefore V_{b2} is at 3 V + 0.8 V = 3.8 V. Assuming Q_2 and Q_3 divide the bias voltage equally, V_{b3} will be at 0.8 V + 0.5 · (9 V + 3 V) = 6.8 V. The resistive dividers convert the DC supply voltage to the required bias voltage. It is desirable to have the resistor from the base node to ground (e.g. R_{b22}) to be much smaller than the effective resistance looking into the base (e.g. βR_{e2}), a factor 10 suffices. This ensures the biasing network to be insensitive to fluctuations in the current gain β. The selected components are in Table 6.2.

The biasing networks for the voltage buffers are designed in a similar procedure. Care should be taken when selecting the bias current, it should be greater than the peak output current that has to be delivered. Typically a 20 - 30 % margin is used, a higher bias current would needlessly increase the power consumption.

Amplification: The gain of the cascode stage, G_{CC}, is expressed in Eq. (6.1), where $Z(j\omega)$ equals the impedance of the BPF at the output, and g_m is the transconductance of Q_3. The amplification is proportional to the frequency response of the tank.

$$|G_{CC}(j\omega)| = \frac{|V_{out}|}{|V_{in}|} = \frac{g_m|Z(j\omega)|}{1+g_m R_{e2}k} \approx \frac{|Z(j\omega)|}{R_{e2}k}, \quad \text{for } g_m R_{e2}k \gg 1 \tag{6.1}$$

where $k \in [0,1]$ representing the fraction of R_{e2} not being bypassed for AC. The amount that is bypass can be adjusted with the potentiometer, allowing for gain control (Fig. 6.2). The denominator of Eq. (6.1) ranges from 1 to 116 which is a 41 dB variation. This seems to meet the requirement of 40 dB (IF1), but the verification is only done in Section 6.4.

Designing the output BPF: We have seen that the gain is proportional to the impedance of the BPF on the output. It is found to be

$$|H_{f2}(j\omega)| = |Z(j\omega)| = R_{f2} \Bigg/ \sqrt{1+(\omega R_{f2}C_{f2})^2\left[1-\left(\frac{\omega_o}{\omega}\right)^2\right]^2} \tag{6.2}$$

with

$$\omega_o = 2\pi f_o = \frac{1}{\sqrt{L_{f2}C_{f2}}}, \qquad \text{and} \qquad |H_{f2}(j\omega_o)| = R_{f2} \tag{6.3}$$

The derivation can be found in Appendix E.1.

Requirement IF7 dictates that amplitude modulation inside the modulation bandwidth should be less than 0.25 dB. Since there will be two BPFs, they can be designed to contribute both less than 0.125 dB. To obtain suitable component values, Matlab is used to solve

$$20\log_{10}\frac{|H(j\omega)|}{|H(j\omega_o)|} = -\alpha \tag{6.4}$$

where α is set to 0.1 dB. The Matlab code is in Appendix F.2.

The resonance frequency f_o is set to 10 MHz and the midband gain is chosen to be 55 dB. This gives some room for the autotransformer to decrease the gain while still meeting the amplifier requirement of > 40 dB.

Solving Eqs. (6.2), (6.3) and (6.4) results in: $R_{f2} = 1.6$ kΩ, $C_{f2} = 37$ pF, $L_{f2} = 6.8$ µH. Furthermore, the inductor is chosen to be tuneable, since the center frequency is very sensitive to component variations. The series resistance of the inductor can be modelled by an equivalent parallel resistance. It should be noted that R_{f2} should be significantly small to reduce the effects of this parallel resistance.

Designing the input BPF: The input filter is required, to add an extra 20 dB/dec roll-off, since the output filter only gives a 20 dB/dec roll-off. The combined amplifier response will achieve the overall 40 dB/dec roll-off, required to meet IF9.

The design of the input filter can be done orthogonally, due to the input buffer and the autotransformer. The benefit of the autotransformer can be seen in Fig. 6.3. The loading on the filter is decreased. The disadvantage, however, is that the voltage gain is reduced. The selection of the turnsratio N is therefore a trade-off.

The design of the filter follows the procedure of the previous one. The frequency response is

$$|H_{f1}(j\omega)| = \frac{|V_{fo}|}{|V_{fi}|} = \left(\frac{R_{f12}}{R_{f11}+R_{f12}}\right) \Bigg/ \sqrt{1+[\omega(R_{f11} \parallel R_{f12})C_{f2}]^2\left[1-\left(\frac{\omega_o}{\omega}\right)^2\right]^2} \tag{6.5}$$

with

$$\omega_o = 2\pi f_o = \frac{1}{\sqrt{L_{f1}C_{f1}}}, \qquad \text{and} \qquad |H_{f1}(j\omega_o)| = \frac{R_{f12}}{R_{f11} + R_{f12}} \tag{6.6}$$

Note the similarity between these design equations and the ones presented earlier. The total gain of the amplifier becomes

$$\begin{aligned} |G_{IF}(j\omega)| &= \frac{1}{N}|H_{f1}(j\omega)||H_{f2}(j\omega)|\frac{g_m}{1 + g_m R_{e2} k} \\ &\approx \frac{|H_{f1}(j\omega)||H_{f2}(j\omega)|}{N R_{e2} k}, \quad \text{for } g_m R_{e2} k \gg 1 \end{aligned} \tag{6.7}$$

The selection of suitable components for the input filter is an iterative process, since the system of equations to solve is nonlinear with multiple degrees of freedom. It is important to consider the scarce availability of tuneable, tapped inductors, for RF applications. Furthermore, the total voltage gain loss, due to the resistive divider and the tapped inductor, may not be larger than 15 dB, to still meet the 40 dB requirement. Other considerations are that the minimum input resistance of the filter should be much greater than the output resistance of the preceding voltage buffer.

Graphical tools in Matlab are used to display the different trade-offs, the code is in Appendix F.3. The final selection (Table 6.2) results in a minimum input resistance of $R_{f1} = 2.2$ kΩ, a 0.9 dB gain loss due to the resistive divider, and a 12 dB loss due to the autotransformer. The input filter is loaded with a 16 times higher resistance and lower capacitance, than the actual input impedance of the cascode, making them negligible ($N^2 = 16$).

6.4 Simulation results

This section presents the simulation results from ADS, and relates them to the specified requirements in Table 6.1. The source impedance, used during simulation, is a 3 kΩ resistor. This represents the output impedance of the mixer stage. The load is a 1.5 kΩ resistor in series with a 2 µH inductor. This load approximates the simulated input impedance of the FM detector, designed by [6]. The input voltage is always 5 mV_{pp}, except for total harmonic distortion and gain compression simulations.

Also, Figs. 6.12 and 6.13 are simulation results where the IF amplifier is connected to the FM detector, designed by [6].

A final remark regarding the simulations: the IF amplifier has an adjustable gain. Some figures, therefore, contain multiple graphs, where the gain is varied. This is indicated by the parameter $k \in [0, 1]$. This represents the amount of AC emitter degeneration at the cascode. The lowest gain, meaning maximum degeneration, is obtained for $k = 1$. Likewise, the gain is maximum for $k = 0$.

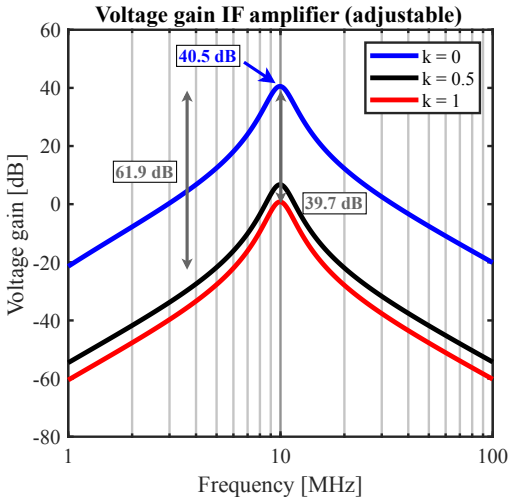

Fig. 6.4: The maximum voltage gain exceeds 40 dB, adhering to IF0. The gain is approximately 40 dB adjustable, meeting IF1. The suppression after the first decade is more than 40 dB, complying to IF9.

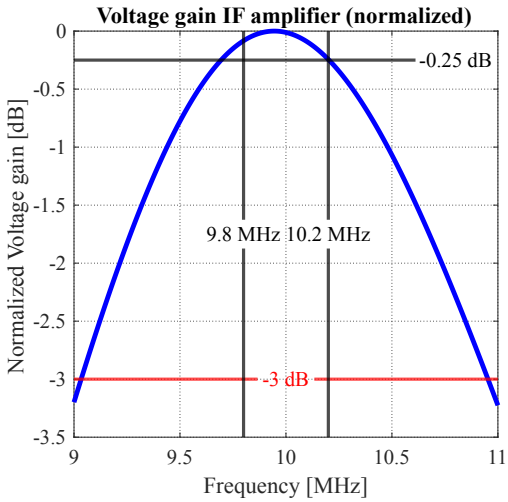

Fig. 6.5: The maximum gain loss over the modulation bandwidth (9.8 - 10.2 MHz) is less than 0.25 dB, adhering to IF7. The -3 dB bandwidth does not exceed 2 MHz, indicating its rejectivity, and thus satisfies IF8.

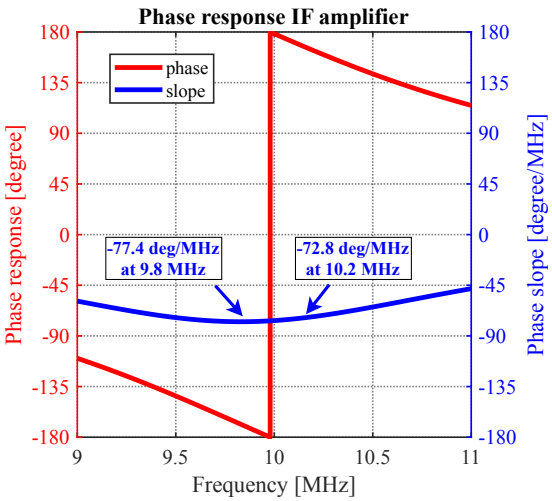

Fig. 6.6: The ideal phase response would be linear. The slope of the response is not constant, unfortunately, and has a parabolic shape, which indicates a non-linearity of the third order. The deviation, from a perfect linear response, is 1.8 degree over the modulation bandwidth of 400 kHz.

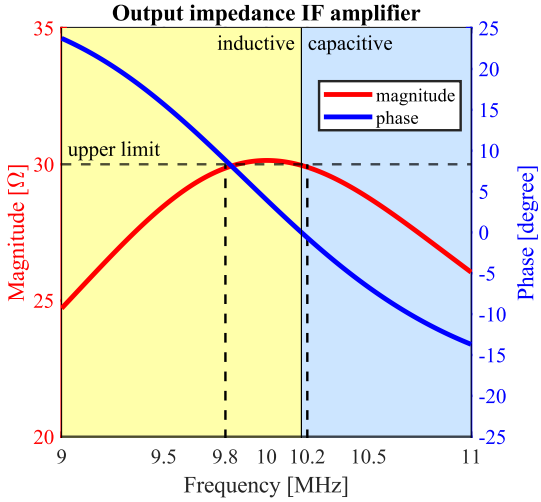

Fig. 6.7: The output impedance adheres to the maximum of 30 Ω (IF5). Notice that it is inductive over the modulation bandwidth.

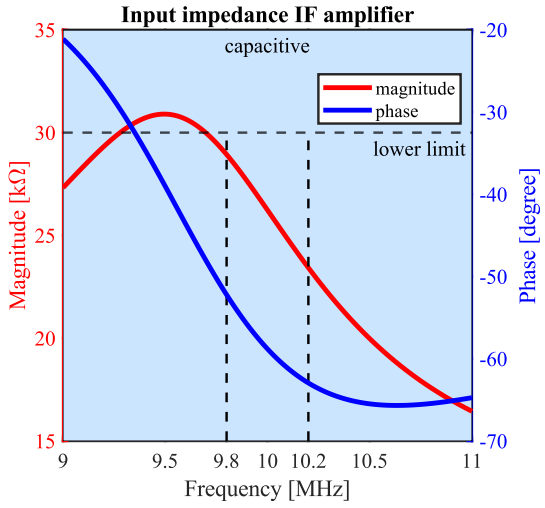

Fig. 6.8: The input impedance does not meet the minimum of 30 kΩ (IF5). The emitter follower at the input stage is not suitable for this frequency range of operation, and should be improved with a different buffer circuit. The problem is illustrated in Fig. 6.9.

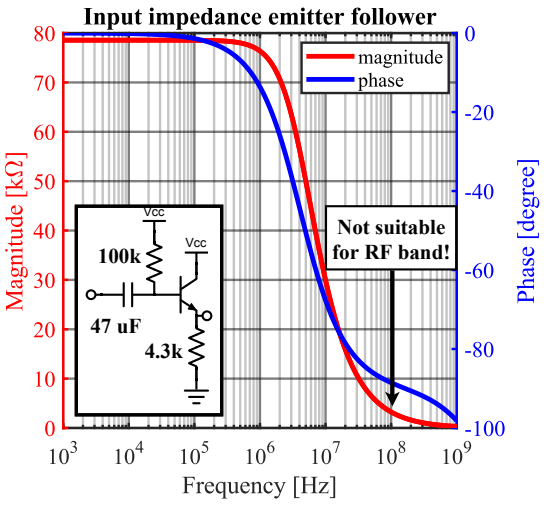

Fig. 6.9: The input impedance of the emitter follower drops significantly for frequencies above 1 MHz. This makes the circuit unsuitable for voltage buffer applications, since this requires a high input impedance.

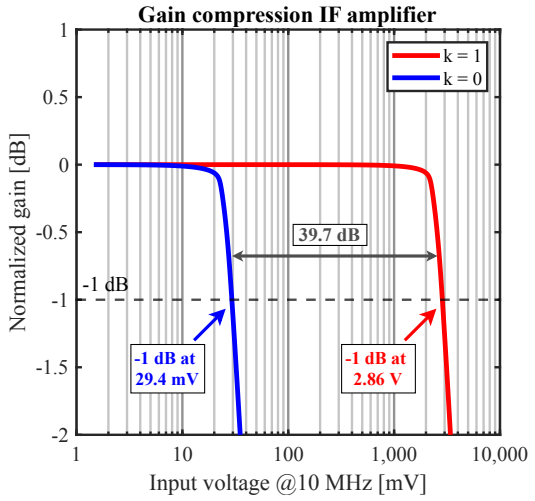

Fig. 6.10: The gain is 40.5 - 1 = 39.5 dB, for an input voltage of 29.4 mV. This results in an output voltage of 2.78 V. This means that the amplifier meets the output swing requirement of 5 V_{pp} (IF2). Notice how the 1 dB compression point moves to the right, by lowering the gain of the amplifier.

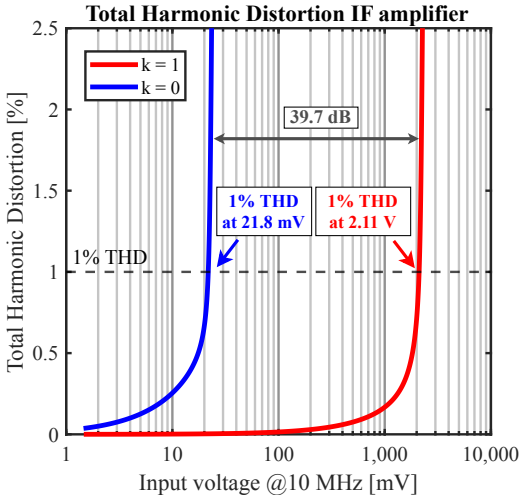

Fig. 6.11: The total harmonic distortion remains well below 1%, except when the input voltage reaches the 1 dB compression point. An input that is 'too large', causes the output to saturate, which is visible in the graph by the steep slope. The high THD for large input signals, is not necessarily bad, since it only indicates that the gain should be lowered. By reducing the gain, the output signal stays in the 5 V_{pp} limit, for which the FM detector is designed (IF2).

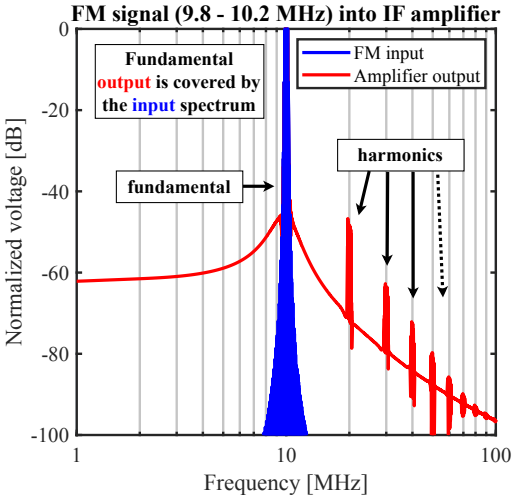

Fig. 6.12: The output spectrum of the amplifier for an FM input signal between 9.8 MHz and 10.2 MHz (transient simulation). The FM signal is generated in ADS from a baseband sawtooth wave (10 kHz) and a voltage controlled oscillator (VCO). The harmonic output is at least 47 dB lower than the fundamental.

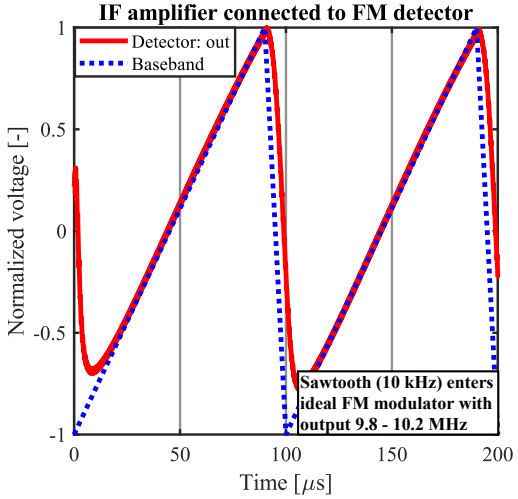

Fig. 6.13: The original baseband signal enters a VCO that generates an FM signal from 9.8 to 10.2 MHz, for testing purposes. This signal is amplified by the IF amplifier and passed through the FM detector, designed by [6]. The distortion of the recovered signal is mainly caused by the FM detector. The IF amplifier has very low distortion, as illustrated in Fig. 6.12.

Summary of the results

An IF amplifier has been designed that satisfies the requirements in Table 6.1, except for the minimum input impedance (IF4). The most important conclusions are:

- The voltage gain is adjustable between 40.5 dB and 0.8 dB.
- The amplifier is centered at 9.95 MHz instead of 10 MHz, but still complies to all requirements regarding the selectivity. It has a -3 dB bandwidth less than 2 MHz, and the gain drop is more than 60 dB after the first decade.
- The phase response is approximately linear. The deviation, from a linear response, is 1.8 degree over the modulation bandwidth of 400 kHz.
- While the output impedance satisfies the maximum of 30 Ω, the input impedance drops below the minimum of 30 kΩ. This is caused by the input buffer, an emitter follower. Its performance deteriorates for frequencies above 10 MHz, as illustrated in Fig. 6.9.
- The input signal at the 1 dB compression point ranges from -30.7 to 9.1 dBV, depending on the gain setting of the amplifier.
- The IF amplifier is theoretically stable for all source and load terminations, except for a shorted output.
- The noise figure of the amplifier is 3.9 dB, and the power consumption is 199 mW.
- The amplifier has been demonstrated, with simulations only, to work with the FM detector.

7. Low Noise Amplifier

The first stage at the receiver is the Low Noise Amplifier (LNA). Its primary purpose is to amplify the weak signal received by the antenna, without severe degradation of the signal to noise ratio (SNR). Having a high gain and low noise figure is critical to the SNR of the receiver's output.

The following chapter starts by discussing fundamental concepts regarding the LNA. This is proceeded by a step-by-step design of the LNA, as a subsystem of the transceiver. The circuit is designed and simulated in ADS.

7.1 Design considerations

The design of the LNA requires an understanding of the concepts discussed in this section.

Noise, gain and Friis equation

Electrical noise has many sources, the most prominent one being thermal noise. These sources should be minimized to improve the noise figure of the LNA. The use of resistors should therefore be avoided as much as possible. Transistors increase the gain but also introduce new noise sources such as shot noise and flicker noise.

The importance of having a high gain and low noise figure for the LNA, is emphasized by Friis formula for noise, applied in Fig. 7.1 [20]. The noise figure of the LNA directly impacts the receiver, and a high gain minimizes the impact of the subsequent stages.

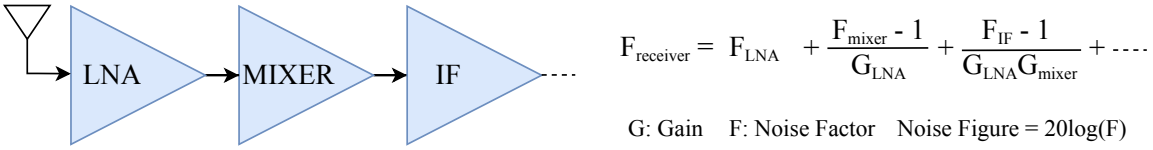

Fig. 7.1: Friis equation applied to the receiver [20]. The noise figure of the receiver is reduced by increasing the gain of the LNA, and recuding its noise figure. As can be derived from the formula, the LNA is critical to the receiver's noise figure.

Trade-off between noise and gain

An amplifier is able to achieve its maximum gain for a specific optimal source impedance. This also holds for achieving minimum noise figure. These two optimal source impedances are not equal in general, making it difficult for the designer to achieve both at the same time. Haus and Adler present a clear discussion on this optimal source impedance, in order to achieve optimum noise performance for linear amplifiers [21].

Richard continues by presenting a procedure for LNA design, that approaches maximum gain and minimum noise figure simultaneously [19, p.641]. We will apply this procedure but slightly modified. Instead of tweaking the device size parameters, which can be done in IC technology, we will replace this with the selection of the transistor.

The first step in the design is to select an RF transistor suitable for LNA applications. The second step is to choose the bias current which theoretically matches the optimal source reflection coefficient with the conjugate of the return loss: $\Gamma_{S,opt} = S_{11}^*$. A practical solution is to use the datasheet of the RF transistor, which usually displays the relation between the minimum noise figure and the bias current.

Third, an input matching network must be used to transform the source impedance of the antenna to the optimal source impedance. A practical approach is to use the S-parameter data of the transistor model, in combination with the ADS Smith Chart Utility tool, to design the matching network.

Important to realize is that the matching network may only be composed of reactive elements, to minimize power dissipation and thermal noise contribution. This implies, however, that the network has a frequency dependent response, which could lead to an undesired filter characteristic if not kept in mind.

7.2 Design requirements

It is crucial for the LNA to achieve a high gain and low noise figure, being the first stage after the antenna. The impedance of the antenna is assumed to be 50 Ω, purely resistive, as stated in Ch. 3. The following requirements are based on the system requirements in Ch. 3, and the system budget calculations, regarding noise figure, power consumption and gain, presented in Appendix A:

Table 7.1: Requirements and specifications for the low noise amplifier.

Category		**Tag**	**Category**		**Tag**
Gain	$>$ 20 dB	LNA0	Noise figure LNA	$<$ 2 dB	LNA1
-3 dB bandwidth	88 - 108 MHz	LNA2	Gain roll-off	$>$ 20 dB/dec	LNA3
In-/output impedance	matched	LNA4	Total harmonic distortion	$<$ 1%	LNA5
Stability	unconditional	LNA6	Power consumption	$<$ 100 mW	LNA7

7.3 Common LNA architectures

There are a couple of different architectures for LNA design. Some of the different design choices that come with these architectures will be discussed.

7.3.1 Resistive emitter degeneration

Emitter degeneration results in a lower but more stable voltage gain, being less dependent on the current gain β. However, adding an additional resistor also contributes noise. Also important to realize, is that the effective emitter resistance, seen from the base terminal, gets increased by β. By shifting the resistor to the base, the noise contribution gets amplified. Since emitter degeneration has a negatively impacts the overall noise figure, resistive emitter degeneration will not be used.

7.3.2 Inductive emitter degeneration

Instead of using resistive emitter degeneration, inductive degeneration can also be used. Inductive degeneration does not add any noise, unlike resistive elements. The inductor can also be tuned to match the input impedance of the amplifier to the antenna. Furthermore, the series inductor also creates a low-pass filter at the input, and any capacitance at the input of the BJT will create a series RLC resonating circuit. If this input capacitance of the amplifier is not clearly defined, a much smaller capacitance can be placed in series to tune the resonator. The Q factor of this series RLC network can be written as $Q = \frac{1}{R}\sqrt{\frac{L}{C}}$. A small capacitance will however result in a large Q factor, which is undesirable for this application since the FM signal can range from 88 MHz - 108 MHz. If this Q factor becomes too high, signals inside the desired band will be filtered out as well.

7.3.3 Biasing technique

To bias the LNA, one might consider using a different biasing technique than previously used. Instead of a voltage divider bias, a fixed biasing resistor can be used to improve the noise performance,

since the biasing resistor will typically be larger, meaning that the noise figure decreases, according to Fig. 5.3. However, due to its dependency on β, the resistive divider biasing technique is used. A more detailed explanation of the different biasing techniques is present in Appendix C.

7.3.4 Differential vs single-ended

Another option for the LNA implementation is using a differential amplifier instead of a single-ended type. A differential amplifier has the advantage of better noise suppression. If the noise or interference is common to both inputs or outputs, they will cancel each other. However, this noise suppression only works for a common noise source, and generally increases the noise figure of the LNA [22]. Another disadvantage of a differential amplifier is the design complexity. You need at least 2 transistors to form the differential pair, and often this becomes more due to current source biasing or cascode structures. For this application, a single ended LNA will be used since common noise suppression is not needed. If the transceiver would be placed inside a noisy environment, common noise suppression is desirable and a differential amplifier would be a better option.

7.4 Proposed design

The topology of the final design is shown in Fig. 7.2. The input matching network transforms the assumed 50 Ω antenna impedance to the optimal source impedance for the amplifier, which maximizes the gain and noise performance. The output matching network improves the power transfer to the next stage. Both matching networks combined must also form a bandpass characteristic.

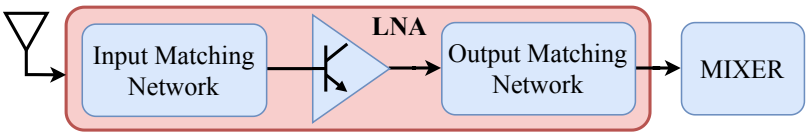

Fig. 7.2: Conceptual topology of the LNA.

The first step is to select the RF transistor. In contrast to the previous designs, which use the BFU550, the LNA will be designed with the BFU580. This transistor has a higher transition frequency (11 GHz compared to 2 GHz), despite the disadvantage of a having lower current gain. Overall, this transistor is more suitable for the operational frequency range of the LNA, being around 100 MHz.

Fig. 7.3 relates the bias current to the minimum noise figure. It is frequency dependent, where a lower operational frequency potentially improves noise performance. Selecting the bias current should consider all the requirements regarding noise, gain, power consumption, and drive capability.

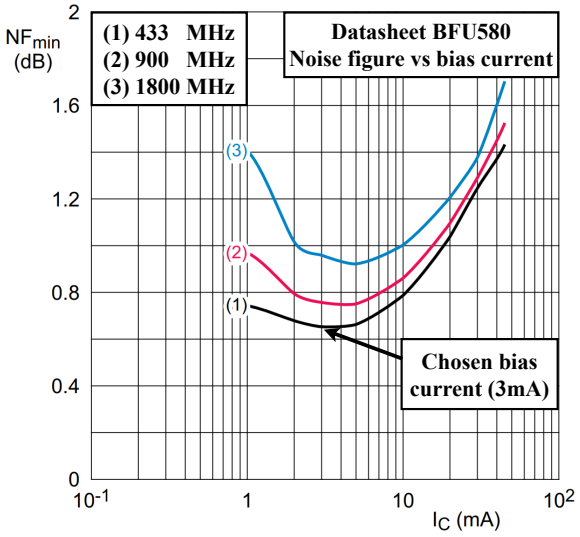

Fig. 7.3: Relation between the minimum noise figure and bias current, for the BFU580 bipolar transistor [23]: there is an optimum to exploit.

The initial design of the LNA, without any matching network, can be seen on the right. A cascode is used to remove the Miller effect. Both transistors are biased with a divider network. The DC operating point would be significantly dependent on temperature for a single biasing resistor from the supply to the base.

The advantage of a single biasing resistor, however, is that the noise figure is reduced in general, as demonstrated in Ch. 5.
The collector of Q_2 is biased around 2 V which increases the available gain compared to a symmetric biasing point (6 V). This voltage level still leaves enough swing capability at the output.

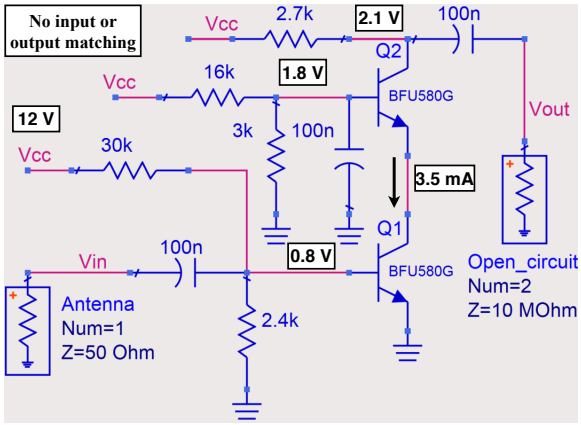

Fig. 7.4: The initial design of the LNA, without any input or output matching network.

To the right we can see the constant gain and noise circles for the circuit in Fig. 7.4, resulting from the S-Parameters simulation. The circles represent either a constant **maximum available gain** or **minimum noise figure**. Every larger circle equals a fixed relative drop in performance, the center being therefore the optimum.

We can see a clear trade-off between the noise performance and gain since the two optima are not coinciding. The current choice is to sacrifice 0.5 dB in noise performance and 1 dB in gain. Note that these results only pose a limit to what is achievable with the current design, without stating the final performance.

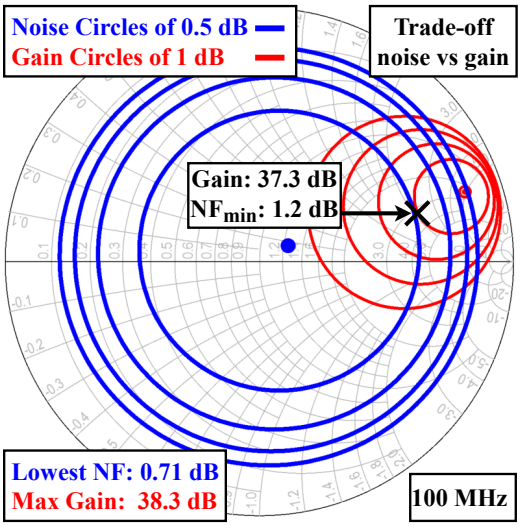

Fig. 7.5: The gain and noise circles of the circuit in Fig. 7.4, at 100 MHz.

An input matching network is designed to map the source impedance of the antenna, to the chosen point on the Smith Chart in Fig. 7.5. Two networks have been designed using the ADS Smith Chart Utility tool, which visually moves the impedance across the plane by placing series and shunt elements. An endless number of possible matching networks can be applied, but we will stick to the two options in Figs. 7.6 and 7.7, due to their simplicity and manageable frequency response. One should namely realize that the matching networks also act as filters, which can go out of design control with very complex networks.

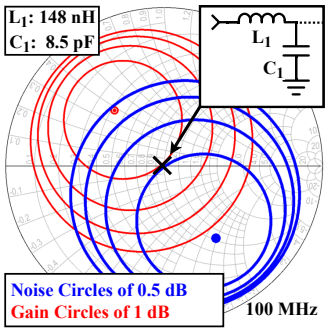

Fig. 7.6: Lowpass filter acting as an input matching network.

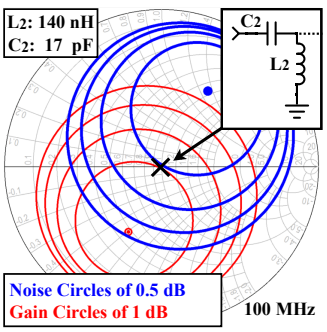

Fig. 7.7: Highpass filter acting as an input matching network.

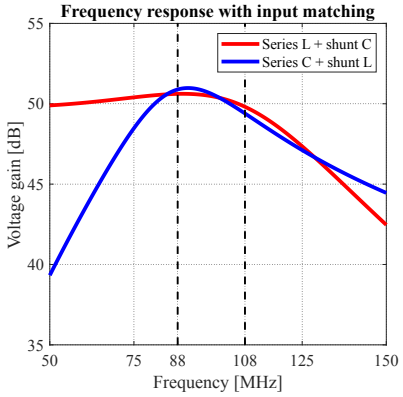

Fig. 7.8: This frequency response is obtained by adding the input matching network. The matching network is either a low- or highpass filter. Note: the voltage gain is able to exceed the maximum power gain of 38.3 dB.

From the frequency response in Fig. 7.8, we can see that the LNA already has a bandpass filter behaviour, when the input matching network is a highpass filter. This is because the gain of the transistor is decreases for increasing frequency, hence it has an inherent lowpass frequency response.

A disadvantage of this matching network, however, is that the input capacitance of the transistor adds up directly to the capacitor of 8.5 pF. Since the input capacitance is in the same order, the matching network can be significantly detuned.

Before we decide on choosing the matching network, we will design two different output matching networks, and evaluate the overall frequency response of the LNA. This approach is chosen since matching networks do not give any freedom in the design of its filter behaviour.

In other words, the required -3 dB bandwidth should be, as much as possible, approximated by the matching networks themselves. Minimal adjustments therefore have to be made afterwards, where the performance must be sacrificed to meet the filter specs.

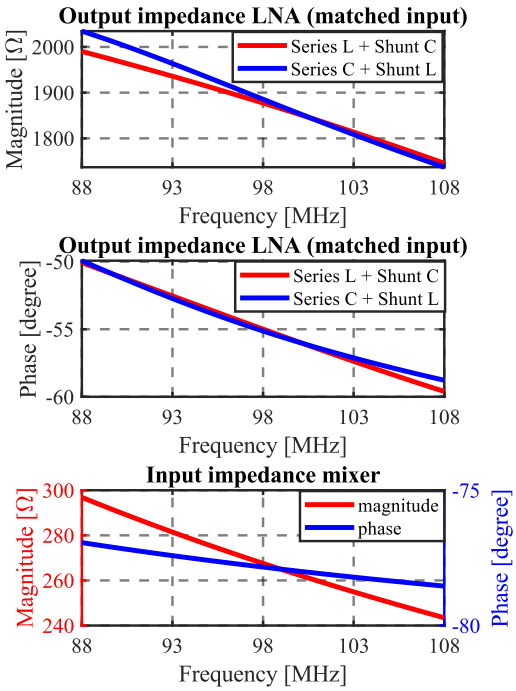

Fig. 7.9: The output impedance of the LNA, and the input impedance of the mixer, obtained from [24]. Knowing these impedances is essential to design the appropriate matching network.

The design of a matching network can only take place if the impedance on both sides is known. The output impedance of the LNA is simulated for both input networks, the results being in Fig. 7.9. The input impedance of the mixer is also displayed, which was obtained from the group responsible for its design [24].

It was demonstrated earlier that two different input matching networks are applicable, namely, a lowpass or highpass filter. At the output, therefore, we should use a highpass or lowpass filter respectively, to create an overall bandpass characteristic. By considering both, it was found that combining the highpass at the input with the lowpass at the output almost gives the desired frequency response. Minimal adjustments were required to meet the specified bandwidth. The complete design in Fig. 7.10.

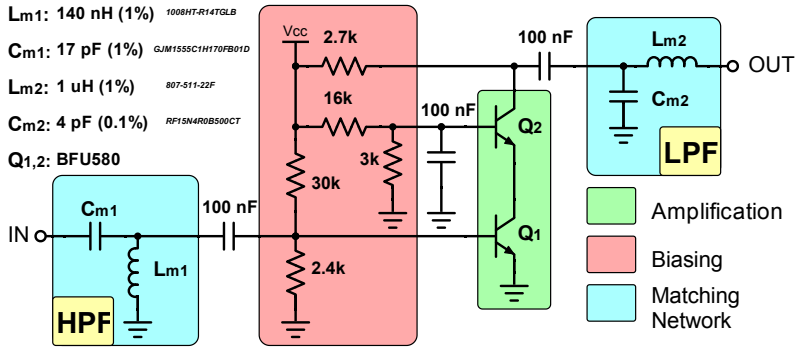

Fig. 7.10: Full circuit of the LNA: includes a cascode stage and matching networks.

7.5 Simulation results

The simulation results of the designed LNA are present in Figs. 7.11 up to 7.18. During simulation, the antenna is modelled as an ideal voltage source with a 50 Ω source resistance. The input impedance of the mixer, being the load of the LNA, is assumed to equal a 55 Ω resistor in series with a 6 pF capacitor. This is an approximation of the simulated load over the RF bandwidth, see Fig. 7.9. The source voltage is set to 50 µV, except for total harmonic distortion and gain compression simulations. Also, input impedance simulations are performed with the output left open. Output impedance simulations have the input grounded and the load replaced with a source.

Summary of the results

An LNA has been designed that satisfies the requirements in Table 6.1. Important conclusions are:

- The gain equals 33 dB, and the maximum noise figure is 1.5 dB, meeting LNA0 and LNA1.
- Matching networks are placed at the input and output, which form an overall bandpass filter.
- The -3 dB bandwidth is 18.9 instead of MHz, and the roll-off is 20 dB/dec, meeting LNA3.
- The gain compresses by 1 dB for an input power -33 dBm. The total harmonic distortion is less than 0.3%, adhering to LNA5.
- The LNA is theoretically stable for all source and load terminations, meeting LNA6.
- The power consumption is 53 mW, satisfying the limit of 100 mW (LNA7).

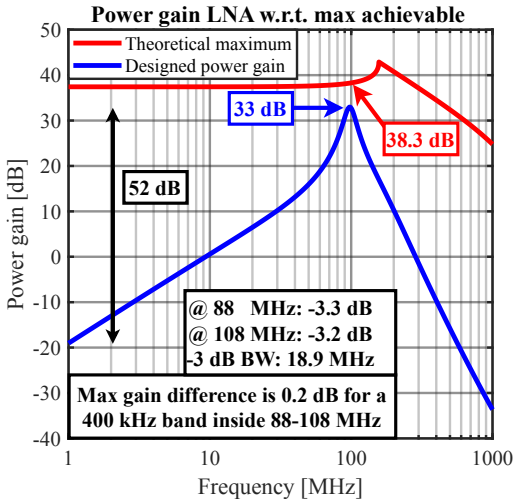

Fig. 7.11: The gain of the LNA over the RF bandwidth meets the minimum of 20 dB (LNA0). The -3 dB bandwidth is 18.9 MHz instead of 20 MHz. Roll-off is asymmetric: 20 dB/dec for decreasing frequencies and 60 dB/dec for increasing frequencies. The latter is caused by, i.a., parasitic capacitances, which create high-frequency poles in the transfer.

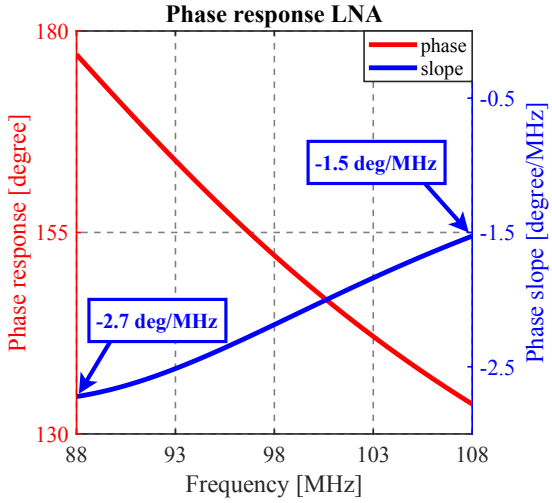

Fig. 7.12: The phase response of the LNA: the slope of the phase response is approximately linear, whereas it should be constant to have an ideal linear phase response. The deviation, over a bandwidth of 400 kHz, from a pure linear phase, is $|-2.7-(-1.5)|$ deg/MHz $\cdot$ 0.4 MHz = 0.5 degree.

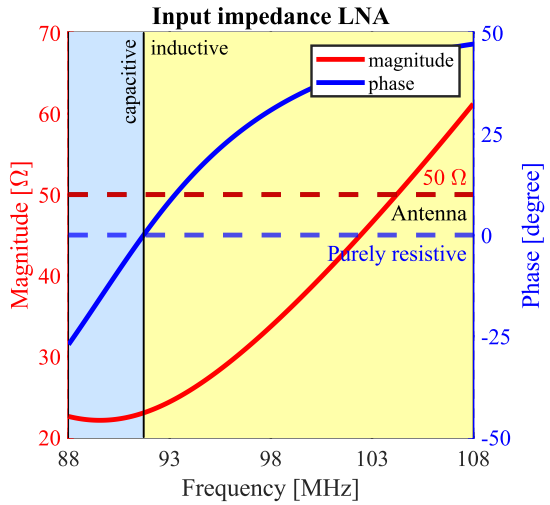

Fig. 7.13: The input impedance of the LNA, compared to the assumed 50 Ω antenna resistance. The LNA is not matched exactly to the 50 Ohm resistance. This results from the trade-off between the noise figure and gain.

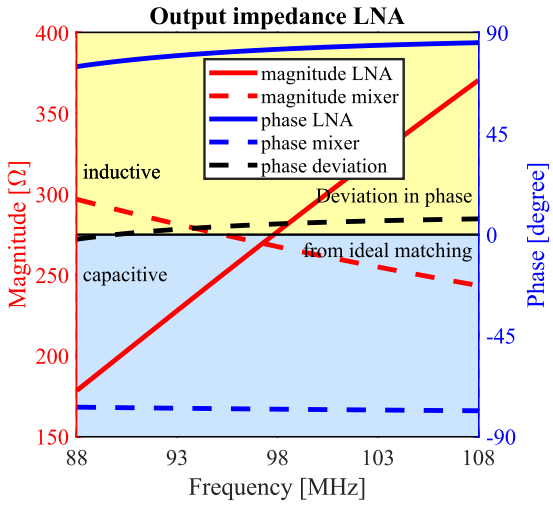

Fig. 7.14: The output impedance, in terms of its phase, is approximately equal to conjugate of mixer's input impedance. However, this does only hold for the magnitude at 97 MHz. A possible improvement, therefore, is to have it decrease in magnitude, instead of increase, for higher frequencies.

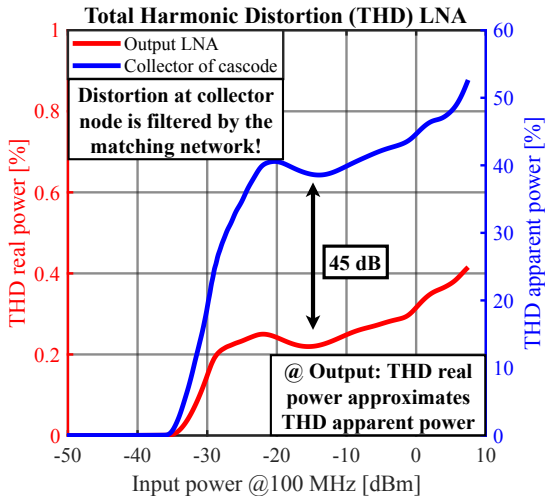

Fig. 7.15: The total harmonic distortion, defined as the ratio of the harmonic power to the fundamental, is limited to 0.4% the output. However, large amounts of harmonic reactive power does flow from the LNA into the matching network. This occurs when the output starts to saturate, see Fig. 7.16.

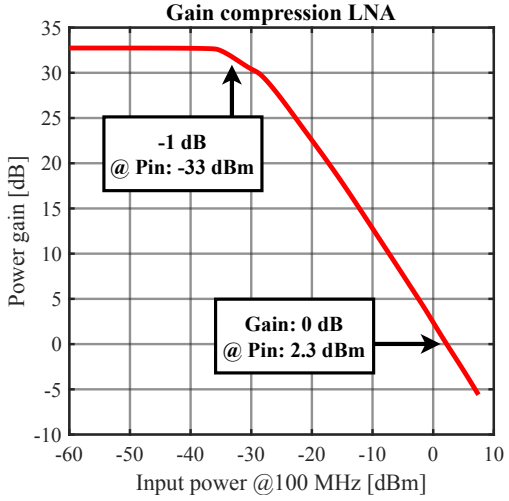

Fig. 7.16: The gain of the LNA drops by 1 dB at an output power of -1 dBm. When the gain starts to compress, the distortion increases, as seen in Fig. 7.15. This occurs when the output saturates, which is mainly determined by the chosen biasing point of the collector.

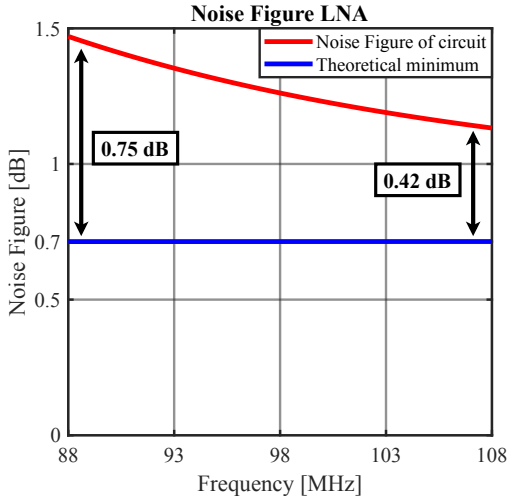

Fig. 7.17: The noise figure of the LNA is between 1.1-1.5 dB, meeting the maximum of 2 dB (LNA1). Note: the increase of around 0.5 dB from the theoretical minimum noise figure, is in line with the performance expected from the noise circles in Fig. 7.5.

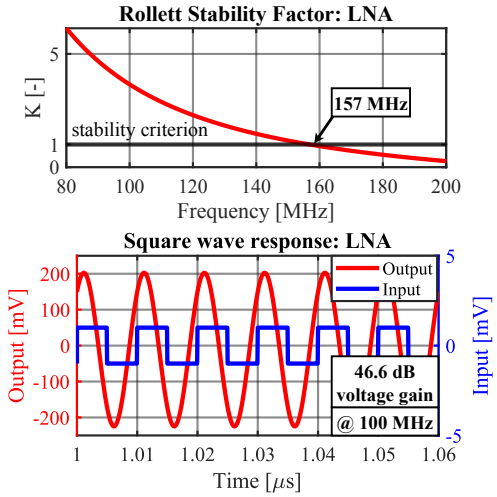

Fig. 7.18: Verifying the stability of the LNA in the time and frequency domain: The amplifier is unconditionally stable for the relevant RF band of 88-108 MHz. The square wave response demonstrates that the higher order harmonics are suppressed by the amplifier, which is expected from Fig. 7.11.

8. Power Amplifier

The modulator at the transmitter produces an FM signal, where the carrier resides in the band of 88 MHz up till 108 MHz, with a bandwidth of 400 kHz. Before this signal can be connected to an antenna, it needs to be amplified to increase the transmitted power. This is done by the RF power amplifier.

8.1 Design requirements

The power amplifier needs to amplify the FM signal, preferably without adding harmonics, since the harmonic power will not be received and is essentially wasted. Furthermore, the frequency of these harmonics depend on the carrier wave frequency, which can vary from 88 MHz up to 110 MHz (SYS5). A complete list of the requirements can be found in the following table:

Table 8.1: Requirements and specifications for RF the power amplifier.

Category		**Tag**	**Category**		**Tag**
Output power	> 525 mW	PA0	Efficiency	$> 70\%$	PA1
Antenna impedance	50 Ω (resistive)	PA2	Operational frequency	88 - 108 MHz	PA3
Input voltage	6 V_{pp}	PA4	Max input current	0.2 mA	PA5

8.2 Different amplifier classes

In the previous chapters, all the amplifiers designed are of class A. Although this class of amplifier is useful in those applications, it is not suitable for an RF power amplifier application, because of its low efficiency. Before the different amplifier classes are compared, it is useful to start with a discussion on some of the metrics, that classify the type.

- **Conduction angle**: this refers to the normalized amount of time that the active device is conducting in a complete cycle. Each cycle of the waveform equals 360°, hence, a conduction angle of 180° means that the transistor conducts for 50% of the time.
- **Linearity**: a linear amplifier does not distort the waveform, in contrast to a non-linear amplifier. For FM applications, however, the information is in the frequency of the carrier. Hence, distortion in the amplitude does not deteriorate the signal-to-ratio at the receiver, like it would for an AM transceiver.

With these metrics in mind, the different amplifier classes will be discussed.

Class A

Class A amplifiers have a conduction angle of 360°. This holds for the amplifiers designed in Chapters 5, 6 and 7. Because of its high conduction angle, this class of amplifier has the lowest efficiency amongst all classes. The maximum theoretical efficiency of a class A amplifier is 50% [25, p. 761]. This already does not comply with requirement PA1, hence, this amplifier class will not be considered.

Class B

Class B amplifiers have a conduction angle of exactly 180°. The efficiency of the amplifier increases, since the transistor is conducting less. Although the maximum theoretical efficiency of this amplifier is 78.5%, see [25, p. 767], practical results show that it lies far below this optimum. For example, the amplifier in [26] reached an efficiency of 54%. Hence, class B amplifiers will not be considered either. A disadvantage of this class, compared to class A, is that the linearity of the output deteriorates,

because of the cross-over distortion. However, since the information is in the frequency of the carrier, not its amplitude, this is less of an issue for the FM transceiver.

Class AB

Class AB amplifiers have a conduction angle between 180° and 360°. Hence, they are viewed as a mix of class A and B amplifiers. By shifting the bias point of the amplifier, the linearity is improved compared to class B. However, this is at the cost of efficiency [27, p. 502]. Since non-linearity is not a serious concern for FM, class AB provide no advantage over class B for the FM transceiver.

Class C

To improve the efficiency, class C amplifiers reduce the conduction angle below 180°. In theory, for a conduction angle just above 0°, the amplifier can approach an efficiency of 100%. In practice, however, the common efficiency of a class C amplifier is between 60% to 70% [28]. Therefore, this class of amplifier will also be disregarded.

The amplifiers discussed until now, use the transistor as a linear current source. The following classes use the transistor as a switching device. While this introduces harmonics, this is less of an issue FM, as mentioned earlier.

Class D

Class D amplifiers are most commonly used in digital systems. They require a PWM (Pulse Width Modulated) signal, which can easily be generated by using a digital system. Although the input of this amplifier is digital, the output is an analog waveform. This digital PWM signal could also be generated from the analog input waveform, but this is not a straightforward way to implement an analog amplifier, and would make the amplifier unnecessarily complex.

Class E

A class E amplifier is another type of switching amplifier, originally discovered in 1975 [29], and still being used often for modern amplifier design. The transistor, usually a MOSFET, is used as a voltage controlled switch. This amplifier can reach a theoretical efficiency of 100%. The class E amplifier tries to minimize the overlap of the voltage and current waveforms across the switch. This minimizes the power dissipated by the switch. All other components are reactive, so they do not dissipate power either.

By using a switch, the output has a lot of harmonic components, which must be suppressed. Also important to realize: class E amplifiers are tuned for a specific frequency band, and will not work properly outside of this range.

Class F

Class F amplifiers use filters to suppress all the odd harmonics at the output. This creates an almost perfect square voltage waveform over the switch. Although these amplifiers can theoretically reach efficiencies of up to 100%, in practice often only the first few harmonics are filtered. This will decrease the efficiency of the amplifier. If, for example, only the first 3 harmonics are filtered, the maximum efficiency drops to 75% [30].

Note: many more amplifier classes, and their variations, exist. It was decided on purpose, however, to limit the scope to the above mentioned classes.

8.3 Proposed amplifier class

Since a high efficiency is required, above 70% (PA1), class A, AB or B are not a good choice. Also, since linearity is not required, switching amplifiers are a valid choice. These classes also bring the advantage of achieving higher efficiencies. When comparing class E to F, it becomes clear that class F amplifiers are a lot more complex than class E, and only reach the same efficiency as class E if many filters are used [30]. Another important note to make is that it is more difficult for class F amplifiers to compensate for device parasitics, whereas class E can adjust the shunt capacitor to compensate for the switch capacitance. Therefore, it was decided to implement a class E amplifier.

8.4 Design approach

The main purpose of the class E amplifier is to minimize the overlapping of the voltage and current waveforms across the switch. To achieve this, class E designers often follow these three guidelines:

1. Voltage across the switch, i.e., transistor, should be zero at the moment the switch closes, and at the moment the switch opens.
2. Current through the switch should be zero at the moment the switch closes.
3. The voltage across the switch should have stopped changing ($dV/dT \approx 0$) before the switch closes.

Consider the classic topology for a class E amplifier:

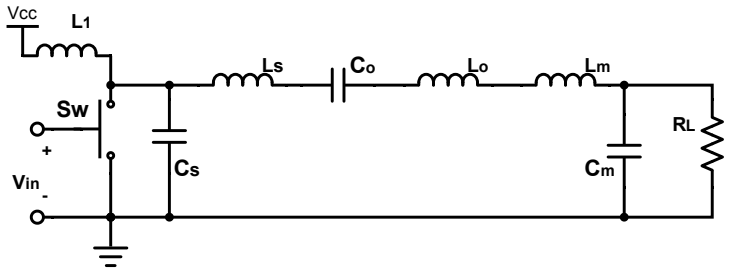

Fig. 8.1: Classical topology of the class E amplifier: L_s, L_o and L_m are drawn separately, but they will be combined into a single inductor for the final implementation. The switch will be replaced with a transistor further on in the design.

8.4.1 Working principle

When the switch is closed, current flows through the switch and charges inductor L_1. When the switch is closed, the inductor L_1 discharges over the shunt capacitor C_s. The repeated switching produce a periodic voltage waveform across the switch. This waveform is filtered using a series oscillator, formed by L_o and C_o. A matching network is placed at the output, formed by L_m and C_m, to match the output of the amplifier to the load, which will be the antenna.

Inductor L_s creates a phase shift in the current through the switch. This phase shift should be designed such that the current is zero at the time the switch closes. This inductor is used to correctly follow the second guideline, mentioned earlier.

8.4.2 Design equations

Most of the design equations for class E assume a duty cycle of 50% for the input signal, and consider L_1 as an RF Choke. These amplifiers often use the following design equations for the load resistance R, shunt susceptance B and excessive reactance X.

$$R = 0.5768 \cdot V_{dc}^2/P_{out} \qquad B = 0.1836/R \qquad X = 1.152 \cdot R \tag{8.1}$$

Although these design equations are common, some different variants have been researched. For example with a duty cycle other than 50% [31], or without assuming inductor L_1 to be an RF Choke [32]. To avoid magnetic coupling between the different inductors used in the power amplifier, the design equations used are the ones from [32], which use a smaller inductor for L_1.

These design equations define z as the ratio of X_{DC}/R_{DC}, with $X_{DC} = \omega L_1$ and $R_{DC} = R_{load}$. From this ratio, the values of R, B and X can be determined by:

for $1 < z < 5$

$$R = \frac{V_{dc}^2}{P_{out}}(1.969 - 0.7783z + 0.1754z^2 - 0.01397z^3) \tag{8.2}$$

$$B = \frac{1}{R}(1.229 - 0.7171z + 0.1881z^2 - 0.01672z^3) \tag{8.3}$$

$$X = R(-1.202 + 1.591z - 0.4279z^2 + 0.03794z^3) \tag{8.4}$$

for $5 < z < 10$

$$R = \frac{V_{dc}^2}{P_{out}}(0.9034 - 0.04805z + 0.002812z^2 - 5.707 \cdot 10^{-5}z^3) \tag{8.5}$$

$$B = \frac{1}{R}(0.3467 - 0.02429z + 0.001426z^2 - 2.893 \cdot 10^{-5}z^3) \tag{8.6}$$

$$X = R(0.6784 + 0.006641z - 0.003794z^2 + 7.587 \cdot 10^{-5}z^3) \tag{8.7}$$

From the values of R, B and X. The component values are determined by:

$$C_s = B/\omega \quad \text{and} \quad L_s = X/\omega \tag{8.8}$$

L_m and C_m can be solved by making the equivalent input resistance of the matching network equal to R. The tank circuit should be tuned at the desired resonance frequency ω_0, and the ratio between the two can be adjusted for the bandwidth. This filter should be sharp enough to sufficiently suppress all the harmonics introduced by the switching behaviour. With all this in mind, the following steps can be followed when designing a class E amplifier.

1. Specify L_o and C_o, based on the desired bandwidth and resonance frequency.
2. Calculate a range of values for L_1 for which $1 < z < 10$.
3. Determine R, B and X.
4. Calculate L_s, C_s, L_m and C_m.

8.4.3 Proposed design

The circuit is first designed and simulated with a voltage controlled switch. The resulting waveforms can be seen in Fig. 8.2.

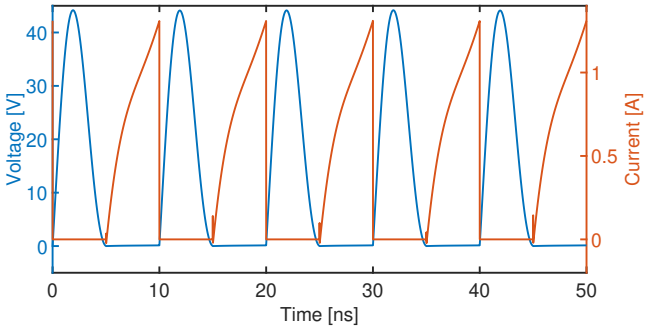

Fig. 8.2: Current and voltage waveforms across the switch. It has an on-resistance of 1 Ω and an off-resistance of 1 MΩ.

The essence of the class E operation is shown on the left: the voltage and current waveforms across the switch do not overlap, minimizing power dissipation. The small positive current spikes near 5, 15, 25 ns etc., are a result of the capacitor C_s still having some charge when the switch starts to conduct. Ideally, this should be prevented by adjusting the value of C_s such that the voltage over the switch is 0 when it switches on. This will be done in a later stage.

8.4.4 Voltage controlled switch

BJTs operate as a current controlled switch, which is not the behaviour desired for the class E amplifier. MOSFETs, on the other hand, operate similar to a voltage controlled switch, being therefore more suitable for this application. MOSFETs are also much more commonly used in high power applications, since they don't dissipate as much power. The MOSFET chosen for this design is the GP1441 from PolyFet [33]. Its switching times are sufficient, furthermore, it has a simulation model for ADS available on their website, which can be scarce for RF applications. This transistor is an N-channel depletion mode MOSFET. This means that it conducts for zero gate-source voltage. It stops conducting for an input voltage below -2.6 V, which is the threshold voltage of the device.

8.4.5 Final schematic

After replacing the voltage controlled switch with the MOSFET, the components must be adjusted to compensate for the device imperfections, such as the drain-source capacitance. This tuning is done with the help of the guidelines mentioned in [34]. The biasing of the transistor is not implemented yet, and the simulation is ran using a DC voltage offset of -2.6 V. The source impedance is set to be 20 Ω. The final schematic can be seen in Fig. 8.3.

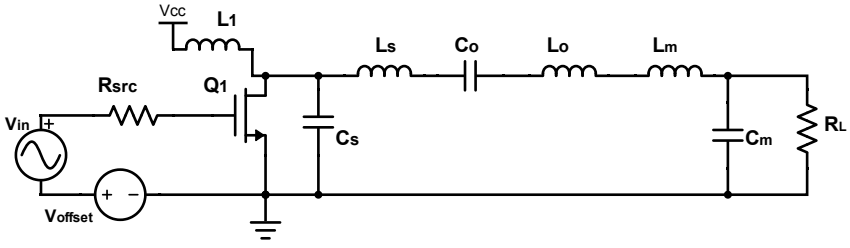

Fig. 8.3: Final schematic of the class E power amplifier.

The component values are listed in Table 8.2.

Component	Value		Component	Value	
L_s	1.3 nH	±1%	C_m	17 pF	±1%
C_s	25 pF	±1%	L_m	33nH	±1%
L_o	160 nH	±1%	L_1	47 nH	±1%
C_o	16 pF	±1%	Q_1	GP1441	

Table 8.2: Component values for the class E amplifier

We were not able to implement the biasing for the power amplifier, but different suggestions for its implementation will be made:

1. Bias the input sinusoid at -2.6 V with an additional power source. The final simulation results are obtained using this solution, but having two different power supplies is undesired in a practical design.
2. Bias the input sinusoid at -2.6 V using a clamper circuit. The problem with this implementation, however, is that the clamper circuit must also drive the gate of the MOSFET, which could be problematic. If you would use a buffer between the clamper and the amplifier, the DC offset will be removed due to the coupling capacitors. Hence, this solution is also not preferred.
3. Convert the sinusoidal waveform into a square wave, with an amplitude greater than 2.6 V. Since the square wave rapidly transitions from maximum to minimum voltage, the MOSFET is turned on and off much faster than with a sine wave. A sinusoid would only turn the transistor off when the peak reaches the threshold voltage, meaning that the duty cycle is not equal to 50% anymore. Note that this implementation allows the use of buffers, since no DC component is required to be preserved. However, this buffer, i.e. the driver circuit, must be suitable for operation at around 100 MHz. The emitter follower, used in the previous designs, has been proven to be unsuitable.

8.5 Simulation results

The resulting current and voltage waveforms over the switch can be seen in Fig. 8.4. The amplifier is biased with an additional DC voltage source.

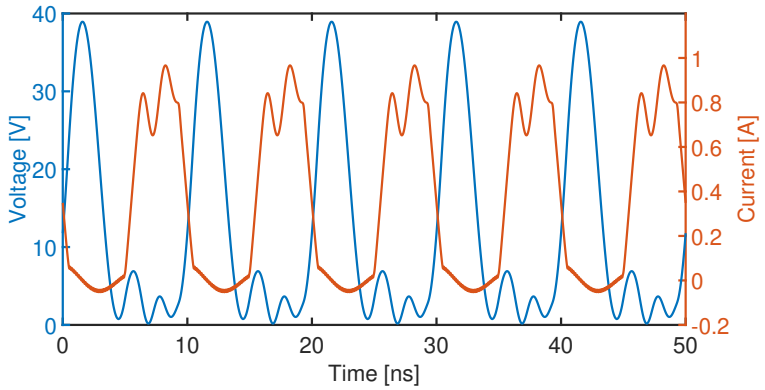

Fig. 8.4: Current and voltage waveforms over the MOSFET. The source impedance is set to 20 Ω; The input is sine wave of 6 V_{pp}, with a DC offset of -2.6 V and a frequency of 100 MHz.

Apart from the voltage and current waveforms, the harmonic distortions of the amplifier are also measured. The results for 88, 100 and 110 MHz can be found in Fig. 8.7 . Also, when amplifying the signal, the amplification is ideally constant, and the phase response linear. This is to minimize introducing errors in the detection stage at the receiver. The results are shown in Figs. 8.5 and 8.6.

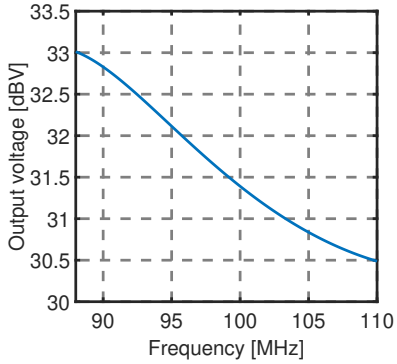

Fig. 8.5: The output voltage over the complete RF band. The input source has a DC offset of -2.6 V.

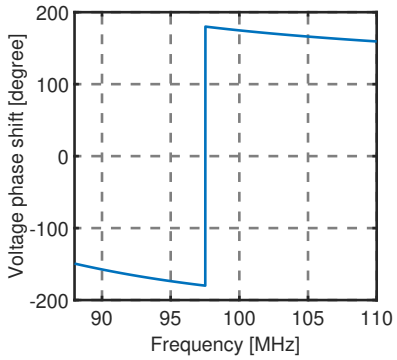

Fig. 8.6: Phase shift caused by the power amplifier.

Table 8.3: Final results of the power amplifier, at 100 MHz.

P_{sig}	2 mW
P_{source}	4.18 W
P_{out}	3.05 W
η	72.9 %
Gain	31.8 dB

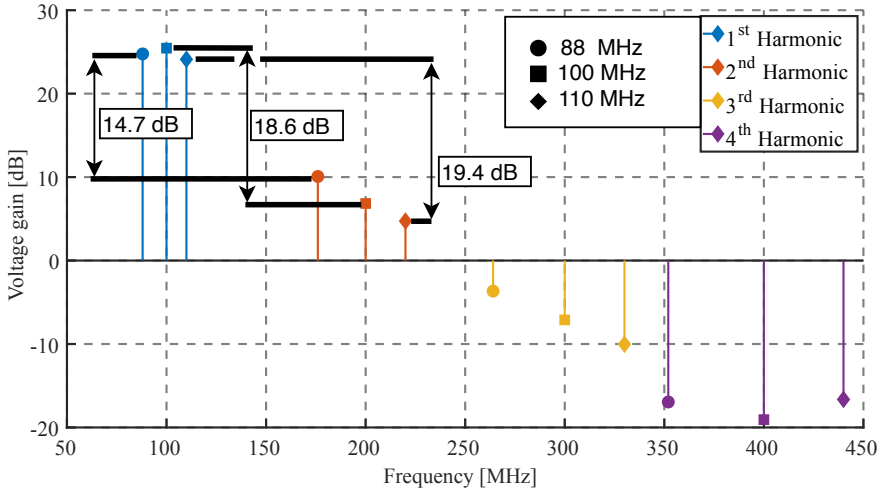

Fig. 8.7: Harmonics created by the power amplifier. Simulated for different input frequencies.

From Fig. 8.5 and 8.6 the largest amplitude modulation and largest phase shift over a bandwidth of 400 kHz are measured. The largest amplitude modulation created a voltage gain difference of 0.06 dBV over the bandwidth of 400 kHz. The largest phase shift over a 400 kHz bandwidth resulted 1.7°. The final results of the power amplifier can be seen in Table 8.3.

With this, it can be concluded that the power amplifier meets the requirements. As mentioned earlier a biasing circuit still needs to be designed. The two suggestions given are both viable options, and further analysis will have to be done to decide between these two. Another important thing to note is the power dissipation over the GP1441, which is 0.83 W. This is lower than the maximum power dissipation for this MOSFET, hence no heatsink is required.

9. Conclusions and Recommendations

9.1 Conclusions

The goal of this project was to design an FM transceiver from discrete components only. In this thesis, more specifically, the design of the different amplifiers, that take part in the transceiver, have been discussed. From the results of each chapter, it can be seen that all the amplifiers meet most of their requirements.

The voltage buffers at the IF amplifiers must be replaced with designs that are suitable for operation at 10 MHz. Also, a driver circuit for the power amplifier must be developed, which either converts a sine wave into a square wave, or is able to bias the circuit with a negative voltage.

In conclusion, most of the designs are ready to be physically realized, and integrated with the other groups that participated in this project.

Summary of the main achievements

- A systematic design approach for amplifier circuits has been presented in Ch. 4.
- Two baseband amplifiers have been designed, in Ch. 5, suitable for applications up to 1 MHz: the first design has an input resistance of 240 kΩ, an output resistance of 15 Ω, with a current drive capability of 2.5 mA. The second design has an input resistance of 11 kΩ, an output resistance of 4 Ω and a drive capability of 15 mA.
- An intermediate frequency amplifier has been designed, in Ch. 6, with a gain of 40.5 dB, which can be lowered by 39.7 dB. It is centered at 9.95 MHz, with a -3 dB bandwidth of 2 MHz, and has a 40 dB/dec roll-off. The total harmonic distortion is less than 1%, with a minimal harmonic suppression of 47 dB. It has an input impedance above 23 kΩ, an output impedance of 30 Ω, and a power consumption of 199 mW.
- A low noise amplifier has been designed, in Ch. 7, with a gain of 33 dB and a maximum noise figure of 1.4 dB over the -3 dB bandwidth of 88 - 108 MHz. The input is matched to the antenna, and the output is matched to the mixer. The total harmonic distortion is less than 0.3%, with an output of -1 dBm at its 1 dB compression point. The amplifier is unconditionally stable, has a linear phase response, and consumes 53 mW.
- A class E power amplifier has been designed, in Ch. 8, with an efficiency of 73%, a transmit power of 35 dBm, and a gain of at least 31 dB over the operating range of 88 - 108 MHz.

9.2 Recommendations

Although the designed amplifiers all work, improving the design is always possible. This section provides multiple recommendations for future designs.

Biasing of the power amplifier

As mentioned in Ch. 8, the power amplifier still requires a biasing circuit to be fully functional. The chapter provided three different suggestions, to implement this biasing circuit:

- Bias the input waveform at -2.6 V using an additional power supply.
- Bias the input waveform at -2.6 V using a clamper circuit.
- Convert the sinusoidal waveform into a square wave, with an amplitude greater than 2.6 V.

All three options provide a viable solution to create the desired 50% duty cycle for the MOSFET. However, the solution most probably requires an additional buffer, that functions as a driving circuit. Since this buffer operates around 100 MHz, previous designs can not be used for this application

Antenna impedance

Both the transmit and receive antenna are modelled as a 50 Ω resistive load. However, this assumption does not hold in practice, since antennas have a frequency dependent impedance. A future recommendation would be to use a more suitable impedance model, that is relevant to our application. When using this model, the matching network at the LNA and PA should be adjusted to match for these impedances.

Linear gain control

The gain control of the IF amplifier is extremely non-linear, as can be seen in Fig. 6.4. To compensate for this non-linearity, a suggestion is to use a logarithmic potentiometer or other non-linear potentiometers, instead of a linear one. This behaviour can then be used to achieve a linear gain control for the IF amplifier.

Electrical gain control

Although gain control via a potentiometer would work, this is a mechanical device and requires manual adjustments. The gain could also be adjusted electrically, this would allow for an automatic gain control.

To control the gain electrically, the biasing of the transistor should be adjusted, with a feedback loop. This can be done by using a current source to bias the transistor. This current source can be controlled using a reference voltage, which changes according to the amplitude of the output. This creates a negative feedback loop, that automatically controls the gain.

Differential pair amplifiers

The LNA currently has a single-ended output, which is converted to a differential signal by the mixer. The LNA could, however, also be designed as a differential amplifier. This would require the conversion of the single-ended signal to a differential signal, to take place at the input of the LNA. Differential pair signals offer a better resilience against common-mode noise sources, and should therefore be considered if such noise sources are present.

Protection circuit

When the power received by the antenna is too high, the voltages and currents entering the LNA could exceed the maximum ratings device ratings, damaging the circuitry. To prevent this, a protection circuit could be designed before the input of the LNA. This protection circuit should preferably add as little noise as possible, since the noise added at this stage will have a high impact on the overall noise performance of the receiver.

High frequency buffers

For high frequencies, above 1 MHz, the emitter follower circuit, frequently used as buffer, is not suitable any more. This is illustrated in Ch. 6. The input impedance drastically drops as the frequency increases, as can be seen in Fig. 6.9. To design a buffer at high frequencies, a different topology will have to be used.

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Part III

Appendix

A. Link budget calculations

The total system has both power and noise requirements: SYS7 until SYS11. In order to meet these requirements, some system level calculations on the power budget and the noise figure have to be performed.

A.1 Power budget

The total transmitted power must be greater than 20 dBm (100 mW). To determine the amount of power that reaches the receiver, Friis formula for free-space transmission is used, obtained from [35]:

$$\frac{P_r}{P_t} = D_t D_r \left(\frac{\lambda}{4\pi d}\right)^2 \tag{A.1}$$

For this purpose, the equation is rewritten into its dB counterpart:

$$P_{r,dB} = P_{t,dB} + D_{r,dB} + D_{r,dB} + 20\log_{10}\left(\frac{\lambda}{4\pi d}\right) \tag{A.2}$$

In this bachelor project, isotropic antennas with a 50 Ω impedance are used. For isotropic antennas, the directivity is 0 dB and can therefore be removed from Eq. (A.2). The carrier wave of the transceiver varies is in the range of 88 MHz until 108 MHz. The free space loss increases for higher frequencies. Hence the worst case in terms of power at the receiver occurs for a carrier frequency of 108 MHz.

The minimal transmission distance should be 5 m, which results in dB free-space loss of 27 dB, hence a received power of -7 dBm is acquired for a transmission power of 20 dBm (SYS9). This is enough to be detected at the receive antenna, but when transmitting 20 dBm, requirement SYS10 can not be met due to the power consumption of the signal generation in the transmitter. To calculate the transmit power required to achieve a 50% efficiency, Eq. (A.3) is used.

$$\eta_t = \frac{P_t}{P_t/\eta_{PA} + P_{budget}} \tag{A.3}$$

With η_{PA} the efficiency of the power amplifier, η_t the efficiency of the complete transmitter, and P_{budget} the power used by the other stages in the transmitter. The power amplifier is assumed to have a 70% efficiency, and P_{budget} is assumed to be 300 mW. Solving for a transmission efficiency of 50% results in a required minimum transmission power of 525 mW, 27.2 dBm. Since this requirement is higher than the previous one, this one is considered. Each component in the transmitter will have their own power requirements, based on the total power budget available. The power division for transmitter and receiver can be seen in Table A.1.

Table A.1: Estimated power consumption for each component

Component	**Estimated power**	**Component**	**Estimated power**
LNA	100 mW	Sawtooth generator	150 mW
Mixer	50 mW	Modulator	100 mW
IF amplifier	200 mW	BB1	50 mW
FM Detector	150 mW	Power amplifier	(4.5 W)
BB2	200 mW		
Local Oscillator	100 mW		
Total	**800 mW**	**Total**	**300 mW (4.8 W)**

In this table, the power amplifier is assumed to have a transmit power of 3 W, and an efficiency of 70%.

The total power consumption of the transceiver results in 5.6 W, which satisfies requirement SYS11.

A.2 Noise figure

The total noise figure of the receiver should be less than 5 dB (SYS7). The total noise figure can be calculated with the Friis equation provided in Fig. 7.1, obtained from [20]. This means that, as stated in Chapter 7, the noise figure of the LNA has the most impact on the total noise figure of the receiver. Since the LNA has a minimum gain of 20 dB, the noise figure of the other stages get reduced by 20 dB. The maximum noise figure for the LNA was set to be 2 dB. The noise figure for the rest of the system can be calculated by Eq. (A.4).

$$F_r = F_{LNA} + \frac{F_{rest} - 1}{G_{LNA}} \tag{A.4}$$

This allows for a possible noise figure of 22 dB for the rest of the receiver. Eq. (A.4) can be used again for the next stages, although these requirements become quite loose due to the gain of previous stages.

A.3 Gain budget

In the receiver, all the different components have different gains, which all add up. The division of these gains can be seen in Fig. A.1. It should be noted that the free space loss, and all the signal values in the following stages are calculated for a distance of 1 km. The free space loss may vary on the distance, according to Eq. (A.2). To compensate for this variable loss, the IF amplifier has been designed to have a tunable gain.

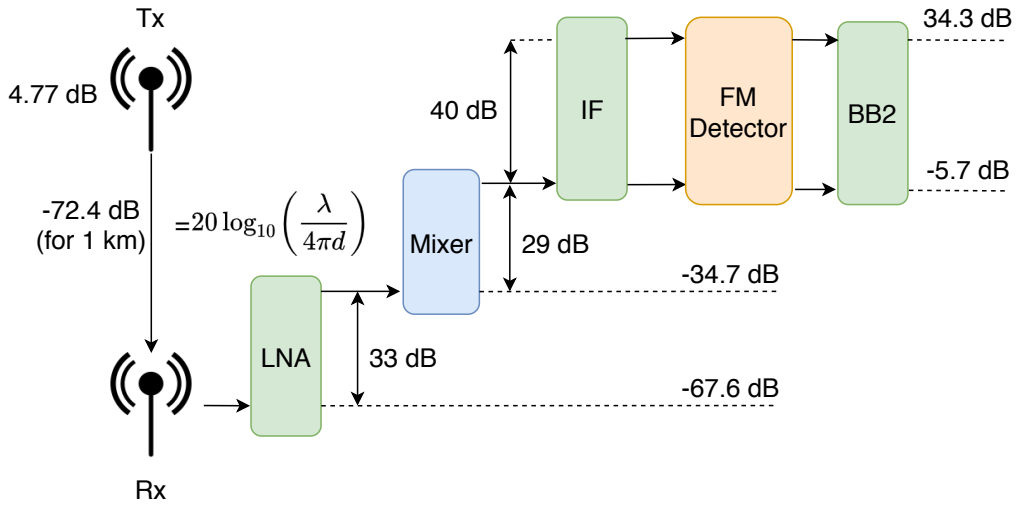


Fig. A.1: Gain budget for all the different components. The gain of the IF is tunable from 0 dB to 40 dB. The free space loss is calculated with a frequency of 100 MHz and a distance of 1 km.

B. Characteristics of the BJT

The BJT (Bipolar Junction Transistor) lies at the heart of the transceiver, hence it is important to have a thorough understanding of this device. While the physics that underly the BJT are of prime importance to understand the device, it lies outside the scope of this thesis. We take the transistor as a given device, and assume the main physical effects to be known. Readers interested in detailed explanations of the related physics are referred to Chapters 7, 8 and 12 of [36].

Furthermore, the discussion is mainly limited to the *npn* transistor. The reader should understand that this is done due to the duality between the *npn* and *pnp* type.

B.1 Device characteristics

The BJT is a three-terminal device manufactured either as an *npn* or *pnp* transistor. This naming states the emitter, base and collector doping type respectively. The two types are shown Fig. B.1. Note that a diode is a pn junction, hence the BJT can be drawn as two diodes!

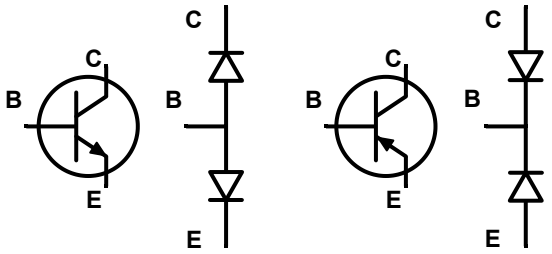


Fig. B.1: Bipolar junction transistors and their diode equivalents; left *npn* transistor, right *pnp* transistor.

The following equations are the basis for amplification: the fundamental relation between the collector current (I_C) and the base emitter voltage (V_{BE}) is

$$I_C = I_S \exp(\frac{V_{BE}}{V_t}) \tag{B.1}$$

The collector current is also related to the base current (I_B) via β

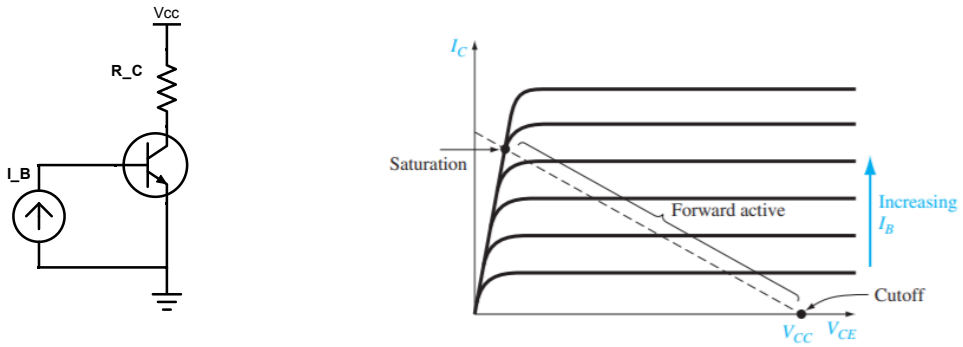
$$I_C = \beta I_B \tag{B.2}$$

In other literature, β might also be denoted as h_{FE}. Furthermore

$$I_E = I_C + I_B = (\beta + 1)I_B, \qquad I_E \approx I_C \quad \text{for } \beta \gg 1 \tag{B.3}$$

where I_s denotes the saturation current and is in the order of pA, but it is highly temperature dependent. The thermal voltage (V_t) $\approx$ 26 mV at room temperature. Eq. (B.2) does only hold in the active region. The operating regions of the device can be seen in Fig. B.2b, the test setup is shown in Fig. B.2a. Following the derivation from [37] we can see that the slope of the load line is equal to -1/R_C in the active region.

Ideally, the transistor acts a a current controlled current source, where the control parameter is the base current and the current source is from the collector to the emitter. An ideal current source delivers the same current independent of the voltage across it. A practical device, such as the BFU160 from NXP, will have a small positive slope as shown in Fig. B.3. This is effect is also known as the **Early effect**. It is typically modelled as a finite output resistance of the current source.



(a) Test setup of the transistor.

(b) The BJT shows the behaviour of a current controlled current source. The dashed line represents the load line. Obtained from [36].

Fig. B.2: Characterising the relation between the collector current and the collector emitter voltage.

From Fig. B.4 we can also see that β is dependent on operating conditions and temperature. It also varies greatly among device batches themselves. The datasheet for this type mentions a typical range of $90 < \beta < 180$ with a typical value of 135, under the specific test conditions. It is important to keep this variability in mind, since this means that transistor circuits should be designed with minimal dependency on the exact value of β.

B.2 Small signal models

Under the appropriate biasing conditions, the transistor can be replaced with a linear circuit model. A commonly used model is the **hybrid-π model**. The model is shown in Figure B.5 along with its simplified version. This model will be used later on in this chapter to evaluate important parameters of a transistor-based amplifier. The following section is devoted to biasing transistors. The subsequent sections analyse the basic common emitter, common collector and common base amplifiers. First the parameters of the simplified model will be explained.

The transconductance, used to linearize the amplification

$$g_m = \frac{dI_C}{dV_{BE}} = \frac{d}{dV_{BE}}\left[I_S \exp(\frac{V_{BE}}{V_t})\right] = \frac{I_C}{V_t}, \quad V_t \approx 26 \text{ mV for } T = 300\text{K} \tag{B.4}$$

The equivalent input resistance, typically in the order of kΩ:

$$r_\pi = \frac{\beta}{g_m} \tag{B.5}$$

The output resistance of the current source, modelling the **Early effect**:

$$r_o = \frac{V_A}{I_C}, \quad \text{with a typical Early voltage between } V_A = 15\text{V - } 150\text{V} \tag{B.6}$$

B.3 The Miller effect

Recall the hybrid-π model shown in Figure B.5. Until now the direct path from base to collector has been ignored. C_μ and r_μ denote the reverse-biased base collector junction capacitance and diffusion

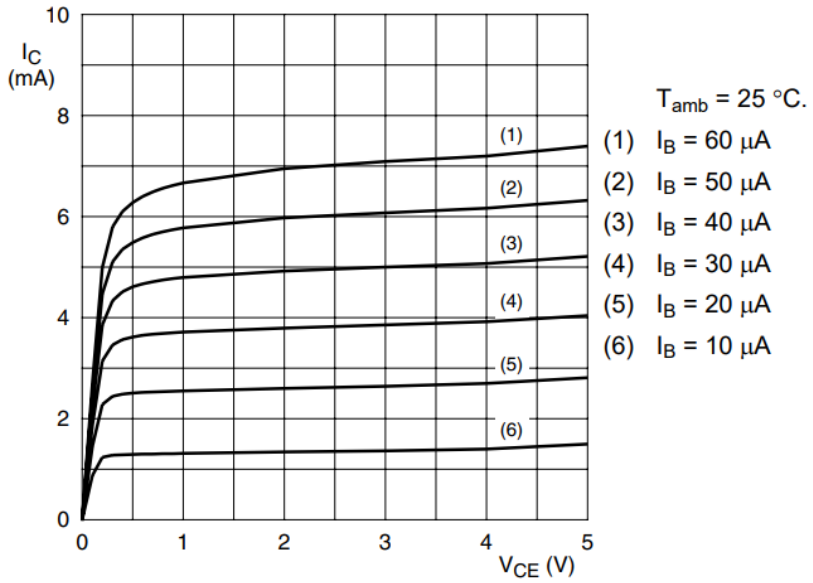


Fig. B.3: The I-V curve of the BFU160 *npn* transistor.[38] The device approximates a current controlled current source, with the base current as the control parameter. In the active region, the transistor is slightly dependent on the voltage across it, which is due to the Early effect.

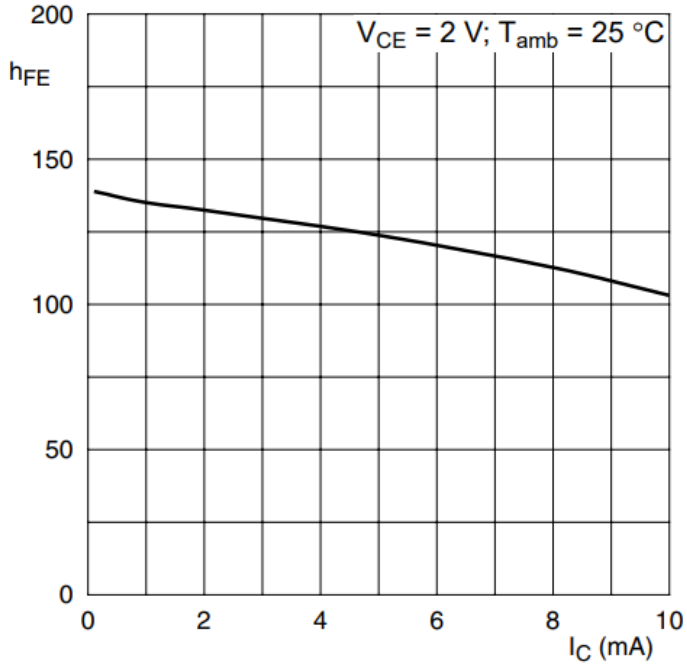


Fig. B.4: The current gain depends on operating conditions and is not well defined in practice! h_{FE} denotes β.[38]

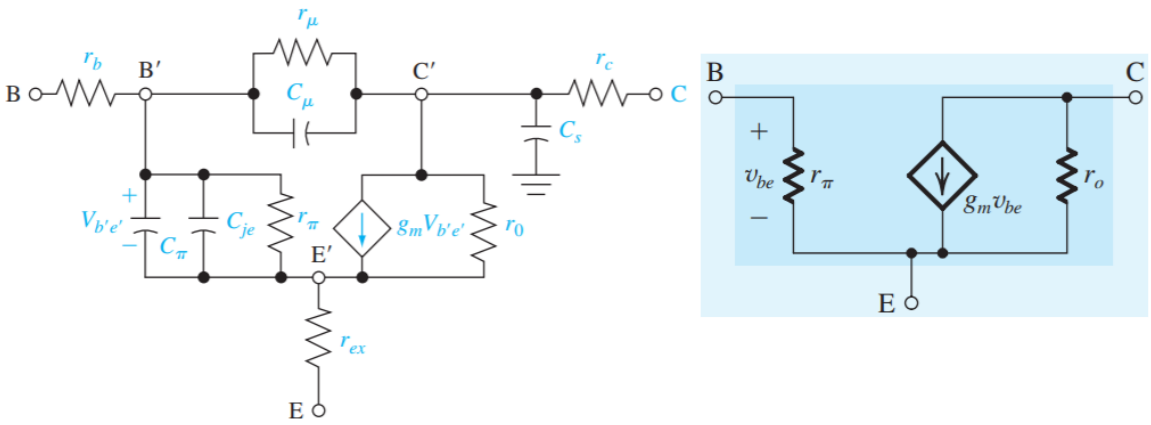


Fig. B.5: The hybrid-π model along with its simplified version. The main parameters are the transconductance g_m and the equivalent input resistance r_π. Parasitic capacitances and contact resistances can be ignored for baseband signals. But they have to be included in the model for the FM signal! The figures are taken from [36] and [39].

resistance respectively. This frequency dependent path is one of the bandwidth limiting factors of the BJT. After a certain upper frequency limit the transistor is not capable of amplification anymore, because the capacitance will be a low resistance path. The base emitter junction will be bypassed, and amplification will thus not take place.

If the base collector junction capacitance C_μ is much smaller than the base emitter diffusion capacitance C_π (which is usually the case), C_μ can be ignored. But due to the feedback loop that exists in for example a simple common emitter amplifier, the effective base collector capacitance is increased. More specifically, C_μ is increased by a factor of the small signal voltage gain (Eq. (D.3)). A small voltage swing at the base, leads to a larger voltage swing at the collector. The voltage swing seen over C_μ is therefore larger than the incoming signal at the base. A larger voltage also means more charge stored for the same capacitance, hence C_μ will draw more current from the base to charge itself, which limits the bandwidth for increasing frequencies. This is also known as the **Miller effect**.

Dealing with the Miller effect is important in designing high frequency amplifiers. An effective measure to reduce this effect is by making use of cascode amplifiers. An example circuit is shown in Figure B.6. In contrast to a standard common emitter amplifier, this amplifier consists of an *npn* in CE configuration, and another *npn* in CB configuration.

To understand how this circuit reduces the Miller effect, the AC analysis on the presented amplifier should be performed. In this case we use a transistor model which is slightly modified, but equivalent to the simplified hybrid-π model. The model is shown in Figure B.7.

By inspecting the circuit, it becomes clear that Q1 is responsible for the current amplification and Q2 for the voltage amplification. The change in the base collector voltage in an *npn* transistor was responsible for the **Miller effect**. For the simplified hybrid-π model, this equals the voltage difference over the current source. For the equivalent cascode amplifier shown in Figure B.8, applying KVL gives

$$V_{B_1C_1} = V_1 + V_2 = V_1(1 + \frac{g_{m1}}{g_{m2}}) = v_{in}(1 + \frac{g_{m1}}{g_{m2}}) \tag{B.7}$$

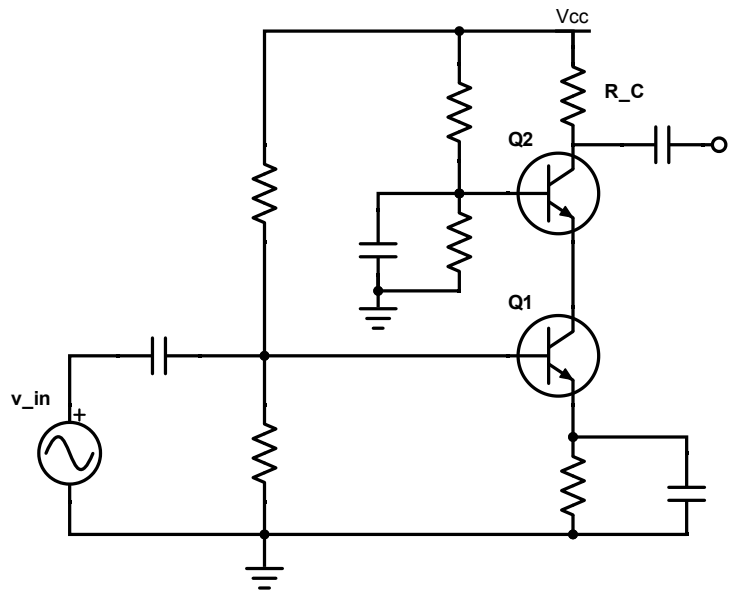


Fig. B.6: The cascode amplifier to reduce the impact of the **Miller effect**: Q1 and Q2 are in CE and CB configuration, respectively. The base of Q2 is assumed to be grounded for the frequency range of interest, due to the bypass capacitors. Both transistors are biased with a resistive divider biasing scheme.

and recall that

$$g_m = \frac{I_C}{V_t}$$

Assuming that both collector currents are the same (which is the case for $\beta_2 \gg 1$) and both transistors are at the same temperature, we get

$$g_{m1} = g_{m2} = g_m$$

thus

$$V_{B_1C_1} = 2v_{in} \tag{B.8}$$

For a standard normal CE amplifier this would equal

$$V_{BC} = (g_m R_C + 1) \tag{B.9}$$

In this configuration, the Miller effect is significantly reduced, as $g_m R_C$ is in general much greater than 1. The small-signal voltage gain will now be derived, to show that the cascode amplifier is equivalent to a standard CE amplifier.

The output voltage can be written as

$$v_{out} = -g_{m2} R_C V_2$$

where

$$V_2 = \frac{g_{m1}}{g_{m2}} V1 = \frac{g_{m1}}{g_{m2}} v_{in}$$

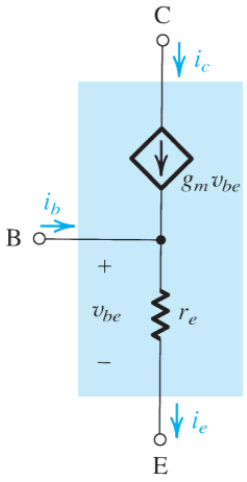


Fig. B.7: The simplified hybrid-π model, equivalent to the simplified model shown in Figure B.5. The output resistance modelling the Early effect is neglected. The small signal emitter resistance r_e is the inverse of the transconductance g_m. Taken from [39].

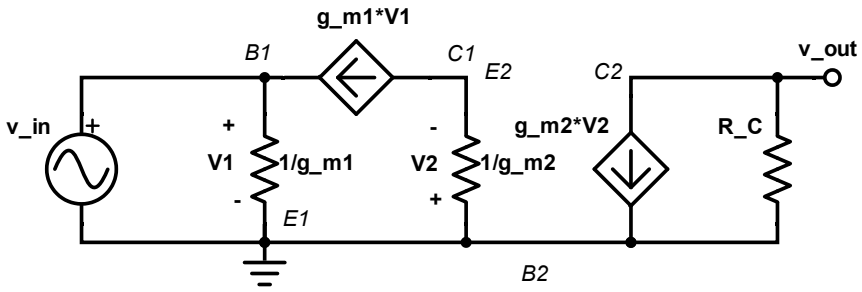


Fig. B.8: Using the simplified hybrid-π model, the cascode amplifier of Figure B.6 can be redrawn as shown. The parallel connection of the biasing resistors of Q1 can be ignored w.r.t. to the much smaller emitter resistance. The biasing resistors of Q2 are grounded due to the bypass capacitor connected to ground.

and therefore

$$v_{out} = -g_{m1} R_C v_{in}$$

and thus

$$A_v = -g_{m1} R_C$$

We can conclude that the presented cascode amplifier is equivalent to a typical common emitter amplifier in terms of small-signal voltage gain. Furthermore, the Miller effect is reduced, because the base collector voltage of Q1 does not get amplified by the small-signal voltage gain anymore, and the base of Q2 does not receive the input signal meaning that the effect does also not occur at Q2.

B.4 Darlington pair

Occasionally, the desired β of the transistor is not high enough. This can for example occur when the load impedance is very small, but the input impedance should be very high. To solve this issue a Darlington pair can be used. An example of a Darlington pair can be seen in Fig. B.9. The Darlington pair can be simplified by a single transistor model with different characteristics. The transconductance of this new transistor is equal to the transconductance of Q2. The β of this new transistor becomes $\beta_1\beta_2 + \beta_1 + \beta_2 \approx \beta_1\beta_2$, where β_1 denotes the β of transistor Q1, and β_2 denotes the β of transistor Q2. This new β is significantly higher, and results in a significantly higher input impedance. An important note is that the base emitter voltage of this transistor will be almost twice as large as that of a single BJT.

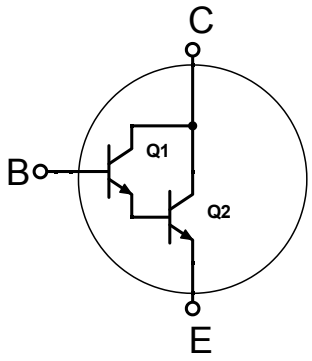


Fig. B.9: Darlington pair modelled as a single BJT

C. Biasing techniques

This chapter discusses different methods to bias the transistor. Before we proceed, it is important to realise the following. At this moment, the purpose is to operate the transistor in the active region, not as a switch. Recall Figure B.2b, if the base current is increased too much the transistor will saturate, since the increasing voltage drop over the connected collector resistor reduces the collector-emitter voltage. We can limit the change in the base current by either constraining the peak amplitude of the input signal, or place a resistor in series with the base. The AC signal should be a *small signal*.

Figure C.1 shows six different biasing schemes. For now we assume no AC signal source, but it can be superimposed at the input of the amplifier with a coupling capacitor. For every biasing scheme we will discuss its pros and cons and also show relevant design equations or rules of thumb. The output voltage is the collector node w.r.t. ground.

The analysis of all biasing schemes will be the same. First the output voltage will be determined using KVL (Kirchhoff Voltage Law). From the resulting expressions we can derive important conclusions.

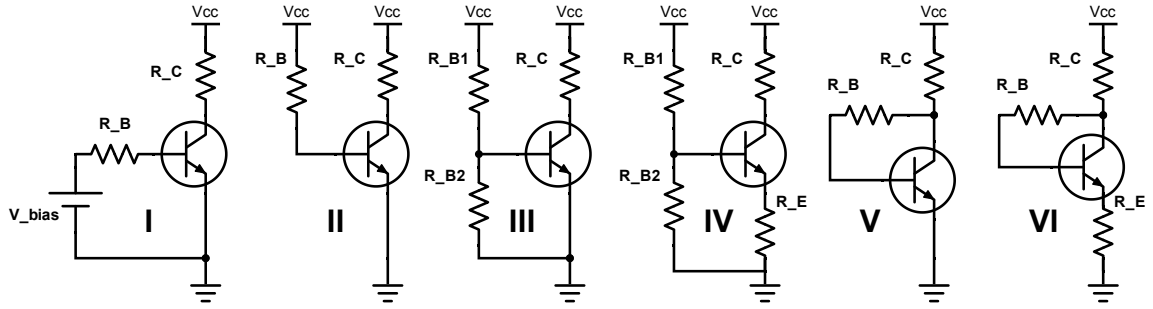


Fig. C.1: Six different biasing schemes to have the transistor operate in the active region under DC conditions. The names of the schemes are: simple bias (I), fixed bias (II), resistive divider bias (III), resistive divider bias with emitter degeneration (IV), self-biased stage (V), self-biased stage with emitter degeneration (VI). The AC signal will be superimposed at the input stage via a coupling capacitor. Due to this capacitor, we can ignore the AC signal source.

I: Simple biasing

The expression for the output voltage (taken from the collector to ground) is

$$V_{out} = V_{CC} - R_C I_C = V_{CC} - \beta I_B R_C, \quad \text{since } I_C = \beta I_B$$

Applying KVL, the base current is written as

$$I_B = \frac{V_{bias} - V_{BE}}{R_B} \tag{C.1}$$

The output voltage can be rewritten into,

$$V_{out} = V_{CC} - \beta \frac{R_C}{R_B}(V_{bias} - V_{BE}) \tag{C.2}$$

From Eq. (C.2) we can conclude that the DC operating point is directly dependent upon β. As we stated earlier, the value of β is not well-defined. This biasing scheme should therefore be avoided as we can not place the operating point according to our specifications! Furthermore, this biasing scheme requires an additional voltage source, which is undesired and unavailable in general.

II: Fixed biasing
This biasing scheme is equivalent to the previous scheme. We can replace V_{bias} with V_{CC} in Eq. (C.2). In this scheme we do not need an additional voltage source, but the operating point is still depending on β which is undesired.

III: Resistive divider biasing
To simplify calculations, we will assume that the base current is much smaller than the current through the resistive divider network. This means that the voltage at the base terminal becomes a simple voltage division. The circuit can then be redrawn with a Thevenin equivalent source V_{th} and resistance R_{th}. We can use Eq. (C.2) to find the corresponding expression.

$$V_{th} = \frac{R_{B2}}{R_{B1} + R_{B2}} V_{CC}, \quad R_{th} = R_{B1} \parallel R_{B2}$$

Using Eq. (C.2):

$$V_{out} \approx V_{CC} - \beta \frac{R_C}{R_{th}} (V_{th} - V_{BE})$$

Rewriting gives:

$$V_{out} = V_{CC} - \beta R_C \left(\frac{V_{CC}}{R_{B1}} - \frac{V_{BE}}{R_{B1} \parallel R_{B2}} \right) \tag{C.3}$$

This approximation is valid when

$$\frac{V_{CC}}{R_{B1} + R_{B2}} \gg I_B = \frac{I_C}{\beta} \tag{C.4}$$

Unfortunately in this configuration the operating point still depends directly on the fluctuating current gain. Also note that $R_{B1} > R_{B1} \parallel R_{B2}$ which means that the contribution of V_{BE} inside the parentheses increases, compared to Eq. (C.2). While V_{BE} is typically between 0.7V - 0.8V, this is still an uncertainty of around 14%.

IV: Resistive divider biasing with emitter degeneration
Again assume that the base current can be neglected w.r.t. to the current through the biasing network, i.e. $I_{R_{B2}} \gg I_B$. For this we require Eq. (C.4) to be valid. Applying KVL with the Thevenin equivalent results in:

$$\begin{aligned} V_{th} &= I_B R_{th} + V_{BE} + I_E R_E \\ &= I_B R_{th} + V_{BE} + I_B(\beta + 1) R_E \end{aligned}$$

Rewriting gives,

$$\begin{aligned} I_B &= \frac{V_{th} - V_{BE}}{R_{th} + (\beta + 1) R_E} \\ &\approx \frac{V_{th} - V_{BE}}{\beta R_E} \end{aligned} \tag{C.5}$$

The above expression only holds when

$$R_{B1} \parallel R_{B2} \ll \beta R_E \quad \text{and} \quad \beta \gg 1 \tag{C.6}$$

In that case

$$I_B \propto \frac{1}{\beta}, \quad I_C = \beta I_B \propto \beta \frac{1}{\beta} \tag{C.7}$$

The collector current becomes independent of β

$$\begin{aligned} I_C &\approx \frac{V_{th} - V_{BE}}{R_E} \\ &\approx (\frac{R_{B2}}{R_{B1} + R_{B2}} V_{CC} - V_{BE})/R_E \end{aligned} \tag{C.8}$$

The output voltage is then

$$\begin{aligned} V_{out} &= V_{CC} - I_C R_C \\ &= V_{CC} \left[1 - (\frac{R_{B2}}{R_{B1} + R_{B2}} - \frac{V_{BE}}{V_{CC}}) \frac{R_C}{R_E} \right] \end{aligned} \tag{C.9}$$

By adding the emitter resistance and complying to Eq. (C.6) we can make the DC operating point less sensitive to β! However, due to the emitter resistance, we have also decreased the sensitivity in small signal variations at the input. This can be treated by adding a bypass capacitor parallel to the emitter resistance, which shorts this resistance under AC conditions.

Comparing Eqs. C.1 and C.5 also results in an important conclusion for intuitive feeling. The emitter resistance seen from the base terminal is much larger than the actual value! It seems a factor β larger. We can make an equivalent network as shown in Figure C.2.

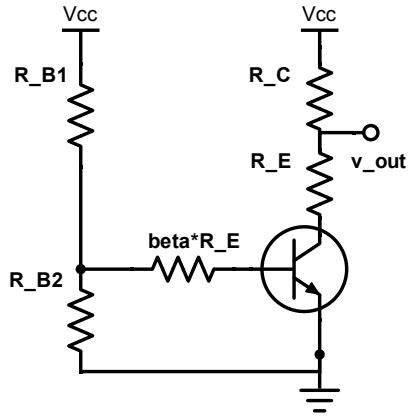


Fig. C.2: Biasing scheme **IV** from Figure C.1 can be redrawn into this equivalent network.

V: Self-biased stage
Applying KVL gives

$$\begin{aligned} V_{CC} &= R_C I_E + R_B I_B + V_{BE} \\ &= [(\beta + 1) R_C + R_B] I_B + V_{BE} \end{aligned}$$

which can be rewritten as

$$I_B = \frac{V_{CC} - V_{BE}}{(\beta + 1) R_C + R_B} \tag{C.10}$$

The output voltage is

$$\begin{aligned} V_{out} &= V_{CC} - R_C I_E \\ &= V_{CC} - (\beta + 1) R_C I_B \end{aligned}$$

which is equivalent to

$$V_{out} = V_{CC} \left[1 - (1 - \frac{V_{BE}}{V_{CC}}) / (\frac{R_B}{(\beta + 1) R_C} + 1) \right] \tag{C.11}$$

From the last expression we can see that the quiescent output voltage is always between V_{CC} and V_{BE}. There is a trade-off however with this scheme, which may be unfortunate. To be independent of the exact value of the current gain, we require $R_B \ll (\beta + 1)R_C$. But in that case the operating point will be equal to the base emitter voltage. However if we want the output voltage at half the supply voltage, the ratio which includes β in the denominator can not be ignored!

VI: Self-biased stage with emitter degeneration
The dependency of the previous biasing scheme on the current gain can be treated with emitter degeneration, similar to how scheme **III** was cured. By adding an emitter resistance it can be shown that the resulting expression is:

$$V_{out} = V_{CC}\left[1 - (1 - \frac{V_{BE}}{V_{CC}})/(\frac{R_B}{(\beta+1)(R_C + \mathbf{R_E})} + \frac{\mathbf{R_E}}{\mathbf{R_C}} + 1)\right] \tag{C.12}$$

The main conclusion that can be drawn from the above discussed biasing schemes is the following: Adding an emitter resistance decreases the sensitivity to fluctuations in β. But emitter resistance should be bypassed for AC signals to increase the gain of the amplifier. These conclusions are extremely important for amplifier design.

D. Amplifier configurations

In this Chapter, the three most common amplifier typologies are discussed. First the large signal analysis is performed, from which the biasing point can be determined. After that the small signal model is used to determine the input and output impedance, as well as the current and voltage gain.

D.1 Common-emitter amplifier

This section will evaluate the performance of a well-known common-emitter (CE) amplifier. The small signal gain and input/output impedances will be determined. This is extremely important for the interface between other subsystems and impedance matching. The amplifier is shown in Fig. D.1. To derive design equations for this amplifier, we apply the **superposition theorem**. The circuit is analysed under DC and AC conditions separately. For this, we assume that all the capacitors are chosen such that they can be replaced with zero-resistance paths for the frequency range of interest. The emitter resistance is bypassed to increase the sensitivity for small signals at the input, as was concluded from the results of the previous section. For the DC analysis, which is important for the biasing, the capacitors are open. Hence the circuit reduces to biasing scheme **IV** from Fig. C.1. To correctly bias the transistor, we can use Eqs. (C.10) and (C) derived earlier.

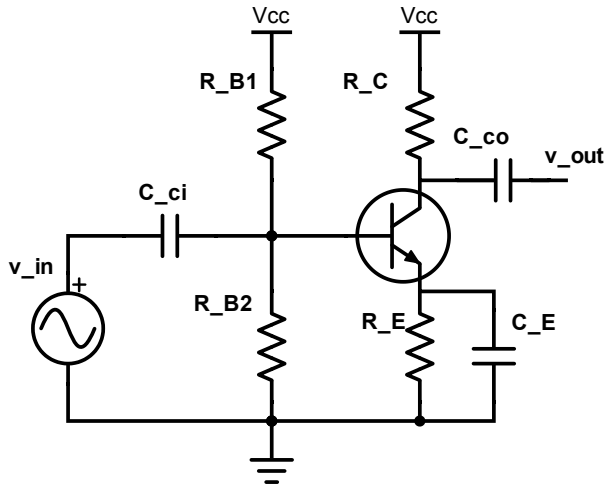


Fig. D.1: Common-emitter amplifier with a resistive divider biasing network, input and output coupling capacitors, and a bypass capacitor for the emitter resistance. Assume that under AC conditions, all capacitors act as a zero-resistance path.

To analyse the amplifier under AC conditions we use the **hybrid-π model** shown in Chapter B. Recall that this is a linear model, for the non-linear behaviour of the transistor. We therefore assume that the linear model holds for the of input signals of interest. Using this model, the CE amplifier circuit can be redrawn into Fig.D.2.

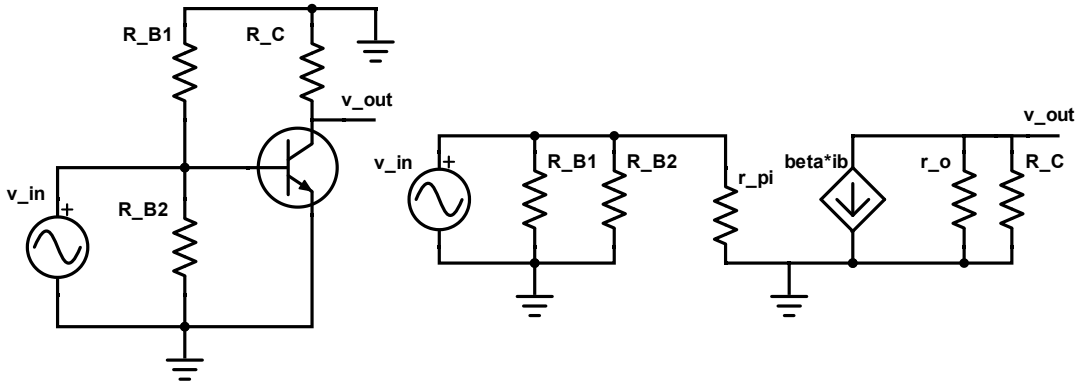


Fig. D.2: Under AC conditions, the CE amplifier can be redrawn as shown. The capacitors are replaced with zero-resistance paths. Constant voltage levels are set to zero (i.e. grounded). The transistor can be replaced with the simplified hybrid-π model.

Under AC conditions, the input resistance of the amplifier equals

$$R_{in} = R_{B1} \parallel R_{B2} \parallel r_\pi \tag{D.1}$$

The output resistance equals

$$R_{out} = R_C \parallel r_o \approx R_C \tag{D.2}$$

This approximation is usually valid as the output resistance r_o, modelling the Early effect, is much larger than the collector resistance in general.

The small signal AC base current is

$$i_b = \frac{v_{in}}{r_\pi}$$

and at the output we have

$$\begin{aligned} v_{out} &= -\beta(r_o \parallel R_C) i_b \\ &= -\frac{\beta}{r_\pi}(r_o \parallel R_C) v_{in} \\ &= -g_m(r_o \parallel R_C) v_{in} \end{aligned}$$

The small signal voltage gain is then

$$\begin{aligned} A_v = \frac{v_{out}}{v_{in}} &= -g_m(r_o \parallel R_C) \\ &\approx -g_m R_C \end{aligned} \tag{D.3}$$

Using the expression for the transconductance in Eq. (B.4) we obtain

$$A_v = -\frac{R_C I_C}{V_t} \tag{D.4}$$

The expression for the thermal voltage is

$$V_t = \frac{kT}{e} \tag{D.5}$$

where k is the Boltzmann constant, T is the temperature and e is the elementary charge. This means that

$$A_v \propto \frac{1}{T} \tag{D.6}$$

We have shown how the CE amplifier can be used to amplify small AC signals. Expressions for the input and output impedances have been derived. The small signal voltage gain was also derived, and it was shown that it is dependent on temperature. The following section will discuss the common-collector (CC) amplifier, and how it can be used to match impedances between subsystems, acting as a voltage buffer.

D.2 Common-collector amplifier

The common-collector (CC) amplifier, also known as the emitter follower, is an amplifier configuration which can be used as a voltage buffer. We will analyse the circuit shown in Fig.D.3 in the same way as the CE amplifier. Similar to the CE amplifier, the superposition theorem can again be applied to separate the AC and DC analysis. The amplifier itself is shown in Fig.D.3.

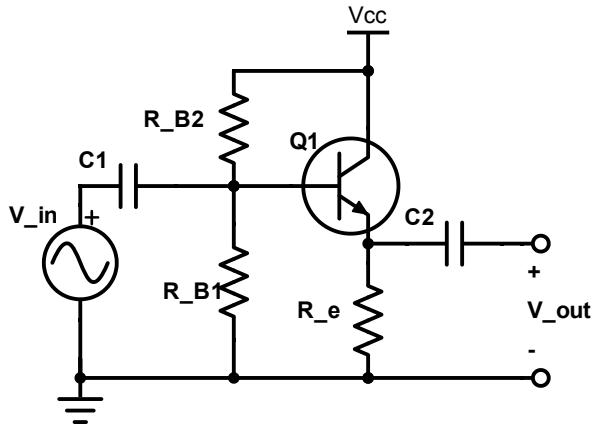


Fig. D.3: Common-collector amplifier with a resistive divider biasing network as well as input and output coupling capacitors

Again similar to the previous analysis, we first analyse the small signal input resistance. Under the AC conditions, the V_{cc} source becomes ground and the capacitors become shorts. This results in the equivalent circuit shown in Fig.D.4.

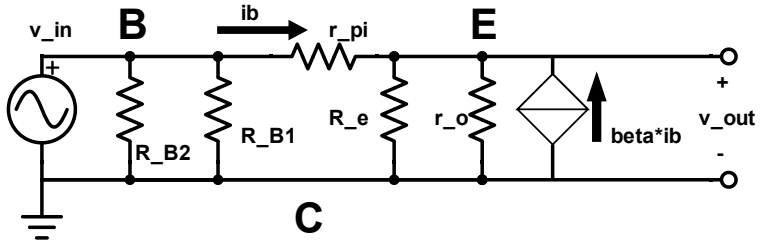


Fig. D.4: Common-collector equivalent circuit under AC conditions, the transistor is replaced by the simplified hybrid-π model

From this equivalent circuit, the input resistance can be calculated as follows:

$$R_{in} = R_{B1} \parallel R_{B2} \parallel R_{base} \tag{D.7}$$

with

$$R_{base} = \frac{v_b}{i_b}, \quad i_b = \frac{v_b - v_e}{r_\pi}, \quad \text{and} \quad \frac{v_e}{R_e \parallel r_o} = (\beta + 1) i_b \tag{D.8}$$

finally this gives the input resistance

$$\begin{aligned} R_{in} &= R_{B1} \parallel R_{B2} \parallel [r_\pi + (\beta + 1)(R_e \parallel r_o)] \\ &\approx R_{B1} \parallel R_{B2} \parallel \beta R_e \end{aligned} \tag{D.9}$$

The approximation holds under the conditions $r_o \gg R_e$, $\beta \gg 1$, and $r_\pi \ll \beta R_e$.

The output resistance can be calculated by shorting the input, and placing a test voltage source at the output. This results in

$$\begin{aligned} R_{out} &= (R_e \parallel r_\pi \parallel r_o) \parallel g_m^{-1} \\ &\approx g_m^{-1} \end{aligned} \tag{D.10}$$

This approximation holds under the same conditions as for the input resistance. The small signal voltage gain can be calculated using the following equations:

$$A_v = \frac{v_{out}}{v_{in}}, \quad (\beta + 1) i_b = \frac{v_{out}}{R_e \parallel r_o}, \quad \text{and} \quad i_b = \frac{v_{in} - v_{out}}{r_\pi} \tag{D.11}$$

simplifying these equations we are left with a small signal voltage gain of

$$\begin{aligned} A_v &= \left(\frac{\beta + 1}{r_\pi} \right) \left[(R_e \parallel r_\pi \parallel r_o) \parallel g_m^{-1} \right] \\ &\approx g_m (R_e \parallel g_m^{-1}) = \frac{R_e}{R_e + g_m^{-1}} \\ &\approx \frac{R_e}{R_e} = 1, \quad \text{when } R_e \gg g_m^{-1} \end{aligned} \tag{D.12}$$

From Eq. (D.12), it can be seen that the small signal voltage gain for a CC amplifier is always less than but close to unity. Another important parameter to observe is the output resistance. It is found to be g_m^{-1} which is very low, since g_m^{-1} is generally a few Ω. Comparing this with the output resistance of the CE amplifier in Eq. (D.2), we can notice a reduction in the order of 1000!

A very low output resistance combined with a unity voltage gain make the CC amplifier approximate an ideal voltage buffer. In practice it is therefore used to preserve the voltage while increasing the voltage drive capability.

D.3 Common-base amplifier

The common-base (CB) amplifier is also called the grounded-base amplifier since the base terminal is connected to ground for the small-signal model. Although this amplifier is least used in practice, it still has some useful characteristics. The most notable characteristics are its input and output resistance which make it useful as a current buffer. It also does not suffer from the so-called Miller effect. This effect is treated in Section B.3. An example of a CB amplifier can be seen in Fig.D.5.

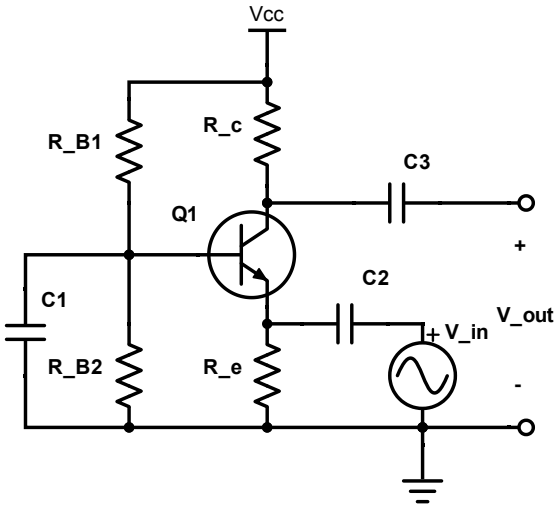


Fig. D.5: Common-base amplifier with a resistive divider biasing network as well as input and output coupling capacitors. The capacitor at the base 'grounds' the base for AC signals.

To analyse the input and output resistance of the amplifier, the small-signal equivalent circuit should be analysed. As done multiple times before, all the DC sources are set to zero and all the capacitors are replaced with short-circuits. The simplified hybrid-π model is applied to analyse the input and output resistance. The resulting circuit is shown in Fig.D.6.

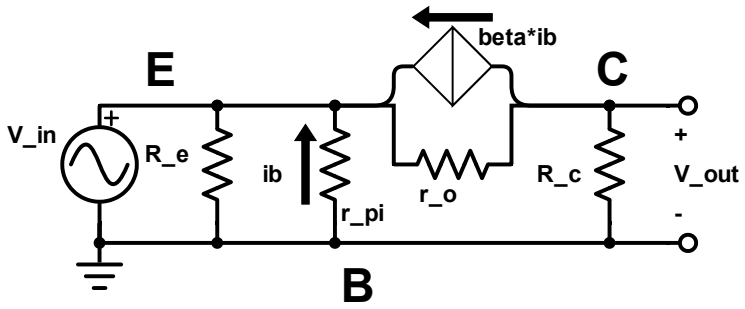


Fig. D.6: Common-base equivalent circuit under AC conditions, the transistor is replaced by the simplified hybrid-π model

From this equivalent circuit, the input resistance can be calculated by:

$$R_{in} = R_e \parallel R_{emitter} \quad \text{with} \quad R_{emitter} = \frac{v_e}{i_e} \tag{D.13}$$

Applying KCL (Kirchhoff Current Law) on the emitter node yields

$$i_e = -(\beta + 1)i_b \quad \text{where} \quad i_b = -\frac{v_e}{r_\pi} \tag{D.14}$$

Solving Eqs. (D.13) and (D.14) gives and ignoring r_o to simplify calculations gives

$$\begin{aligned} R_{in} &\approx R_e \parallel \frac{\beta + 1}{r_\pi} \\ &\approx \frac{\beta}{r_\pi} = \frac{1}{g_m} \end{aligned} \tag{D.15}$$

The approximation holds under the condition that $\beta \gg 1$ and $R_e \gg g_m^{-1}$. In a similar way, the output resistance can be calculated by shorting V_{in}, and placing a test source at the output. The output resistance is found to be

$$R_{out} = R_c \parallel r_o \tag{D.16}$$

Apart from the small signal voltage gain, it is also interesting to calculate the small signal current gain for this amplifier.

$$A_v = \frac{v_{out}}{v_{in}} \quad \text{and} \quad A_i = \frac{i_{out}}{i_{in}} \tag{D.17}$$

For the voltage gain, we can use KCL (Kirchhoff Current Law) at the collector to obtain:

$$\beta i_b + \frac{v_{out} - v_{in}}{r_o} + \frac{v_{out}}{R_c} = 0 \quad \text{where} \quad i_b = -\frac{v_{in}}{r_\pi} \tag{D.18}$$

Rewriting this gives

$$\begin{aligned} A_v &= (g_m + \frac{1}{r_o})(R_c \parallel r_o) \\ &\approx g_m R_c \end{aligned} \tag{D.19}$$

The approximation holds if $R_c \ll r_o$ and $g_m r_o \gg 1$. Note that $g_m r_o$ is sometimes also referred to as the *internal gain* of the transistor. It could be that this approximation is not always valid. Using the transconductance of the circuit and the input resistance, the current gain is found to be

$$\begin{aligned} A_i &= (g_m + \frac{1}{r_o})R_{in} \approx g_m R_{in} \\ &\approx \frac{g_m}{g_m} = 1 \end{aligned} \tag{D.20}$$

The approximation holds if $g_m r_o \gg 1$ and $\beta \gg 1$. From this we can conclude that a CB amplifier does not amplify the current, it only amplifies voltage. This configuration is also seen as a heavy load by the preceding stage, as it tries to draw maximum current. Another important thing to note is that the output resistance is rather large, which helps to isolate the output from the input. Hence this amplifier is also used in combination with other amplifiers where such input-output isolation is needed.

D.4 Amplifier type comparison

Finally, it is useful to observe the different parameters of the three different configurations. The expressions found previously with approximations, have been restated in Table D.1.

Table D.1: Comparison between CE, CC and CB amplifiers

Amplifier type	A_v	A_i	R_{in}	R_{out}
Common-emitter	$-g_m R_C$	β	$R_{B1} \parallel R_{B2} \parallel r_\pi$	$R_c \parallel r_o$
Common-collector	1	β	$R_{B1} \parallel R_{B2} \parallel \beta R_e$	g_m^{-1}
Common-base	$g_m R_c$	1	g_m^{-1}	$R_c \parallel r_o$

In conclusion, the CE amplifier can amplify both current and voltage where CC and CB amplifiers can amplify either current or voltage. The input and output resistances of the CE amplifier could cause some issues however. When a low input resistance is required, a CB stage might be necessary. A CC amplifier on the other hand, has a very low output resistance. Thus, combining the different topologies can lead to better matching between preceding and succeeding stages of the system.

E. Filter design of the IF amplifier

The design equations for the filters used in the IF amplifier are derived in this Chapter.

E.1 Output filter

Consider the following RLC tank circuit:

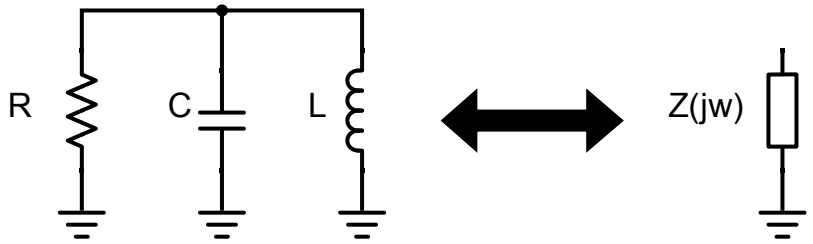


Fig. E.1: Second order RLC tank.

The equivalent impedance will be derived:

$$\begin{aligned} Z(j\omega) &= R \parallel \left(\frac{1}{j\omega C}\right) \parallel (j\omega L) \\ &= \frac{1}{\frac{1}{R} + j\omega C + \frac{1}{j\omega L}} \\ &= \frac{R}{1 + j\omega RC(1 - \frac{1}{\omega^2 LC})} \end{aligned} \tag{E.1}$$

Define the resonance frequency

$$\omega_o = 2\pi f_o = \frac{1}{\sqrt{LC}} \tag{E.2}$$

The equivalent impedance is then

$$Z(j\omega) = \frac{R}{1 + j\omega RC(1 - \frac{\omega_o^2}{\omega^2})} \tag{E.3}$$

This magnitude response is then

$$|Z(j\omega)| = R \Bigg/ \sqrt{1 + (\omega RC)^2 \left[1 - \left(\frac{\omega_o}{\omega}\right)^2\right]^2} \tag{E.4}$$

with

$$|Z(j\omega_o)| = R \tag{E.5}$$

E.2 IF input filter

Consider the following filter circuit:

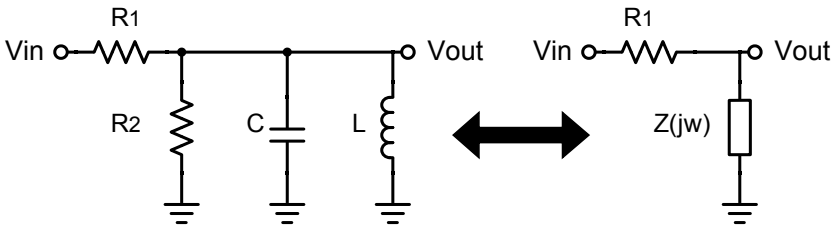


Fig. E.2: The input filter of the IF amplifier.

The transfer function can be written as

$$\begin{aligned} H(j\omega) = \frac{V_{out}}{V_{in}} &= \frac{Z(j\omega)}{R_1 + Z(j\omega)} \\ &= \frac{1}{R_1 Y(j\omega) + 1}, \qquad \text{where } Y(j\omega) = \frac{1}{Z(j\omega)} \\ &= \frac{R_2}{R_1\left[1 + j\omega R_2 C\left(1 - \frac{\omega_o^2}{\omega^2}\right)\right] + R_2} \\ &= \left(\frac{R_2}{R_1 + R_2}\right) \Bigg/ \left(1 + j\omega(R_1 \parallel R_2)C\left[1 - \left(\frac{\omega_o}{\omega}\right)^2\right]\right) \end{aligned} \tag{E.6}$$

The magnitude response is then

$$|H(j\omega)| = \frac{|V_{out}|}{|V_{in}|} = \left(\frac{R_2}{R_1 + R_2}\right) \Bigg/ \sqrt{1 + [\omega(R_1 \parallel R_2)C]^2\left[1 - \left(\frac{\omega_o}{\omega}\right)^2\right]^2} \tag{E.7}$$

with

$$|H(j\omega_o)| = \frac{R_2}{R_1 + R_2} \tag{E.8}$$

F. MATLAB scripts

F.1 Common-collector amplifier

The script below is used to determine the component values of a common collector amplifier. The script indicates if a Darlington pair is required based on the specifications

```
% Author: Lars Bouman
% Date: 18-6-2020
% Description: Generates the componenet values for a common collector
% amplifier. The amplifier is biased with a voltage divider, and uses a
% darlington pair if required

%% Clear the workspace
clear;
close all;

%% Setup design parameters
Ic = 1e-3;
Vcc = 12;
Rin = 70e3;
Rl = 1500;
Vbe = 0.8;
beta = 90;

%% Set the q point to half the supply voltage and calculate the required Re
Vq = Vcc/2;
Re = Vq/Ic;

%% Calculate the base biasing resistors
Vb = Vq + Vbe;

Rb2 = beta* (Re*Rl/(Re+Rl))/10;
syms Rb1;
S = solve(Vb == Vcc*Rb2/(Rb1 + Rb2), Rb1);
Rb1 = double(S);

%% Check the input resistance
syms R_in
S = solve(1/R_in == 1/Rb1 + 1/Rb2 + 1/(beta*Re) + 1/(beta*Rl));
R_in = double(S);

%% Decide whether a darlington pair is needed
if R_in < Rin
    disp('Darlington pair required!');
    Vb = Vq + Vbe + Vbe;

    Rb2 = beta*beta*(Re*Rl/(Re+Rl))/10;
    syms Rb1;
    S = solve(Vb == Vcc*Rb2/(Rb1 + Rb2), Rb1);
    Rb1 = double(S);
end

%% Check the input resistance again
```

```
48 syms R_in
49 S = solve(1/R_in == 1/Rb1 + 1/Rb2 + 1/(beta*Re) + 1/(beta*Rl));
50 R_in = double(S);
51
52 if R_in < Rin
53     error('Failed to create desired input impedance');
54 end
55
56 %% Display results
57 disp(['Re: ', num2str(Re)]);
58 disp(['Rb1: ', num2str(Rb1)]);
59 disp(['Rb2: ', num2str(Rb2)]);
```

F.2 Output filter IF amplifier

The following MATLAB script calculates the required components values for the RLC tank, which is at the output of the IF amplifier. The gain, assuming no emitter degeneration, equals the transconductance multiplied by the impedance of the RLC tank. Using this code, the designer has the following degrees of freedom: choosing the bias current, the midband gain, the gain drop at one specific frequency (e.g. 0.1 dB at 10.2 MHz), and the center frequency of the bandpass filter.

```
1  % Author: Abbas Sabti
2  % Date: 18-6-2020
3  % Description:  Determines components RLC tank
4
5  % Parameters
6  G   = 55;   % [dB] Desired midband gain
7  a   = 0.1;   % [dB] Drop in gain at bandwidth edge
8  fo  = 10e6;  % [Hz] Resonance frequency
9  Ic  = 10;    % [mA] Biasing current
10
11 % Pre-calculations
12 a   = abs(a);   % To be sure it is positive
13 K   = 10^(-a/20);
14 gm  = Ic/26;    % [S] transconductance
15 BW  = 400e3;    % [Hz] Modulation bandwidth
16 wo  = 2*pi*fo;
17
18 % Calculations
19 R = 10^(G/20)/gm;
20 R = 1600
21
22 f1 = fo - BW/2;     % low cut-off
23 f2 = fo + BW/2;     % high cut-off
24
25 % filter can not hit both frequencies as desired
26 w = 2*pi*f1;
27 %w = 2*pi*f2;
28
29 syms L C positive
30 eqns = [(w*R*C)^2*(1-(wo/w)^2)^2 == K^(-2)-1, L*C == 1/wo^2];
```

```
vars = [L,C];
[Lx, Cx] = solve(eqns, vars);

R_kOhm = R/1e3
C_pF = double(Cx)/1e-12
L_uH = double(Lx)/1e-6
```

F.3 Input filter IF amplifier

The following MATLAB script calculates the required components values for the bandpass filter, at the input of the IF amplifier. As demonstrated in Subsection 6.3.2, the system to solve has too many degrees of freedom. Hence, the script focuses on displaying the various trade-offs:

```
% Author: Abbas Sabti
% Date: 18-6-2020
% Description:  Determines component values RLC tank in series with a
% resistor

clear all % Clear workspace

% Parameters
G = 55;     % [dB] Desired midband gain
a = 0.25;   % [dB] Drop in gain due to resistive divider
fo  = 10e6; % [Hz] Resonance frequency
Ic  = 10;   % [mA] Biasing current

% Pre-calculations
a   = abs(a);   % To be sure it is positive
K   = 10^(-a/20);
gm  = Ic/26;    % [S] transconductance
BW  = 400e3;    % [Hz] Modulation bandwidth
wo  = 2*pi*fo;

% Calculations
R = [100:50:1000, 1000:1000:3e3]; % There is an extra degree of freedom!
f1 = fo - BW/2;     % low cut-off
f2 = fo + BW/2;     % high cut-off

% filter can not hit both frequencies as desired
w = 2*pi*f1;
%w = 2*pi*f2;

Cx = zeros(numel(R));
Lx = zeros(numel(R));
syms L C positive
for i = 1:numel(R)
    eqns = [(w*R(i)*C)^2*(1-(wo/w)^2)^2 == K^(-2)-1, L*C == 1/wo^2];
    vars = [L,C];
    [Lx(i), Cx(i)] = solve(eqns, vars);
end

```

```
%% results
semilogx(R,Cx)
figure
yyaxis left
semilogx(R/1e3, Cx(:,1)/1e-12)
ylabel('C [pF]')
yyaxis right
semilogx(R/1e3, Lx(:,1)/1e-6)
ylabel('L [uH]')
title(['Tradeoff RLC'])
xlabel('R [k\Omega]')

%% extra
R = 200; % Select R based on previous tradeoff
R2 = [2e2:1e2:1e3, 1e3:100:3e3];
R1x = zeros(numel(R),numel(R2));
syms R1 positive
for i = 1:numel(R)
    for j = 1:numel(R2)
        eqns = [R1*R2(j)/(R1+R2(j)) == R(i)];
        vars = [R1];
        result = solve(eqns,vars);
        if (~isempty(result))
            R1x(i,j) = result;
        end
    end
end

n = ceil(sqrt(numel(R)));
m = ceil(numel(R)/n);
figure
for i = 1:numel(R)%:1:(numel(R)/2)
    subplot(n,m,1)%i)
    K = 100*(R2./(R2+R1x(i,:)));
    plot(R2, K)
    title(['R: ', num2str(R(i)), '\Omega'])
end
```

F.4 Class E amplifier

The following script is used to calculate all the required component values of a class E amplifier, based on the specifications.

```
%% Made by using https://ieeexplore.ieee.org/document/1523070
% Author: Lars Bouman
% Date: 18-6-2020
% Description: Calculate the component values of a Class E amplifier

%% Clear the workspace
clc;
close all;
```

```
clear;

%% Specs
Vcc = 12;         % [V]   supply voltage
Pl = 5;           % [W] Power delivered to the load
f0 = 98.4e6;      % [Hz]
w = 2*pi*f0;      % [rad]
L1 = 47e-9;       % [H] DC-feed inductance (between Vcc and collector)
Q = 2;            % Q factor
Rl = 50;          % [Ohm] Load impedance

%% Calculate ratio Xdc Rdc
Rdc = Vcc*Vcc/Pl;
Xdc = w*L1;
z = Xdc/Rdc;

%% Calculate R, B and X
if z < 5 && z > 1
    R = (Vcc*Vcc/Pl) * (1.979 - 0.7783*z + 0.1754*z*z - 0.01397*z*z*z);
    B = (1/R) * (1.229 - 0.7171*z + 0.1881*z*z - 0.01672*z*z*z);
    X = R * (-1.202 + 1.591*z - 0.4279*z*z + 0.03894*z*z*z);
elseif z >= 5 && z < 10
    R = (Vcc*Vcc/Pl) * (0.9034 - 0.04805*z + 0.002812*z*z - (5.707e-5)*z*z*z);
    B = (1/R) * (0.3467 - 0.02429*z + 0.001426*z*z - (2.893e-5)*z*z*z);
    X = R * (0.6784 + 0.006641*z - 0.003794*z*z + (7.587e-5)*z*z*z);
else
    disp('Error: z (Xdc/Rdc) not between 1 and 10!');
    L1_upper = 10*Rdc/w;
    L1_lower = Rdc/w;
    disp(['To adjust, put L1 between ', num2str(L1_lower), ' and ', num2str(L1_upper), '.']);
    error('Invalid z');
end

%% Calculate shunt capacitance and inductance
Cs = B/w;
Ls = X/w;

%% Calculate the RC oscilator parameters
syms L0 C0;
eqns = [Q == (1/Rl)*sqrt(L0/C0), f0 == 1/(2*pi*sqrt(L0*C0))];
S = solve(eqns, [L0 C0]);
L0 = double(S.L0(2));
C0 = double(S.C0(2));

%% Calculate matching capacitance and inductance
syms Lm Cm;
eqns = [R == Rl/(1+Rl*Rl*Cm*Cm*w*w), 0 == (w*Lm) - (w*Cm*Rl*Rl)/(1+Cm*Cm*w*w*Rl*Rl)];
S = solve(eqns, [Lm, Cm]);
Lm = double(S.Lm(2));
Cm = double(S.Cm(2));
fm = 1/(2*pi*sqrt(Lm*Cm));

%% Display the results
```

```
62 disp('DC inductor:');
63 disp(['L1: ', num2str(L1)]);
64
65 disp('Oscilator parameters:');
66 disp(['L: ', num2str(L0)]);
67 disp(['C: ', num2str(C0)]);
68
69 disp('Shunt parameters:');
70 disp(['L: ', num2str(Ls)]);
71 disp(['C: ', num2str(Cs)]);
72
73 disp('Matching parameters:');
74 disp(['L: ', num2str(Lm)]);
75 disp(['C: ', num2str(Cm)]);
76 disp(['Resonance at: ', num2str(fm)]);
```

Acronyms

ADS Advanced Design System.

AM Amplitude Modulation.

BJT Bipolar Junction Transistor.

CB Common Base.

CE Common Emitter.

EM Electromagnetic.

FM Frequency Modulation.

FMCW Frequency-Modulated Continuous-Wave.

IF Intermediate Frequency.

LNA Low Noise Amplifier.

LO Local Oscillator.

PA Power Amplifier.

radar RAdio Detection And Ranging.

RF Radio Frequency.

SNR Signal-to-Noise Ratio.

VCO Voltage Controlled Oscillator.

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