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Numerical Model of an Injection-Locked Wideband Frequency Modulator for Polar Transmitters

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(Invited Paper)

***Abstract*— We present a numerical model of a wideband injection-locked frequency modulator used in a polar transmitter for 3G cellular radio application. At the heart of the system is a self-injection-locked oscillator with a programmable linear tuning range of up to 200 MHz at 4-GHz oscillation frequency. The oscillator is injection locked to a time-delayed version of its resonating voltage, and its frequency is modulated by manipulating the phase and amplitude of the injected current. The model is used to study the feasibility of the proposed system by analyzing the impact of various impairments in the auxiliary injection loop on the system performance. The model is written in MATLAB/SIMULINK, and the simulation output is analyzed by a vector signal analyzer in terms of 3GPP specifications. Based on the simulation results, key specifications for individual blocks in the system are determined. The key benefits of the presented modeling methodology are simplicity, efficiency, and portability.**

***Index Terms*— All-digital phase-locked loop (ADPLL), digital phase rotator (DPR), digital-to-frequency converter (DFC), digital-to-RF amplitude converter (DRAC), digitally controlled oscillator (DCO), frequency control word (FCW), injection-locked frequency modulator (ILFM), multistage noise shaping (MASH), time-to-digital converter (TDC).**

I. Introduction

POLAR transmitters face a unique set of challenges when implemented in radios designed for wideband modulation standards such as WCDMA and LTE. The FM and AM paths require high linearity in order to maintain spectral purity of the transmitted signal. The design constraints are exacerbated if the transmitter implementation is discrete time and discrete amplitude, as in [1] where the information signal is processed by a digital-to-frequency converter (DFC) to generate FM and digital-to-RF amplitude converter (DRAC) to generate AM [2]. The DFC and DRAC are essentially DACs that must be designed with enough resolution in order to limit in-band and out-of-band quantization noise. The sampling rate f_s of these DACs should be set such that the replica images of the input signal are located far away from the carrier and especially outside the receive band if the intended operation of the transceiver is full duplex. However, if the sample rate of DFC is f_s, the extent of FM modulation is $\pm f_s/2$ [3]. Consequently, a high f_s imposes stringent linearity requirements on the RF oscillator over a wide frequency range. As an example, a DFC operating at 500 MHz will produce replica images at offsets beyond $\pm$250 MHz from the carrier. The RF oscillator gain must be constant within reasonable limits over a range of $\pm$250 MHz around the carrier frequency in order to preserve the signal integrity at the transmitter (TX) output. This is not a trivial challenge for an RF oscillator design. In the next section, we will describe various DFC architectures that address the aforementioned constraints for various wireless standards.

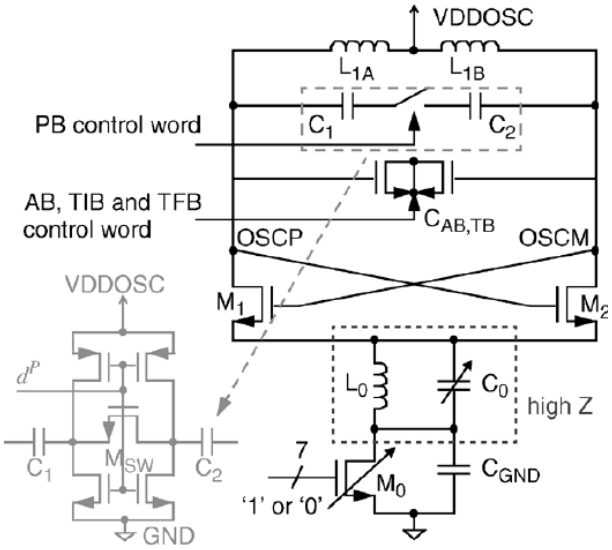

Fig. 1. DCO with capacitive tuning [4].

II. Evolution of Digital-to-Frequency Converters

One of the earliest implementations of DFC is detailed in Fig. 1 [4], which shows a digitally controlled oscillator (DCO) where FM is generated by varying the capacitance in the LC tank. The capacitor with the finest frequency resolution is controlled by a tuning word (TW) split into integer and fractional parts. The fine capacitor bank comprises an array of unit-weighted MOS capacitors (unit cells) selected by thermometer row and column decoders. The integer portion drives these capacitors directly while the fractional portion

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is applied to an 8-b multistage noise shaping (MASH) $\Sigma\Delta$ modulator (OSR $\geq$16) that drives a few unit cells in the capacitor array. The published FM tuning range is 5 MHz at 4-GHz oscillation frequency while the finest frequency step size with and without $\Sigma\Delta$ is 40 Hz and 40 kHz, respectively. The DCO gain (in units of Hz/LSB) in a switched-capacitor implementation such as [4] is linear over a small frequency range and therefore is suitable for narrowband modulation schemes, such as GMSK or 8-phase-shift keying only. Any FM distortion due to nonlinear DCO transfer function on a wideband FM signal will result in degradation of adjacent channel power (ACP) and noise far away from the carrier. Another challenging aspect is keeping the DCO frequency quantization noise low while achieving large linear FM range. One approach in addressing this challenge is to increase the number of finest capacitor cells in the array. This complicates the array implementation because increasing the matrix size will require high-order decoders, which in turn would increase routing complexity and would also impact the quality factor (Q) of the LC tank. The other approach is to increase the capacitor size while shifting the quantization noise away from the carrier into far-out frequencies. In this scenario, the peak of the quantization noise ("noise bump") at the DCO output is located at $f_s/2$, which is half the $\Sigma\Delta$ clock frequency. This noise bump may end up in the receive band or, in the worst case, at the duplex receiver channel, if implemented for a 3G/4G transceiver, and therefore will limit the local receiver sensitivity.

However, a proper balance between frequency resolution, total FM range, and far-out phase noise can be achieved through the use of segmented capacitor banks [5]. That design uses two segmented (coarse and fine) capacitor banks (thermometer encoded) to generate FM over a 250-MHz range. The coarse and fine segments contain 128 and 16 capacitors, respectively, with a gain of 1.95 MHz/LSB and 120 kHz/LSB, respectively. Three additional fine capacitors are driven by a 6-b MASH $\Sigma\Delta$ to improve the frequency resolution to 1.875 kHz. The published frequency range for this design is suitable for most wideband modulation schemes; however, the capacitor mismatch (either within a segment or between the segments) can limit the spectral purity of the transmitted signal if not constrained by design.

An improved version of the previously mentioned architectures uses incrementally sized capacitors instead of binary sizing. That architecture can address issues such as nonmonotonic frequency gain by employing one-hot encoding in the capacitor bank, i.e., select only one capacitor at a time to generate a discrete frequency. Reference [6] uses such topology on coarse and fine capacitor segments, where the i'th capacitor is $C_0 + i \cdot \Delta C$ and ΔC is proportional to the transistor width. The incremental change in transistor width is not as constrained in process technology as the smallest transistor width. This feature enables the DFC to achieve very fine frequency resolution while ensuring a monotonically increasing tank capacitance void of any discontinuities or overlaps between the coarse and fine segments. The published frequency resolution and total tuning ranges in [6] are 5 kHz and 10.24 MHz, respectively.

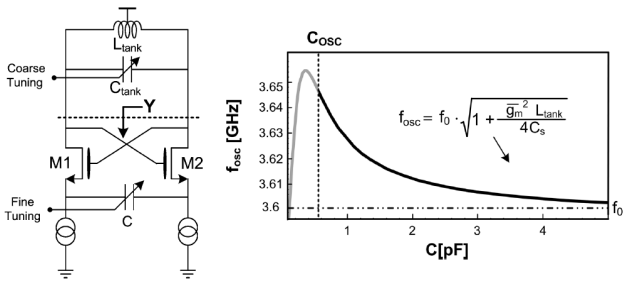

Fig. 2. High-resolution DCO using capacitive degeneration [7]. Left: circuit diagram. Right: DCO frequency versus tuning capacitance.

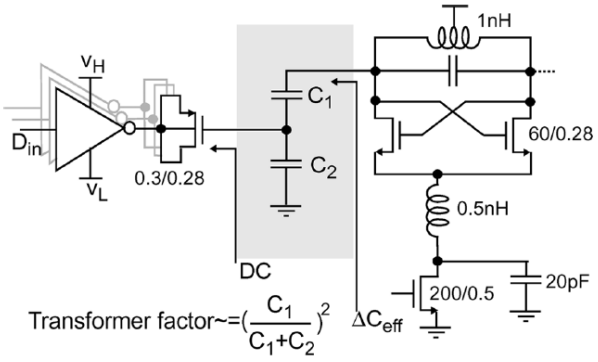

Fig. 3. DCO with capacitive transformer [8].

Another variant of switched-capacitor implementation that achieves very fine frequency resolution without $\Sigma\Delta$ dithering is through tuning of degeneration capacitor C, as shown in Fig. 2 [7]. C is typically large to facilitate the flow of ac currents in the circuit. The tuning range is approximately linear over a range that can be increased at the expense of current consumption. The published frequency gain range is 0.15–1.5 kHz, while the total tuning range is 2–12 MHz. The most positive attribute of this architecture is its ability to generate FM signals of high fidelity without burning current in a high-speed $\Sigma\Delta$ and its interface to the DCO.

The architecture presented in [8] meets the frequency tuning range requirement between narrowband and wideband FM modulations with the same capacitor bank using a capacitive transformer, as shown in Fig. 3. For wideband FM standards, the transformer factor (the equation in Fig. 3) is 0.5, and therefore the resulting ΔC_{eff} seen by the LC tank is large. For narrowband FM standards, the transformer factor is very low, thus reducing the frequency quantization to an acceptable level. This DFC was used to generate FM as part of an outphasing transmitter for 3G application.

The focus in most of the referenced works in this section so far has been in designing a DCO with linear and monotonic transfer function with respect to the tank capacitance. A very different strategy outlined in [9] bypasses the challenges in the aforementioned architectures completely by shifting the focus away from the oscillator and into a secondary loop. This architecture uses a negative feedback loop, also known as the frequency-to-voltage converter, to linearize the oscillator gain as a function of the input control, as shown in Fig. 4. Despite this advantage, there is a tradeoff between accuracy and speed of the negative feedback loop. The latency of the

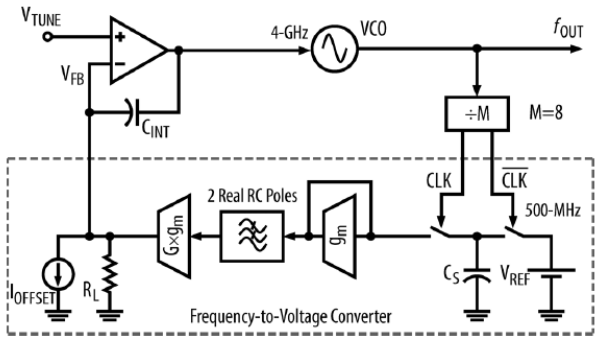

Fig. 4. Wideband frequency modulator using frequency-to-voltage converter in negative feedback loop.

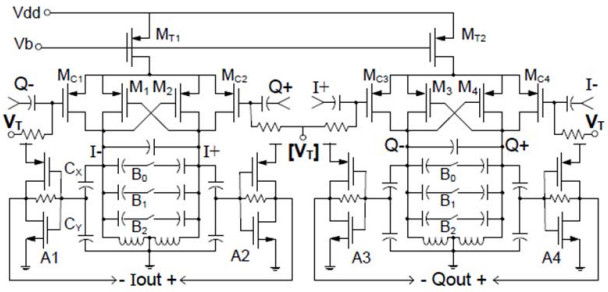

Fig. 5. QVCO with frequency tuning by varying coupling strength [10].

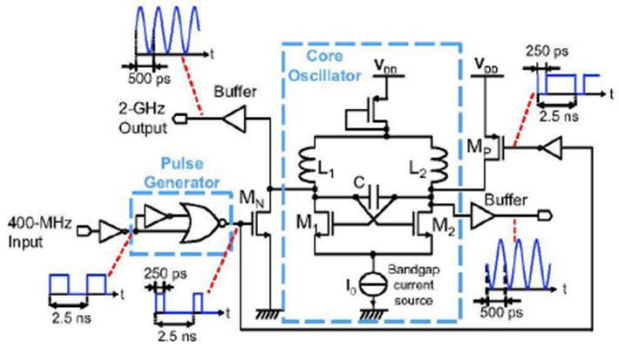

Fig. 6. Injection-locked transmitter for narrowband FM [11].

loop is measured to be 20±1.8 ns, and only the static portion of this group delay is compensated for. While this architecture cannot be classified as a DFC because of its continuous time and analog operation, it is worth mentioning here because it is the only reference published with decent EVM and ACLR performance on a 3G test vector.

In addition to the presented architectures, another class of frequency modulators uses the injection-locking technique, as shown in Fig. 5. This circuit is also known as quadrature voltage-controlled oscillator (QVCO) in which two oscillator cores are cross coupled such that once the system is injection locked, the pair generates quadrature phases. In this implementation, the FM is generated by modulating the coupling strength between the two cores through an analog voltage V_T. The published linear tuning range is 60 MHz. The main challenge with this system is the presence of mismatches between the two cores that can generate spurious emissions in sensitive bands and risk compliance with radio specification.

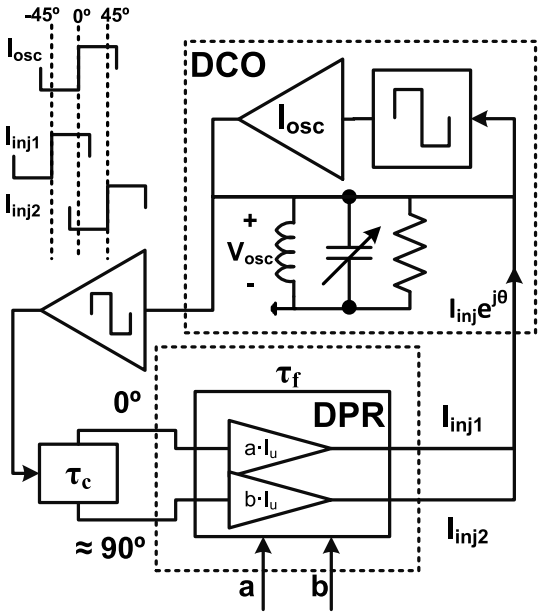

Fig. 7. Block diagram of the wideband frequency modulator through self-injection locking [12].

Finally, Fig. 6 shows an injection-locked GMSK transmitter [11]. In this architecture, the oscillator is injection locked to a harmonic of the injected signal. The FM at transmitter output is a scaled version of the FM on the injected signal. Although this simple architecture offers FM bandwidth scaling, its limiting factor is the injection-locking range, which is proportional to the injected signal strength. The pulse generator circuit generates the harmonic in the passband of the LC tank depending on the duty cycle of the output signal. Other challenges include managing the duty cycle of the pulse generator output across process, supply voltage, and temperature.

III. Proposed Solution

Our proposed solution generates FM through injection locking, as shown in Fig. 7 [12] where the oscillator is injected with a current $I_{\text{inj}}e^{j\theta}$ that is a θ phase delayed version of its resonating voltage V_{osc}. The frequency of the injection-locked oscillator ω_{out} under such a condition can be derived from Adler's equation [14]

$$\omega_{\text{out}}[n \cdot t_s] = -\frac{\omega_0}{2Q} \cdot \frac{I_{\text{inj}}}{I_{\text{osc}}} \cdot \sin(\theta[n \cdot t_s]) + \omega_0 \qquad (1)$$

where ω_o is the resonant frequency of the LC tank, Q is its quality factor, I_{osc} is the peak oscillator current, and I_{inj} is the peak injected current into the LC tank. $\theta[n \cdot t_s]$ is the phase between I_{osc} and I_{inj} sampled at the DFC rate $f_s = 1/t_s$. By manipulating the phase of the injected current, and consequently θ, the steady-state oscillator frequency ω_{out} varies according to (1). Within a reasonable range of θ around 0°, ω_{out} linearly increases with θ. The maximum variation of ω_{out} about ω_0, for which the DCO is injection locked, is limited by the injection-locking range ω_L given by the following equation:

$$\omega_L = \omega_0 \cdot \frac{I_r}{2Q} \qquad (2)$$

where $I_r = I_{\text{inj}}/I_{\text{osc}}$. In this design, θ is modulated by the digital phase rotator (DPR) block. The DPR block is essentially two interleaved current steering DACs that are used to interpolate between two quadrature signals, namely, I_{inj1} and I_{inj2}. θ, therefore, is determined by the ratio of I_{inj1} and I_{inj2}. The magnitude of the injected current I_{inj} is controlled by the unit cell current I_u and the digital code a and b. The linear frequency tuning range is determined by ω_L, which is proportional to I_r. Both I_{osc} and I_{inj} are digitally controlled, and therefore the DCO gain (Hz/LSB) and the linear FM tuning range can be scaled according to the desired application. This is the strongest feature of this architecture when compared with the DFC architectures presented in Section II.

The performance of the circuit shown in Fig. 7 is critical in determining the system (described in Section IV) performance. Of particular interest is the effect of noise originating from two critical blocks: all-digital phase-locked loop (ADPLL) and DPR. We propose a numerical model developed in MATLAB/SIMULINK that can model a vast number of impairments in the FM path and apply it to a baseline IQ vector for the desired standard. The AM path impairments are not modeled as they are considered outside the scope of this paper. The resulting IQ vector at the transmitter output can be analyzed by a vector signal analyzer (VSA) to calculate important metrics such as EVM and ACP. A similar exercise can be performed in Verilog-AMS; however, certain blocks such as RF oscillator may have to be abstracted to reduce simulation time [2]. A full transistor-level simulation of the injection-locked frequency modulator (ILFM) shown in Fig. 8 is useful for the final verification test before tape out. However, such flow is impractical for comparative study, architectural analysis, and noise budgeting. The proposed modeling scheme has several benefits. First, it relieves the burden of developing postsimulation processing scripts. The complexity of such scripts increases with emerging standards that are supporting a wide variety of signaling scenarios, modulation schemes, and packet types. Countless hours have to be invested in maintaining such scripts for an evolving wireless standard. Second, the impact of block-level impairments can be studied directly in terms of key performance metrics of the wireless standard.

IV. System Overview

The intended application for the proposed solution is a wideband digital polar TX, as shown in Fig. 8. In this architecture, the switched-capacitor bank in the DCO is tuned to the desired channel, while the proposed technique is used to perform the wideband FM modulation around the channel frequency. The digital frequency TW is normalized according to the calibrated DCO gain and then converted into current control inputs (a and b) to the DPR circuit. The 6-b integer portion of the current control is applied to the DPR array after binary-to-thermometer encoding process. The 6-b fractional portion is applied to the array post-$\Sigma\Delta$ processing. Current controls a and b determine the magnitude of the quadrature vectors I_{inj1} and I_{inj2} that are interpolated by the LC tank of the DCO while θ from (1) is $\tan^{-1} b/a$. The circuit enclosed by the dashed line in Fig. 8 is the ILFM that was fabricated and tested in [12]. All measurements in that work were performed in open-loop configuration and without the ADPLL. The focus of this paper is to present a model of the entire transmitter system with the simulation results.

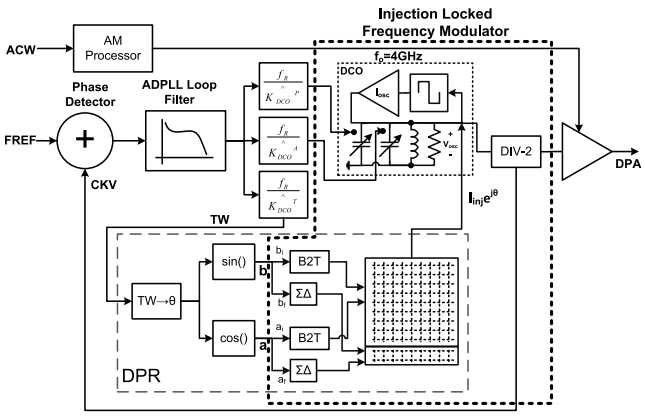

Fig. 8. Block diagram of complete TX system employing ILFM.

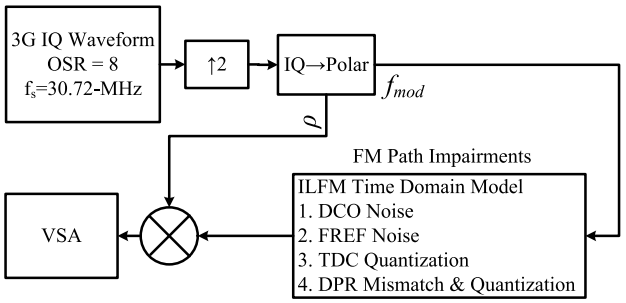

Fig. 9. System test bench of DFC employing ILFM.

V. System Model

The system evaluation test bench of the DFC employing the ILFM is shown in Fig. 9. We have chosen a simple form of 3G voice signal to test the model. The final complex vector is analyzed by VSA to determine EVM and ACLR per 3GPP specification. The first block in the model generates the 3G IQ waveform. The method of generating spread-spectrum signals for UMTS applications is described in great detail in [13]. As discussed earlier, the sampling rate of the DFC is constrained by the out-of-band spurious emissions specification and the linear tuning range of the RF oscillator. In our study, a baseband oversampling rate of 8 is used, which is upsampled by a factor of two using a cubic Lagrange interpolator bringing the sampling rate of the DFC to 61.44 MHz. The replica images are located at a distance of $\pm$30.72 MHz from the carrier. The required linear FM range at DCO output is $\pm$61.44 MHz for the TX high-band port and $\pm$122.88 MHz for the TX low-band port. This is assuming that the oscillator core is running at 4 GHz, and the TX high and low-band ports are sourced from a divide-by-two and divide-by-four stage, respectively.

The time-domain model of ILFM comprises the ADPLL employing a two-point modulation scheme, as shown

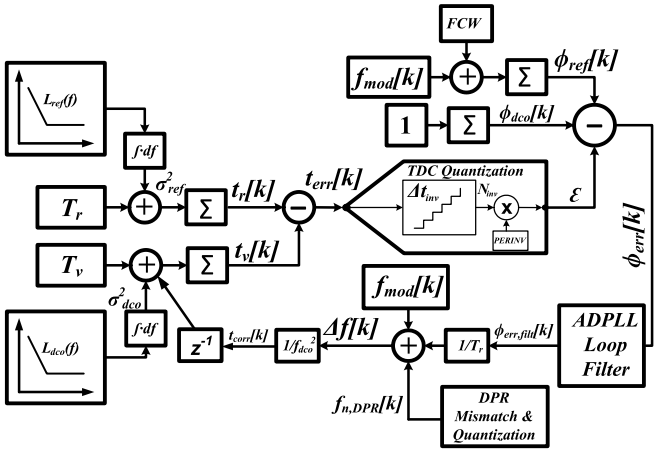

Fig. 10. Time-domain model of ILFM with impairments.

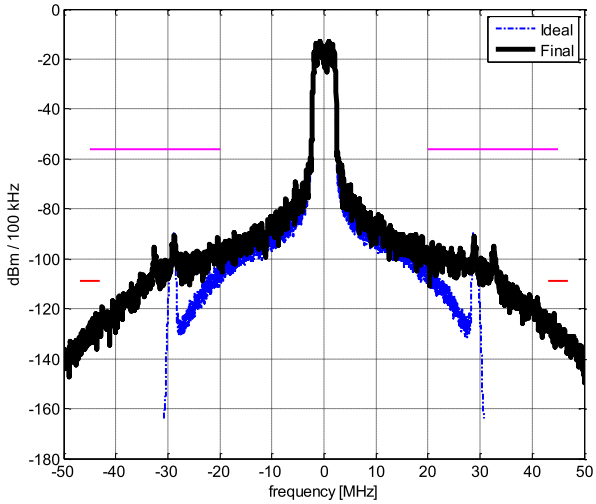

Fig. 11. Wideband spectrum simulated with 2% mismatch in DPR array.

in Fig. 10. The FM portion of the baseband signal is passed to the model as discrete-time samples $f_{\rm mod}[k]$ after undergoing the processes shown in Fig. 9. The model includes impairments such as reference phase noise $\mathcal{L}_{\rm ref}(f)$, DCO phase noise $\mathcal{L}_{\rm dco}(f)$, time-to-digital converter (TDC) quantization noise and DPR quantization, and mismatch noise. The TDC quantizes the time between the reference clock and the DCO clock edges into a number of inverter delays in a similar fashion that a flash ADC quantizes an input voltage by comparing it with references generated by a resistive ladder network. Therefore, the TDC quantization noise is proportional to the inverter delay $\Delta t_{\rm inv}$ similar to a flash ADC whose quantization noise is proportional to a voltage step Δ. The reference and oscillator phase noise spectra are integrated into timing error variance $\sigma^2_{\rm ref}$ and $\sigma^2_{\rm dco}$, respectively. This timing jitter is added to the reference period T_r and accumulated over time to generate reference time stamps $t_r[k]$. Similarly, the oscillator timing jitter is added to the oscillator period T_v and is accumulated over time to generate oscillator time stamps $t_v[k]$. The timing error correction value from the loop, $t_{\rm corr}[k]$, is 0 for $k = 0$. Since the oscillator clock frequency is much higher than the reference frequency, the oscillator period is accumulated until it is just within one clock period of $t_r[k]$. This time stamp is labeled as $t_v[k]$ in Fig. 10. The difference between $t_v[k]$ and $t_r[k]$ is quantized by the TDC into a number of inverter delays and normalized into fractional phase error ϵ by a calibrated factor $PERINV = T_v/\Delta t_{\rm inv}$. Without $PERINV$, the number of delays between two clock edges would be meaningless. During the calibration, DCO clock is sampled by the TDC while the digital logic captures the number of delay stages between two successive 0-to-1 transitions of the DCO signal. This information is stored in register as $PERINV$. The integer phase error is determined by subtracting the oscillator phase $\phi_{\rm dco}$ and reference phase $\phi_{\rm ref}$. $\phi_{\rm ref}$ is the accumulation of FM from the baseband signal $f_{\rm mod}$ and the frequency control word (FCW), where FCW determines the channel frequency at the TX output. $\phi_{\rm dco}$ is the number of oscillator clock cycles. It should be noted that due to the coarse nature of phase error in this path, the phase error due to jitter (phase noise) is not included in this path. The final phase error $\phi_{\rm err}$ is the sum of fractional phase error calculated by the TDC and the coarse phase error, which is the difference between the number of reference and oscillator clock cycles.

$\phi_{\rm err}$ is filtered by the ADPLL loop filter defined by loop parameters α, ρ, and γ [2]. The rate of change of $\phi_{\rm err,filt}$ with respect to the sampling time of the ADPLL, T_r, determines the frequency correction. This correction combined with the FM part of the information signal $f_{\rm mod}[k]$ is applied to the DCO as oscillator TW. At this point in the loop, we can add impairments in the DPR, such as random mismatch and quantization noise. The DPR quantization noise is determined by the current of the unit cell in the array that can be translated into frequency quantization post-$\Sigma\Delta$ processing. The DPR random mismatch in current, determined by the transistor size and overdrive voltage of the current source, is translated into frequency noise. The sum of these two frequency noise sources $f_{\rm n,DPR}[k]$ is added to the frequency error signal at the PLL output with $f_{\rm mod}[k]$ to determine $\Delta f[k]$. $\Delta f[k]$ is the final frequency offset from the initial DCO frequency $f_{\rm dco}$ that can be translated into a time-domain correction of $t_{\rm corr}[k]$ using an approximation derived in [2, eq. (2.21)] that relates an infinitesimally small timing correction required to compensate for reasonably small frequency error

$$t_{\rm corr}[k] = \frac{\Delta f[k]}{f_o^2}. \tag{3}$$

The timing correction is fed back into the loop to determine the next time stamp of the oscillator $t_v[k+1]$. It is important to understand how the current mismatch in the DPR is injected as frequency noise in the ADPLL. The ADPLL utilizes two-point modulation scheme [2] to generate desired FM at the TX output. In this case, the loop gain transfer function derived in [15] has a term $r = K_{\rm DCO}/\widehat{K}_{\rm DCO}$, where $K_{\rm DCO}$ is the physical DCO gain and $\widehat{K}_{\rm DCO}$ is the estimated DCO gain. In such a predictive close-loop modulation scheme, $r \approx 1$, which means that the loop gain is independent of DCO gain (unlike in conventional analog PLLs). This condition is necessary for a distortion-free transmission of FM signal $f_{\rm mod}[k]$. However, due to the current mismatch in the DPR array, $K_{\rm DCO}$ should be

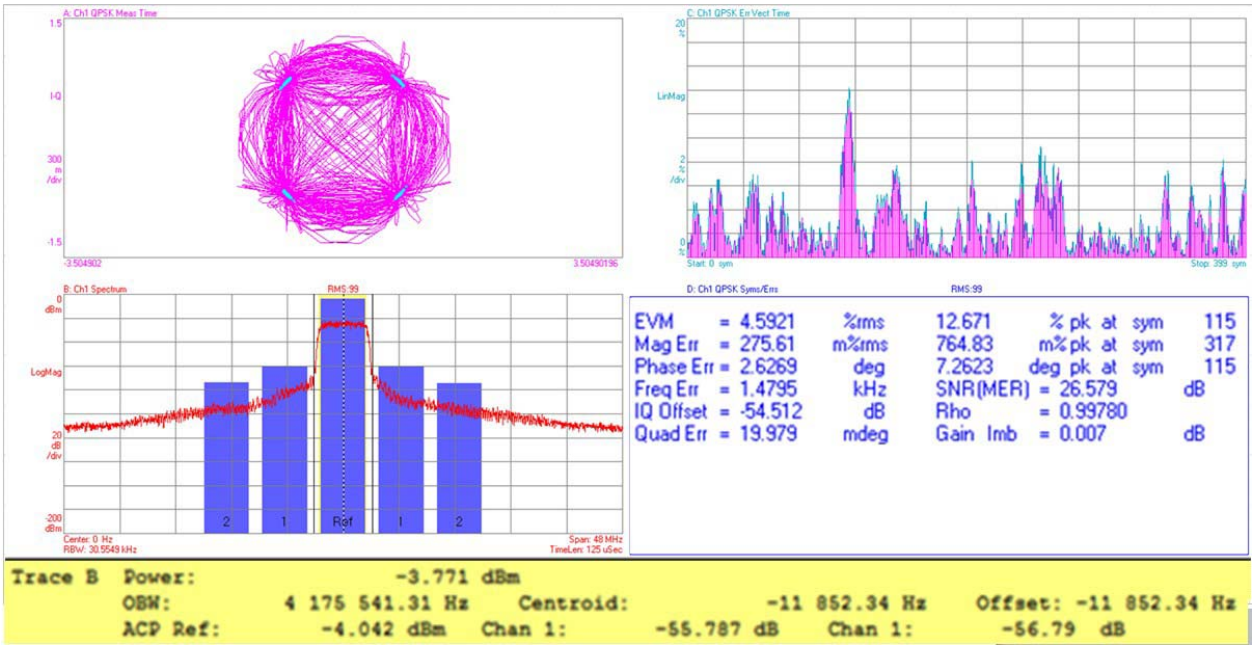

Fig. 12. VSA simulation result with 1% mismatch in DPR array.

treated as a random variable. Therefore, r becomes a random variable since $\widehat{K}_{\mathrm{DCO}}$ is not dynamically controlled with the DPR controls a and b. The net result is a frequency noise injected at the DCO input, and the effect of this impairment is more severe at far-out frequency offsets. The simulation results shown in Section VI will underscore this fact.

VI. Simulation Results

The model shown in Fig. 10 is run over an entire 3G frame of 10 ms. The root mean square (rms) phase error for the oscillator (at 2 GHz) and the reference (at 38.4 MHz) is 1.2° and 0.01°, respectively. The setting of α, ρ, and γ is such that the 0-dB closed-loop bandwidth (after peaking) is around 120 kHz. The TDC quantization (Δt_{inv}) is 20 ps, DCO gain is 1 MHz/LSB, and DCO quantization post-$\Sigma\Delta$ dithering is 1 kHz/LSB. This is assuming a 6-b input to the MASH $\Sigma\Delta$ modulator and an OSR of 8.

Fig. 11 shows the TX wideband spectrum with all the distortions turned on and a DPR random mismatch of 2%. The magenta line is the specification limit for TX noise in RX band through the antenna port that could desensitize a neighboring mobile-station receiver. The red line is the specification limit for TX noise in RX band that can leak into the local receiver and desensitize it. In order to be compliant with this specification, the mismatch in DPR block needs to be less than 2%. From Fig. 11, the replica images of the baseband signal are visible around 30 MHz.

Fig. 12 shows the VSA measurement of the final IQ data with all the distortions turned on. The top-left window shows the constellation, and the bottom-left window shows the ACLR. Table I shows the EVM and ACLR measured by the VSA for varying degrees of mismatch in the DPR circuit. With no mismatch, the baseline rms EVM is 4%, which is due to ADPLL noise. The impact on DPR mismatch is most severe on ACLR at 5- and 10-MHz offsets and less on EVM.

TABLE I
Effect of DPR Mismatch on EVM and ACLR

Case	RMS EVM [%]	PK EVM [%]	ACP5MHz Lower [dB]	ACP5MHz Upper [dB]	ACP10MHz Lower [dB]	ACP10MHz Upper [dB]
Ideal	4.0	18	-61.5	-61.7	-72.7	-72.4
$\sigma^2_{DCO}+\sigma^2_{REF}+TDC$	4.0	18	-61.5	-61.7	-72.7	-72.4
+1% Mismatch	4.6	18	-55.8	-56.8	-70.1	-70.1
+2% Mismatch	6.5	23	-54.2	-53.0	-67.9	-67.4
+3% Mismatch	6.6	24	-49.8	-52.5	-62.9	-61.9
+4% Mismatch	6.5	30	-47.2	-51.2	-59.3	-59.4
+5% Mismatch	7.5	30	-51.4	-50.4	-66.5	-64.8

The 3GPP specification for rms EVM and ACLR (at 5-MHz) is 17% and −33 dBc at the PA output. From Table I, we conclude that the transmitter performance is within specification with mismatches as high at 5% at which point the ACLR (at 5-MHz offset) is −50 dBc. While the TX has a plenty of margin for ACP with a DPR mismatch of 5%, the performance-limiting specification in that case is the noise in RX band that can desensitize the local receiver.

VII. Conclusion

We have proposed a time-domain model for an ILFM for a wideband discrete-time polar transmitter. The sample rate of the baseband signal and FM bandwidth are set in order to satisfy spectral mask and linearity requirements. Finally, the noise sources in the ADPLL and DPR are budgeted through quantitative analysis. The runtime of the model is less than 15 s per 3G frame. The model is portable to numerous radio standards and avoids the burden of developing postprocessing algorithms for compliance testing.

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