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ABSTRACT

This paper investigates the electrical properties of boron-doped diamond-graphene (B:DG) nanostructures, focusing on their semiconductor characteristics. These nanostructures are synthesized on fused silica glass and Si wafer substrates to compare their behaviour on different surfaces. A specialized measurement system, incorporating Python-automated code, was developed for an in-depth analysis of electronic properties under various contact configurations. This approach allowed for a detailed exploration of charge transport mechanisms within the nanostructures. The research highlights a decrease in resistivity with increased deposition time, as shown by Arrhenius plot analysis. This trend is linked to the formation and evolution of multi-wall graphene structures. SEM images showed nanowall structures formed more readily on amorphous fused silica substrates, enabling unrestricted growth. TOF-SIMS analysis revealed uneven boron atom distribution through the film depth. A significant finding is a reduction in conductive activation energy in samples grown in microwave plasma from 197 meV to 87 meV as deposition time increased from 5 to 25 min. Furthermore, the study identifies a shift in transport mechanisms from variable range hopping (VRH) below 170 K to thermally activated (TA) conduction above 200 K. These insights advance our understanding of the electronic behaviours in B:DG nanostructures and underscore their potential in electronic device engineering, opening new paths for future research and technological developments.

1. Introduction

Researchers are directing their attention toward the development of materials that possess high thermal and electrical conductivity, biodegradability, and compatibility with living systems. Numerous paths of investigation are dedicated to exploring carbon structures at the nanoscale such as graphene [1], carbon nanotubes [2], fullerenes [3], nano-onions [4], diamond films [5], and carbon nanowall structures [6], which can meet the majority of the criteria mentioned above.

The primary methods of synthesising carbon structures are the different variants of plasma-enhanced chemical vapour deposition (PECVD): using microwave plasma (MW CVD) [7,8], radio wave-excited plasma (RF CVD) [9,10], direct current-excited plasma (DCP CVD) [11], and radical injection [7,12]. Other CVD methods do not use plasma [6,13], including hot filament reactors (HF CVD) [14]. The utilisation of CVD techniques capable for controlled fabrication [15] has resulted in the development of carbon structures doped with other elements with modified semiconductive properties [16–20].

Thin diamond-graphene structures, used in the production of supercapacitors [21], hydrophobic surface coatings [22], field emitters [20], electrodes for lithium-ion batteries [22], miniaturized electrochemical and spectroelectrochemical cells [23,24], and sensors [25,26] are self-organised, vertically-oriented stacks of flat graphene structures, such as carbon nanowalls (CNWs) additionally covered with diamond

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phases [17,27]. The sheets form a self-supporting network of wall structures, which are merely 1–2 μm tall, 0.1–2 μm wide, and with thickness values ranging from a few to several tens of nanometres [8,18,28].

Depending on the fabrication method and process parameters, the growth of CNWs can be controlled, including their height [19,29], density [12,19], and shape of nanowall [30,31], which consequently influences electrical parameters such as resistivity [32], conductivity [33,34], or carrier mobility [19]. Additionally, the type and concentration of dopants can also change the electrical properties of the material, including resistivity [13,26], charge capacity [35], and field emission [10,28,36]. Notably, both p-type and n-type conductivity can be obtained [35].

Several recent works have explored key methodologies for analysing the current–voltage (I-V) characteristics of nanocarbon semiconductors in relation to temperature variations [37,38]. An automatic I-V testing is notable for its application in assessing electrical properties like resistance and capacitance, which is especially valuable in the electronic industry [39–41]. The mentioned method aided in optimizing industrial processes by guiding the selection of appropriate design parameters, thus enhancing the understanding of semiconductors' performance in quick changing environments [42].

This work aims to explain the interplay between the electronic parameters of boron-doped nanowall diamond-graphene (B:DG) structures and their growth parameters and measurement temperatures. The investigation delves into these nanostructures, synthesized on fused silica glass and silicon wafer substrates to establish a reference surface. First, high-resolution scanning electron microscopy and time-of-flight secondary ion mass spectrometry were employed for surface morphology analysis and boron concentration profiling, respectively. Then, to facilitate a comprehensive analysis of the electronic properties under diverse contact configurations, a dedicated low-cost measurement system allowing to work with various source-measure units was developed. This system integrates automated Python-supported code investigations, enabling an exploration of the electronic characteristics. Within the scope of this study, a comprehensive discourse on the factors having a discernible impact on charge transport mechanisms is presented. This discussion is underpinned by a thorough correlation analysis that intertwines these observed transport mechanisms with the morphological parameters and the inherent molecular structure of the (B:DG) architectures. Through this investigation, a deeper understanding of the underlying principles governing electronic behaviours is possible.

2. Experimental procedures

2.1. Growth of boron-doped diamond-graphene (B:DG) nanostructures

Boron-doped diamond-graphene structures (B:DG) were fabricated utilising the Microwave Plasma Assisted Chemical Vapour Deposition system (AX5200S MWPECVD System, Seki Technotron) with the parameters shown in Table 1. Before growth, the substrates (fused silica, 99.99 % purity, JGS-2, Continental Trade, Poland; and silicon wafer, 10×10×5 mm, p-type ⟨1 0 0⟩, Microactiv, Poland) were cleaned twice in an ultrasonic bath: first in acetone for 5 min, and second in 2-propanol for 5 min. Subsequently, substrates were immersed in a deionized water suspension containing 1 % detonated nanodiamonds (NanoAndo, Japan) and placed in the ultrasonic bath for 15 min [43]. The cleaning and seeding procedures were previously reported in [44,45]. Two process times were used – 5 and 25 min. The two-colour pyrometer (Williamson Pro 92-40-C, USA) was controlling the temperature of graphite induction susceptor on which was placed molybdenum stage with substrates. The pyrometer was set to measure temperature at the centre of the stage. Diborane was used as a dopant precursor during the growth. Additionally, N_2 was used as a nitrogen precursor (flow rate = 3 sccm).

2.2. Structural characterization

The topographies of the B:DG surfaces were analysed utilising an FEI Quanta FEG 250 scanning electron microscope (SEM). The microscope operated at a 10 kV beam acceleration voltage and observations were conducted under high vacuum conditions (pressure: 0.1 mPa). The SE-ETD detector (secondary electron – Everhart-Thornley detector) was employed for these observations. Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) measurements were performed to evaluate the boron concentration in depth at room temperature in Q-850-05 and Q-850-25 samples. Analysis was performed on the as-prepared samples using a "TRIFT V nanoTOF" instrument (Physical Electronics, Chanhassen, MN) equipped with a 30 keV Ga^+ source. The bunched, primary Ga^+ ion beam was scanned over an area of 100 μm × 100 μm. Positive secondary ion spectra were collected from 0 to 1850 *m/z*. Charge compensation was achieved by flooding the sample surface with low-energy electrons and with 10 eV Ar^+ ions. The mass scale of the positive ion spectra was calibrated using the CH_3^+, $C_2H_3^+$, and $C_3H_5^+$ peaks before further analysis. For sputtering, a 3 keV Ar beam was scanned over an area of 400 μm × 400 μm with a 10 s sputter time per step with 20 or 28 steps in total. The sputter rates are different in BDD and substrate (specifically, when fused silica substrate is used), therefore, a direct conversion of depth per sputter time might not be accurate. Crater depths of approximately 316 nm and 468 nm, reflecting layer thicknesses, were obtained for the Q-850–05 and Q-850–25 samples, respectively. Before analysis, the samples were coated with a thin layer of gold (20 nm).

2.3. Setup for electrical measurement

The laboratory setup for electrical measurements of B:DG structures is shown in Fig. 1. It contains a computer, a probe stage with controller (T95, Linksys), a cooling system (LNP95, Linksys), a microscope (LAB40, OPTA-TECH), and a source-measure unit (2400, Keithley) integrated with a custom-designed system (Fig. 1A). The source-measure unit can serve as a source of voltage or current, and is thus capable of measuring both current and voltage. The photo of the setup is shown in Fig. 1B.

The samples (Q-850-05 and Q-850-25) were measured using the four-point Van der Pauw method at a constant voltage in four different configurations. Fig. 1C shows the control system connected to the probe stage with numbered points, where points 1 and 2 are responsible for measuring the current flowing through the sample, while points 3 and 4 measure the voltage applied to the sample. The next configuration rotates these points clockwise by 90°, changing the sample side currently being measured.

In case of the samples on silicon wafer (Si-850-05 and Si-850-25),

Table 1
B:DG samples and the corresponding deposition parameters.

Sample	Substrate	H_2 [sccm]	H/C [%]	N/C [%]	B/C [ppm]	Temperature [°C]	Pressure [Torr]	Microwave power [kW]	Time [min]
Si-850-05	Silicon	107.5	12	0.6	5 k	850	50	1.3	5
Si-850-25	Silicon	107.5	12	0.6	5 k	850	50	1.3	25
Q-850-05	Fused silica	107.5	12	0.6	5 k	850	50	1.3	5
Q-850–25	Fused silica	107.5	12	0.6	5 k	850	50	1.3	25

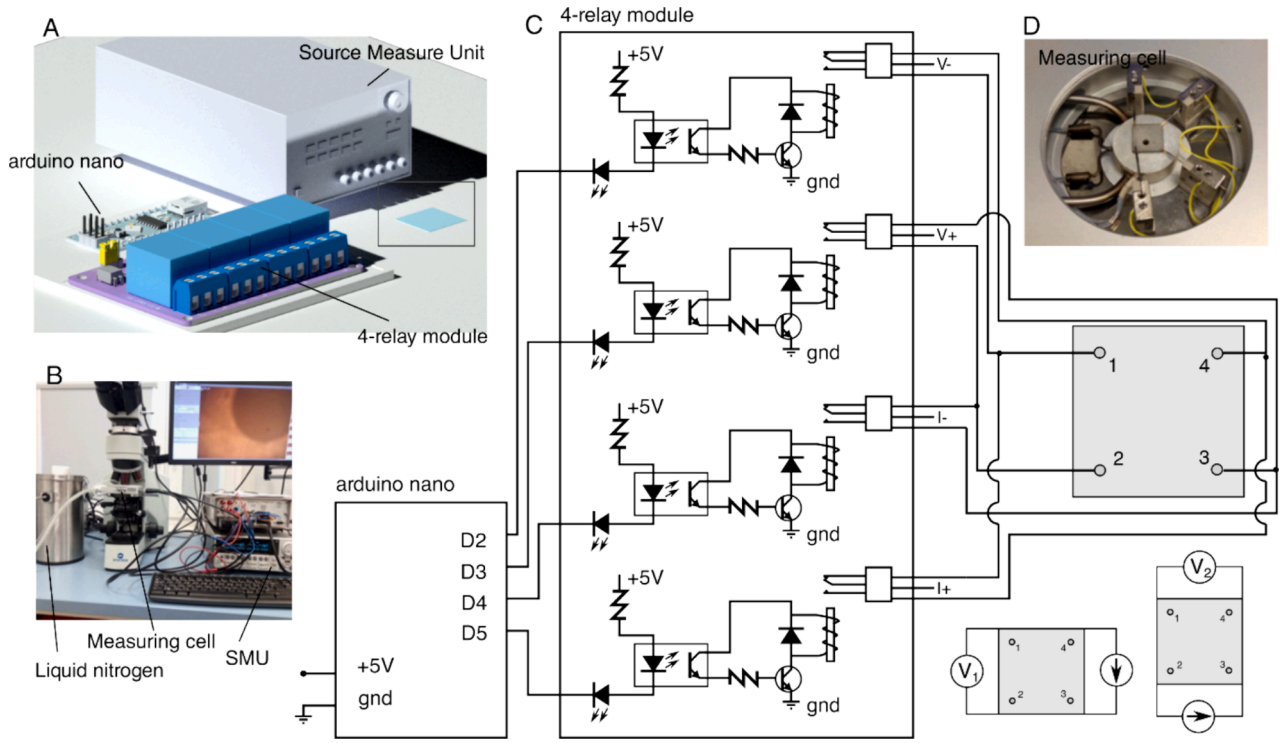

Fig. 1. Laboratory setup for resistivity measurements. **A)** Schematic illustration of the power source and measure unit, and the probe stage and control system. **B)** Image of the actual setup with the liquid nitrogen. **C)** Electronic diagram of the control system. **D)** Image of the Linkam probe stage.

measurements were conducted in a sandwich configuration utilising ohmic contacts. The current flow through the samples was investigated under voltage excitation (up to 0.1 V).

The probe stage shown in Fig. 1D is equipped with four gold-plated tungsten needles and is capable of electric measurements of the samples while accurately controlling the temperature inside the gas-tight environment. The samples are placed on the heating stage, and the positions of the four needles are adjusted manually so that their tips touch the corners of the square-shaped sample. The Python dedicated code was developed to control designed system. At the beginning of the code, the necessary libraries for data analysis, data visualization, communication with external devices, folder creation, and time delay are imported. Then, several global variables are defined, such as the initial and final measurement temperature, temperature step, ramp rate, correction factors, stabilization time, measurement time, Arduino and source measure unit address, maximum measurement current/voltage, and measurement mode (two-wire or Van der Pauw method). In the further part of the code, the 'init()' function is called, which initializes the connection with the source-measure unit. It sets the sense and source function, range and measurement mode. Then, depending on the user's choice of a measurement mode (van der Pauw/two-wire), the 'vdp()' or iv()' function is called. The 'vdp()' function sends a configuration message to the Arduino and waits for a response. Then, it calls the 'measurement()' function five times for one Van der Pauw configuration and stores the results in an Excel file and saves a figure as a PNG file. The saved files contain the average resistance from five measurements and the standard deviation. In the case of two-wire measurements, the iv()' function is called, which calls the 'measurement()' function five times for one temperature. In this case, only one configuration is required. After running the code, the measurement begins. From this point on, the measurements take place in a loop at a specified time interval defined by the user.

3. Results and Discussion

3.1. Structure and topography of B:DG nanostructures

Sample surface images made with a scanning electron microscope on fused silica and silicon plates are shown in Fig. 2. Nanowall structures were formed more effectively on fused silica glass plates (Q-850) compared to silicon wafer substrates (Si-850). For 5-minute samples, only localised point structures can be seen. As the deposition process duration increases, these structures begin to combine, forming more pronounced lines. After 25 min of deposition, the samples show clear nanowall structures. The SEM images were used to estimate the wall thickness and length of the structures produced: for the Q-850-25 sample, the nanowall length was 208 to 369 nm with a thickness of 58 to 73 nm, while for the Si-850-25 sample, the nanowall length was 157 to 298 nm with a thickness of 50 to 66 nm. Analysis of the SEM images of the samples shows how much substrate and deposition duration of the B:DG structure affect the surface. Nanowall structures are formed more effectively on fused silica plates due to the amorphous structure of the plate, which allows the structures to grow without having to conform to the crystal system of the plate. This permits the nanowalls to form directly at the nucleation sites, resulting in longer nanowalls with a lower count per 1 μm^2 compared to fused silica plates. Process duration is crucial when producing carbon structures, as it determines the quality of the resulting nanostructures. Briefly, the growth mechanism involves producing CN and HCN radicals and substituting them with CH_x radicals on the sample surface; the process is described in [36].

During a very short 5-minute growth, the structures do not have sufficient time to form on fused silica plates, and as a result, produce cauliflower structures, while when given 25 min, the nanostructures form developed maze-like carbon nanowalls similar to the structures produced during much longer growth times of 6 or 12 h [17,46]. The observed variations in the surface morphology of the samples are largely influenced by the substrate on which they are fabricated and the duration of the growth process. Topographic differences are projected to be

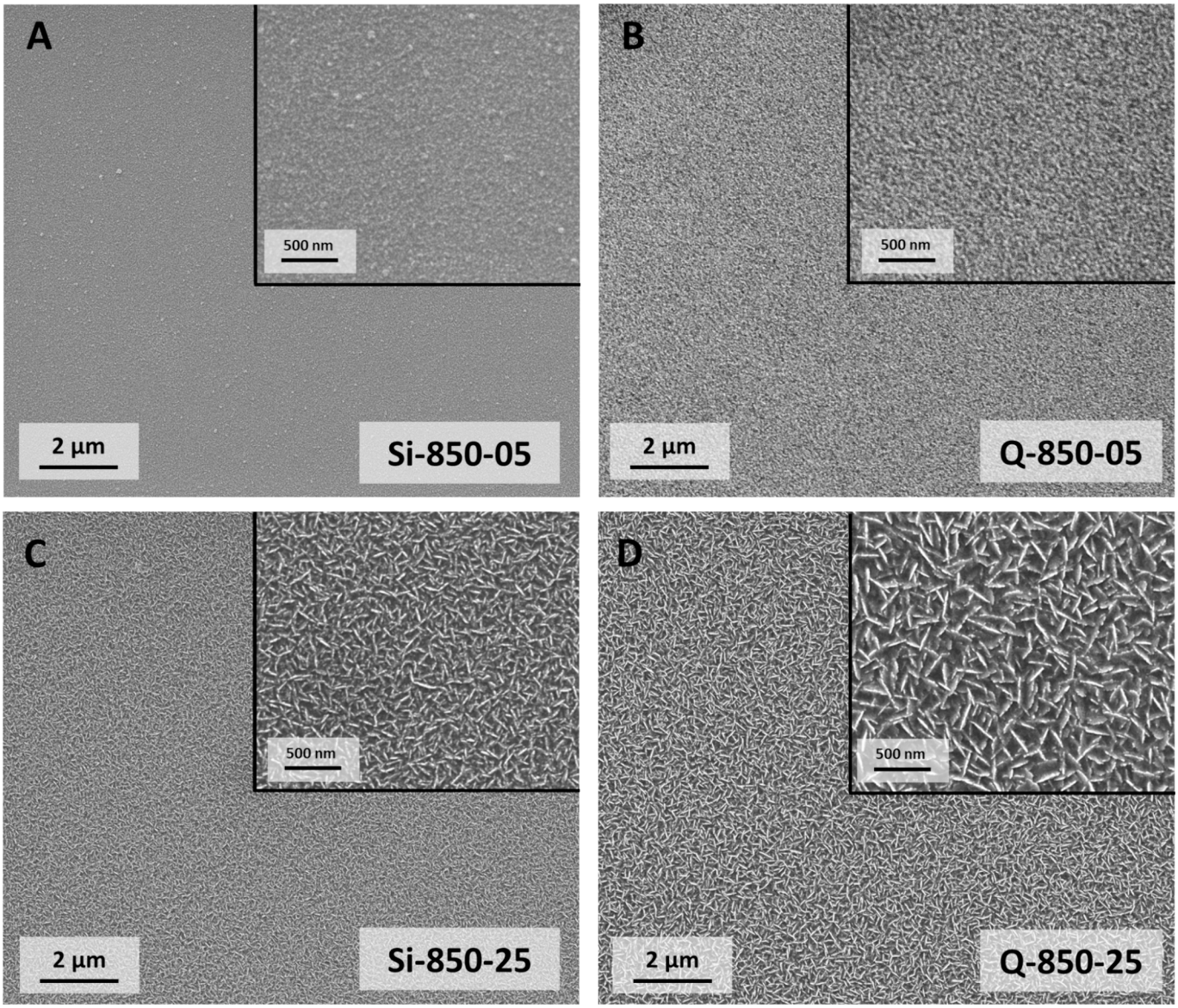

Fig. 2. SEM images show surface morphology for individual samples: **A)** Si-850-05, **B)** Q-850-05, **C)** Si-850-25, **D)** Q-850–25.

especially responsible for changes in electrical parameters like the current–voltage (I-V) characteristics or activation energy.

In the initial phase of B:DG shaping, an intermediate layer is formed between the substrate and the carbon walls. The process by which the intermediate layer forms and subsequently leads to the growth of carbon nanowalls was previously elucidated in [17]. The formation of such an intermediate layer is much more effective on fused silica glass substrates due to the amorphous character of the glass [47]. In contrast, due to its crystalline structure, silicon substrates alter the formation of the expected carbon structures, such as B:DG [48] and hamper the formation of vertical graphene walls. This can be observed in the SEM images shown in Fig. 2. Importantly, the vertical walls reduce the B:DG resistivity. This effect is caused by neutral impurity scattering [49]. Furthermore, diamond cauliflower structures formed in 5 min on the silicon substrate can be observed, which is in agreement with the literature [50,51]. Such structures then turn into wall-based structures via the mechanism described in the Jung-Min Cho et al. paper [52]. Nanowall formation is promoted by the presence of nitrogen in the plasma atmosphere described in our previous paper [36]. Synthesis duration is crucial for the electric properties of these layers due to the differences in morphology and molecular structure. The growth time adds a layer of complexity, as it directly contributes to the evolving morphology. As a result, this affects the charge transport paths, as well as the value of the activation energy, which is associated with the energy barrier for carriers to overcome during the conduction process. Additionally, the study conducted by M. Pierpaoli et al. [20] demonstrated that the optical properties of the material undergo corresponding changes as its electrical properties are modified.

Fig. 3 shows the results of ToF SIMS analysis performed on the samples Q-850-05 and Q-850-25. Considerable amounts of both elements B and C were found in the top layers of both samples. Sample Q-850-05 exhibited a boron concentration gradient, with higher levels (8×10^{19} atoms/cm^3) in the middle region that decreased (6×10^{17} atoms/cm^3) approaching the interface with the substrate. This interfacial zone is profoundly impacted by complex growth kinetics, making an abrupt transition challenging to achieve. Some mixing is inevitable at the interface, as evidenced by SEM, preventing a remarkably distinct demarcation of the boron gradient. This decrease in boron incorporation in the B:DG nanostructures towards the fused silica substrate is attributed to the initial stages of growth. Furthermore, boron diffuses into the fused silica substrates in both samples during the initial CVD nucleation phase [53], until a continuous carbon layer is formed to encapsulate and

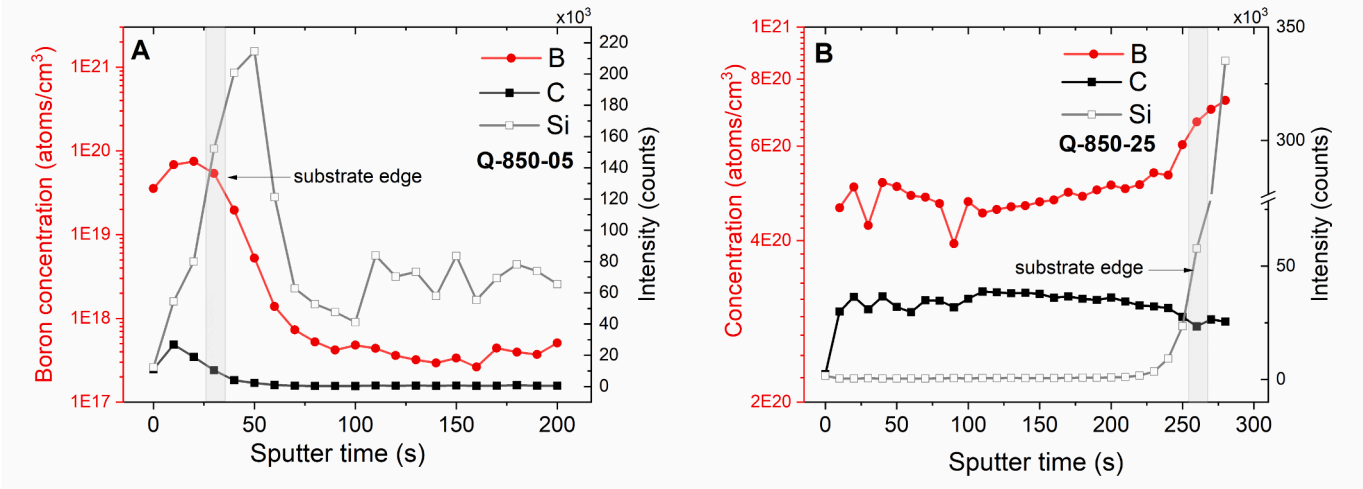

Fig. 3. SIMS in-depth profiles of boron and carbon recorded for samples: **A)** Q-850-05, **B)** Q-850-25.

protect the substrate surface. The oxygen enriched plasma atmosphere originated from fused silica substate exposed in that stage to atomic hydrogen suppress boron incorporation into solid phase as reported analogously for boron-doped diamond e.g. in [54,55].

The C and B profiles follow a similar trend in a short time sample Q-850-05, which is attributed to limited boron incorporation and surface development to cauliflower morphology. The edge of the substrate is identified as saturation levels of both B and C elements. Additionally, Si-O was identified at the interface of the film and substrate starting to increase at the marked substrate edge (not shown here). The sample Q-850-25 is characterised by almost one order of magnitude higher values and a more stable variation of boron profile through the depth, slightly rising towards the interface with the substrate. A sharper transition with an increase of Si-O is observed at the interface for that sample. The samples grown for 25 min exhibited enhanced conductivity compared to those grown for 5 min, along with reduced activation energies. These

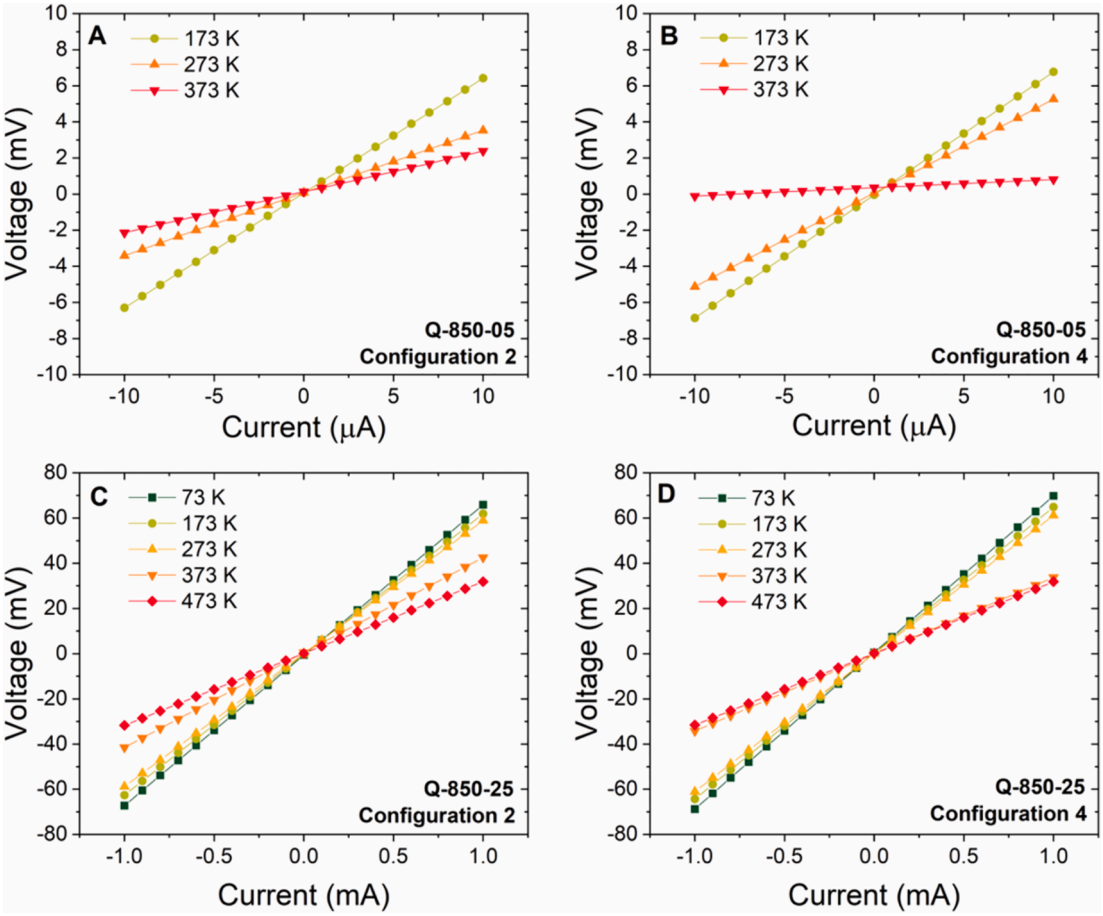

Fig. 4. Voltage-current characteristics as a function of temperature (ranging from −200 °C to 200 °C) for different measurement configurations: **A), B)** Q-850-05 and **C), D)** Q-850-25. (Attn.: 2 chosen configurations were selected in agreement with Fig. 1c.).

improvements can be attributed to two key factors: a higher concentration of boron and an even distribution throughout the depth of the material without interruption from the interface. In the case of the Q-850-05 sample, the carbon layer was thin enough to interfere with the interface of the substrate [56,57]. Carbon-silicon interface contains amorphous carbon, which exhibits lower electrical performance [58]. This synergistic combination contributes to higher charge carrier densities, thus facilitating improved conduction properties.

3.2. Studies of electrical properties of B:DG grown on fused silica plates

To evaluate the designed diagnostic system, a comprehensive study of the electrical properties of B:DG samples was conducted. Fig. 4 shows the voltage-current characteristics as a function of temperature for four measurement configurations.

At a given excitation current, the characteristics are linear and can be described according to Ohm's law. Increasing the temperature raises the conductivity of the structure. The resistivity of the films can be calculated according to the Equation (1):

$$\rho = \frac{\pi}{\ln(2)} \cdot \frac{\frac{R_1+R_2}{2} + \frac{R_3+R_4}{2}}{2} \cdot t \cdot f \tag{1}$$

where R is a linear approximation of the V-I curves for different configurations, t is the thickness, and f is the correction factor. The correction factor can be approximated as shown in Equation (2) [59]:

$$f = 1 - \frac{\ln 2}{2} \cdot \left(\frac{\frac{R_1+R_2}{2} - \frac{R_3+R_4}{2}}{\frac{R_1+R_2}{2} + \frac{R_3+R_4}{2}} \right)^2 - \left[\left(\frac{\ln 2}{2} \right)^2 - \frac{(\ln 2)^3}{12} \right] \cdot \left(\frac{\frac{R_1+R_2}{2} - \frac{R_3+R_4}{2}}{\frac{R_1+R_2}{2} + \frac{R_3+R_4}{2}} \right)^4 \tag{2}$$

The temperature-dependent resistivity of samples grown on fused silica glass plates exhibits behaviour characteristic of semiconductors, where an increase in material temperature leads to a decrease in resistivity, as illustrated by the V-I curves in Fig. 4.

Additionally, the duration of diamond-graphene structure deposition similarly influences resistivity, with samples subjected to longer growth periods displaying lower resistivity and enhanced stability. The estimated conductivity basing on derived from R values (see Figure S1) for the fabricated films as a function of temperature is shown in Fig. 5.

For both Q-850-05 and Q-850-25 samples, a metallic Ohmic conduction is inferred, as evidenced by a decrease in current with increasing temperature and a normalized conductance close to one, indicative of linear transport in the temperature range of −200 °C to 200 °C. A decrease in resistivity from 13.6 mΩ cm for Q-850-05 to 2.8 mΩ cm for Q-850-25 at room temperature is attributed to larger concentration of B atoms and the higher contribution of N atoms to the π states incorporated in graphenic lattice [60], which is confirmed by the increased carrier concentration observed as lower activation energy of Q-850-25. Moreover, the electrical behaviour of diamond/graphene films is highly responsive to surface morphology, which undergo significant changes during the initial stages of growth. Fig. 5A shows the relation of the natural logarithm of conductivity and the inverse of temperature for individual Q-850 series samples. The activation energy was calculated according to the Equation (3):

$$\sigma = \sigma_0 \exp\left(\frac{E_A}{kT}\right) \tag{3}$$

where σ is the conductivity, σ_0 is the pre-exponential factor, k is the Boltzmann constant, T is the temperature, and E_A is the activation energy. It should be noticed that the activation energy of samples fabricated using microwave plasma decreases gradually from 197 meV to 87 meV as the deposition time increases from 5 to 25 min. The lower activation energy of the longer deposited B:DG films indicates that lower energy is required to transfer charge from the impurity level to the conduction band, which would be helpful for carrier movement in heterostructures [60]. Accordingly, a change in the conductive activation energy was found to be associated with a change in the quality of the multiwall structure [61], which is observed in the SEM as a well-organized multiwall maze. Moreover, the decreasing activation energy with process time confirms that the oxidation process of B:DG samples grown on silica glass does not occur in this temperature range [47]. Comparing the results with other groups, Engstrøm et al. [62] reported the growth activation energy of 0.9 ± 0.4 eV for vertically aligned carbon nanotubes in the temperature range between 575°C and 800°C attributing it to the limited dissociation of C_2H_2 on the Fe catalyst. Chhowalla et al. [63] estimated 0.56 eV as the activation energy derived from the Arrhenius plot in the low-temperature range (520 ∘C–700 ∘C) of carbon nanotubes grown by PECVD from C_2H_2 by the catalytic action of Ni nanoparticles. In both cases, the processes were carried out from a C_2H_2 plasma, which even without plasma becomes unstable when reaching 400 ∘C, while methane (gas used in our experiments) totally dissociates when it reaches 1200°C in thermal processes. These study results in much lower activation energies of B:DG samples formed in microwave plasma H_2:CH_4 at 700 °C. Furthermore, no catalyst was applied to initiate vertical graphene walls formation. These facts suggest that applied plasma is highly stable and delivers high levels of CH_4 dissociations. Graphene heterostructures shown by Zhao et al. revealed frequency dependant activation energies of 0.22 eV and 0.24 eV most likely related to the two conduction mechanisms shown in the

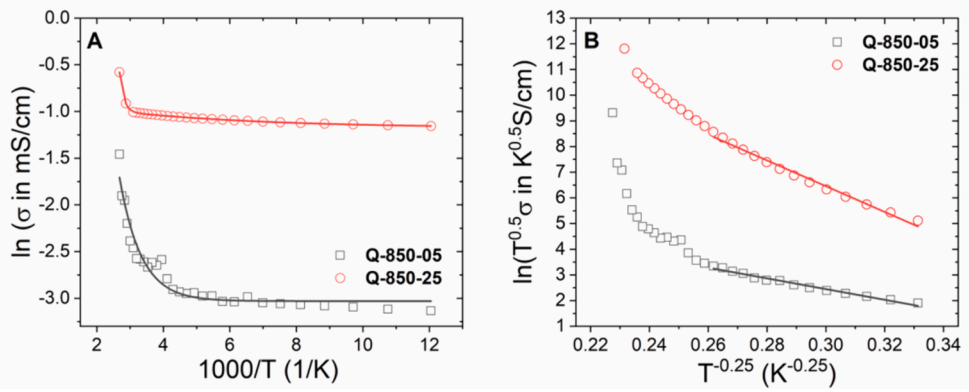

Fig. 5. The thermal = dependence of electrical properties of B:DG grown on fused silica plates – Q-850 series: **A)** Arrhenius plots describing the relation of the natural logarithm of conductivity and the inverse of temperature 1000/T [1/K] and **B)** Mott plot estimated as $\ln(T^{\frac{1}{2}}\sigma)$ as a function of $T^{-\frac{1}{4}}$. (Attn.: The electrical properties presented here correspond to the surface conductivity measured between the contacts, that is, an influence of in-plane and in-depth structural anisotropy on the current path is not taken into account.

equivalent circuit model with two RC in series [64]. For temperatures below −50 °C, the fabricated films exhibit a dominant variable range hopping (VRH), which follows the rule (4):

$$\sigma \propto \exp\left(-\left(\frac{T_0}{T}\right)^{\frac{1}{4}}\right) \quad (4)$$

where T_0 is a constant [65]. The variable-range hopping mechanism, which was developed by Mott [66], was used to explain the electrical conductivity as a function of temperature for disordered materials at low temperatures. This mechanism is governed by the carrier transport via hopping between localized states (Attn.: See the fitting in Fig. 5B). VRH are weakened for temperatures above –60 °C. When the temperature rises higher than 50°C, the VRH model is no longer suitable for Q-850-25, but rather thermal activation conduction is the main transport mechanism [65].

3.3. Electrical measurement of B:DG nanostructures fabricated on Si wafers

The resistance of B:DG nanostructures on conductive silicon wafers (Si-850 series) was measured in a two-wire mode utilising a sandwich configuration and is characterised by a relation typical for electric current-semiconducting materials. The voltage-current curves for Si-850 series samples are shown in Fig. 6.

The point plot corresponds to values obtained from measurements, while the lines are linear approximations used to estimate the resistance. Linear symmetric response characteristics are observed in both samples within the temperature range of −200 °C to 200 °C. Notably, the 25-minute samples exhibit slightly steeper slopes, leading to a drop of resistance. This lower resistance of Si-850-25 sample is ascribed to a higher thickness including also enhanced concentration of boron atoms and a more significant contribution of nitrogen atoms to the π states within the B:DG structure. It should be noticed that while going from −200 °C to 200 °C current was increased from ~100 μA to 500 μA and from ~80 μA to 700 μA for Si-850-05 and Si-850-25 respectively. This results in a considerable decrease in resistance. The observed lower resistances, corresponding to a decrease in temperature, can be ascribed to the immobilization of charge carriers or the hindered electron transport, which contribute to the conductance across the junction.

Fig. 7A presents Arrhenius plots that illustrate the correlation between the natural logarithm of conductance (ln(G[S])) and the inverse temperature (1000/T [1/K]) for the Si-850 series samples [67,68]. The analysis of these plots exhibits minor changes in conductance G with an increase in the duration of deposition on the samples. The Si-850-25 reveals higher conductance than Si-850-05 at temperatures over −50 °C, while the slightly reduced value in comparison to Si-850-05 were observed for lower temperatures. This effect could be attributed to more intense trapping and freezing electrons by various defects highly populated in thicker Si-850-25. In the low-temperature regime below 220 K, VRH conduction prevails, as evidenced by the pronounced slope of the Arrhenius plot beyond 220 K. This indicates the predominance of nearest-neighbour hopping (NNH) effects, with conductivity characterised by the relation $\sigma \propto \exp(-T_0/T)$. The influence of VRH diminishes in the temperature range from 200 K to 300 K, as delineated in Fig. 7A. Beyond 300 K, the applicability of the VRH model diminishes, transitioning to thermally activated (TA) conduction as the principal transport mechanism confirmed also in the Mott plot (see Fig. 7B). The TA conduction in regions exceeding 200 K is mathematically represented as $\sigma = \sigma_0 \exp(-E_a/2kT)$, where σ_0 is the pre-exponential factor, E_a is the activation energy, k is Boltzmann's constant, and T is the temperature [referenced from [65]].

The study notes a gradual reduction in the activation energy of Si-850 samples, synthesized in microwave plasma, from 0.1 to 0.137 meV as the deposition time decreases from 25 to 5 min. This effect might be explained by more intense trapping and freezing electrons by different defects highly populated in thicker and developed multi-wall diamond-graphene nanostructures of Si-850-25 [69]. In the B:DG films subjected to extended deposiption periods, a slightly higher activation energy signifies an elevated energy requirement for charge transfer from the impurity level to the conduction band. At elevated temperatures, our observations reveal a minor thermally activated modification in conductivity, indicating the presence of extended states. We assert that in these instances, the conductivity is predominantly governed by Mott variable range hopping [70] (see Fig. 7B). This implies that the density of localized electronic states near the Fermi level remains constant. The hopping mechanism involves tunnelling transitions between occupied and unoccupied localized states, with the energy difference between states being compensated by either the emission or absorption of a single phonon, as per Mott's model. Consequently, at high temperatures, conduction displays thermal activation, suggesting a quasi-metallic conduction. It is noteworthy that an inverse relationship exists between conductivity and activation energy: higher conductivity correlates with lower activation energy. In disordered materials, conduction often adheres to the Mott-type variable-range hopping (VRH) model.

Table 2 provides a comprehensive summary of the comparison of

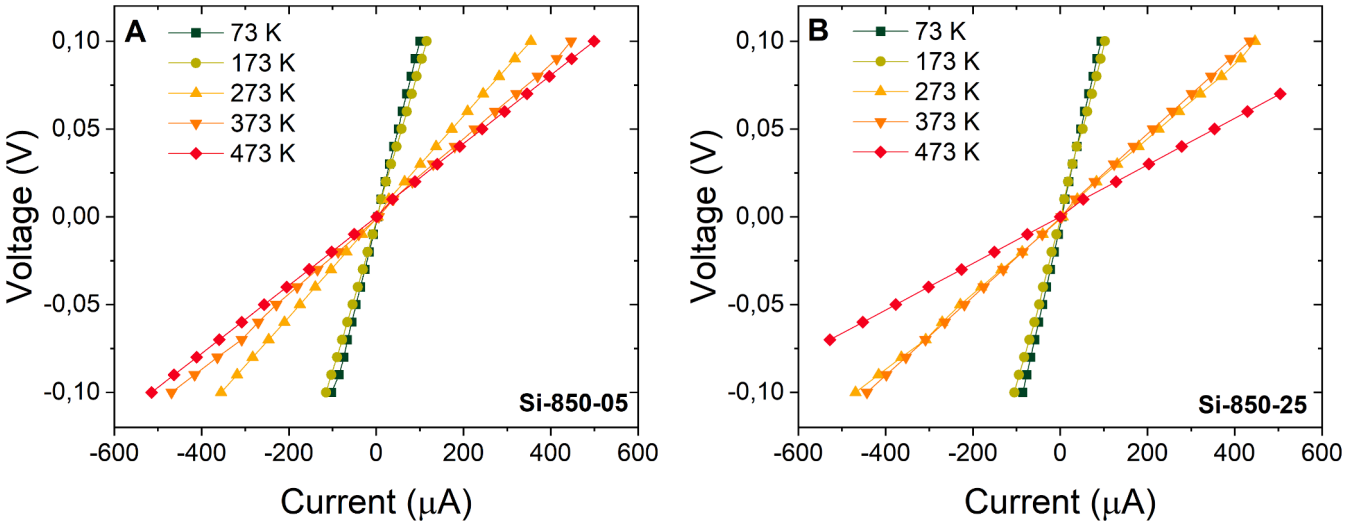

Fig. 6. Voltage-current characteristics as a function of temperature for B:DG samples grown on Si wafer substrates: A) Si-850-05 and B) Si-850-25 within a temperature range from −200 °C to 200 °C (Attn.: single selected configurations were selected in agreement with Fig. 1C).

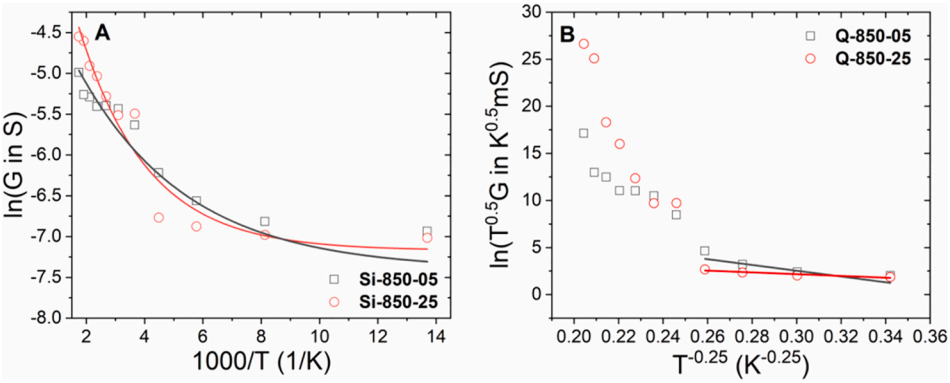

Fig. 7. Arrhenius plots describing the relation of the natural logarithm ln(*G*[S]) and the inverse of temperature 1000/*T* [1/K] for Si-850 series samples: **A)** Si-850-05 and **B)** Si-850-25.

Table 2
Comparison of activation energies acquired for various types of carbon nanowall heterostructures estimated by Arrhenius plots.

Structure	Activation energy / eV	Reference
VGN at Si	0.57	[71]
Graphene heterostructure	29 meV/cell (=0.81 meV/atom)	[72]
Graphene-pentacene at Si/SiO_2	0.3	[73]
BCNW at stainless steal	E_{low_Tact} = (1.09 ± 0.21) E_{high_Tact} = (0.58 ± 0.15)	[61]
n-type nanowalls Si/SiO_2	0.003–0.02	[74]
Semimetalic BCNW- Si/SiO_2	0.008–0.004	[75]
Nanowalls Si/SiO_2	0.02–0.003	[76]
Semimetalic BCNW −Si/SiO_2	0.006–0.03	[77]
Nanowalls Si/SiO_2	0.0015–0.009	[29]
B:DG at fused silica / B:DG at Si wafer	0.197–0.087 / 0.1–0.137	This work

activation energies derived from Arrhenius plots for a variety of carbon nanowall heterostructures. It offers a concise overview of the energy barriers associated with different nanowall configurations, shedding light on the thermodynamic characteristics of these structures.

Studied electrical performance observed by designed system in B:DG samples allows for considering the interactions at the graphene/diamond interfaces and carbon nanowall (CNW) surfaces. At elevated temperatures, the oxidation of graphene layers leads to an increase in their insulating properties, particularly at the CNW surfaces and the interfaces. Consequently, the CNW/diamond junction acts as a series resistor, encompassing a blend of resistive elements. These elements include the variable resistances offered by the CNWs and the CNW/diamond interfaces, in addition to the inherent resistance of the diamond material itself. It is noteworthy that the thermal oxidation of graphite predominantly occurs at the graphene edges and in-plane vacancies within the sample, a process that intensifies with rising temperatures. This observation aligns with prior research findings [61,62,78]. Furthermore, the analysis of the presented data reveals that the B:DG samples exhibit a complex electrical behaviour. The electrical conductivity in these materials is influenced by both electrons and holes, which are introduced through hetero-doping with boron and other atoms. This behaviour is analogous to that observed in bulk reduced graphene oxide (rGO) and graphene oxide (GO), as manifested in [79,80], where conductivity analysis (ln(σ) plotted against various inverse temperature powers) indicated the predominance of Variable Range Hopping (VRH). Similar effects were also noted in the a-C:H matrix, where enhanced conductivity was attributed to the formation of πC=N, σC–N, and σ*C=N bonds, contributing to free electron generation [70]. The thermally induced conduction mechanism observed in B:DG samples aligns with findings by Liu et al [81], who reported that boron/nitrogen co-doped samples grown in microwave plasma exhibited B–O defects (B_3O and B_4O) formed during diamond crystallization. These defects provide a pathway to create n-type diamond semiconductors.

The exploration and understanding of tailored charge transport in complex graphene/diamond and nanocarbon structures are crucial in the realm of material physics, especially for device applications. By analysing the temperature-dependent resistivity, two distinct solid-state classes can be discerned: i) a transition from metal to semiconductor behaviour, and ii) a deviation in semi-metallic character [82]. Charge carrier localization, as a disorder-induced transition, is a phenomenon that may occur in nanocarbon materials with significantly disrupted lattice structures, such as defected graphene. This disorder can localize electronic states at the Fermi energy, potentially leading to insulating performance.

4. Conclusions

In conclusion, this study provided a detailed examination of the electrical properties of B:DG nanostructures, with a focus on the impact of substrate type and deposition duration. High-resolution SEM was utilised to analyse the surface morphology of samples prepared on quartz and silicon substrates. The SEM images revealed that nanowall structures formed more effectively on quartz glass plates, which is attributed to the amorphous nature of the substrate, facilitating unrestricted growth.

The research underscored the importance of growth duration in the development of these nanostructures. Shorter growth periods resulted in less developed structures, while longer durations led to the formation of distinct nanowall structures. This correlation between growth time and morphological development of the nanostructures was a key finding. Significant differences in the electrical properties of the samples were observed, influenced by both the substrate and growth duration. Longer deposition processes resulted in lower resistivity values for both silicon wafer and fused silica plate samples. However, samples grown on silicon wafers exhibited higher resistivity values than those on fused silica plates. The surface morphology of the samples played a significant role, closely linked to the parameters of B:DG structure growth and the properties of the substrates. These variations were particularly evident in the current–voltage characteristics and activation energy of the nanostructures. The study identified a transition in the transport mechanisms within the B:DG samples, shifting from variable range hopping (VRH) at lower temperatures to thermally activated (TA) conduction at higher temperatures. This connection led to higher resistivity values for samples with shorter deposition times. By conducting a thorough analysis of the observable variations in I-V characteristics and activation energy, we can gain a deeper understanding of the underlying conduction mechanisms and potentially explore innovative applications across various fields.

Overall, this study provided valuable insights into the factors

influencing the formation and electronic properties of B:DG nanostructures. The findings highlighted the crucial role of substrate selection and process duration in the synthesis of these materials and contributed to a deeper understanding of their potential applications in the field of electronic device engineering.

CRediT authorship contribution statement

Michał Rycewicz: Data curation, Investigation, Software, Visualization, Writing – original draft, Writing – review & editing. **Mariusz Banasiak:** Data curation, Investigation, Methodology. **Mateusz Ficek:** Conceptualization, Formal analysis, Investigation, Methodology, Writing – original draft. **Stephan Kubowicz:** Investigation, Writing – original draft. **Simona Baluchová:** Data curation, Investigation. **Bogusława Sobczak:** Data curation, Investigation. **Elizaveta Vereshchagina:** Investigation, Project administration, Supervision. **Robert Bogdanowicz:** Conceptualization, Funding acquisition, Project administration, Resources, Supervision, Visualization, Writing – original draft, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

All data analyzed during the study are included in this article and will be made upon reasonable request.

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Appendix A. Supplementary material

Supplementary data to this article can be found online at https://doi.org/10.1016/j.measurement.2024.115290.

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