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A 120.9-dB DR Digital-Input Capacitively Coupled Chopper Class-D Audio Amplifier

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***Abstract*— This article presents a digital-input class-D amplifier (CDA) achieving high dynamic range (DR) by employing a chopped capacitive feedback network and a capacitive digital-to-analog converter (DAC). Compared with conventional resistive-feedback CDAs driven by resistive or current-steering DACs, the proposed architecture eliminates the noise from the DAC and feedback resistors. Intermodulation between the chopping, pulsewidth modulation (PWM), and DAC sampling frequency is analyzed to avoid negative impacts on the DR and linearity. Real-time dynamic element matching (RTDEM) is employed to address distortion due to mismatch in the DAC, while its intersymbol interference (ISI) is eliminated by deadbanding. The prototype, implemented in a 180-nm bipolar, CMOS, and DMOS (BCD) process, achieves 120.9 dB of DR and a peak total harmonic distortion plus noise (THD+N) of −111.2 dB. It can drive a maximum of 15/26 W into an 8-/4-Ω load with a peak efficiency of 90%/86%.**

***Index Terms*— Capacitively coupled chopper amplifier (CCCA), class-D amplifier (CDA), digital-to-analog converter, dynamic element matching (DEM), intersymbol interference (ISI).**

I. Introduction

CLASS-D amplifiers (CDAs) have become increasingly popular in audio applications due to their high efficiency, which is enabled by their switching output stage [1]. Due to the digital format of most modern audio sources, digital-input CDAs are preferred to their analog counterparts. Their monolithic integration reduces system size and cost, and their input is much more robust to interference than an analog-input CDA [2]. However, while the dynamic range (DR) and total harmonic distortion plus noise (THD+N) performance of analog-input CDAs have been significantly improved recently [3], [4], [5], [6], [7], [8], [9], [10], less progress in these respects has been made for monolithic digital-input CDAs, whose THD+N remains above −100 dB and DR limited to about 115 dB [11], [12], [13], [14].

A digital-input CDA can be implemented in a straightforward fashion with an open-loop architecture [15], which features a mostly digital implementation, as shown in Fig. 1(a). The input is processed by a digital signal processing block to derive the CDA's discrete output waveform, using delta–sigma modulation and/or pulsewidth modulation (PWM). However, this architecture suffers from distortion produced by the output stage and high sensitivity to clock jitter and supply noise. Although feasible, achieving a DR of 120 dB requires a clock jitter below 2 ps due to the rail-to-rail transitions [16]. In [13], 8× better jitter immunity is achieved by reducing the supply by the same factor for small input signals. However, this requires an extra dc–dc converter, which adds extra external components and degrades the overall power efficiency.

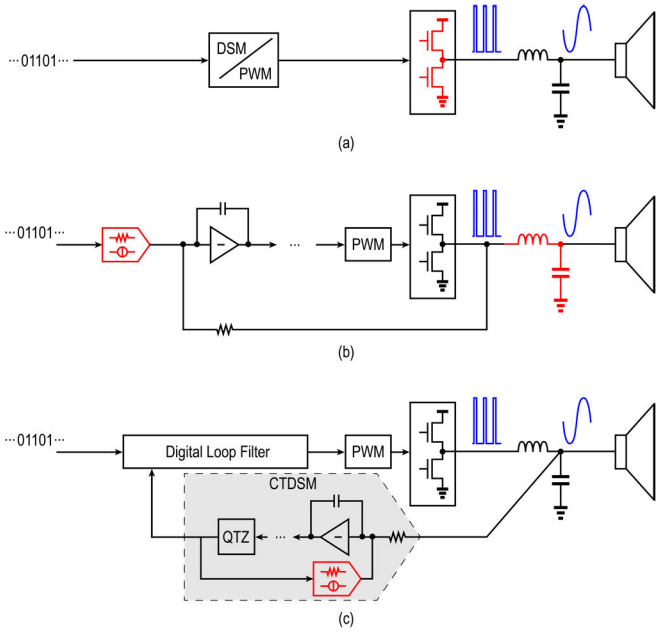

Fig. 1. Conventional digital-input CDA architectures. (a) Open-loop, (b) closed-loop with analog loop filter, and (c) closed-loop with digital loop filter. Dominant sources of noise and distortion are highlighted in red.

To address the limitations of open-loop CDAs, feedback is typically applied around the output stage. For a digital-input CDA, closing the loop requires an analog/digital interface, which is conventionally achieved by a digital-to-analog converter (DAC) placed upfront, as shown in Fig. 1(b) [12], [14], [17]. With the noise and distortion of the output stage suppressed by the loop gain, the output *LC* filter then becomes a dominant source of distortion [18]. The resistive or current-steering DAC also introduces noise and distortion, which limits the overall DR to about 115 dB.

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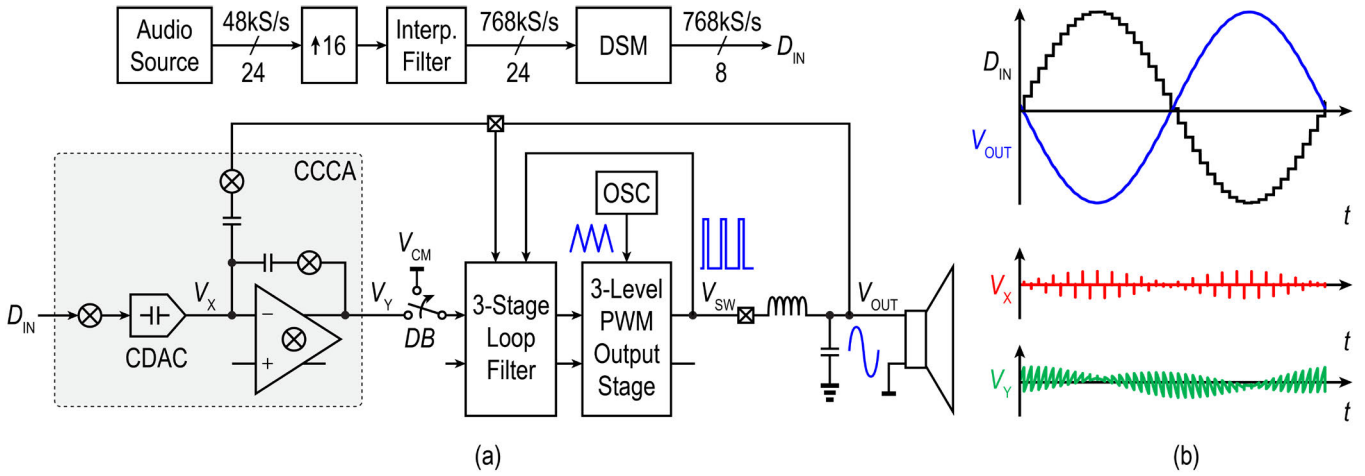

Fig. 2. (a) Architecture of the proposed capacitively coupled digital-input CDA and (b) waveform at key nodes for a sinusoidal input.

Alternatively, an analog-to-digital converter (ADC) can be employed to sense the CDA's output, and the loop can then be closed by a digital loop filter that drives the output stage, as shown in Fig. 1(c) [11]. In [11], feedback is taken from the speaker terminals, thus suppressing *LC*-filter nonlinearity, and a 50-dB loop gain is implemented by a fifth-order loop filter. Although a 1-bit finite-impulse response (FIR) DAC with a dual return-to-zero (RZ) switching scheme is employed in the feedback $\Delta\Sigma$ ADC's IDAC, to eliminate mismatch and intersymbol interference (ISI) errors and to improve its jitter immunity, its DR and THD+N are still limited by the IDAC's noise to about 115 and −90 dB, respectively.

In all the abovementioned closed-loop architectures, the CDA output is sensed using resistors, which necessitates the use of an IDAC or RDAC in the analog/digital interface, which introduces thermal and $1/f$ noise. Furthermore, since their analog loop filter or feedback ADC is typically implemented in a low-voltage (LV) domain, a resistive divider [12] or common mode regulation loop [11] is required to protect the LV circuitry from the high-voltage (HV) CDA output, which adds more noise. Reducing noise by increasing the DAC's output current would not only increase power consumption but also require larger integration capacitors in the loop filter. To overcome these limitations, a capacitively coupled chopper CDA is introduced in [10], which eliminates the noise contribution from the resistive feedback network. In addition, the use of chopping largely eliminates the $1/f$ noise from the loop filter, and its feedback-after-*LC* structure suppresses the *LC* filter's distortion. However, it requires an analog input, fed in through a switched-capacitor network, which is not trivial to drive while maintaining high linearity.

In this article, a digital-input CDA based on the capacitively coupled chopper amplifier (CCCA) topology is presented, which achieves a DR of 120.9 dB and a THD+N of −111.2 dB. Several challenges must be overcome to achieve such performance. The capacitive DAC (CDAC), which replaces the chopped capacitor input network in [10], could introduce distortion due to mismatch and ISI. Although similar CDAC structures have been employed in ADCs recently [19], [20], [21], [22], [23], their DR is much lower than that required in this work. Furthermore, the high-frequency components present in the DAC output can cause intermodulation distortion due to the use of chopping and PWM in the system.

This article, which is an extension of [24], is organized as follows. Section II provides an overview of the proposed digital-input capacitively coupled CDA and discusses its design considerations. Section III discusses techniques to mitigate DAC mismatch and ISI. Section IV presents the circuit implementation of the closed-loop CDA, followed by measurement results in Section V. This article ends with conclusion.

II. Digital-Input Capacitively Coupled Chopper CDA

A. Overview

Fig. 2(a) presents an overview of the proposed digital-input capacitively coupled CDA. The digital input is up-sampled to $f_S = 768$ kHz and truncated to 8 bit by a digital delta–sigma modulator (DSM). The DSM output (D_{IN}) then drives a CDAC, which feeds into the virtual ground of a capacitively coupled chopper CDA. The CDA employs a 14.4-V multilevel PWM-based output stage and has a closed-loop gain of 8 [10]. Its front end consists of a preamplifier, implemented as a CCCA, which amplifies the error signal ($V_{ERR} = D_{IN}V_{REF} - V_{OUT}/8$), thus suppressing the noise from the subsequent loop filter. However, due to the preamplifier's finite-slew rate, chopping and DAC transitions cause nonlinear transients at the CCCA's output. Thus, a 20-ns deadband is introduced to block them from the loop filter [10]. Driving the capacitively coupled CDA by a CDAC presents several additional challenges. The CDA's internal swing is increased by the presence of high-frequency components in the DAC output waveform. In addition, distortion can arise due to DAC mismatch, ISI, and the intermodulation between chopping, DAC, and PWM operations. These issues will be discussed in detail in the following sections.

B. DAC Sampling Frequency

In this work, a non-RZ (NRZ) DAC is chosen for its high immunity to clock jitter. In contrast to the analog input of

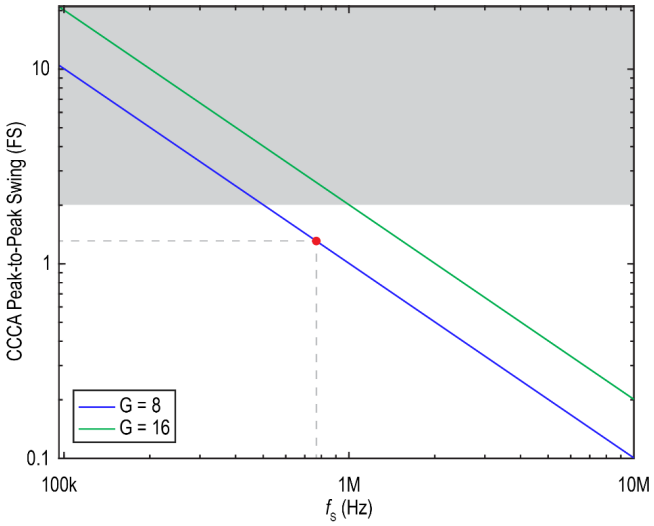

Fig. 3. Peak-to-peak swing of the DAC image for different choices of f_S and CCCA gain.

the CDA in [10], the DAC output contains high-frequency components, including out-of-band quantization noise and DAC image, which increase the preamplifier's output swing. While quantization noise can be reduced by increasing the DAC resolution, the DAC image will still be amplified by the loop filter's preamplifier, leading to a sawtooth-like waveform at its output V_Y, as illustrated in Fig. 2(b). To maintain high linearity, the DAC image should not exceed the linear output range of the CCCA.

For a full-scale sinewave signal $u(t) = \sin(2\pi f_{IN} t)$, the peak swing of the DAC image (before being amplified by the CCCA) can be approximated by

$$V_{IMAGE,PP} \approx \max\left|\frac{du}{dt}\right| \cdot \frac{1}{f_S} = \frac{2\pi f_{IN}}{f_S} \leq \frac{\pi}{OSR}. \quad (1)$$

Hence, it can be reduced by increasing the DAC's sampling frequency f_S. Fig. 3 shows the preamplifier's output swing, normalized to its 1.8-V supply, for different choices of f_S under a worst case 20-kHz full-scale input, assuming infinite DAC resolution. To ensure enough suppression for the loop filter noise, a gain of G of about 8 is required for the preamplifier. While $G = 16$ as in [10] is also possible, it would require a higher f_S and thus a higher clock frequency for the dynamic element matching (DEM) logic (Section III-B).

C. DAC Resolution

Besides the DAC image, shaped quantization noise also consumes some of the preamplifier's output swing, which is a function of the DAC resolution and the out-of-band gain (OBG) of the DSM's noise transfer function (NTF) [25]. By choosing a relatively low OBG, a peak-to-peak quantization noise swing of 2 LSB can be achieved. Therefore, the extra swing due to quantization noise is given by $G/2^{N_{DAC}-1}$ LSB, where N_{DAC} is the DAC's resolution in bits. According to behavioral simulations, the shaped quantization noise can fit into the remaining output swing of the preamplifier as long as the DAC's resolution is more than 6 bits.

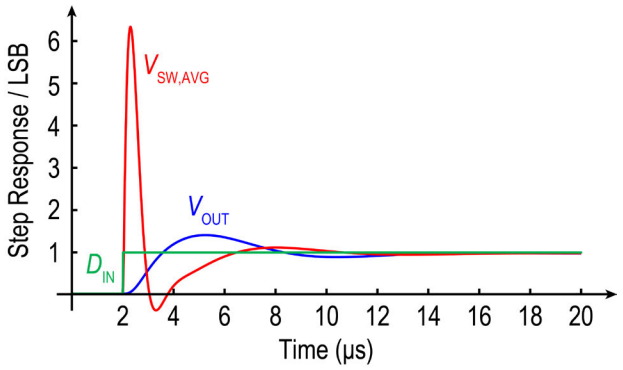

Fig. 4. Simulated step response from the input (D_{IN}) to the LC filter input ($V_{SW,AVG}$) and output (V_{OUT}).

However, the DAC's resolution also impacts the linear output range of the overall CDA due to the following. The capacitively coupled CDA employs feedback after the LC filter to suppress the latter's nonlinearity as well as the rail-to-rail switching edges produced by the output stage, which would, otherwise, saturate the preamplifier. To suppress the LC filter nonlinearity by about 50 dB, a feedback loop with a unity gain frequency of about 500 kHz is employed around the LC filter [9], whose cutoff frequency is about 88 kHz ($L = 3.3\ \mu$H and $C = 1\ \mu$F). Fig. 4 shows the simulated waveform after a DAC input step. For clarity, the PWM output stage is replaced with a linear model [26]. As shown, the LC filter output follows the DAC input step with a rise time of about 2 μs, requiring an overshoot at the LC filter's input ($V_{SW,AVG}$) that is about six times ($\approx 500 \div 88$) larger, thus consuming part of the output stage's signal range. Since the DAC input can change by up to 2 LSBs at once, keeping this loss within 0.5 dB ($\approx$5.6% FS) means that the DAC's LSB size must be less than

$$\underbrace{5.6\%\text{FS}}_{-0.5\text{dBFS}} \div [\underbrace{2}_{\substack{2\text{ LSB}\\ \text{input step}}} \times \underbrace{(500 \div 88)}_{\substack{\text{overshoot at}\\ \text{LC filter input}}}] = 0.49\%\text{FS}. \quad (2)$$

Therefore, $N_{DAC} = 8$ bit is chosen.

D. Intermodulation

Chopping demodulates DAC high-frequency components at even multiples of the chopping frequency f_{CH}, which can significantly degrade the SNR [19], [20], [27], [28]. In this work, the DAC spectral nulls at multiples of f_S are exploited to mitigate such folding [19], and therefore, $f_{CH} = f_S/2 =$ 384 kHz is adopted. This also allows the chopping and DAC transitions to coincide, allowing a simple way to eliminate nonlinear transients due to chopping and DAC settling, which will be explained in detail in Section III. Chopping also demodulates the PWM sidebands and thus degrades the THD. As explained in [10] and [29], this can be avoided by setting f_{PWM} to an odd harmonic of f_{CH}. A factor of 13 is chosen in this work, implying an f_{PWM} of 4.992 MHz.

Given $f_{PWM} = 6.5 f_S$, the DAC's-shaped quantization noise in the sixth Nyquist zone is present around f_{PWM}. The PWM operation could then potentially demodulate this noise to the baseband. Fortunately, this intermodulation is introduced at the output of the loop filter and is thus suppressed by the loop

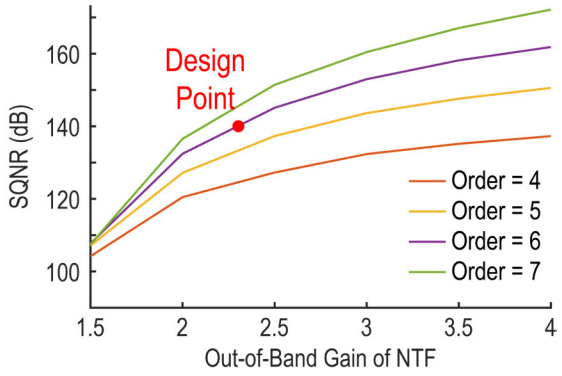

Fig. 5. SQNR as a function of the NTF's OBG for an 8-bit DSM with an OSR of 19.2.

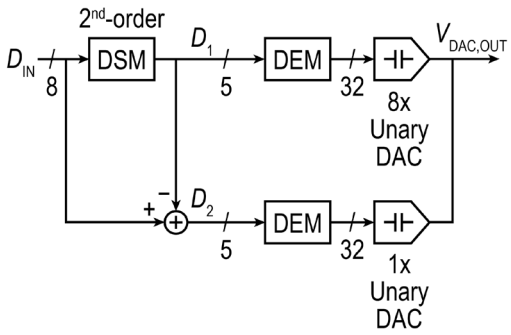

Fig. 6. 2nd-order NS segmentation scheme is employed in this work.

gain, which is above 80 dB [9]. Hence, the impact on SNR is negligible.

III. DAC Implementation

A. Delta–Sigma Modulator

The digital DSM is designed using the Schreier Toolbox [30]. The requirement is to achieve sufficient signal-to-quantization-noise ratio (SQNR) while restricting the maximum input step to 2 LSB. Simulations show that, given the abovementioned choice of $f_S = 768$ kHz and $N_{DAC} = 8$ bit, an NTF of sixth order or higher is required. In this work, a sixth-order modulator is used, which has an OBG of 2.4, as shown in Fig. 5. A higher order NTF with a lower OBG could also have been used. To ensure the absence of idle tones, its quantizer is dithered using a linear-feedback shift register (LFSR)-based pseudorandom generator, at the expense of 3 dB lower SQNR. The resulting SQNR is 133 dB.

B. Dynamic Element Matching

Unit-element mismatch in the 8-bit CDAC causes significant distortion and quantization noise fold-back, so it must be addressed using DEM. Conventional DEM techniques, such as data-weighted averaging (DWA), are based on unary DAC elements, leading to high digital complexity given the 8-bit DAC resolution. While the segmented tree DEM [21], [22], [31], [32] simplifies the logic, it still offers only 1st-order shaping, introducing significant in-band mismatch noise and degrading the DR. In [23], this limited the DR to below 95 dB at an OSR of 40. In comparison, this work targets 120-dB DR with an OSR of only 19.2. Therefore, 1st-order mismatch shaping is insufficient for this work,[1] and the real-time DEM (RTDEM) technique [33], [34] is employed instead, since it averages out mismatch errors within each sample period. However, conventional RTDEM is also based on unary elements, which would require high logic complexity and a clock frequency of about 200 MHz ($\approx 2^8 \times f_S$).

1) Noise-Shaped Segmentation: To reduce the complexity and clock frequency of the RTDEM logic, noise-shaped (NS) segmentation is employed [14], [34], [35], [36]. As shown in Fig. 6, the 8-bit DAC input D_{IN} is processed by a second digital DSM to yield a 5-bit word (D_1) that controls an MSB DAC segment. The quantization noise introduced in D_1 is canceled by an LSB DAC segment driven by $D_2 = D_{IN} - D_1$. The total DAC output is given by

$$\begin{aligned} V_{DAC,OUT}(z) &= G_1 D_1(z) + G_2 D_2(z) \\ &= G_1[D_{IN}(z) - D_2(z)] + G_2 D_2(z) \\ &= \underbrace{G_1 D_{IN}(z)}_{\text{ideal output}} + \underbrace{(G_2 - G_1)}_{\Delta G} \cdot \underbrace{D_2(z)}_{-Q_{SEG}(z)\text{NTF}_{SEG}(z)} \end{aligned} \tag{3}$$

where G_1 and G_2 are the normalized gains from D_1 and D_2 to the DAC output, respectively, ΔG is the gain mismatch between the 8× and 1× DACs, Q_{SEG} is the unshaped quantization noise of the DSM in Fig. 6, and $\text{NTF}_{SEG}(z)$ is its NTF.

In [14], [34], and [35], 1st-order NS segmentation is employed. However, the 1st-order DSM exhibits "frequency-modulated idle tones" [37], causing D_2 to include harmonics of the input, which will degrade the output spectrum. To mitigate this effect, 2nd-order NS segmentation [38] is employed in this work, since it is less prone to tonal behavior. The 2nd-order $\text{NTF}_{SEG}(z)$ also reduces the in-band power of D_2, and hence, its contribution to $V_{DAC,OUT}$, by about 20 dB. Since the 2nd-order NTF produces more out-of-band power than a 1st-order NTF, D_2 spans 32 LSBs, thus requiring a 5-bit LSB DAC.

2) Real-Time DEM: The mismatch error within each DAC segment is addressed using RTDEM [33], which avoids the idle tone issue and SNR degradation of DWA. Fig. 7(a) shows the element selection pattern of RTDEM. The operation of a 3-bit DAC is illustrated for simplicity. In general, for a DAC with N_E unit elements, each sample period is evenly divided into N_E sub-intervals, defined by a high-frequency master clock MCLK. Then, a thermometer code corresponding to the input is rotated at the MCLK frequency. Therefore, a full rotation is completed in a sample period, and each element is turned on for an equal amount of time.

As shown in Fig. 7(b), if the input is chopped, the number of elements switching between two samples can be quite large, and the total number of rising and falling edges will be signal-dependent, causing nonlinear ISI [34]. To illustrate this, Fig. 8 shows the simulated output spectra of the MSB DAC for the cases, where a unit element's rising edge or falling edge adds

[1]MATLAB simulations show that the residual mismatch noise is still enough to degrade the target DR even if f_S is as high as 10 MHz.

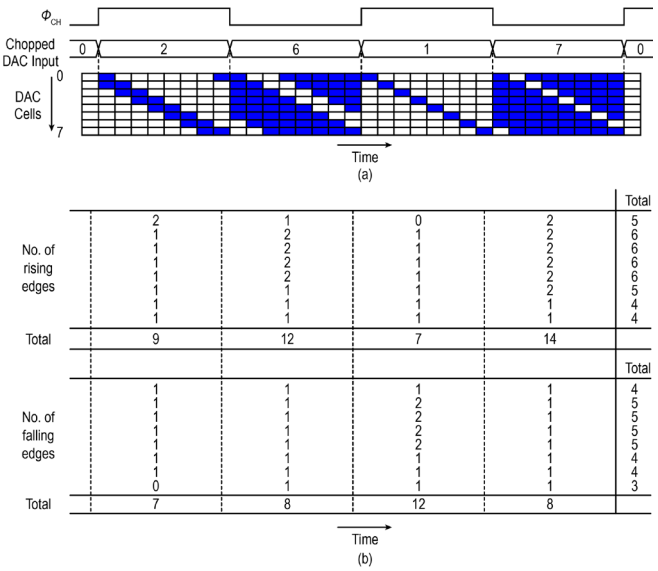

Fig. 7. (a) Usage pattern of unit elements with RTDEM (3-bit example) and (b) number of rising and falling edges.

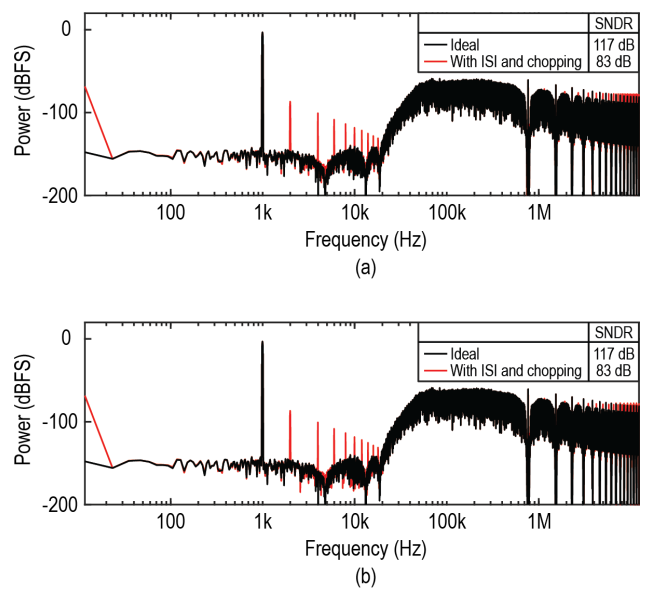

Fig. 8. Simulated MSB DAC spectrum of a chopped DAC with RTDEM assuming 1% ISI error on (a) rising edges and (b) falling edges.

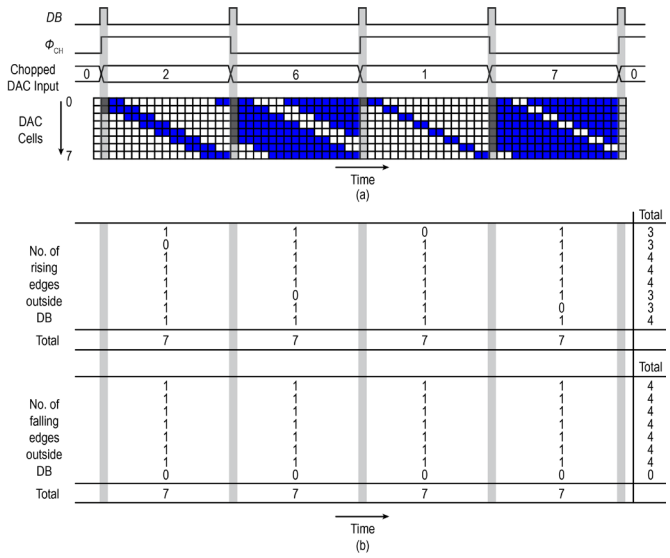

Fig. 9. (a) RTDEM with deadband employed in this work (3-bit example) and (b) number of rising and falling edges outside the deadband.

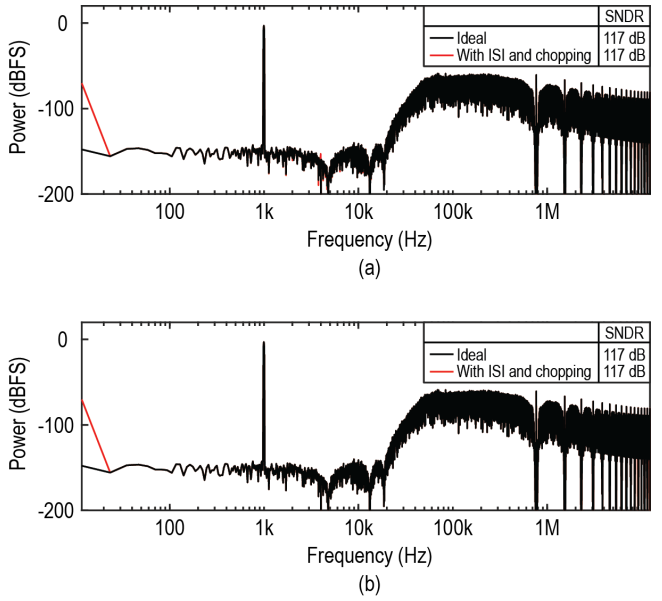

Fig. 10. Simulated MSB DAC output spectrum with ISI on (a) rising edges and (b) falling edges, with the deadband, where the ISI error of each element follows a normal distribution with a mean of 1% and a standard deviation of 0.006%.

a 1% ISI error to its output in the subsequent sub-interval. The ISI clearly causes extra harmonics of the input signal.

In this work, the dead-band switch at the preamplifier's output can also be used to mitigate this source of distortion, since the DAC and the choppers can be configured to switch at the same time. As shown in Fig. 9(a), the deadband is introduced as an additional MCLK cycle at the beginning of each DAC sample, when the states of the unit elements are updated based on the new input code. Given the DAC and preamplifier's settling speed, a 20-ns deadband is sufficient, leading to an MCLK of ~50 MHz, which is ~65 f_S. Therefore, the unit-element inputs are rotated every other MCLK cycle. In the two MCLK cycles after the deadband, the state of the unit elements is not changed. This ensures that they are all still equally used outside the deadband.

With this approach, although the number of rising edges of each unit element outside the deadband still varies with the input, the total number of transitions in each direction becomes signal independent, as shown in Fig. 9(b). Therefore, the ISI distortion is only limited by the mismatch between the unit elements. According to transistor-level Monte-Carlo simulations, the ISI mismatch is $\pm 0.006\%$ (1σ) with respect to the unit element's output in one MCLK cycle. Therefore, the ISI distortion is reduced significantly, as shown in Fig. 10.

Although RTDEM turns on each unit element for an equal amount of time, their mismatch still leads to some residual errors. This is because each unit element is driven by phase-shifted PWM signals that have the same dc value but different spectra. This spectral distortion is inherent to the

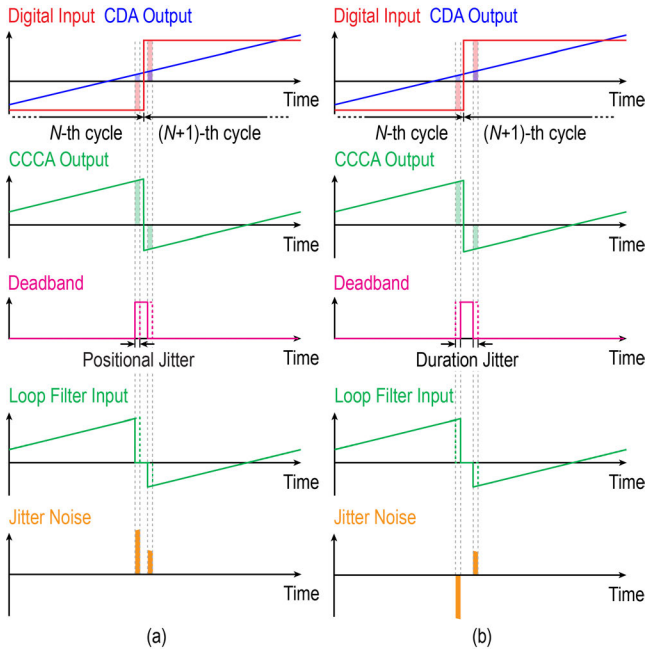

Fig. 11. Impact of (a) positional and (b) width jitter on the proposed DAC with deadband. Dashed lines represent the waveform affected by the jitter.

pulse-code modulation (PCM)-to-PWM operation [33], and its magnitude scales with input amplitude and increases with input frequency. In this work, it is about −72 dBc for a −1 dBFS input at 6 kHz. If the DAC had no mismatch and the timing was perfect, these distortion spectra cancel each other out, resulting in the spectrum of a perfect NRZ pulse. In practice, mismatch and timing errors cause a small portion of this distortion to appear in the output.

C. Clock Jitter

The introduction of a deadband as shown in Fig. 9, effectively converts the DAC output into an RZ waveform, thus increasing its jitter sensitivity. However, this is mitigated by the fact that the deadband is applied to the loop filter's error signal rather than to the full DAC output. This section discusses the impact of clock jitter on this work.

The noise due to the clock jitter can be decomposed into two components that are due to: 1) the jitter of the dead-band's position and 2) the jitter of the deadband's duration. The former is determined by the MCLK's absolute jitter, while the latter is determined by its period jitter. Note that the deadband acts on the CCCA output. Therefore, noise introduced by both types of jitter is divided by the CCCA gain of 8 when referred to the input.

Since the CCCA output is the amplified difference between the digital input and CDA output, the effect of positional jitter can be analyzed separately and then evaluated using superposition. As shown in Fig. 11(a), the impact on the digital input is much more than that on the CDA output due to the former's step change. When the deadband is delayed by jitter, the output sees the previous sample longer and the next sample shorter. This introduces a noise at the DAC output given by

$$v_{n,\mathrm{DAC},pj}[n] = V_{\mathrm{REF}}(D_{\mathrm{IN}}[n+1] - D_{\mathrm{IN}}[n])t_{pj}[n] \quad (4)$$

where $t_{pj}[n]$ is the positional jitter of the deadband after the nth DAC sample. This is the same expression as that for a conventional NRZ DAC. MATLAB simulation predicts an SNR of 131.5 dB for 100 ps of positional jitter.

The positional jitter also affects when the loop filter sees the CDA output. This introduces a noise component given by

$$\begin{aligned} v_{n,\mathrm{OUT},pj}[n] &= [V_{\mathrm{OUT}}(nT_{\mathrm{S}}) - V_{\mathrm{OUT}}(nT_{\mathrm{S}} + T_{\mathrm{MCLK}})]\frac{t_{pj}[n]}{T_{\mathrm{S}}} \\ &\approx -\frac{dV_{\mathrm{OUT}}(nT_{\mathrm{S}})}{dt} \cdot \frac{T_{\mathrm{MCLK}}}{T_{\mathrm{S}}} \cdot t_{pj}[n] \end{aligned} \quad (5)$$

where $T_{\mathrm{S}} = 1/f_{\mathrm{S}}$ and T_{MCLK} is the period of MCLK and also the duration of the deadband. Approximating the CDA output by a sine wave, the SNR due to this noise is given by

$$\begin{aligned} &10\log_{10}\left(\frac{\overline{V_{\mathrm{OUT}}^2(nT_{\mathrm{S}})}}{v_{n,\mathrm{OUT},pj}^2[n]} \cdot \frac{1}{\mathrm{OSR}}\right) \\ &= 10\log_{10}\left[\frac{1}{(2\pi f_{\mathrm{IN}})^2 \cdot \left(\frac{T_{\mathrm{MCLK}}}{T_{\mathrm{S}}}\right)^2 \cdot \sigma_{pj}^2 \cdot \mathrm{OSR}}\right]. \end{aligned} \quad (6)$$

In this work, $T_{\mathrm{MCLK}}/T_{\mathrm{S}} = 1/65$ and OSR = 19.2. Therefore, for $f_{\mathrm{IN}} = 20$ kHz and $\sigma_{pj} = 100$ ps, the SNR is 147 dB, so this source of noise is negligible.

Duration jitter, on the other hand, is more easily analyzed with the CCCA output waveform. As shown in Fig. 11(b), if the deadband is wider, error pulses are added to the CCCA output both before and after the deadband. Since the CDA output straddles the DAC input, the two error pulses mostly cancel each other because they often have opposite polarities. MATLAB simulation predicts an SNR of 136 dB due to a 100-ps jitter, i.e., 0.5%, of period jitter on MCLK, in the deadband's duration.

Furthermore, in the RTDEM scheme, the jitter on MCLK slightly varies the contribution of each DAC element to the output, potentially impacting its efficacy. As mentioned previously, DAC mismatch and imperfect timing cause a small portion of the PCM-to-PWM distortion to leak into the output. MATLAB simulations were performed to evaluate this effect. For a −1-dBFS input, with both 0.5% mismatch and 100 ps of MCLK jitter, the simulated SNR is 126 dB. For a −60-dBFS input, this noise is lower, and the simulated SNR is 72 dB.

IV. Closed-Loop CDA Implementation

A. Top Level

Fig. 12 shows a top-level schematic of the proposed digital-input capacitively coupled CDA. It adopts the output stage from [8]. To stabilize the loop in the presence of the pair of complex poles introduced by the *LC* filter, the dual-loop structure of [9] is employed. The overall structure is similar to that of [10]. The feedforward path from the input to the input of the 3rd integrator is omitted in this work to avoid the need for another DAC. As a result, the 2nd integrator must now process the full signal swing and the 1st integrator's output swing increases by 6 dB/octave with respect to the input frequency. To maintain sufficient linearity for these two stages under the worst case of an FS input at 20 kHz, relatively

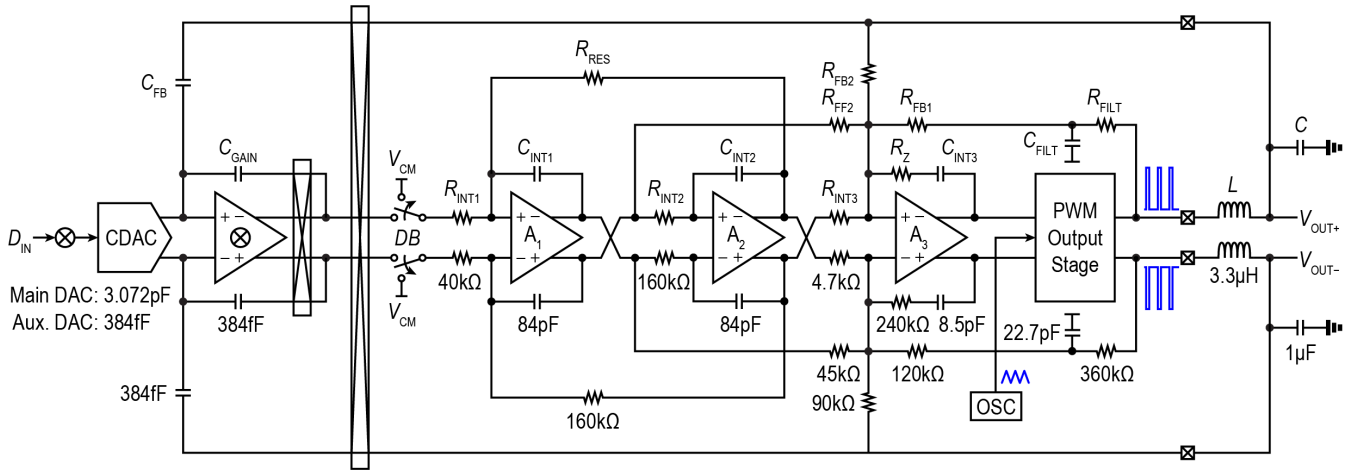

Fig. 12. Top-level schematic of the proposed digital-input capacitively coupled CDA.

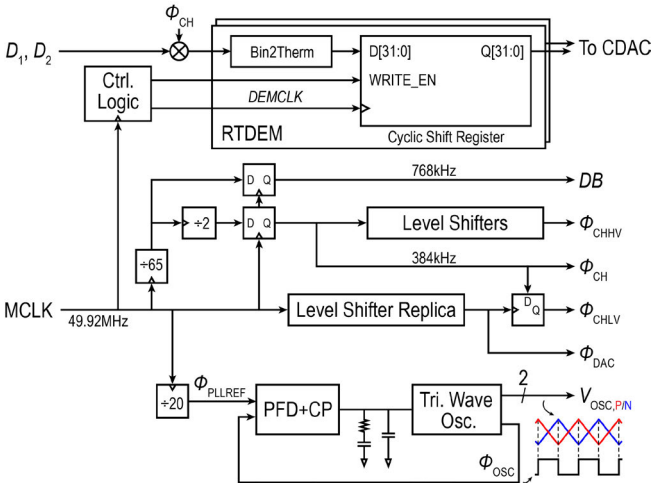

Fig. 13. Timing circuitry for chopping, RTDEM, deadband, and PWM.

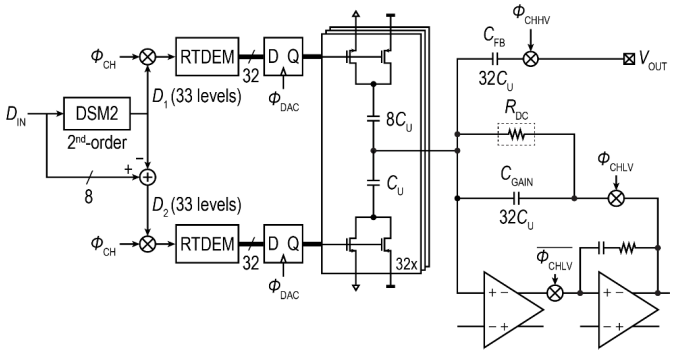

Fig. 14. Schematic of the DAC and CCCA.

large integration capacitors (80 pF) are employed to limit the swing of these integrators, consuming 6% of the total chip area. Process variations on the *RC* time constants are addressed by a 2-bit trim of the integration capacitors as in [8], [9], and [10] to keep them within 7% of their nominal values.

B. Timing and RTDEM Logic

A high-frequency clock (MCLK) is required to define the sub-intervals for RTDEM, as shown in Section III-B. The MCLK frequency is $f_{MCLK} = 49.92$ MHz, which equals $65 f_S$. For each DAC sample, one MCLK cycle is allocated for the deadband and the remaining 64 for RTDEM. In the prototype, the sampling clock f_S and chopping clock f_{CH} are divided down from MCLK using digital counters, as shown in Fig. 13. The PWM frequency $f_{PWM} = f_{MCLK}/10$ is ensured by embedding the triangle wave oscillator in [8] into a charge-pump phase-locked loop (PLL) [39]. Timing skew introduced in the HV feedback chopper is mitigated using a replica level shifter [10]. The RTDEM is realized by cyclic shift registers, as shown in the upper part of Fig. 13.

C. DAC and CCCA

Fig. 14[2] shows a schematic of the DAC and CCCA. The cyclic shifter register outputs are retimed by Φ_{DAC}, the level shifter replica's output, to align the chopping transitions of the DAC output and HV feedback. A unit capacitance of 12 fF is chosen such that the total capacitance corresponding to the signal component D_1 ($256C_U$) dominates over the parasitic capacitance at the summing node. All capacitors connected to the summing node are implemented with custom MOM capacitors for their high voltage rating and use the same 12-fF unit cell to ensure good matching. As shown in Fig. 9, RTDEM always activates consecutive DAC elements. To mitigate the effect of process gradients, a recursive layout pattern is employed for the unit elements [40].

V. Measurement Results

A prototype of the proposed digital-input capacitively coupled CDA is fabricated in a 180-nm bipolar, CMOS, and DMOS (BCD) technology. Fig. 15 shows a microphotograph

[2]In [10], a resistor R_{HV} was added in series with each feedback capacitor C_{FB} to avoid over-voltage conditions at the virtual ground node due to impedance imbalance caused by the relatively high resistance of the input chopper. In this work, the input chopper is replaced with the parallel combination of all DAC switches, which has an equivalent resistance of $<1\Omega$, much less than the ON-resistance of the HV chopper. Therefore, a resistor in series with C_{FB} is no longer needed.

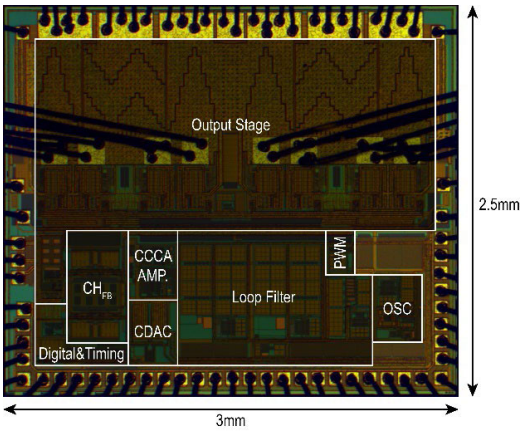

Fig. 15. Die micrograph.

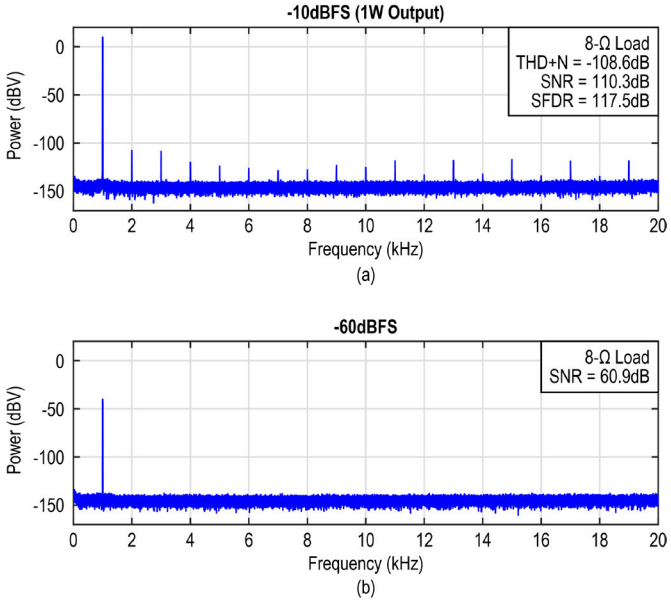

Fig. 16. Measured output spectra for (a) −10 dBFS input and (b) −60 dBFS input (256k-point FFT, 4× averaged).

of the die, which occupies 7.5 mm^2. During idle operation, it draws 200.2 mW from the 14.4-V output-stage supply (PVDD), 23.4 mW from the 1.8-V analog supply (AVDD, including loop filter, triangle wave oscillator, and PLL), 0.46 mW from the 1.8-V digital supply (DVDD, including timing logic), and 25 μW from the 1.8-V DAC reference. A 10-μF external decoupling capacitor is employed for the DAC reference, and care was taken in the PCB layout to minimize interference to the reference, which is driven by a commercial off-the-shelf linear regulator with a thermal noise floor of 2 nV/$\sqrt{\text{Hz}}$. A crystal oscillator provides MCLK [41]. For flexibility, the interpolation filter and digital DSMs are implemented on an field-programmable gate array (FPGA). Their synthesized area and power in the 180-nm BCD process would be 0.36 mm^2 and 350 μW, respectively. An Audio Precision APx555B audio analyzer provides a 24-bit digital input and captures the CDA output.

Fig. 16(a) shows the measured output spectrum when the CDA drives 1 W into an 8-Ω load, corresponding to about −10 dBFS. The measured THD+N is −108.6 dB, and the SNR is 110.3 dB. Fig. 16(b) shows the output spectrum for a −60-dBFS input, showing a clean spectrum. An SNR of 60.9 dB is observed, indicating a DR of 120.9 dB for the CDA.[3]

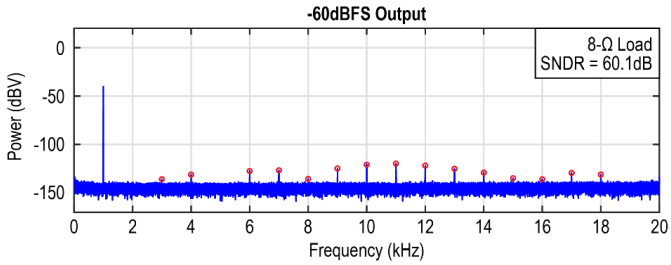

Fig. 17. Output spectra when NS segmentation is performed by a 1st-order DSM.

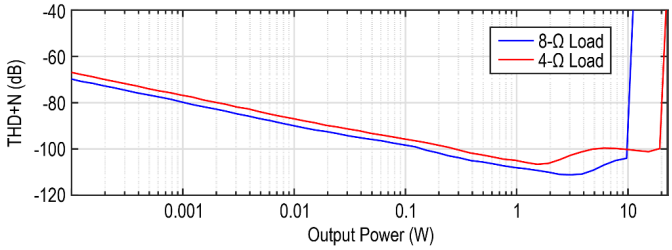

Fig. 18. Measured THD+N versus output power.

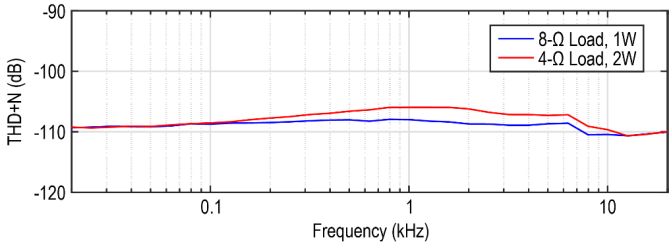

Fig. 19. Measured THD+N versus input frequency.

A test mode was implemented to evaluate the effect if only a 1st-order DSM is used for NS segmentation. Its output spectrum is shown in Fig. 17. Harmonics at the −80-dBc level due to the "frequency-modulated idle tones" [37] are clearly visible. Although some 20 dB below the total integrated noise, Pavan et al. [25] suggest that they could be discerned by human hearing and thus should be avoided.

The measured THD+N across output power is plotted in Fig. 18, reaching a minimum of −111.2 dB for the 8-Ω load and −106.6 dB for the 4-Ω load. The rise in distortion levels toward high output power is dominated by HD2 [already visible in Fig. 16(a)]. It is likely due to the magnetic coupling between the CDA output current and the DAC reference traces on the test PCB. According to simulations, −110 dB of coupling can lead to a similar result. Fig. 19 shows the THD+N across the audio band for a −10-dBFS input.

Fig. 20 shows the measured power efficiency across output power up to the point of 10% THD. The peak efficiency is 90% for an 8-Ω and 86% for a 4-Ω load. The degradation compared to that in [10] is due to the increased output current and

[3]This method of determining the DR is consistent with prior works on digital-input audio drivers [13], [14], [15], [16], [34].

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART DIGITAL-INPUT HV CDAS

	This Work	E. Cope ISSCC 2018	D. Schinkel JSSC 2017	J.-M. Liu JSSC 2014	T. Ido ISSCC 2006	ADI SSM3582A	Cirrus Logic CS35L45
Area (mm^2)	**7.5**	4.3	-	-	23[1]	-	6.5
Architecture	**Closed-Loop**	Closed-Loop	Closed-Loop	Open-Loop	Closed-Loop	Closed-Loop	Closed-Loop
DAC Type	**CDAC**	RDAC	IDAC	-	IDAC	-	-
Supply (V)	**14.4**	8~20	25	18	35	4.5~16.5	2.5~15
$I_{Q,PVDD}$ (mA)	**13.9**	20.5	-	9.4	-	12.3	-
R_{LOAD} (Ω)	**8/4**	8/4	4	8	4/6/8	8/4	8
$P_{OUT,MAX}$ (W)	**13/23**	20	80	13	130/99/74[1]	18/32	6.8
Efficiency	**90%/86%**	90%	>90%	88%	81%[1]	94%/91%	88%
Peak THD+N @ 1kHz	**-111.2/-106.6**	-97.2[2]/-93.1[2]	-88.6	-62.5	-94.9	-94[2]	-79
DR (dB)	**120.9**	115.5	115	84	113	109	-
A-wt. Output Noise (μV_{RMS})	**9.3**	20	34	-	-	36	5
PSRR (dB) (Freq./Hz)	**97~78 (20~20k)**	80~50 (20~20k)	88~60 (100~20k)	-	-	88 (1k)	-
Suppress LC Filter Distortion	**Yes**	No	Yes	No	No	No	No

[1] Output stage is off chip
[2] Extracted from figure

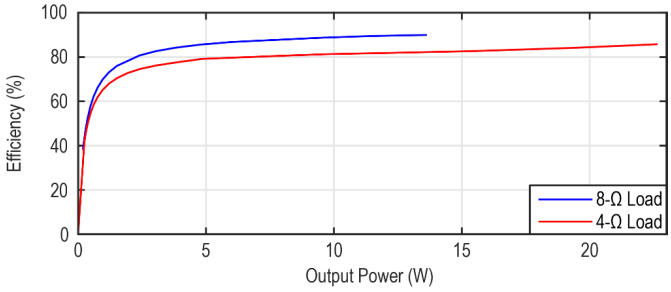

Fig. 20. Power efficiency across output power.

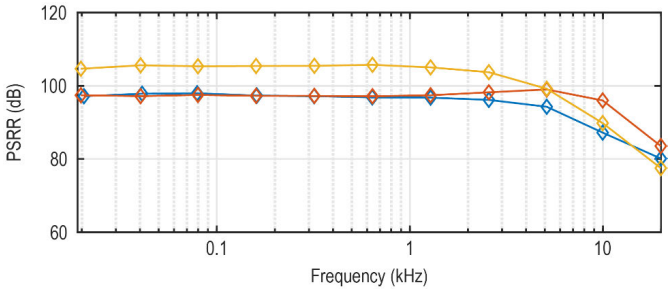

Fig. 21. Measured PSRR across the audio band for three samples.

switching activities from shaped quantization noise. Fig. 21 shows the measured PSRR across the audio band for three samples.

Table I summarizes the performance of this work and compares it with thr state-of-the-art HV digital-input CDAs [11], [12], [15], [17], [42], [43]. It achieves the highest DR and the best peak THD+N, thanks to the capacitively coupled architecture and proposed mismatch and ISI mitigation techniques. Meanwhile, it features competitive power efficiency, idle power, and PSRR.

VI. CONCLUSION

This article presents a digital-input capacitively coupled CDA. Distortion sources due to DAC mismatch and ISI are mitigated using NS segmentation, RTDEM, and a deadband. Intermodulation distortion between the DAC, chopping, and PWM are avoided by carefully choosing f_S, f_{CH}, and f_{PWM}. Measurement results of the 180-nm prototype show a DR of 120.9 dB and a peak THD+N of −111.2 dB, which advances the state-of-the-art in HV digital-input CDAs by 5.4 and 14 dB, respectively.

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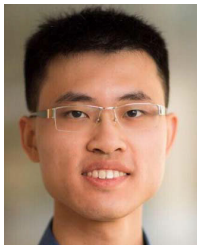

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