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EMT Simulation Based Parametric Tuning of Damping Support in MMC- HVDC Networks

Monika Sharma[1], Peter Palensky[1], and Jose Luis Rueda Torres[1]

[1]Department of Electrical Sustainable Energy, Delft University of Technology, Delft, Netherlands
{ *M.sharma-3,P.Palensky,J.L.RuedaTorres*}*@tudelft.nl*

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***Abstract*—One crucial aspect of Modular Multi-level Converter (MMC)- Bipolar Point-to-Point (BPP) configuration systems is the occurrence and damping of oscillations on the DC side of HVDC networks. These oscillations can arise due to various factors, including the interaction between the AC and DC systems, de-blocking of converters after a fault, and the dynamic behaviour of connected power sources. Various investigations consider damping methods that delve to mitigate oscillatory tendencies and establish stability during Post-Fault (PF) recovery. However, the current research on damping predominantly focus on the impact of AC fault or unbalanced conditions on the DC side. This paper presents an investigation that addresses the gap concerning with sub-synchronous oscillations occurring during the de-blocking of a MMC-BPP within the post-DC fault recovery. The investigation also considers active damping and enhanced current control loop as a combined mitigation measure. A meticulous real-time digital simulation supported parametric sensitivity analysis is conducted on a four-terminal MMC-BPP synthetic power system. Numerical results provide insight into the level of effectiveness that can be achieved by the considered concept of active damping.**

***Index Terms*—Bipolar point-to-point network, Active damping controller, Electromagnetic Transient (EMT) simulation, High Voltage Direct Current (HVDC) network.**

I. Introduction

THE surge in power electronics adoption presents challenges for power systems, diminishing inertia and damping and potentially leading to instability. This alters power system architecture and introduces novel stability concerns [1]. The progression of Voltage Source Converters (VSC) propels the development of High Voltage Direct Current (HVDC) networks, with VSC-HVDC gaining traction for connecting offshore wind farms to local power systems. The preferred approach for constructing HVDC networks is the Modular Multi-level Converter (MMC), offering advantages such as the output voltage of the MMC at the AC terminal can be closed to ideal sinusoidal waveform, and the filters at the Point of Common Coupling (PCC) can be eliminated [2]. MMC is envisioned as a replacement for the two-level VSC in HVDC and DC grid transmission systems. However, the stability challenges of MMC Bipolar Point-to-Point (MMC-BPP) systems necessitate exploration, prompting researchers and engineers to address the interactions between control and physical systems. This paper delves into damping techniques to enhance Power Fault (PF) recovery in HVDC networks, pinpointing a DC voltage regulation control mechanism and an enhanced current control loop for MMC-BPP as an effective strategy. A parametric sensitivity analysis evaluates system performance under diverse conditions.

The paper is structured with an overview of the state-of-the-art, limitations, and literature review in Section II. Section III discusses active damping control and the approach for parametric sensitivity analysis, while Section IV presents a comprehensive examination of results and analysis. The conclusion is provided in Section V.

II. State-of-the-art

In maintaining the stability of HVDC networks, the PF recovery process holds paramount significance, especially in cases of DC faults. These faults encompass temporary or prolonged disruptions in the regular operation of the HVDC networks, stemming from diverse factors like insulation failures, short-circuits, or equipment malfunctions.

The efficacy of the PF recovery process hinges significantly on the operational status of converters within the HVDC network during fault occurrences. Various Fault Ride-Through (FRT) conditions necessitate the temporary blocking of converters, with the maximum disturbance to power flow primarily contingent upon the specific scenario at hand.

Upon the deblocking of the converter following post-DC fault recovery, the restoration of the system to normal operation can incite voltage oscillations, current imbalances, and power fluctuations within the DC side. Swift changes in converter operations, such as the reconnection of affected converters, may introduce transient oscillatory behaviors in DC voltage and current. These oscillations can manifest at different frequencies, dependent on system characteristics and employed control strategies, ranging from sub-synchronous to super-synchronous frequencies [3].

To counteract and stabilize DC-side oscillations during the deblocking process, several control techniques and strategies, including damping control, DC-side filtering, and refined control system designs, can be implemented.

Ensuring a rapid and stable post-DC-side fault recovery is indispensable in a fault-clearing strategy aimed at sustaining uninterrupted operations in interconnected HVDC networks. While numerous studies have scrutinized the recovery process of a single converter, the comprehensive understanding of post-DC-side fault recovery in interconnected HVDC networks

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and the intricate interplay between converters and the HVDC network during system recovery remains a largely unexplored area in existing literature [4] [5] [6].As the restoration of converters during post-DC-side fault recovery can trigger inadequately damped oscillations, thorough investigation in this domain is imperative.

The PF recovery strategy is tasked with the stable restoration of DC voltage to levels closely resembling pre-fault values. This necessitates the swift recovery of voltage (and consequently, power flow) while effectively managing oscillations, preventing over-currents, and averting over-voltages.

The presence of capacitive and inductive components, such as converters, cables, and line inductors, within the HVDC network results in the emergence of resonant frequencies. The switching or deblocking of converters at voltage levels differing from the grid voltage can stimulate oscillations at these resonant frequencies.

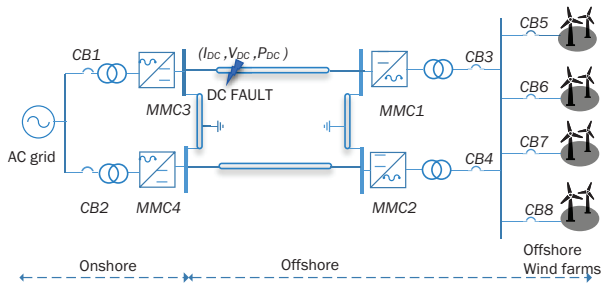

Fig. 1: Four terminal bipolar point-to-point offshore AC-DC network

Before addressing methodologies for enhanced damping, understanding the origins of oscillations during post-fault recovery is pivotal. Uncontrolled oscillations manifest during converter de-blocking, arising from the interplay between converters and the HVDC network in the recovery phase. These oscillations' magnitude depends on network damping characteristics unless the converter controller effectively regulates and suppresses non-DC component frequencies. Poor damping, influenced by DCCB inductors or converter deblocking due to faults, contributes to oscillations, potentially causing overvoltages or overcurrents on the DC side (as shown in Fig. 1).

The configuration, as illustrated in Fig. 1, involves onshore MMCs (MMC3 and MMC4) for positive and negative poles, linked to an AC source representing a robust onshore power system. Onshore MMC models enhance the accurate capture of dynamics in offshore-onshore power transfer, with MMC1 and MMC2 forming the offshore terminal connected to 2GW offshore wind farms.

This study focuses on Sub-Synchronous Oscillations (SSO) during converter de-blocking at the DC side of HVDC networks. Triggered by factors like faults and disturbances, SSOs result in power fluctuations and voltage deviations, posing threats to power system operation and equipment [7]. Damping SSOs is crucial for reliable operation, as they limit power transfer capabilities, risk system failures, and stress components [8].

Recent literature suggests effective control strategies for damping SSOs during post-fault recovery. Active and passive damping methods, including modulated signals like model predictive control or DC-side voltage regulation, show promise in rapidly attenuating oscillations and enhancing damping efficacy [8].

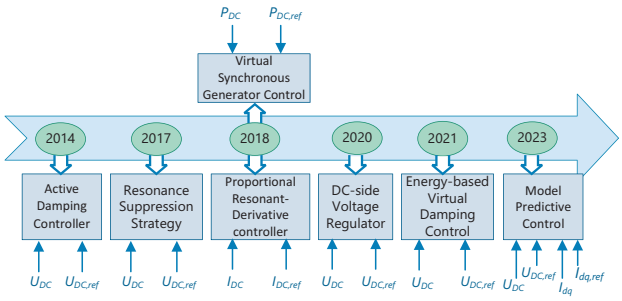

Fig. 2: Illustrates various damping control techniques available for SSOs damping.

Nevertheless, damping control in power systems encounters various challenges owing to system complexity, restricted observability, fluctuations in parameters, coordination intricacies, and the emergence of new oscillatory modes. These factors can hinder damping technique efficacy, emphasizing the need for continual enhancements. Enhanced control strategies, refined measurements, precise modeling, and coordinated control mechanisms effectively address these challenges, fostering improved damping capabilities to maintain system stability.

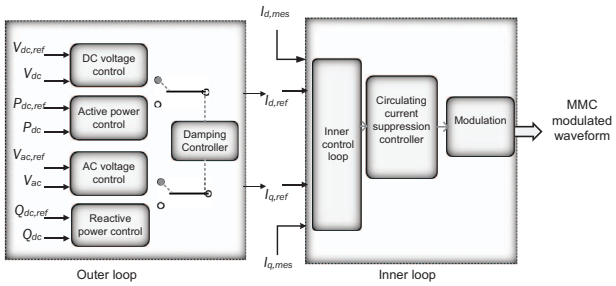

Fig. 3: Control loop structure inside MMC

In HVDC network operations, various supplemental controllers have been proposed to curb voltage and current oscillations, enhancing damping at the DC side. Fig. 2 provides an overview of diverse damping control methods to mitigate SSOs. Incorporating a damping controller requires an additional control loop within the outer loop of VSC-HVDC control, as shown in Fig. 3. The utilization of a modulated signal involves implementing damping methods for HVDC networks, introducing an additional signal injected into the converter current control loop to modulate the DC current/voltage and have better damping of SSO.

Each damping control strategy has distinct characteristics

and benefits. Modulated signals improve SSO damping by elevating the damping coefficient and reducing overshoot and settling time. In a recent study by Liu et al. [9], adopting the D-Q Circulating Current Suppression Control (CCSC) method and modulated signal yielded notable improvement at the DC side. Modifying the D-Q type CCSC suppressed non-DC components, resulting in a 2.59% reduction in overshoot and a 3.57

Virulkar et al. [8] integrated CCSC with Model Predictive Control (MPC) to effectively suppress circulating current and enhance damping. Their research demonstrated a 13.6% reduction in settling time compared to the conventional PI control method. In a separate study by Li et al. [10], a novel active damping method termed virtual active damping or resonance suppression strategy was employed to investigate DC-link voltages. This approach emulated the resonance suppression effect similar to that of a passive damping controller, ensuring the maintenance of DC-link voltages within an acceptable range of $\pm 10\%$. D. Wu et al. [11] proposed the utilization of virtual synchronous generators, employing virtual inertia and virtual damping control with a proportional-derivative controller to enhance the damping and inertia of DC networks. Their analysis emphasized the detrimental impact of time delays on the stability of DC networks.

Post-fault oscillations propagate from the voltage loop and grid currents to the inner current loop, as shown in Fig. 3. Without a damping controller, the reference currents (I_{dref} and I_{qref}) experience distortion due to oscillations. Effective damping within the current loop can attenuate Sub-Synchronous Oscillations (SSO) before reaching the PWM block. Thus, further exploration into the damping capabilities of the inner current loop, which regulates the current in each arm of the converter, is warranted.

The CCSC method modulates the DC current within the current control loop to suppress oscillations. The CCSC output is crucial in determining the DC current's behavior during post-fault recovery, operating by detecting current instabilities and implementing corrective measures to dampen oscillations, ensuring stable operation [3] [12]. Numerous CCSC algorithms have been proposed, based on D-Q coordinates, energy control methods, and PR controller-based or repetitive controllers, as highlighted in existing literature [3], [12]–[14].

The D-Q coordinate-based CCSC is a common method, utilizing two Proportional-Integral (PI) controllers to directly suppress circulating current in the D-Q frame by setting the reference value to zero [12]. The energy control method aims to reduce circulating current by controlling the total energy and balancing the energy difference between upper and lower arms, as circulating current is caused by the energy difference [3]. The PR controller or repetitive controller-based method eliminates high-order harmonics in the circulating current and can serve as compensation for other control methods [14].

While the conventional D-Q type CCSC is commonly used to eliminate double-frequency circulating currents, recent research highlights inadequately damped oscillations or instabilities linked to DC-side current [15]. Freytes et al. [16] introduced a Fast Circulating Current Controller (FCCC) that differs in its approach, presenting a 7% reduction in overshoot and a 12% reduction in settling time compared to the conventional D-Q CCSC. This indicates the potential of the modulated signal with CCSC in enhancing oscillation damping, contributing to improved stability and performance in HVDC networks [12]. Therefore, literature suggests that utilizing a modulated signal with CCSC enhances oscillation damping, leading to improved stability and performance in HVDC networks.

III. System Analysis

For context, the system model depicted in Figure 1 is simulated using the Real Time Digital Simulator (RTDS), which is controlled by the control loops elucidated in Section II. The RTDS tool is closely linked with a software known as RSCAD, tailored specifically for conducting EMT simulations on the dedicated hardware of the RTDS Simulator. With a user-friendly interface, RSCAD can be operated on a user's computer while the simulation processes on specialized RTDS units, such as PB5 cards or NovaCor units [17]. In this research, three NovaCor units, each equipped with four cores are utilized.

The parameters considered for this study are based on the model outlined in [18]. The voltage level of 640 kV DC for the HVDC network is considered, necessitating 320 submodules per arm to achieve a voltage of ± 320 kV for the positive and negative poles, respectively. The offshore wind farm has a total capacity of 2 GW, comprising four collective OWFs (each housing 500 MW installed capacity, represented by the Wind Generation System) and MMCs rated at 1 GW each. The cables are emulated using Bergeron models with RLC data parameters.

A. Performance of Active Damping Control and Enhanced CCSC

The necessity for an active damping approach holds significant significance in the pursuit of improving post-fault recovery in BPP-HVDC networks. This study focuses notably on the DC-voltage regulation technique, especially when integrated with the improved D-Q type CCSC controller, and employs parametric sensitivity analysis as a crucial means for system assessment.

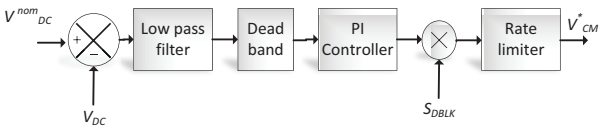

Fig. 4: DC-voltage regulation method control loop

1) DC-voltage regulation method: The primary focus of this study revolves around the control loop of the DC-voltage regulation method, as illustrated in Figure 4. Instances where the post-fault DC-side voltage consistently drops below the designated minimum threshold (V_{DC}^{min}) often lead to a disparity between the grid-side and converter DC-side voltage,

attributable to the constraints of existing controls and voltage evaluation criteria. To rectify this discrepancy during the de-blocking process, it becomes imperative to align the converter DC-side output voltage precisely with the grid-side DC voltage. This alignment is achieved by reducing the number of actively engaged sub-modules during the de-blocking moment, thereby effectively decreasing the converter DC-side voltage to closely match the grid-side voltage.

The DC-voltage regulation method achieves a reduction in submodule count during de-blocking by subtracting the control loop output from the internal voltage reference. The controller activation is specifically triggered solely at the de-blocking instance through the signal S_{DBLK}. A rate limiter has been implemented to manage the rate at which submodules are adjusted. This limiter facilitates the acceleration of submodule reduction until the nominal DC-side voltage is reached, preventing sudden fluctuations while regulating the rate of submodule insertion. The voltage error, representing the deviation between the nominal DC voltage and the grid voltage, is integrated into the controller ($G(s)$) to fine-tune the system response during de-blocking. Typically, a proportional controller suffices for DC-side voltage regulation, with the inclusion of a low-pass filter to eliminate undesirable high-frequency components. Under normal operating conditions, the controller output remains at zero due to the dead-band block, as the DC-side voltage closely aligns with the nominal value. However, if the DC-side voltage falls below V_{DC}^{min} at the de-blocking moment, leading to an error surpassing the predefined dead-band, the controller output is engaged to reduce the inserted submodules, thus aligning the system with the grid voltage.

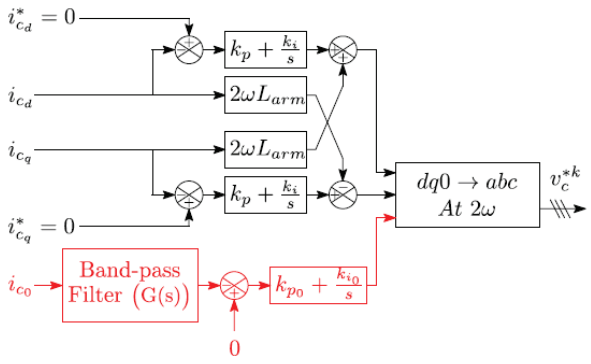

Fig. 5: Modified D-Q CCSC [3]

2) Role of enhanced D-Q CCSC: As highlighted in Section II, the utilization of the D-Q type CCSC configuration serves to improve damping properties while maintaining the steady-state DC current. This study involves a parametric sensitivity analysis of the enhanced D-Q type CCSC, illustrated in Figure 5. The configuration is specially crafted to minimize the impact of zero-sequence non-DC elements in the circulating current, ensuring minimal disruption to the steady-state DC component [3].

Non-DC components infiltrate the zero-sequence component (i_{c_0}) during post-fault recovery, which ideally should only contain a DC component during steady-state operation, as depicted in Figure 5. To handle these non-DC components within the zero-sequence current, a band-pass filter is used to effectively isolate them from the DC component. Additionally, a PI controller is employed to drive these non-DC components toward zero. The band-pass filter's bandwidth is carefully chosen to cover a wide range of resonant frequencies, identified through a comprehensive analysis of DC-side resonance.

The aforementioned study emphasizes the importance of carefully selecting appropriate parameters for DC-voltage regulation methods and enhanced CCSC in order to enhance the damping of post-fault oscillations during the de-blocking of the converter. The subsequent section will delve into the key parameters that need to be considered to improve post-fault recovery on the DC side of networks.

IV. Results and Analysis

This study investigates a four-terminal BPP configuration (Figure 1) without DC circuit breakers. During a severe DC fault near MMC3, the switch on the DC side is instantaneously opened to isolate the fault, effectively blocking MMC3. Upon fault resolution, MMC3 is deblocked.

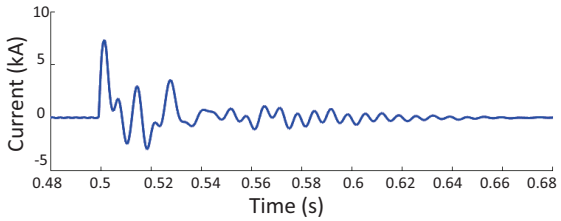

Fig. 6: Current at PCC after deblocking of MMC3 converter

Figure 6 represents the current at PCC near MMC3 when no damping controller is utilized. To facilitate improved post-fault recovery, a DC voltage regulation method is adopted as a damping controller. Parametric sensitivity analysis is conducted on the crucial parameters of the DC voltage regulation method, specifically the Low Pass Filter (LPF), where stability relies on the relationship between the Gain (G) and the Time Constant (TC). Experimentation is employed to fine-tune the values of G and TC. Table Ia and Figure 7 demonstrate the outcomes for various G and TC values at the moment the MMC3 converter is deblocked, as shown in Figure 1, subsequent to recovery from a severe DC fault. The results indicate the optimal values of a gain at 1 and time constant at 0.01. Furthermore, variations in G and TC lead to an increase in peak overshoot value and settling time.

Following the low-pass filter is the dead-band controller, where values are chosen to prevent oscillations of the dead-band controller output around the setpoint, ensuring the controller remains responsive to changes in the error signal. In this case study, the DC reference and measured DC voltage are

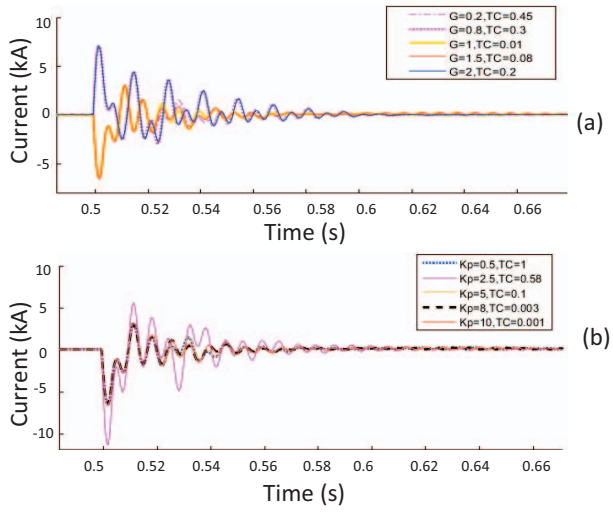

Fig. 7: Parametric sensitivity analysis DC-voltage regulation method (a) low pass filter (b) PI control coefficients

considered in per unit. Consequently, the error becomes zero when the measured DC voltage equals the DC reference. For the study, high level and low level thresholds are maintained at 1.05 and 0.95, respectively, while the slope is set at 1.

Optimizing the PI controller K_P (Proportional Gain) and Integral Time Constant (ITC) is critical to determine the controller's sensitivity to the error signal and eliminate steady-state error. Different values of K_P and ITC are examined to achieve the desired response for the DC voltage to closely track the DC reference. Table Ib and Figure 7 present various combinations of K_P and ITC, with the optimal values determined as 8 and 0.003, resulting in a notable reduction in overshoot time and settling time at the PCC point when the MMC3 converter is deblocked. Additionally, a rate limiter is incorporated to prevent the PI controller from making rapid and significant output changes, which could potentially lead to instability. The rate limiter's limits are set to control the rate of change of the PI controller's output.

The optimal values derived from the parametric sensitivity analysis for the DC voltage regulation method are utilized and introduced as input to the inner control loop. As detailed in Section III, the modified D-Q CCSC involves the tuning of the band-pass filter and PI controller to minimize the influence of zero-sequence non-DC elements. The frequency of the band-pass filter should be carefully selected to permit the desired frequency components to pass through while suppressing frequencies beyond this designated range. Table II presents the results of the frequency domain analysis, aiding in the selection of the band-pass filter's cutoff frequency based on the Gain Margin (GM) and Phase Margin (PM). For a cutoff frequency of 300 Hz, a GM of 1.23 and a PM of 0.76 degrees suggest that the system remains relatively stable, offering some flexibility for adjustments in gain. However, the small phase

TABLE I: Outcome of the Variation in the Parameters of Damping Controller (a) Low Pass Filter (b) PI Control Coefficients

Gain (G)	Time Constant (TC)	Peak Overshoot Value	Settling Time
0.2	0.45	3	0.07887
0.8	0.3	6.91	0.12283
1.5	0.08	3.5	0.05761
1	0.01	2.7	0.052667
2	0.2	7	0.181607

(a)

Proportional Gain (K_P)	Integral Time Constant (ITC)	Peak Overshoot Value	Settling Time
0.5	1	3.136	0.092652
2.5	0.58	5.4	0.1353
5	0.1	3.2	0.084924
8	0.003	2.8	0.063586
10	0.001	3.132	0.182092

TABLE II: Frequency Domain Analysis to Select Cut-off Frequency of BPF

Cut-off frequency	Gain Margin	Phase Margin
300 Hz	1.23	0.76
400 Hz	11.32	119.51
500 Hz	15.01	-57.07
600 Hz	12.41	-173.82

margin indicates that the system is near its stability limit. With a cutoff frequency of 400 Hz, a GM of 11.32 signifies a comfortable gain margin, indicating favorable stability. A PM of 119.51 degrees further reinforces the system's stability and robustness, indicating a substantial phase lead. However, at frequencies 500 and 600 Hz, the high GM suggests a significant safety margin against gain-induced instability. Nevertheless, the negative phase margins of -57.07 and -173.82 degrees raise concerns. A negative phase margin of such magnitude implies that the system is likely to be unstable or highly underdamped, potentially leading to oscillations or poor transient response.

TABLE III: Tunning of PI Control Coefficients of D-Q CCSC

Proportional Gain (K_{PCCSC})	Integral Time Constant ITC_{CCSC}	Peak Overshoot Value	Settling Time
0.05	1	7.41	0.229805
0.2	0.5	7.5	0.134063
0.4	0.1	7.04	0.142502
0.6	0.05	5.2	0.125116
0.8	0.01	2.6	0.080074
1	0.005	6.9	0.078798

Moreover, the PI controller is meticulously adjusted while examining the response with varying values, as illustrated in Table III and Figure 8. An increase in K_{PCCSC} from 0.05 to 0.8 correlates with a noticeable decrease in the peak overshoot value. This reduction aligns with expectations, as

higher K_{PCCSC} values correspond to less overshoot, given the amplified control action of the proportional gain. Significantly, the settling time diminishes when ITC_{CCSC} is reduced from 1 to 0.01. This shift occurs due to the smaller ITC_{CCSC} value, enabling the integral action to promptly accumulate and rectify errors. However, further escalation of K_{PCCSC}

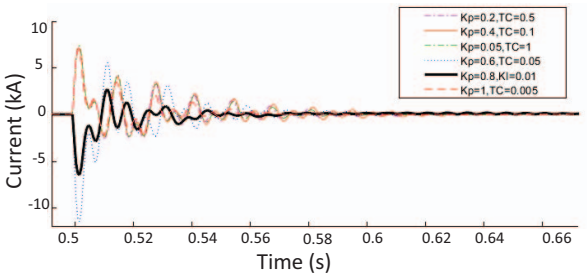

Fig. 8: Parametric sensitivity analysis for PI control coefficients of D-Q CCSC

and ITC_{CCSC} values would lead to increased peak overshoot. Consequently, the controller with K_{PCCSC} = 0.8 and ITC_{CCSC} = 0.01 strikes a balance, yielding relatively low overshoot (2.6) and a rapid settling time (0.080074).

With the finely tuned parameters of the damping controller and CCSC, the reduction in overshoot and settling time amounts to 63.89% and 49.954%, respectively, compared to the BPP-HVDC network without the use of a damping controller, as depicted in Figure 8 compared to Figure 6.

V. Conclusion

This paper provides a comprehensive overview of a 2 GW offshore network within the RSCAD-enabled BPP-HVDC system. The literature review conducted aimed to identify the existing research gaps concerning the damping of subsynchronous oscillations on the DC side of HVDC networks. A DC-voltage regulation method, coupled with a modified CCSC, has been explored in detail to enhance post-fault recovery following the deblocking of the converter. Through meticulous parametric sensitivity analysis, this study seeks to offer a comprehensive evaluation of the system's performance, contributing to the development of more effective post-fault recovery mechanisms and fortifying the resilience and robustness of intricate bipolar HVDC networks.The work in the future will be further extended to enhance the active power controller performance, making the system more resilient during post-fault recovery.

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