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DOI
10.1109/JSSC.2024.3354574

Publication date
2024

Document Version
Final published version

Published in
IEEE Journal of Solid-State Circuits

A 120-MHz BW, 122-dBFS SFDR CTΔΣ ADC With a Multi-Path Multi-Frequency Chopping Scheme

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***Abstract*— Advances in CMOS technologies and circuit techniques have led to the development of continuous-time delta–sigma modulators (CTΔΣMs) that sample at gigahertz (GHz) frequencies and achieve high linearity [<−100 dBc and >120 dBFS spurious-free dynamic ranges (SFDRs)] in wide bandwidths (>100 MHz). However, at low frequencies (≤10 MHz), their performance is limited by the 1/*f* noise generated by the near-minimum size devices used in their wide-bandwidth input stages. This, in turn, limits their use in radio receivers intended to cover both the AM and FM bands. In this work, a multi-path multi-frequency chopping scheme is proposed to suppress 1/*f* noise, while preserving interferer robustness, thermal noise levels, and linearity. Implemented in a CTΔΣ analog-to-digital converter (ADC) sampling at 6 GHz, it achieves a 22× reduction in 1/*f* noise, as well as 122-dBFS SFDR and −98.3-dBc THD in a 120-MHz BW.**

***Index Terms*— Analog-to-digital converter (ADC), continuous time (CT), delta–sigma (ΔΣ), multi-path chopping, wideband receiver.**

I. Introduction

ANALOG-TO-DIGITAL converters intended for high-quality radio receivers often require linearity better than −100 dBc, spurious-free dynamic ranges (SFDRs) better than 120 dBFS, and bandwidths above 100 MHz. High-speed analog-to-digital converters (ADCs) based on continuous-time delta–sigma modulators (CTΔΣMs) sampling at gigahertz (GHz) frequencies can meet these requirements, and so have been used in broadband AM/FM radio front ends [1], [2]. However, the 1/*f* noise added by their first integrator limits their performance at low frequencies (≤10 MHz) since near-minimum size devices must be used to realize amplifiers with sufficiently high-unity gain frequencies (≥10 GHz) [1], [2], [3], [4], [5]. In principle, their 1/*f* noise can be mitigated by chopping. However, chopping the input stage of a CTΔΣM typically results in the folding of out-of-band quantization noise from multiples of twice the chopping frequency ($2f_{ch}$) [6]. Since the output spectrum of a CTΔΣM contains spectral nulls at multiples of the sampling frequency (f_s), such folding can be mitigated by setting f_{ch} to $f_s/2$ or f_s [3], [7]. In high-speed ADCs, however, this approach results in GHz chopping frequencies, which then significantly reduces the effective gain of the input stage and thus, increases the input-referred noise of the first integrator.

Alternatively, f_{ch} can be reduced to $f_s/2N$ by employing an N-tap finite-impulse-response (FIR) digital to analog converter (DAC), and then exploiting the spectral nulls it creates at multiples of f_s/N [6], [8]. However, the lack of feedback at these nulls limits modulator robustness to out-of-band interferers, while the extra feedback delay necessitates the use of extra high-speed compensation DACs [9]. Alternatively, time-interleaved multi-path chopping [10], [11], [12], in which an input stage is divided into M-paths, can be used to reduce the chopping frequency by a factor of M, since quantization noise will now be folded down from $2Mf_{ch}$. In practice, however, some folding will still occur due to the inevitable mismatch between different paths.

In this work, which is an extended version of [13], a multi-path multi-frequency chopping technique is proposed to improve the mismatch sensitivity of a conventional multi-path chopper amplifier and to effectively facilitate chopping at $f_s/6$. Measurements on a prototype CTΔΣM show that with three-path two-frequency chopping, 1/*f* noise is reduced by 22×, while out-of-band interferer rejection is improved by 9 dB compared with the use of conventional single-frequency three-path chopping.

The rest of this article is organized as follows. Section II presents a brief overview of the architecture of the prototype CTΔΣM. Section III discusses the use of conventional chopping techniques in CTΔΣMs. The proposed multi-path multi-frequency chopping technique is described in Section IV. The measurement results are presented in Section V, and this article ends with the conclusion.

II. CTΔΣM Architecture

Fig. 1 shows a simplified block diagram of the proposed wideband CTΔΣM, which employs a 4th-order loop filter

Manuscript received 1 September 2023; revised 4 November 2023 and 29 December 2023; accepted 2 January 2024. Date of publication 1 February 2024; date of current version 28 March 2024. This article was approved by Associate Editor Ron Kapusta. *(Corresponding author: Sundeep Javvaji.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2024.3354574.

Digital Object Identifier 10.1109/JSSC.2024.3354574

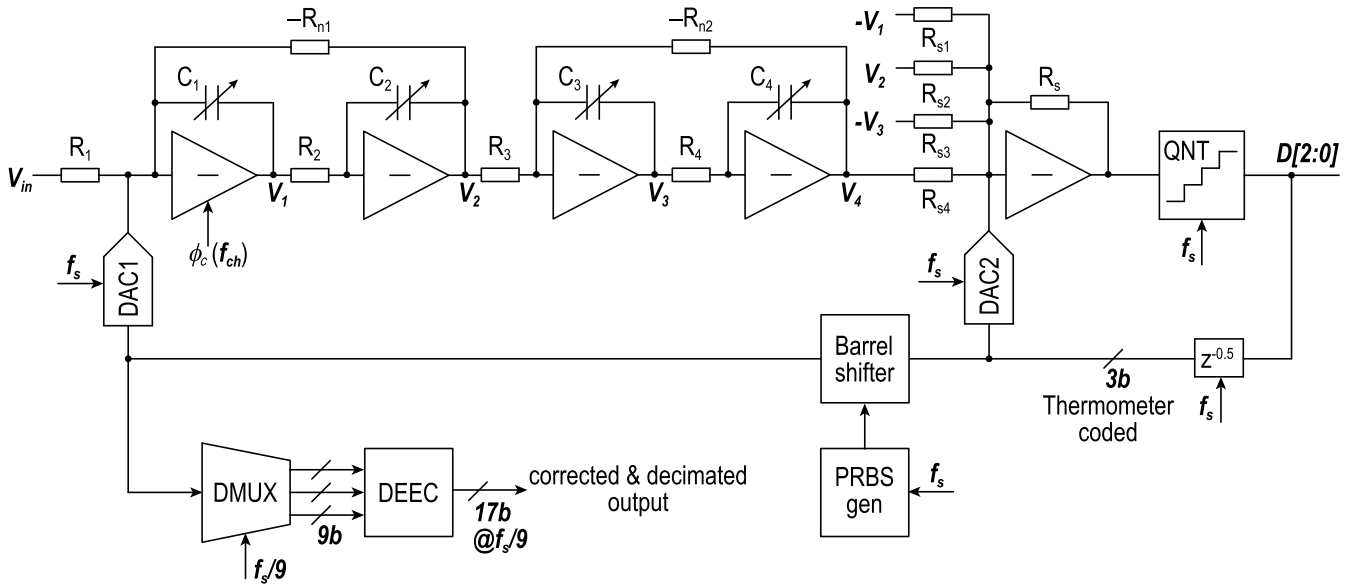

Fig. 1. Simplified architecture of the 4th-order CTΔΣMs modulator.

based on a cascade of two resonators and a 2-b quantizer [1]. The loop filter uses a cascade of integrator with a feed-forward (CIFF) structure for high linearity, together with an active summing amplifier. Sampled at 6 GHz, the modulator achieves a peak signal to quantization noise ratio (SQNR) of 86 dB in a 120-MHz bandwidth. For a single-loop ΔΣ modulator, multi-bit quantization is essential to reduce the required sampling frequency and enable the aggressive shaping of in-band quantization noise needed to achieve high dynamic range [4], [5], [14], [15]. Mismatch errors in the DAC will then limit linearity. Since conventional mismatch-mitigating techniques, such as data weighted averaging (DWA), do not provide sufficient error suppression at low over-sampling ratios (OSR; = 25 in this design), the DAC error estimation and correction (DEEC) technique proposed in [1] is employed to address static mismatch errors. Dynamic errors caused by inter-symbol interference (ISI) are mitigated using a dual return-to-open (RTO) DAC. Since the offset of a multi-bit quantizer can also cause spectral tones, the background offset correction technique proposed in [1] is also used.

For high gain bandwidth (GBW), the integrators of the loop filter are based on multistage inverter-based amplifiers, with the first integrator's input stage being the dominant contributor of 1/*f* noise. Although 1/*f* noise can be decreased by increasing the area of the devices used in the input inverter, this would also limit its bandwidth. Alternatively, the inverter can be chopped, but as discussed in Section I, this can only be done at specific frequencies to mitigate quantization-noise folding.

III. Chopping Techniques in CTΔΣM

Fig. 2 shows a three-stage inverter-based amplifier with a chopped first stage. Also shown are the parasitic input (C_g) and output (C_p) capacitors associated with the first stage. The amplifier employs hybrid (Miller and feed forward) compensation and an active common mode feedback loop (CMFB). The amplifier's power supply is provided by an on-chip low dropout regulator (LDO), which ensures consistent operation by compensating for process and temperature variation [1].

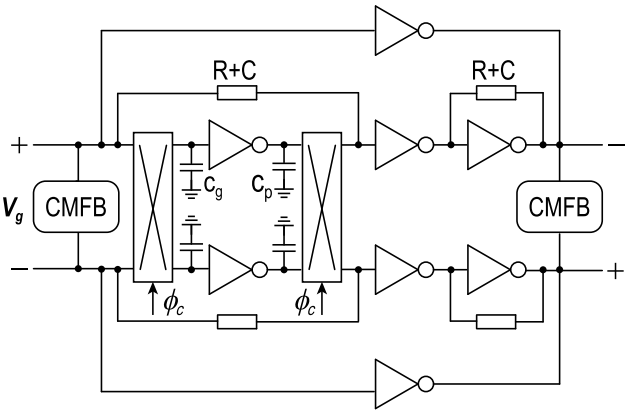

Fig. 2. First amplifier with a chopped input stage.

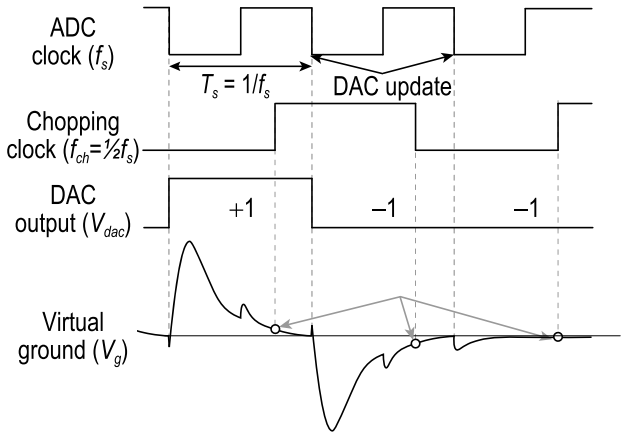

Fig. 3. Virtual ground sampling due to chopping.

In a CTΔΣM, the input of the first integrator is the difference between the input signal and the DAC output and, thus,

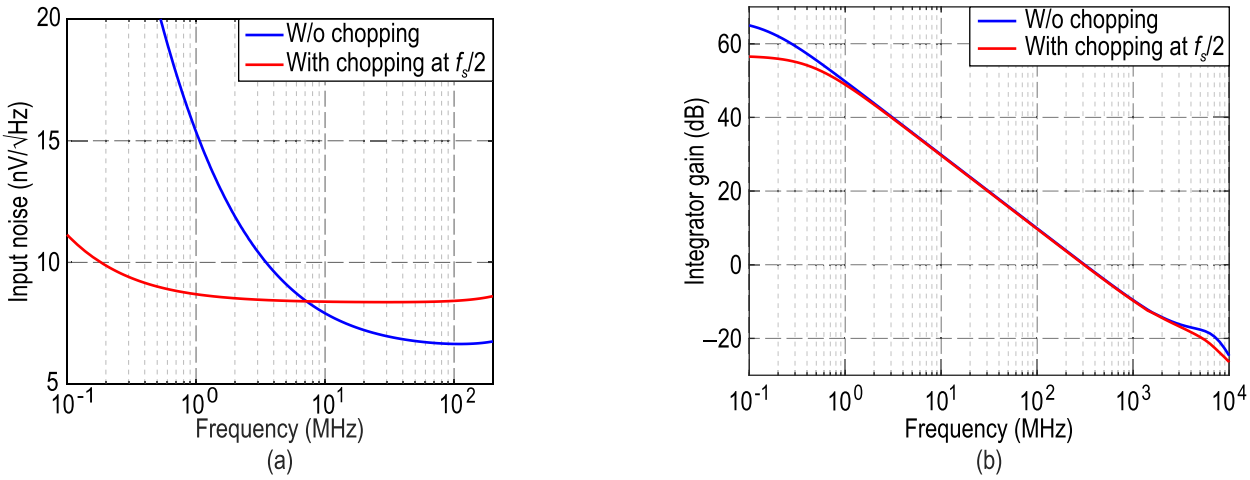

Fig. 4. (a) Simulated input-referred noise from the 1st integrator. (b) Simulated gain of the 1st integrator.

contains significant out-of-band quantization noise. At each falling edge of the ADC sampling clock, as shown in Fig. 3, the DAC updates and, due to the amplifier's finite bandwidth, the virtual ground voltage will have a component that is proportional to the quantization noise. However, the voltages across C_g and C_p are inverted at every chopping transition, causing impulsive currents that are supplied via the integrating capacitor C_1, effectively sampling these voltages at $2f_{\text{ch}}$, and thus fold down quantization noise at multiples of $2f_{\text{ch}}$ [6]. The sequence of error voltages sampled on the integrating capacitor C_1 can be described by

$$V_e[n] = (C_g/C_1)2V_g[n \times 1/2f_{\text{ch}}]. \tag{1}$$

A. Input Switched Capacitor Resistor

At GHz sampling frequencies, the switched capacitor resistors formed by chopping $C_{g,p}$ will significantly degrade the performance of the 1st integrator. Due to the inverter's voltage noise, the input switched-capacitor resistor ($R_{\text{in\_chop}} = 1/4C_g f_{\text{ch}}$) will increase the current noise flowing into the 1st integrator [16]. The operational transconductance amplifier (OTA) input noise referred to the input of the integrator can then be expressed as follows:

$$V_{n,\text{OTA1}}^2 = (4kT\gamma/g_m)\left(\frac{R_1}{R_1||R_{\text{dac}}||R_{\text{in\_chop}}}\right)^2 \tag{2}$$

where g_m is the transconductance of the input inverter, and R_1 and R_{dac} are the input and DAC resistors, respectively.

Schematic-level simulations of the input-referred noise of the first integrator with ($f_{\text{ch}} = f_s/2$) and without chopping are shown in Fig. 4(a). Chopping the first inverter significantly reduces the flicker noise; however, it also causes a 2 dB increase in thermal noise.

B. Output Switched Capacitor Resistor

The switched capacitor resistor formed by the output chopping network along with C_p reduces the low-frequency gain of the amplifier, as shown in Fig. 4(b). This will, in turn, reduce the ADC's linearity at low frequencies and modify its noise transfer function (NTF); which can be seen in measurement results [Fig. 14(d)].

C. Negative-R Technique

Alternatively, the flicker and thermal noise added by the first OTA can be mitigated by using a negative-R at the virtual ground of the first integrator, as shown in Fig. 5 [17]. By matching the negative resistance to the equivalent resistance (R_{eq}) seen from the virtual ground, a high-pass transfer function ($sR_{\text{IN}}C_{\text{INT}}$) can be achieved from the OTA's input voltage noise to the CT$\Delta\Sigma$M output.

The noise suppression for in-band frequencies is proportional to OSR, and so may not be enough in low-OSR (=25) designs. Typically, the negative resistor is implemented using an OTA in positive feedback. Therefore, the noise contribution from the negative resistor is in the same order as the noise added by both the input and DAC resistors, which is often higher than the noise introduced by the first integrator's OTA. In addition, the negative resistor still needs to be chopped at multiples of $f_s/2$ to mitigate its own flicker noise.

D. FIR DACs

The use of FIR DACs in the feedback path is another way to lower the chopping frequency without causing quantization noise folding [6]. As shown in Fig. 6, an N-tap low-pass FIR filter creates nulls in the feedback waveform at multiples of f_s/N, which allows the input stage to be safely chopped at multiples of $f_s/2N$.

However, many taps may be required to achieve wideband suppression of quantization noise in low-OSR designs. The associated feedback delay must then be compensated by adding a direct path around the quantizer, which requires the use of extra high-speed compensation DACs. Since the virtual ground voltage of the first integrator also contains an input component, and the nulls from the FIR DAC are present only in the feedback path, out-of-band interferers at multiples of $f_s/2N$ will not be suppressed and so will be folded into the signal band after chopping.

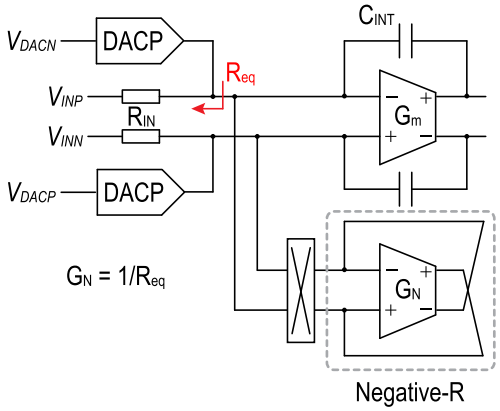

Fig. 5. Negative-R technique.

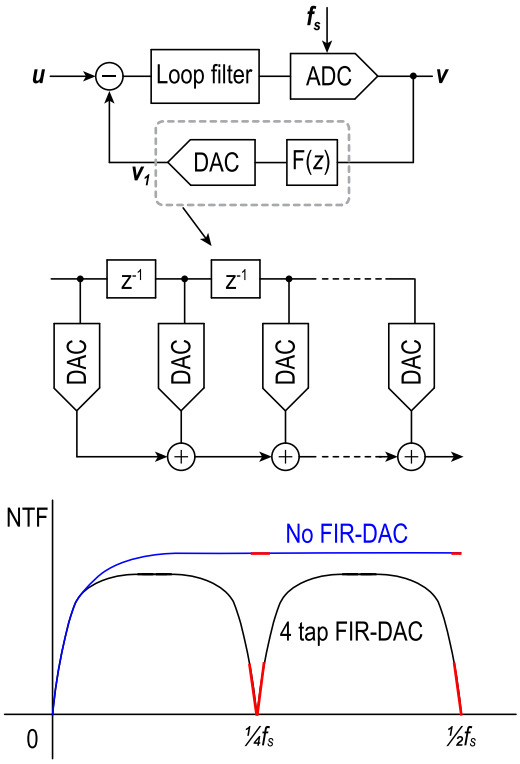

Fig. 6. FIR DACs.

IV. Multi-Path Chopping

A. Conventional Three-Path Clocks

Multi-path chopping [10], [11], [12] is an alternative way of reducing the chopping frequency without incurring quantization-noise folding. Fig. 7 shows the implementation of a three-path inverter-based amplifier, where the first stage of the amplifier is divided into three equal parts. As illustrated in Fig. 8(a), the three pairs of input inverters are all chopped at the same frequency, $f_s/6$, but interleaved in such a way that the clock edges are delayed by $1/f_s$ with respect to each other. This guarantees that there will always be exactly the one chopping clock edge within each sampling period of the CTΔΣM ($1/f_s$).

$V_e[n]$ represents an example sampled sequence due to chopping, assuming that the DAC is outputting strings of

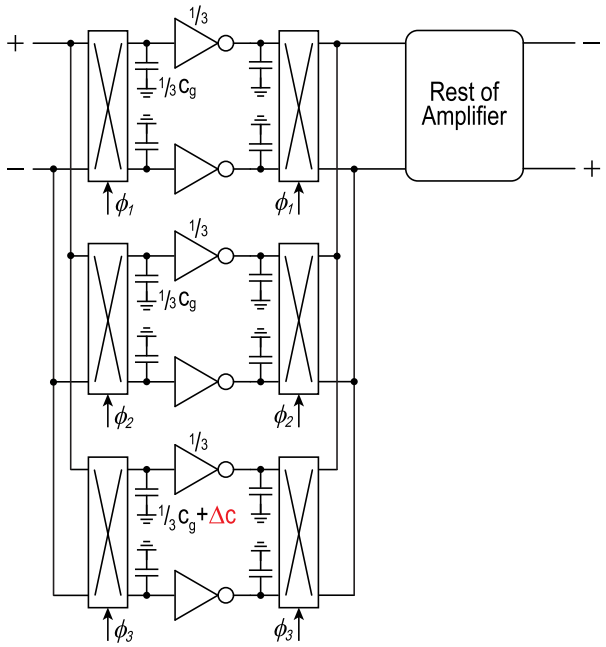

Fig. 7. Three-path chopper amplifier.

"1"s. This is similar to chopping at $f_s/2$ and, thus, should not incur any quantization noise folding. With only a third of the parasitic capacitance being switched or flipped at each chopping clock edge, all the artifacts caused by the input and output switched capacitor resistors will be reduced by a factor of 3 (≈9 dB).

Without mismatch, the sampled sequence $V_e[n]$ due to chopping will consist of identical samples. However, any mismatch between the three paths, either due to parasitic capacitor mismatch or clock skew, will result in quantization-noise sub-sampling and, thus, some residual noise folding. For example, with a mismatched 3rd inverter, one in every three samples is different, resulting in the folding of quantization noise and out-of-band interferers from multiples of $f_s/3$.

B. Proposed Three-Path Clocking Technique

To reduce the sensitivity to mismatch, this work proposes an improved multi-frequency chopping technique based on the observation that quantization noise folding can be avoided as long as there is always one chopping clock edge in each sampling period; and thus, this chopping edge can be in any one of the three paths. Therefore, noise folding will not occur with/without mismatch if just one inverter is chopped at $f_s/2$ while the other two are not chopped, as shown in Fig. 8(b). Even with a mismatch between the three paths, all the samples of $V_e[n]$ will be identical since the quantization noise sampling will always occur in the chopped first path. However, although this solution is mismatch robust, it would result in significant in-band $1/f$ noise from the other paths, which are not chopped.

In this work, as depicted in Fig. 8(c), the two inverters are chopped at the lowest possible frequency ($f_s/26$) that modulates their $1/f$ noise outside the signal band, where it can be removed by the decimation filter. The chopping clock of the first inverter is then configured to ensure that just

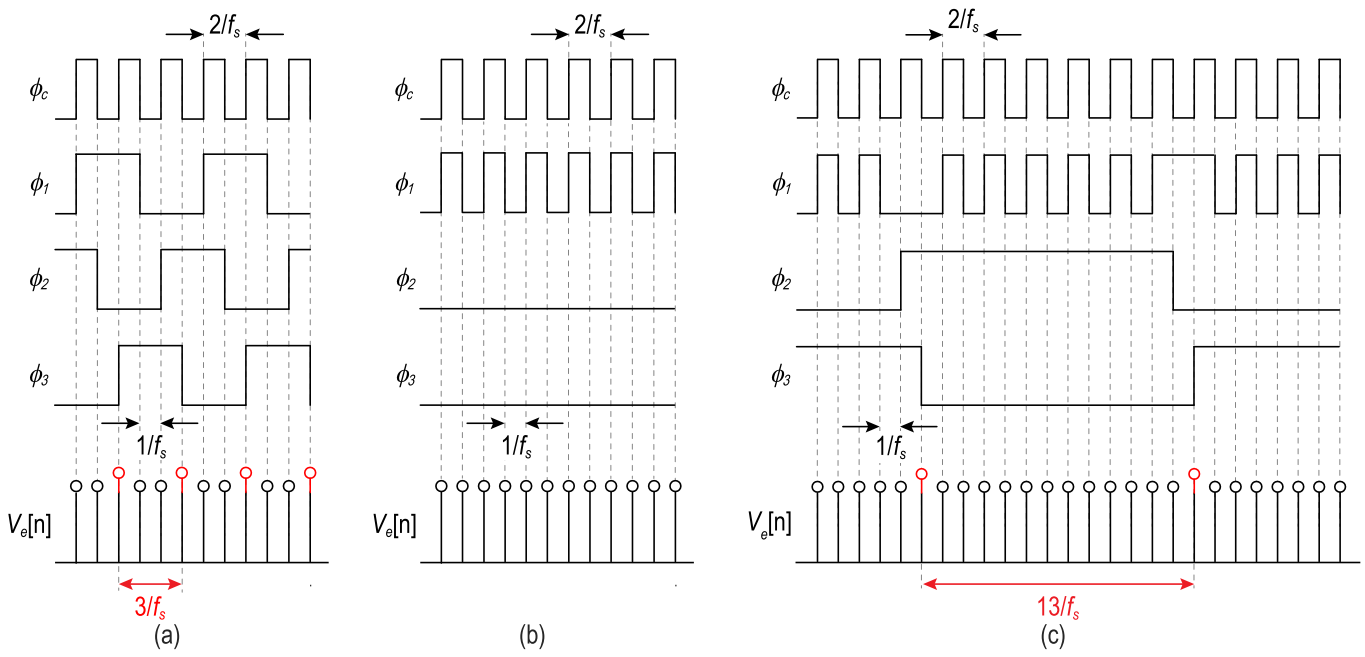

Fig. 8. (a) Conventional three-path clocking. (b) Mismatch-robust three-path clocking. (c) Proposed three-path clocking.

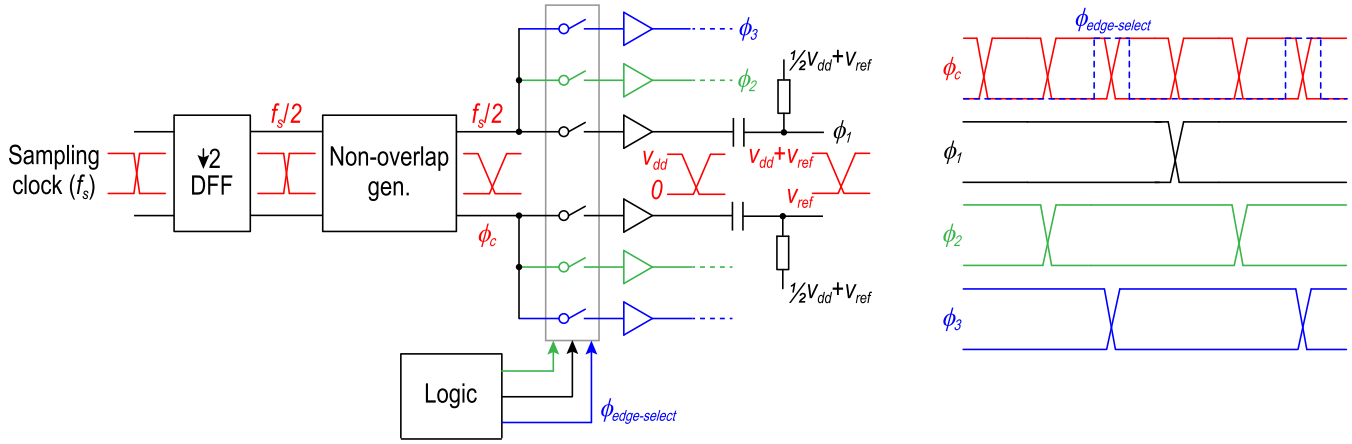

Fig. 9. Chopping clock generation.

one chopping clock edge occurs within each sampling period. The chopping clock edge will occur in the first path most of the time. Since sampling of the quantization noise happens primarily in the first path, the frequency of mismatch-related errors is reduced. For example, a mismatch in the 3rd inverter will now cause errors only once in every 13 samples instead of once in every three samples in the case of conventional multi-path clocking. This leads to quantization noise folding from multiples of $f_s/13$. However, the folding magnitude of quantization noise at these multiples is significantly lower than at multiples of $f_s/3$. In addition to the quantization noise, out-of-band interferers will also fold from multiples of $f_s/13$. As will be shown in the measurement results (Section V), this results in a 9-dB reduction in the out-of-band interferer folding level compared with conventional multi-path chopping. Since there are at least two different chopping frequencies, we will refer to this technique as multi-frequency three-path chopping.

In order to compare the performance of conventional multi-path chopping and the proposed multi-frequency chopping, a flexible clock generation block was designed to generate the required chopping clocks from the external sampling clock (f_s). As shown in Fig. 9, a fully differential D flip-flop generates the $f_s/2$ clock (ϕ_c) from the sampling clock. Noise folding due to duty cycle error is minimized by using non-overlapping clocks and positioning the chopping clock edge far from the DAC switching transient, as shown in Fig. 3. The chopping clocks for different clocking modes (ϕ_1, ϕ_2 and ϕ_3) are generated by selecting the appropriate clock edges from the $f_s/2$ clock using edge selection ($\phi_{\text{edge-select}}$). In this way, the power consumption of the logic can be minimized as the accuracy of $\phi_{\text{edge-select}}$ is not critical. As the chopping switches operate at the common-mode voltage of the amplifier V_{cm} ($=V_{\text{dd}}/2$), a level shifter is used to shift the clock levels from (0, V_{dd}) to (V_{ref}, $V_{\text{ref}} + V_{\text{dd}}$), where $V_{\text{ref}} = 0.4 \times V_{\text{dd}}$. This ensures that the gate-source voltages of all the switches

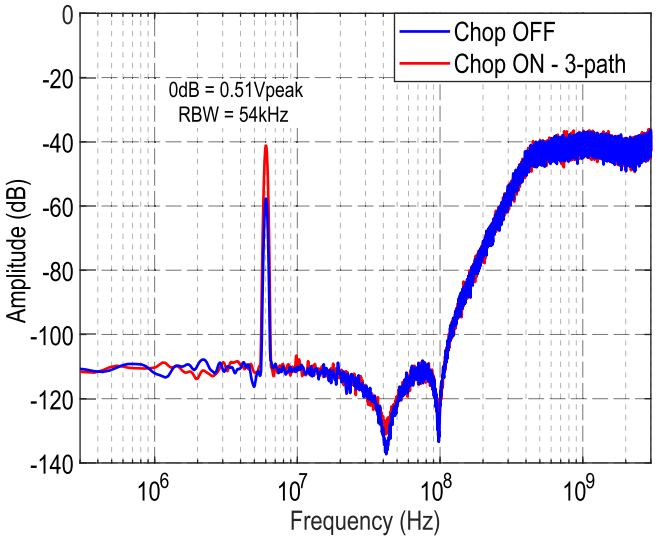

Fig. 10. Simulated output spectrum (input: 0.51 V and $f_s + 6$ MHz).

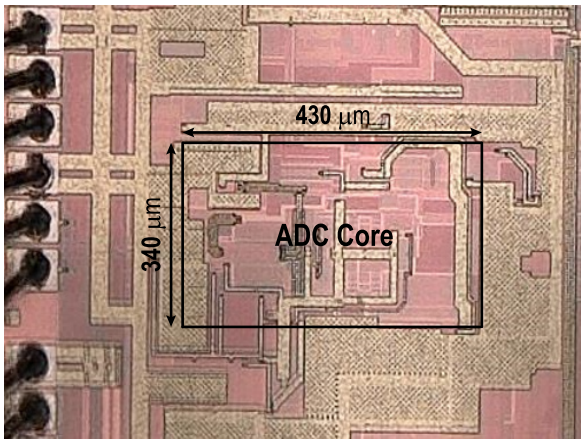

Fig. 11. Chip micrograph.

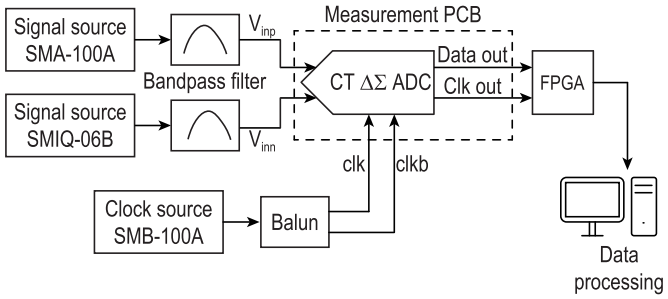

Fig. 12. Measurement setup.

are within their safe operating limits. This facilitates the use of NMOS-only chopping switches and enables smaller switch sizes for the same ON resistance. The input chopper switches are designed to minimize their thermal noise ($R_{\mathrm{ON}} \approx 8\ \Omega$) contribution, while the output chopper switches are optimized to minimize their excess parasitic delay ($R_{\mathrm{ON}} \approx 11.5\ \Omega$).

C. Alias Rejection

As discussed earlier, chopping at $f_s/2$ effectively samples the virtual ground voltage at f_s. Since the virtual ground voltage also has an input signal component, interferers at f_s will also be sampled, leading to degraded alias rejection. Fig. 10 shows the modulator's simulated output spectrum for a 0.51-V (0 dB) input signal at ($f_s + 6$ MHz). As the quantizer samples at f_s, part of this signal will be folded back to 6 MHz, resulting in limited alias rejection. Without chopping, the modulator's alias rejection is about −57.5 dB; and with three-path chopping, either with the conventional or multi-frequency clocking techniques, the alias rejection reduces to −41 dB. This can be improved by increasing the number of paths or the bandwidth of the first amplifier.

It should be noted that due to finite amplifier bandwidth, the interaction between the input signal (f_{in}) and the chopping clock will give rise to inter-modulation distortion (IMD) at $f_{\mathrm{in}} \pm nf_{\mathrm{ch}}$, where n is an even integer [18]. Since the modulator's first integrator is effectively chopped at $f_s/2$, IMD-related tones will also be folded back from multiples of f_s. However, these tones are much smaller in magnitude compared with the components resulted due to limited alias rejection.

V. Measurement Results

A. Measurement Setup

The prototype CTΔΣM is designed and fabricated in a 28-nm CMOS process with an active area of 0.15 mm^2, as depicted in Fig. 11. The CTΔΣM consumes 117.8 mA from 0.9 V and 6.6 mA from 1.35 V for the comparators. The comparator is implemented using dual differential PMOS input pairs (0.9-V core devices) with a tail current source (1.8-V device) and an NMOS latch [1]. The total power consumption, including DMUX and clock distribution, is 115 mW.

Fig. 12 shows the measurement setup used to evaluate the ADC performance. Input signals from two separate signal sources (Rohde and Schwarz SMA 100A and SMIQ-06B) were filtered through bandpass filters to remove their harmonics and achieve THD much lower than −100 dBc. Phase and amplitude mismatches introduced by the bandpass filters were removed by adjusting the relative phases and amplitudes of the signal sources. Another signal source (Rhode and Schwarz SMB-100A) generates a 6-GHz sine wave, which is then converted into a differential signal by a balun for the ADC's clock input.

B. In-Band Power Spectral Density (PSD)

Fig. 13 shows the measured in-band PSD with chopper off and chopper on, using different chopping techniques, without an input signal. With chopping off, the 1/f noise corner is at 7.8 MHz and limits the SFDR to 112 dBFS at low frequencies (150 kHz). Chopping at $f_s/2$ reduces this corner frequency to 400 kHz but increases the thermal noise floor by 1.3 dB due to the input switched-capacitor resistor. Three-path chopping reduces the 1/f noise corner to 350 kHz without increasing the thermal noise floor. Residual 1/f noise originates from the 3rd integrator and 2nd stage of the first integrator. Chopping with the conventional three-path clocks limits the SFDR performance to 113.4 dBFS due to path mismatch and the associated residual folding of the quantization noise. Chopping with the

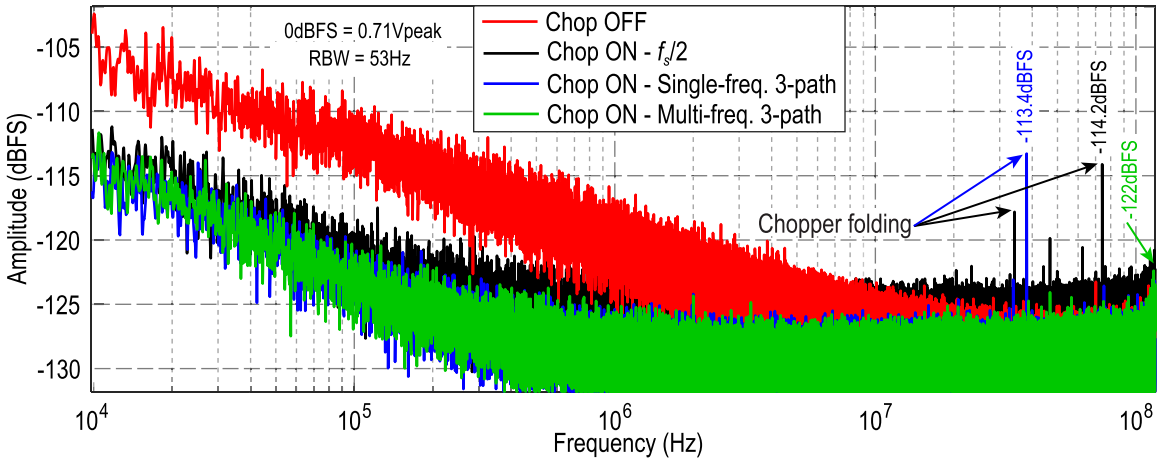

Fig. 13. Measured in-band spectra.

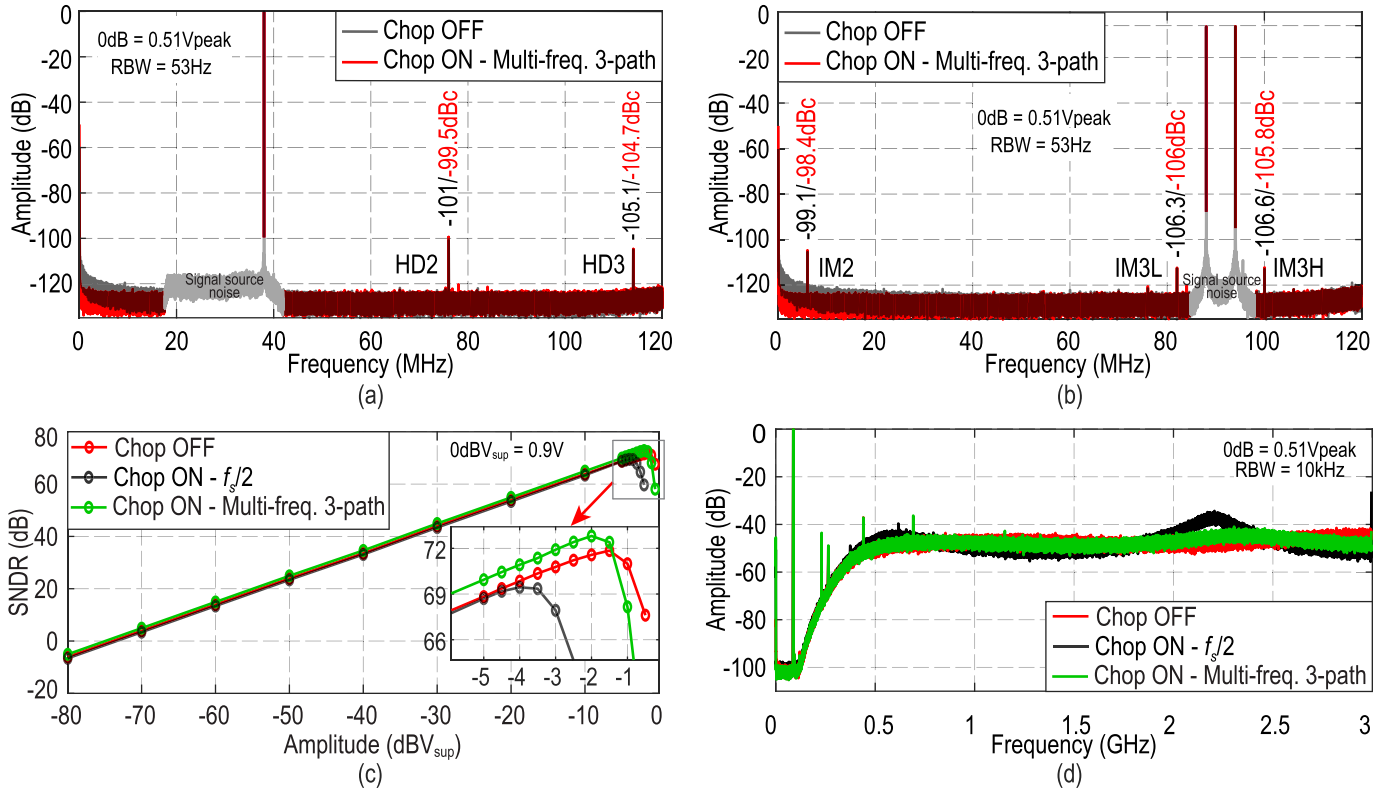

Fig. 14. (a) Measured output spectrum of a 0.51-V, 38-MHz input signal. (b) Measured output spectrum of a 0.25-V two-tone input signal at 88 and 94 MHz. (c) Measured SNDR versus input level. (d) NTF with chopping frequency.

multi-frequency clocking technique improves this significantly, resulting in an SFDR of 122 dBFS in a BW from 150 kHz to 120 MHz.

C. Linearity

The linearity of the ADC is measured with a single-tone (0 dB/−2.9 dBFS at 38 MHz) input signal with chopper off and on, as shown in Fig. 14(a). The maximum stable amplitude (MSA; 0 dBFS) is equal to −2 dBV$_{sup}$, where the nominal supply voltage (V$_{sup}$) is 0.9 V. The THD with chopper off and on is −99.6 and −98.3 dBc, respectively. The asymmetry in the noise spectrum of the signal source is due to the bandpass filter that was used to remove the harmonics from the input signal.

To measure the inter-modulation distortion (IMD), the CT$\Delta\Sigma$M is driven with a two-tone (−8.9 dBFS at 88 and 94 MHz) input signal with chopping turned on and off, as shown in Fig. 14(b). After chopping, there is a maximum degradation of 0.8 dB in the intermodulation components IM2, IM3L, and IM3H.

D. Dynamic Range

The dynamic range plot of the ADC with chopping turned on and off is shown in Fig. 14(c). Without chopping, the

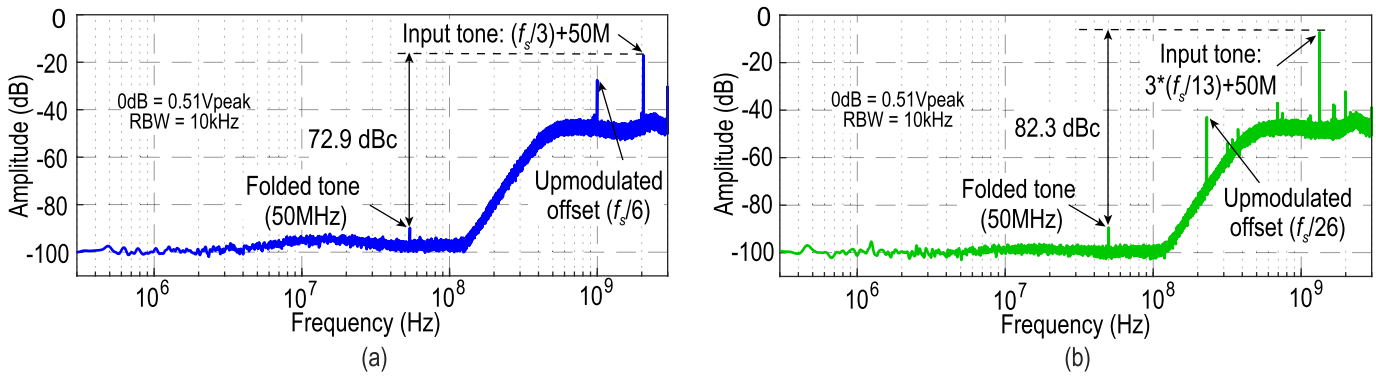

Fig. 15. Interferer folding. (a) Conventional three-path chopping. (b) Multi-frequency three-path chopping.

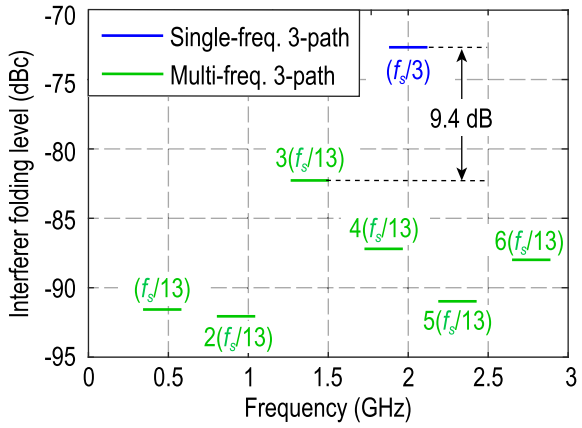

Fig. 16. Interferer folding level.

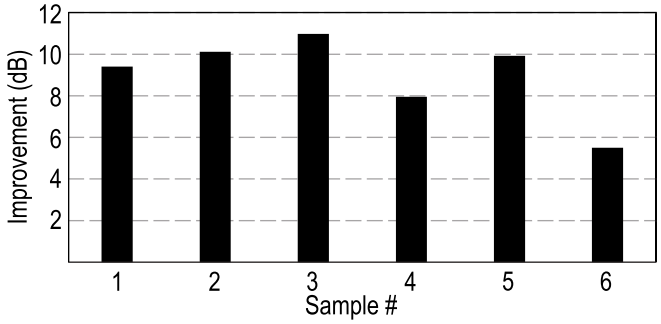

Fig. 17. Improvement in interferer folding level.

peak signal to noise and distortion ratio (SNDR) and DR are 71.8 and 73 dB, respectively, which improved to 72.8 and 73.4 dB after three-path chopping.

The out-of-band peaking observed in the NTF as shown in Fig. 14(d) may be attributed to the decreased effective gain and change in high-frequency behavior of the first integrator after chopping [Fig. 4(b)]. This peaking reduces the MSA of the CTΔΣM, which combined with an increased thermal noise floor limits the peak SNDR and DR to 69.4 and 70 dB when chopping at f_s/2.

E. Interferer Rejection Ratio

Fig. 15(a) illustrates the folding of the out-of-band interferers when using conventional three-path chopping. With a mismatch between the three inverters, interferers fold from multiples of twice the chopping frequency. Therefore, interferers fold back to in-band from multiples of f_s/3; for example, an interferer at (f_s/3) + 50 MHz folds back to 50 MHz with a folding rejection ratio of −72.9 dB, proportional to the mismatch between the paths.

Out-of-band interferer folding with multi-frequency three-path chopping is shown in Fig. 15(b). Interferers fold back to in-band from multiples of f_s/13; for example, an interferer at 3×(f_s/13) + 50 MHz folds back to 50 MHz, with a folding level of −82.3 dB.

The worst case folding level can be determined by sweeping the interferer frequency till f_s/2. The folding level can be seen in Fig. 16. When using conventional three-path chopping, there is only one folding frequency band around f_s/3, whereas multi-frequency three-path chopping introduces multiple folding frequency bands at multiples of f_s/13.

Even though interferers fold from lower frequencies with multi-frequency chopping, the folding level is significantly lower. Measurements have demonstrated that compared with conventional three-path chopping, multi-frequency chopping

TABLE I
PERFORMANCE SUMMARY

	Performance summary			
Technology (nm)	28			
Sampling freq. (MHz)	6000			
Quantizer bits	2			
DAC	Dual RTO			
Bandwidth (MHz)	120			
Chopping mode	**Multi freq. 3-path**	**Single freq. 3-path**	**1-path**	**Chop OFF**
Chopping freq. (MHz)	**f_s/26, f_s/2**	f_s/6	f_s/2	-
Peak SNDR (dB)	**72.8**	72.7	69.4	71.8
SFDR (dBFS)	**122.0**[1]	113.4[1]	114.2[1]	112.0[1,2]
THD (dBc)	**-98.3**	-98.3	-97.0	-99.6
NSD (nV/√Hz)	**11.0**	11.1	12.9	13.0
SNDR in 30MHz AM band (dB)	**78.9**	78.8	75.7	75.5
DR (dB)	**73.4**	73.3	70.0	73.0
Power (mW)	**115.0**	115.0	117.2	113.3
FoM Schreier (dB)	**163.0**	162.9	159.5	162.1

[1] SFDR is excluding harmonic distortion in a BW from 150kHz to 120MHz.
[2] Limited by FFT resolution

reduces the worst case folding levels by 9.4 dB. On average, a 9-dB improvement was seen across six different chips as shown in Fig. 17.

The measurement results are summarized and compared between various chopping techniques in Table I. The SNDR can be improved by 3.4 dB when the noise is integrated within a BW of 150 kHz-30 MHz for AM radio applications. Furthermore, the proposed multi-path multi-frequency chopping CT$\Delta\Sigma$M achieves an SFDR of 122-dBFS in the widest reported BW of 120-MHz. To emphasize broadband AM/FM radio applications, SFDR and THD are reported separately.

VI. Conclusion

Although chopping the input stage of a CT $\Delta\Sigma$ modulator at high frequencies (multiples of $f_s/2$) avoids quantization-noise folding, it can severely degrade the dynamic range and linearity of the modulator. By using a multi-path chopper amplifier, the chopping frequency of each path can be reduced while retaining interferer robustness. However, the effectiveness of this technique is limited by path mismatch. This work describes a multi-frequency three-path chopping technique implemented in a 6-GHz, 2-bit CT $\Delta\Sigma$ modulator that achieves -98.3-dBc THD and 122-dBFS SFDR in a BW of 150 kHz-120 MHz. Compared with the use of conventional multi-path chopping, its sensitivity to mismatch is improved by using different clocks for each channel, such that most of the chopping edges occur in one path, while still emulating $f_s/2$ chopping by ensuring that one chopping clock edge always occurs in each sampling period. Measurements show that the proposed technique achieves an 8.5-dB improvement in SFDR and a 9-dB improvement in its out-of-band interferer folding level. With the $1/f$ noise corner frequency reduced to 350 kHz, the ADC can be also used in AM radio applications enabling a 3.4-dB improvement in SNDR in a BW of 150 kHz-30 MHz.

Acknowledgment

The authors would like to thank Paul Swinkels, Willem Jan Wagenaar, Athon Zanikopoulos, G. Ranjith, Nico Morskieft, Ferdinand Manalac, M. A. Kalpashree, Tanmeet Kaur, Ivaylo Bakalski, Jocelyn Cahigas, Vijayanthi Venkatesh, Yihan Gao, Hans Brekelmans, Pierluigi Cenci, Bernard Burdiek, and Marcello Ganzerli.

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