Characterization and modeling of mismatch in Cryo-CMOS

Hart, P. A.R.; Babaie, M.; Charbon, E.; Vladimirescu, A.; Sebastiano, F.

DOI
10.1109/JEDS.2020.2976546

Publication date
2020

Document Version
Final published version

Published in
IEEE Journal of the Electron Devices Society

Received 24 December 2019; accepted 22 February 2020. Date of publication 27 February 2020; date of current version 10 March 2020.
The review of this article was arranged by Editor M. J. Kumar.

Digital Object Identifier 10.1109/JEDS.2020.2976546

Characterization and Modeling of Mismatch in Cryo-CMOS

P. A. 'T HART [1], M. BABAIE [1] (Member, IEEE), EDOARDO CHARBON [2] (Fellow, IEEE), ANDREI VLADIMIRESCU[1,3,4] (Life Fellow, IEEE), AND FABIO SEBASTIANO [1] (Senior Member, IEEE)

1 Department of Quantum and Computer Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands
2 Advanced Quantum Architectures Laboratory, EPFL, 2002 Lausanne, Switzerland
3 Micro-Nano Electronics and Radio Communications, Institut supérieur d'électronique de Paris, 75006 Paris, France
4 Berkeley Wireless Research Center, University of California at Berkeley, Berkeley, CA 94708, USA

CORRESPONDING AUTHOR: P. A. 't HART (e-mail: p.a.thart@tudelft.nl)

ABSTRACT This paper presents a device matching study of a commercial 40-nm bulk CMOS technology operated at cryogenic temperatures. Transistor pairs and linear arrays, optimized for device matching, were characterized over the temperature range from 300 K down to 4.2 K. The device parameters relevant for mismatch, i.e., the threshold voltage and the current factor, were extracted, from which the change in both absolute value and variability as a function of temperature and device size were investigated. It is shown that the Pelgrom scaling law is valid also at 4.2 K and that the simplified Croon model is able to accurately predict drain-current mismatch from moderate to strong inversion over the entire temperature range. Additionally, the characterization of linear device arrays shows exacerbated edge-effects at extremely low temperatures, thus requiring the addition of dummy devices at the array boundary. The result of this study is the first model capable of predicting mismatch over a wide range of operating regions and temperatures.

INDEX TERMS Mismatch, cryogenics, MOSFETs, Cryo-CMOS, modeling, stress, quantum computing.

I. INTRODUCTION

Quantum computers exploit quantum phenomena to solve computational problems that are intractable even by today's most powerful supercomputers. The essential computing elements of any quantum computer, the quantum bits (qubits), must be typically cooled to deep-cryogenic temperatures (10-100 mK) for proper operation and therefore must reside in dilution refrigerators. Although the actual computations are carried out by the qubits, classical electronics are still required to keep qubits in a coherent state and to perform operations on the qubits as well as to readout their state. Today, such an electronic interface is implemented by standard instrumentation equipment at room temperature (RT, 300 K) and long cables running through the refrigerator propagate the electric signals from and to each of the qubits. Such interconnect strategy is feasible for the few qubits (<100) available today but poses severe limits in terms of reliability and cost when scaling up to the thousands or even millions of qubits required in the future practical quantum computers [1]. In order to overcome the above mentioned challenges, the classical control interface must operate in close vicinity to the qubits and hence also at cryogenic temperatures down to the liquid-helium temperature (LHT, 4.2 K) and below. CMOS operating at cryogenic temperature (cryo-CMOS) is the preferred electronic technology thanks to its maturity, high level of integration and speed, as required for handling the narrow voltage/current pulses and microwave signals employed to control millions of qubits [1]–[7].

For the reliable design of a such controller, device models, able to predict device behavior at cryogenic temperatures, are indispensable. Effort has already been dedicated to create DC models valid in the temperature range from RT down to LHT [8]–[11]. However, device mismatch at extremely low temperatures has not gained much attention up until now.

Device mismatch can have severe detrimental effects on the performance of sensitive circuits, such as data converters and on-chip references, that are an integral part of the cryogenic controller. Mismatch has been extensively investigated over the military temperature range (−55–125°C) [12]–[14], indicating a degradation of matching at lower temperature,

which, when extrapolated, suggest mismatch effects exacerbated at cryogenic temperatures. Cryogenic experiments indeed confirm this assumption by showing an increase in the variability of the current factor (β), the threshold voltage (V_{TH}) and the drain-current (I_D) for 0.5-µm Silicon on Sapphire (SOS) CMOS devices at LHT [15] and for 0.35-µm bulk CMOS devices at 5 K [16]. However, only [17] (of which this paper is an extension) focused on the cryogenic characterization of mismatch in an advanced nanometer CMOS technology, typically required in the interface for a quantum processor.

To bridge this gap, this work reports the characterization over the temperature range from RT down to LHT of N- and PMOS device pairs with 8 different geometries manufactured in a commercial 40-nm bulk CMOS technology. The variability of the device parameters relevant for mismatch analysis, i.e., β and V_{TH}, have been extracted and their behavior over temperature and device area has been investigated, demonstrating that the Pelgrom model [18] holds for nanometer CMOS down to LHT. With the use of these parameters, a drain-current mismatch ($\sigma_{\Delta I_D/I_D}$) model valid from moderate to strong inversion is validated against measurements. This analysis is extended beyond the characterization of simple device pairs by experimentally studying the LHT mismatch in large arrays of matched devices and assessing the effect of dummy devices at the array edges.

This paper is structured as follows. In Section II a description of the experimental setup and of the parameter extraction algorithms is given. Section III details the methods employed for the mismatch analysis. The measurement results are presented in Section IV and the results are discussed in Section V. Conclusions are drawn in Section VI.

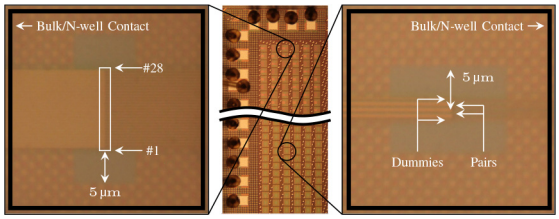


FIGURE 1. Die micrograph (*center*) with zoomed detail. *Left*: matched-device array; *right*: matched pair.

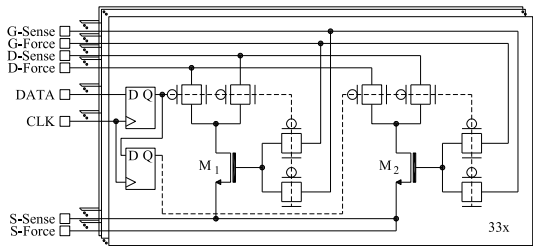


FIGURE 2. Simplified schematic of the circuit used to measure the matched pairs (M_1 and M_2). Arrays comprise 14 such circuits.

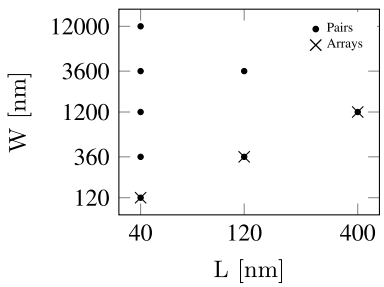


FIGURE 3. Device geometries available for mismatch and dummy/stress characterization.

II. EXPERIMENTAL SETUP AND METHODS

A. EXPERIMENTAL SETUP

Measurements have been carried out on 3 dies manufactured in a commercial 40-nm bulk CMOS process comprising low-threshold-voltage (LVT) 1.1-V N and PMOS devices. The two types of test structures are highlighted in the die micrograph of Fig. 1: the device pairs, designed for mismatch characterization and the linear device arrays, targeted at edge effects.

All the devices share a common source connection while the drain and gate connections can be independently enabled by means of transmission gates, as depicted in the block diagram of Fig. 2. Each transmission gate can be individually enabled by a latched shift register, which is daisy-chained to form a chip-level shift register. The voltage drop across the cables, bondwires and transmission gates was mostly compensated for by using Kelvin connections up to the source and drain diffusions of the devices.

Each die contains devices with 8 different geometries, as summarized in Fig. 3. For each geometry, 33 device pairs per die with dummies placed on both sides (to mitigate stress effects) were available. The linear arrays consist of 28 devices placed at the minimum allowable distance in a single row. No dummy transistors were placed adjacent to the first (device #1) and last device (device #28) in each array. A total of 9 arrays per die were available for each of the array geometries described in Fig. 3. Unless specifically mentioned, metal fillers were kept away further than 5 µm from the active devices in the pairs and arrays to minimize the effect of metal coverage, stress and asymmetries on device matching.

For the electrical characterization, Keithley 2636B Source Measurement Units (SMUs) were used to force voltages at the source, drain and gate terminals and record the drain current. To allow for the measurement of low currents, active guarding in combination with triaxial cabling was employed. In all the experiments, the drain current (I_D) as a function of gate voltage (V_G) was measured by electrically shorting the source voltage to the bulk, i.e., to 0 V for the NMOS and to 1.1 V for the PMOS and setting the drain-source voltage to $|V_{DS}| = 50$ mV and to $|V_{DS}| = 1.1$ V for operation in triode or saturation, respectively.

All devices were measured sequentially in a 3-step procedure: 1) after selecting the target transistor by shifting the correct bit pattern into the shift register, the I_D-V_G curve is

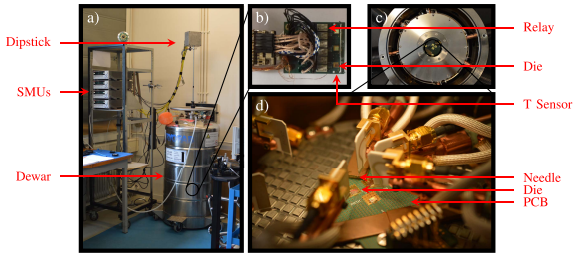


FIGURE 4. Measurement setup. a): dipstick; b) detail of PCB on the dipstick. The temperature sensor (Cernox RTD) is located on the opposite side of PCB. Relays used for die selection; c) cryogenic probestation; d) detail of the PCB in the cryogenic probestation.

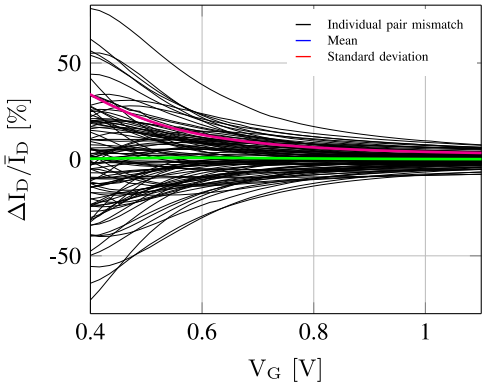


FIGURE 5. Drain-current mismatch per device pair for 99, W/L = 360n/120n NMOS pairs. Ensemble mean (green) and standard deviation (magenta) indicated.

measured; 2) the same measurement is carried out a second time; 3) all devices are de-selected by shifting in an all-0 pattern and the measurement is carried out a third time. The measurement in step 1 is the actual measurement used for the analysis, while the measurement in step 2 is done to check the Short-Time-Repeatability (STR) of the characterization, which is an indication of the reliability of the experiment and is used to guard against measurement errors due to bad contacts, sudden (unintended) temperature changes and interference. The STR is always below 0.2% over the bias range, thus not significantly impacting measurement results. The measurement in step 3 quantifies the leakage current (∼200 nA @ 300 K) due to the large number (5136) of transmission gates connected in parallel and it is required to compensate for such leakage in order to extend the measurement range to lower current levels. Since the transmission-gate leakage is weakly bias and temperature dependent, a residual error remains after compensation. By discarding measured data for too low drain current, it was ensured that the leakage-induced error was always below 10%.

Three dies were glued and wire-bonded to a PCB that was either placed in a Lakeshore CPX cryogenic probestation equipped with Lakeshore model-336 temperature controllers, or on a dipstick inserted into a dewar containing liquid helium for cryogenic cooling, see Fig. 4. Ambient temperature was continuously monitored during the measurement, to ensure that the temperature had settled and that the temperature difference between the measurement of each device in a pair was below 5 mK.

B. PARAMETER EXTRACTION PROCEDURE

From the measured $I_D - V_G$ data, the threshold voltage (V_{TH}) and the current factor (β) were extracted via the maximum-G_m method [19]. Although the long-channel approximation used by this scheme may not be the most appropriate choice for advanced technology nodes, it extracts the parameters at a point derived from the data itself, i.e., the bias point with the maximum transconductance G_m. This is an advantage over the other two well-known extraction methods, i.e., the constant current [19] and the 3-point [20] method, that either rely on an arbitrary target current or on multiple points chosen on the $I_D - V_G$ curve. Moreover, since this work is mainly concerned with parameter mismatch, the extraction of the actual physical parameter value is of minor importance. Mismatch is extracted accurately as long as the parameters are derived in a reliable and repeatable way for every device [21].

Following the extraction of V_{TH} and β for each pair, their mismatch (ΔV_{TH} and $\Delta\beta/\beta$) and their variability, i.e., their standard deviation $\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\beta}$, are calculated from a sample size of 99 device pairs. The error bars in the following plots indicate 95% confidence intervals. Only for the geometries used for both the pairs and the arrays (see Fig. 3), a sample size of 351 is employed by also exploiting the devices in the array, thus resulting in a better statistical accuracy. For the arrays 27 devices per position were considered. The resulting $\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\beta}$ are used as input to the Croon model to compute the drain-current mismatch $\sigma_{\Delta I_D/I_D}$ (see Section III-B) [22].

III. MISMATCH ANALYSIS

A. DRAIN-CURRENT MISMATCH

When a single transistor pair (M_1, M_2) is considered, its drain-current mismatch can be defined as follows:

$$\frac{\Delta I_D}{\bar{I}_D} = \frac{2\left(I_{D_1} - I_{D_2}\right)}{I_{D_1} + I_{D_2}}, \tag{1}$$

where the overbar is the average value operator and the subscript indicates the first or second device of a pair.

Two different types of mismatch can be distinguished: systematic and random mismatch. Systematic mismatch arises from any asymmetry between the devices of a pair, e.g., when paired devices are (partially) covered by metal, have different proximity to wells or have their drain-current flowing in different directions. These sources of mismatch can be minimized by careful layout. Random mismatch can be mostly attributed to microscopic variations, e.g., Random Dopant Fluctuation (RDF), Line Edge Roughness (LER) of the gate and Oxide Thickness Variation (OTV) [23], which are inevitably introduced during manufacturing and cannot be compensated at design time. In

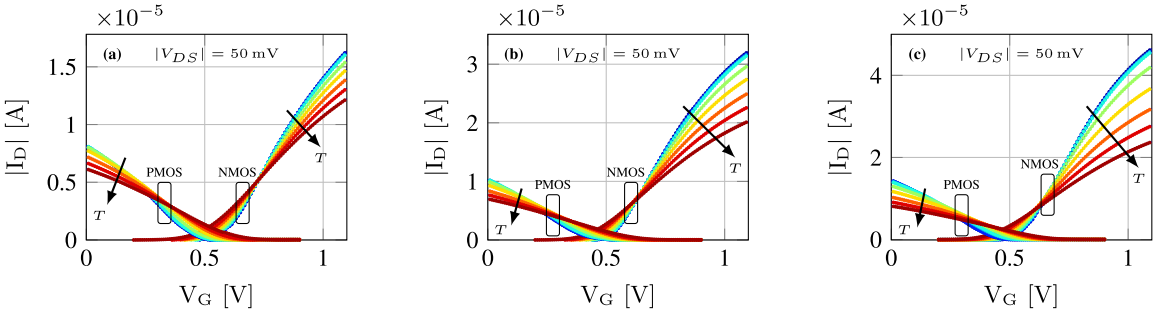


FIGURE 6. $I_D - V_G$ curves as function of temperature for: a) NMOS/PMOS W/L = 120n/40n; b) NMOS/PMOS W/L = 360n/120n and c) NMOS/PMOS W/L = 1.2µ/400n. T = 4.2, 10, 40, 50, 100, 150, . . . , 300 K. V_S = 0 V and V_S = 1.1 V for NMOS and PMOS, respectively.

this work, care was taken to minimize any systematic mismatch in the device-pair structures, so as to accurately characterize the random mismatch. At the same time, the array structures are used to characterize some systematic effects.

As an example, the drain-current mismatch of 99 NMOS device pairs (W/L = 360n/120n) measured at RT is plotted in Fig. 5, together with its ensemble mean and standard deviation curves. The mean value of the drain-current mismatch is close to 0 over the full operating range, well within the margin of both the experimental and the statistical inaccuracy. This indicates a mismatch dominated by random, rather than systematic variation, thus validating the experimental approach. Similar considerations apply to the other pair geometries.

B. MISMATCH MODELING

In order to provide designers of cryogenic circuits with the ability to predict device variability, the Croon model is used for drain-current mismatch [22]:

$$\sigma^2_{\Delta I_D/\bar{I}_D} = \sigma^2_{\Delta\beta/\bar{\beta}} + \left(\frac{G_m}{\bar{I}_D}\right)^2 \sigma^2_{\Delta V_{TH}}, \tag{2}$$

where σ is the standard deviation operator and G_m is the transconductance.

This model is based on a Taylor expansion of the drain current expressed as:

$$I_D = \beta f(V_{GS} - V_{TH}), \tag{3}$$

with $f(\cdot)$ an arbitrary function and $G_m = \partial I_D/\partial V_{GS}$.

The well-known area dependence of the threshold-voltage and current-factor variability is described by the Pelgrom law [18]:

$$\sigma_{\Delta V_{TH}} = \frac{A_{VTH}}{\sqrt{WL}} \quad \sigma_{\Delta\beta/\bar{\beta}} = \frac{A_\beta}{\sqrt{WL}}, \tag{4}$$

where A_{VTH} and A_β are technology-dependent factors and W and L are the active device width and length, respectively.

Eq. (2) and (4) were first validated with cryogenic measurements, after which the temperature dependent $\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\bar{\beta}}$ interpolated from Eq. (4) were fed into Eq. (2) to form a full mismatch model.

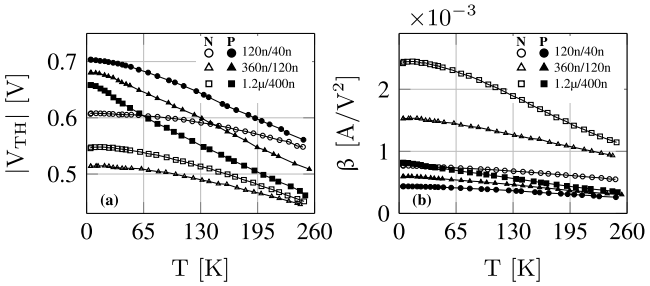


FIGURE 7. Threshold voltage (a) and current factor (b) as a function of temperature for NMOS and PMOS devices with different geometries.

IV. MEASUREMENT RESULTS

This Section describes the measured data and observations for individual devices, device pairs and device arrays, from which new insights are gained for mismatch of transistor pairs and the impact of layout and placement for transistor arrays.

A. CRYOGENIC TRANSISTOR BEHAVIOR

Fig. 6 shows typical $I_D - V_G$ curves obtained at various temperatures between RT and LHT by averaging data measured from the 99 device pairs for each of the 3 reported geometries. To further investigate the temperature dependence of V_{TH} and β, these parameters were extracted at different temperatures, see Fig. 7. As expected, both a V_{TH} (Fig. 7a) and β (Fig. 7b) increase for both NMOS and PMOS devices was observed when temperature is decreased. Both parameter values saturate below approximately 40 K.

Devices in this technology did not show any specific cryogenic non-idealities, such as the "kink-effect", i.e., a sudden increase in I_D at high $|V_{DS}|$ and $|V_{GS}|$, or hysteresis in the $I_D - V_D$ or $I_D - V_G$ characteristics. This matches the expectations of [11], which predicts the absence of such effects in nanometer CMOS. Those effects are mainly due to a combination of the increased impact ionization and of the higher bulk resistivity at cryogenic temperatures, which are mitigated in nanometer CMOS by the increased doping levels, by the lower mobility due to higher vertical electric fields and, more relevantly, by the lower supply voltage [11].

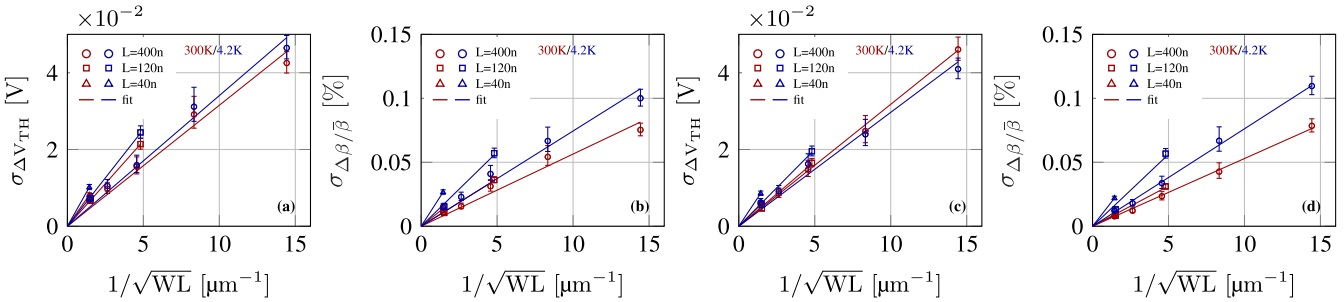


FIGURE 8. Pelgrom plots for V_{TH} and β with length dependency indicated by separate fitting for each length at RT (red) and LHT (blue). a), b) NMOS; c), d) PMOS. Error bars indicate 95% statistical confidence intervals.

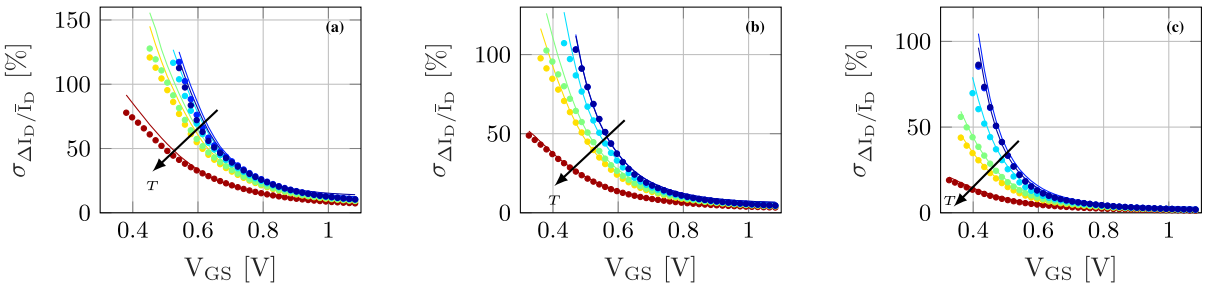


FIGURE 9. Drain-current mismatch for NMOS devices as a function of temperature (V_{DS} = 50 mV). T = 4.2, 40, 100, 150, 200 and 300 K. a) W/L = 120n/40n; b) W/L = 360n/120n; c) W/L = 1.2µ/400n. Dots: measured data; lines: simplified Croon model as in Eq. (2).

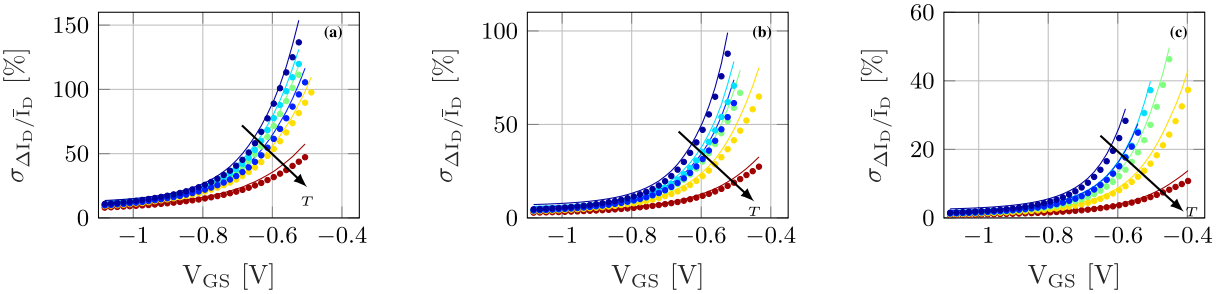


FIGURE 10. Drain-current mismatch for PMOS devices as a function of temperature ($|V_{DS}|$ = 50 mV). T = 4.2, 40, 100, 150, 200 and 300 K. a) W/L = 120n/40n; b) W/L = 360n/120n; c) W/L = 1.2µ/400n. Dots: measured data; lines: simplified Croon model as in Eq. (2).

TABLE 1. Scaling factors as function of temperature and device length in [m], 95% confidence interval indicated.

T [K]	A_{VT} [mV · µm]						A_β [% µm]					
	NMOS			PMOS			NMOS			PMOS		
	40n	120n	400n	40n	120n	400n	40n	120n	400n	40n	120n	400n
300	3.2 ±0.2	4.5 ±0.2	5.7 ±0.3	3.2 ±0.1	3.4 ±0.2	3.9 ±0.3	5.6 ±0.2	7.4 ±0.4	9.5 ±0.5	5.3 ±0.3	6.3 ±0.3	6.0 ±0.4
4.2	3.4 ±0.2	5.0 ±0.3	7.0 ±0.4	3.0 ±0.1	4.0 ±0.2	5.9 ±0.4	7.4 ±0.3	11.6 ±0.7	18 ±1	7.6 ±0.4	11.3 ±0.6	15 ±1

B. TRANSISTOR PAIRS

The extracted $\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\bar{\beta}}$, are plotted as a function of device geometry for both RT and LHT in the Pelgrom plots in Fig. 8. The geometries have been grouped according to device length into 3 bins (L = 40nm, 120 nm and 400 nm) to highlight the length dependency of the A-factors.

Pelgrom's law was fit to the measured data using a linear fitting weighted by the error bars. The resulting A_{VT} and A_β values are reported in Table 1. It can be concluded that variability of both parameters increases at LHT compared to RT and that Pelgrom's law is valid at both temperatures with increased A-factors at cryogenic temperatures. The $\sigma_{\Delta V_{TH}}$ increase is statistically less significant if compared to $\sigma_{\Delta\beta/\bar{\beta}}$, as error bars in Fig. 8a and c are partially overlapping. This is reflected especially in the A_{VT} of the smallest geometry as can be seen in the confidence intervals reported in Table 1. If RT and LHT A-factors are compared by averaging their increase over the 3 geometries and 2 device types, it becomes clear that A_β shows the largest temperature variations (+75%) with respect to

A_{VT} (+22%). The A-factor length dependency is particularly significant for β, increasing in value as devices become longer.

Mismatch fluctuation sweeps [14] for devices at different temperatures between LHT and RT are shown in Fig. 9 and Fig. 10. With these data, the performance of the measurement setup was assessed by comparing the standard deviation of the 300 K data with Monte Carlo simulations generated using the model provided by the foundry, which resulted in less than 13% deviation over the plotted range. Drain-current mismatch was found to increase with decreasing $|V_{GS}|$ for all temperatures. When temperature is decreased from RT to LHT, mismatch increases in all operating regimes from moderate to strong inversion. Over the reported temperature range, matching can deteriorate up to 10× in moderate inversion, if evaluated at equal $|V_{GS}|$ (Fig. 9c). In all the 6 plots, the model in Eqn. (2) using the above-mentioned parameters ($\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\bar{\beta}}$ in Fig. 8) is superimposed on the experimental data. The model is able to predict the measured data over all the measured geometries and temperatures by using the *unmodified*, extracted $\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\bar{\beta}}$ values, without employing any fitting.

C. TRANSISTOR ARRAYS

Dummy devices are routinely placed adjacent to matched devices in order to mitigate edge and stress effects and improving the overall geometrical symmetry of these structures, thereby improving matching. As matching deteriorates at cryogenic temperatures, it is worthwhile to investigate the effect of dummy devices on parameter variability at these low temperatures. This is especially interesting, as an increase in mechanical-stress-induced mismatch can be expected due to a significant thermal expansion/contraction at very low temperatures [24]. For this experiment I_{DSAT}, V_{TH} and β were extracted from devices placed in linear arrays.

In Fig. 12 and Fig. 13, I_{DSAT} ($I_D|_{|V_{GS}|,|V_{DS}|=1.1\ \mathrm{V}}$) is plotted as a function of device position for NMOS and PMOS devices. The values at RT and LHT are normalised to the corresponding median value to enable a comparison between the two temperatures. A variability increase for both NMOS and PMOS devices can be recognized by elongated error bars, both when temperature and the device area are decreased. Considering the NMOS devices in Fig. 12, the effect of array position starts to become significant only for large devices, while it is overshadowed by random mismatch for smaller devices. A significantly larger I_{DSAT} for the two outer devices (position #1 and #28) can be seen in Fig. 12c, although a clear temperature dependence is not visible.

Compared to NMOS, the PMOS devices in Fig. 13 exhibit larger and opposite sensitivity to placement in the array. Significant I_{DSAT} changes are visible in the outer devices for both medium (Fig. 13b) and large sizes (Fig. 13c) at both RT and LHT. When the structures are cooled down to LHT, I_{DSAT} of these outer devices changes by a factor of approximately 2 compared to RT. A statistically significant deviation of the drain current of the outer device is also visible for the small devices (Fig. 13a), but to a lesser extent.

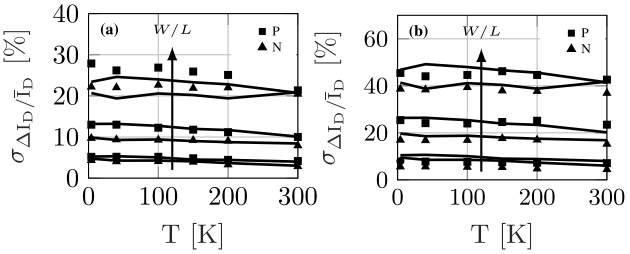


FIGURE 11. Drain-current mismatch as a function of temperature at a fixed g_m/I_D in saturation (V_{DS} = 1.1 V). a) g_m/I_D = 5 V^{-1}; b) g_m/I_D = 10 V^{-1}. Marks: measured data, lines: simplified Croon model as in Eq. (2). Arrow points in direction of decreasing W/L: 1.2 µ/40n, 360n/120n and 120n/40n.

To gain more insight into the physical mechanisms at play, the extracted (normalised) V_{TH} and β are plotted at both RT and LHT for both NMOS and PMOS devices in Fig. 14 and Fig. 15.

These devices show an average V_{TH} increase of ∼100 mV for NMOS and ∼180 mv for PMOS devices, respectively, and a β improvement by a factor of 1.3 to 1.5 at LHT compared to RT, depending on geometry.

Starting with RT data, the small and medium NMOS devices shown in Fig. 14a, b, g and h do not exhibit significant changes at the edge of the array. For the largest geometry, a significant 1% increase in β can be observed at device positions #1 and #28 in Fig. 14i, while the V_{TH} is not affected. Similar results are found for NMOS arrays cooled down to LHT in Fig. 14.

PMOS devices start to show very significant sensitivity to array position for geometries larger than W/L = 360n/120n, as plotted in Fig. 15. Considering minimum size devices at RT, only device position #1 (Fig. 15g) shows a clear deviation from the median, while this is not the case for LHT (Fig. 15j) or other positions. Therefore this is not considered a dummy effect. The medium and large geometries at RT exhibit a significant β decrease (∼1%) in positions #1 and #28 as seen in Fig. 15h and i. The effect is stronger at LHT (Fig. 15k and l), where β decreases with ∼3.3% for the outermost devices. For these positions there is also a slight V_{TH} increase, especially for the largest device with an increase of ∼2 mV at RT and ∼3 mV at LHT.

V. RESULT INTERPRETATION

The increased drain current at high $|V_{GS}|$ in Fig. 6 is related to the competing cryogenic effects of β and V_{TH} increase. The improved mobility, due to reduced phonon and increased Coulomb scattering at cryogenic temperatures [25], directly relates to an increase of β, improving current drive. Conversely the V_{TH} increase lowers the drain current and is mainly the result of bandgap widening and Fermi-Dirac scaling at deep-cryogenic temperatures [26]. Depending on

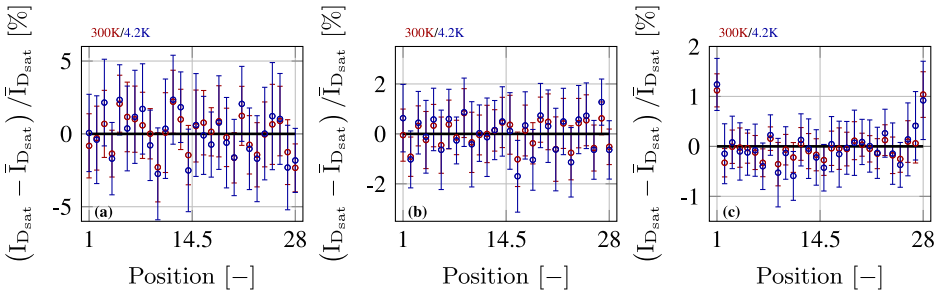


FIGURE 12. Relative $I_{D_{sat}}$ ($I_D|V_{DS}=V_{GS}=1.1$ V) values as a function of device position for NMOS devices at RT (red) and LHT (blue): a) W/L = 120n/40n; b) W/L = 360n/120n and c) W/L = 1.2µ/400n. Zero deviation emphasized by the black lines and error bars indicate 95% confidence intervals.

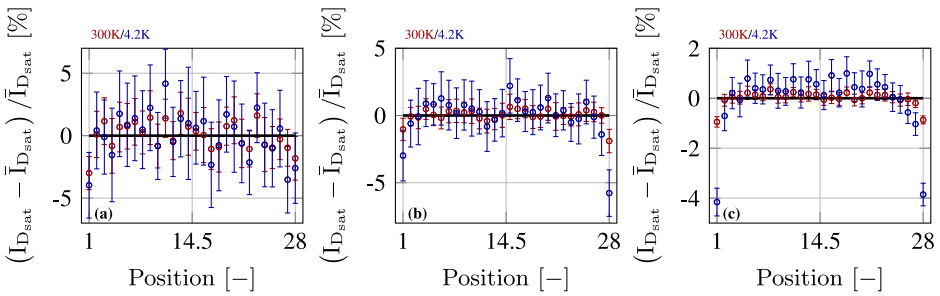


FIGURE 13. Relative $I_{D_{sat}}$ ($I_D|V_{DS}=V_{GS}=1.1$ V) values as a function of device position for PMOS devices at RT (red) and LHT (blue): a) W/L = 120n/40n; b) W/L = 360n/120n and c) W/L = 1.2µ/400n. Zero deviation emphasized by the black lines and error bars indicate 95% confidence intervals.

the operating regime, either V_{TH} (moderate inversion, MI) or β (strong inversion, SI) governs the drain-current behaviour and the cross-over point, where the two effects cancel, is approximately temperature insensitive, as visible in Fig. 6. The drain current saturates close to 4.2 K, visible when zooming into Fig. 6, which is compatible with the flattening of V_{TH} and β curves visible in Fig. 7, also shown in [26].

The V_{TH} variability increase at cryogenic temperatures in Fig. 8a and c can be attributed to charge trapping in shallow traps at the Si/insulator interface, which due to the low carrier energy at LHT, remain trapped and perturb V_{TH} [15]. β variability increase can be attributed to the above mentioned shift from phonon-dominated scattering to impurity (dopant) scattering, which is a major contributor to mobility fluctuations [14]. It can be concluded from the data in Fig. 8 and Table 1 that mobility fluctuations are impacted at cryogenic temperatures much more strongly than threshold-voltage fluctuations.

The observed length dependency of the A-factor, visible in Fig. 8 and Table 1, can be attributed to halo/pocket implants employed to mitigate short-channel effects. Although these implants degrade matching because of RDF by increasing the doping concentration (RDF), this mechanism is not strongly concentration dependent [23]. However, due to the strong control of device electrostatics in the heavily doped pockets, the area where fluctuation impact device behavior is reduced, increasing mismatch [27]. The observed effects are in agreement with the data supplied by the foundry for RT.

The drain-current mismatch increase for lower $|V_{GS}|$ (Fig. 9 and Fig. 10), observed for all temperatures and devices, is due to the higher G_m/I_D when moving towards weak inversion (WI), which modulates the V_{TH} variability contribution in Eqn. (2). The increase of $\sigma_{\Delta I_D/\bar{I}_D}$ with decreasing temperature for a fixed V_{GS} bias is mainly caused by the V_{TH} increase (Fig. 7), since a higher V_{TH} reduces the gate overdrive and shifts the device operating region towards WI, where drain-current mismatch is inherently larger, as explained above. As the subthreshold slope (SS) is enhanced at cryogenic temperatures [11], G_m/I_D is higher at lower temperature, thus increasing the impact of the $\sigma_{\Delta V_{TH}}$ term even more.

To investigate the effect of biasing and to indicate possible techniques that mitigate mismatch for cryogenic circuit design, $\sigma_{\Delta I_D/\bar{I}_D}$ has been plotted at two different G_m/I_D values as a function of temperature in Fig. 11. As the G_m/I_D term is kept constant, the only deterioration observed when the temperature is reduced from RT to LHT is caused by the temperature dependence of the parameter variability. In these bias regions, it is mainly the V_{TH} variability that controls drain-current mismatch, which does not increase by more than 1.2×, in agreement with the extracted increase of $\sigma_{\Delta V_{TH}}$ over this temperature range.

The sensitivity of I_{DSAT} to dummy placement in Fig. 12 and Fig. 13 is found to be opposite for NMOS and PMOS. This points to an effect of piezo-resistive origin, whose coefficients have typically different signs for n- and p-type silicon [28]. The effect alters mobility as a function of

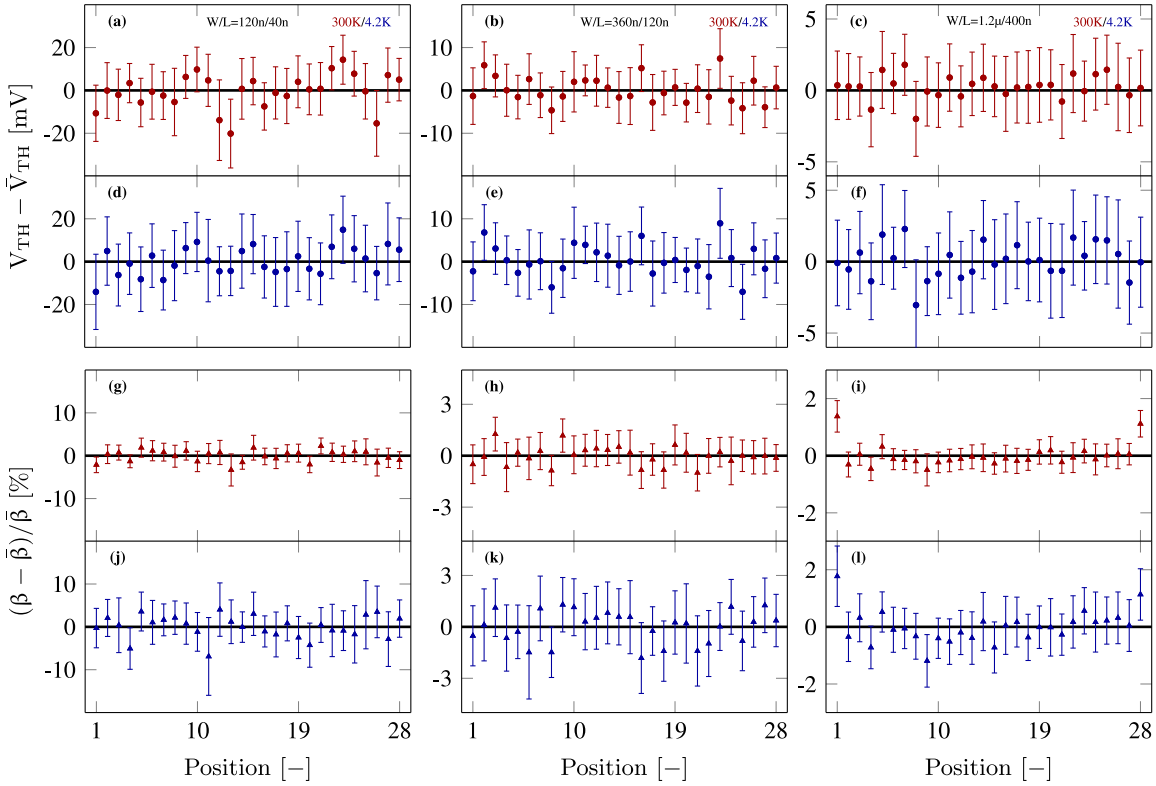


FIGURE 14. **Normalised V_{TH} (circle) and β (triangle) as a function of device position for NMOS devices at RT (red) and LHT (blue). First column: W/L = 120n/40n; second column: W/L = 360n/120n; third column: W/L = 1.2µ/400n. Error bars indicate 95% confidence intervals.**

mechanical stress originating from, for example, Shallow Trench Isolation (STI) surrounding each device. The effect of STI stress on MOSFETs has been known for years [29] and has been widely reported as compressive in nature, enhancing hole- and deteriorating electron-mobility [30], [31]. However, an increase in NMOS and decrease in PMOS I_{DSAT} observed in these measurements is opposite to what is typically reported. The piezo-resistive effect is highly anisotropic, resulting in changes in electron- or hole-mobility with any combination of sign, depending on crystal, device-current and stress orientation [32]. Unfortunately, the device orientation with respect to the crystal for the transistor pairs/arrays is not known. Additionally, prior works also report deviations from the often encountered compressive, longitudinal (i.e., parallel to device current), uni-axial stress. In [24] it is shown that apart from the longitudinal stress component also the transverse component needs to be taken into account, which, if compressive, can degrade PMOS mobility. In [33] PMOS insensitivity to STI stress is reported, which was attributed to the wafer crystal orientation. The device arrays characterized in this work are placed in a rectangular STI cut-out. The large aspect ratio of the cut-out, could potentially lead to compressive transverse, and tensile longitudinal stress for the outer devices. This is different from single devices surrounded by STI and could also explain the difference observed here.

Another factor that has been shown to impact MOSFET mobility is metal coverage [34]. The reported mobility shifts as a result of metal-1 coverage (M1) are compatible with the results presented in this work. The devices in the interior of the array are impacted by the inevitable source/drain M1 interconnect of the two neighboring devices, while the two outer devices only encounter the effect of metal coverage from one neighboring device, thus also explaining the mobility shifts observed.

Apart from the mobility change, V_{TH} is also found to shift for the outer most devices in Fig. 15c and f, which can also be attributed to mechanical stress, as also reported in [24] and [33].

A practical guideline for circuit designers is that dummies can mitigate such effects, but no more than one dummy device on each side is required. Furthermore, the beneficial effect of such dummy is only significant for large devices for which device mismatch is not overpowering the stress effects.

VI. CONCLUSION

A commercial 40-nm bulk CMOS process was characterized over the temperature range from 300 K down to 4.2 K. The analysis of threshold-voltage and current-factor variability in matched transistor pairs showed that the Pelgrom scaling law remains valid down to deep-cryogenic temperatures. The current-factor variability, and consequently the A-factors, increase at these low temperatures by ∼75%, while the threshold-voltage variability

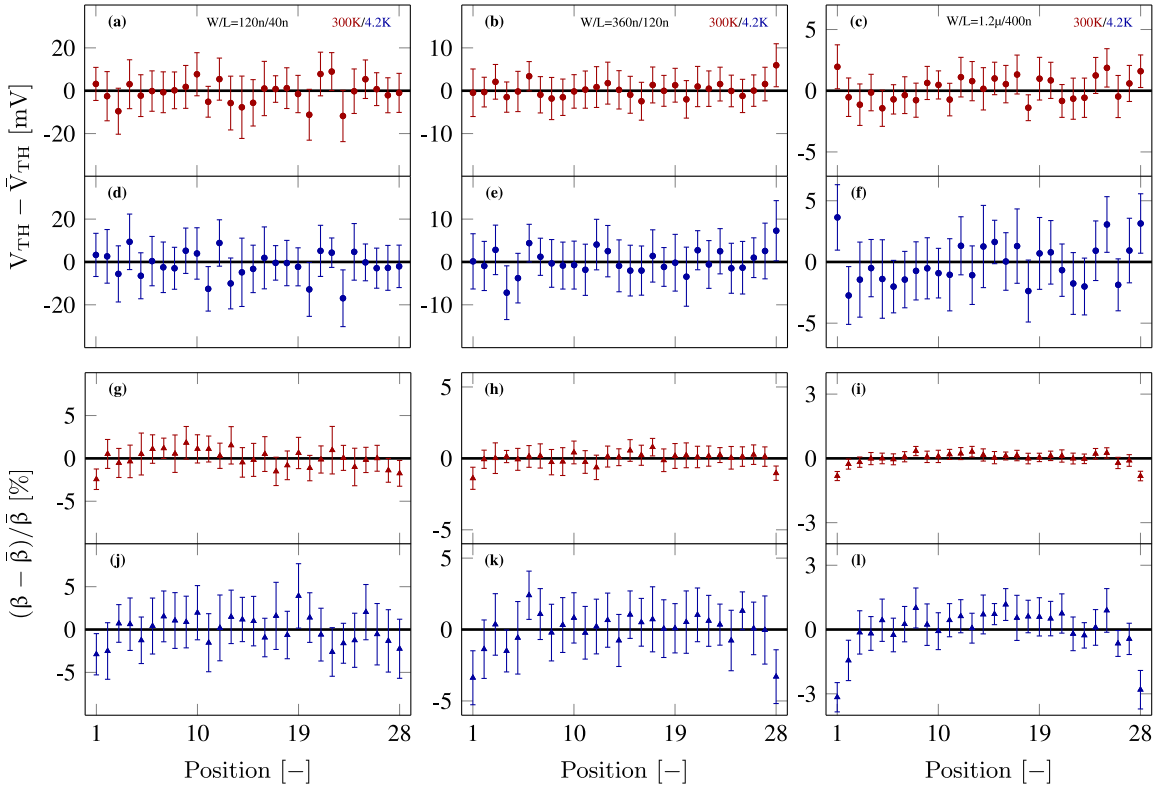


FIGURE 15. Normalised V_{TH} (circle) and β (triangle) as a function of device position for PMOS devices at RT (red) and LHT (blue). First column: W/L = 120n/40n; second column: W/L = 360n/120n; third column: W/L = 1.2µ/400n. Error bars indicate 95% confidence intervals.

remains substantially unaffected. The Croon model was successfully employed to accurately predict drain-current mismatch over the above-mentioned temperature range and for several device geometries. Further measurements on linear arrays of transistors uncovered a systematic mismatch related to device placement at the array edges, which has been attributed to mechanical stress. It was shown as a countermeasure that, when random mismatch is not overshadowing such an edge effect, placing dummy devices at the array edge can alleviate such effect. The availability of the presented mismatch model and of data on dummy placement for such advanced nanometer CMOS process enable the reliable design of the cryogenic circuits required for future large-scale-quantum computers.

ACKNOWLEDGMENT

The authors would like to acknowledge J. P. G. van Dijk for chip design, Dr. H. P. Tuinhout and Dr. M. J. M. Pelgrom for the helpful discussions and Intel for funding.

REFERENCES

[1] J. van Dijk, E. Charbon, and F. Sebastiano, "The electronic interface for quantum processors," *Microprocessors Microsyst.*, vol. 66, pp. 90–101, Apr. 2019.

[2] B. Patra *et al.*, "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2018.

[3] L. Vandersypen *et al.*, "Interfacing spin qubits in quantum dots and donors—Hot, dense and coherent," *npj Quant. Inf.*, vol. 3, Dec. 2016, Art. no. 34.

[4] D. Reilly, "Engineering the quantum-classical interface of solid-state qubits," *npj Quant. Inf.*, vol. 1, Oct. 2015, Art. no. 15011.

[5] S. R. Ekanayake, T. Lehmann, A. S. Dzurak, and R. G. Clark, "Quantum bit controller and observer circuits in SOS-CMOS technology for gigahertz low-temperature operation," in *Proc. 7th IEEE Conf. Nanotechnol. (IEEE NANO)*, Hong Kong, Aug. 2007, pp. 1283–1287.

[6] C. Degenhardt, L. Geck, A. Kruth, P. Vliex, and S. van Waasen, "CMOS based scalable cryogenic control electronics for qubits," in *Proc. IEEE Int. Conf. Rebooting Comput. (ICRC)*, Washington, DC, USA, Nov. 2017, pp. 1–4.

[7] F. Sebastiano *et al.*, "Cryo-CMOS electronic control for scalable quantum computing," in *Proc. 54th ACM/EDAC/IEEE Design Autom. Conf. (DAC)*, Jun. 2017, pp. 1–6.

[8] A. Beckers, F. Jazaeri, and C. Enz, "Characterization and modeling of 28-nm bulk CMOS technology down to 4.2 K," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 1007–1018, Mar. 2018.

[9] A. Beckers, F. Jazaeri, H. Bohuslavskyi, L. Hutin, S. D. Franceschi, and C. Enz, "Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures," *Solid-State Electron.*, vol. 159, pp. 106–115, Sep. 2019.

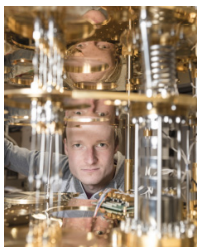
[10] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOS transistor model," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3617–3625, Sep. 2018.

[11] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and compact modeling of nanometer CMOS transistors at deep-cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 996–1006, Apr. 2018.

[12] S. Mennillo, A. Spessot, L. Vendrame, and L. Bortesi, "An analysis of temperature impact on MOSFET mismatch," in *Proc. IEEE Int. Conf. Microelectron. Test Struct.*, Mar. 2009, pp. 56–61.

[13] J. J.-Y. Kuo, W. P.-N. Chen, and P. Su, "Temperature dependence of device mismatch and harmonic distortion in nanoscale uniaxial-strained pMOSFETs," in *Proc. IEEE Int. Conf. IC Design Technol.*, May 2011, pp. 1–4.

[14] P. Andricciola and H. P. Tuinhout, "The temperature dependence of mismatch in deep-submicrometer bulk MOSFETs," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 690–692, Jun. 2009.
[15] K. Das and T. Lehmann, "Effect of deep cryogenic temperature on silicon-on-insulator CMOS mismatch: A circuit designer's perspective," *Cryogenics*, vol. 62, pp. 84–93, Jul./Aug. 2014.
[16] N. C. Dao, A. El Kass, C. T. Jin, and P. H. W. Leong, "Impact of series resistance on bulk CMOS current matching over the 5–300K temperature range," *IEEE Electron Device Lett.*, vol. 38, no. 7, pp. 847–850, Jul. 2017.
[17] P. A. 't Hart, J. P. G. van Dijk, M. Babaie, E. Charbon, A. Vladimircscu, and F. Sebastiano, "Characterization and model validation of mismatch in nanometer CMOS at cryogenic temperatures," in *Proc. 48th Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2018, pp. 246–249.
[18] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. SSC-24, no. 5, pp. 1433–1439, Oct. 1989.
[19] A. Ortiz-Conde, F. G. Sánchez, J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectron. Rel.*, vol. 42, no. 4, pp. 583–596, 2002.
[20] M. F. Hamer, "First-order parameter extraction on enhancement silicon MOS transistors," *IEE Proc. I Solid-State Electron Devices*, vol. 133, no. 2, pp. 49–54, Apr. 1986.
[21] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterisation and modeling of mismatch in MOS transistors for precision analog design," *IEEE J. Solid-State Circuits*, vol. SSC-21, no. 6, pp. 1057–1066, Dec. 1986.
[22] J. A. Croon, M. Rosmeulen, S. Decoutere, W. Sansen, and H. E. Maes, "An easy-to-use mismatch model for the MOS transistor," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1056–1064, Aug. 2002.
[23] G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy, and A. Asenov, "Simulation study of individual and combined sources of intrinsic parameter fluctuations in conventional nano-MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 3063–3070, Dec. 2006.
[24] S. K. Marella and S. S. Sapatnekar, "The impact of shallow trench isolation effects on circuit performance," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, San Jose, CA, USA, Nov. 2013, pp. 289–294.
[25] A. K. Jonscher, "Semiconductors at cryogenic temperatures," *Proc. IEEE*, vol. 52, no. 10, pp. 1092–1104, Oct. 1964.
[26] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOSFET threshold voltage model," in *Proc. 49th Eur. Solid-State Device Res. Conf. (ESSDERC)*, 2019, pp. 94–97.
[27] A. Cathignol, S. Bordez, A. Cros, K. Rochereau, and G. Ghibaudo, "Abnormally high local electrical fluctuations in heavily pocket-implanted bulk long MOSFET," *Solid-State Electron.*, vol. 53, no. 2, pp. 127–133, 2009.
[28] C. S. Smith, "Piezoresistance effect in germanium and silicon," *Phys. Rev.*, vol. 94, pp. 42–49, Apr. 1954.
[29] A. Shimizu *et al.*, "Local mechanical-stress control (LMC): A new technique for CMOS-performance enhancement," in *Int. Electron Devices Meeting Tech. Dig.*, Dec. 2001, pp. 19.4.1–19.4.4.
[30] S. E. Thompson *et al.*, "A 90-nm logic technology featuring strained-silicon," *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1790–1797, Nov. 2004.
[31] C. Maiti and T. Maiti, *Strain-Engineered MOSFETs*. Boca Raton, FL, USA: Taylor & Francis, Nov. 2012.
[32] J. F. Creemer and P. J. French, "Reduction of uncertainty in the measurement of the piezoresistive coefficients of silicon with a three-element rosette," in *Smart Structures and Materials 1998: Smart Electronics and MEMS*, vol. 3328, V. K. Varadan, P. J. McWhorter, R. A. Singer, and M. J. Vellekoop, Eds. Bellingham, WA, USA: SPIE, 1998, pp. 390–400.
[33] N. Wils, H. P. Tuinhout, and M. Meijer, "Characterization of STI edge effects on CMOS variability," *IEEE Trans. Semicond. Manuf.*, vol. 22, no. 1, pp. 59–65, Feb. 2009.
[34] N. Wils, H. Tuinhout, and M. Meijer, "Influence of metal coverage on transistor mismatch and variability in copper damascene based CMOS technologies," in *Proc. Int. Conf. Microelectron. Test Struct. (ICMTS)*, Mar. 2010, pp. 182–187.



P. A. 'T HART received the M.Sc. degree in electrical engineering from the Delft University of Technology, The Netherlands, in 2014, where he is currently pursuing the Ph.D. degree in characterizing and modeling cryogenic MOSFETs. For his thesis, he worked with the Electronic Components, Materials and Technology Department (ECTM) and the Electronic Instrumentation Laboratory, where he did characterization of the piezojunction effect in bipolar transistors. In 2017, he joined the Group of Edoardo Charbon, Delft University of Technology. His research interests include low temperature electronics, modeling, and characterization.

M. BABAIE (Member, IEEE) received the B.Sc. degree (Highest Hons.) in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, in 2004, the M.Sc. degree in electrical engineering from the Sharif University of Technology, Tehran, in 2006, and the Ph.D. degree (*cum laude*) from the Delft University of Technology, Delft, The Netherlands, in 2016. From 2014 to 2015, he was a Visiting Scholar Researcher with the Berkeley Wireless Research Center, Berkeley, CA, USA. In 2016, he joined the Delft University of Technology as an Assistant Professor. His current research interests include RF/millimeter-wave integrated circuits and systems for wireless communications, and cryogenic electronics for quantum computation. He was a co-recipient of the IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award from 2015 to 2016, and the IEEE ISSCC Best Demo Award in 2019. He received the Veni Award from The Netherlands Organization for Scientific Research in 2019. He has been a Committee Member of Student Research Preview of the IEEE International Solid-State Circuits Conference (ISSCC) since 2017 and will join as a Technical Program Committee of the IEEE European Solid-State Circuits Conference from 2020.

EDOARDO CHARBON (Fellow, IEEE) received the Diploma degree in electrical engineering and EECS from ETH Zurich in 1988, the M.S. degree in electrical engineering and EECS from the University of California at San Diego in 1991, and the Ph.D. degree in electrical engineering and EECS from the University of California at Berkeley in 1995. He has consulted with numerous organizations, including Bosch, X-Fab, Texas Instruments, Maxim, Sony, Agilent, and the Carlyle Group. He was with Cadence Design Systems from 1995 to 2000, where he was the Architect of the company's initiative on information hiding for intellectual property protection. In 2000, he joined Canesta Inc., as the Chief Architect, where he led the development of wireless 3-D CMOS image sensors. Since 2002, he has been a member of the faculty of EPFL, where he has been a Full Professor since 2015. From 2008 to 2016, he was with the Delft University of Technology as the Chair of VLSI design. He has been the driving force behind the creation of deep-submicron CMOS SPAD technology, which is mass-produced since 2015 and is present in telemeters, proximity sensors, and medical diagnostics tools. He has authored or coauthored over 350 papers and two books, and he holds 21 patents. His interests span from 3-D vision, FLIM, FCS, NIROT to super-resolution microscopy, time-resolved Raman spectroscopy, and cryo-CMOS circuits and systems for quantum computing. He is a Distinguished Visiting Scholar with the W. M. Keck Institute for Space, Caltech, a fellow of the Kavli Institute of Nanoscience Delft, and a Distinguished Lecturer of the IEEE Photonics Society.

ANDREI VLADIMIRESCU (Life Fellow, IEEE) received the M.S. and Ph.D. degrees in EECS from the University of California at Berkeley, Berkeley, where he was a key contributor to the SPICE simulator, releasing the SPICE2G6 production-level SW in 1981. He pioneered electrical simulation on parallel computers with the CLASSIE simulator as part of his Ph.D. He has authored *The SPICE Book* (Wiley). For many years he was an R&D Director leading the design and implementation of innovative software and hardware electronic design automation products for Analog Devices Inc., Daisy Systems, Analog Design Tools, Valid Logic, and Cadence. He is currently a Professor involved in research projects with the University of California at Berkeley, the Delft University of Technology, and the Institut Supérieur d'Électronique de Paris, as well as a consultant to industry. His research activities are in the areas of ultralow-voltage CMOS, design, simulation, and modeling of circuits with new devices and circuits for quantum computing.

FABIO SEBASTIANO (Senior Member, IEEE) received the B.Sc. (*cum laude*) and M.Sc. (*cum laude*) degrees in electrical engineering from the University of Pisa, Italy, in 2003 and 2005, respectively, the M.Sc. degree (*cum laude*) from the Sant'Anna School of Advanced Studies, Pisa, Italy, in 2006, and the Ph.D. degree from the Delft University of Technology, The Netherlands, in 2011. From 2006 to 2013, he was with NXP Semiconductors Research, Eindhoven, The Netherlands, where he conducted research on fully integrated CMOS frequency references, deep-submicron temperature sensors and area-efficient interfaces for magnetic sensors. In 2013, he joined the Delft University of Technology, where he is currently an Assistant Professor. He has authored or coauthored one book, 11 patents, and over 60 technical publications. His main research interests are cryogenic electronics for quantum computing, quantum computing, sensor read-outs, and fully integrated frequency references. He has been a member of the "Emerging technologies" sub-committee of the technical program committee of the RFIC Symposium. He was a co-recipient of the best student paper at ISCAS in 2008, the Best Paper Award at IWASI in 2017, and the Best IP Award at DATE in 2018. He is a Distinguished Lecturer of the Solid-State Circuit Society.