MOSFET Optimization for Solar Cell Integration

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Fabrication and Characterization of a Power MOSFET

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Preface

اَلسَّلَامُ عَلَيْكُمْ وَرَحْمَةُ اللهِ وَبَرَكَاتُهُ

With this master thesis I am closing a very important chapter in my life as a student in Electrical Engineering at TU Delft. Even though it was not always as fun, I thoroughly enjoyed these past five years thanks to the love and support of my family, friends, and colleagues. They provided me with the motivation and dedication to achieve my goals.

I would like to thank my family and friends first, because even though they could not help me with this thesis theoretically, they did help me emotionally (and sometimes financially). I would like to give a special thanks to my parents who always did everything in their power to support me whichever way they could.

I also want to show my appreciation to my great supervisors from the PVMD group. My daily supervisor, David van Nijen, who guided me during these nine months and was always there to provide me with with a analytical and different perspective on some of the problems I faced these past few months. He was especially helpful during the month of vacation he took. I would also thank Dr. Patrizio Manganiello for his enthusiasm, expertise during our meetings and wisdom. His office was always open and he always welcomed me with a smile.

Likewise, my gratitude goes out to the other members of the PVMD group and EKL staff for assistance in operating and maintaining the machinery and making sure I did not destroy all of my research. Notably Katarina and Jim, my office mates, who were always willing listen to me complain when I actually did break something.
I am finishing my 5 years as a student at TU Delft the same way I started them, happy and enthusiastic for what's to come next.

Y.Mercimek
Delft, June 2022

Abstract

As PV capacity in urban areas keeps increasing, non-uniform illumination of panels will become more prevalent. This could cause the partial shading to become more frequent, reducing PV system performance. Some ways to solve this problem is by the use of module-level maximum power point tracking (MPPT), micro inverters, or reconfigurable modules. To this end, the integration of metal-oxide-semiconductor field-effect transistor (MOSFET) on solar cells could play an important role in future methods to prevent this issue. This integration of a MOSFET allows for module level, and potentially sub-module level, MPPT, as well as the application of reconfigurable modules to circumvent this issue. This thesis aims to optimize the MOSFET dimensions and fabrication process to be able to handle the short circuit current and open circuit voltage of a PV module, and to analyze the optoelectrical effects under direct illumination of the MOSFET performance.

In this thesis report, a flowchart is proposed on how to fabricate a working power MOSFET while combining the fabrication techniques used in the Integrated Circuits and Photovoltaics industries. This process closely resembles the fabrication of solar cells and uses similar techniques used to fabricate interdigitated back contacted (IBC) solar cells. It is shown that

It is shown that the use of wider devices can reduce channel resistance from 167Ω for a PMOS device with a width of 500μm down to 20Ω for a device with a width of 5000μm. For NMOS devices a similar relationship can be seen where the channel resistance is 49Ω for a width of 500μm and 8.1Ω for a device width of 5000μm. The current density of the devices drop from 115$\mu A/\mu m$ for an NMOS device with a width of 500μm to less than 80$\mu A/\mu m$ for a 5000μm wide device. For PMOS this density drop is smaller where the drop is from 33$\mu A/\mu m$ to 27$\mu A/\mu m$. A study on the effects of implantation energy and scattering layer thicknesses showed that both lower energies and thicker layers yield higher drain currents and lower channel resistance. A possible explanation for this is that a shift in the threshold voltage increased the overdrive voltage and therefore the drain current.

In the investigation of the effects of direct illumination on the electrical characteristics of the device it was found that the threshold voltage increases for PMOS devices from -0.21V under no illumination to -0.06V under full spectrum illumination at 1000W/m^2 and decreases for NMOS devices from 0.06V under no illumination to -0.15V under full spectrum illumination at 1000W/m^2. Furthermore the off state gate leakage current increases by factor 33 under illumination at 1000W/m^2 for NMOS devices and by a factor of 10^7 for PMOS devices. The electron mobility of the NMOS transistor increases with incident light, improving the drain current gate voltage relationship. The channel resistance for the NMOS devices improved between 5-13%, depending on the intensity of the illumination, while the channel resistance of the PMOS increases up to 2%.A similar effect for the hole mobility of the PMOS was not observed. Similarly, the channel resistance of the NMOS transistor improved, possibly due to the shift in threshold voltage or improved electron mobility. This improvement in performance was not recognized for PMOS transistors, however.

A flowchart has been proposed for a process in which a MOSFET is fabricated on the backside of an Interdigitated Back Contacted (IBC) solar cell while combining as many steps as possible from their respective flowcharts to reduce complexity and costs, possibly leading the best balance between MOSFET and IBC fabrication.

Contents

1

Introduction

Humanity is faced with a climate crisis. Billions of tons of greenhouses gasses, like carbon-dioxide (CO_2), methane (CH_4) and nitrous oxide (N_2O),are released into the atmosphere every year as a result of fossil fuel production and consumption, such as coal, oil and gas. Greenhouse gasses have widespread environmental effects as they act as an insulating blanket around the Earth while they absorb and trap infrared radiation in the form of heat within the atmosphere, which would normally dissipate in space. The concentration of greenhouse gasses in the atmosphere fluctuates on a cyclical basis. Since human industrialization, this cyclical pattern has however seemingly been broken and the concentration of greenhouse gasses has been skyrocketing and reaching higher levels ever since, as can be seen in figure 1.1 [1].

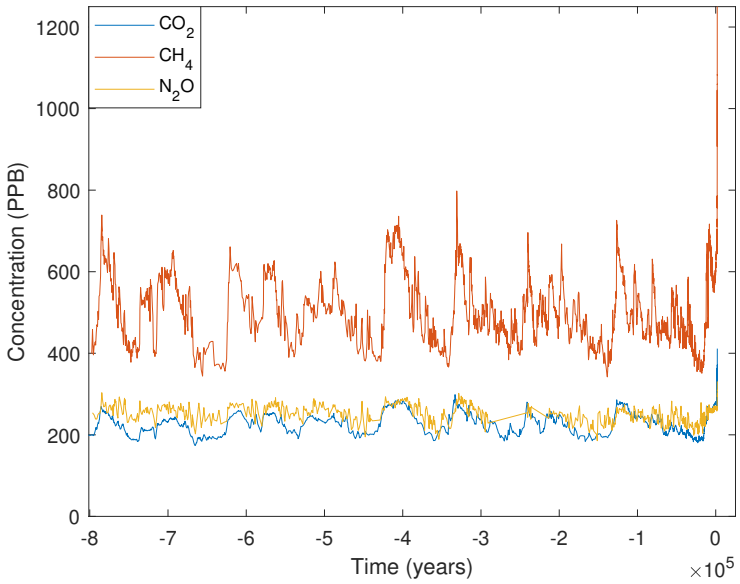


Figure 1.1: Atmospheric concentrations of greenhouse gasses of the past 800.000 years, data acquired from [1]

Human activity can be held responsible for almost all of the increase in greenhouse gasses over the last 150 years [2]. In 2010, 25% of the global greenhouse gas emissions is attributed to the production of electricity and heat, as is reported by the Intergovernmental Panel on Climate Change (IPCC) [3]. Additionally, global electricity generation has almost tripled in the past 40 years [4]. These numbers are likely to rise even higher as more economic sectors are electrifying. Transportation (14% of greenhouse gasses) and buildings (6%) have been rapidly electrifying and will continue to do so in the coming decade. The Earth is 1.1 °C warmer than compared to pre-industrial times and further increase can

have drastic effects on the environment [5]. An alternative sustainable fuel source has to be found to satisfy this increase in electricity demand, while at the same time reduce greenhouse emission as to prevent a further increase in global temperatures.

1.1. Solar energy as a potential fuel source

One such sustainable electricity source is solar energy. The sun is the most abundant source of energy in the entire solar system and thus the most logical one to use. The installed global photovoltaic (PV) power capacity has seen an exponential growth the past decade, from 74GW in 2011 to 714GW in 2020 [6] as can be seen in figure 1.2. Not only that, but the number of residential installations has seen a significant increase in the same time period as well [7].

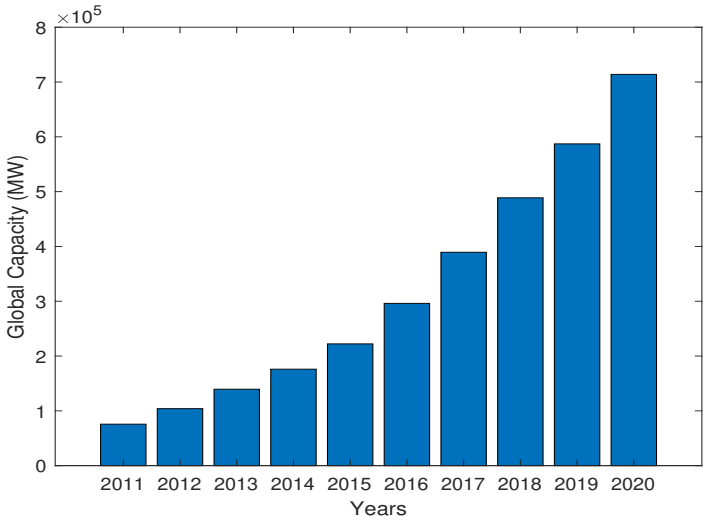


Figure 1.2: Global power capacity in MW from solar energy, data obtained from [6]

This growth can be attributed to the significant decline in the costs of PV electricity generation in the past decade. A study done in the Netherlands shows almost 50% of the households who have not yet installed a PV system are willing to do so if the price drops significantly [8]. Figure 1.3 show that the levelised cost of electricity generated using PV solar has decreased from 0.381 $/kWh in 2010 to 0.057$/kWh in 2020. PV power generation is currently one of the cheapest sources of electricity and even cheaper than fossil fuels.

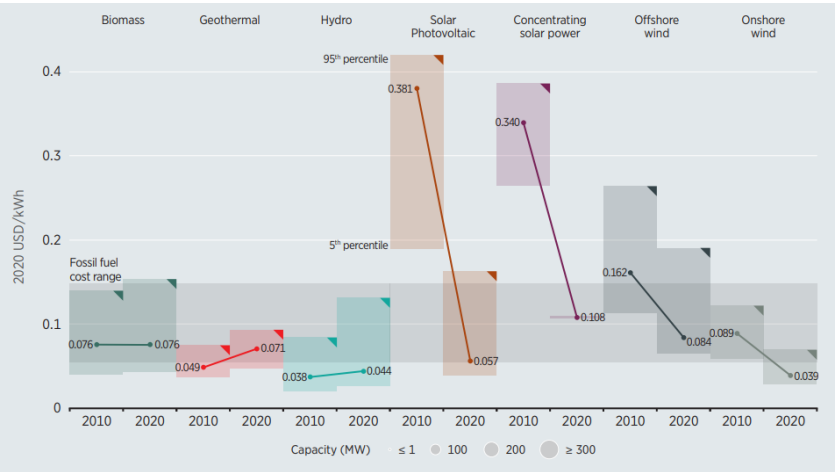


Figure 1.3: Global LCOEs from newly commissioned, utility-scale renewable power generation technologies, 2010-2020. from [9]

Figure 1.3 shows however that globally, PV is not the absolute cheapest sustainable source of energy. Both hydro and onshore wind are on average 20% cheaper to produce than PV solar. The advantage of PV solar however is its high power density compared to both hydro and wind. Figure 1.4 shows that, even though fossil fuels still have by far the highest power density , Solar has the highest power density of all renewable energy sources being twice as dense as wind and almost ten times as dense as hydro. An additional advantage of solar is also its integration with its environment. While both wind and hydro need dedicated land area, such as wind parks and hydro power plants, where the area has to primarily be dedicated to this application, solar panels can be used as a auxiliary application. On the roofs of office buildings for example. The higher power density and easier application solar systems are compelling reasons for widespread adoption. Lastly, while the levelized cost of energy might still be more expensive on a global level, significant differences in cost can be observed sunnier countries, where costs of less than 2 cents per kilowatt hour have been reached[10].

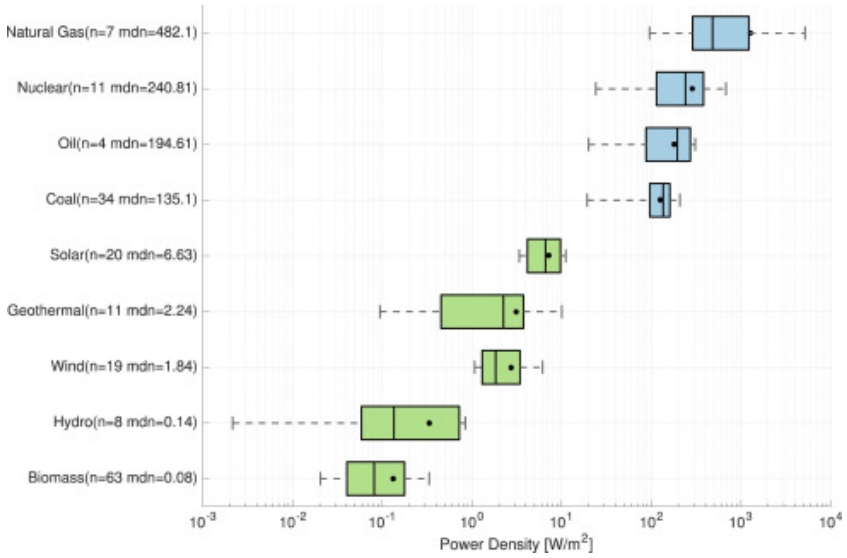


Figure 1.4: Box plots of power densities for all energy types visualized on a log scale. The annotations n and mdn give the number of values found for each energy type, and the median power density respectively. From [11]

1.2. Power Electronics in Photovoltaics

Power electronics is essential for correct operation of a PV system.The power electronics in PV systems are used for various reasons such as, Maximum power point tracking (MPPT) which increases performance of the system [12], inverters (also known as DC-AC converters) to change DC power produced by the panels to AC such that it can be connected to the grid [13], DC-DC converters to connect the PV System to other DC appliances [14], and charge controllers, which is needed when connecting the PV system to a battery[15]. The power electronic components of a PV system are generally separate from the PV module itself, but do have significant impact on the overall performance of the system.

Currently grid connected PV systems are more widely adopted than off-grid systems in many practical applications [16]. Grid connected PV systems typically need DC-AC converters, and sometimes DC-DC converters depending on the topology, to operate properly with the grid. In grid connected systems, the inverter is directly connected from the PV array to the grid. The four main inverter architectures are the central inverter, micro inverter, string inverter and the central inverter with optimisers [17], as is shown in figure 1.5. Each of these inverter architectures has their own advantages and disadvantages. The central inverter is usually used for large scale PV plants [18], due to its simplicity and low specific costs, while for smaller PV applications, such as in households, a string inverter is more widely implemented [17], which in addition to being low in cost can also apply MPPT more accurately. One big issue that affects solar cells in both central inverter as well as string inverter topology is the hot spot effect. This effect occurs when a cell in the string generates less current than the rest of the cells it is connected in series with. A cell can generate less current if the cell is (partially) shaded, is damaged or due to interconnection failure [19]. This mismatch between the cells can cause the mismatched cell

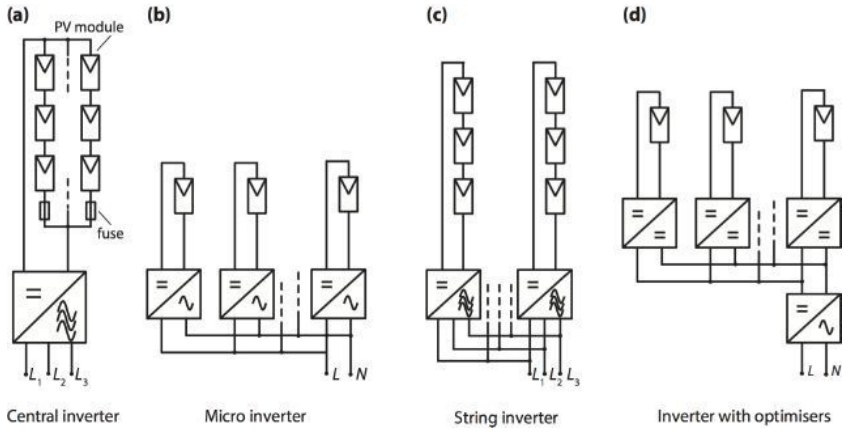


Figure 1.5: Different system architectures employed in PV systems, image obtained from [17]

to be reverse biased, dissipating the power instead of generating [20]. This causes the cell to overheat and cause irreversible damage, such as glass breakage and loss of electrical insulation [19].

One way to solve the problematic issues of the hot spot effect is by implementing bypass diodes[21]. These diodes are placed in parallel to a single cell or to a group of cells. If there is no current mismatch between the cells, then the bypass diode will not be in use and will act as an open circuit. If however a mismatch does occur, due to (partial) shading for example, then the current will flow trough the bypass diode, instead of the cells, and the unshaded cell(s) will be circumvented. This allows the PV module to still operate at the current of an unshaded solar cell. Generally, bypass diodes are not placed in parallel with every cell, but are placed in parallel with groups of cells[17]. Usually between 15-24 cells will be placed in parallel to one bypass diode [22]. This potentially means that one cell being shaded could reduce the power generated by roughly one third of a 60 cell solar module, as is shown in figure 1.6. Increasing the amount of bypass diodes to be equal to the amount of solar cells can be done to further reduce the effects of current mismatching, but this does come at the drawback of increased losses for every additional diode. Activated diodes would have a voltage drop and inactive diodes will have leakage currents, which reduces overall system performance [22].

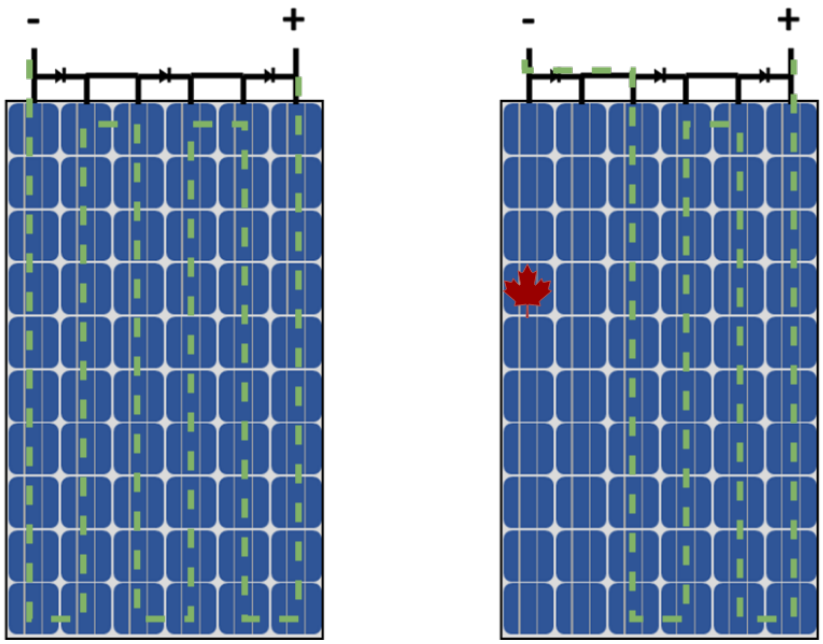


Figure 1.6: Current flow trough a solar panel without shading (left), and one where one cell is shaded (right)

Another technology that can be used reduce the effect of hot spot on system efficiency is the micro inverter. While the advantage of centralized inverter is their simplicity and low cost, with the drawback being low flexibility and their high losses when current mismatching occurs between different PV modules. The micro inverter operates directly at one PV module [23], [17]. This gives the advantage that the MPP can be optimally tracked for every independent module instead of a whole string. This means that any performance losses from shading can be contained within a single module. Because of the low voltage rating of a PV module, these type of inverters operate in two stages. In the first stage, a DC-DC boost conversion is performed, while in the second stage the DC-AC inversion is executed.

Micro inverters also have a significant drawback. These inverters are directly attached to the PV module and therefore have to be resistant to harsh environments and rapid changes to both weather and temperature. The inverters typically also have a very narrow input voltage range, which makes the use of bypass diodes, that bypass a third of the module and therefor voltage, not possible. Additionally, since the PV module voltage is much lower than the output AC voltage, the DC-DC conversion has to boost the voltage a lot. This has a negative effect on the inverter efficiency [17]. Another drawback is the increased capital cost of the microinverter. However, due to its increased efficiency, it will reach the break-even cost with the string inverter configuration well within the lifetime of the system[24].

Alternatively, an optimiser box could be attached to every module in a central inverter configuration. An optimiser box contains a MPP tracker and DC-DC converter and can only operate within a certain range of input voltages. If the input voltage is not within range, the current is altered such that the voltage falls within the acceptable range again [17]. This means that the output voltage of the optimiser is determined by the output power of the PV module. This can be especially useful for systems where performance varies widely between modules, due to orientation or shading for example, as this allows every module to operate in MPP. A drawback to the power optimiser is however their inability to improve efficiency when partial shading at sub module level occurs [25].

Another method to solve the hot spot effect is by using reconfigurable modules. In these modules the series connection can be reconfigured if partial shading does occur[26]. During shading, it is much more desirable to have parallel connected cells compared to the standard series connection, since in a parallel connection the overall current is the sum of all parallel currents and not limited by the lowest current producing cell as happens in string configuration. This helps reduce irradiance mismatch losses under nonuniform illumination. However, cabling is more expensive as well as more complex for such reconfigurable systems.

Essential in all the previously mentioned power electronics are transistors. In power electronics, transistors are generally used to achieve the desired switching behaviour. Transistors are semiconductor devices and can be considered as one of the building blocks of modern electronics [27]. They are commonly implemented to either switch or amplify electrical signals.

In this work we examine a solution that can support these developments. We investigate the integration of transistors into crystalline-Silicon(c-Si) solar cells .

More specifically, this project will focus on integrating a transistor on IBC cells rather than front-back contacted (FBC) solar cells.The main difference between an FBC and IBC is that the IBC has all its metal contacts on the back, while an FBC has one pole on the front and the other on the back, as can be seen in figure 1.7. The main advantage of IBCs compared to FBCs however is that it can use the full front surface for light absorption. The drawback however is that IBCs are more complex and costly to produce [28]. Lately, the research done on IBCs has increased. This is mainly due to their potentially better performance compared to standard FBC panels [29].

As the standard solar cell fabrication processes has been thoroughly optimized to fabricate high-efficiency cells, it is important that the changes necessary to integrate a transistor will have as limited impact as possible on the performance of the solar cell itself. The fabrication process should also combine as many processing steps as possible to further simplify production and reduce costs. lithography, for example, is still widely used for integrated circuit fabrication, even though the PV industry is moving

away from using photolithography for the production of IBC solar cells due to its costs [28]. This could function as a more cost effective method as both the IBC as well as the transistor integrated on it could be fabricated using the same photolithography steps, possibly increasing the cost effectiveness. This allows, in the case of a lateral transistor design for all of the contacts to be placed on the back side of the PV cell. This way monolithic integration between the component and the cell contacts can be achieved.

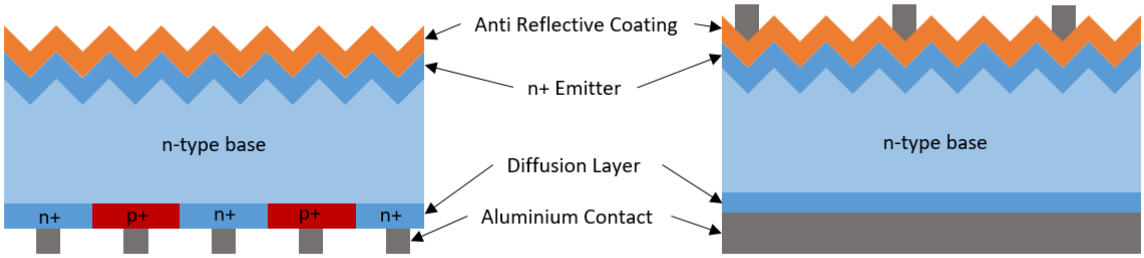
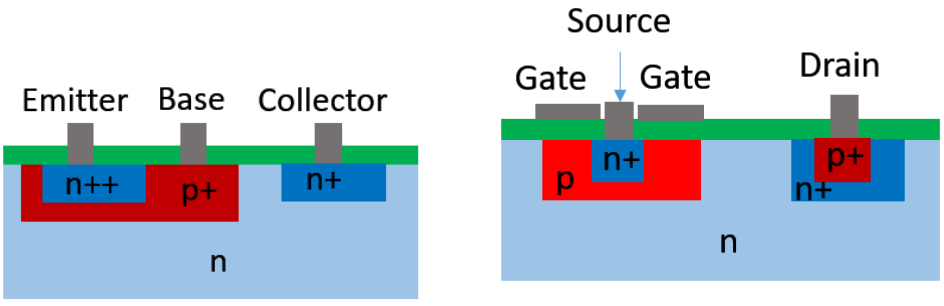


Figure 1.7: Simplified schematic of Front/Back Contacted (FBC, right) and Interdigitated Back Contact (IBC, left) solar cells.

1.3. Integration of a MOSFET

The most common type of transistor currently in use is the metal-oxide-semiconductor field-effect transistor (MOSFET) and is purposely chosen as the transistor for this project, rather than other transistors such as the Bipolar Junction transistor (BJT) or insulated-gate bipolar transistor (IGBT). A reason for opting for a MOSFET design for the transistor rather than a BJT or IGBT is the more similar design of a MOSFET compared to an IBC cell, with respect to the BJT and IGBT. Figure 1.8a and 1.8b show the cross section of a lateral BJT and IGBT respectively. In figure 1.8 it can already be seen that both of them make use of nested doping regions, which cannot be easily integrated into the production process of c-Si IBC solar cells.



(a) Bipolar Junction Transistor

(b) Insulated-Gate Bipolar Transistor

Figure 1.8: Cross section of BJT and IGBT

This is unlike a MOSFET, which does not necessarily use nested regions to operate, as is shown in figure 1.9. Unlike the BJT, Thyristor and IGBT, its source and drain can be simultaneously implanted in a single step. It is also possible that the ion implantation of the MOSFET could be combined with the implantation of the localised carrier selective contacts of the IBC, as they can be implanted with similar energy and doses[30][31]. Taking these arguments in consideration the MOSFET is the most promising due to its ease of integration with the IBC cell fabrication process.

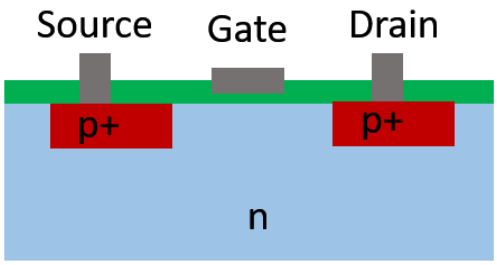


Figure 1.9: cross section of a PMOS transistor.

Various limits have to be taken into account however. The MOSFET should be able to handle the open circuit voltage and short circuit current of the solar cell to prevent breakdown. The power losses caused by using a MOSFET have to also be analyzed. In order to achieve this, MOSFETs of various feature sized and different fabrication methods will be investigated to determine the optimum MOSFET features.

In addition, transistors are usually encased to protect it from environmental effects such as wind rain, and most notably, light. It will not be possible to encase the MOSFET when it is integrated on a solar cell. In this case the MOSFET performance might be affected by incident light might lead to the generation of extra charge carriers in the MOSFET, causing a change in both controllability and performance. The effects of different wavelengths and intensities will also be analyzed.

1.4. Project Description and Outline

The subject of this Master thesis project is the integration of a power MOSFET into the body of an IBC solar cell. This project consists of the following research questions:

- How can we optimally fabricate a power MOSFET while using fabrication techniques used in solar cell production?
- What is the effect of direct illumination on the controllability and performance of the MOSFET?
- What is the optimal feature sizes to handle the power generated by the solar cell?

To answer the research questions mentioned above, this thesis will use a total of 9 chapters. In chapter 1 the scope and background to the research topic have been explained. Chapter 2 provides the necessary theoretical knowledge needed to the reader. Chapter 3 treats the manufacturing and characterization tools as well as the fabrication method. In chapter 4 the direct current (DC) performance of the MOSFETs is analyzed and a recommendation is given regarding the optimal features. Chapter 5 Discusses the effects and resulting influence of illumination on the performance of the MOSFETs. Then in chapter 6, the alternating current (AC) performance of the MOSFET will be characterized. Afterwards, in chapter 7, a new flowchart for the combined fabrication of solar cell and MOSFET is proposed. Lastly, in chapter 8 the results from this thesis will be discussed and concluded and a future outlook will be given.

2

Theoretical background

This chapter explains some theoretical background regarding semiconductor fundamentals, MOSFET design and photovoltaic technology that is relevant for this thesis project.

2.1. Semiconductor Fundamentals

A semiconductor is a type of material with a conductivity between those of metals and insulators. By far the most common type of semiconductor used in integrated circuits is silicon(Si). One of the most important semiconductor features is the possibility to control its electrical conductivity by doping. Doping of silicon means the incorporation of atoms of another element, from either group 13 or group 15 from the periodic table, to replace Si atoms in the lattice. The most used elements for doping c-Si is Boron (group 13) and phosphorus (group 15). Doping using these elements adds either free electrons, if doped with an element from group 15, or extra holes in the case of doping with an element from group 13 of the periodic table. A silicon layer with an majority amount of negatively charged electrons is called n-type layer. Likewise, a silicon layer with an majority of positively charged holes, due to boron doping, is called a p-type layer [17][32].

The doping concentration of electrons and holes as well as the mobility decide the electrical conductivity within semiconductor material. However, the operation of transistors and other semiconductor devices, are heavily dependent on the electron and hole behaviour at the interface between two layers, called a p-n junction. At this junction there is a very large density gradient in both electron and hole concentrations. This causes the majority charge carriers from both materials to diffuse to the other material. As this diffusion of electrons from the n-type region to the p-type region occurs positively charged donor atoms are left behind. Likewise, the diffusion of the holes from the p-type region to the n-type region leaves behind negatively charged acceptor atoms. These positive and negative charges in the n and p regions induce and electric field around the junction. This region is commonly known as the *depletion region* or *space charge region* and can be seen in figure 2.1

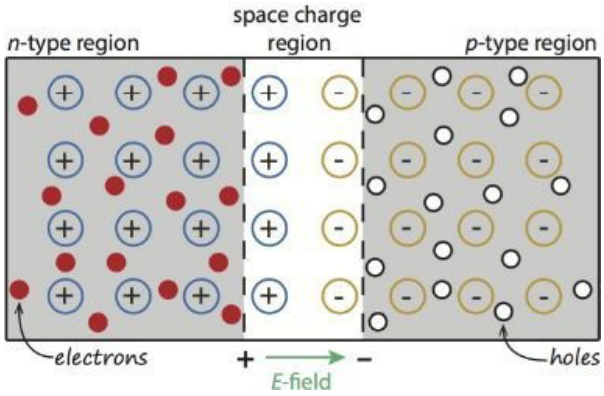


Figure 2.1: Space charge region and its electric field. [17]

When the junction is in zero bias and no voltage is applied to the pn junction, the presence of the internal electric field generates and electrostatic potential difference called the Built-in voltage, V_{bi}. This V_{bi} maintains equilibrium between diffusion forces and the electric field. This equilibrium means that no current is produced by V_{bi}.

When the junction is in reverse bias, which means a negative voltage is applied to the p-type region with respect to the n-type region, the potential barrier increases equal to the applied voltage. This increases the maximum electric field and the depletion region width. Similar to zero bias conditions, essentially no charge will flow, hence almost no current will flow.

In forward bias however, where a positive voltage is applied over the pn junction, this potential barrier will decrease equal to the applied voltage ($V_{bi} - V_a$). This decreases the depletion region width and weakens the electric field strength. This reduces the barrier for the diffusion of the charge carriers from one side of the junction to the other and allows charge to flow through it. This flow of charge generates a current through the pn junction [17].

2.1.1. Junction Breakdown

The reverse bias on a p-n junction can not be infinitely increased without limitations. At a certain voltage the reverse bias current will increase rapidly. The voltage at which this occurs is called the breakdown voltage [32]. Breakdown occurs through three different mechanisms: Zener effect, avalanche effect and punch through. Zener effect works trough a tunneling mechanism. During reverse bias operation the conduction and valence band of the material might be sufficiently close that electrons may tunnel directly from the valence band to the conduction band. Avalanche breakdown happens when electrons or holes acquire enough energy to generate electron holes pairs from collision with electrons in the depletion region of the p-n junction. These newly created electrons and holes move in the opposite direction due to the reverse bias voltage and thus create reverse bias current. Additionally the newly generated holes and electrons may also have enough energy to ionize other atoms creating an avalanche process. The breakdown voltage can be calculated using a simplified formula 2.1 for a one sided pn junction acquired from [32]:

$$V_B = \frac{\epsilon_s E_{crit}^2}{2eN_B} \tag{2.1}$$

Where ϵ_s is the permitivity of the semiconductor, E_{crit} the maximum electric field of a p-n junction, e is the elementary electron charge and N_B is the semiconductor doping in the low-doped region of the one-sided junction. It can be seen that reducing the doping concentration will increase the breakdown voltage. Reducing the dopant concentration will also increase the depletion region width however, which increases the total current density in the pn junction during conduction for a given voltage in the on state [32]. Thus, while designing the transistor, the doping concentration must be carefully taken into consideration in order to optimize for both current density and breakdown voltage.

The third type of breakdown, punch through, does not occur with only one pn junction, but rather two pn junctions in relatively close proximity of each other, such as in a MOSFET. Punch though occurs

when a sufficient voltage is applied such that the space charge region of one pn junction extends over space charge region of the other pn junction. In this situation the barrier between both junctions would not exist anymore and junction breakdown will occur [32].

2.2. MOSFET structure

Figure 2.2 shows a simplified structure p-type MOSFET on a n-type substrate, also called the 'bulk' or 'body'. A MOSFET consists of two heavily doped regions (in this case *p* regions) called the source and drain, a heavily doped piece of polysilicon functioning as gate, and a thin layer of silicon dioxide, SiO_2, insulating this polysilicon gate from the substrate. The lateral distance between the source and drain is called the channel length (*L*), while the dimension perpendicular to that is known as the device width (*W*). These type of MOSFETs are symmetric devices, as in the source and drain can be used interchangeably of each other.

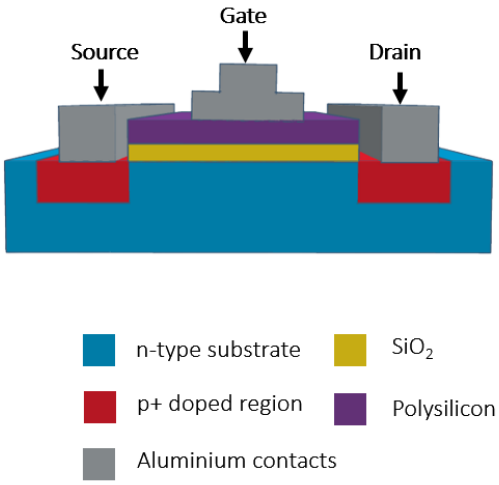
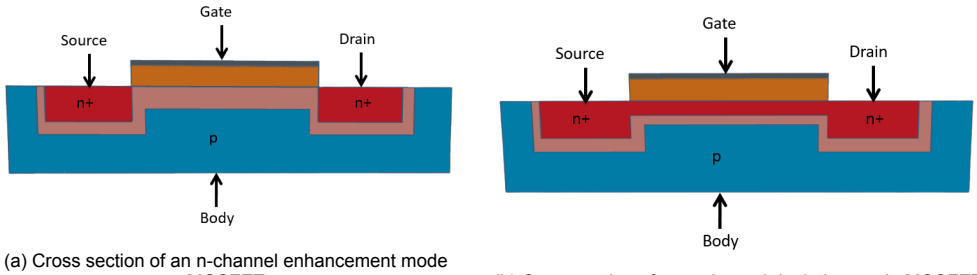


Figure 2.2: Structure of a MOS device

There are four basic MOSFET device types. The first differentiation is their majority charge carriers. N-channel type MOSFETs use electrons as their charge carrier and are called NMOS. Likewise, p-channel type MOSFETs use holes as charge carrier and are called PMOS [33]. NMOS devices can be switched an will have a higher current density due to the fact that electrons have a higher mobility than holes, which are used in PMOS devices.

The other differentiation made is corresponding to whether the MOSFET is in a conducting state or a non-conducting state when the gate to source voltage is zero. When the MOSFET is conducting at zero gate to source voltage, the device is in depletion mode. When the device is off at zero gate to source voltage, the device is in enhancement mode. An enhancement mode device can be turned on by applying either a negative (PMOS) or a positive voltage (NMOS) on the gate. Figure 2.3 shows the difference between the channels of enhancement and depletion mode devices at zero gate voltage. When a positive voltage is applied to enhancement mode devices, they also will create a channel between the source and drain. This project will focus on enhancement mode devices.



(a) Cross section of an n-channel enhancement mode MOSFET

(b) Cross section of an n-channel depletion mode MOSFET.

Figure 2.3: Cross section of enhancement and depletion mode devices [32]

2.3. MOSFET operation

A MOSFET has three regions of operation: cut-off, triode, and saturation. Its region of operation is determined by the relationships between the gate to source voltage (V_{GS}), the drain to source voltage (V_{DS}) and the threshold voltage(V_{th}). V_{GS} and V_{DS} are simply the potential difference between the gate and source, and drain and source respectively. The threshold voltage is the minimum gate to source voltage that is needed to create a conduction path between the source and drain for enhancement mode devices. This means that an NMOS device is turned off when $V_{GS} < V_{th}$ and almost no current will flow trough the device.

2.3.1. Triode region

When $V_{GS} > V_{th}$ and $V_{DS} < V_{GS} - V_{th}$ the NMOS enters the triode region. The I-V relationship between the current flowing from drain to source, also known as the drain current I_D, and V_{DS} will follow a parabolic behaviour shown in figure 2.4 until $V_{DS} = V_{GS} - V_{th}$ according to the following formula[33]:

$$I_D = \mu_n C_{ox} \frac{W}{L}((V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2) \tag{2.2}$$

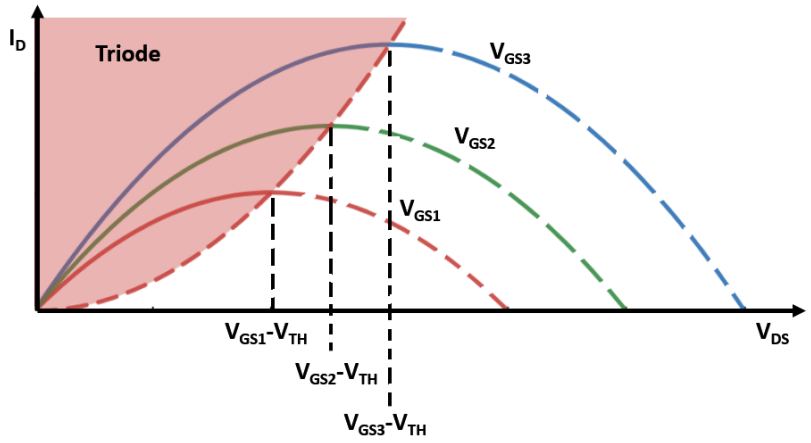


Figure 2.4: Drain current Vs. drain to source voltage in triode region.

Where μ_n is the electron mobility and C_{ox} is the gate oxide capacitance per unit area. For $V_{DS} << 2(V_{GS} - V_{th})$ the drain current formula can be approximated by formula 2.3. This means that for small values of V_{DS} the drain current operates as linear function. A MOSFET can therefore be used to operate as a resistor for small values of V_{DS} [33].

$$I_D \approx \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})V_{DS} \tag{2.3}$$

2.3.2. Saturation region

The drain current of a MOSFET operating in triode will ideally follow the parabolic behaviour described in formula 2.2 until $V_{DS} = V_{GS} - V_{th}$, which is equal to the maximum drain current, at which point the

MOSFET enters the saturation region. When $V_{DS} > V_{GS} - V_{th}$ the MOSFET enters the saturation region, in this region the drain current no longer behaves parabolic with respect to V_{DS} but becomes relatively constant, as is shown in figure 2.5, and can be calculated using formula 2.4.

$$I_D = \mu_n C_{ox} \frac{W}{L}((V_{GS} - V_{th})^2 \tag{2.4}$$

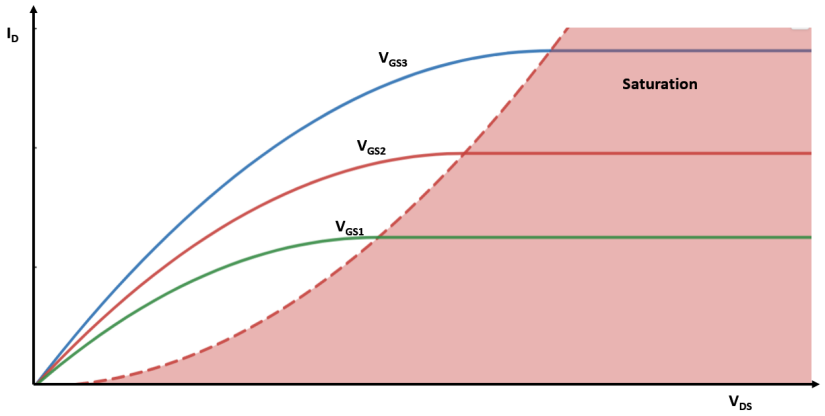


Figure 2.5: Drain current Vs. drain to source voltage in saturation region region.

However when the MOSFET is biased in the saturation region, the depletion region at the drain will extend laterally into the channel, effectively reducing its length. This phenomenon is called channel length modulation. The shortening of the effective channel reduces the channel resistance and will thus increase the current in saturation linearly to V_{DS} multiplied with a parameter λ, knows as the *channel length modulation parameter* according to the following formula 2.5

$$I_D = \mu_n C_{ox} \frac{W}{L}((V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \tag{2.5}$$

2.4. MOSFET characteristics

In this section, the most important MOSFET characteristics are explained.

2.4.1. Threshold voltage

The gate, dielectric and the p-substrate of an NMOS together form a capacitor. As the gate voltage, V_G, increases, the holes in the substrate are repelled and only negative ions are left behind to mirror the charge at the the gate, similar to a depletion region. When V_G is further increased, so will the width of the depletion region and at a certain value, an inversion layer will form and current will start to flow from source to drain and the MOSFET is 'turned on'. The value of V_G for which current will start to flow is called the threshold voltage. In semiconductor physics the threshold voltage is generally defined as the gate voltage for which the interface is 'as much the n-type as the substrate is p-type' [33].

The threshold voltage can be derived from electrical and geometrical properties and differs between PMOS and NMOS transistors. Formulas 2.6 and 2.7 show the relationship between these properties and the threshold voltage for both NMOS and PMOS respectively[32].

$$V_{TN} = \frac{|Q'_{SD}(max)|}{C_{ox}} - \frac{Q'_{ss}}{C_{ox}} + \phi_{ms} + 2\phi_{fp} \tag{2.6}$$

$$V_{TP} = \frac{-|Q'_{SD}(max)|}{C_{ox}} - \frac{Q'_{ss}}{C_{ox}} + \phi_{ms} - 2\phi_{fn} \tag{2.7}$$

Where $Q'_{SD}(max)$ is the maximum space charge density per unit area, Q'_{ss} is the equivalent trapped oxide charge per unit area, ϕ_{ms} is the metal–semiconductor work function difference, and ϕ_{fn} and

ϕ_{fp} are potential differences between the intrinsic Fermi level and the Fermi level in n-type and p-type semiconductors. This means that the threshold voltage can be controlled using various methods. Increasing the oxide thickness for example, decreases the oxide capacitance, which in turn decreases the threshold voltage.

There are also some non ideal effects that occur for MOSFETS with smaller dimensions such as short and narrow channel effects[32]. In short channel effects, a relatively large part of the threshold voltage is no longer controlled by the gate voltage but rather by the space charge regions of the source and drain, shifting the threshold voltage in negative direction for n-channel MOSFETs. Likewise, narrow channel effect is when the channel width extends farther than the gate width, thus increasing the threshold voltage comparatively to wider NMOS devices with the same doping.

2.4.2. Transconductance

The transconductance, g_m, is defined as the change in drain current with respect to the change in gate voltage and is also referred to as the transistor gain:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{2.8}$$

From formula 2.8 it can be derived that the transconductance is a function of the geometry of the device, its carrier mobility, and threshold voltage.

2.4.3. On resistance

The drain to source on resistance, $R_{DS(on)}$, is the total resistance measured from drain to source of the device. This term is used in this paper for the resistance in the linear area of triode region of operation during conduction and includes the channel resistance, source contact resistance and drain contact resistance. In the linear region of operation the channel resistance can be approximated by:

$$R_{CH} = \frac{L}{W\mu_n C_{ox}(V_{GS} - V_{TH})} \tag{2.9}$$

The contact resistances are proportional to the semiconductor resistivity and inversely proportional to the mobility [32]. It is defined as the resistance between the metal contact and the diffusion layer underneath it. In addition to the resistivity, it is also a function of the sheet resistance of the underlying diffused layer[34].

2.4.4. MOSFET breakdown voltage

Breakdown in MOSFETs happened in the same way as mentioned earlier in chapter 2.1.1, where either Zener, avalanche, or punch through breakdown can occur. These are all forms of semiconductor breakdown. Due to the geometry of the MOSFET however, other types of breakdown may also occur, including near breakdown effects. The following types of breakdown may occur in a MOSFET[32]:

- $Oxide\ breakdown$: The gate oxide is not a perfect insulator. If the electric field in the oxide becomes too large enough, breakdown will occur. In silicon dioxide, this electric field limit is in the order of 6×10^6 V/cm. Due to the relative thinness of the gate oxide compared to other features, a safety margin of factor 3 is common. This would mean that if the oxide thickness is 100nm, oxide breakdown would occur at 60V. The maximum safe gate voltage is then set at 20V. Such a margin is necessary as there may be defects in the oxide causing breakdown at lower voltages.

- $Avalanche\ breakdown$: Avalanche may occur in the space charge region near the drain of MOSFET by impact ionization. The previously discussed breakdown voltage was for a planar junction. However a MOSFET drain may be diffused in a shallow region with a large curvature. The electric field in the depletion region tends to be concentrated in this curvature, as is shown in figure 2.6, which lowers its breakdown voltage from the theoretical planar junction.

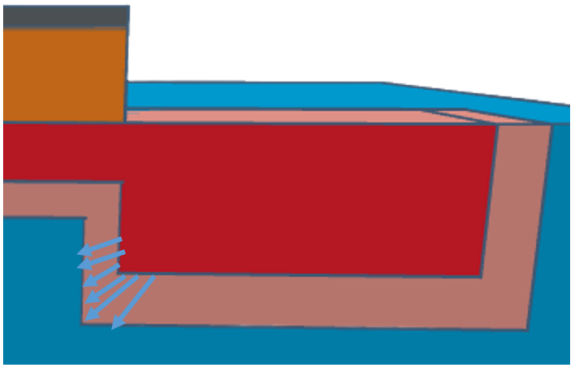


Figure 2.6: Curvature effect on the electric field in the drain junction

- $Near\ Avalanche\ and\ Snapback\ Breakdown$: This breakdown mechanism received its name due to the S-shaped breakdown curve shown in figure 2.7 it results into. This is due to a feedback loop caused by the parasitic bipolar transistor inherent to the MOSFET design. The breakdown voltage of this parasitic transistor is inversely related to the drain current. This means that when breakdown starts for the MOSFET, its drain current will start to increase. At the same time the parasitic bipolar transistor is turned on by the voltage generated from the avalanche-generated substrate current. Then breakdown voltage decreases, which causes this snapback phenomenon.

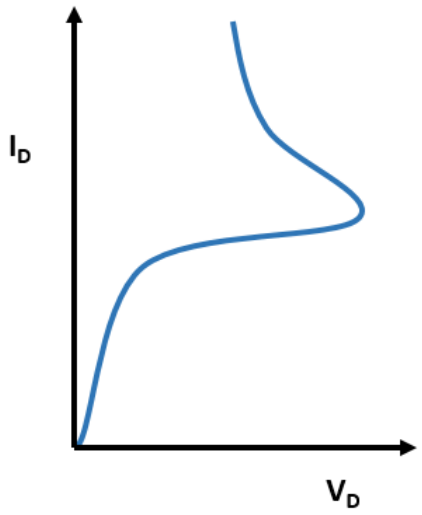


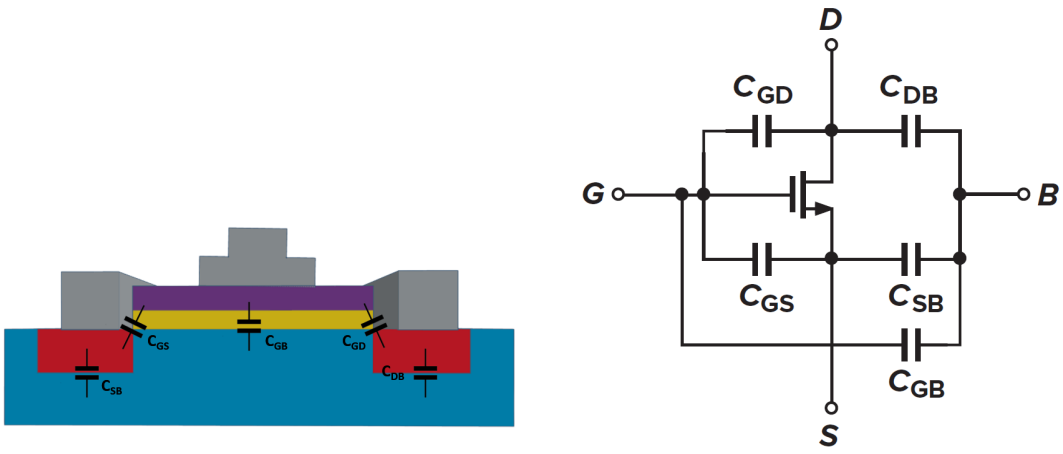
Figure 2.7: Curvature effect on the electric field in the drain junction.

- $Near\ Punch-Through\ Effect$: Punch through happens when the space charge regions of the drain and source get too close together. The barrier between source and drain is lowered in this case and a large current will start to flow. Before punch through is reached however the drain current will start to rapidly increase, which is known as Drain-Induced Barrier Lowering (DIBL).

2.4.5. Capacitances

The advantage of MOSFETs over some of the other transistors is that they do not have any excess minority carrier that must be moved into or out of the device when it turns on or off. The only charges that have to be moved are of the parasitic capacitances. A MOS device exhibits 5 different capacitances shown in figure 2.8[33] and can be summarized in the following list:

- C_{ox}:The oxide capacitance between the gate and the channel.
- C_{dep}: The depletion capacitance between the channel and the substrate.
- C_{ov}: The overlap capacitance between the source/drain and polysilicon owing to fringing electric field lines, independently known as C_{GD} and C_{GS}.
- C_{SB} / C_{DB}: the junction capacitance between the source/drain and the substrate.
- C_{GB}: Although not a different capacitance, the gate-bulk capacitance consist of the series combination of C_{ox} and C_{dep}.



(a) Representation of capacitances in a MOS device

(b) Symbolic representation of capacitances of a MOSFET [33]

Figure 2.8: Capacitances of a MOSFET [32]

2.5. MOSFET loss mechanisms

2.5.1. Conduction losses

Disregarding operation at higher frequencies, almost all of the power dissipated in the MOSFET in a switch-mode power application occurs in the on state of the device from conduction. The instantaneous power dissipation in the on state of a MOSFET is given by formula 2.10[35].

$$P_{on} = I_D^2 R_{DS(on)} \tag{2.10}$$

Conduction losses can be minimized by either reducing the drain current or on resistance. Reducing the drain current will not be possible as that will be determined by the current generated from the solar cells. The on resistance however can be reduced using several techniques. One way is to increase the doping in each region in accordance with the limit for avalanche breakdown, as that limit will decrease with an increased dopant concentration. Secondly, the dimension of the MOSFET could be altered to reduce the resistance by either widening the gate width, or metal width, to allow for more current to pass trough, or by shortening the channel length. Alternatively, the contact resistance of the drain and source could be reduced by improving the contact between the aluminium and silicon interface.

2.6. Photovoltaic fundamentals

When a pn junction is illuminated, some of the incident photons are absorbed by the semiconductor materials. This absorption of photons results in the generation of extra charge carriers that change the carrier concentration in the junction. Minority charge carriers will then flow across the depletion region. Electrons in the p-type material will flow to the n-type, while holes in the n-type will flow in the opposite direction. This flow of carrier produces the so called photo current. When an electrical circuit is connected to a pn junction, current will flow through it and the electron hole pair will recombine that way [32][17]. This is the basic principle on how solar cells use illumination to generate electricity.

2.7. IBC structure

This thesis focuses on the integration of MOSFETs on crystalline silicon (c-Si) interdigitated back contacted (IBC) solar cells. C-Si solar cells are the most common cell type used in the PV industry. They are so-called diffusion based devices in which the free charge carrier transport is based on diffusion. The separation of these charge carriers in pn junctions which only let one type of charge carrier through[17].

A successful high efficiency concept based on crystalline silicon is the IBC solar cell and can be seen in figure 2.9 [31]. The main benefit of the IBC is to have no shading losses at the front by removing the front metal contacts. All contacts are instead placed on the back side of cell. IBC cells do not use one large pn junction, rather they implement many localized junctions instead. The holes are separated at the p^+n junction between the substrate and the emitter, while the electrons are collected using the n^+n junction between the back surface field (BSF) and substrate. The semiconductor metal interfaces are kept small to reduce surface recombination. The cross section of the metal contacts however can be made much larger as they do not cause any shading and therefore losses. The passivation layer is made from a low refractive index material that operates as a backside mirror[17]. the IBC design shown in figure 2.9 will also be used as the basis for the MOSFET design.

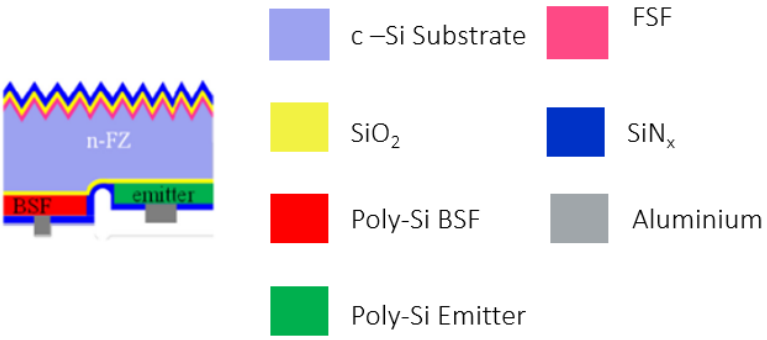


Figure 2.9: Cross section of the IBC solar cell [31]

Surface recombination at the front side is suppressed by a front surface field created by a highly doped n^+ region at the front of the surface. This n^+n junction acts similar to an np junction. It will act as a barrier to prevent minority holes in the n-region to diffuse towards the front surface. This allows for higher levels for the hole minority density in the n-doped bulk [17]. Reflective losses at the front are reduced by deposition of anti reflection coatings (ARC) and texturing of the front surface [17]

2.8. Loss mechanisms in solar cells

This section describes different loss mechanisms in solar cells that are relevant to take into account while integrating a MOSFET on a IBC cell. There are many more loss mechanisms in solar cells, the ones mentioned in this section however are the ones most likely to be affected by the integration of the MOSFET.

- Transmission losses: Not all light incident on the solar is absorbed. Some of it is reflected at the surface, but some can still transmit through the surface. The probability of a photon transmitting through a surface is directly related to the thickness of the absorber layer. Light scattering techniques and back reflection layers to increase the path length of a photon are used to enhance absorption. Integration of a MOSFET might have an effect on the back surface reflectance of solar cell, as a small part will have to consist of a different material or thickness with a different refractive index.

- Shading losses: Shading happens when an object blocks the path of light hitting the solar cell. This causes that less photons reach the cell and decreases the generated photocurrent. While there is no shading losses at the front side of an IBC, there is on the back side. IBC cells can be applied as bifacial cells, which means that photons can be absorbed from the front as well as from the back side. Placing a MOSFET on the backside of the IBC cell will thus reduce the amount of incident light falling on the backside of the cell and decrease its efficiency. This can be minimized by making the transistor and the metal contacts as small as possible.
- Surface recombination: Dangling bonds at a surface can introduce trap states that facilitate recombination. Surface recombination can be minimized by using surface passivation techniques. Some fabrication steps necessary to fabricate a MOSFET however might have adverse effects on the passivation of the cell.

2.9. Solar cell parameters

In this section some important solar cell parameters for this thesis project are explained.

2.9.1. Open circuit voltage

The open circuit voltage V_{oc} is the maximum voltage available from a solar cell and happens at zero current. It corresponds to the forward bias voltage, at which the saturation current density compensates the generated photocurrent density. V_{oc} depends on the photo current density and can be calculated using formula 2.11 [17]

$$V_{oc} \approx \frac{k_B T}{e} ln(\frac{J_{ph}}{J0}) \tag{2.11}$$

In this equation, k_B is the Boltzmann constant, T the temperature, and e the elementary charge constant. Furthermore, the V_{oc} is dependent on the photocurrent density J_{ph} and the saturation current density J_0. The J_{ph} is the current resulting from the flux of photo generated carriers. The open circuit voltage is also generally seen as a measure of the amount of recombination

2.9.2. Short circuit current

The short circuit current I_{sc} is the current that flows through the external circuit when the electrodes of the solar cell are short circuited. The short circuit current of a solar cell depends on the photon flux incident on the solar cell, which is determined by the spectrum of the incident light. For standard solar cell measurements, the spectrum is standardized to the AM1.5 spectrum. The I_{sc} depends on the area of the solar cell. In order to remove the dependence of the solar cell area on I_{sc}, the short-circuit current density,in mA/cm^2, is often used to describe the maximum current delivered by a solar cell. The maximum current that the solar cell can deliver strongly depends on the optical properties of the solar cell, such as absorption in the absorber layer and reflection.

3

MOSFET fabrication and characterization

This chapter will describe the production and characterization methods that were used during this thesis. First, section 3.1 the tools used for the fabrication of the MOSFETs is described. Section 3.2 a step by step description will be given of the methods used to fabricate the MOSFET. Lastly, in section 3.3 the tools used for characterization are treated.

3.1. Fabrication tools

This section will describe the techniques and tools used to fabricate the MOSFET during this thesis. These tools were all located in the Else Kooi Laboratory (EKL) at Delft University of Technology. All fabrication tools were located in the either the class 100 or class 10000 area of the cleanroom in EKL. The classification of a cleanroom represents the allowed number of particles per cubic metre smaller than 0.5 μm in the air.

3.1.1. Photolithography

Photolithography is a series of techniques used to project a pattern onto a silicon substrate. Ultra violet light is used to transfer a geometric pattern from a photomask to a photosensitive, chemical photoresist that is on the substrate. It can be used for the very precise definition of structures due to its small feature size, below 1μm, as compared with other technologies [36]. First a layer of photoresist (PR) is deposited on the entire wafer in a procedure called coating. Secondly, a mask is used the cover the the wafer and project the desired pattern on the PR in a process called exposure. Positive PR will become soluble after exposure with UV light, while negative PR will become insoluble after exposure. After exposure, the wafer is developed. If the PR is positive, the portion of the photoresist that was exposed to light will dissolve. Likewise , if the PR was negative, the exposed PR will not dissolve using the developer, but rather the unexposed parts will. Photolithography leaves the required design outlined by the exposure mask ready for the next fabrication step, which is generally some form of etching or deposition. Figure 3.1 shows the process of how photolithography could be used to etch a certain pattern of SiO_2 using both positive and negative photoresist.

In this thesis photolithography is used to define multiple components of the MOSFET design, such as the gate and the metal contacts. This way, only the specific area exposed by the lithography will undergo the necessary fabrication steps to fabricate the MOSFET. For the coating and development the EVG 120 tool from EV Group was used. For exposure the SUSS MicroTec MA/BA8 mask aligner was used.

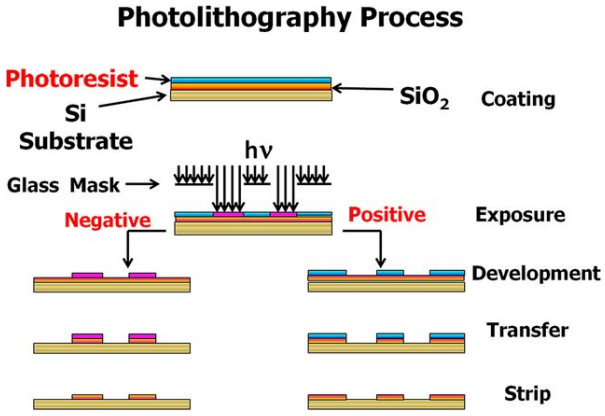


Figure 3.1: Steps performed in photolithography for both positive and negative photoresist [37]

3.1.2. Etching

Etching is a fabrication method to remove a layer from the surface of a wafer and can be done after lithography to create a pattern on the wafer. There are two methods of etching: wet and dry etching. Wet etching is done by immersing the wafer in an etchant solution, such as buffered hydrofluoric acid (BHF) or hydrofluoric acid (HF). Different specialised etchants can be used depending on the surface being etched. Wet etching methods used during this thesis are isotropic however, which means that it will not only etch parallel to the pattern made with the PR, but it will also etch in all other directions under the PR, causing an undercut. This isotropic etching could thus potentially negatively alter the pattern when etching for a long duration on a thicker material.

Dry etching on the other hand is an anisotropic process and makes used of plasma to etch the wafer. It involves ejecting an etching gas at the wafer into a lower pressure chamber, where plasma is created by applying a radio frequency voltage. The positively charged ions in the plasma are then shot toward the surface of the wafer. This plasma will chemically combine with the material on the wafer and will be removed with a vacuum pumping system [38][32]. An advantage of plasma etching over wet etching is that it is anisotropic, meaning less undercut will happen and the etching will be more precise. Dry etching also allows for better control of the etch rate compared to wet etching. The disadvantage of using dry etching for PV applications however is their chemical unselectivity. Unlike wet etching, which is chemically selective, plasma etching is less selective and can thus cause the layer underneath to be slightly etched, which will cause dangling bonds and thus reduce surface passivation. For dry etching, the Drytek Triode and the Trikon Omega are used during this thesis.

3.1.3. Plasma-enhanced chemical vapour deposition

Plasma-enhanced chemical vapour deposition (PECVD) can be used for the growth of layers such as thin film silicon, such as amorphous silicon, nanocrystalline silicon and silicon oxide and silicon nitride. PECVD allows the deposition at low temperatures between 200-400 °C. Depending on the material, a mixture of different gasses is converted into plasma in a reaction chamber at ultrahigh vacuum. This conversion is regulated through an oscillating electric field at radio frequency (RF) or very high frequency (VHF). The plasma generated atomic an molecular particles which form an interaction with the substrate allowing the formation of the desired layer. A PECVD reaction chamber is schematically represented in figure 3.2. The quality of the deposited layer is dependent on the pressure, temperature, gas flow rate and composition, and the power.

The tool used for PECVD for this thesis is the Concept 1 by Novellus and is used to deposit a silicon nitride layer on the wafer which acts as a passivation layer for the IBC cell.

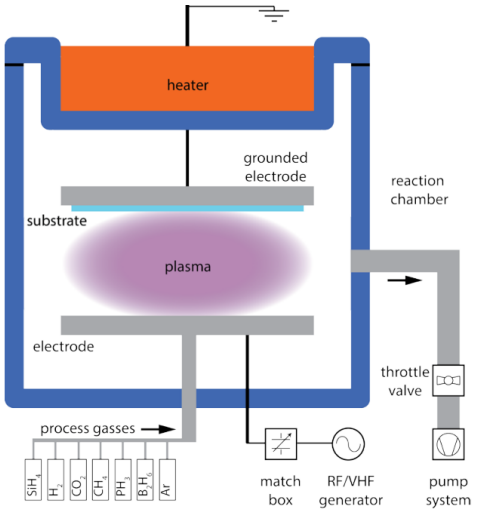


Figure 3.2: Schematic representation of a PECVD setup [39]

3.1.4. Low pressure chemical vapor deposition

Low pressure chemical vapor deposition (LPCVD) is another form of chemical vapor deposition. Unlike PECVD, LPCVD does not use plasma. Silane is heated up to temperatures in the range of 500-600 °C. Process conditions are usually controlled and selected so that growth rate is limited by the surface area reaction. This allows for excellent wafer to wafer uniformity. The slow process also means minimal diffusion of the reactant gasses, which will lead to a high level of uniformity and purity in the layer[40]. This thesis uses LPCVD for the deposition of the polysilicon layer.

3.1.5. Ion implantation

Ion implantation is a technique that is used in the semiconductor industry to introduce doping atoms into a semiconductor wafer. It is a very high precision technique which allows control over dopant species, dosage and implantation energy, which allows for accurate management of the doping profile of the device. Ion implantation starts by extracting positively charged ions from the ion source. These ions are then accelerated using an electric field and are bombarded at the surface of the wafer. Figure 3.3 shows a schematic representation of the process. Ion implantation is used during this thesis to implant the dopant regions of the source, drain and grounding contact. Different implantation energy and doses are implanted in the n-type wafer to analyze its effects on the performance of the PMOS transistors.

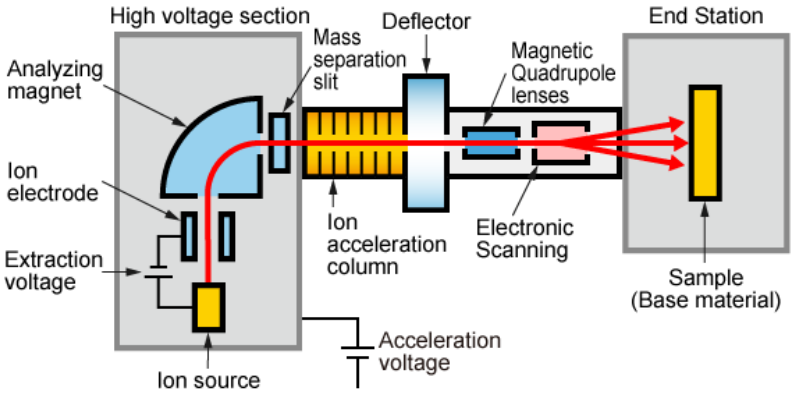


Figure 3.3: Schematic representation of ion implantation [41]

Ion channeling
In a crystalline structure such as c-Si, ions that are shot from the implanter could potentially pass through one of the openings in the structure. This cause the ion to travel much deeper into the substrate and increasing the implantation depth. For this reason, most implantation is carried out a few degrees off-axis.

Additionally, a scattering layer (dirt barrier) could also be used. In this case the substrate is covered with a thin amorphous silicon layer such as silicon dioxide, to scatter the implanted ions and therefore reducing ion channeling and improving the doping profile. Figure 3.4 shows the effects of the scattering layer on the depth of the boron implantation. This thesis will also research whether using a scattering layer will improve the performance of the MOSFET.

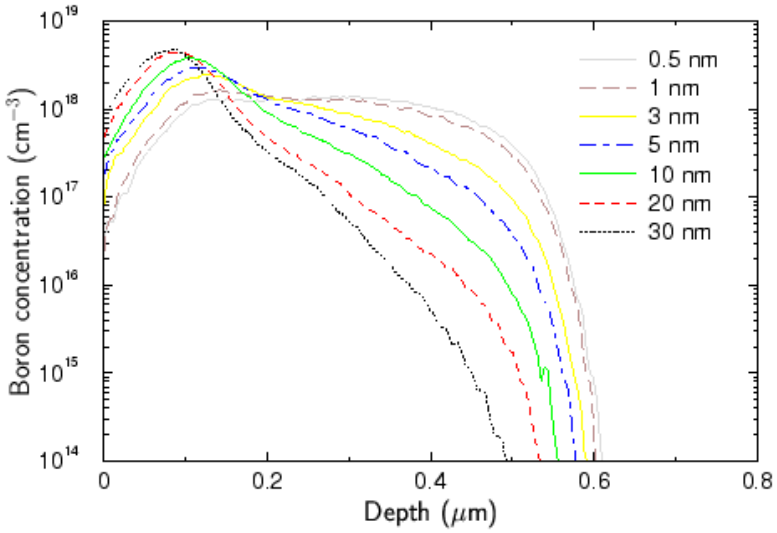


Figure 3.4: Simulated ion implantation of boron ions into <100> silicon through a scattering layer of SiO_2. The implantation was performed with an energy of 90 keV and a dose of $5{\cdot}10^{13}cm^{-2}$. A tilt of 7 ° (top) and 0 ° (bottom) were used. The scattering layer thickness was varied from 0.5 nm to 30 nm. [42]

3.1.6. Metal evaporation

Evaporation is method of physical vapour deposition (PVD), which means that it is a technology that produces the source gas by a non chemical method. It is mostly applied to metals. There are two types of evaporation: electron beam and resistive evaporation. In general during evaporation, the material is heated up above its melting point and consequently condensates when it contacts the cooler surface of the wafer. Resistive evaporation is performed in an open boat which is heated resistively by applying a high current. Electron beam evaporation is done by loading the metallic source in a water cooled crucible and is irradiated by an electron beam which heats the source [17]. These processes can be seen in figure 3.5

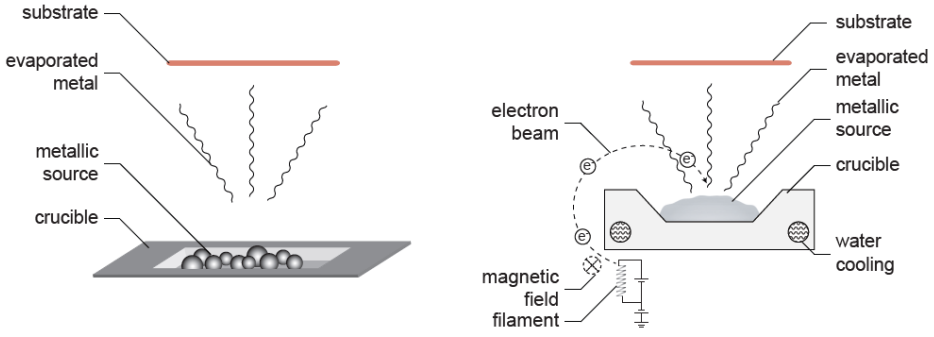


Figure 3.5: Schematic representation resistive evaporation (left) and electron beam evaporation (right) [43]

3.2. Fabrication method

This section will discuss the fabrication method of the MOSFET. The specification of the wafers used for fabrication can be found in table 3.1. For this project both n- and p-type wafers will be fabricated so to measure the performance of both NMOS and PMOS transistors, even though NMOS transistor generally perform better with the same physical dimensions than PMOS. The reason for this is that the PV market is shifting to n-type IBC solar cells due to their advantages, such as no light induced degradation and lower impurity sensitivity which improves recombination [17]. As this thesis is about integrating MOSFETS into IBC with changing as little as possible about the fabrication process, both NMOS and PMOS transistors are investigated to provide more information when integration of the MOSFET with the IBC is done. This also means that methods generally used for MOSFET fabrication will not be possible for this MOSFET fabrication process, as it would interfere too much with the fabrication of the IBC. The process used to fabricate the MOSFETs is described step by step, including visual clarification. A total of sixteen different wafers varying in substrate type, dirt barrier thickness, and implantation energy/dose were fabricated.

Table 3.1: c-Si Wafer specifications

Parameter	Value
Doping	n-type/p-type
Orientation	<100>
Finish	Double sided polished
Resistivity	1-5 Ωcm
Thickness	280 $\pm$ 20 μm
Diameter	100 mm
Brand	TOPSIL (floatzone)

3.2.1. Zero layer

A total of five masks are needed to fabricate the devices. It is essential that the patterns in the mask are correctly oriented to each other. In other words, the alignment of the mask to the pattern that is already on the wafer is within certain margins. For this reason, alignment markers are first etched into wafer near the edges, an example of which can be seen in figure 3.6. These markers can then be used to properly align each subsequent mask correctly. This is done by first coating the wafer with a layer of PR and exposing it using the mas *COMURK* in the ASML PAS5500/80 automatic wafer stepper. The wafer is subsequently etched in the openings of the PR using the Trikon Omega to etch the 120nm deep alignment markers into the silicon substrate. After removal of the PR and a cleaning step they will be ready for fabrication.

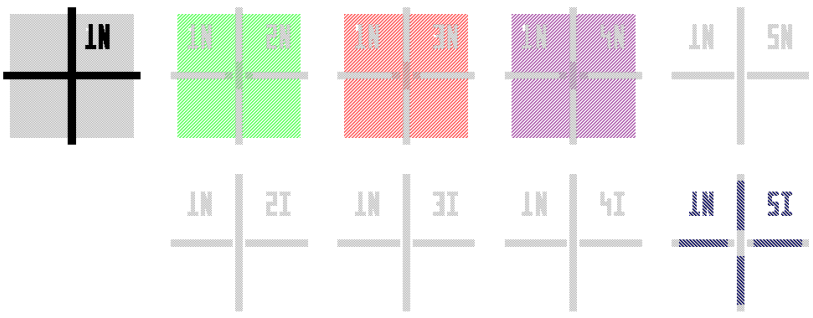


Figure 3.6: Example of alignment markers, the number signifies which layer has to be aligned while the letter defines the type of mask used

3.2.2. Gate definition

This section describes the production steps to fabricate the MOSFET gate. The process is described step by step below, visually clarified in figure 3.7.

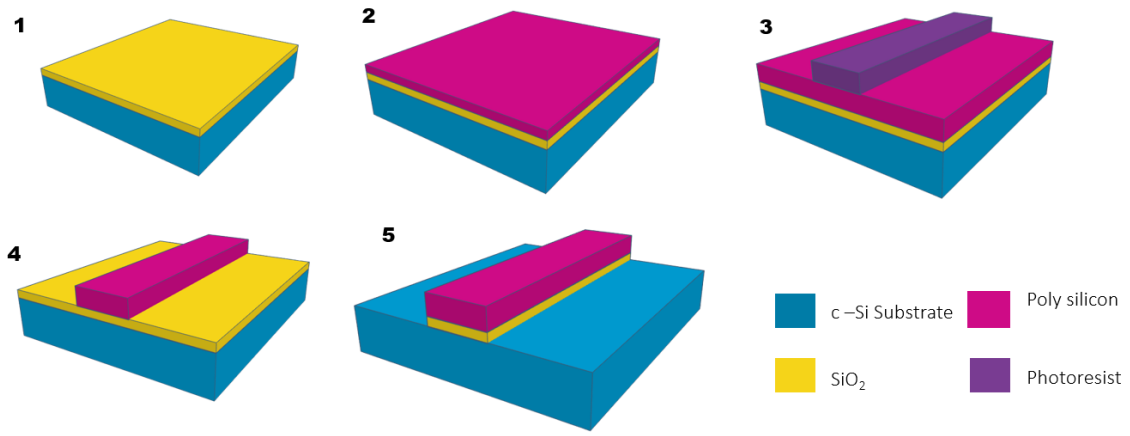


Figure 3.7: Schematic representation of the fabrication of the MOSFET gate

1. First a dry oxidation step of 42 minutes in a furnace at a temperature of 1050 °C is performed to grow a 40nm thick thermal SiO_2 layer. This SiO_2 layer will be used as the gate oxide between the gate and the substrate channel.

2. Afterwards, a 250nm thick amorphous silicon layer is deposited on top of the gate oxide using LPCVD deposition for 113 minutes inside an LPCVD furnace.This amorphous silicon layer will function as the gate of the MOSFET

3. After the silicon dioxide and amorphous silicon layer are deposited on top of the entire wafer, the gate area has to be defined. This is done by coating the wafers with positive PR SPR3012, with a thickness of 1.4μm. For exposure, mask $DVN1GATE$ is used for a exposure time of 10s and a total dose of 90mJ/cm^2. Afterwards, the wafer is developed.

4. After the wafer is coated and developed, the amorphous silicon layer is etched in the Trikon Omega plasma etcher for a etching time of 16 seconds. Subsequently the PR is removed and the wafer is cleaned.

5. Lastly, to remove the SiO_2 at areas it is not necessary, wet etching in BHF is used for approximately 70 seconds. The selectivity of BHF etching of SiO_2 is much higher that of silicon. This means that during BHF etching neither the amorphous silicon gate, nor the silicon substrate will be etched.

3.2.3. Implantation

This section describes the implantation of the various regions of the MOSFET, which are the source, drain and grounding contact. A grounding contact is used as a reference point to the substrate. The reason for also doping the grounding contact is to reduce the effects of the Schottky barrier diode, which occurs at a metal semiconductor interface. By increasing the dopant concentration, the voltage over the diode will be lowered[32]. Figure 3.8 give a visual representation of the process. Information regarding the scattering layer thickness, and implantation dose and energy can be found in table 3.2 and 3.3.

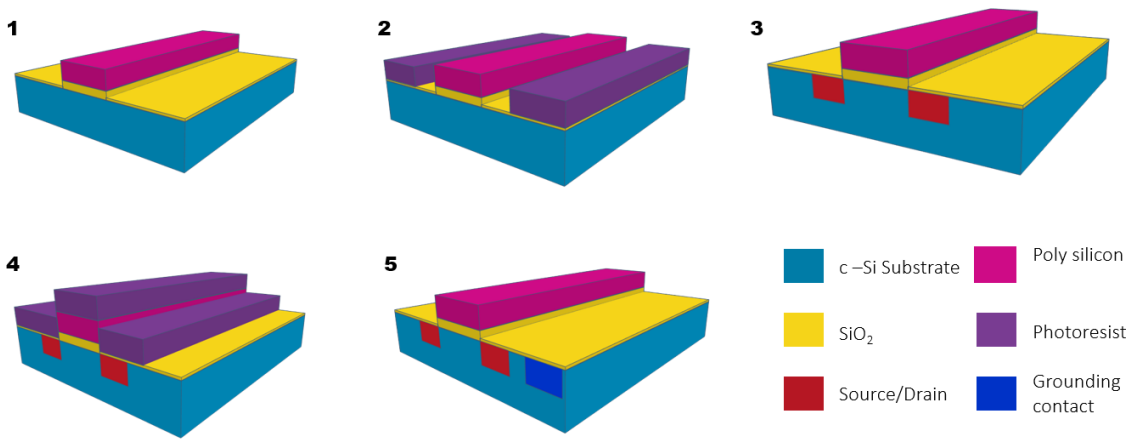


Figure 3.8: Schematic representation of the fabrication of the MOSFET implantations

1. First a SiO_2 scattering layers of various thicknesses ,shown in tables 3.2 and 3.3, is deposited on the wafers using LPCVD deposition at 400°C with a deposition rate of approximately 11.9nm/min.

2. After the scattering layer is deposited, the wafer is coated with positive PR SPR3012, with a thickness of 1.4μm. For exposure, mask $DVN2IMPSD$ is used for a exposure time of 10s and a dose of 90mJ/cm^2. Afterwards, the wafer is developed.

3. After coating and developing, the source and drain of the devices is implanted according to tables 3.2 and 3.3. These implantation characteristics are based on optimal solar cell processing conditions of the IBC cell[31] . After wich the PR is removed and the wafers are cleaned.

4. Subsequently, the wafers are again coated similar to step 2. This time using mask $DVN3IMPGR$ to allow for the implantation of the grounding contacts.

5. Lastly, the grounding contacts are doped by means of ion implantation, the PR is stripped, the wafers are cleaned and a thermal annealing step of 5 minutes in a nitrogen environment is performed. This annealing step is necessary to activate the implanted dopants.

6. After the thermal annealing is finished, the scattering layer previously used to prevent the ion channeling effect is no longer needed and is removed by an HF etch followed by marangoni drying. This consists of first a wet etching step using 0.55% HF, after which isopropyl alcohol (IPA) is applied to the wafer. IPA reduces the formation of native SiO_2 on the wafer. After applying the IPA the wafer is placed in a HNO_3 69.5 % bath at 110 °C for 10 minutes to perform nitric acid oxidation on silicon (NAOS).This replaces the scattering layer removed by the HF etch with a new SiO_2 layer. NAOS is used in the IBC design of [31] as tunneling oxide and is very thin (<2nm). This oxide reduces surface recombination.

Table 3.2: Implantation characteristics for NMOS transistors

p-type wafer/ NMOS		Source/Drain implantation (Phosphorus)		Grounding implantation (Boron)	
Wafer ID	scattering layer (nm)	Energy (keV)	Dose	Energy (keV)	Dose
1	0	20	6,00E+15	15	5,00E+15
2	0	20	6,00E+15	15	5,00E+15
3	0	20	6,00E+15	15	5,00E+15
4	0	20	6,00E+15	15	5,00E+15
5	10	20	6,00E+15	15	5,00E+15
6	10	20	6,00E+15	15	5,00E+15
7	20	20	6,00E+15	15	5,00E+15
8	20	20	6,00E+15	15	5,00E+15

Table 3.3: Implantation characteristics for PMOS transistors

n-type wafers / PMOS		Source/Drain implantation (Boron)		Grounding implantation (Phosphorus)	
Wafer ID	scattering layer (nm)	Energy (keV)	Dose	Energy (keV)	Dose
1	0	5	5,00E+15	20	6,00E+15
2	0	5	5,00E+15	20	6,00E+15
3	0	5	5,00E+15	20	6,00E+15
4	0	15	5,00E+15	20	6,00E+15
5	10	5	5,00E+15	20	6,00E+15
6	10	15	5,00E+15	20	6,00E+15
7	20	15	5,00E+15	20	6,00E+15
8	20	15	5,00E+15	20	6,00E+15

3.2.4. Metallization

The final step of fabricating the MOSFETS is the metallization. Before the aluminium can be deposited however, an additional layer of silicon nitride is deposited. This layer acts as a passivation layer and reflective coating for the IBC solar an cell but also as isolation for the metallization to reduce the semiconductor metal interface. A visual representation for this can be seen in figure 3.9

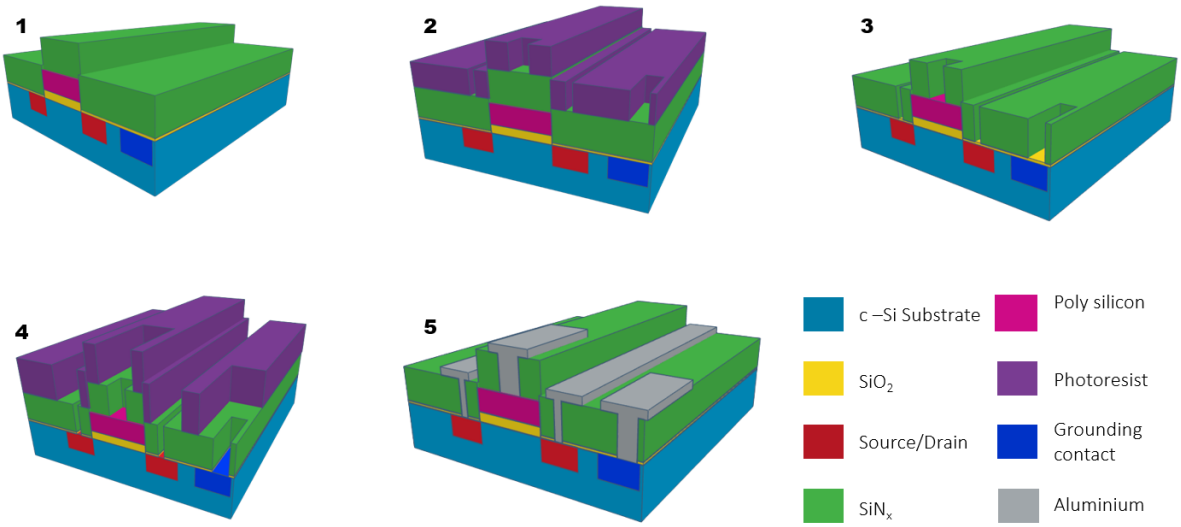


Figure 3.9: Schematic representation of the fabrication of the MOSFET metallization

1. Directly after NAOS, 300nm of SiN_x is deposited on the wafers using PECVD at 400°C
2. After the SiN_x deposition the wafer is coated with positive PR SPR3012, with a thickness of 1.4μm. For exposure, mask $DVN4OPEN$ is used for a exposure time of 10s and a dose of 90mJ/cm^2. Afterwards, the wafer is developed.
3. The contact openings on the wafer are then dry etched using the Drytek Triode for 56seconds using recipe $StdSiN$. Afterwards the PR is removed and the wafer is cleaned
4. Subsequently the wafer is again coated, only this time with negative PR. For exposure, mask 5 called $DVN5LIFT$ is used for a exposure time of 10 seconds. Afterwards, the wafer is dipped into HF(0.55%) for 4 minutes to remove the NAOS layer that is still remaining.
5. Immediately after the HF dip, 1.5 μm layer of aluminium is evaporated on top of the negative PR. Lastly, the PR and excess aluminium is removed using a process called lift off where the wafer is subdued in a chemical called N-Methyl-2-pyrrolidone (NMP) which reacts with the negative PR and thus removes it, together with the aluminium from the wafer.
6. After lift off, the wafer is annealed at 350°C for 5 minutes minutes by hot plating to improve the aluminium semiconductor interface.

3.2.5. Compromises in design

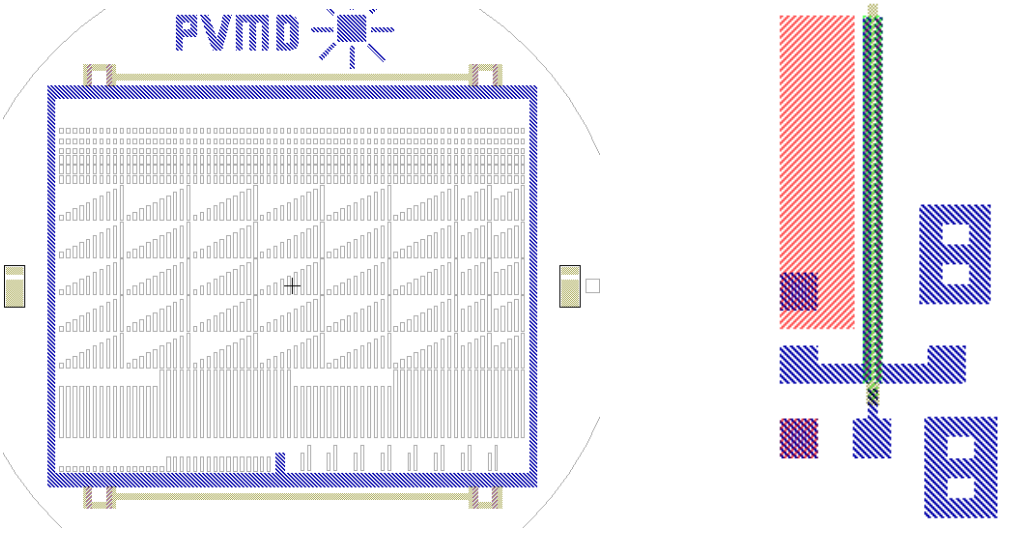
For this design, several compromises were made. One of which was to replace as many plasma etching steps as possible with chemical etching methods. This is due to the better passivation of the surface chemical etching yields compared to plasma etching, as was explained earlier. Another compromise was the direct fabrication of the MOSFET into the substrate. In the industry epitaxy is used to grow a higher purity layer on top of the substrate [17][32], allowing for better performing devices. However the IBC used as base for this design does not use such a layer [31], and therefore incorporating such techniques would prove very complex to properly integrate. Lastly, for the metallization, evaporation is used instead of metal sputtering. The benefit of Sputtering would be that it can be used to sputter 99%Al/1%Si for the metal contact reducing the chances of spiking, and subsequently the shorting of the devices, from occurring.

3.2.6. Wafer Layout

Since the features of the designed MOSFET are in the order of micrometers, it is inefficient to fabricate merely one MOSFET per wafer. Multiple MOSFETs with different feature sizes are fabricated per wafer, both for area efficiency along with a more reliable way of comparing the effects of different feature sizes with each other, as this nullifies the potential for variation in they process. Figure 3.10a show the layout of the whole wafer, while figure 3.10b shows the design of the final MOSFET. The wafer consist of fifteen rows of seventy MOSFETs for a total of 1050 MOSFETs per wafer. The gate lengths of row 1-9 are in ascending order from left to right, starting at 1μm up to 15μm. Rows 1-3 are identical to each other and have a gate width of 100μm. Rows 4-6 have a gate width of 500μm, and rows 7-9 are 1mm wide. This can be used to analyze the effects of different gate width and lengths on the I-V relationships.

Rows 10-14 are used to further analyze the effects on increasing the gate widths at 10 different intervals (500μm - 5mm) for different gate lengths (2-7μm). Increasing the gate width however, increases the maximum current throughput of the MOSFET. This however will in turn increase the resistive losses through the metal contacts, as they may be too small to properly handle such currents. For this reason, rows 10-14 also have an increasing metal width, 20μm up to 100μm.

The last row, row 15, consists of MOSFETs with a high gate width (7.5mm-10mm) for various gate lengths and metal widths.



(a) Schematic layout of the whole wafer (b) Schematic layout of a single wafer

Figure 3.10: Layout of the whole wafer (a) and a single MOSFET(b)

3.3. Characterization tools

This section describes the various characterization tools that were used during this thesis project.

3.3.1. Ellipsometry

When designing semiconductor devices it is important to know the exact thickness of the applied layer. These values can be measured using spectroscopic ellipsometry. Additionally optical constants can also be determined by fitting the measurements with an appropriate model. This thesis uses ellipsometry to accurately measure PECVD deposition that is needed for the passivation layer as well as to determine etching rate of certain etching techniques.

Spectroscopic ellipsometry is a technique that measures the difference between incident light and scattered light to determine the optical properties of the surface material[44]. Figure 3.11 shows a schematic process of this.

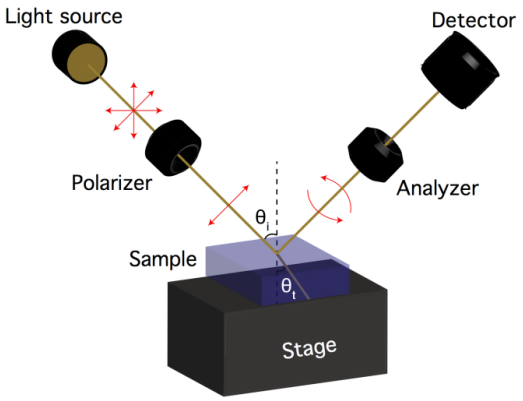


Figure 3.11: Schematic representation of spectroscopic ellipsometry [45]

3.3.2. Performance measurements

Measurements done regarding MOSFET performance are conducted using the Cascade probe station, shown in figure 3.12 The Cascade is used to connect the contacts of the MOSFET with the characterization tool. Connected to the Cascade is the Agilent 4156 Precision Semiconductor Parameter Analyzer. This device is used to measure the DC performance of the MOSFET, such as the I_D v. V_{DS} and I_D v. V_{GS} current voltage relationships.

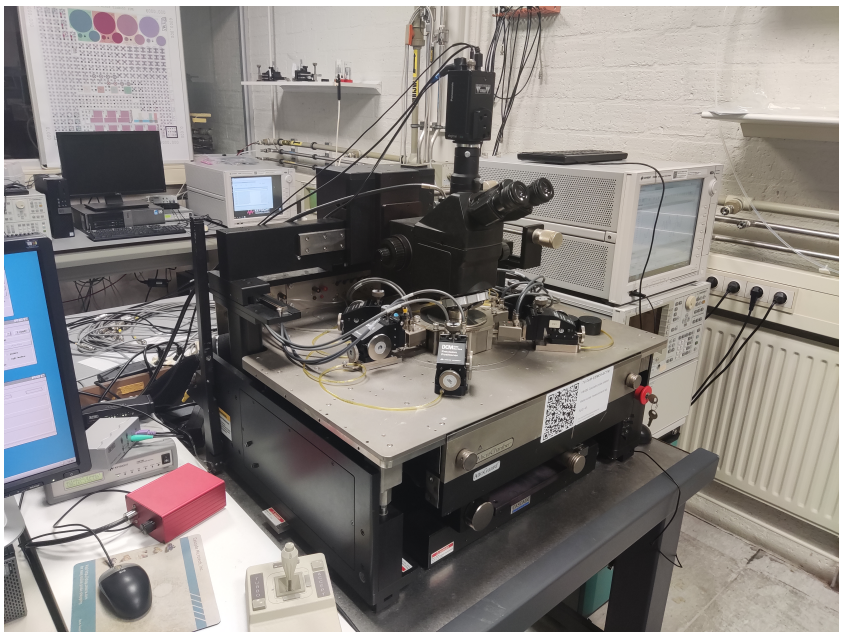


Figure 3.12: Cascade probe station

The AC characteristics of the of the MOSFET are measured using the Agilent 4284A Precision LCR Meter. This LCR meter can measure the series and parallel capacitance and resistance between two contacts of the MOSFET.

The effect of incident light on the performance of the MOSFET is measured by placing LED of the desired wavelength on top of the Cascade from a distance of 7cm from the wafer. Using a Power supply, the intensity of the LED can be altered and its effects can be measured. This was done for 3 different types of LEDs. The effects of 'Blue'(462nm) and 'Red'(641nm) light were measured separately to compare the effects of photons with different energy in addition to full spectrum measurement to have more realworld comparison. The spectral irradience for these LEDs can be found in figure 3.13. For the blue and red light irradiences up to 300W/m^2 were measured, while for the full spectrum LED the effect of an irradience up to 1000W/m^2 was measured.

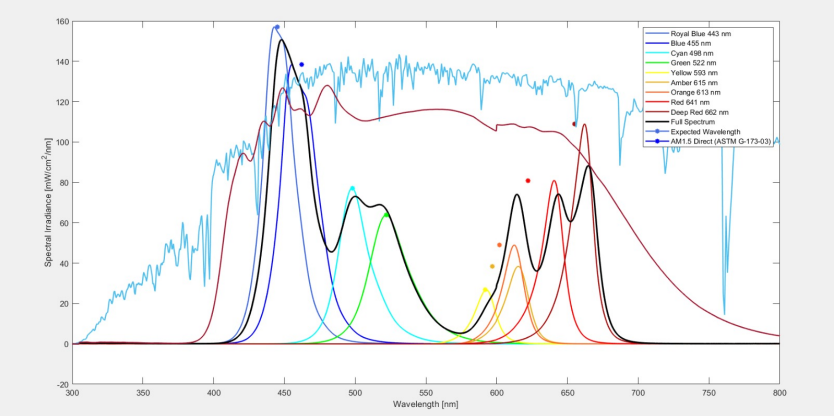


Figure 3.13: Spectral irradience of the used LEDs

4

DC Characterization

This chapter will focus on the DC characteristics of the fabricated MOSFETs, such as the threshold voltage and I-V relationships. Furthermore, the effects of different gate lengths, widths, and metal contact widths will be analyzed. Additional to single wafer measurements, the performance of the MOSFETs between the different wafers is also analyzed. A total of 12 different wafers were fabricated, 6 wafers with PMOS and 6 with NMOS transistors, with differences between implantation doses and dirt barrier thickness . This chapter will also look at the effects of light on the performance of the MOSFETs. Moreover in order to optimize the MOSFET performance, tests were done regarding the ideal annealing time and temperature. Lastly, one of the wafer fabricated was made using a SiN_x passivation layer and aluminium evaporation for the metal contacts, but rather using SiO_2 as passivation layer and mixture of 99%Al/1% was sputtered on the wafer instead. Whether this change effects the MOSFET performance will also be analyzed this chapter. Table 4.1 and 4.2 shows the differences in fabrication between the different wafers.

As is mentioned earlier, the final MOSFET design should be suitable to handle both the short circuit current of a solar cell, as well as the open circuit voltage to prevent any of the breakdown mechanisms to initiate. However the device as to operate on low drain to source voltage (<100mV) to minimize the voltage loss over the device.

Table 4.1: Differences between NMOS wafers

NMOS Wafer ID	scattering layer (nm)	Comment
3	0	
4	0	
5	10	Wafer 4 was made with a
6	10	SiO_2 insulation layer instead
7	20	of SiN_x,Al evaporation was
8	20	replaced with Al/Si sputtering

Table 4.2: Differences between PMOS wafers

PMOS Wafer ID	scattering layer (nm)	Source/Drain implantation (Boron) Energy (keV)
3	0	5
4	0	15
5	10	5
6	10	15
7	20	15
8	20	15

4.1. Threshold voltage derivation

The threshold voltage is an important parameter in MOSFET characterization as it represents the onset of large current flow through the device. Formulae 2.6 and 2.7 can in theory be used to calculate the threshold voltage. However since these formulae are derived from ideal scenarios, they may differ from the actual threshold voltage of the device. For this reason, threshold voltage value extraction is generally done using I_D v. V_{GS} characteristics of the device[46].

A widely used method of obtaining the threshold voltage V_T is by linear extrapolation(LE). It is done by finding the x-axis intercept point from linear extrapolation of the I_D v. V_{GS} curve at its maximum slope. This point of maximum slope is also the point of maximum transconductance (g_m) and can be found by taking the derivative of the I_D v. V_{GS} curve. From that point the tangent can be drawn and the threshold voltage is then determined from the x-axis intercept, as is shown in figure 4.1a, where the threshold voltage is approximately V_T = 0.06V for this NMOS device. The same method can be used for PMOS devices, as is shown in figure 4.1b One drawback to this method is that the maximum transconductance is strongly influenced by mobility degradation and parasitic series resistance of the source and drain [47]. However for the scope of this project this method will suffice.

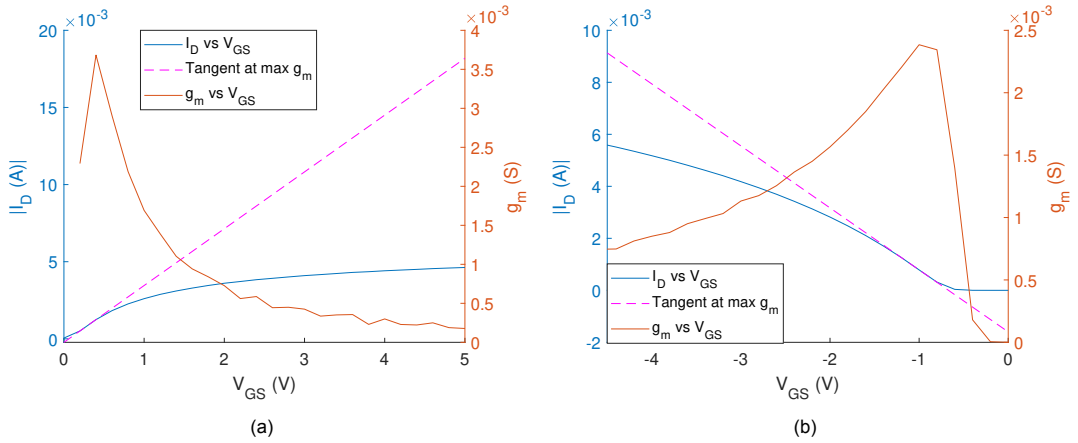


Figure 4.1: Threshold voltage derivation using linear extrapolation for an NMOS(left) and PMOS(right) transistor. I_D vs V_{GS} (blue), g_m vs V_{GS} (red) and linear approximation (magenta)

The threshold voltage is not only affected by mobility degradation however. Both short and narrow channel effects influence the threshold voltage [32]. For NMOS transistor, shortening the channel decreases the threshold voltage. This effects occurs due to the space charge regions of the source and drain. For long channels, this space charge region is only a small part of the channel and the gate voltage will essentially control the whole channel. As the channel length decreases, this fraction controlled by the the space charge regions becomes relatively larger. In turn, the gate will control less of the bulk charge, which affects the threshold voltage.

Adversely to short channel length effects, were the gate controls relatively less area for shorter gate lengths, the gate controls relatively more area in narrow channels. The depletion region of the gate extends along the width of the device over its edges, meaning that the gate controls additional charge. This effects becomes more prevalent at narrow channels, as the additional space charge region becomes a larger fraction of the total charge. The relationship between the narrow channel effect and the threshold voltage is quantified in formula 4.1. Where increasing the gate width decreases the threshold voltage. Additionally, the doping uniformity in the c-Si substrate differs widely, which also influences the threshold voltages.

$$\Delta V_T = \frac{eN_a x_{dT}}{C_{ox}} \left(\frac{\xi x_{dt}}{W}\right) \tag{4.1}$$

All of this can be seen in figure 4.2 where the threshold voltage for increasing gate length as well as increasing gate width has been plotted for n-type wafer 7 with PMOS devices. Figure 4.2 shows the results according to what is expected, showing small shifts in threshold for increasing gate widths and

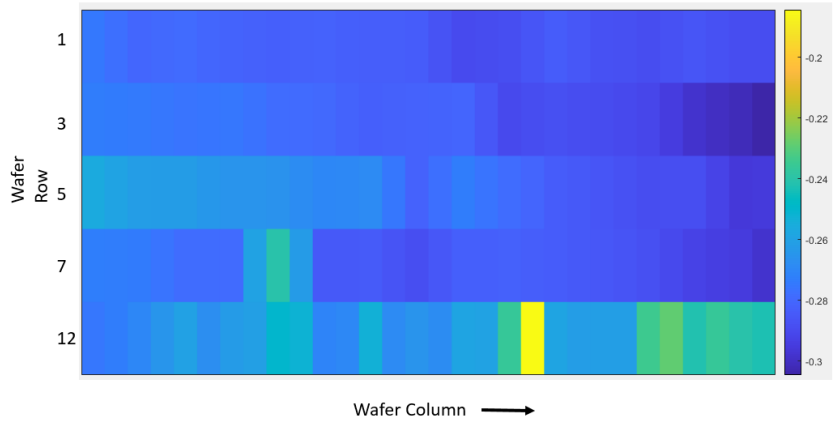


Figure 4.2: Heatmap of the threshold voltage of different devices for rows 1-7 the columns indicate increasing gate length, for row 12,gate width/metal thickness

lengths. The outliers can possibly be explained by variance in the substrate doping of the wafer. A similar effect can also be seen across p-type wafers with NMOS devices

There are however also differences between device with the same implantation and physical dimension across different wafers however as is shwon in figure 4.3. A possible explanation be explained by the effects of the scattering layer present on some of the wafers. As is mentioned in chapter 3.1.5, the scattering layer inhibits the effects of ion channelling limiting the doping depth and increasing the dopant concentration near the oxide surface during diffusion. Comparing the average threshold voltage of 10 different devices across PMOS wafers 4, 6 and 7, which have a scattering layer of 0nm, 10nm and 20nm respectively shows that having a scattering layer reduces the absolute value of the threshold voltage with more than 20% as can be seen in figure 4.3. A possible explanation for this relationship is that during annealing of the wafers, implanted ions diffuse towards the substrate region under gate effectively reducing the dopant concentration in that region, shifting the threshold voltage. Using a scattering layer will cause a much higher concentration at the surface and improve the implantation tail [48], possibly reducing the effects of this diffusion by reducing the implanted area, lowering the amount of ions diffusing to under the substrate. Another possibility is that some of the implanted ions get trapped in the scattering layer, therefore reducing the dopant concentration. This increases the series resistance of the device, lowering the I_D vs v_{GS} curve and shifting the threshold voltage. Alternatively, this could also be seen as measurement errors, as the total differences in threshold voltage is relatively small (≈0.08V). An error in the extraction of the maximum transconductance due to a low resolution of the could potentially cause this error. Figure 4.1b for example shows that the actual maximum transconductance is somewhere in between two of the measurement points causing an error.

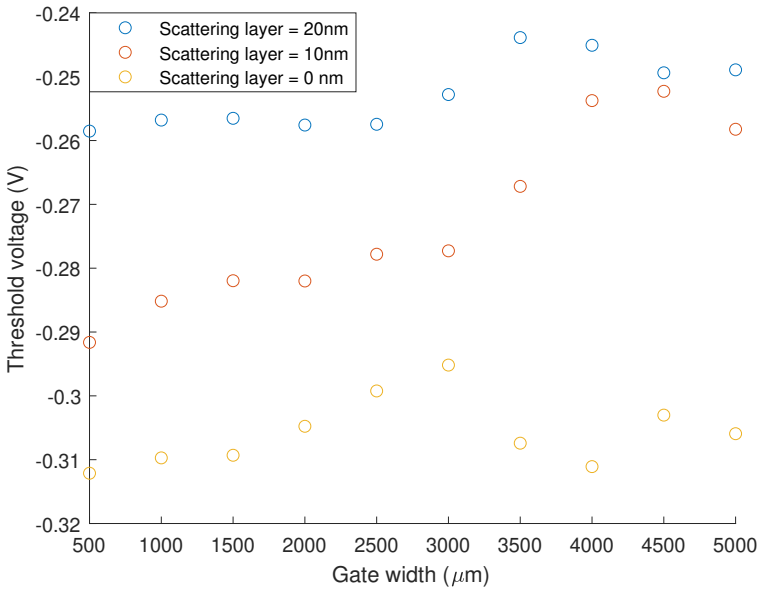


Figure 4.3: Relationship between scattering layer and threshold voltage for increasing gate width for PMOS transistors, L = 4μm, V_{DS} = 100mV.

Furthermore, the transconductance, g_m, is also linearly related to the gate width and length according to formula 4.2. Similar to the drain current, increasing gate width increases the path the current has to laterally flow through and thus increasing its transconductance. Likewise, increasing the gate length decreases the transconductance. Figure 4.4 shows the relationship between the gate width/length and the maximum transconductance. It can be seen that g_m does decrease linearly with gate length and increases linearly with gate width.

$$g_m = \sqrt{\frac{1}{2}\frac{W}{L}\mu C_{ox} I_D} \tag{4.2}$$

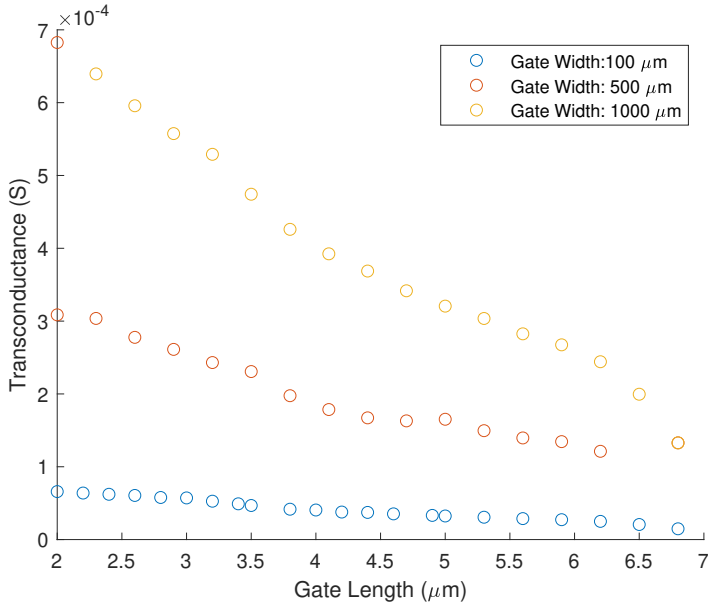


Figure 4.4: Effect of gate width and length on transconductance.

4.2. I-V measurements

In this section the effect of various variations in the MOSFET fabrication and geometry on the I_D v. V_{DS}. This includes the effect of increasing the gate width, metal width, implantation dose and dirt barrier thickness. Another important aspect in I_D vs V_{DS} relationship is the channel resistance. The channel resistance is an important aspect of the transistor losses, and thus a very important parameter.

Furthermore, the MOSFET must also be able to handle the current generated by the solar cell, while still operating at a low drain to source voltage, in order to minimize losses. As the resistance of the MOSFET becomes extremely high in the saturation region, causing losses. These effects will be analyzed in this section.

4.2.1. Effect of gate width on drain current

According to formula 4.3, the drain current of a MOSFET is linearly related to its gate width , W. This is only in theory however as realistically, if the gate width would become sufficiently large, a voltage drop would occur laterally over the width due to the increased path length of the current. Figure 4.5 shows a schematic representation of the amount of current flowing though MOSFETs with large gate widths. At a certain gate width, the voltage drop over the width will be so high that it negates any gain of the increased current flow.

$$I_D = \mu_n C_{ox} \frac{W}{L}((V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2) \tag{4.3}$$

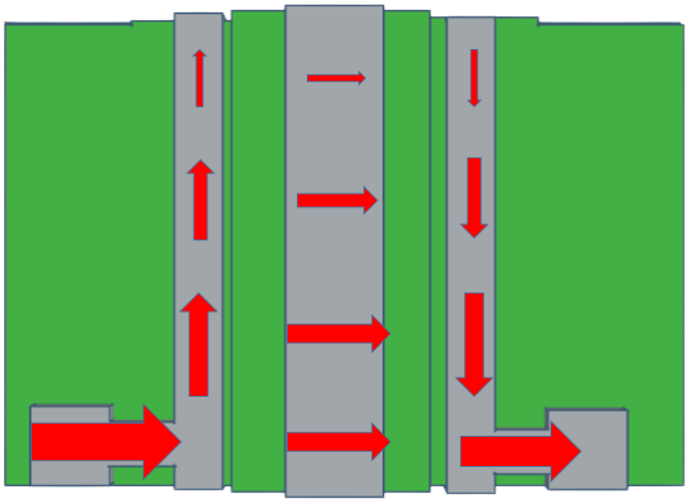
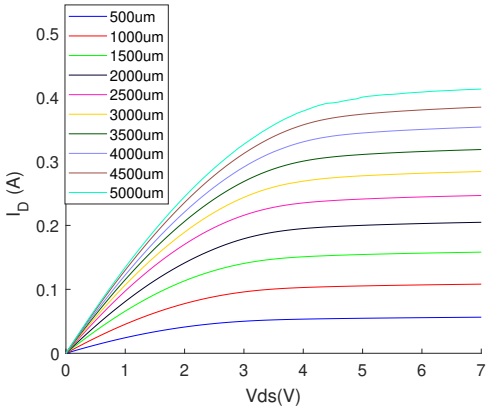


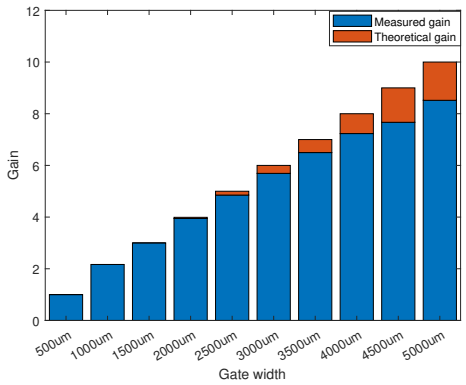
Figure 4.5: Effect of large gate width on current flow. Total current density is indicated by the size of the arrows.

As such there exists a gate width were further increasing it does not yield any sufficient advantage. Add to this the fact that increasing the width of the device means decreasing the usable surface area for the solar cell. Selecting the proper gate width is paramount to the MOSFET operation when integrated with a solar cell to reduce any unnecessary losses.

Figures 4.6a and 4.6b show the relationship between increasing the gate width and its associated current for NMOS wafer 8 at $v_{GS} = 5V$. Figure 4.6b shows how much the ratio of the drain current of a device is compared to the 500μm device for increasing gate widths. It can be seen from figure 4.6a that the drain current does increase with increasing gate width. However, figure 4.6b shows that, while the drain current may be increasing according to formula 4.3 for smaller gate widths, for larger gate widths the previously mentioned voltage drop makes that the gain deviates from the expected trend. It can be seen that losses become significant for MOSFETs with larger gate widths than 3000μm



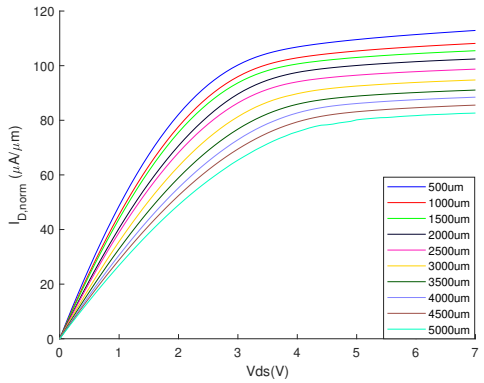
(a) I_D vs V_{DS} for increasing gate width.



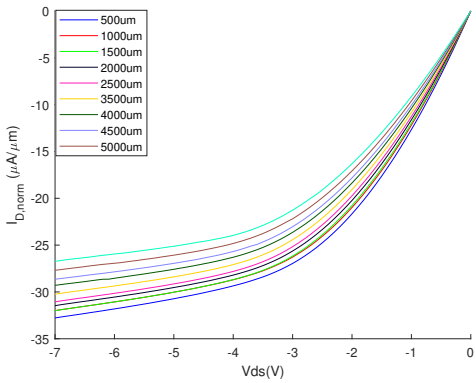
(b) Ratio of the drain current of larger gate width MOSFETS compared to an NMOS MOSFET with a width of 500μm

Figure 4.6: Relationship between drain current and gate width for NMOS wafer 8, L = 4μm, metal width = 60μm

Another method of looking a the losses from increasing the width, is by looking at the normalized linear current density for each device width. This way the current carried by every μm of width for every device can be objectively compared. Figure 4.7 shows the linear current density of the MOSFETs of various gate widths. A clear relationship between the device width and its current density for both NMOS and PMOS is visible. This indicates that the wider devices are have more relative losses in the metal source and drain contacts compared to smaller devices and offer comparatively lower performance. Although this effect seems more pronounced with NMOS devices, where the decrease between 500 μm and 5000μm is approximately 30%, compared to the PMOS devices, which has a decreased density of roughly 20%. This difference could be explained by the post annealing step explained in section 4.4. The annealing creates an additional layer of aluminium silicide which behaves as a p-type semiconductor, thus effectively increasing the dopant concentration of the PMOS transistor. Table 4.4 also shows how the annealing is more beneficial for PMOS compared to NMOS transistors, thus explaining the difference in current density drop for wider devices.



(a) Normalized linear current density vs V_{DS} for increasing gate width for NMOS wafer 8. V_{GS} = 5V, L = 4μm, metal width = 60μm



(b) Normalized linear current density vs V_{DS} for increasing gate width for PMOS wafer 4. V_{GS} = 5V, L = 4μm, metal width = 60μm

Figure 4.7: Relationship between normalized drain current and gate width for NMOS and PMOS devices.

However, the channel resistance also decreases with increasing gate width. The larger cross section of the wider MOSFETs allow the current to more easily flow through the device, decreasing its resistance. For this only the linear part ($V_{DS} < 2$V) of the triode region is taken into account, as this is where the resistance is the lowest and the devices will operate in. To calculate the channel resistance r_{on} in this linear region, simply the slope of the curve has to be calculated. Since the curve is linear for $|V_{DS}| < 2$V the channel resistance can be calculated the following way:

$$r_{on} = \frac{\Delta V_{DS}}{\Delta I_D} \tag{4.4}$$

Calculating these resistances for various gate widths is shown in table 4.3. Figure 4.8 shows the same data plotted in a graph. From this graph it is clear that the on resistance has an inverse exponential relationship with gate width. The resistance increases exponentially for decreasing device widths.

Table 4.3: Conduction resistance for both NMOS wafer 8 and PMOS wafer 7 devices at various gate width. V_{GS} = 5V, L = 4μm, metal width = 60μm

Gate Width (μm)	$R_{on,NMOS}$ (Ω)	$R_{on,PMOS}$ (Ω)
500	48.6	167.4
1000	25.7	83.3
1500	17.6	55.4
2000	14.1	49.5
2500	11.7	36.5
3000	10.5	29.2
3500	9.6	25.6
4000	9.0	22.7
4500	8.4	20.8
5000	8.1	19.6

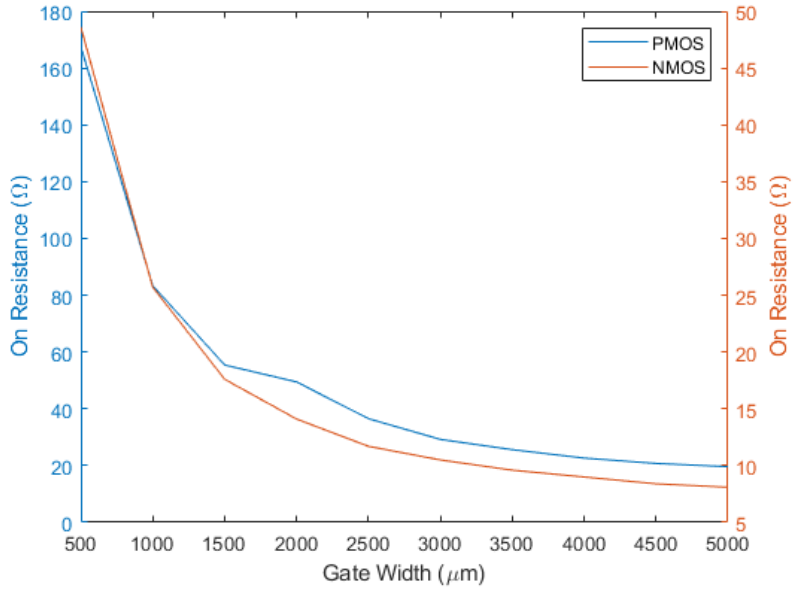
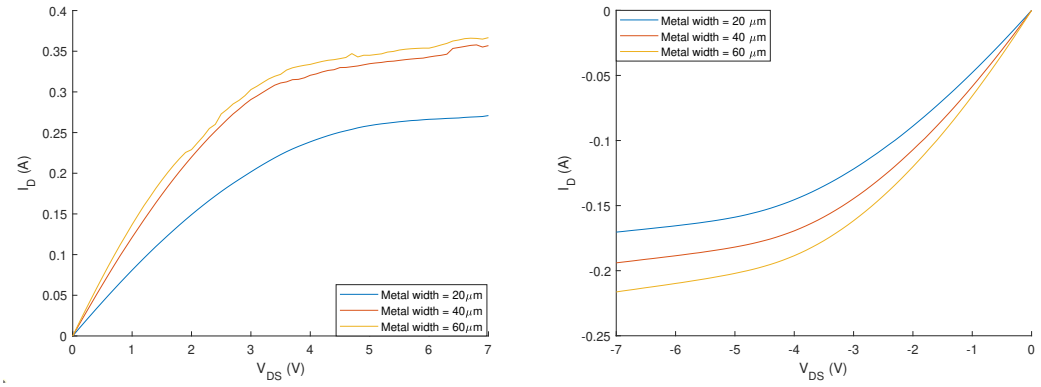


Figure 4.8: The On resistance of PMOS and NMOS transistors for various gate widths.

4.2.2. Effect of metal width on drain current

A way to reduce the current drop for wider devices shown in the previous section is by increasing the cross section of the contacts, as is illustrated in figure 4.9. wider metal contacts reduce the resistance of the contact and thus reduces the voltage drop over it. For this different metal widths were compared with each other for performance. These differences can be seen for both NMOS and PMOS in figures 4.10a and 4.10b respectively.



(a) Difference between I_D vs V_{DS} curves for different metal widths for NMOS wafer 6, $V_{GS} = 5V$, L = 4 μm, W = 5000μm

(b) Difference between I_D vs V_{DS} curves for different metal widths for PMOS wafer 7, $V_{GS} = -5V$, L = 4 μm, W = 5000μm

Figure 4.10: Relationship between drain current and metal width

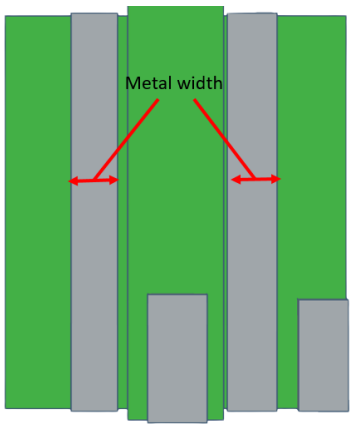


Figure 4.9: Illustration of the metal width of the source and drain of a device.

The figures show that wider metals indeed do improve current throughput, in both triode and saturation region. From this it can be concluded that in order to improve the current throughput as well as minimize losses from large gate width, wider metal contacts can be used. Downside is however that wider metal devices require considerably larger surface areas. The gained current and channel resistance is however not linear to the increased surface area and therefore a careful consideration has to be made between the used surface area and the improved performance

4.2.3. Effect of scattering layer on drain current

As was explained in chapter 3.1.5, scattering layers help prevent ion channelling and thus improve surface implantation of the source and drain of the MOSFET. A better doping profile has considerable effects on the I_D vs V_{DS} curves, as is seen in figure 4.11. Both channel resistance as well as maximum drain current in saturation are considerably higher for devices with a dirt barrier. A possible explanation for the higher drain current for devices with thicker scattering layers is the change in threshold voltage. It has been shown in this chapter that a thicker dirt barrier causes the threshold voltage to shift towards zero. This then increases the overdrive voltage, increasing the drain current of he device.

From this it can be concluded that a scattering layer is an important addition to the MOSFET fabrication process, as even adding a thin dirt barrier of 10nm already improves performance of the device considerably. Even though the scattering layers experimented in this thesis, thinner scattering layers could also be tested in further research. NAOS, for example is already a widely used method of oxidization for the fabrication of the IBC cells and produces a SiO_2 layer of approximately 1-2nm. The effects might be less impressive for such thin layers, but it can be more easily integrated in the combined fabrication process opposed to a dedicated thermal annealing step, saving time and money.

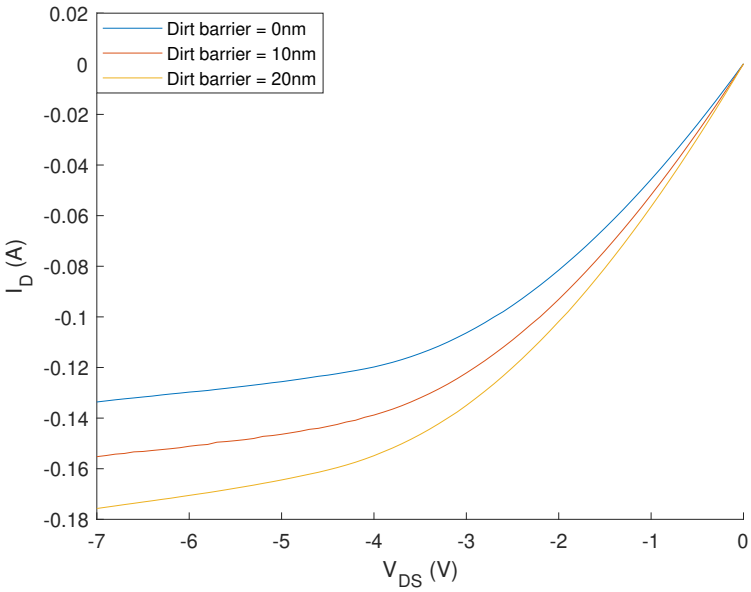


Figure 4.11: Comparison of I_D vs V_{DS} curves for different dirt barrier thicknesses. V_G = 5V, L = 4μm, W = 5000μm

4.2.4. Effect of implantation energy on drain current

While all of the NMOS wafer were implanted using exactly the same dose and energy (20kEv, 6e+15), the effect of differing implantation energies were tested for boron implantation of the PMOS transistors(5kEv and 15kEv). The reason for this is that Boron penetrates deeper into the substrate compared to phosphorus at the same implantation energy[49]. Thus using the same implantation energy will cause a large doping profile tail and reduce device performance. Figure 4.12 shows that devices implanted with a lower energy actually have a 20% higher drain current than devices implanted with higher energy. This could be explained similar to the effect of the scattering layer. Lower energies causes the ions to be implanted less deep into the device, reducing the doping profile depth and increasing the surface concentration.
The effect is slightly lower for devices which were implanted while having a scattering layer. In this case the added benefit of using lower energies only improved the average drain current with approximately 10%. Nonetheless, using lower energies significantly improves the current handling capabilities of the devices. Adding all these fact together leads to the conclusion using 5kEv for the ion implantation of n-type wafers would be all around better. A definite conclusion cannot be made for the p-type wafers with NMOS transistors. This is due to the lower implantation depth of phosphorous. which may possibly not be able to penetrate thicker scattering layers with lower implantation energy However, since the same mechanics apply in both instances, further testing has to be done for a definitive answer.

4.3. MOSFET breakdown voltage

In this section the breakdown voltage of the devices will be analyzed. Two types of breakdown will be discussed, the first one will be dielectric breakdown, and the second one will be avalanche breakdown. Dielectric breakdown occurs when the electric field in the oxide is sufficiently strong to break the oxide down. In the case of a MOSFET this means increasing the gate to substrate voltage to a high level. The gate oxide thickness for these MOSFET is 30nm which means that breakdown occurs at 18V and operational limits would be 6V, to prevent any defects in the oxide from causing early breakdown of the device .

Another type of breakdown that can occur is avalanche breakdown. This breakdown happens when the drain to source voltage is increased sufficiently. Figure 4.13 shows avalanche breakdown happening for both NMOS (figure 4.13a) and PMOS(figure 4.13b). These figures show that the NMOS and PMOS devices reach avalanche breakdown at different potentials. NMOS breaks down around 11V across deivces with varying dimensions while PMOS devices can hold much higher voltages and only start

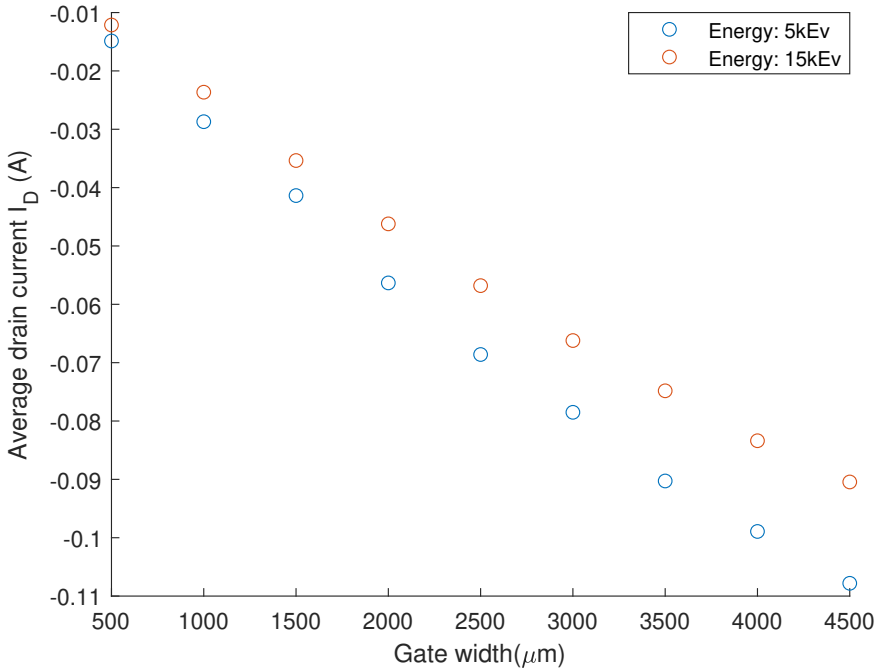
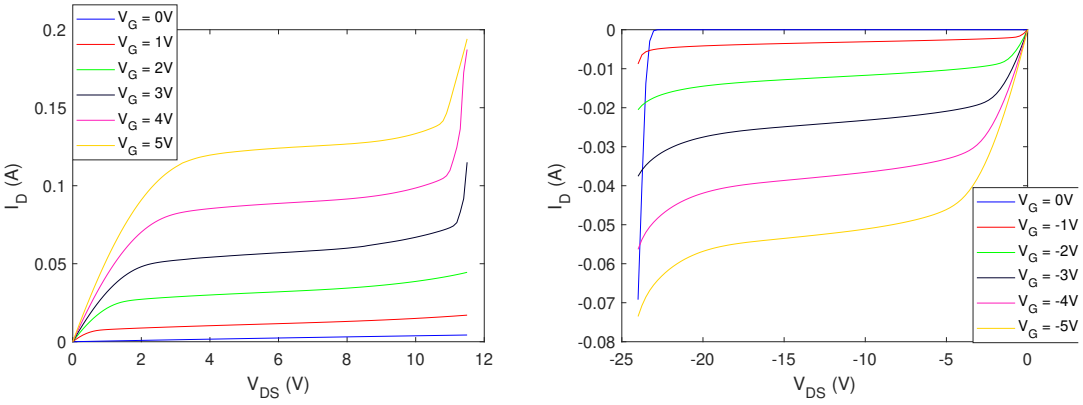


Figure 4.12: Comparison between different implantation energies for PMOS transistors with varying gate widths. PMOS wafers 3 and 4 were compared, V_{GS} = -5V, L = 4μm, V_{DS} = -7V

breaking down at -23V. This could explained by their charge carrier mobilities. Avalanche breakdown essentially happens due to free electrons with high acceleration knocking other bound electrons free, in turn the freed electrons accelerate as well and they then too knock other bound electrons free, causing an avalanche effect. Since electrons have a approximately 10x higher mobility then holes [50], they reach their necessary speed to free bound electrons at lower electric field strengths then holes. Due to this PMOS devices can achieve higher drain to source voltages before entering breakdown.



(a) NMOS avalanche breakdown

(b) PMOS avalanche breakdown

Figure 4.13: Avalanche breakdown of NMOS wafer 4 and PMOS wafer 7 devices, W = 1000 μm, L = 4μm.

4.4. Optimizing of post annealing

After metallization of the devices, usually an annealing step is performed. This annealing is done to improve adhesion, eliminate electrical damage associated with the metal deposition process, prevent the interface trap[51] and lower the threshold voltage by reducing the surface charge [32]. However, when aluminium on silicon gets annealed, a layer of aluminium silicide (AlSi) is formed. AlSi is a p-type semiconductor, where the doping concentration increases with higher temperatures and longer

annealing. This means that for the NMOS transistor, which have n-type doped region in contact with p-type doped AlSi could decrease performance if the wafer is annealed for too long and at a too high temperature. Likewise, the PMOS devices could see the inverse effect, an annealing step with a longer duration at a higher temperature could prove to be more beneficial for the device performance. This can not be done indefinitely however, as the eutectic temperature of aluminium and silicon is around 577 °C and spiking may occur, shorting the devices. A careful consideration must be made for the post annealing conditions of the devices. In this section the MOSFET performance for different temperatures and annealing times was analyzed.

Table 4.4 shows the effect of different temperatures on the average I_D vs V_{DS} curves. The table shows that annealing at 350°C is still better for NMOS transistor. The performance difference between 250°C and 350°C is possibly due to the surface charge at the Si/SiO_2 interface not being completely removed, therefore not reducing the threshold voltage equally and thus performing worse. The difference between NMOS and PMOS transistors for the same annealing condition can be explained by the additional doping the PMOS receives from the AlSi.

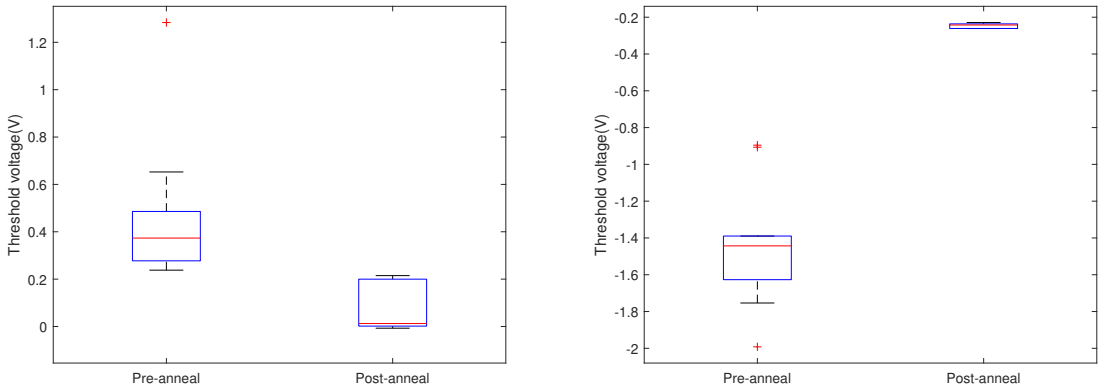
Table 4.4: Comparison of drain current improvement at V_{DS} = 5V pre and post hot plate annealing

Gate width (μm)	% Improvement of Average drain current			
	PMOS 5min at 250°C	PMOS 5min at 350°C	NMOS 5min at 250°C	NMOS 5min at 350°C
500	+115%	+241%	+43%	+92%
1000	+88%	+214%	+31%	+103%
1500	+75%	+184%	+38%	+94%
2000	+62%	+204%	+33%	+93%
3000	+56%	+185%	+27%	+85%
3500	+55%	+179%	+28%	+77%
4000	+53%	+170%	+26%	+76%
4500	+52%	+166%	+29%	+74%
5000	+50%	+148%	+24%	+72%

Another notable effect is that annealing has a considerably better effect on devices with a smaller gate width compared to wider devices. This could be due to the larger contact area for wider devices allowing current to already more easily flow through the silicon aluminium interface. Similar to how adding an additional lane to a 6 lane road will have less effect to congestion than adding a lane to a 2 lane road.

Further more annealing also has a significant effect on the threshold voltage. The threshold voltage is largely influenced by the trapped surface charge,Q'_{SS}, shown in formula 4.5. Figures 4.14a and 4.14b show the box plots of the threshold voltages for both NMOS and PMOS pre- and post-anneal. It can be seen that annealing significantly reduces both the variance as well as the mean threshold voltage. This could also explain the difference between the drain current improvement of the PMOS and NMOS, as figure 4.14 show that annealing had a more significant effect on the PMOS devices compared to NMOS devices. If the threshold voltage is lowered, the operating current is higher due to an increased overdrive voltage (V_{GS} - V_{th}).

$$V_{TN} = \frac{|Q'_{SD}(max)|}{C_{ox}} - \frac{Q'_{ss}}{C_{ox}} + \phi_{ms} + 2\phi_{fp} \tag{4.5}$$



(a) Boxplot of threshold voltage for NMOS devices pre- and post-anneal of 10 random transistors.

(b) Boxplot of threshold voltage for PMOS devices pre- and post-anneal of 10 random transistors.

Figure 4.14: Boxplot of PMOS and NMOS pre anneal and after annealing for 5 minutes at 350°C.

From these experiments it can be concluded that annealing at a slightly higher temperatures of around 350°C for 5 minutes is already sufficient to considerably improve the MOSFET performance.

4.5. Conclusion

In this chapter the DC operation characteristics of the NMOS and PMOS transistors that were fabricated have been discussed. The differences of the fabrication processes regarding device performance was analyzed. It was discovered that using a scattering layer yields considerable additional device performance. This is presumably due to a reduction in ion channeling and therefore implantation profile depth. Of the three experimented dirt barrier thicknesses it was found that a 20nm barrier had the highest drain current and lowest channel resistance. Furthermore, the effects of different implantation energies was also analyzed. Here it was discovered that using lower energy actually improved the I_D vs V_{DS} performance of the device. This can again likely be attributed to a lower implantation dept and tail. Unfortunately no research was done on the effect of implantation energy of phosphorus implantation, but it can be concluded that using a lower implantation energy of 5keV improves device performance compared to 15keV for Boron implantation of the PMOS devices.

In addition to process differences, physical characteristics of the devices, such as gate length and width and metal width were also compared in regards to threshold voltages and I_D vs V_{DS}. In regards to the threshold voltage, it could be seen that there were some inconsistencies, likely due to the non uniform doping of the substrate. Overall however a trend could be observed where increasing the gate width shifts the threshold voltage positive while increasing the gate length shifts the threshold voltage negative. Overall the variance of the threshold voltage over the entire wafer was approximately 150mV.

The effects of gate width and length were also compared to the I_D vs V_{DS} performance of the MOSFETS. It was shown that increasing the gate width above a certain limit breaks the linear relationship between drain current and gate width, and losses start to accumulate from the lateral voltage drop in the metal and source contacts. A similar trend can be seen in the current density of the various devices. Smaller width devices have larger linear current density compared to wider devices. On the other hand however The channel resistance shows an inverse relationship with the gate width. For the sake of optimizing for channel resistance it would be better to use devices larger than 2500 μm. The last dimensional difference analyzed was the effect of the metal width. It was shown that devices with wider metal contacts have both lower channel resistance as well as a larger drain current. It is therefore best to use a metal width of 60μm to allow for better performance.

Additionally the breakdown voltage of the devices was analyzed and it was found that the avalanche breakdown for NMOS is at $V_{DS} = 11V$ while for PMOS it is around $V_{DS} = -23V$. This difference between NMOS and PMOS is likely due to the higher mobility of electron in NMOS transistor, gain the

needed acceleration much earlier than the holes in the PMOS.

Lastly, the post annealing conditions of the devices were experimented on. It was found that 350°C for 5 minutes considerably improves device performance for both NMOS and PMOS. PMOS device improve more however, this is likely due to the forming of aluminium silicide, which is a p-doped material, effectively enhancing the PMOS performance.

5

Effect of Illumination on Device Performance

Similar to how the absorption of incident illumination can generate additional charge carriers in the pn junctions of solar cells, absorbed photons can also have the same effect on the pn junctions of MOSFETs and other semiconductor devices, altering their performance and behaviour.This is one of the reasons why semiconductor devices are generally encased to prevent such effects from occurring. However since the devices discussed in this thesis will be directly integrated on the back side of a solar cell, and thus will be exposed to photons and photo generated charge carriers. It is therefore important to study the opto-electrical effects in illuminated conditions on the performance of the devices. In this chapter the effects of illumination on gate to source voltage and drain to source voltage will be analyzed.

5.1. Measurement Setup

To measure these opto electrical effects of the photo generated charge carriers LEDs with three different irradiance spectra are mounted on top of the Cascade with a distance of 7cm from the devices. In real world applications illumination of the devices would be from the back through the substrate of the solar cell. With the Cascade this is not possible however as the LED can not be mounted below the wafer, and the wafer cannot be flipped with the backside up. Thus illumination is done from the front of the MOSFETs and effectively from the back of the solar cell.

Three separate illumination conditions were tested, a blue light (462nm), a red light(641nm) and a full spectrum light, their spectra are shown in figure 5.1. Reason for studying different wavelengths is the difference between the measurement setup and real world application. Since the device would normally be illuminated through the substrate of the solar cell, higher wave length photons would be more likely to reach the device compared to lower wavelengths. Thus a comparison between the effects of high wavelength (red) and low wavelength(blue) illumination could help to determine if the energy of the photon affects the opto electric effects.
It has to be noted however that only a single NMOS and PMOS device was measured and that their opto electrical effects are only representable for devices with similar behavioural characteristics

5.2. Drain current versus gate to source voltage under illumination

Figure 5.2 shows the effect of different sources of illumination on the I_D vs V_{GS} curves of a NMOS transistor. Across all three figures it can be seen that incident light significantly increases the drain current for a given gate voltage compared to the I_D vs V_{GS} curve without illumination. The reason for the low drain current for increasing gate voltage for the case without illumination is due to surface scattering. The electric field between the gate and the substrate produces a force on the electrons travelling through the channel. While moving from source to drain through the channeling this force attracts the electrons to the surface only to be repelled by the localized coulombic forces, reducing its mobility by 'zigzagging' instead of moving straight trough the channel[52] [32]. This effect increases

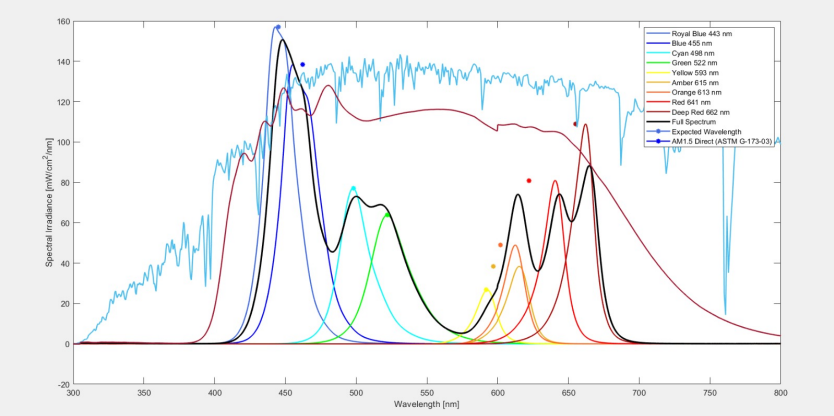
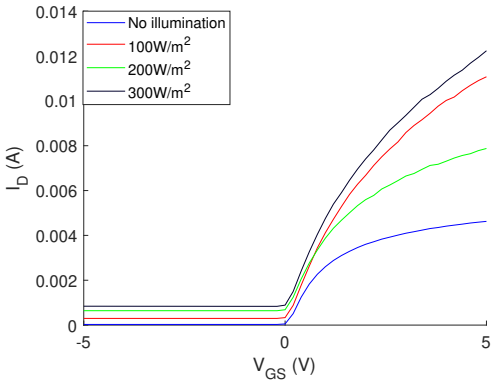
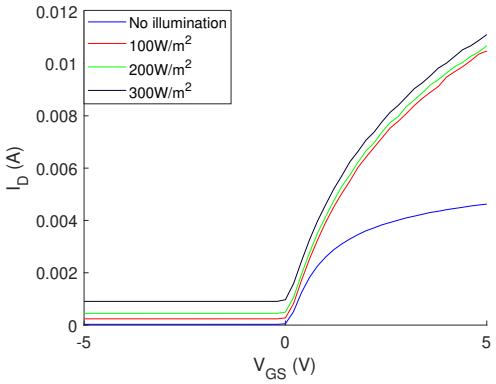


Figure 5.1: Spectral irradiance of the used LEDs

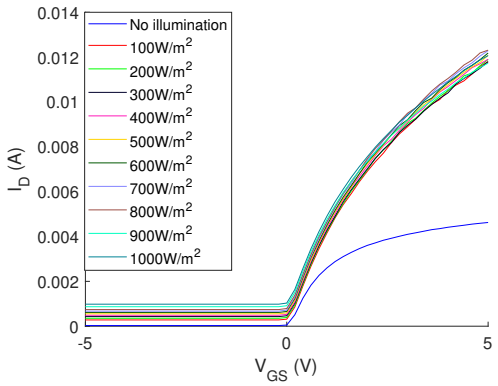
with increasing gate to source voltage and thus reduces the drain current, which is linearly dependent on the mobility. Under illumination however, the free carrier density increases, which enhances the electron mobility[53].



(a) Effect of red (620-625nm) light with varying intensity on I_D vs V_{GS} curves



(b) Effect of blue (460-465nm) light with varying intensity on I_D vs V_{GS} curves



(c) Effect of full spectrum (380-840nm) light with varying intensity on I_D vs V_{GS} curves

Figure 5.2: Relationship between I_D vs V_{GS} and varying sources of illumination for NMOS transistor. V_{DS} = 100mV, W = 2500μm, L = 4μm

Furthermore a shift in threshold voltage which is related to irradiance can also be observed. It can be seen in table 5.2 that the threshold voltage shifts in the negative direction for all light sources that were used, and the threshold voltage shift increases with irradiance. This shift is due to the photovoltaic effect

Table 5.1: Leakage current in off state of PMOS device

Irradiance (W/m^2)	I_D at V_{GS} = -5V
0	29 μA
100	280 μA
200	353 μA
300	428 μA
400	488 μA
500	554 μA
600	615 μA
700	672 μA
800	742 μA
900	869 μA
1000	982 μA

in which the holes generated in the channel due to incident photons move to the source of the device and accumulate at the space charge region between the source and channel, lowering the potential barrier for electrons and thus decreases the threshold voltage[54][55]. This effect is disadvantageous for the devices as now the NMOS devices can only be turned off by applying negative gate voltages, which will cause a gate leakage current, losing unnecessary power. The threshold voltages shown in chapter 4 already have a low threshold voltage, which already meant that a voltage had to be applied to ensure off state, but now an even higher potential difference is needed. However, unlike proper depletion mode devices which have much more negative threshold voltages in the case of NMOS transistor and can conduct properly without a driving gate voltage, these devices will also need a driving gate voltage for conduction. This will increase the total losses of the system due to leakage current losses from the gate.

It is also worth noting that the figures show that there will a higher leakage current even if the transistor is turned completely off. The leakage current increase from approximately 29μA under no illumination to almost 1mA under full spectrum illumination at 1000 W/m^2, shown in table 5.1. This is a serious disadvantage as it means the blocking capabilities of the MOSFET are reduced and more current will leak through the device, reducing system efficiency. This increased leakage current could possibly be caused by the increased amount of charge carriers due to photo generation diffusing through the device.

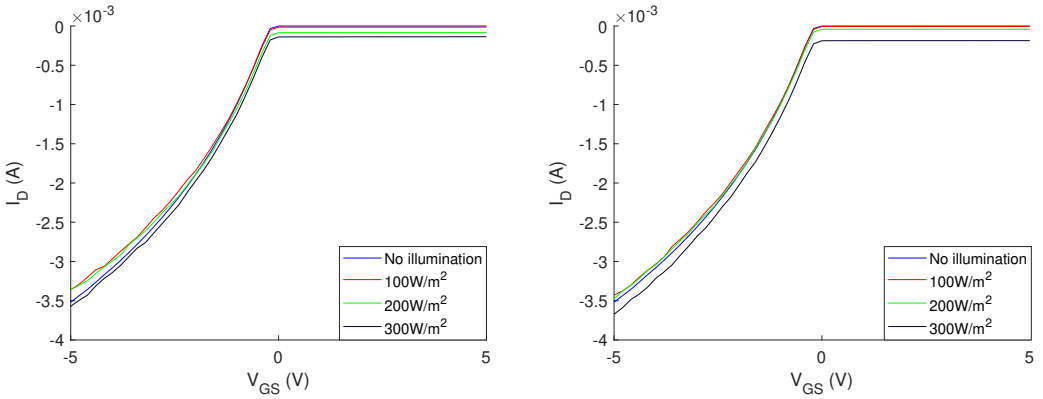
Table 5.2: Threshold voltage for NMOS transistor for various light sources and intensities.

	Threshold voltage (V)		
irradiance	Red light illumination	Blue light illumination	Full spectrum illumination
0 W/m^2	0.0616	0.0616	0.0616
100W/m^2	0.0055	0.0184	0.0168
200W/m^2	-0.103	-0.038	-0.0027
300W/m^2	-0.125	-0.162	-0.022
400W/m^2	-	-	-0.038
500W/m^2	-	-	-0.050
600W/m^2	-	-	-0.065
700W/m^2	-	-	-0.076
800W/m^2	-	-	-0.098
900W/m^2	-	-	-0.125
1000W/m^2	-	-	-0.150

Figure 5.3 also indicates that the maximum transconductance changes due to incident light. For both full spectrum illumination and blue light illumination the maximum transconductance changes immediately from 0.0037S (no illumination) to 0.0047S. The increased transconductance could be either due the a decrease in channel resistance caused by the extra photo generated electrons [55], or by a decrease of effective channel thickness due to an increase of the electric field caused by the photo

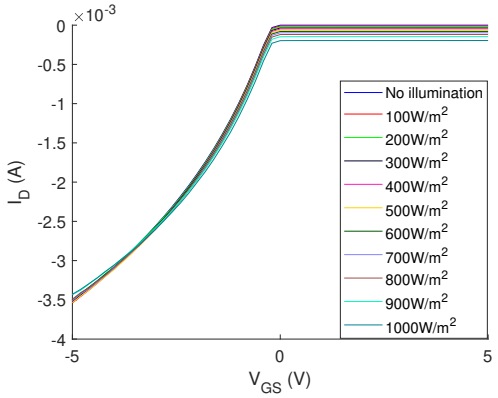
generated holes [56]. Seeing as how the increased electric field mentioned in Drummond et al [56] does not influence the scattering effect previously mentioned, it seems like the the increased transconductance is due to a decreased channel resistance.

Unlike the NMOS transistor, illumination does not improve the scattering effect for the PMOS transistor, as can be seen in figure 5.3. It can be seen that for every method of illumination tested the curve remains similar. This could mean that either the PMOS transistors did not suffer from the scattering effect the same way NMOS transistor did, or that that the extra photo generated holes do not improve hole mobility sufficiently for it to affect the I_D vs V_{GS} relationship for the PMOS transistor. The off state leakage current of the for PMOS devices however show a more significant increase. The leakage current in the off state shown in table 5.3 is in the order of 40 pico amperes, while under illumination the leakage current increases to the order of 40-200 μA. This is a factor 10^6 increase



(a) Effect of red (620-625nm) light with varying intensity on I_D vs V_{GS} curves

(b) Effect of blue (460-465nm) light with varying intensity on I_D vs V_{GS} curves



(c) Effect of full spectrum (380-840nm) light with varying intensity on I_D vs V_{GS} curves

Figure 5.3: Relationship between I_D vs V_{GS} and varying sources of illumination for PMOS transistor. V_{DS} = -100mV, W = 2500μm, L = 4μm

Furthermore in can also be noted that the threshold voltage of the PMOS device, shown in table 5.4, shifts opposite to that of the NMOS device shown in table 5.2. This can be explained due to the same process earlier, where photo generated electrons in the channel move from the channel to the depletion region between the channel and source, lowering the barrier for the holes to pass through and thus shifting the threshold voltage towards the positive side. The threshold voltage shift for the PMOS is about 150mV in this case, while the shift for the measured NMOS transistor is approximately 210mV. While the threshold voltage does not increase enough to become positive, a positive gate voltage will still have to be applied to keep the channel properly closed. Otherwise current leaking from source to drain while in sub-threshold conditions could significant losses due to to improper blocking. The transconductance in the case of the PMOS is 0.0013S with and without illumination and thus remains unaffected by it.

Table 5.3: Leakage current in off state of PMOS device

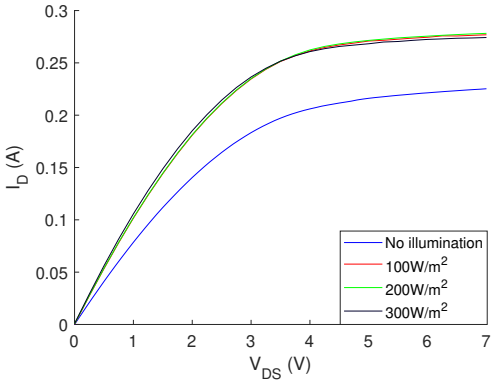
Irradiance (W/m^2)	I_D at V_{GS} = 5V
0	-45 pA
100	-22 μA
200	-36 μA
300	-48 μA
400	-64 μA
500	-80 μA
600	-97 μA
700	-118 μA
800	-146 μA
900	-196 μA
1000	-196 μA

Table 5.4: Threshold voltage for PMOS transistor for various light sources and intensities.

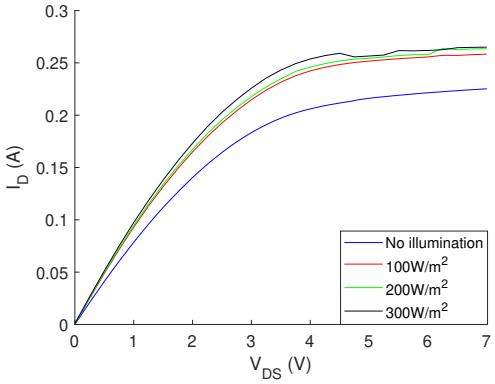
	Threshold voltage (V)		
irradiance	Red light illumination	Blue light illumination	Full spectrum illumination
0 W/m^2	-0.211	-0.211	-0.211
100W/m^2	-0.190	-0.196	-0.204
200W/m^2	-0.132	-0.169	-0.195
300W/m^2	-0.087	-0.054	-0.183
400W/m^2	-	-	-0.173
500W/m^2	-	-	-0.160
600W/m^2	-	-	-0.148
700W/m^2	-	-	-0.135
800W/m^2	-	-	-0.118
900W/m^2	-	-	-0.094
1000W/m^2	-	-	-0.056

5.3. Drain current versus drain to source voltage under illumination

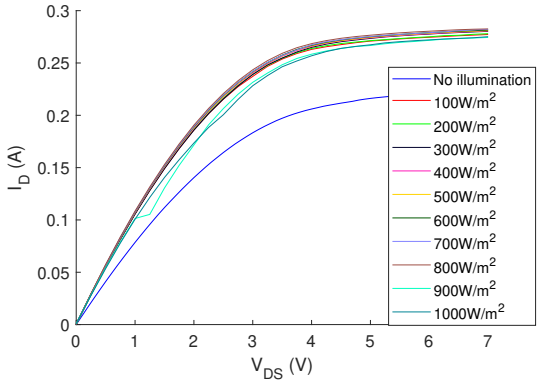
In this section the I_D vs V_{DS} performance for both NMOS and PMOS under illumination will be analyzed at $|V_{GS}|$ = 5V. Figure 5.4 show the effects of red, blue and full spectrum illumination on the I_D vs V_{DS} curve of the NMOS transistor. It can be seen that under illumination both the maximum drain current in saturation as well as the slope in the triode region have improved. This could be due to the increased mobility caused incident light however in that case, there should be a more visible differentiation between the different irradiances for the red illumination like in figure 5.2a. Alternatively it could be that the photo generated electron decreases the threshold voltage, which increases the overdrive voltage and in turn increases the drain current. In that case however, one would also expect increased performance from PMOS transistors, which is not the case as can be seen in figure 5.5. Similar to figure 5.3, the I_D vs V_{DS} performance of the PMOS is largely unaffected by the light with only a slightly lowered current interestingly. If it would be the case that the extra photo generated charge carriers decreased the potential barrier in the pn junction, and thus increased the current flow, then the PMOS transistor would also perform better under illumination.



(a) Effect of red (620-625nm) light with varying intensity on I_D vs V_{DS} curves

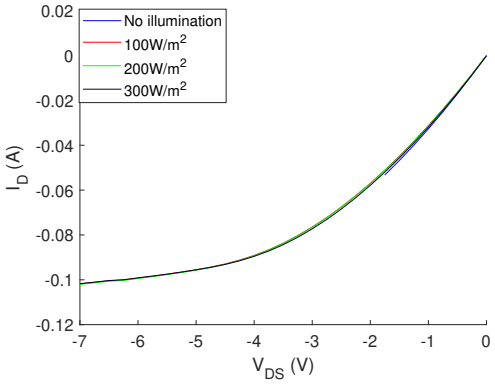


(b) Effect of blue (460-465nm) light with varying intensity on I_D vs V_{DS} curves

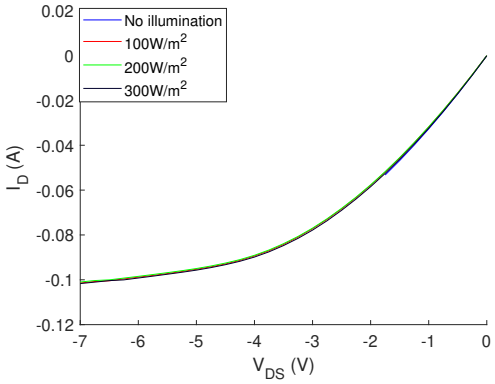


(c) Effect of full spectrum (380-840nm) light with varying intensity on I_D vs V_{DS} curves

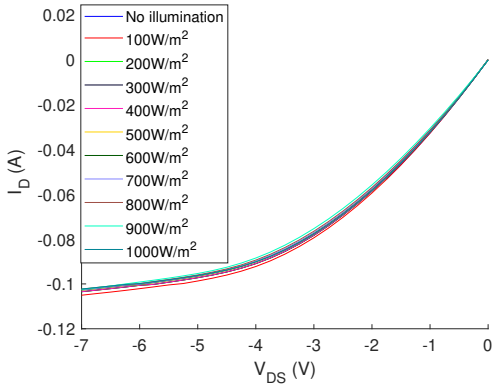
Figure 5.4: Relationship between I_D vs V_{DS} and varying sources of illumination for NMOS transistor. V_{GS} = 5 100mV, W = 2500μm, L = 4μm



(a) Effect of red (620-625nm) light with varying intensity on I_D vs V_{DS} curves



(b) Effect of blue (460-465nm) light with varying intensity on I_D vs V_{DS} curves



(c) Effect of full spectrum (380-840nm) light with varying intensity on I_D vs V_{DS} curves

Figure 5.5: Relationship between I_D vs V_{DS} and varying sources of illumination for PMOS transistor. V_{GS} = -5V, W = 2500μm, L = 4μm

In addition to a higher saturation current, the channel resistance of the NMOS transistor is decreased by the influence of light as is shown in table 5.5. The channel resistance for the NMOS transistor decreases with approximately 10%. Interestingly, the inverse happens with the PMOS transistor under illumination, where the resistance seems to slightly increase.

Table 5.5: Channel resistance for differing irradiance with full spectrum illumination for NMOS and PMOS

irradiance (W/m^2)	$R_{on}(\Omega)$ NMOS	$R_{on}(\Omega)$ PMOS
0	13.73	37.55
100	11.89	37.46
200	11.82	37.97
300	11.89	38.00
400	11.77	38.03
500	11.72	38.40
600	11.68	38.58
700	11.66	38.72
800	11.58	39.11
900	13.13	39.93
1000	12.69	38.18

5.4. Conclusion

In this chapter, the effects of incident light was analyzed. It is shown that for NMOS devices the I_D vs V_{GS} curve will remain linear for higher gate voltages, presumably due to an increase in mobility. The transconductance will be higher under illumination due to a lowered channel resistance, and the threshold voltage will shift in the negative direction with increasing irradiance. This means that the driving circuit has to apply a voltage to the gate to ensure that it is off, costing additional power.

Furthermore, it is shown that NMOS devices will drive slightly larger current at the same drain to source voltage under illumination compared to in the dark. This could have multiple explanations, one is the shift in threshold voltage increases the overdrive voltage and therefore the drain current. Another explanation is that the increased electron mobility also affected the I_D vs V_{DS} relationship. Additionally increasing the intensity of illumination also decreases the channel resistance in triode region of NMOS transistors.

The PMOS transistor seems to be less affected by illumination in the on state. It does have an increased leakage current under subthreshold conditions similar to the NMOS as well as a shift in the positive direction of the threshold voltage. Similarly this likely means that a voltage has to be applied to turn off conduction, decreasing efficiency.

Lastly it was seen that the subthreshold leakage current increases significantly with increasing irradience. This will pose a problem for the MOSFET integration as this leakage current could affect the losses in the system. Further research has to be done to the exact effects but it is possible to a shielding device has to be integrated between the MOSFET and solar cell to prevent illumination from affecting the device.

6

AC Characterization

In addition to be able perform well in DC operation, such as high drain current and low on resistance, another important aspect is the AC capabilities of the device, such as switching speed and capacitances. The switching performance of a device is determined by the time required to establish voltage changes across capacitances. This is due to the necessity of releasing/collecting the charge held by the capacitances before the MOSFET switches from state. It is therefore important that the capacitance is as small as possible to prevent charge build up in them. This chapter will the capacitive measurements of the MOSFETs will be analyzed.

6.1. Capacitance measurements

Figure 6.1 show the capacitances between the gate and drain(c_{gd}), source(C_{gs}), and substrate(C_{gsub}). Another name for C_{gsub} is the MOS capacitor, which is parallel plate capacitor which the MOSFET gate as one plate and the Si substrate as the other. The gate oxide is used dielectric material in which the electric filed is formed.The capacitance scales linearly with surface area of the gate and will be in series with the output capacitance of the solar cell. For the MOS capacitor there are three important regions of operation: accumulation, depletion and inversion. Like the name suggest, accumulation happens in a p-type substrate when a negative voltage is applied, inducing the accumulation of holes at the semiconductor oxide interface. in accumulation the capacitance is equal to the oxide capacitance times the surface area of the gate. When the voltage increases, C_{gsub} enters depletion mode. The positive voltage at the gate creates a space charge region in the c-Si substrate, which is in series with the oxide capacitance[32].

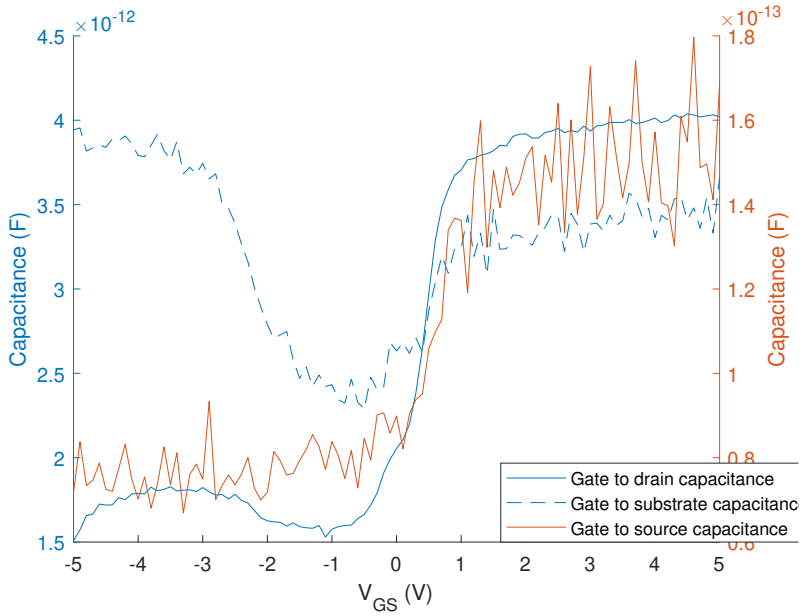


Figure 6.1: Capacitance measurement of NMOS transistor. L = 3300 μm, W = 500μm

As this space charge region widens, the total capacitance in depletion decreases. A minimum will be reached when there is essentially zero inversion charge density, after which it will enter inversion. The inversion charge density will increase and ideally will reach the oxide capacitance. However, it can already be seen that C_{gsub} does not reach the same capacitance in inversion as it does in accumulation. This has to do with the source of electrons that can change the charge density of the inversion layer[32].

The first source of electrons is by diffusion of minority carrier electrons from the substrate across the depletion region, similar to reverse biased pn-junctions. The second source is from the thermal generation of electron hole pairs within the depletion region. They however have a separate electron generation rate. If high frequency AC voltage is used to switch the voltage rapidly, the electrons in the inversion layer will not be able to respond. The capacitance measurement will then become a function of the frequency of the ac signal used. This eventually lowers the measured capacitance in the inversion region, as is the case in figure 6.1.

Both c_{gd} and c_{gs} are both parasitic capacitances inherent to the device structure. it can be seen that that c_{gd} is approximately twenty times larger then c_{gs}. This could have multiple reasons. One of which is that there is a higher overlap between the gate and the drain compared to the source due this misalignment during fabrication. This would increase the drain capacitance equally to the overlapping area.

The output capacitance C_{oss} of this device would then be the sum of these capacitances at V_{GS} = 5V, meaning that $C_{oss} \approx 8pF$. With this a rough estimate could be made of the potential rise and fall time of the device using The RC time constant τ. The RC time constant indicated how low it takes for a capacitor to charge to approximately 63.2% or discharge to 36.8% of the total charge. Then the (dis)charge time of a capacitor can be calculated using formulas 6.1 and 6.2[57].

$$V(t) = V_0(1 - e^{-t/\tau}) \tag{6.1}$$

$$V(t) = V_0(e^{-t/\tau}) \tag{6.2}$$

Where V_0 is the initial gate voltage. Thus if an external gate resistance of 50Ω is assumed, the RC constant would then be $50\Omega * 8pF = 400pS$. If the initial gate voltage is assumed to be 5V and the threshold voltage is 0.1V. then the total discharge time can be calculated to be equal to $1.56ns$. However as the external gate resistance is dependant on the external driving circuit it can not be said for certain that these times are feasible in practice.

Additionally, this is for a single device, which has a drain current of approximately 2.5mA at V_{DS} = 100mV. If a cell has a short circuit current of 5A a total of 2000 of these devices would have to be placed in parallel to accommodate for this current. This would increase the capacitance by the same amount as the gate surface area increases linearly. Increasing the capacitance by that amount would increase the rise and fall time equally, increasing the switching losses.

7

Updated Flowchart Proposal

This chapter will discuss the integration of the MOSFET production with the production of the IBC solar cell. First the drawbacks of the original combined fabrication process of the IBC and MOSFET. Afterwards an updated flowchart which used a different IBC fabrication technique will be discussed together with the fabrication process of the IBC solar cell with integrated MOSFET.

7.1. Original Process Drawbacks

The original MOSFET fabrication process is based on an IBC cell design from [31] shown in figure 7.1. In this process however, two different poly silicon deposition steps are used to fabricate the carrier selective passivating contacts. In the process, after deposition of poly silicon on the n-type substrate, it is first implanted with n-type dopants creating an n^+ poly silicon layer. This polysilicon layer is then locally etched and covered with SiN_x and another polysilicon layer is deposited on top, this time implanted with positive p-type dopants.

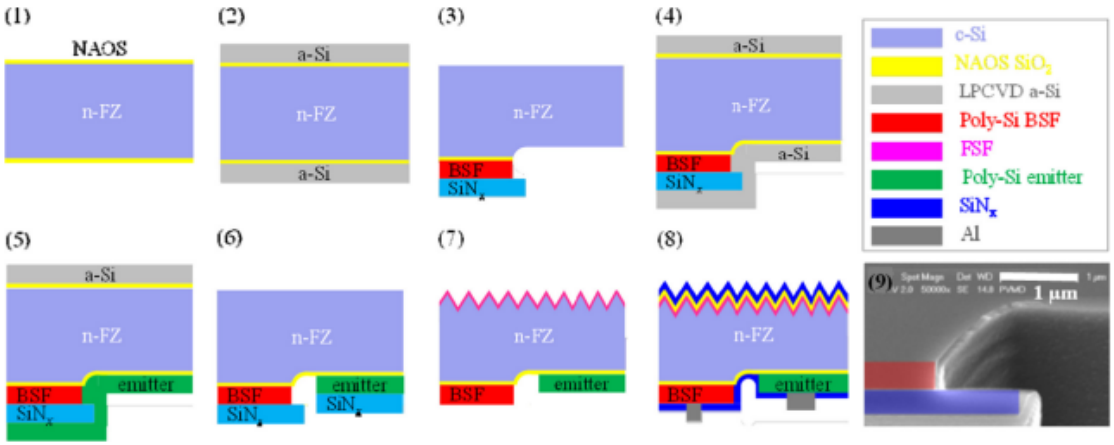


Figure 7.1: (1–8) Schematic representation of the self-aligned process for IBC solar cells; (9) cross-sectional scanning electron microscope picture of the trench formed in step (3) [31]

This double deposition of a poly silicon layer increases complexity, due to the fact that, before both n- and p-type ion implantation steps, multiple similar etching and lithography steps have to be performed to remove the SiN_x, poly silicon and SiO_2 in order to also implant substrate for the source, drain and grounding contact. This could significantly increase production cost, time and complexity and therefore, the double deposition of poly silicon is undesired. Additionally this double deposition also causes the need to etch the c-Si substrate surface which causes nano-scale roughness. This surface roughness influences the passivation properties of the emitter deposited on top of it, decreasing the solar cell performance.

Therefore, a new IBC fabrication technique designed by the same group called 'etch-back' [58] that uses only one poly silicon deposition. This is achieved by patterning the BSF and the emitter in a different way which allows both the BSF and emitter to be deposited on the polished c-Si surface and hence will enable optimal passivation for both BSF and emitter. A schematic representation of the patterning process of the backside is shown in figure 7.2

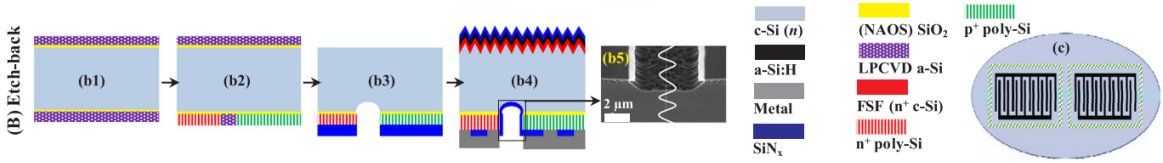


Figure 7.2: (b1 b4)schematic representation of the etch back process for IBC solar cells; (b5) cross-sectional SEM picture of the trench between the poly-Si BSF and emitter fingers. (c) Schematic representation of the back side of the wafer, containing two solar cells. For sake of simplicity, the back side SiNx layer was not drawn. [58]

This can significantly simplify the fabrication process as now the etching steps for the source/drain and grounding contact, which were separate at first, can be done simultaneously. This has the potential to streamline the fabrication process and reduces cost and time.

7.2. Integrated MOSFET Process

This section will discuss the combined fabricated method of the IBC solar cell and MOSFET. The specifications of the wafer used for this process can be found in table 7.1. Since the IBC cell fabricated in [58] uses an n-type substrate, the combined process will also use n-type wafers. This means that the integrated MOSFET discussed in this section will be a PMOS. The process listed below can also be used for the fabrication of p-type IBC cells with an integrated NMOS transistor by simply replacing the dopant types during ion implantation.

Table 7.1: c-Si Wafer specifications

Parameter	Value
Method/Dopant/Type	PFZ/Phosphorous/P
Orientation	<100>
Finish	Double sided polished
Resistivity	1-5 Ωcm
Thickness	255 - 305 μm
Diameter	99.7-100.3 mm

7.2.1. Zero Layer

Similar to the explanation given in chapter 3.2.1, this process requires multiple lithography steps and thus need accurate alignment between layers on the wafer. For this reason the first step is again etching alignment markers in the sides of the wafers to properly align the mask. This is again done by coating the wafer with PR, exposing the wafer using the ASML PAS5500/80 using mask COMURK and subsequently developing the PR. The etching is done using the Trikon OMEGA using program $urk - npd$. Lastly the PR is removed and the wafer is cleaned.

7.2.2. MOSFET openings

The first steps in the combined process will be the MOSFET gate deposition, NAOS deposition and subsequent opening of the source, drain and grounding contact surfaces. All of this will be done on the backside of the wafer. A visual representation of this is given in figure 7.3

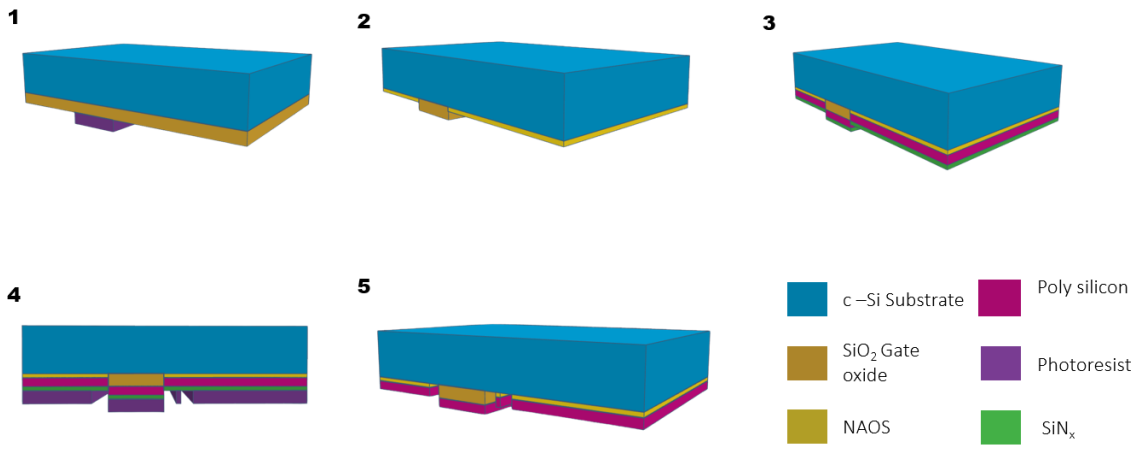


Figure 7.3: Schematic representation of process of creating the MOSFET openings in the solar cell

1. Firstly, similar to what was explained in chapter 3.2, a SiO_2 layer of 30nm thick will be formed using dry oxidation in a high temperature furnace. This SiO_2 layer will function as the gate oxide of the MOSFET. The gate oxide is too thick to function as tunneling oxide however and thus a layer of PR will be deposited and exposed on top to define the gate area using lithography.

2. The SiO_2 gate oxide will be chemically etched using BHF and removed from the c-Si substrate to define the gate area. Subsequently,NAOS will be performed by placing the wafer in a HNO_3 69.5 % bath at 110 °C for 10 minutes forming the thin 1-2nm tunneling oxide layer.

3. Afterwards, a 250nm thick poly silicon layer that will function as the gate, emitter and BSF can be deposited on top of the oxide layers using LPCVD deposition. To create the openings for the source, drain and gate, an additional thin layer of PECVD SiN_x will also be deposited on top

4. Then using lithography the areas of of the source, drain and gate will be defined.

5. First the exposed SiN_x will be etched in a BHF bath, leaving the poly silicon layer above the source, drain and gate exposed. This will be etched using a poly silicon dip etch. Subsequently the PR will be stripped and the wafer is cleaned. Lastly, the wafer will again be etched in BHF to remove the tunneling oxide on top of the source, drain and gate. At same time, the BHF will also etch away the newly exposed SiN_x to remove it from the surface

7.2.3. Implantation

This section will describe the implantation of the various regions of the cell, which are solar cell emitter, back and front surface fields, and the MOSFET source, drain, grounding contact and gate. The back and front surface fields of the cell are highly doped regions at the surface of the substrate. Having highly doped layers at the substrate prevents surface recombination by creating a pn junction which prevents minority carrier flow. Additionally the solar cells are also textured during these steps. Silicon has a high surface reflection [59]. One method to reduce the reflection of silicon is by texturing the wafers. This roughening of the surface increases absorption by increases the chance of light to reflect back onto the surface, instead of the surrounding area[17]. A visual representation is show in figure 7.4.

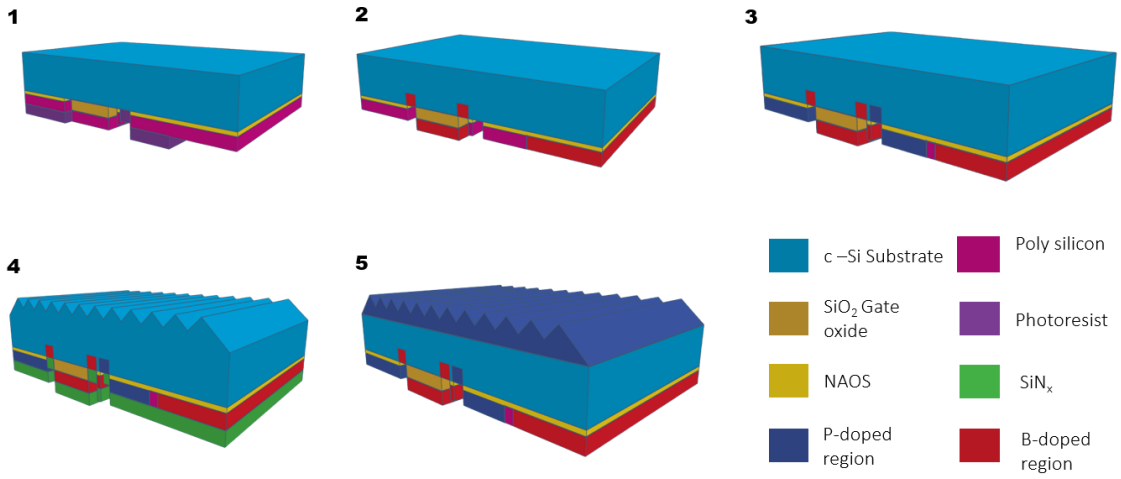


Figure 7.4: Schematic representation of the implantation process of both the MOSFET and solar cell.

1. First boron implantation of the p+ type emitter, source, drain and gate will be performed, which means that the areas than will not be implanted, such BSF and grounding contact will have to covered. This is done using PR by coating the whole wafer and exposing the areas that have to be coated using a mask.

2. After that Boron implantation will be done. The PR will be removed and the wafer will be cleaned.

3. After boron implantation, phosphorous implantation will be done to create the n+ back surface field and to dope the grounding contact of MOSFET. This will be done similarly to B-implantation, by coating the wafer with PR and exposing the areas that have to be doped. The wafer is then subsequently stripped of the remaining PR and again cleaned.

4. Next the front side of the wafer will be textured. This will be done by placing the wafer in a mixture of H_2O, TMAH (Tetramethylammonium hydroxide) and IPA at a temperature of approximately 80 °C. To prevent the backside from also getting textured a layer of PECVD SiN_x, which does not react to the mixture, will be deposited on the back side.

5. Lastly, the FSF is created by implanting the front surface with phosphorous ions. Then the silicon nitride can be etched away in BHF and the wafer is annealed in a high temperature furnace to activate the implanted dopants.

7.2.4. BSF definition and ARC deposition

This section will discuss the definition of the back surface field and the front anti-reflective coating(ARC) of the solar cell. The BSF definition is used to prevent the forming of a pn junction between the p-doped emitter and n-doped BSF. Furthermore, this definition allows for the bifaciality of the solar cells as this allows light to also hit the substrate from the back side. The ARC is similar to wafer texturing used to reduce reflection. By depositing a thin layer of a dielectric material with a specific chosen thickness waves reflected from the surface of the substrate can be destructively interfered with waver reflected from the ARC, resulting in no reflected light [17]. A schematic representation is shown in figure 7.5

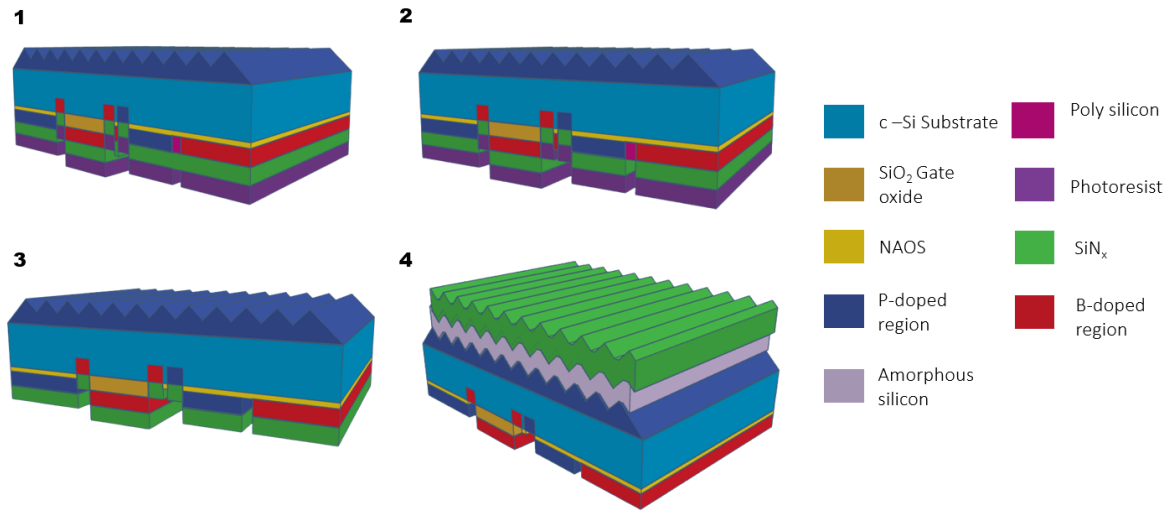


Figure 7.5: Schematic representation of the BSF definition and front surface ARC deposition.

1. For the BSF definition, first a new PECVD SiN_x layer is deposited on the backside of the wafer. This is then coated with a layer of PR and is exposed.

2. The silicon nitride in the openings is subsequently etched using BHF to expose the undoped poly silicon area between the emitter and BSF and the between the MOSFET grounding contact and drain/source.

3. Then, after stripping the PR and cleaning the wafer, the poly silicon between the emitter and BSF, and the ground and source/drain is etched using a poly silicon dip etch to create the BSF definition.

4. The next step is to etch the SiN_x on the backside away using BHF and to deposit an amorphous silicon using an LPCVD deposition and PECVD SiN_x layer stack on the front side of the wafer to act as ARC.

7.2.5. Metallization

The final step, similar to chapter3.2, is the metallization of the contacts. Again a SiN_x layer has to be coated to prevent surface passivation in the opening between the emitter and BSF and to also act as a backside mirror to reflect light passing the cell back through the substrate. A schematic representation is shown in figure 7.6.

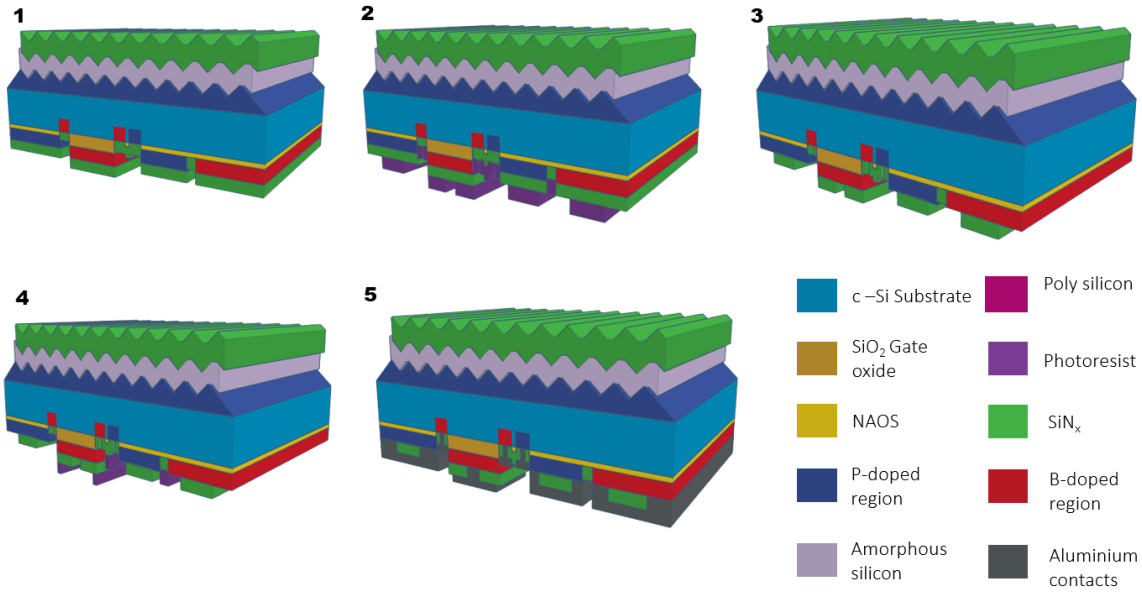


Figure 7.6: Schematic representation of the fabrication of the MOSFET and solar cell metallization.

1. First, another layer of PECVD SiN_x is deposited on the backside of the wafer. This layer will function as passivation layer and as backside mirror to increase the absorption of incident light.
2. The wafer is subsequently coated with PR and openings are made through exposure to etch the silicon nitride away for the contacts.
3. The SiN_x is wet etched in BHF to create the contact openings. Subsequently the remaining PR is stripped from the wafer.
4. A new negative PR is coated on the wafer. The mask used in this step has slightly wider openings at the contacts than the previous one to improve conductance.
5. Then 1.5 μm layer of aluminium is evaporated on top of the negative PR. Lastly, the PR and excess aluminium is removed using a process called lift off where the wafer is subdued in a chemical called N-Methyl-2-pyrrolidone (NMP) which reacts with the negative PR and thus removes it, together with the aluminium from the wafer.
6. Finally, the wafer is annealed at 350°C for 5 minutes to improve the contact resistance for both the MOSFET and solar cell.

7.2.6. Conclusion

The proposed flowchart aims to combine as many steps between the MOSFET and solar cell fabrication as possible. No additional implantation steps are necessary this way. Some additional lithography steps are necessary however, such as for the creation of the source, drain and ground openings. These however have been combined as much as possible with other lithography steps necessary for the solar cell fabrication and have been decreased compared to the original flowchart with the double poly silicon deposition.

8

Conclusion & Discussion

In this thesis, multiple variations in MOSFET fabrication methods and device characteristics have been analyzed. This chapter will summarize the main findings of this thesis project in according with the research questions defined in chapter 1.4. First, the main conclusions will be presented. Afterward a future outlook will be given regarding further research in the integration of a MOSFET on the back of IBC cells.

8.1. Conclusion

The first research question was to find a method to fabricate the MOSFET using solar cell design techniques in order to ensure ease of integration, low cost, and simplicity. The initial fabrication method used in this thesis in shown in chapter 3.2. One such compromise is the use of chemical etching methods instead of plasma etching. The drawback of using plasma etching for solar cell fabrication is that it reduces surface passivation, increasing the surface recombination, and therefore decreases efficiency. Plasma etching is generally a more precise method of etching as it is an isotropic etching method, allowing for smaller and more precise features. Another is the direct implantation of the substrate of the device instead of using an epitaxially grown layer. Nonetheless is was shown that a working MOSFET can indeed be made using techniques used primarily in PV fabrication.

Additionally, a new flowchart was proposed in chapter 7 which integrates both MOSFET fabrication using the flowchart in chapter 3.2 with the fabrication of a newer IBC design with only 1 amorphous silicon layer [58]. It was shown that with this new IBC, multiple processing steps for both the MOSFET and IBC can be more easily integrated allowing cheaper and simpler fabrication.

The second research objective was to analyze the effects of illumination on the MOSFET behaviour. For this three different light sources were used to compare the effects of incident photons with different energies. The effects of a red, blue, and full spectrum light were tested. It was found that for the NMOS illumination increased both the drain current versus gate voltage, up to a factor 3 at V_G = 5V. Drain current versus drain to source voltage relationship has also seen and increase of up to $25\$$ in saturation. Channel resistance has decreased between 5-13$\%$ for the NMOS device. These effects are presumably due to either an improvement in electron mobility or a shift in threshold voltage, increasing the overdrive voltage of the device. The size of the threshold voltage shift is dependant on the intensity of the incident light. A negative threshold voltage shift of approximately 160mV can be observed for illumination with an irradiance of $1000 W/m^2$. For the PMOS device, a similar shift of threshold voltage occurs. With increasing irradiance the threshold voltage increases and shifts positive. This however did not yield a difference in performance for the PMOS device. Rather opposite to the NMOS, the drain current and channel resistance ($+2\%$) are only marginally worse under illumination. For both NMOS and PMOS devices, the drain current leakage in subthreshold conditions increases with significantly under illumination, with a factor of 33 for the NMOS under 1000 W/m^2 illumination compared to no illumination, and a factor of 10^7. This could increase the losses in the system as now a larger current will flow in the off state, increasing system power losses.

The last research objective was to optimize the device features of the MOSFET for optimal performance. For this, several factors were considered. One of these factors is the gate length of the device. Longer devices can handle more current and have lower channel resistance. Shorter devices however have a higher current density and are not as much impacted by the lateral voltage drop experienced by wider devices. Short devices however could experience punch-through effects, reducing the blocking capabilities of the device. However the shortest channel length on the tested wafers was 4μm, and no punch-through effects were observed. Devices with smaller feature sizes were not transferred with the contact photolithography that was used. Therefore a channel length of 4μm was chosen as the most optimal length within the tested MOSFETs. Furthermore the effects of the scattering layer and implantation energy were compared and it was found that using a thicker dirt barrier and lower implantation energy improves the drain current and channel resistance of the device. Furthermore the breakdown voltage for both NMOS (11V) and PMOS(-23V) was found. The reason for their difference can be attributed to their mobility. Lastly, the optimal condition for the post annealing process was determined to be 350° for 5 minutes to improve the aluminium semiconductor interface.

By using the results obtained during this research, the main research objective of the of this thesis could be fulfilled. Namely to analyze certain effects to play a role in a MOSFET designed for integration with an IBC solar cell. A single MOSFET discussed during this thesis is however not able to handle the current produced by a solar cell (V_{oc} = 700mV, I_{sc} = 5A). Further research has to be to analyze methods that could further improve this technology to a level that can handle this amount of current and voltage.

8.2. Future outlook

In this section recommendations for further research will be discussed. These recommendations discussed here could not be explored in this thesis due to the limited time available.

Firstly the purpose of this thesis was to give helpful insights on certain effects that occur, such as the effect of illumination and wider devices. More research has to be done to further optimize the MOSFET design to make it suitable for integration by, for example shortening the channel length. This would allow for higher current to flow through the device as well as decrease the channel resistance. Changing the position of the metal contacts could also be implemented, this way the parasitic resistive losses in the metal source and drain contact could be reduced. Alternatively, research can be done regarding the parallel implementation of multiple MOSFETs to reduce the parasitic on-state resistance and current handling capabilities that way. A method of dealing with the increased leakage current under illumination will also have to be devised. One way could be by shielding the MOSFET from illumination, thus preventing this effect from occurring.

Secondly, further research could be done on the AC capabilities of this device, as the research done for this thesis was mainly constricted due to time constraints. Further research could be done to properly analyze the switching capabilities of the MOSFETs with a specially designed gate driving circuit.

Thirdly, in chapter 7, a new flowchart in which a MOSFET is simultaneously fabricated on the backside of an IBC solar cell. It would be interesting to see how both the MOSFET as well as the IBC would perform using this (further optimized) flowchart.

Lastly, this thesis has only focused on the integration of MOSFETs on IBC. For the integration of complete power converters, other components also have to be developed and/or integrated, such as the inductor needed for power conversion, or a system that can reconfigure the modules quickly and efficiently.

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