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Development of a Ti/Au TES microcalorimater array as a backup sensor for the Athena/X-IFU instrument

K. Nagayoshi[1] • M.L. Ridder[1] • M.P. Bruijn[1] • L. Gottardi[1] • E. Taralli[1] • P. Khosropanah[1] • H. Akamatsu[1] • S. Visser[1] • J.-R. Gao[1,2]

[1]SRON Netherlands Institute for Space Research
[2]Kavli Institute of Nanoscience, Delft University of Technology

Abstract We are developing a transition edge sensor (TES) microcalorimeter array based on a Ti/Au superconducting bi-layer, as a backup option for the X-IFU instrument on the Athena X-ray observatory. The array is read out by a frequency-division multiplexing (FDM) readout system using a 1-5 MHz frequency band. Extensive research collaborations between NASA/Goddard and SRON have led to new design rules for microcalorimeters such as: low resistivity of the superconductor bi-layer, moderately high ohmic resistance of the TES by changing the aspect ratio and no extra metal strips. We have improved our detector fabrication process according to these design principles and produced TES arrays. Although single pixel characterizations of these arrays are ongoing, the best energy resolution of 2.0 eV for 5.9 keV X-ray has been observed with a 120×20 μm^2 TES with a normal resistance of 150 mΩ, biased at 2.2 MHz frequency. This shows that our Ti/Au TES array has a potential to fulfill the detector requirements of the X-IFU instrument.

Keywords transition edge sensor • X-ray • X-IFU • Athena

1 Introduction

Athena is an ESA-led X-ray space observatory to be launched in the early 2030s. The X-ray Integral Field Unit (X-IFU) instrument on board Athena will provide high resolution spectral data in the 0.3-12 keV band (ΔE = 2.5 eV for X-ray energy below 7 keV) on hot gases located in various astronomical objects and structures, which are crucial to study how the universe has grown as it is observed today [1]. The main sensor of the X-IFU instrument is an array of close-packed ~3200 TES microcalorimeters based on a Mo/Au bi-layer, which is under development by NASA/GSFC [2].

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SRON is developing a FDM readout system using the 1-5 MHz frequency band to readout the TES array efficiently [3].

It is known that when a TES is operated under AC bias, the energy resolution tends to be degraded compared to DC bias especially at the high frequency regime. In the past few years, an extensive research collaboration on this issue has been made between NASA/Goddard and SRON. As outcomes, two types of frequency-dependent physical effects, namely AC losses and the Josephson effect, have been identified and theoretical analyses have shown that both effects can be mitigated by increasing the total TES normal resistance [4, 5]. This is possible by decreasing the TES thickness however, it seems also important to have a thick TES film for a better thermal conductivity. Moreover, bare TESs (i.e. without normal metal stripes which were originally introduced to suppress the so-called excess-noise) have shown less weak-link effect and a smooth transition curve [6]. Taking these into account, new TES design rules have emerged as: low square resistance with a thick bi-layer, moderately high ohmic resistance enabled by changing the aspect ratio and no metal strips.

SRON is developing a TES array used as a European backup option for the X-IFU instrument. We have improved our detector fabrication process along the new design principles and produced TES arrays. In this paper, we present our successful fabrication results with the process details. For a spectral performance, we only show the best result observed so far, as validation of the fabrication process, more detailed discussions can be found elsewhere [7].

2 Detector Fabrication

We here describe our fabrication details for each step. We start the process with a 300 μm thick 4-inch Si wafer, which is thermally oxidized (250 nm) and coated with a 500 nm LPCVD low stress silicon nitride layer. On the backside of the wafer, a 3.5 μm thick PE-CVD SiOx is deposited as an etch mask for a deep reactive ion Si etching (deep-RIE) step performed at the nearly end of the process. We produced 5×5 and 32×32 arrays on each wafer, considering our test purposes and limitations on capabilities of our cryogenic experimental setups. However, we have confirmed that the process steps and techniques presented in the following subsections are scalable towards the large TES array required for the X-IFU instrument (e.g. film thickness uniformity and wiring density).

2.1 Ti/Au bi-layer TES

Deposition of the Ti/Au bi-layer is done in a dual electron-beam (EB) evaporation system. Au is deposited immediately after finishing Ti deposition with an interval of 2 seconds controlled by automatic shutters which ensures the reproducibility of the Ti-Au interface condition. Typical background pressure during the deposition is 2×10^{-8} mbar. The thickness of the Ti and Au layer is 35 nm and 200 nm, respectively, which are selected to show a sheet resistance of 25 mΩ/□ with superconducting transition temperature of ~90 mK. To study an optimal TES design for the FDM readout system, TES pixels with the normal resistance ranging from 25 to150 mΩ are available in 5×5 arrays by changing the width and aspect ratio. The Ti and Au layers are patterned with wet etching, using an iodine-iodide based solution and hydrofluoric acid of 1%, respectively.

2.2 Wiring process

Fig. 1 shows a microphotograph of a 100×30 μm^2 TES, connected to a microstrip line via interconnecting leads, and also a cross-section of the device schematically. We first deposit a 280 nm thick PE-CVD SiOx as a protection layer, which prevents roughening and thinning of the nitride membrane during subsequent etches. Secondly, we fabricate Nb-SiOx-Nb microstrip lines from bonding pads to connections following the procedure presented in [8]. The SiOx protection layer (about 80 nm is left after the microstrip line process) is then removed with buffered hydrofluoric acid. Thirdly, the Ti/Au bi-layer is deposited across the wafer and patterned with wet etching as described in the preceding subsection. Finally, the Nb interconnecting leads between the microstrip lines and Ti/Au bi-layer are fabricated with a lift-off process.

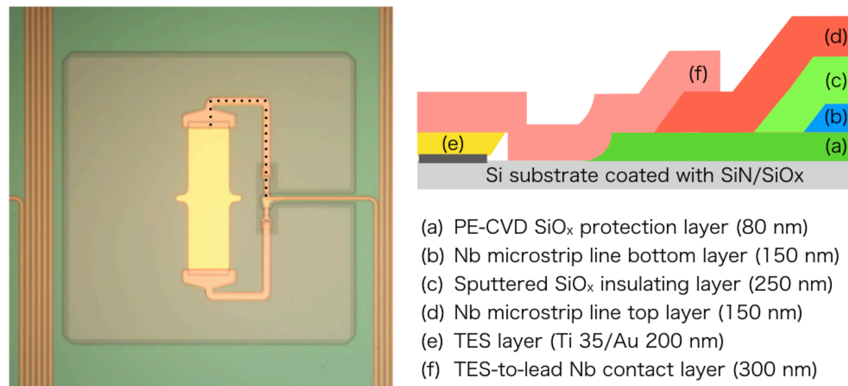

Fig. 1 *Left*: Microphotograph of a 100×30 μm^2 TES connected to a microstrip line via interconnecting leads. *Right*: The cutting view along with the dotted line indicated in the photo (Color figure online).

The bi-layer wet etch process creates undesired negative slope on the edge of the TES, probably due to Galvanic effects [9]. We might introduce an ion milling process to make the TES edge to a positive slope in the future. However, with this process we confirmed that the connection yield is already more than 99% across the wafer.

2.3 X-ray absorber and membrane

Subsequent to the wiring process, we fabricated a cantilevered Au X-ray absorber using electroplating in combination with a double photoresist layer process. Fig. 2 shows a microphotograph of a 32×32 TES array detector chip and an enlarged SEM micrograph of one of the pixels. The absorber is thermally coupled to the TES via the two stems, located near the center of the pixel. The other four stems stand on the silicon nitride membrane. We first define the structure of the absorber support stems using a 3.5 μm positive photoresist, which is thermally softened at 135 °C after developing the pattern. A 125 nm Au layer with a 3 nm Ti adhesion layer is then deposited as a seed layer. The grid that consists of 240×240 μm^2 absorber regions with a gap of 10 μm is defined on top of the seed layer by using a positive photoresist mold. We use "Techni gold 25E RTU" electrolyte for Au electroplating [10]. The temperature of the solution is kept at 56 °C using a hot plate and agitation of 300 rpm is applied with a magnetic stirrer. Electroplating is performed using a constant current with a platinized titanium mesh anode. The current is adjusted for a current density of 1.75 mA/cm^2 considering the total electroplating area on the wafer. The thickness of the absorber is 2.35 μm that corresponds to the heat capacity of 0.85 pJ/K at 90 mK. We typically observe a residual-resistance ratio of 30 from our Au absorber layer, which is limited by the process conditions for fabricating a flat and uniform absorber array with the photoresist grid.

After electroplating, the top photoresist is dissolved with acetone and the seed layer is etched away with a sputter etching in a RIE machine. The bottom photoresist remains for creating local SiN membranes with deep-RIE, and the wafer is bonded onto a carrier wafer upside-down by using Crystal Bond 509. The deep-RIE process is stopped at the thermal SiOx, which acts as an etch stopper. The thermal SiOx is then etched away with buffered hydrofluoric acid. Detector chips are also separated from each other with the same deep-RIE process and finally released from the carrier wafer after metallization (described in the next subsection) by using a photoresist remover, which dissolves the Crystal Bond and the bottom photoresist.

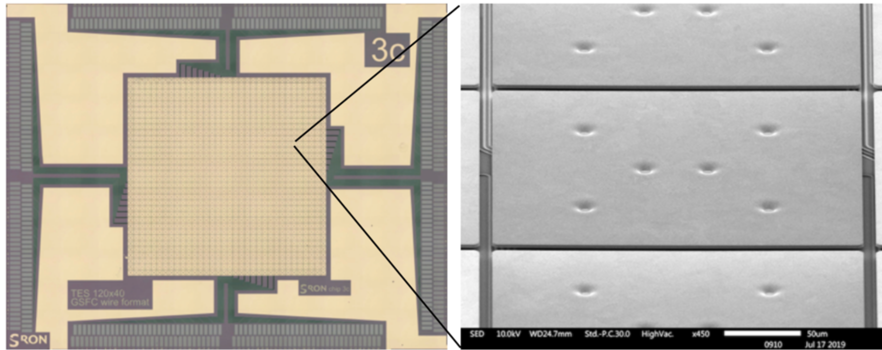

Fig. 2 *Left*: Microphotograph of a 32×32 array detector chip (15×19 mm^2). *Right*: SEM picture of the X-ray absorbers located in the 32×32 array. The absorber size is 240×240 μm^2 (Color figure online).

2.4 Metallization of a detector chip

A detector chip has heatsinking layers on both the front and back sides of the chip. On the front side, we deposit 0.5 μm thick Au with electroplating in combination with a lift-off photoresist mold just before absorber fabrication. On the backside, 1 μm thick EB-evaporated Cu coated with 20 nm Au is deposited subsequently to the deep-RIE process. The side walls inside the Si wells are also metallized, using a shadowing deposition technique [11].

3 Microcalorimeter performance and future works

We are characterizing 5×5 arrays to evaluate our fabrication procedure and to characterize TES designs optimized for the FDM readout system. We measured a transition temperature of ~110 mK of our TES, although 90 mK was anticipated. Nevertheless, many pixels with various TES geometries showed encouraging results of 2.4-2.8 eV X-ray resolution at 6 keV photons. Next, we reduced the transition temperature by applying a metal diffusion process because the energy resolution is scaled with the three-halves power of the transition temperature. The detector chips were baked in a vacuum oven for 3 hours at 135 °C, which was determined from the experience in the previous work [12]. In this way, we could obtain a transition temperature of 90 mK and also confirmed that there were almost no changes in the shape of the transition curve. Although single pixel characterizations of the baked arrays are ongoing, a very promising energy resolution of 2.0 eV has been achieved experimentally so far with a 120×20 μm^2 TES (the normal resistance

of 150 mΩ) with the bias frequency of 2.2 MHz. The result is shown in Fig. 3.

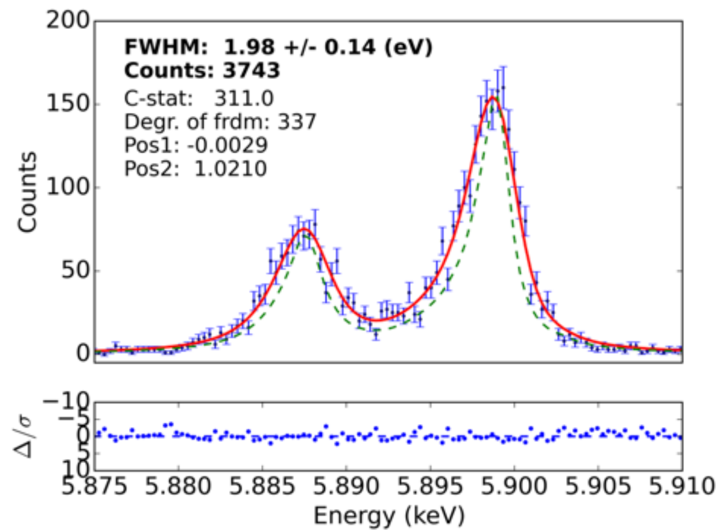

Fig. 3 The best achieved energy resolution at 5.9 keV is measured using a 120×20 μm^2 TES under the bias frequency of 2.2 MHz. The *blue dots* show measured data, the *red solid line* is the best fit to data, and the *green dashed line* indicates the natural line shape of the Mn-Kα complex [13] (Color figure online).

We plan to measure a 32×32 pixels array to validate uniformity in terms of the spectral performance over a number of pixels and evaluate the effect of electrical/thermal cross-talks. Our Au absorber device has quantum efficiency of ~83% at 6 keV. Although the X-IFU requirement for the quantum efficiency depends on X-ray telescope optics and filters, 90% efficiency or higher is expected from the sensor. We are also developing Au/Bi bi-layer absorbers in order to increase the X-ray stopping power while keeping the heat capacity at the current level [14]. We plan to continue optimization of the Bi electroplating process and produce devices with the Au/Bi absorbers in the near future.

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