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DOI
10.3390/ electronics11132076

Publication date
2022

Document Version
Final published version

Published in
Electronics (Switzerland)

Citation (APA)
Jiang, J., Wang, S., Liu, X., Liu, J., Li, J., Zhou, D., Zhang, K., Ye, H., & Tan, C. (2022). Electron-Irradiation-Induced Degradation of Transfer Characteristics in Super-Junction VDMOSFET. *Electronics (Switzerland)*, *11*(13). https://doi.org/10.3390/ electronics11132076

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Article

Electron-Irradiation-Induced Degradation of Transfer Characteristics in Super-Junction VDMOSFET

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Abstract: High electric-field stress is an effective solution to the recovery of irradiated devices. In this paper, the dependence of the recovery level on the magnitude of gate voltage and duration is investigated. Compared with the scheme of high gate-bias voltage with a short stress time, the transfer characteristics are significantly recovered by applying a low electric field with a long duration. When the electric field and stress time are up to a certain value, the threshold voltage almost approaches the limitation, which is less than that before irradiation. Meanwhile, the effect of temperature on the recovery of the irradiated devices is also demonstrated. The result indicates that a high temperature of 175 °C used for the irradiated devices' annealing does not play a role in promoting the recovery of transfer characteristics. In addition, to obtain a deep-level understanding of threshold degradation, the first-principles calculations of three Si/SiO_2 interfaces are performed. It is found that new electronic states can be clearly observed in the conduction bans and valence bands after the Si-H/-OH bonds are broken by electron irradiation. However, their distribution depends on the selection of the passivation scheme. Ultimately, it can be observed that the threshold voltage linearly decreases with the increase in interface charge density. These results can provide helpful guidance in the deep interpretation of threshold degradation and the recovery of the irradiated super-junction devices.

Keywords: electron irradiation; transfer characteristics; degradation; Si/SiO_2 interface; first-principles calculation; interface charge density; threshold variation

Citation: Jiang, J.; Wang S.; Liu, X.; Liu, J.; Li, J.; Zhou, D.; Zhang, G.; Ye, H.; Tan, C. Electron-Irradiation-Induced Degradation of Transfer Characteristics in Super-Junction VDMOSFET. *Electronics* **2022**, *11*, 2076. https://doi.org/10.3390/electronics11132076

Academic Editor: M. Tariq Iqbal

Received: 15 May 2022
Accepted: 28 June 2022
Published: 2 July 2022

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1. Introduction

With the advent of super-junction technology, the trade-off characteristic between breakdown voltage (BV) and specific on-resistance (R_{on}) in silicon-based power devices has dramatically improved [1,2]. Therefore, power-device manufacturing for higher voltages and currents can be realized. As one of the beneficiaries, vertical double-diffused MOSFETs (VDMOSFETs) have been extremely successful in the high-voltage power-conversion market due to the improvement of the theoretical limit of silicon ($R_{on}{\cdot}A \propto BV^{2.5}$) [3,4]. At present, Super-Junction VDMOSFET (SJ-VDMOSFET) has become a sole dominant flagship technology in the field of high-power switching and inverter systems where its blocking voltage is required in the range of 600–900 V [3]. Nevertheless, the switching performance of SJ-VDMOSFETs is significantly limited under high-frequency operation

due to the long minority-carrier lifetime of silicon chips. Consequently, in order to realize the improvement of the comprehensive performance of SJ-VDMOSFETs, the minority-carrier lifetime of the devices must be reduced properly by utilizing some lifetime control techniques. The underlying mechanism of these techniques to reduce minority carrier lifetime is the introduction of recombination centers in silicon devices.

Currently, the lifetime control techniques are mostly divided into two categories: (I) introducing heavy metal impurities in the chip-manufacturing process, such as gold [5], palladium [6], platinum [7], and so on; (II) high-energy (MeV) radiation, such as electron irradiation [8,9] and Co^{60} gamma irradiation [10]. For the first technique, owing to the inferior controllability of the diffusion process for heavy metal impurity and nonuniform distribution of diffusing impurity, the power devices possess the disadvantages of high leakage current and the poor blocking characteristics of high temperature. Therefore, this technique is not recommended for practical manufacturing processes. On the contrary, the second technique can accurately modulate the minority-carrier lifetime of the power devices by controlling the implantation dose; thus, the comprehensive performance of the power devices can be optimized. Furthermore, this technique greatly simplifies the manufacturing processes and design complexity of the power devices because it is used after device fabrication. Accordingly, high-energy radiation is widely used in the manufacture of power-switching devices, especially electron irradiation. Nevertheless, electron irradiation results in the buildup of oxide-trapped charge and the generation of interface traps [11,12], which severely influence the stability of electrical characteristics and reliability of MOS devices [13]. In particular, the negative shift of threshold voltage (V_{th}) after the electron irradiation is the most serious problem for the commercial MOS devices because the operation mode of devices may be changed from enhancement mode to depletion mode, thus leading to a possible failure of power system. In order to explore the basic mechanism of degradation of the V_{th}, an enormous number of studies have been conducted and abundant achievements have been reported [14–21]. However, the basic mechanism of radiation-induced degradation of the V_{th} in the SJ-VDMOSFET devices is still lacking. Meanwhile, previous studies mainly focus on an experimental level of influence mechanism and the relationship between the radiation dose and the V_{th}, but a deep-level theoretical research on the atomic scale has not been taken into account. Consequently, the degradation mechanism of the V_{th} caused by the electron irradiation and the recovery of the irradiated super-junction devices are worth investigating to meet the scientific research and commercial applications.

In this article, a study for the irradiation-induced degradation on the transfer characteristics (I_D–V_G) of SJ-VDMOSFETs is conducted, focusing on the recovery of the irradiated devices and the degradation mechanism in the atomic scale. It is found that the V_{th} of SJ-VDMOSFETs after electron irradiation can be recovered by applying a high gate-bias voltage at a suitable amount of time. The recovery level significantly increases with the decrease in the applied gate voltage and the multiplication of stress time. Moreover, a high temperature of 175 °C does not play a facilitating role in the recovery process. According to the density of states of the Si/SiO_2 interface, we find that new electronic states will be generated in the conduction bands and valence bands due to the fracture of the Si-H/-OH bonds induced by high-energy electrons. Their distribution is related to the passivation of the Si/SiO_2 interface. In addition, the quantitative relationship between the interface charge density (Q_{ss}) and threshold variation (ΔV_{th}) is also taken into account. The result clearly shows that the response of the threshold variation to the increasing multiples of interface charge density is a linear behavior.

2. Experimental and Computational Methods

The silicon-based Super-Junction VDMOSFET (*N*-channel) devices investigated in this article are fabricated by the same manufacturing process. The schematic diagram of two half-cells of SJ-VDMOSFET is shown in Figure 1. In detail, the chip size of the device is 0.049 cm^2. The thickness of the gate oxide layer of the device is 80 nm. In addition, the

V_{th} of the pristine SJ-VDMOSFET is 3.5 V and 2.1 V at 25 °C and 175 °C, respectively (Test condition: $V_{DS} = V_{GS}$, $I_{DS} = 250$ uA). For the irradiation experiment, the SJ-VDMOSFET chips were irradiated by using a high-energy electron source to a total dose of 50 kGy. Among them, we applied the irradiation experiment to 100 SJ-VDMOSFETs in the form of TO-220F outline package. Subsequently, we selected postirradiation SJ-VDMOSFETs with similar V_{th} (with an error of no more than 0.05 V) for recovery experiments and selected 10 SJ-VDMOSFETs with typical rules for discussion and analysis. For the recovery experiment, a high gate voltage was applied to the postirradiation SJ-VDMOSFETs, whereas source and drain were grounded at room temperature. In order to determine a critical voltage applied on gate, the voltage was gradually increased by an interval of 1 V. Simultaneously, since the reliability of the gate oxide may degrade under high electric-field stress, the time of electric-field stress applied on the gate should be considered. Additionally, the postirradiation SJ-VDMOSFETs were analyzed at room temperature of 25 °C and high temperature of 175 °C, respectively, to demonstrate the effect of temperature on the recovery of the irradiated devices. The theoretical models used for device performance calibration before and after ion irradiation included mobility models (Doping Dependence and High Field Saturation), recombination models (Shockley Read Hall and Auger), and effective intrinsic density model (OldSlotboom). In addition, the most important HeavyIon model was considered. The static characteristics of the irradiated devices were measured by ADVANTEST V93000 SOC.

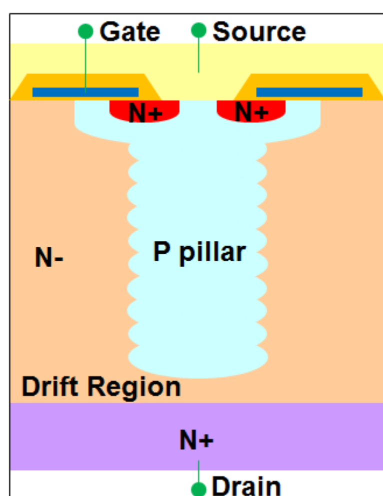

Figure 1. The cross-section schematic of *N*-channel Super-Junction VDMOSFET.

In order to obtain an insight into the degradation mechanism of the I_D-V_G in the atomic scale, the quantum mechanical calculations within the framework of density functional theory (DFT) were performed by using DMol^3 package, as implemented in Materials Studio [21,22]. The exchange–correlation density functional is described by employing the generalized gradient approximation (GGA) in the form of Perdew–Burke–Emzerhof (PBE) parameterization [23,24]. The full relaxation of atomic positions and lattice constants of Si/SiO_2 interface were conducted by adopting the double numerical plus polarization (DNP) basis set with the global cutoff of 5.0 Å. The convergence tolerance of energy and force on each atom were set to be 10^{-5} eV and 0.002 eV/Å, respectively. For the long-range van der Waals interactions in the Si/SiO_2 interface, the dispersion-corrected density functional theory (DFT-D) approach proposed by Grimme was adopted to effectively remedy the deficiency of the standard PBE functional [25,26]. A vacuum space of 15 Å was placed on the top and bottom of Si/SiO_2 interface to ensure no spurious interaction between the periodic interfaces in the direction perpendicular to the SiO_2 (0 1 0) plane. The Monkhorst–Pack k-point sampling in the Brillouin zone was set to be 9 × 9 × 4 for structural optimization and 13 × 13 × 4 for electronic structure calculations. Moreover, a

technology computer-aided designed (TCAD) simulation was performed to confirm the relationship between the increasing multiples of interface charge density (∇Q_{ss}) and ΔV_{th}.

3. Results and Discussion

In Figure 2, as observed in the irradiation experiment, it can be seen that the I_D-V_G curves shift toward the direction of the gate voltage, decreasing after the electron irradiation (a total dose of 50 kGy), which indicates that the operational reliability of SJ-VDMOSFETs will deteriorate due to the decrease in the V_{th}. Moreover, the V_{th} of the irradiated devices is less than 0.9 V, which is 2.7 V smaller than that of the pristine devices. In the case of large-dose irradiation, the interface traps and oxide traps increase, and the threshold voltage of the device shifts due to their combined effect. Following the introduction of a high electric-field stress at the gate, the purpose of our experiment is to fill the interface traps and oxide traps induced by irradiation with electrons to recover the V_{th} of the irradiated device to the initial level. In order to explore the relationship between the electric-field stress and stress time, a tremendous amount of testing was performed. Interestingly, for the case of gate voltage of 62 V, the leakage current of the gate dramatically decreases within the range of 0 s to 6 s, whereas it exhibits a nonlinear increasing trend when the stress time continues to increase from 6 s to 30 s, as depicted in Figure 3a. Considering the fluctuation of the gate oxide-layer thickness in the gate oxide-layer growth process, when the gate voltage is applied to 62 V, the charging process of the gate capacitor is completed within 0 s to 6 s. Subsequently, part of the gate oxide layer reaches its limit electric-field strength (10 MV/cm) and is broken down. This is also the main reason why the leakage current of the device exhibits a nonlinear increasing trend. On the contrary, when the applied gate bias is 60 V, the leakage current rapidly decreases in the range of 0 s to 20 s and then gradually stabilizes with the increase in stress time, as illustrated in Figure 3b. The stress time of applying bias voltage at the gate is five times longer than that in the case of 62 V. Simultaneously, a similar variation tendency for the leakage current of gate is also observed in two cases where the applied gate biases are 58 V [Figure 3c] and 55 V [Figure 3d], respectively. However, it should be noted that the leakage current still presents a downward trend after the bias voltage (58 V or 55 V) is applied at the gate for a long stress time. In a word, the time duration of the electric-field stress applied at the gate has a relationship of negative correlation with the magnitude of gate voltage. In addition, owing to a decrease of 2 V or 3 V in the applied gate bias, the stress time needs to be increased by at least twice. Therefore, it is extremely important to determine an appropriate gate voltage and the corresponding stress time for the recovery of irradiated devices.

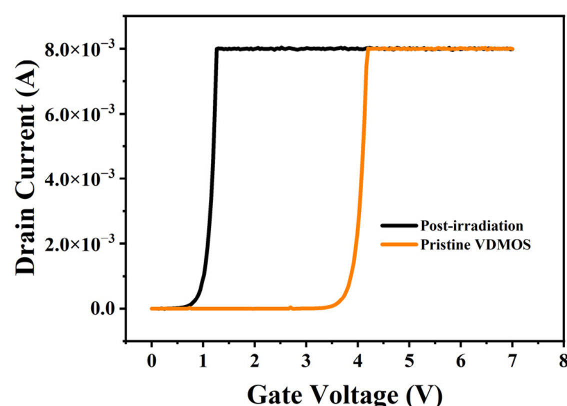

Figure 2. The transfer characteristic curves of the device before and after electron irradiation (a total dose of 50 kGy).

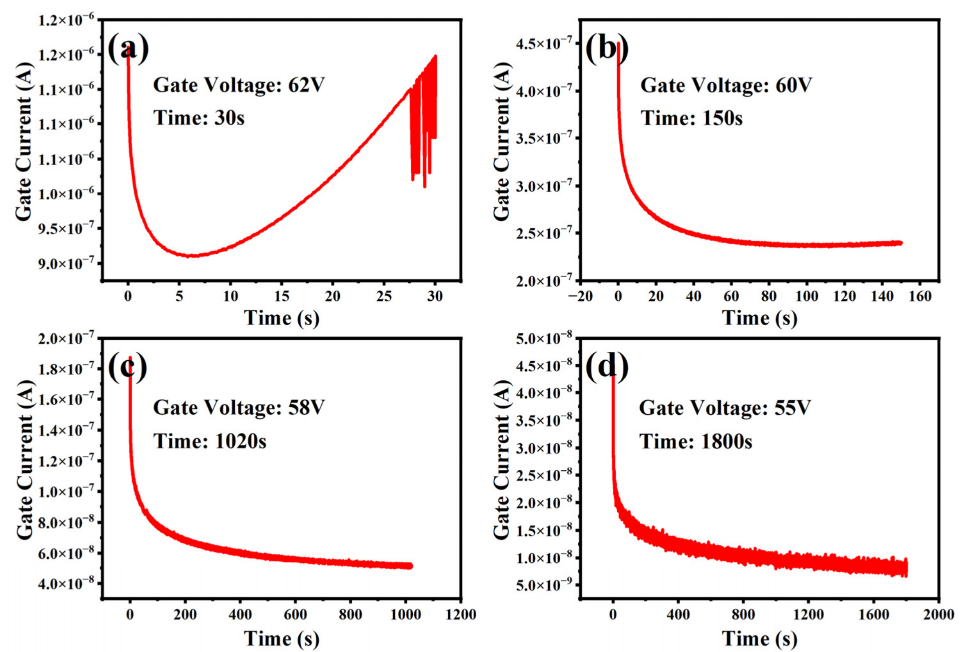

Figure 3. The leakage current of gate under different the electric field stress and stress time at room temperature.

In order to demonstrate the effectiveness of a high electric-field stress applied at the gate for the recovery of V_{th}, the measurement of the I_D–V_G curves and the corresponding V_{th} of the irradiated devices are carried out. Figure 4 clearly shows the shift of the I_D–V_G under different electric-field stress conditions. As observed in Figure 4a, the I_D–V_G curve shifts toward that of preirradiation after the voltages of 60 V, 58 V, and 55 V are introduced into the gate of the irradiated devices for a period of time, respectively. The recovery level in two cases where the applied gate biases are 58 V and 55 V is larger than that of the gate voltage of 60 V, which means that the utilization of a low bias voltage and a long stress time is more effective and feasible compared with that of a high bias voltage and a short duration. Furthermore, it is worth noting that the recovery level of the I_D-V_G curve under the condition of the gate bias of 55 V and the stress time of 1800 s is almost the same as the case where the gate voltage and the time duration are 58 V and 1020 s, respectively. A short stress time is responsible for this result based on the above-discussed of the leakage current at room temperature. For the case of the gate bias of 62 V, a negative shift relative to the direction of the gate bias increasing is observed after the stress time of 150 s, being attributed to the increase in the leakage current induced by the high electric field applied at the gate for a long stress time. The probability of temperature facilitating the recovery of the irradiated devices is investigated by performing testing under a temperature of 175 °C. The I_D–V_G of the irradiated devices annealed at 175 °C is described in Figure 4b. Clearly, there is no apparent change of the I_D-V_G curves compared with that without electric-field stress. Although an observable positive shift relative to the direction of the gate bias decreasing is obtained under the gate voltage of 60 V, the recovery level of V_{th} is still tiny in comparison to the V_{th} of preirradiation. Therefore, we can reach a conclusion that a high temperature of 175 °C applied for annealing the irradiated devices is not conducive to the recovery of the I_D-V_G. For quantitative comparative analysis, the V_{th} of the irradiated devices with and without the gate biases are measured and listed in Table 1. In the case of the room temperature, the V_{th} of the irradiated devices without a gate bias is 0.84 V. This is changed to 0.63 V, 1.65 V, 2.48 V, and 2.52 V for the gate voltages of 62 V, 60 V, 58 V, and 55 V, respectively. With the exception of the case of 65 V, the V_{th} has a remarkable recovery for other three cases and the maximum increment is 1.68 V. Conversely, the maximum variation of the V_{th} is only 0.3 V for the case of 175 °C, being much smaller than that at the room temperature.

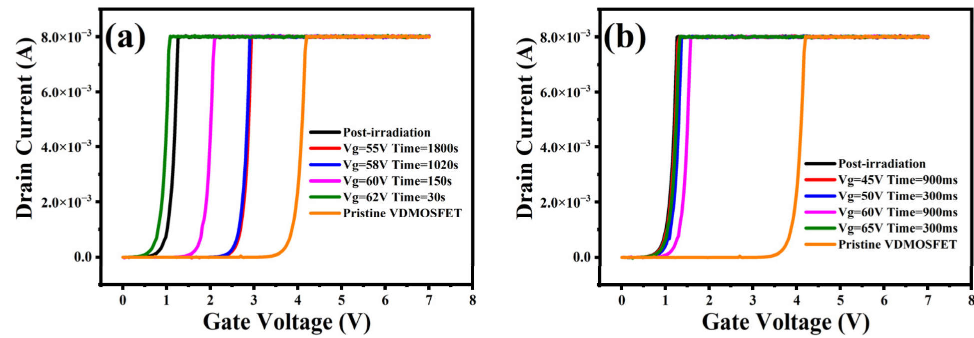

Figure 4. The transfer characteristics of the irradiated devices under different gate-voltage conditions: (**a**) At room temperature of 25 °C; and (**b**) a temperature of 175 °C.

Table 1. The threshold voltage of the irradiated devices before and after applying the testing conditions.

Tem. (°C)	$V_{thini.}$ (V)	Vg (V)	Stress Time (s)	$V_{threc.}$ (V)	ΔV_{th} (V)
25	0.84	55	1800	2.52	1.68
		58	1020	2.48	1.64
		60	150	1.65	0.81
		62	30	0.63	−0.21
175	0.84	45	0.9	0.85	0.01
		50	0.3	0.93	0.09
		60	0.9	1.14	0.30
		65	0.3	0.88	0.04

Up to now, many experimental studies [27–31] focusing on the macroscale analysis of physical mechanisms of threshold degradation for high-power devices have been performed in detail, but atomic-scale analysis based on the quantum mechanics for Super-Junction VDMOSFETs is still lacking. Moreover, the enormous number of previous reports [32–36], including theoretical and experimental research, show that the quantum mechanical calculation has been a powerful tool in deeply understanding the atomic structures and electronic properties in interfacial engineering. Consequently, it is very meaningful to investigate the atomic structures and electronic properties of the Si/SiO_2 interface with and without electron irradiation. In this section, we mainly discuss the variation of density of states of the Si/SiO_2 interface before and after irradiation.

Atomic structures of the Si/SiO_2 interface. There are three different interfacial models formed by silica and silicon, namely the hydrogen model (HGM), hydroxyl model (HXM), and hydrogen-hydroxyl model (HGXM), as displayed in Figure 5. Among the various possibilities of interfacial passivation [37], we are interested only in the hydrogen atom (H) and hydroxyl group (OH), because the mainstream concept of previous studies for threshold degradation is the destruction of Si-OH bonds and Si-H bonds where the interaction between Si atom and -OH/-H is weak. The crystalline β-cristobalite is adopted to represent the amorphous SiO_2 of oxidation process in all models, for which it has been found that the potential barrier heights of β-cristobalite for electrons and holes are almost in accordance with that of amorphous silica [37,38]. More importantly, the lattice constant of β-cristobalite is approximately $\sqrt{2}$ times that of diamond silicon [39]; thus, the average mismatch of lattice constant is smaller than 6%. Furthermore, by means of introducing H atoms, the Si dangling-bonds at the top and bottom of the interfacial models are saturated to obtain the accurate and reliable results [40]. The unit cell is an abrupt interfacial structure without a nominal transition region. We carry out the structural relaxation of the Si/SiO_2 interfacial models to reach the ground state of models and obtain the correspond-

ing authentic parameters by depending on the aforementioned DFT method. The calculation results based on the lowest-energy conformation are listed in Table 2. It can be found that the lengths of Si-H bonds and Si-OH bonds located between the Si layer and SiO_2 layer are 1.48 Å and 1.70 Å for HGM and HXM, respectively. In the case of HGXM, the bond lengths of Si-H and Si-OH are 1.47 Å and 1.68 Å, respectively, which are greatly close to that of HGM and HXM. However, there is a big difference between the angle of Si-Si-OH in the HXM; the θ_1 and θ_2 are 73.7° and 113.5°, respectively.

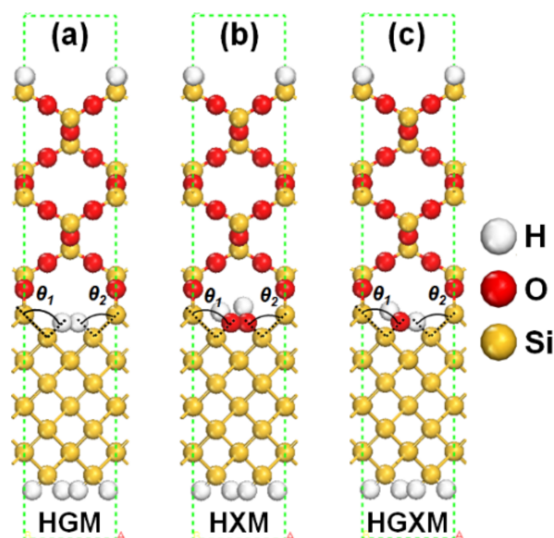

Figure 5. The atomic configuration of three Si/SiO_2 interfacial models investigated in the first-principles calculation: (**a**) with hydrogen atom, (**b**) with hydroxyl group, and (**c**) with both hydrogen atom and hydroxyl group.

Table 2. Calculated structural information of HGM, HXM, and HGXM. d_1 and d_2 are the corresponding length of Si-H/-OH bonds in the angle of Si-Si-H/-OH (θ_1 and θ_2), respectively.

Model	Bond Length (Å)		Bond Angle (°)	
	d_1	d_2	θ_1	θ_2
HGM	1.48	1.48	102.7	102.8
HXM	1.70	1.70	73.7	113.5
HGXM	1.68	1.47	98.9	108.8

Density of states of the Si/SiO_2 interface. After determining the Si/SiO_2 interfacial configurations, we calculated their total and partial density of states (TDOS and PDOS) without and with electron irradiation to better understand the physical mechanism of threshold degradation at the atomic level. The TDOS and PDOS of HGM, HXM, and HGXM are presented in Figures 5 and 6, respectively. One can find that there are some new electronic states in the energy band within the range of 0.0 eV to 0.7 eV after one H atom of HGM is removed, whereas for the HGM without H atoms the new electronic states are distributed in the range of 0.35 eV to 1.5 eV [see Figure 6a]. This result manifests that the new states in the band gap are caused by Si atoms with dangling bonds. The PDOS of the HGM with one and two Si dangling-bands provides further evidence to the origin of new states. As presented in Figure 6b, three new peaks of electronic states for the case of one Si dangling-band are observed and located at 0.06 eV, 0.32 eV, and 0.56 eV, respectively. There are four new peaks located above valence bands due to the fracture of two Si-H bonds; their energy coordinates are 0.48 eV, 0.60 eV, 0.80 eV, and 1.26 eV, respectively. For the scheme of passivation with OH group, it can be found that two new peaks are localized in the vicinity of the Fermi level when one of Si-OH bands is broken by high-energy electrons, while the TDOS of the HXM with two Si dangling bonds is almost similar with that of the HGM without H atoms [see Figure 6c]. The result is further confirmed by the PDOS of the

HXM with one and two Si dangling-bands, as illustrated in Figure 6d. As can be seen, one new peak is generated in the valence bands and its energy coordinate is −0.25 eV; another two peaks are located above the valence bands at 0.09 eV and 0.42 eV for the case of one Si dangling bond, respectively. For the case of two Si dangling bonds, four new peaks are distributed in the conduction bands and the corresponding coordinates are almost the same as that of the HGM without H atoms. It is worth noting that the electronic states in the conduction bands are distinguished from those of the HXM with one Si dangling bond when the Si-H bond of HGXM is broken, as displayed in Figure 6e,f. A weak peak at 0.39 eV is almost negligible, being five times smaller than the electronic-state peak induced by the Si dangling bond of the HXM. Nevertheless, the variation of electronic states in the conduction bands caused by the break of the Si-OH bond or Si-H/-OH bond after irradiating shows nearly no difference based on their TDOS and PDOS. These results clearly indicate that electron irradiation only affects the electronic states of the conduction bands in the HGM due to the fracture of Si-H bands, while for the HXM and HGXM, the electronic states near the Fermi level are changed on account of the existence of Si dangling bonds. Moreover, the variation of electronic states depends on the number of Si dangling bonds and the passivation scheme. In fact, the electronic states of conduction bands and valence bands (near the Fermi level) of the Si/SiO_2 interface will be simultaneously influenced in the practical engineering.

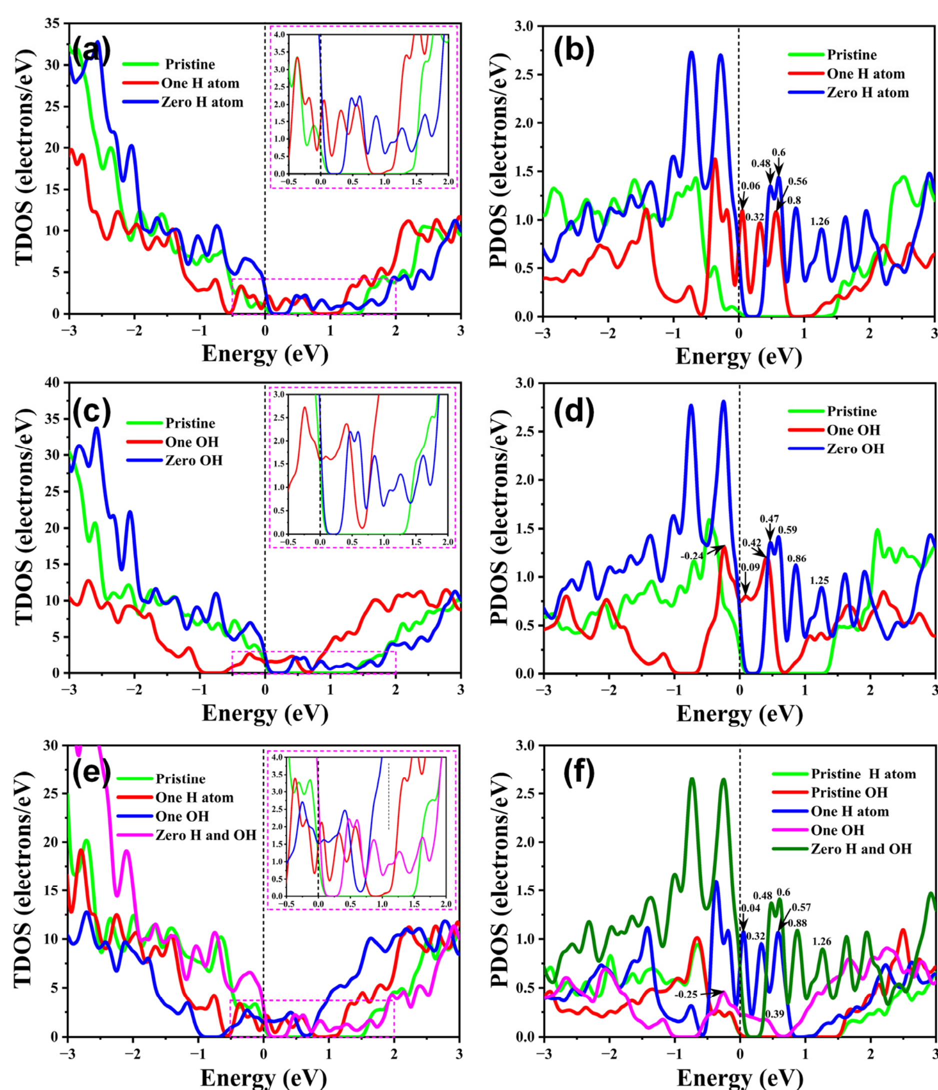

Figure 6. The total and partial density of states of (**a**,**b**) HGM, (**c**,**d**) HXM, and (**e**,**f**) HGXM before and after irradiating. The Fermi level is set to zero and denoted by the black dashed line.

According to the above discussion, the diminution of V_{th} is ascribed to the increase in Q_{ss} after irradiating. Therefore, to further explore the quantitative relationship between the ∇Q_{ss} and ΔV_{th}, we carried out a TCAD simulation. Before starting the numerical simulation of the I_D–V_G of the irradiated devices, it is essential to validate the correctness and availability of the simulated model to acquire reasonable and reliable results. Figure 7 clearly shows that the I_D-V_G curve of the simulated model is nearly in accordance with that of SJ-VDMOSFETs before irradiating, and the V_{th} of the simulated model with the Q_{ss} of 3×10^{10} cm^{-2} is 3.5 V. These results authoritatively demonstrate the correctness and rationality of structural parameters of the simulated model. Afterwards, we determined the Q_{ss} corresponding to the D of 50 kGy is 7.2×10^{11} cm^{-2} according to the comparison of simulation result with experimental result. The simulated V_{th} for the Q_{ss} of 7.2×10^{11} cm^{-2} is 0.80 V which is in good agreement with that of the irradiated device. The I_D-V_G curves of the simulated model with the Q_{ss} of 3×10^{10}, 3×10^{11}, 4×10^{11}, 5×10^{11}, 6×10^{11}, 7.2×10^{11}, 8×10^{11}, and 9×10^{11} cm^{-2} are shown in Figure 8a. It can be found that the I_D-V_G curve gradually shifts along the direction of decreasing gate voltage with the increase in Q_{ss}, but the variation trend of the drain current with the increasing gate voltage is unchanged. The channel is almost open when the Q_{ss} is up to 9×10^{11} cm^{-2}, and the corresponding V_{th} is only 0.15 V; that is, 23 times smaller than the value with 3×10^{10} cm^{-2}. The absolute value of ΔV_{th} ($|\Delta V_{th}|$) as a function of the ∇Q_{ss} is illustrated in Figure 8b. As a note, the Q_{ss} of 3×10^{10} cm^{-2} and the V_{th} of 3.5 V are used as a benchmark for the change of Q_{ss} and V_{th}, respectively. It is clearly shown that the $|\Delta V_{th}|$ increases linearly with the increase in ∇Q_{ss} and the increment between two $|\Delta V_{th}|$ is 0.4 V in the range of 4×10^{11} cm^{-2} to 6×10^{11} cm^{-2} with a step of 1×10^{11} cm^{-2}. The linear function obtained by fitting the scatter points is represented as $|\Delta V_{th}| = 0.116\nabla Q_{ss} - 0.137$, where $|\Delta V_{th}| = |V_{th}' - 3.5|$ and $\nabla Q_{ss} = Q_{ss}'/(3 \times 10^{10})$. This formula clearly shows that the interface charge density is a critical factor for the reliability of gate oxide and the operation mode of MOS devices.

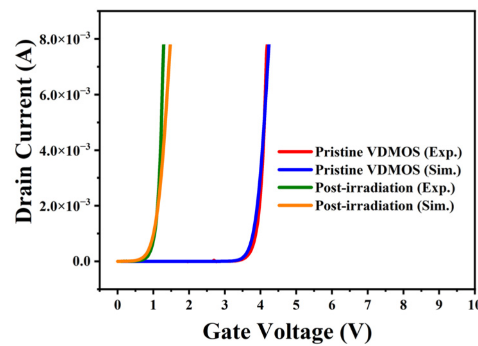

Figure 7. The transfer characteristics of pristine VDMOS and postirradiation in the experiment and simulation.

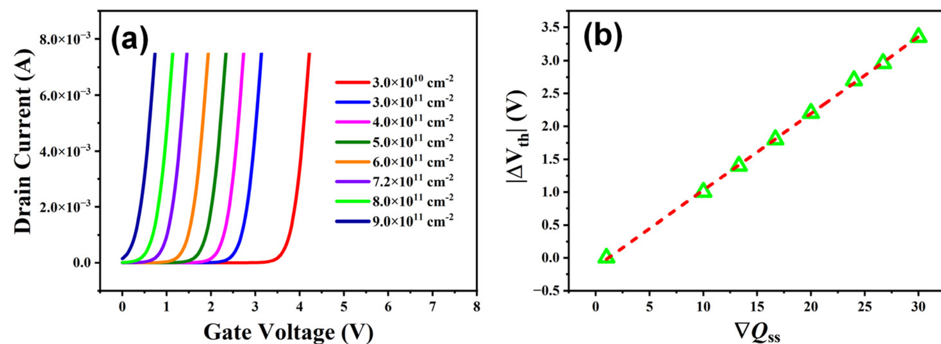

Figure 8. (**a**) The transfer characteristics of simulate model with different interface charge density. (**b**) The variation of threshold voltage as a function of the increasing multiples of interface charge density.

4. Conclusions

In summary, we perform a detailed study on irradiated SJ-VDMOSFET devices, focusing on the recovery of transfer characteristics, the degradation mechanism at the atomic level, and the dependence of threshold voltage on interface charge density. By applying a high positive bias voltage to the gate of the irradiated devices at a moderate stress time, the threshold voltage of the irradiated devices can be effectively recovered due to the reduction in interface charge. The recovery level depends on the magnitude of gate bias and stress time, but the threshold voltage is barely unchanged when the positive electric field and stress time reach a certain value, respectively. A low positive gate bias with a long duration is beneficial to promote the recovery of the irradiated devices. Meanwhile, we also found that a high annealing temperature does not act as a positive impact in the recovery process by comparing the results at room temperature and a temperature of 175 °C. The first-principles calculations demonstrate that the new electron states after irradiating can be observed in the conduction bands and valence bands, which is attributed to the break of Si-H/-OH bonds in the Si/SiO_2 interface. The distribution of these states is determined by the passivation schemes. Finally, it can be found that the threshold variation linearly depends on the increasing multiples of interface charge density. Our works can provide an insight into the degradation mechanism at an atomic level and recovery of the irradiated super-junction devices.

Author Contributions: Writing—original draft preparation, J.J.; writing—review and editing, S.W.; investigation and software, X.L.; methodology, J.L. (Jianhui Liu) and C.T.; resource, D.Z.; project administration and funding acquisition, J.L. (Jun Li); supervision, G.Z., H.Y., and C.T. All authors have read and agreed to the published version of the manuscript.

Funding: this research was funded by the National Key R&D Program of China (2018YFE0204600), the Shenzhen Fundamental Research Program (JCYJ20200109140822796), the NSQKJJ under grant K21799119, and the Key Technology Projects in Shenzhen (JSGG20201201100406019).

Data Availability Statement: Data available on request from the authors.

Conflicts of Interest: The authors declare no conflict of interest.

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