A 590 µw, 106.6 dB SNDR, 24 kHz BW Continuous-Time Zoom ADC with a Noise-Shaping 4-bit SAR ADC

Mehrotra, Shubham; Eland, Efraim; Karmakar, Shoubhik; Liu, Angqi; Gonen, Burak; Bolatkale, Muhammed; Van Veldhoven, Robert; Makinwa, Kofi A.A.

DOI
10.1109/ESSCIRC55480.2022.9911295

Publication date
2022

Document Version
Final published version

Published in
ESSCIRC 2022 - IEEE 48th European Solid State Circuits Conference, Proceedings

A 590 µW, 106.6 dB SNDR, 24 kHz BW Continuous-Time Zoom ADC with a Noise-Shaping 4-bit SAR ADC

Shubham Mehrotra[1,2], Efraïm Eland[1], Shoubhik Karmakar[1], Angqi Liu[1], Burak Gönen[1,3], Muhammed Bolatkale[1,2], Robert van Veldhoven[2], and Kofi A. A. Makinwa[1]
[1]Delft University of Technology, Delft, [2]NXP Semiconductors, Eindhoven, [3]Ethernovia, Zeist, The Netherlands
Email: shubham.mehrotra@nxp.com

***Abstract*—This paper presents a continuous-time zoom ADC for audio applications. It combines a 4-bit noise-shaping coarse SAR ADC and a fine delta-sigma modulator with a tail-resistor linearized OTA for improved linearity, energy efficiency, and handling of out-of-band interferers compared to previous designs. In 160 nm CMOS, the prototype chip occupies 0.36 mm², achieves 107.2 dB SNR, 106.6 dB SNDR, and 107.3 dB dynamic range in a 24 kHz bandwidth while consuming 590 µW from a 1.8 V supply. This translates into a Schreier figure-of-merit (FoM_S) of 183.4 dB and a FoM_{SNDR} of 182.7 dB.**

***Keywords*—A/D conversion, audio analog to digital converter (ADC), continuous-time delta-sigma ADC, dynamic zoom ADC, low-power circuits, noise-shaping SAR ADC, high linearity operational transconductance amplifier (OTA)**

I. Introduction

ADCs for audio applications such as battery-powered CODECs often require high linearity, dynamic range (DR), and energy efficiency. Zoom ADCs meet these requirements by using a low-power coarse SAR ADC to update the references of a fine delta-sigma modulator (ΔΣM). However, previous discrete-time (DT) zoom ADCs [1, 2] place stringent requirements on the linearity of the input and reference drivers needed to charge their sampling capacitors with large signal-dependent peak currents. The resistive input of a continuous-time (CT) zoom ADC [3] is easier to drive but a power-hungry OTA is needed to ensure that its first integrator achieves sufficiently high linearity. Another limit on the linearity of zoom ADCs is the non-unity STF of their fine ΔΣMs which causes in-band leakage of the SAR ADC's quantization noise (also referred to as "fuzz"). This can be mitigated, at the expense of complexity, by adding a digital filter after the SAR ADC [2], or by using a feedforward path in the fine ΔΣM to enforce a unity STF [1]. However, the effectiveness of both techniques is limited by analog spread.

To address these limitations, this work presents a CT zoom ADC that employs passive noise-shaping in its coarse SAR ADC to robustly and efficiently shape its fuzz out of band (OOB). Furthermore, the 1st integrator of the fine ΔΣM employs a tail-resistor linearized (TRL) OTA, allowing it to be designed solely for noise, rather than for linearity, thus reducing power dissipation. Together, these techniques result in high energy efficiency (FOM_{SNDR} = 182.7 dB), and the lowest in-band noise and distortion spectral density (NDSD = −150.4 dBFS/Hz) amongst state-of-the-art audio ADCs.

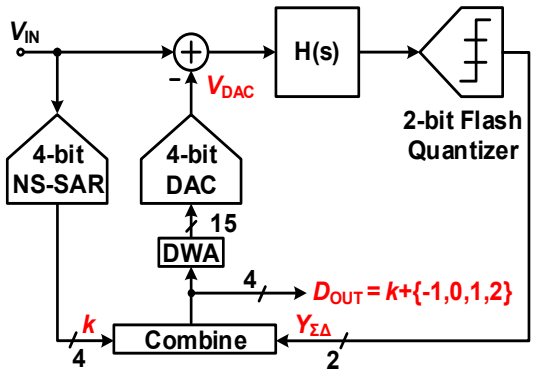

Fig. 1. Proposed CT zoom ADC architecture.

II. Proposed CT Zoom ADC

A. Architecture

Fig. 1 shows the simplified architecture of the proposed zoom ADC. It consists of a 4-bit asynchronous SAR ADC and a 2-bit CT ΔΣM running concurrently at a sampling frequency (F_s) = 5.12 MHz. The SAR output (k) updates the references of ΔΣ DAC with 1 LSB of over-ranging such that $V_{REF-} = (k-1).V_{LSB} < V_{IN} < (k+2).V_{LSB} = V_{REF+}$, where V_{LSB} is the quantization step-size of the fine ΔΣ DAC. As in [1], the resulting 3 LSB range can then be well matched to the steps of the 2-bit ΔΣM.

In a zoom ADC, OOB interferer tracking is limited by the conversion speed of the SAR ADC and F_s, making the ΔΣM susceptible to overload in the presence of fast OOB interferers. Although these interferer signals can be easily removed by using a low pass filter at the input, a sharp cut-off filter is undesirable in a CT ΔΣM that should benefit from relaxed anti-aliasing filter requirements. For improved robustness to OOB interferers, this work uses a 4-bit SAR ADC as a coarse quantizer rather than the 5-bit SAR of previous designs [1, 2, 3], thereby relaxing the anti-overloading filter requirements. However, this introduces more quantization noise and fuzz in the zoom ADC's output spectrum. Apart from limiting its in-band linearity, the presence of OOB fuzz increases the requirements on the digital decimation filter. In this work, this is addressed by implementing noise-shaping in the 4-bit SAR ADC, which effectively decorrelates and shapes the quantization noise of the SAR ADC OOB, and thus reduces the fuzz significantly.

ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC) | 978-1-6654-8494-7/22/$31.00 ©2022 IEEE | DOI: 10.1109/ESSCIRC55480.2022.9911295

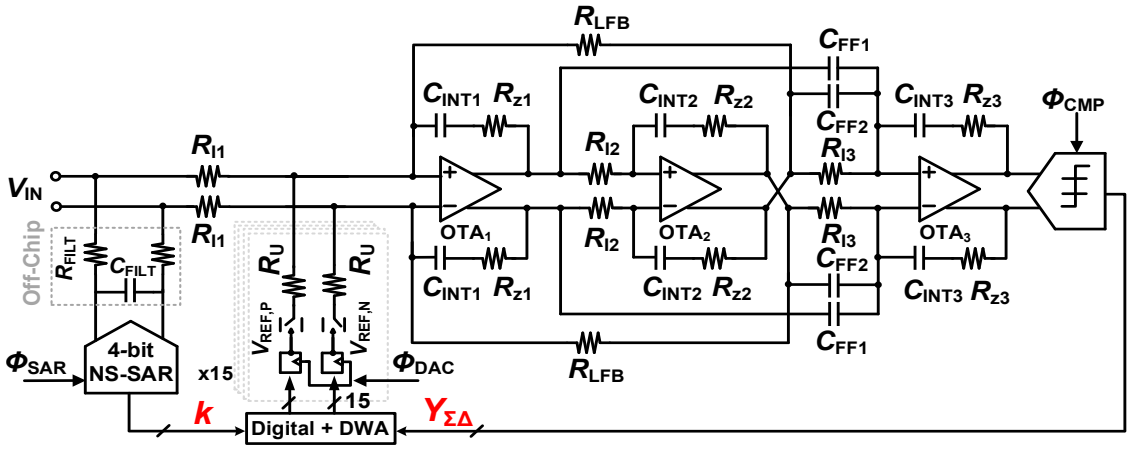

Fig. 2. Simplified schematic of the proposed CT zoom ADC.

To maintain energy efficiency, the noise shaping (NS) in the SAR ADC is realized with a passive integrator [4].

B. Circuit Implementation

Fig. 2 shows a simplified schematic of the proposed zoom ADC. The ΔΣM employs a 3rd order CIFF loop filter. In contrast to [3], the loop filter employs a local feedback loop (via R_{LFB}) which creates an NTF notch for better noise shaping. Furthermore, the linearity of OTA$_1$ is improved by the tail-resistor linearization technique [5]. The resulting OTA (Fig. 3) is >17x more linear than the one used in [3], allowing it to be biased at half the tail current (I_{tail} = 56 μA, R_{tail} = 167 Ω) to meet noise requirements while achieving a DC gain of 60 dB over PVT. The improved linearity also facilitates the use of noise shaping in the SAR ADC, despite this producing ~3x more virtual ground swing than a conventional 4-bit SAR (Fig. 4). OTA$_1$ is chopped at F_s, which mitigates its 1/f noise, and also improves its CMRR and PSRR. As in [3], OTA$_{2,3}$ are implemented as current-reuse amplifiers, while the feedback DAC consists of a 4-bit unary NRZ R-DAC. The 2-bit flash quantizer has a conversion time of <8 ns over PVT, which even with the added delay of the DWA logic, is well within the fixed loop delay of $T_s/8$ = 24 ns.

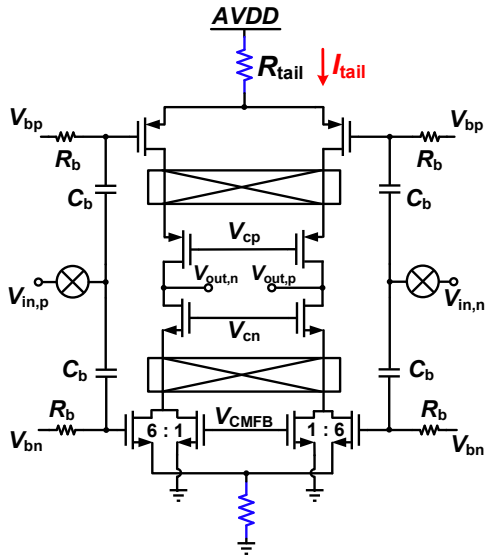

Fig. 3. Tail-Resistor-Linearized OTA$_1$.

As shown in Fig. 5, the SAR ADC consists of a 4-bit C-DAC (C_u = 1.8 fF), a comparator, asynchronous digital logic, and a passive noise shaper. At the end of the SAR conversion, the residue signal is sampled on one of two pairs of capacitors ($C_{1R(P,N)}$ or $C_{2R(P,N)}$). These are then used in a ping-pong scheme to sample the residue during a conversion cycle ($C_{1R(P,N)}$ in ϕ_{NS1} and $C_{2R(P,N)}$ in ϕ_{NS2}) and then transfer it to a pair of integration capacitors (C_{IP} and C_{IN}) during the next cycle [4]. The aggressiveness of this passive noise-shaping scheme is determined by the ratio $C_{(1,2)RP}/C_{IP}$, which is set to 0.6 to ensure that the output swing of the SAR ADC does not exceed the range of the fine ΔΣM.

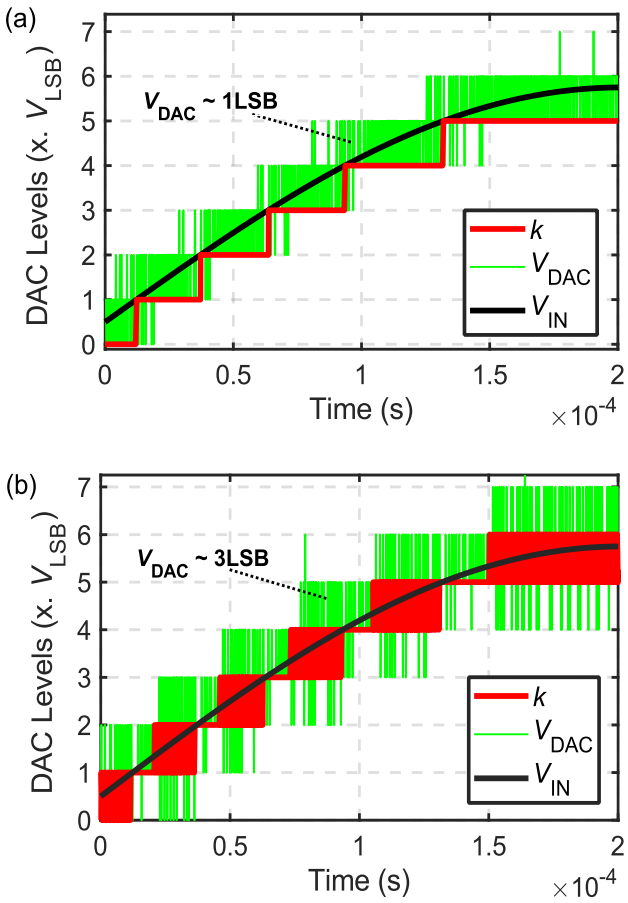

Fig. 4. SAR ADC (k) and ΔΣ DAC (V_{DAC}) output (a) w/o NS in SAR ADC (b) w/i NS in SAR ADC.

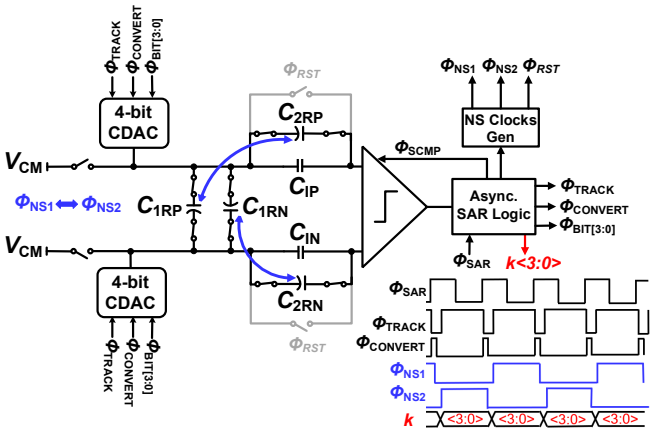

Fig. 5. Simplified schematic of the 4-bit NS-SAR ADC.

III. Measurement Results

The fabricated prototype chip occupies an active area of 0.36 mm^2 (Fig. 6) and draws a current of 327.7 µA from a 1.8 V supply. The analog, digital, and reference blocks account for 40.1%, 26.4%, and 33.5% of the total power consumption, respectively. For a 1 kHz, –0.35 dBFS input signal, the measured SNDR and THD of the 4-bit SAR ADC with NS "OFF" is 30.3 dB and –30.4 dB, respectively, (Fig. 7). With NS "ON", its in-band quantization noise is suppressed by about 9.5 dB, while its SNDR and THD improve by 14.5 dB and 14.6 dB, respectively. With NS "OFF", the measured peak SNR, SNDR, and THD of the zoom ADC are 107.2 dB, 105.4 dB, and –110.5 dB, respectively (Fig. 8). Turning NS "ON" effectively suppresses in-band fuzz and improves the SNDR, and THD of the zoom ADC by 1.2 dB and 5.5 dB, respectively. The tone at $F_s/2$ with NS "ON" comes from the SAR ADC as it toggles predominately between 2 levels while resolving the residue. The design achieves a DR of 107.3 dB (Fig. 9) with NS "ON", which is mainly limited by residual DWA tones. Fig. 10 shows the integrated in-band noise of the ADC (20 Hz to 24 kHz) when a –1.5 dBFS input signal is swept over frequency. The integrated noise is unaffected for input frequencies < 95 kHz, which is higher than that reported for previous zoom ADCs. Over the entire audio band, the measured CMRR and PSRR of the ADC are greater than > 66 dB (Fig. 11). For -6 dBFS input signals around F_s, the measured alias rejection of the zoom ADC is > 80 dB in the audio band (Fig. 12). As in [3], a relaxed 800 kHz RC low-pass filter (R_{FILT} =20 kΩ, C_{FILT} =5 pF) is enough to suppress the effects of aliasing in the SAR ADC itself.

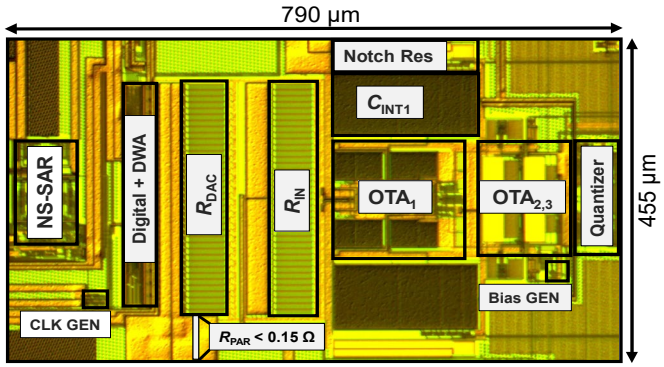

Fig. 6. Die Micrograph of the CT zoom ADC.

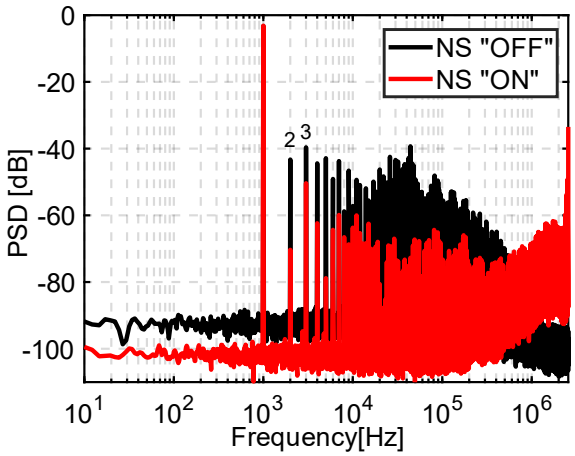

Fig. 7. Measured PSD of SAR ADC.

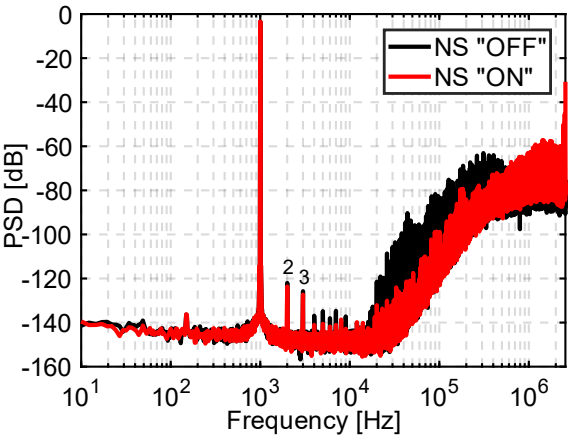

Fig. 8. Measured PSD of zoom ADC (2^{21} points, 8 averages, Blackman-Harris window).

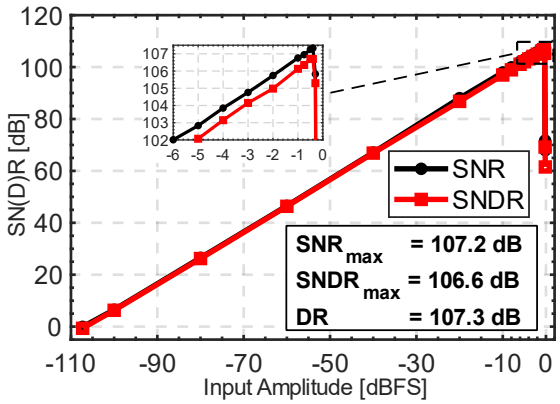

Fig. 9. Measured SN(D)R of zoom ADC across input amplitude.

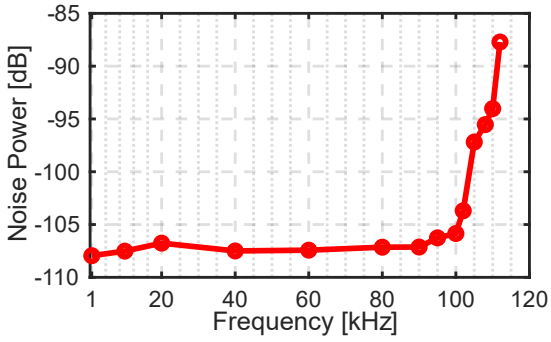

Fig. 10. Total in-band noise power across F_{IN} for a -1.5 dBFS input signal.

Table I. Performance summary and comparison

	This Work	*ISSCC'22* [9]	*ISSCC'21* [6]	*ISSCC'21* [7]	*JSSC'21* [1]	*ISSCC'20* [8]	*JSSC'20* [3]
Architecture	**CT Zoom**	DT PPD	CT	CT FIR DAC	DT Zoom	CT 3-level	CT Zoom
Tech (nm)	**160**	180	28	65	160	65	160
Area (mm^2)	**0.36**	0.03	0.07	0.39	0.27	0.28	0.27
Supply (V)	**1.8**	1.8/1.1	1.8/1.0	1.2	1.8	1.2	1.8
Power (µW)	**590**	203.5	116	139	440	134	618
F_s (MHz)	**5.12**	5.80	6.144	7.2	3.5	8	5.12
BW (kHz)	**24**	20	24	24	20	24	20
SNR_{max} (dB)	**107.2**	106.7	100.7	102.0	107.5	101.0	108.1
$SNDR_{max}$ (dB)	**106.6**	105.4	100.6	100.9	106.5	99.4	106.4
DR (dB)	**107.3**	108.8	104.4	104.8	109.8	103.5	108.5
NDSD$^+$(dBFS/Hz)	**-150.4**	-148.4	-144.4	-144.7	-149.5	-143.2	-149.4
$FoMS_{NDR}^*$ (dB)	**182.7**	185.3	183.7	183.3	183.1	181.9	181.5
$FoMS^{**}$ (dB)	**183.4**	188.7	187.5	187.2	186.4	186.0	183.6

$^+$Noise+Distortion Spectral Density (NDSD) = $-(SNDR_{max} + 10\log_{10}(BW))$dBFS/Hz
*$FoMS_{NDR}$ = SNDR + $10\log_{10}$(BW/Power) **$FoMS$ = DR + $10\log_{10}$(BW/Power)

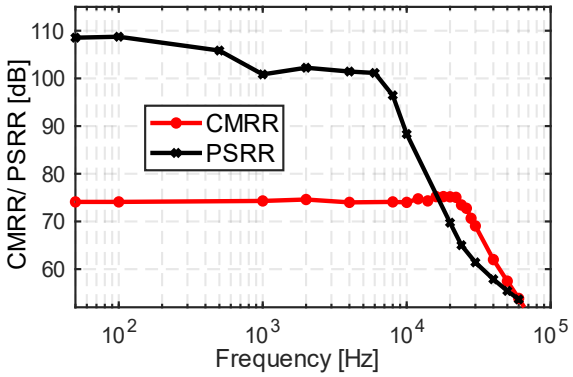

Fig. 11. Measured CMRR & PSRR across input/supply frequency.

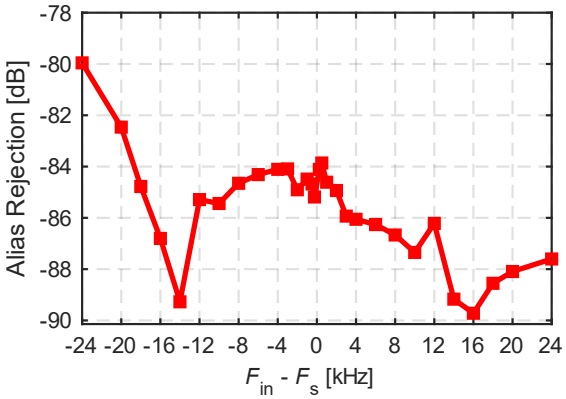

Fig. 12. Alias rejection of the CT zoom ADC (input: -6 dBFS).

Table I summarizes the performance of the designed CT zoom ADC and compares it with that of other state-of-the-art audio ADCs. When compared to the previous CT zoom ADC [3], this design achieves higher energy efficiency ($FoMS_{NDR}$) over a somewhat wider bandwidth (24 kHz versus 20 kHz), demonstrating the effectiveness of the techniques used in this work. The ADCs in [1, 9] have better FoM but are DT and require high-power input buffers to drive their switched-capacitor front ends, resulting in overall higher system power. The ADCs in [6, 7, 8] have higher energy efficiency but are realized in more advanced technologies resulting in significantly lower digital power and area, especially for clock generation and the DWA logic. It should be noted that the designs in [6, 7, 8] also target significantly lower (~6 dB) $SNDR_{max}$ specifications.

IV. Conclusions

This paper describes a CT zoom ADC for audio applications. Through the use of analog techniques such as passive noise shaping in the coarse SAR ADC and tail-resistor-linearization in the OTA_1, high linearity is achieved without compromising the energy efficiency. The proposed ADC achieves a competitive Schreier figure-of-merit ($FOMS$) of 183.4 dB and $FOMS_{NDR}$ of 182.7 dB, together with the lowest in-band noise and distortion spectral density (NDSD = –150.4 dBFS/Hz) amongst state-of-the-art audio ADCs.

References

[1] E. Eland, S. Karmakar, B. Gönen, R. van Veldhoven and K. A. A. Makinwa, "A 440-µW, 109.8-dB DR, 106.5-dB SNDR Discrete-Time Zoom ADC With a 20-kHz BW," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 4, pp. 1207-1215, April 2021

[2] S. Karmakar, B. Gönen, F. Sebastiano, R. van Veldhoven and K. A. A. Makinwa, "A 280 µW Dynamic Zoom ADC With 120 dB DR and 118 dB SNDR in 1 kHz BW," in *IEEE Journal of Solid-State Circuits*, vol. 53, no. 12, pp. 3497-3507, Dec. 2018

[3] B. Gönen, S. Karmakar, R. van Veldhoven and K. A. A. Makinwa, "A Continuous-Time Zoom ADC for Low-Power Audio Applications," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 1023-1031, April 2020

[4] Y. -Z. Lin, C. -Y. Lin, S. -C. Tsou, C. -H. Tsai and C. -H. Lu, "20.2 A 40MHz-BW 320MS/s Passive Noise-Shaping SAR ADC With Passive Signal-Residue Summation in 14nm FinFET," *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2019, pp. 330-332

[5] S. Pan and K. A. A. Makinwa, "A 10 fJ·K^2 Wheatstone Bridge Temperature Sensor With a Tail-Resistor-Linearized OTA," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 2, pp. 501-510, Feb. 2021, doi: 10.1109/JSSC.2020.3018164.

[6] C. Lo *et al.*, "10.1 A 116µ W 104.4dB-DR 100.6dB-SNDR CT ΔΣ Audio ADC Using Tri-Level Current-Steering DAC with Gate-Leakage Compensated Off-Transistor-Based Bias Noise Filter," *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, 2021, pp. 164-166, doi: 10.1109/ISSCC42613.2021.9365807.

[7] S. Mondal, O. Ghadami and D. A. Hall, "10.2 A 139 µ W 104.8dB-DR 24kHz-BW CT ΔΣM with Chopped AC-Coupled OTA-Stacking and FIR DACs," *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, 2021, pp. 166-168

[8] M. Jang, C. Lee and Y. Chae, "9.2 a 134µw 24khz-bw 103.5db-dr ct ΔΣ modulator with chopped negative-r and tri-level fir dac," *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2020, pp. 1-3

[9] C. Y. Lee and U. -K. Moon, "A 0.0375mm^2 203.5µW 108.8dB DR DT Single-Loop DSM Audio ADC Using a Single-Ended Ring-Amplifier-Based Integrator in 180nm CMOS," *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, 2022, pp. 412-41