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A 40-nm CMOS Complex Permittivity Sensing Pixel for Material Characterization at Microwave Frequencies

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Abstract—A compact sensing pixel for the determination of the localized complex permittivity at microwave frequencies is proposed. Implemented in 40-nm CMOS, the architecture comprises a square patch, interfaced to the material-under-test (MUT) sample, that provides permittivity-dependent admittance. The patch admittance is read out by embedding the patch in a double-balanced, RF-driven Wheatstone bridge. The bridge is cascaded by a linear, low-IF switching down-conversion mixer, and is driven by a square wave that allows simultaneous characterization of multiple harmonics, thus increasing measurement speed and extending the frequency range of operation. In order to allow complex permittivity measurement, a calibration procedure has been developed for the sensor. Measurement results of liquids show good agreement with theoretical values and the measured relative permittivity resolution is better than 0.3 over a 0.1–10 GHz range. The proposed implementation features a measurement speed of 1 ms and occupies an active area of $0.15 \times 0.3 \text{ mm}^2$, allowing for future compact arrays of multiple sensors that facilitate 2-D dielectric imaging based on permittivity contrast.

Index Terms—bridge circuits, biomedical sensors, complex permittivity measurement, integrated microwave circuits, microwave sensors

I. INTRODUCTION

BROADBAND dielectric spectroscopy at microwave frequencies has been identified as a promising tool for a large number of applications, ranging from the agricultural, food and automotive industry to the biomedical domain [1]–[8]. This method relies on the fact that the dielectric footprint of various materials of interest, i.e. their complex permittivity across frequency, varies in conjunction with a parameter that needs to be detected or quantified.

To highlight a few examples, in agriculture, the complex permittivity of fruits and vegetables has been correlated to changes in temperature, water and inorganic material content [1]–[3], while in the automotive industry, it is the preferred method for oil and fuel quality inspection [4], [5]. On the biomedical side of the application spectrum, examples include blood glucose monitoring [6] and *ex-vivo* or *in-vivo* cancer detection and assessment [8], [9]. The latter application is supported by measurements on bulk animal and human tissue, suggesting that the permittivity of cancer tissue can vary by up to 20% compared to healthy tissue [10], [11].

Despite the promising potential suggested by these studies, conventional microwave permittivity measurement techniques, used to acquire the aforementioned literature data, employ expensive and bulky equipment such as vector network analyzers (VNAs) and probe or cavity sensors interfaced to the material-under-test (MUT) [12], [13]. These setups are not suitable for most practical application scenarios, such as outdoor, remote-location measurements, and point-of-care medical testing. Moreover, their high cost hinders potential wider adoption of the technology.

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Miniaturization of sensors and measurement systems is, therefore, essential in order to leverage the true potential of microwave permittivity sensing in real-life applications. Moreover, miniaturized sensors can facilitate new applications that deviate from the bulk-level measurement regime, such as the unexplored area of 2-D sensor arrays for permittivity contrast measurement and visualization at microwave frequencies. Such imaging functionality can prove useful in a variety of applications such as:

- (a) label-free, *in-vivo* cancer visualization as an assisting tool in removal surgery [14],
- (b) food and flower quality inspection for early detection of storage disorders (e.g. browning, skin spots, etc),
- (c) evaluation of drug penetration through the skin,
- (d) non-destructive film coating testing in industry.

A differentiation should be made at this point between microwave permittivity sensors and low-frequency permittivity/impedance sensors, operating below 100 MHz. For the latter, arrayed implementations have already been implemented successfully [15], [16]. Nevertheless, motivation to move towards broadband microwave frequency implementations still exists for two main reasons: i) in order to achieve better penetration in the material-under-test (MUT) and ii) to employ the higher redundancy implicit in acquiring a permittivity dataset which is more complete and flexible in the frequency domain. Such redundancy is directly linked to increased sensitivity and specificity in biomedical applications.

To enable such imaging systems, focus has to be put on a fast readout, with acceptable resolution to fulfill the application requirement, as well as the overall size of the sensor and its signal conditioning circuitry, since this will determine its scalability in a dense array towards a fine spatial resolution. Efforts towards miniaturization of microwave permittivity sensing systems have been mainly concentrated towards CMOS implementations because of the ultimate form factor that CMOS offers. Several microwave CMOS implementations during the last years have demonstrated accurate permittivity readout [17]–[24]. Oscillator-based approaches exist, which are very narrow-band, area-consuming and limited to measurement of the real part of permittivity, thus are not suitable for implementation of a broadband permittivity sensing pixel [17], [19], [22], [24]. Several other implementations achieve an operation frequency range of at least a decade by employing broadband down-conversion [18], [20], [21], [23] or wide-band PLL-based architectures [22]. However, since they are not meant for imaging applications, little optimization and analysis has been done on the readout speed, resulting in potentially long measurement times. Moreover, the active area still remains quite large if implementation of a sub-mm-resolution imager is targeted.

In the following sections, we detail an integrated complex permittivity sensor, suitable for use as an imaging pixel, which was prototyped in 40-nm CMOS and occupies sub- mm^2 area while achieving fast readout. The proposed sensor, briefly presented in [25], features a single-ended patch sensing element, embedded in a fully-differential double-balanced RF-driven impedance bridge. A multi-harmonic measurement scheme is employed to extend the

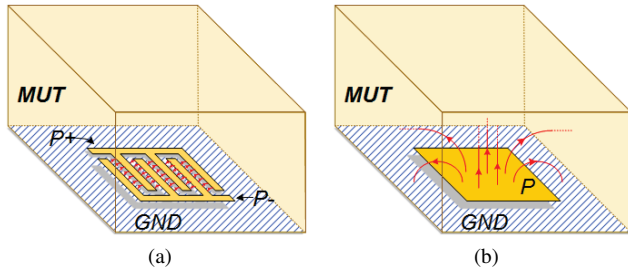


Fig. 1. 3D depiction of (a) a differential and (b) a single-ended patch sensing element.

frequency range and increase the effective measurement speed. In this work, we analyze the utilized sensing element in depth, and develop a calibration procedure, based on the analysis of the RF bridge. Moreover, the noise sources that contribute to the system resolution limit are identified and their contribution is quantified. Additional measurement data are complementing the preliminary results reported in [25] that demonstrated the ability to measure material complex permittivity. Independent measurements with the sensing pixel loaded by a probe that offers a known termination are used to validate the bridge transfer characteristic, while statistical data of material measurements have been collected to evaluate the permittivity resolution of the sensor when fundamental, third and fifth harmonic are measured.

The paper is organized as follows; section II analyzes the basic principles behind the system architecture, including the near-field patch sensor, the RF impedance bridge it is embedded in, as well as the multi-harmonic IF down-conversion read-out concept. Section III describes the physical implementation of the permittivity-sensing system in a 40-nm CMOS technology. In section IV, a calibration procedure for the developed sensor is given and the resulting accuracy and resolution are discussed. Experimental results are presented in section V. Finally, conclusions are drawn in section VI.

II. SYSTEM ARCHITECTURE

To address the aforementioned application scenarios, it is desirable that the sensor features the following qualities:

- Broadband operation that allows flexibility in choice of frequency.
- Complex material permittivity detection, i.e. ability to detect both real and imaginary part of the permittivity.
- Suitability for embedding in a 2-D array for permittivity contrast imaging, implying small size and fast read-out.

The proposed architecture consists of a near-field patch sensor, an RF-driven impedance bridge in a double-balanced configuration and a multi-harmonic, IF down-conversion scheme.

A. Near-Field Sensor

The sensing element translates the relative permittivity of the material, expressed as a frequency-dependent complex number $\epsilon^*(\omega) = \epsilon'(\omega) - j\epsilon''(\omega)$, into a lumped equivalent complex admittance that can be read out by subsequent circuitry.

Previously reported CMOS permittivity sensors typically employ differential capacitive sensing elements, similar to the one depicted in Fig. 1a, implemented on the top metal of the CMOS metal stack, with a passivation opening for direct contact to the MUT [17], [19]–[22]. These sensor types provide convenient access to both terminals ($P+$ and $P-$ in Fig. 1a) and are directly compatible with fully differential read-out chains. However, due to their planar configuration, the

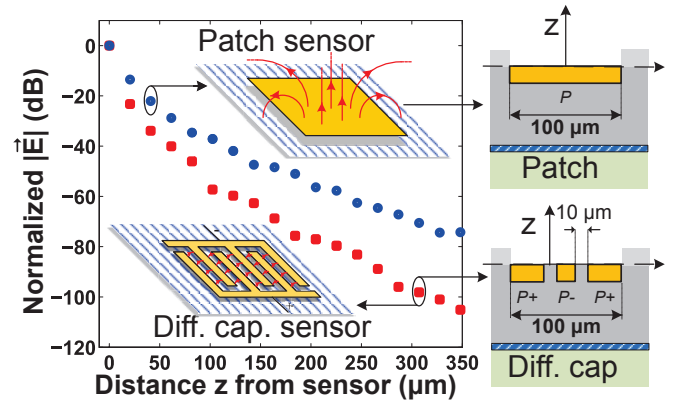


Fig. 2. EM simulation of normalized electric field magnitude versus vertical distance from the sensor interface for two types of sensors both occupying the same $100 \times 100 \mu\text{m}^2$ area: a single-ended patch and a differential capacitor with $10 \mu\text{m}$ between fingers.

electric field is mainly concentrated in the vicinity of the sensor surface, i.e. the surface-MUT interface. On the contrary, the electric field lines of a single-ended metal patch sensor, portrayed in Fig. 1b, penetrate deeper in the MUT, thus allowing sensing further from the sensor-MUT interface.

To demonstrate this, EM simulations were carried out to determine the electric field as a function of vertical distance from the sensor surface, using a commercial 3D EM simulation tool (Keysight EMPro). The two simulated sensors occupy an area of $100 \times 100 \mu\text{m}^2$ and a distance of $10 \mu\text{m}$ between fingers was chosen for the differential sensor. A typical 40-nm CMOS metal stack was considered and the EM simulation was carried out at 1 GHz, in a worst case scenario where the sensor is interfaced to air ($\epsilon^* = 1 - j0$). As seen in the simulation results in Fig. 2, a much steeper decay of the electric field is evident in the case of the differential sensor. At a distance of $300 \mu\text{m}$, the electric field magnitude is approximately 100 dB lower than the maximum strength, whereas for the patch sensor this reduction is in the order of 70 dB, a difference of 30 dB.

A patch sensor is, therefore, less sensitive to potential air-gaps, since a smaller portion of the field is concentrated at the interface. This property is desired in solid or semi-rigid material measurements (e.g. biological tissue), but also in applications when a permittivity contrast measurement deeper in the MUT is targeted. Although the patch sensor is expected to provide a poorer isolation to neighboring pixels, the fact that it is not inherently bound to differential sensing also allows the use of more advanced driving schemes where multiple patches are used to inspect a sample. Examples of such schemes include multi-phase patch excitation, selective differential sensing between different sensors and bootstrapping, i.e. driving neighboring pixels without reading them in order to cancel capacitive cross-coupling [26]. Based on the above, the patch configuration was favoured as a sensing element in this implementation.

Fig. 3a shows the cross-section of the a square patch sensor implemented on the top metal of a generic CMOS stack. When the patch is in contact with air the patch node P is loaded by the parallel-plate capacitance C_0 , formed between the top metal and the ground plane. When interfaced to a MUT, the load will change depending on the MUT complex permittivity. Since permittivity relates to electric energy storage and loss (ϵ' and ϵ'' respectively), the sensing element is expected to represent a lossy capacitor of which the reactive and resistive behavior will strongly depend on the real and imaginary part of the MUT permittivity, respectively. Hence, the admittance Y_P at the

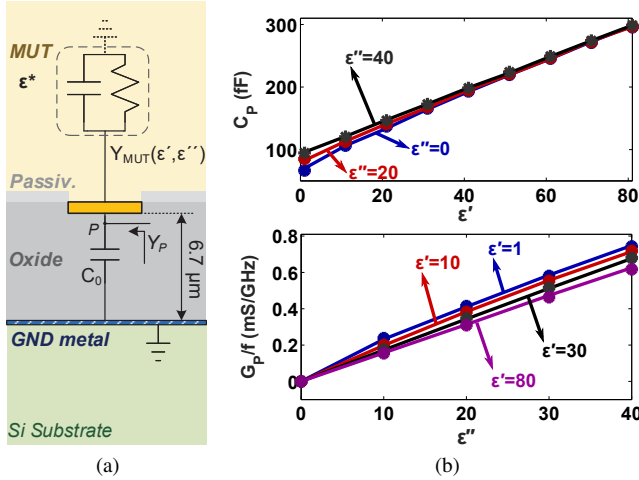


Fig. 3. (a) Cross section of utilized patch sensing element and (b) equivalent patch capacitance and conductance from EM simulations (solid lines) and RFM model (dots) for various values of ϵ' and ϵ'' at $f = 1$ GHz.

TABLE I
PARAMETERS OF LINEAR ϵ -TO-Y MODEL

Parameter	Value
C_0	82.56 fF
α_r	2.745 fF ⁻¹
α_i	17.5 μ S ⁻¹ · GHz ⁻¹

patch node can be expressed as a parallel combination of a material-dependent admittance $Y_{MUT} \approx G_{MUT}(\epsilon'') + j\omega C_{MUT}(\epsilon')$ and the baseline admittance $Y_0 = j\omega C_0$, yielding $Y_P = Y_0 + Y_{MUT}$.

In order to quantify the permittivity-to-admittance behavior of the patch, a 3D model of a 100×100 - μm^2 patch on a realistic representation of the available 40-nm CMOS stack, in direct contact with a MUT, was simulated versus varying ϵ' and ϵ'' . The solid lines in Fig. 3b show the capacitance and conductance of node P versus ϵ' and ϵ'' , for different values of ϵ'' and ϵ' , respectively, at a simulation frequency of 1 GHz. An explicit relation of capacitance to ϵ' and conductance to ϵ'' exists that can be linearly approximated by

$$Y_P(\epsilon', \epsilon'', \omega) \approx \alpha_i \cdot \omega \cdot \epsilon'' + j\omega \cdot (C_0 + \alpha_r \epsilon'), \quad (1)$$

where α_r and α_i are real parameters. Note that the ω contribution in the real part of the admittance results from the fact that conductivity of the material is given by $\sigma = \omega \epsilon''$ [27]. Table I summarizes the parameters of the model in (1) extracted after least square fitting with the EM-simulated curves.

Although the linear model is simple, intuitive and useful for preliminary analysis, it is clear from the simulated results of Fig. 3b that G_{MUT} and C_{MUT} also vary with ϵ'' and ϵ' , respectively, an effect not captured by (1). For the purpose of calibration, a rational function model (RFM), fitted from EM simulations, can be used to arrive to an analytical model, a methodology widely used in permittivity measurements performed with open-ended coaxial probes [13], [28], [29]:

$$Y_P(\epsilon^*, \omega) \approx j\omega C_0 + \frac{\sum_{n=1}^N \sum_{p=1}^P \alpha_{np} (\sqrt{\epsilon^*})^p (j\omega a)^n}{1 + \sum_{m=1}^M \sum_{q=1}^Q \beta_{mq} (\sqrt{\epsilon^*})^q (j\omega a)^m}, \quad (2)$$

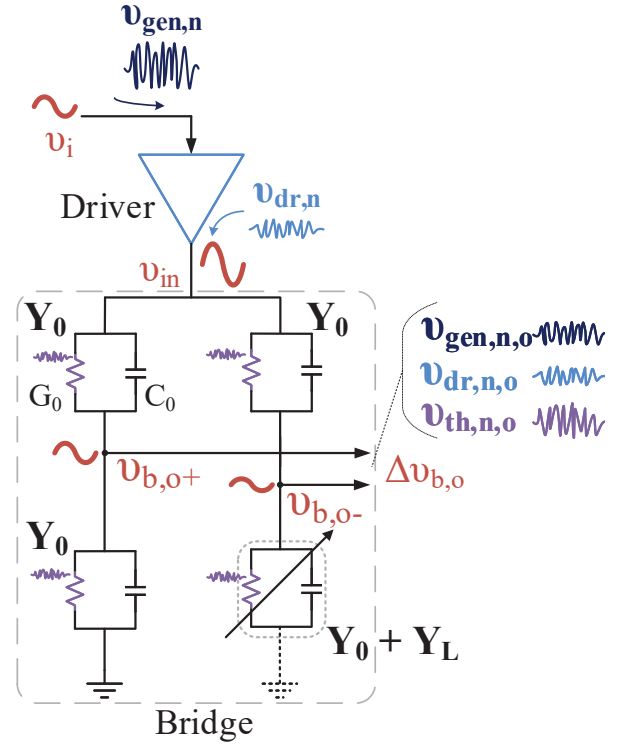


Fig. 4. Balanced impedance bridge, driven at RF frequency by a driver, with annotated signals and noise sources contributing to the total noise at the output of the bridge.

where a is a scaling parameter, set equal to the patch dimension, and α_{np}, β_{mq} are $N \times P$ and $M \times Q$ real model parameters, respectively. In order to find the parameters, eq. (2) is fitted with parametric EM simulations across ϵ' , ϵ'' and frequency. A fitted model with $N = P = M = Q = 4$ is deemed sufficient since it already achieves 1% maximum deviation from simulations over a 0.1-10 GHz frequency range.

B. RF Impedance Bridge

Following the established analytical ϵ -to-Y model for the patch, a method of reading out the admittance is required. A Wheatstone bridge [30], [31] is a widely adopted method of measuring or sensing electrical impedance since it offers a quantification of impedance variation relative to a constant baseline value, such as C_0 in the case of the patch sensor. At RF frequencies, impedance bridges have been widely used in broadband vector network analysis as directional detection elements, as an alternative or complementary to bi-directional couplers [32].

In this subsection, an alternative analysis of the AC-driven Wheatstone bridge with complex branch loads is presented. A mathematical manipulation of the bridge equation is performed to extract useful information for the calibration of the sensor. This analysis is later verified by measurements of various known RF impedances in a probed measurement environment. Moreover, the bridge output noise is calculated to extract information about the minimum detection limit.

1) *Bridge Analysis*: Consider the RF impedance bridge shown in Fig. 4 with branch admittances Y_0 and the load measurand Y_L deviating from a baseline admittance Y_0 . The bridge is excited at a given frequency ω with a signal of amplitude v_{in} , through bridge driver that amplifies a signal v_i of the same frequency. The differential

output voltage of the bridge can be found after straightforward circuit analysis:

$$\Delta v_{b,o} = v_{b,o+} - v_{b,o-} = v_{in} \cdot \frac{Y_L}{4Y_0 + 2Y_L}, \quad (3)$$

where $Y_L = G_L + jB_L$ and $Y_0 = G_0 + jB_0$ are the generic complex representation of the admittances. A common approximation is that, for small variations of the measured load admittance, i.e. $G_L \ll G_0$ and $B_L \ll B_0$, equation (3) denotes that the output varies linearly with the measured load admittance:

$$\Delta v_{b,o} \approx v_{in} \cdot \frac{Y_L}{4Y_0} \quad (4)$$

This approximation, however, can result in large errors in the estimation of Y_L . A more generic result that accounts for any value of measured load is possible, irrespective of how much it unbalances the bridge and without requiring any approximations. Indeed, assuming that $Y_L \neq 0$, inverting (3) results in

$$\frac{1}{\Delta v_{b,o}} = \frac{1}{v_{in}} \left(2 + \frac{4Y_0}{Y_L} \right). \quad (5)$$

Substituting for Y_0 and Y_L yields

$$\Re \left\{ \frac{1}{\Delta v_{b,o}} \right\} = \frac{1}{v_{in}} (2 + 4G_0 \cdot G_{Lw} + 4B_0 \cdot B_{Lw}) \quad (6)$$

and

$$\Im \left\{ \frac{1}{\Delta v_{b,o}} \right\} = \frac{4}{v_{in}} (B_0 \cdot G_{Lw} - G_0 \cdot B_{Lw}), \quad (7)$$

where $G_{Lw} := G_L/|Y_L|^2$ and $B_{Lw} := B_L/|Y_L|^2$ are defined as the weighted load conductance and susceptance values, respectively.

Therefore, irrespective of deviation of Y_L from Y_0 , the real and imaginary part of the inverse bridge differential output are linear combinations of the weighted load conductance and susceptance. Formulating the bridge behavior as in (6) and (7) allows to present a linear relation between an output quantity (inverse of output) to the input quantity (weighted conductance and susceptance). In this manner, an intuitive calibration procedure can be obtained that is closer to the bridge operation, rather than utilizing high-order polynomial fitting [18], [20], [21]. The calibration procedure is described in detail in section IV-A.

2) *Bridge Noise*: In order to calculate the noise at the output of the bridge, we can break it down into three uncorrelated components shown in Fig. 4: thermal noise generated by the bridge resistive elements ($v_{th,n}$), flicker, shot and thermal noise generated by any internal active elements driving the bridge ($v_{dr,n}$), and input noise to the bridge driver originating from the RF signal generator, either external or internal ($v_{gen,n}$). By applying superposition, the contribution of each component to the output noise can be analyzed. The total noise is thus the mean-square sum of these three components: $\overline{v_{n,o}^2} = \overline{v_{th,n,o}^2} + \overline{v_{dr,n,o}^2} + \overline{v_{gen,n,o}^2}$.

The thermal noise power at the differential output of the bridge is given by

$$\begin{aligned} \overline{v_{th,n,o}^2} &= 4kT \int_{\omega-\Delta\omega/2}^{\omega+\Delta\omega/2} \Re \left(\frac{1}{4Y_0 + Y_L} \right) \cdot d\omega \quad (8) \\ &= 4kT \int_{\omega-\Delta\omega/2}^{\omega+\Delta\omega/2} \frac{4G_0 + G_L}{(4G_0 + G_L)^2 + (4B_0 + B_L)^2} \cdot d\omega, \quad (9) \end{aligned}$$

where $\Delta\omega$ is the observation bandwidth. Since the complex permittivity is translated to conductance and capacitance, the bridge susceptance will essentially be that of a capacitance, i.e. $B = \omega C$. In addition, the observation bandwidth is typically much smaller than

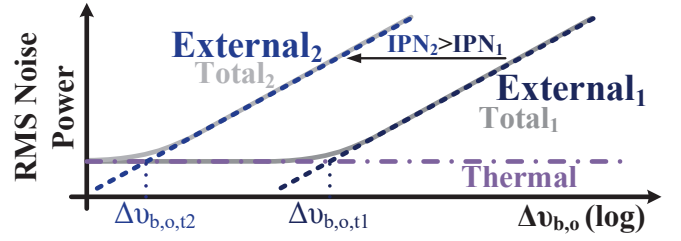


Fig. 5. Thermal and external noise contributions to the bridge output noise versus bridge differential output voltage for different level of integrated phase noise of the external source.

the frequency of interest ($\Delta\omega \ll \omega$) and thus we can safely neglect the frequency variation of the integrated quantity:

$$\overline{v_{th,n,o}^2} \approx 4kT \left(\frac{4G_0 + G_L}{(4G_0 + G_L)^2 + \omega^2(4C_0 + C_L)^2} \right) \Delta\omega. \quad (10)$$

As will be analyzed in section III-C, a clipping buffer is used as the bridge driver. Assuming a quiet power supply, the contribution of noise from the bridge driver is in the form of cyclo-stationary phase-modulated (PM) noise that results from up-conversion of thermal and flicker noise to the frequency of operation [33]. This noise will be scaled by the bridge similarly to the bridge drive signal v_{in} and can, therefore, be expressed as a function of the single-side-band (SSB) phase noise of the driver, L_{dr} , and the differential output ($\Delta v_{b,o}$) of the bridge:

$$\overline{v_{dr,n,o}^2} = 2 \int_0^{\Delta\omega} 10^{L_{dr}(\omega)/10} \cdot \Delta v_{b,o}^2 \cdot d\omega = IPN_{dr} \cdot \Delta v_{b,o}^2, \quad (11)$$

where IPN_{dr} is the integrated phase noise of the driver up to the measurement bandwidth $\Delta\omega$. Similarly for the external generator noise, any amplitude-modulated (AM) component is suppressed by the buffer, but the PM noise will be propagated to the bridge through a phase noise transfer of unity, since any timing variation in the input of the switching buffer will be transferred directly to its output. As a consequence, the contribution of the generator noise to the output of the bridge can be expressed, identically to (11), as

$$\overline{v_{gen,n,o}^2} = IPN_{gen} \cdot \Delta v_{b,o}^2, \quad (12)$$

where IPN_{gen} is the double sideband (DSB) integrated phase noise of the generator within the measurement bandwidth $\Delta\omega$.

Notice from (11) and (12) that the noise components related to the bridge drive are proportional to the output power, which suggests that the more balanced the bridge is, the less the external noise contribution to the output. These contributions can be grouped together into what we can call external noise contributions. Fig. 5 shows how the two noise contributions (thermal and external) will vary versus the bridge output voltage. The total noise power, being the mean-square sum of the two, is dominated by the external sources when the bridge is unbalanced and is limited by the thermal noise level when the bridge is close to balanced state. The transition point between the two dominant noise regimes is denoted as $\Delta v_{b,o,t}$ in Fig. 5 and is closer to the balanced state for an external source with higher IPN.

In practice, the total noise is in many cases dominated by the external sources since the phase noise levels of buffers and generators are much higher than the thermal noise level of the bridge, even for small bridge output voltages. As an example, consider a realistic case of the RF bridge as in Fig. 4, with $G = 1 \text{ mS}$, $C = 100 \text{ fF}$, $G_L = 0.01 \text{ mS}$ and $C_L = 1 \text{ fF}$ (1% imbalance), driven at 1 GHz ($\omega = 2\pi \cdot 1 \text{ G} \cdot \text{rad/s}$) with an amplitude of $v_{in} = 1 \text{ V}$ and read out at an observation time of 1 ms

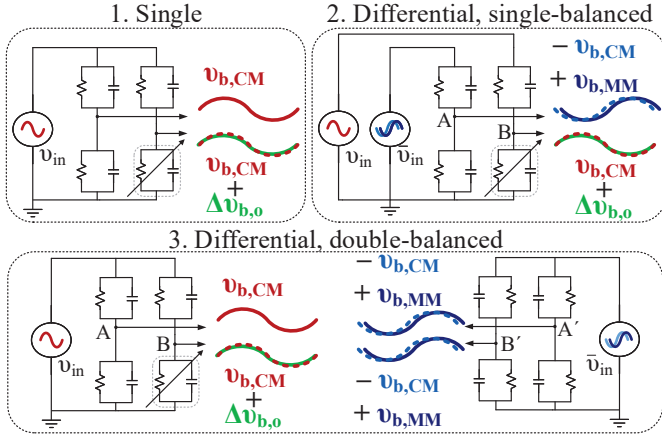


Fig. 6. Evolution of single-driven, single-ended impedance bridge towards a fully-differential, double-balanced topology. $v_{b,CM}$ denotes for common-mode signal, while $v_{b,MM}$ is the signal caused by the phase mismatch between the two out-of-phase driving sinusoids.

($\Delta\omega = 2\pi \cdot 1 \text{ k} \cdot \text{rad/s}$). According to (3) and (10), the signal output of the bridge is $\Delta v_{b,o} = 2.5 \text{ mV}$ and the thermal noise power at the output is $v_{th,n,o}^2 = 1.489 \cdot 10^{-15} \text{ V}^2$. For an external source (driver or generator) to contribute the same level of noise at the bridge output, a required integrated phase noise of -85.2 dBc is calculated from (11) or (12), which corresponds roughly to a SSB phase noise of -118 dBc/Hz over all frequency offsets below 1 kHz . This performance is at the boundary of what is achievable by state-of-the-art frequency synthesizers at this frequency of operation [34], [35].

3) *Double-Balanced, Fully-Differential Bridge*: The single RF impedance bridge of Fig. 4, analyzed till this point, suffers from a large common-mode signal at its output. In order to achieve the highest sensitivity to load changes, equation (3) suggests that the drive amplitude voltage $|v_{in}|$ should be maximized. In a CMOS implementation, where the bridge is actively driven by MOS transistors, this maximum amplitude is in the order of the nominal supply (VDD). Moreover, the highest sensitivity is achieved when all branch nominal admittances are equal (Y_0). Under these assumptions, the worst-case common mode-signal $v_{b,CM}$ at the differential output of the bridge is half the supply voltage (peak-to-peak), on top of a useful differential signal $\Delta v_{b,o}$, orders of magnitude smaller, as illustrated in the single-driven topology of Fig. 6a. Such a large common mode voltage poses a stringent requirement to the common-mode rejection ratio (CMRR) of the read-out chain and compromises the linearity of the active circuitry following the bridge.

An anti-phase drive of each branch of the bridge, as shown in Fig. 6b, can mitigate this problem since the baseline signals, having a phase difference of 180° , will cancel out when combined at the output of the bridge, preferably capacitively to additionally achieve DC blocking. However, this results in a single-ended output of the bridge and the benefits of a fully differential read-out chain cannot be employed. Moreover, if the two drive signals are not exactly 180° out-of-phase, a phase mismatch signal ($v_{b,MM}$) will appear in the output of the bridge. This cannot be treated as a constant offset when this phase mismatch is load-dependent due to limited driving capability of the bridge driver.

A double-balanced configuration, depicted in Fig. 6c, uses an anti-phase driven copy of the bridge (without the load connection). Capacitively combining the four bridge nodes (A to A' and B to B', respectively) results in a differential output. Additionally, any signal caused by phase mismatch of the bridge drive turns into a common-

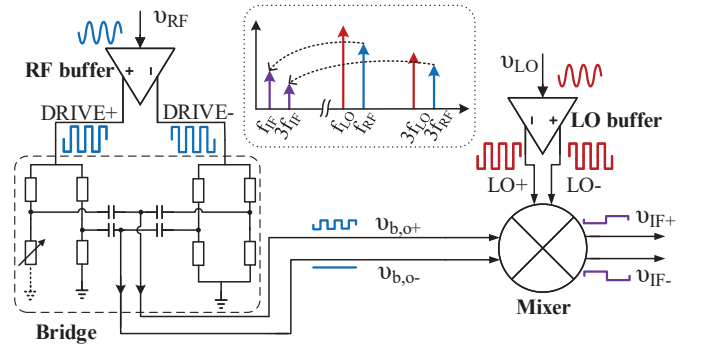


Fig. 7. Block-level diagram of the multi-harmonic IF down-conversion architecture with annotated signals and their frequency-domain representation (insert).

mode signal, which is much smaller than $VDD/2$ and can easily be rejected in a fully-differential chain. Nevertheless, using a double-balanced bridge configuration instead of a single one, comes at the price of doubling both the area and the noise power as well as an increased power consumption needed for driving the bridge because the loading of the drivers is increased.

C. Multi-Harmonic Down-Conversion

The RF output of the bridge needs to be down-converted from the characterization frequency f_{RF} to a convenient intermediate frequency in order to be digitized and further analyzed. To achieve this, the bridge is connected to a down-conversion mixer, as shown in Fig. 7, in which the output signal of the bridge is mixed with an LO signal at f_{LO} , generating an output signal Δv_{IF} , which is an exact replica of $\Delta v_{b,o}$ at $f_{IF} \ll f_{RF}$, assuming a perfectly linear mixing operation.

A switching mixer with square-wave LO drive is preferred as it can achieve a higher conversion efficiency than a small-signal equivalent [36], [37]. As a result, the LO signal also contains odd higher-order harmonics of the fundamental f_{LO} . At the same time, it is convenient to apply a square drive to the bridge, in order to maximize its drive amplitude (signals DRIVE+ and DRIVE- in Fig. 7). Therefore, the bridge is driven at multiple odd harmonics which will be down-converted to odd harmonics of f_{IF} , after being mixed with the odd harmonics of LO, as shown in Fig. 7. Situated $2f_{IF}$ apart, these harmonics can be isolated and analyzed, enabling characterization of the load at higher frequencies than the highest achieved by the fundamental drive, and at more than one frequency point at the same time.

Since the amplitude of the higher-order odd harmonics in the square wave reduces by at least $1/n$ compared to the fundamental, where n the harmonic, order a lower sensitivity is expected at these higher harmonics. Nevertheless, useful information can still be acquired, contributing to the previously mentioned goal of redundancy. In addition to the baseband products of the mixing process, cross-mixing can create content close to the even harmonics of f_{RF} (e.g. $3f_{RF} - f_{LO}$). Careful design of the mixer and LO signal is required to minimize self-mixing with the odd harmonics of LO, which will fall within the useful signal frequency f_{IF} . In general, a fully-differential chain with layout matching techniques can minimize second-order harmonic content and non-linearities.

III. CIRCUIT DESIGN

In this section, we discuss the specific implementation and integrated circuit design of the permittivity sensor based on the previously

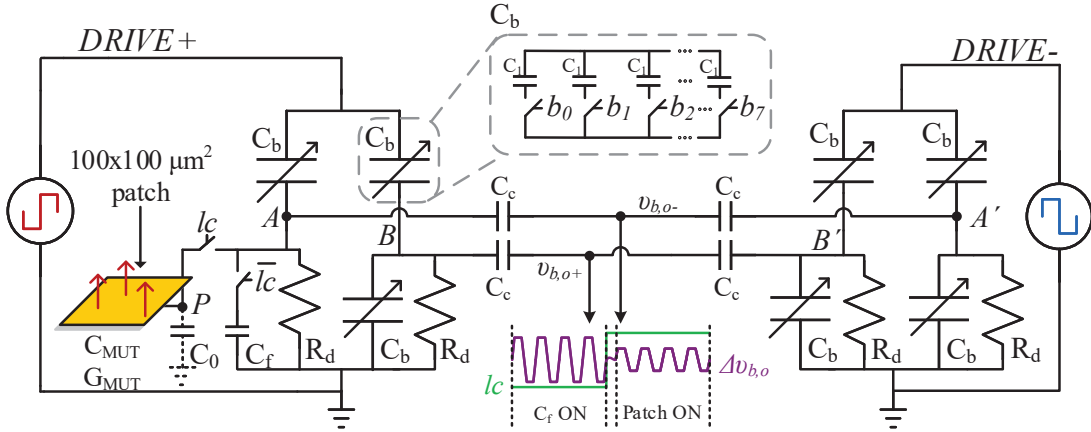


Fig. 8. Schematic of the implemented fully-differential, double-balanced bridge and 3D view of patch implementation on two top metals of the 40-nm CMOS technology.

reported architecture. The three circuit blocks comprising the sensor is the RF bridge, the down-conversion mixer, and the bridge and LO drivers that provide the square wave for multi-harmonic operation.

A. Double-balanced, Fully-Differential Bridge Design

The implemented sensing element is a square $100 \times 100 \mu\text{m}^2$ -patch implemented in the top ultra-thick metal of the CMOS stack (M7), with a nitride opening for direct interfacing with a MUT or used for probing. The patch also utilizes patterned thick metal layer (M6) connected to ultra-thick through a large via, respecting all stress-related DRC rules for probing. This structure is EM-simulated in order to generate the RFM model of Fig. 3b, discussed in II-A, which is later used for calibration of the system.

Fig. 8 shows the schematic of the implemented bridge in which the sensor patch is embedded, implementing the fully differential, double balanced architecture discussed in II-B3 with some additions for reconfigurability and practical considerations that will be discussed further.

As seen in Fig. 8, the main part of the branch admittance is a capacitor C_b . In order to accommodate wide capacitive load variations and experimentally investigate the behavior of the bridge at various imbalanced states, C_b is implemented as a parallel combination of eight switchable capacitors. Each of these comprises a capacitor C_1 of roughly 100 fF , in series with a $10 \mu\text{m}/40 \text{ nm}$ CMOS switch. The capacitor bank is controlled by a unitary weighted 8-bit digital signal b .

Due to the finite quality factor of the capacitor and the equivalent on/off resistance of the switch, we can model the switched capacitor as an equivalent conductance in parallel with a capacitance, with varying values versus frequency during the on and off state. Fig. 9 shows the simulated on/off parallel conductance and capacitance versus frequency for the switched capacitor (post-layout extraction). The simulated on-capacitance and conductance vary versus frequency from 130 fF to 100 fF and from 0.01 mS/GHz to 0.2 mS/GHz , respectively, while the off-capacitance and conductance are between 30 fF to 12 fF and 0.01 mS/GHz to 0.06 mS/GHz , respectively. At each frequency, the total branch capacitance and admittance depends on the number of on capacitors, determined by the value of b as: $Y_b = b \times Y_{on} + (8 - b) \times Y_{off}$. A proper value of b can be used to bring the branch admittance to a value such that the balanced state falls close to the range of loads measured. For example, for the permittivity range of simulations in Fig. 3b, we expect a load variation of $60 - 300 \text{ fF}$ and $0 - 0.8 \text{ mS/GHz}$ for patch capacitance and

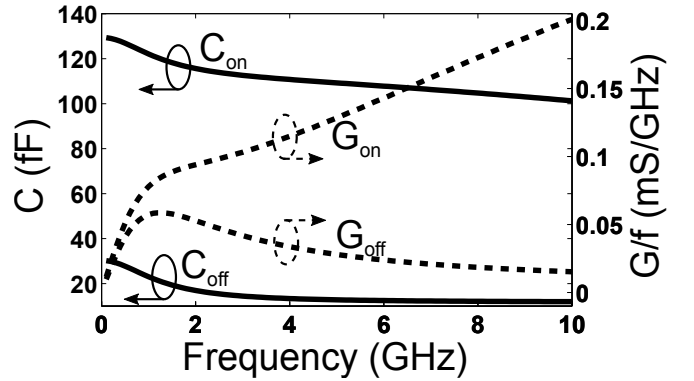


Fig. 9. Equivalent parallel capacitance and conductance of switched capacitor at on and off stage.

conductance, respectively. A value of b between 0 and 3 can fall within this range.

An $1.2\text{-k}\Omega$ discharge resistor R_d is placed between the bridge middle nodes (A , A' , B , B') and ground in order to ensure a DC discharge path that sets the DC bias condition for the proper operation of the NMOS switches. The value of the resistor is a trade-off between size consideration and minimum voltage drop due to bridge loading. Similarly, the four 25-fF combining capacitors C_c are of the same order of magnitude as the input capacitance of the mixer, for optimum voltage division.

As suggested by (3), the output of the bridge is proportional to the amplitude of the drive signal v_{in} . Since this value depends on the supply voltage, it is desirable to decouple the system output from the bridge drive amplitude. In addition, in order to gain information of both capacitance and conductance, we need to acquire both the real and imaginary part of the bridge output. Therefore, an amplitude and phase measurement of the bridge output is required. For the phase measurement to be consistent, a reference phase also needs to be measured. This is required in order to determine the relative phase variation at the output of the bridge, caused only by the patch load variation.

A relative amplitude and phase measurement can be achieved without the introduction of any additional active circuitry, by disconnecting the bridge from the patch and connecting it to a fixed on-chip capacitance $C_f \approx 100 \text{ fF}$, during a continuous-time measurement,

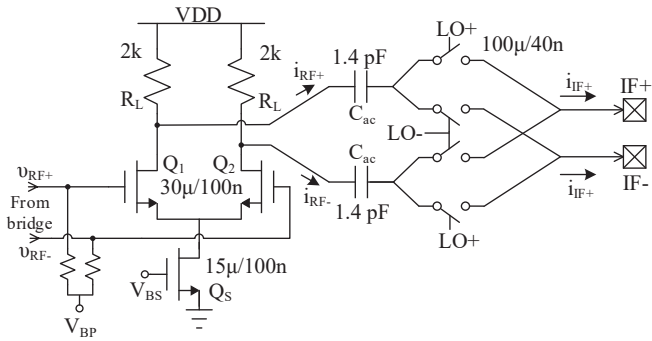


Fig. 10. Current-mode down-conversion mixer schematic consisting of a transconductance stage and a current-mode switch quad.

through a series NMOS switch, as shown in Fig. 8. This switch operates in its linear region, because the discharge resistor R_d sets its DC bias point to zero and the maximum voltage swing across the switch (350 mV in the presence of resistor R_d and parasitics to ground) is well below the simulated 1-dB compression point of 760 mV below 5 GHz. A digital signal lc (see Fig. 8) that controls the connection of the bridge to either the patch sensor the fixed capacitor C_f , is used to acquire a continuous measurement trace containing the both outputs of the bridge during these two load-connection cases. The acquired signal is down-converted and digitized and the two separate outputs are isolated in the digital domain by synchronization to the control signal lc . The fast Fourier transform (FFT) of the two outputs is then calculated and divided in order to acquire a consistent relative phase difference and amplitude ratio, which only depend on the relation between the fixed and the measured load. Note, however, that this solution does not eliminate short-term variations of the bridge drive voltage that happen independently during the measurement of the two load-connection cases, as these variations are uncorrelated to each other.

B. Down-Conversion Mixer

Fig. 10 shows the schematic of the down-conversion mixer connected to the bridge to perform a frequency translation of the RF bridge output to IF. The topology implements a current-mode switching mixer that achieves low $1/f$ noise operation and high linearity [38]. The transistors Q_1 and Q_2 , along with resistors R_L , form a differential transconductance (g_m) stage. If the value of R_L is large enough, most of the drain current of the transistors will be transferred to the output, converting the bridge output voltage (v_{RF+} , v_{RF-}) to a differential current (i_{RF+} , i_{RF-}). The transistor Q_s sets the bias current, which is generally limited for two main reasons: a) the large resistor value limits headroom of Q_1 and Q_2 , which is required for good linearity and b) Q_s needs to be small in order to minimize its parasitic drain capacitance that deteriorates the common-mode rejection ratio and second-order non-linearity. On the contrary, a higher bias current results in a larger amplification and, hence, a better noise performance. As a trade-off, a bias current of 700 μ A was chosen to achieve a transistor g_m of 5 mA/V.

The output current of the g_m stage is fed to a CMOS switching quad that performs the mixing action. Capacitive coupling is used to prevent DC current through the CMOS switches, which is a source of flicker noise and non-linearity [38]. An optimum switch size can be found since a large size reduces the on-switch resistance (and thus the insertion loss) but increases the parasitic capacitance to ground and the loading to the LO driver. In order to convert the down-converted signal current back to voltage and perform digitization of the waveforms using an A/D converter (ADC), a low-noise external

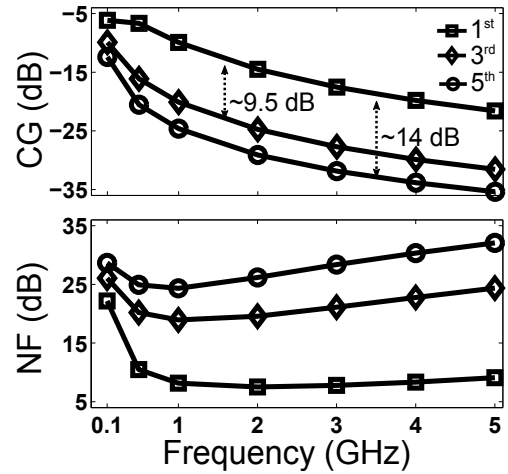


Fig. 11. Simulated conversion gain (top) and noise figure (bottom) versus of down-conversion mixer with an IF of 150 kHz for three LO harmonics.

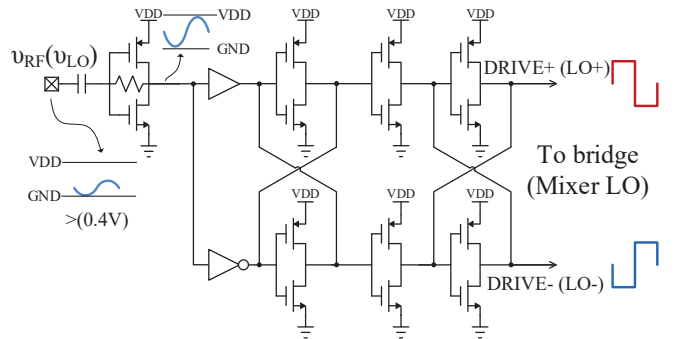


Fig. 12. Schematic of the bridge and mixer drivers.

transimpedance amplifier is used, which converts the current to voltage through a 10-k Ω resistance and amplifies this voltage with a variable 0-40 dB gain.

Fig. 11 shows the simulated conversion gain and noise figure of the mixer when terminated with an external 10-k Ω resistance and driven by an input port with impedance equal to that of the bridge. To investigate the multi-harmonic operation, the gain and noise of the LO third and fifth harmonic component are also simulated. Due to the $1/n$ reduction in the LO amplitude, the conversion gain of the third and fifth harmonic is expected to be 9.5 dB and 14 dB lower than the first harmonic, respectively. This trend is seen at frequencies above 1 GHz while below that the first and third harmonics experience a larger loss in the RF path due to the capacitive coupling at the bridge-mixer and g_m -quad connections. A 20-dB/dec gain roll-off is observed above 1 GHz. The noise figure is 7.5 dB at 2 GHz and stays below 10 dB in the GHz range. Below that, it increases rapidly to 22 dB because of the signal loss at the bridge output capacitor C_c . As expected, the noise figure of the third and fifth harmonic down-conversion process deteriorates by at least as much as the conversion gain deterioration.

C. Square-wave Drivers

The bridge and LO drivers share the same topology that utilizes inverter amplifiers to achieve a square-wave rail-to-rail output. Shown in Fig. 12, the driver consists of a self-biased inverter that sets the DC voltage of the input waveform to the desired mid-rail value by proper choice of the NMOS and PMOS size. Two complementary copies of the input are created and a series of increasingly larger

cross-coupled inverters further amplify the signal and ensure rise-fall edge alignment, thus minimizing phase imbalance. Optimization of the inverters' transistor size ratio allows to minimize rise-fall mismatch that creates a common-common mode voltage at the output of the bridge. In general, steeper edges (i.e. larger sized transistors and higher power consumption) minimize rise-fall mismatch across PVT variations. In fact, the simulated typical common-mode output on the bridge, caused by the driver at an 1.1-V supply, is 5 mV, while the worst-case (fast-n/slow-p, VDD=1V) was simulated to be 20 mV, which poses no risk for the linearity of the g_m stage, as would be the case with a large common mode caused by the use of a single bridge. Finally, the simulated integrated phase noise (IPN) of the bridge driver, which contributes to the bridge output noise, is between -92 dBc at 1 GHz and -81 dBc at 5 GHz, for an integration bandwidth of 0.01-1 kHz.

IV. SYSTEM CALIBRATION, ACCURACY AND RESOLUTION

A. Calibration

As discussed in II-B1 and summarized in (6) and (7), the real and imaginary part of the inverse bridge differential output are linear combinations of the weighted load conductance and susceptance. This result allows us to perform a linear fitting procedure for calibration. The benefit of such an approach is that it theoretically requires a minimum number of two known loads, if no systematic or random errors are induced by the calibration materials or measurement noise, although practically more points help average out such errors. In any case, a linear output expression alleviates any error induced from approximating (3) to a Taylor polynomial expansion of a certain order, bounded by the available number of calibration materials.

Equations (6) and (7) hold true with the assumption that the bridge is perfectly balanced to the baseline load admittance, i.e. in the middle of the measured load range. In practice, however, due to the asymmetric nature of the patch node (A in Fig. 8) to the rest of the bridge, and the finite quality factor of the switched branch capacitors, it is quite impractical to accurately ensure such a condition. A generic approach would be to assume that $Y_A = Y_b + Y_{off} + Y_L$, where $Y_{off} = G_{off} + j\omega C_{off}$ indicates how much load should be added at the patch node so that the bridge is balanced to the baseline load admittance. Being a fictional admittance, Y_{off} can assume both positive and negative values. The unbalance of the bridge can be defined as $\Delta Y = Y_{off} + Y_L$. Assuming a linear behavior of the circuitry following the bridge, we can use the result of (6) and (7) and formulate the calibration equations about the measured chip output quantity out :

$$\Re \left\{ \frac{1}{out} \right\} = K_R + K_{GR} \cdot \Delta G_w + K_{CR} \cdot \Delta C_w \quad (13)$$

and

$$\Im \left\{ \frac{1}{out} \right\} = K_I + K_{GI} \cdot \Delta G_w + K_{CI} \cdot \Delta C_w \quad (14)$$

where $\Delta G_w = \Delta G / |\Delta Y|^2$, $\Delta C_w = \Delta C / |\Delta Y|^2$ the unbalance weighted loads and $K_R, K_{GR}, K_{CR}, K_I, K_{GI}, K_{CI}$ are real valued numbers, further referred to as the K coefficients. A calibration operation would consist of the estimation these coefficients as well as Y_{off} . Provided they are available, the sensor load Y_L can be estimated by observing the respective chip output out_m . More specifically, by solving the system of (13) and (14) the measured weighted load values are acquired:

$$\Delta G_{w,m} = \frac{\hat{K}_{CI} \left(\Re \{1/out_m\} - \hat{K}_R \right) - \hat{K}_{CR} \left(\Im \{1/out_m\} - \hat{K}_I \right)}{\hat{K}_{CI} \hat{K}_{GR} - \hat{K}_{CR} \hat{K}_{GI}} \quad (15)$$

$$\Delta G_{w,m} = \frac{\hat{K}_{GI} \left(\Re \{1/out_m\} - \hat{K}_R \right) - \hat{K}_{GR} \left(\Im \{1/out_m\} - \hat{K}_I \right)}{\hat{K}_{CI} \hat{K}_{GR} - \hat{K}_{CR} \hat{K}_{GI}} \quad (16)$$

From the definition of the weighted loads we get

$$\Delta G_m = \frac{\Delta G_{w,m}}{\Delta G_{w,m}^2 + \omega^2 \Delta C_{w,m}^2} \quad (17)$$

and

$$\Delta C_m = \frac{\Delta C_{w,m}}{\Delta G_{w,m}^2 + \omega^2 \Delta C_{w,m}^2}. \quad (18)$$

from which, the measured load is calculated as $\hat{Y}_{L,m} = \Delta Y_m - \hat{Y}_{off}$.

Although approximate values of Y_{off} and the K coefficients can be estimated during the design process, their exact value remains unknown due to fabrication tolerances and modeling or simulation inaccuracies. In order to determine these values, a calibration procedure can be defined as follows:

- Measure the sensor output at a set of known load values $\mathbf{Y}_{L,cal}$
- Search for the combination of K coefficients and Y_{off} that achieve the best linear fit of $\Delta C_{L,m}$ and $\Delta G_{L,m}$ versus inverse output, according to (13) and (14), using the adjusted R^2 as a goodness-of-fit merit figure.
- Store the combination of Y_{off} and K coefficients corresponding as the calibration parameters of the chip.

Note that the calibration coefficients are frequency specific since both Y and Y_{off} are frequency dependent (see Fig. 9). Moreover, even with the presence of mismatch of the branch admittances of the bridge, the calibration procedure still holds, because there always exists a Y_{off} such that linear equations (13) and (14) still hold true. Therefore, minimizing mismatch during the design procedure is not a strict requirement, if Y_{off} is found through a search algorithm.

B. Accuracy and Resolution

A distinction should be made at this point between the accuracy and the resolution of the sensor. The accuracy of the permittivity measurement indicates its difference to the actual permittivity of the MUT and it is affected by temperature variation, accuracy of reference liquids and the accuracy of the assigned ϵ -to- Y transfer characteristic. Absolute accuracy is crucial for instrumentation applications, such as material characterization. In this work, we make use of tabulated permittivity values that originate from Debye models and that are accurate within 1% [39], [40]. Combined with the fact that no precise temperature is measured or imposed upon the MUT, the accuracy of the calibration procedure is expected to be at best within the same order.

For the intended application of imaging, which requires contrast detection, we are rather interested in the measurement resolution, which relates to the minimum detectable permittivity variation, and is directly linked to the noise levels at the output. Since the read-out of the real and imaginary part of the bridge output is done by measuring amplitude and phase, we need to link the resolution of the amplitude and phase read-out to the noise level, and, from that, assess the expected system resolution.

Let $v_{IF} = |v_{IF}| \cdot e^{-j\phi_{IF}}$ be the single-ended, amplified and digitized voltage output of the chip. Assuming that the A/D conversion quantization noise is far below the signal noise, we can relate the minimum variance bound of the amplitude and phase, acquired by the FFT of v_{IF} , to its signal-to-noise ratio (SNR), through the Cramér-Rao bound [41]:

$$\text{var} \{|\hat{v}_{IF}|\} \geq \frac{1}{\text{SNR}_{n,IF}^2}, \quad (19)$$

$$\text{var} \left\{ \hat{\phi}_{IF} \right\} \geq \frac{2\pi}{SNR_{IF}}, \quad (20)$$

where $v_{n,IF}^2$ is the noise at the system output. Using the definitions for SNR, $SNR_{IF} = \Delta v_{b,o}^2 / (F \cdot v_{n,bo}^2)$, and the conversion gain $CG = v_{IF} / \Delta v_{b,o}$, and using, as explained in II-B2, that $v_{n,bo}^2 = IPN \cdot \Delta v_{b,o}^2 + v_{th,n,o}^2$, we acquire

$$\text{var} \{ |\hat{v}_{IF}| \} \geq IPN \cdot F \cdot v_{IF}^2 + CG \cdot F \cdot v_{th,n,o}^2, \quad (21)$$

$$\text{var} \left\{ \frac{\hat{\phi}_{IF}}{2\pi} \right\} \geq IPN \cdot F + \frac{v_{th,n,o}^2}{\Delta v_{b,o}^2} \approx IPN \cdot F, \quad (22)$$

where $F = 10^{NF/10}$ the system noise factor. Since a ratiometric measurement is carried out by dividing two chip output voltages (the output due to the measured load and the fixed capacitor output), we can infer, by propagation of uncertainty calculations, that the variance of the measured ratio signal out is

$$\text{var} \{ |out| \} \geq 2 \cdot IPN \cdot F \cdot out^2 + 2 \cdot CG \cdot F \cdot v_{th,n,o}^2, \quad (23)$$

$$\text{var} \left\{ \frac{\hat{\phi}_{out}}{2\pi} \right\} \geq 2 \cdot IPN \cdot F. \quad (24)$$

As expected, a larger external integrated phase noise (IPN) and system noise factor (F) incurs a more noisy readout of both amplitude and phase. Moreover, an unbalanced bridge negatively affects only the variance of the signal amplitude while the phase stays, to a first order approximation, unaffected, and only depends on the input noise and the noise performance of the read-out circuitry.

The variance of the measured amplitude and phase propagates to the real and imaginary part and, through (6)-(7) and (1), to a variance of the load (G and C) and permittivity, respectively. We can thus come to the conclusion that the optimal permittivity resolution of both real and imaginary part occurs when the bridge is perfectly balanced to the measured admittance. Indeed, as derived in (3) and (4), a balanced bridge has the highest Y_L -to-output sensitivity (equal to $4Y_0/v_{in}$). Moreover, the measured output variance is also minimized to the thermal noise level at balance, as predicted from (23).

In order to evaluate the achievable permittivity resolution and confirm the optimum operating conditions, a perturbation analysis is carried-out on the equations that govern the designed system (eq. (3) multiplied by the system gain) using parameter values provided by the circuit-level simulations. A complex permittivity sweep is performed and the calculated output amplitude and phase of the chip is superimposed by the random noise predicted by (23) and (24), respectively. Then, the calibration procedure is performed to evaluate the standard deviation of the permittivity and, hence, the resolution. The result of this procedure is surfaces such as the ones in Fig. 13 for the simulated resolution of the real and imaginary part of permittivity. For the specific bridge capacitance setting of $b = 1$ (approx. 260 fF branch capacitance and $42 \mu\text{S}$ conductance) and frequency of $f = 1 \text{ GHz}$, there is a certain complex permittivity value that balances the bridge best, thus offering best resolution. As such, the complex permittivity resolution contains local minima at $\epsilon' \approx 20.5$ and $\epsilon'' \approx 19.5$.

Fig. 14 shows the simulated permittivity resolution versus MUT permittivity for various values of the branch capacitance setting b at 1 GHz. At this frequency, the best permittivity resolution is expected since the noise figure and external IPN of the used RF generator (Keysight E8257D) are minimum. By choosing the proper control value b an absolute permittivity resolution of < 0.05 can always be achieved. However, the deterioration of noise figure at lower frequencies (see Fig. 11), and the IPN at higher frequencies (due to external generator [34]) is expected to deteriorate accordingly the

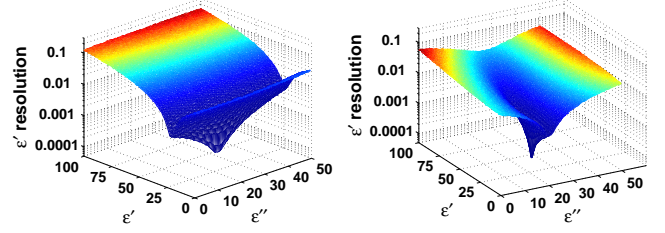


Fig. 13. Simulated ϵ' and ϵ'' resolution versus permittivity for the chip model for $f = 1 \text{ GHz}$, $b = 2$, $\Delta f = 1 \text{ kHz}$, $IPN = -90 \text{ dBc}$, $NF = 7.5 \text{ dB}$, $CG = 30 \text{ dB}$ (off-chip amplification included).

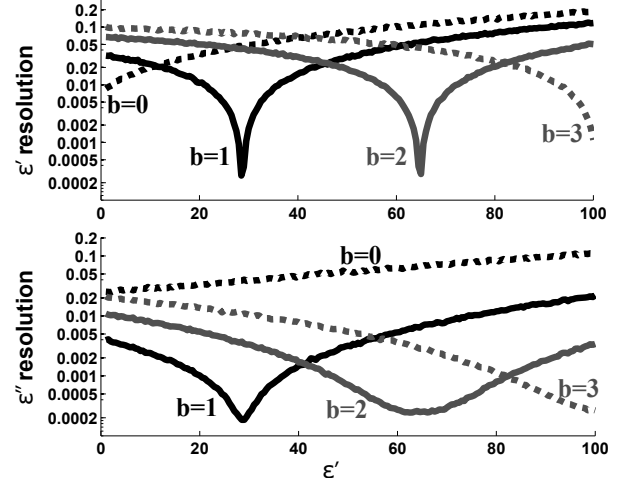


Fig. 14. Simulated ϵ' (top) and ϵ'' (bottom) resolution versus real part of permittivity, at different bridge capacitance settings for $f = 1 \text{ GHz}$, $\Delta f = 1 \text{ kHz}$, $IPN = -90 \text{ dBc}$, $NF = 7.5 \text{ dB}$, $CG = 30 \text{ dB}$ (off-chip amplification included).

permittivity resolution. In fact, if we assume a linear ϵ -to- Y_L model as well as a linearized bridge operation, the permittivity resolution deteriorates 10 times for every 10 dB increase of IPN or the noise figure, when the external bridge driver noise is dominating the overall measured noise (unbalanced bridge), as is practically the case.

V. EXPERIMENTAL RESULTS

The reported design was incorporated in a test IC, fabricated in a 7-metal, 40-nm CMOS process, with an ultra-thick top metal option, used for the sensing element. Using such an advanced technology node allows extension of frequency range, although is not expected to offer significant area advantages, due to the extensive usage of analog circuitry and passive elements. The chip micrograph, along with the test PCB and the packaging used for the measurement of liquids, is shown in Fig. 15. The chip area is $1.6 \times 0.5 \text{ mm}^2$ while the active pixel area is $0.15 \times 0.3 \text{ mm}^2$, thus suitable for embedding in a sub-mm spatial resolution array. As seen in the zoomed-in micrograph, the size of the active circuitry is similar to the patch, making it possible to adopt a circuit-under-pad approach in the future, with the trade-off of higher patch parasitic capacitance, due to the implementation of the ground plane at a higher metal level.

In order to enable verification of the bridge operation by loading it with a tunable admittance, two ground pads are included in the design, in such a way that the patch is embedded in a G-S-G configuration and can be interfaced by a probe.

For all measuring purposes, the IC was mounted and wire-bonded on a test PCB. In order to enable liquid material measurements, a

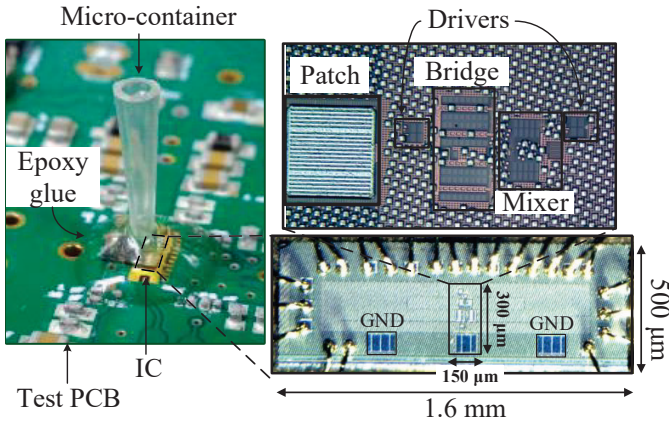


Fig. 15. Fabricated IC micrograph and packaging on a test PCB for measuring liquid materials.

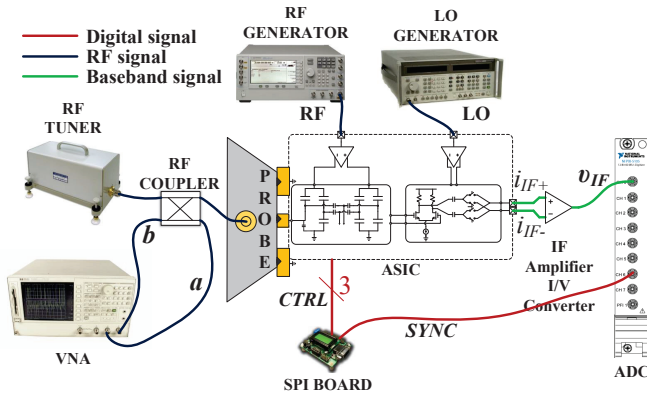


Fig. 16. Schematic of chip measurement setup for the verification of the bridge operation. The RF, LO, control and read-out part remains the same for liquid material measurement.

15-nL micro-container with a 500- μm bottom opening was carefully placed on top of the chip so that it encloses the patch. The rest of the chip was covered by epoxy glue in order to protect the bondwires (see Fig. 15). In order to apply a uniform liquid on top of the patch, the container was washed with ethanol and dried using pressurized air before every measurement. To avoid the formation of air bubbles, the liquid MUT was injected slowly into the micro-container by pointing a micro-needle towards the container walls. For the same purpose, the liquid was slightly stirred and the needle was carefully removed.

A. Load Measurements

In order to verify the operation of the bridge and the calibration procedure described in sections II-B and IV-A, respectively, the patch was contacted by a probe (Cascade Z40-V-GSG-500) to a digitally-controlled RF tuner (Maury MT982E) in order to allow loading of the bridge with various RF admittances. As shown in the diagram of the experimental setup in Fig. 16, the patch is interfaced to the tuner by directly probing the former and connecting the probe to the tuner through the forward path of a low-loss bi-directional RF coupler (Mini-circuits GDC35-93HP+). The coupling ports of the coupler are connected to a VNA (HP 8753D) for on-the-fly measurement of the forward (a) and reflected wave (b), in order to acquire the load admittance. Calibration is performed using a SOL wafer calibration kit for the probe while the source is driving the termination port of the RF tuner. During measurement, the VNA power is turned off and only the a and b waves are measured. Inverting the measured

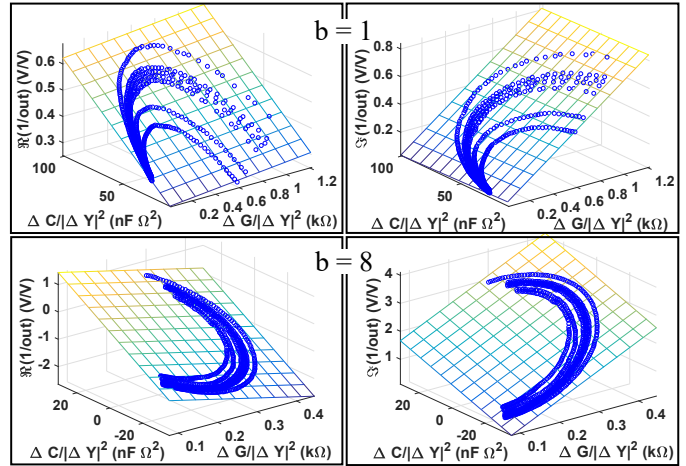


Fig. 17. Calibration surfaces acquired from all admittance measurements, showing a linear dependence of the real and imaginary part of the inverse output to the normalized admittance and conductance, as suggested by eq. 6 and 7.

reflection coefficient (Γ) provides the calibrated Γ of the measured load, therefore, its admittance Y_L can be calculated and expressed as a parallel combination of a capacitance C_L and a resistance R_L . This procedure is identical to the one used in load- and source-pull measurement systems to measure the load or source admittance [42].

Two external generators are used for the RF (Agilent E8257D) and LO (HP 8657) signals. Since the RF generator close-in noise performance is the most critical for the achievable noise performance of the permittivity sensor, the highest available quality generator is used for the RF signal. An intermediate frequency of 150 kHz was deemed high enough to stay outside the observed $1/f$ corner frequency of the mixer. An external IF amplifier (AD 624ADZ) converts the output differential current ($i_{IF+} - i_{IF-}$) to a differential voltage through a 10 k Ω resistance and, further, to a single ended voltage (v_{IF}) of an appropriate amplitude range for the external 12-bit, 60MS/s ADC (NI-5105), through an adjustable conversion gain of 0–40 dB. As such, the ADC quantization noise does not contribute significantly to the overall measured noise. An external board provides the required digital controls to the chip, i.e. the branch capacitance setting b and the lc bit control for ratio-metric measurement. The lc signal is also used for synchronization of the ADC. A trace of 1 ms is acquired at each measurement, corresponding to a frequency resolution bandwidth (Δf) of 1 kHz. The digitized data are transferred to a PC, where the FFT is performed and the corresponding amplitude and phase at IF is calculated and the calibration procedure is carried out. The RF measurement frequency of this experiment was 1 GHz.

At 960 discrete tuner position settings, the bridge load was varied between 53.5 fF and 920.2 fF and the resistance between 540 Ω (1.85 mS) and 988 Ω (1.01 mS). Therefore, the baseline admittance value of the bridge is a 486.7-fF capacitor in parallel to a 764- Ω resistance (1.31 mS conductance). These loading conditions are similar to what is expected for the permittivity of interest. The calibration coefficients are calculated as described in IV-A, for the two bridge settings of $b = 1$ and $b = 8$. Fig. 17 shows the calibration surfaces, as described by (13) and (14), for these two bridge settings, with the annotated measurement points. The measured data are fitted to the calibration surface with an adjusted R^2 always better than 99.97% and an rms error less than 0.94%.

As already mentioned, apart from the K coefficients of the calibration surfaces, an offset admittance Y_{off} is always associated with

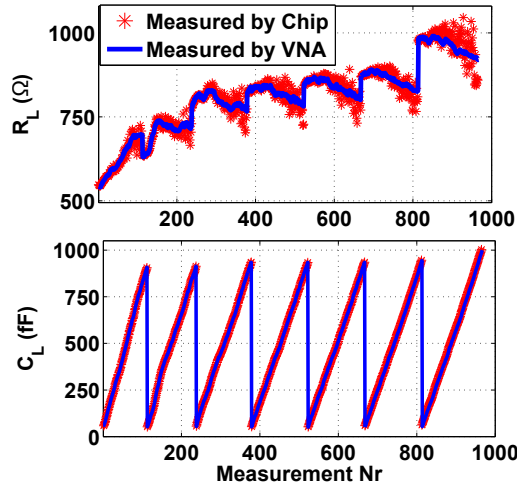


Fig. 18. Measured load parallel capacitance and resistance for 960 different tuner settings at $b = 1$.

the calibration procedure to denote the deviation of the load baseline value from the bridge balance. The offset admittance that maximizes the calibration surface fit to the materials is $27.3 fF || 0.15 mS$ for $b = 1$ and $752 fF || -1.35 mS$ for $b = 8$. The difference of offset capacitance between these two settings is $724.7 fF$, which agrees well with the simulated branch capacitance difference of $693.5 fF$ from the simulations (see section II-B). On the other hand, the conductance difference is $1.5 mS$, as opposed to the simulated value of $0.14 mS$, which indicates an inaccurate model of the switched capacitor losses at this frequency. Nevertheless, the low offset values for $b = 1$ indicate that the bridge can be close to the balanced state for the range of loads used.

To validate the calibration, the inverse calibration procedure is followed to extract the load capacitance and resistance measured by the chip. Fig. 18 shows the capacitance and resistance values measured by the chip and the VNA, for $b = 1$. The rms capacitance error between the VNA and chip measurements is $1.63 fF$ while the resistance error is 20.7Ω . For $b = 8$, the errors are $2.24 fF$ and 10Ω , respectively.

B. Material Permittivity Measurements

A number of six liquid materials was available for permittivity measurement: de-ionized water, methanol, ethanol, 2-propanol (IPA), 1-butanol and air. Except for air, which we assume to be a lossless dielectric with a unity relative permittivity at every frequency, all other materials exhibit a frequency-dependent permittivity, described by their unique Debye model parameters [39]. Fig. 19 shows the permittivity profile versus frequency of the utilized materials. All materials except ethanol are used for calibration of the chip while ethanol was chosen as the independent measurement material because its permittivity is, for most of the frequency range, in-between all the available material permittivities.

For every available material, 100 1-ms measurements of the output are acquired, at every b value from 0 to 8, and at various values of RF fundamanetal frequency, covering 0.1-5 GHz. The third and fifth harmonic could also be measured up to a certain frequency, as described in II-C, achieving a meaningful signal at an overall frequency range of 0.1-10 GHz. The chip power consumption on a 1.1-V supply was measured between 1.2 mW at 0.1 GHz and 24 mW at 5 GHz, a difference due to the fact that bridge and LO drivers are inverter-based circuits and, as such, their power consumption varies linearly with frequency.

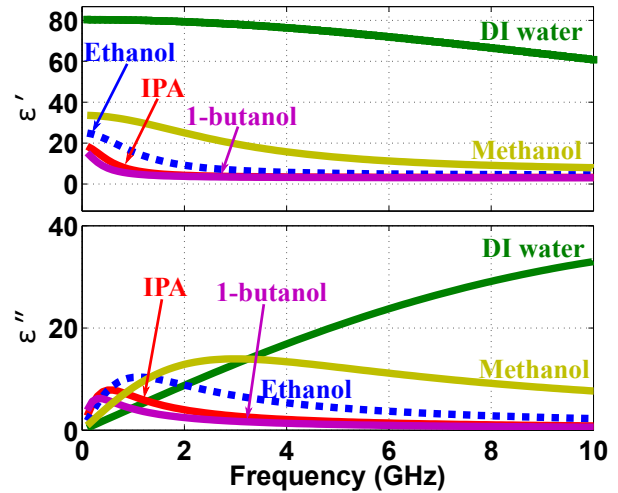


Fig. 19. Real and imaginary part of permittivity of the materials measured, versus frequency, generated from their Debye models [39]. Ethanol (dashed line) is used for validation as an independent material.

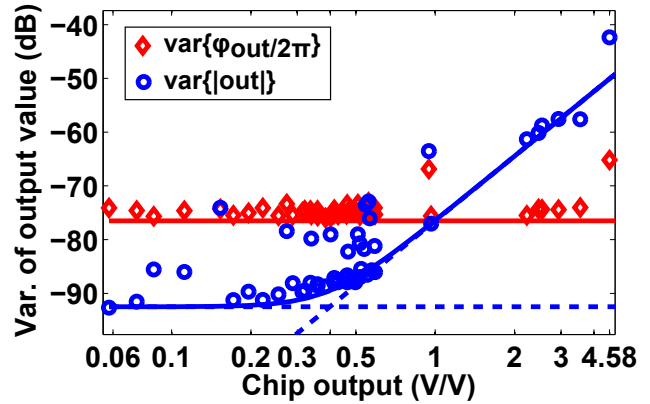


Fig. 20. Output phase and amplitude variance versus chip ratiometric output value for all measured materials and all bridge capacitance settings (varying bridge imbalance) at 1GHz, with annotated expected Cramér-Rao measurement bounds of (23) and (24). $\Delta f = 1 kHz$, $IPN = -90 dBc$, $NF = 7.5 dB$, $CG = 30 dB$ (off-chip amplification included).

The variance of the measured amplitude and phase versus chip output at 1 GHz is shown in Fig. 20. In the same plot, the predicted Cramér-Rao measurement bounds of (23) and (24) are annotated. It is observed that the measurement variances are concentrated on or above the bound. A very good agreement between prediction and measurement is seen in the output phase, which does not show a dependence on the bridge imbalance. On the contrary, larger bridge imbalance affects the amplitude variance, as expected by the model. The discrepancy of some measurement points from their lower bound is likely due to the sensitivity of the measurement amplitude to short-term supply-voltage variations, or to variations of other measurement conditions that happen within the measurement time of 1 ms.

Translation from a permittivity to an admittance value and vice-versa is performed using the rational function model for the patch, explained in II-A. Subsequently, the established calibration procedure is followed at each frequency and b value setting. An average of all 100 measurements is used for the calibration to reduce the random statistical variation of the measurements. Since permittivity read-out noise is generated by white Gaussian noise, we can assume a Gaussian distribution of the permittivity measurement variation as well.

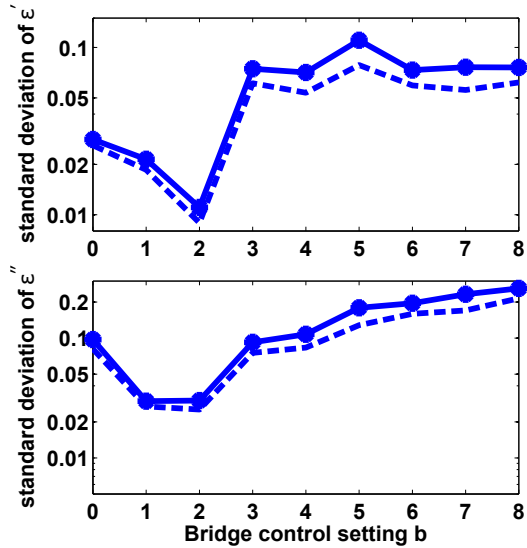


Fig. 21. Permittivity resolution versus bridge control setting b , for ethanol measurement at 1 GHz (solid line). The dashed line corresponds to the expected resolution if the phase and amplitude variance was equal to the Cramér-Rao bound.

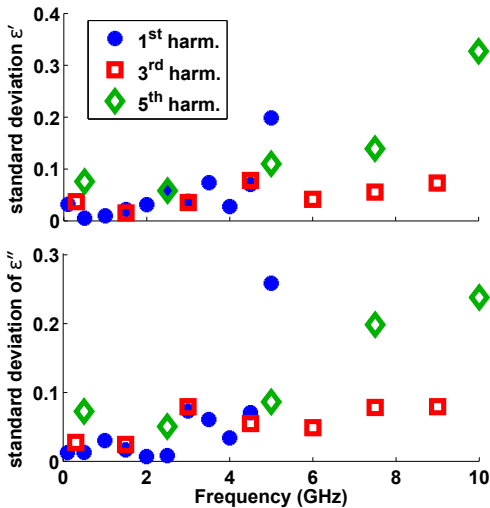
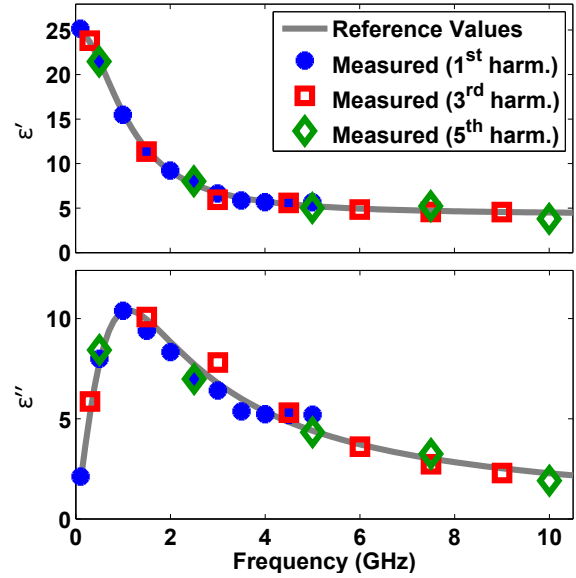


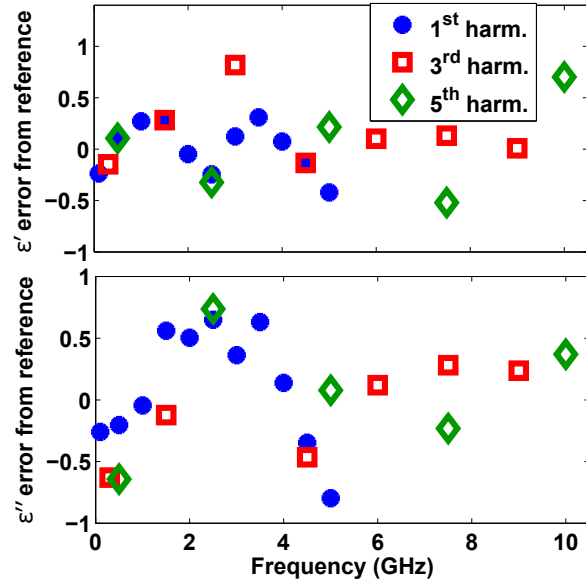
Fig. 22. Measured permittivity resolution of ethanol using first, third, and fifth frequency harmonics.

Therefore, to assess the permittivity resolution of the independent material (ethanol), the standard deviation of 100 consecutive permittivity measurements is examined. This is an indication of the minimum resolvable permittivity difference at the resolution bandwidth that corresponds to each of the individual 1-ms measurements. Fig. 21 shows how permittivity resolution varies with the b setting when measuring ethanol at 1 GHz. As expected from previous analysis, the resolution worsens when the bridge is set to unbalanced states and is minimized when it is close to the balanced state. A very good agreement is also observed between the measured and theoretical resolution corresponding to the Cramér-Rao bound.

It was found that the bridge balances best for ethanol at $b = 2$ below 5 GHz and at $b = 1$ above that frequency. Fig. 22 shows the measured permittivity resolution of ethanol for these capacitance settings versus frequency, demonstrating measurements at the first, third and fifth harmonic. Owing to the worse noise figure at the higher harmonics, the resolution at the first harmonic point of each



(a)



(b)

Fig. 23. (a) Independent measurement of ethanol permittivity versus frequency. The Debye model of ethanol is shown as a reference value. (b) Error between the measured permittivity of ethanol and the values corresponding to its Debye model.

measurement is always better than that at the third harmonic, which, in turn is always better than that at the fifth. The measured resolution also follows the generator's integrated phase noise profile versus frequency, therefore, it worsens at higher frequencies. Over the frequency range of 0.1–10 GHz, the permittivity resolution always stays below 0.4 and 0.3 for the real and imaginary part, respectively.

As has been discussed, the achieved permittivity resolution is bounded by external phase noise sources as well as short term supply variations that cannot be correlated due to the time-division measurement of the reference load. These effects can be mitigated in a future implementation of a pixel array by the inclusion of a reference pixel to be read out simultaneously with the pixel of interest in a parallel measurement path. Thus, global external noise sources as well as supply variations can be canceled out

TABLE II
COMPARISON OF IMPLEMENTED SENSING PIXEL WITH STATE-OF-THE-ART CMOS INTEGRATED PERMITTIVITY SENSORS

	CMOS node	Sensing element	Architecture	Operating frequency (GHz)	Permittivity range	Permittivity accuracy	Permittivity resolution (σ)	Mes. time	Power (mW)	Area [Active] (mm ²)
This work	40 nm	Single-ended patch	Multi-harm. IF down-conversion	0.1–10	ϵ' : 1 – 80 ϵ'' : 0 – 40	$\epsilon' < 1$ $\epsilon'' < 1$	$\epsilon' < 0.4$ $\epsilon'' < 0.3$	1 ms	1.2–24	1.6×0.5 [0.15 \times 0.3]
[17] JSSCC'12	90 nm	Differential capacitor	LC VCO	7–9	ϵ' : 2.4 – 20.2	N/A	$\epsilon' < 1^*$ (@8 GHz)	N/A	16.5	2.5×2.5 [1.5 \times 2.2] [†]
[18] IMS'13	65 nm	CPW t-line	IF down-conversion	1–50	ϵ' : 4 – 5 ϵ'' : 1 – 4	N/A	$ \epsilon $: 0.0445* (@20 GHz)	20 ms	114	N/A [0.6 \times 2]
[19] T-MTT'13	90 nm	Differential capacitor	LC Frac-N PLL	10.4	ϵ' : 1 – 8	$\epsilon' < 0.1^*$	N/A	N/A	22	1.7×1.3 [0.9 \times 0.9] [†]
[20] JSSCC'14	0.35 μ m	Off-chip μ -strip line	Super-heterodyne	0.05–3	ϵ' : 1 – 48	$\epsilon' < 0.6^*$	N/A	1 ms	4–9	3×3 [0.9 \times 2.5] [†]
[21] T-MTT'14	0.18 μ m	Differential capacitor	Zero-IF	0.62–10	ϵ' : 1 – 40 ϵ'' : 0 – 20	$\epsilon' < 0.7^\ddagger$ $\epsilon'' < 0.1^\ddagger$	N/A	>10 ms	65–72	3×3 [0.9 \times 2.3] [†]
[22] TCAS-I'15	0.18 μ m	Differential capacitor	RO Int.-N PLL & ALL	0.7–6	ϵ' : 1 – 80 ϵ'' : 0 – 40	$\epsilon' < 1.75^*$ $\epsilon'' < 0.7^*$	N/A	1 s	69–140	2.5×2.5 [0.9 \times 1.3] [†]
[23] T-BioCAS'15	0.35 μ m	Off-chip 3D capacitor	Zero-IF	0.009-2.4	ϵ' : 1 – 94 ϵ'' : 0 – 465	$\epsilon' < 0.5^*$ $\epsilon'' < 1^*$	N/A	N/A	61–94	3.3×3.3 [2.5 \times 2.5] [†]
[24] JSSC'16	65 nm	Differential capacitor	Injection-locked VCOs	6.5/11/ 17.5/30	ϵ' : 1 – 60	N/A	$\epsilon' < 0.008^\S$	0.01 ms	65	$1.5 \times 1.2^\dagger$

*Extracted from reported maximum percentage error and ϵ value at that error

[†]Estimated from chip micrograph

[‡]Estimated from provided graph

[§]Extracted from minimum detectable capacitance change and EM-simulated sensor sensitivity versus ϵ'

by the ratio-metric measurement. This modification appears more imperative in a – possibly desired, yet not necessarily required for the intended application – fully-integrated solution that includes on-chip RF generators, since the latter are expected to feature a much worse phase noise performance than the off-chip generators used in the measurements presented in this work.

At the same permittivity settings that minimize the resolution, the average measured permittivity values of ethanol are plotted versus frequency in Fig. 23a. The error between measurement and reference numbers, indicated in Fig. 23b, stays below 1, with an rms value of 0.32 and 0.48 for the real and imaginary part, respectively. Notice the random distribution of the error versus frequency or harmonic, resulting in cases where the third and fifth harmonic measurement has lower error than the first, which is an indication that the accuracy errors are due to the combination of tolerances originating from the Debye models used for calibration standards and reference, the rational-function model and the calibration fitting, rather than a statistical error associated with noise, as is the case for the measured resolution.

VI. CONCLUSION

The design, calibration and measurement of a compact 40-nm CMOS complex permittivity sensing pixel has been presented. Introducing a reconfigurable double balanced wheatstone bridge, multi-harmonic down-conversion scheme, the sensor can achieve a high-resolution and fast permittivity read-out across a wide frequency range of 0.1–10 GHz.

Table II summarizes the achieved performance of the sensor along with the results of previously published state-of-the-art integrated permittivity sensors. To the best of the authors' knowledge, this work features the smallest active area while achieving fast and precise operation over two decades of bandwidth. Moreover, compared to previous works, this contribution quantifies both accuracy and resolution of measured permittivity over the operation frequency

range, while differentiating between the two, based on their sources. A single-ended patch sensing element approach is followed, which facilitates better EM interfacing with the MUT as well as offering more flexibility for more advanced drive schemes in future EM-based multi-pixel arrays. These properties, along with its compact size, fast readout and broadband architecture, make it suitable for utilization as a pixel element in 2D permittivity-based imaging sensors for biomedical and industrial applications.

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