High efficiency IBC solar cells with poly-Si implanted passivating contacts

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HIGH EFFICIENCY IBC SOLAR CELLS WITH POLY-SI IMPLANTED PASSIVATING CONTACTS

By

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Abstract

Crystalline silicon (c-Si) interdigitated back contacted (IBC) solar cell with poly-Si passivating contacts is one of the most promising approaches to achieve high conversion efficiency solar cells. The fabrication of IBC silicon-based solar cells provided by poly-Si passivating contacts is investigated in this thesis.

The passivating poly-Si contacts structure used in this work is based on an ultra-thin layer of t-SiO_X with optimized poly-Si thicknesses of 250 nm and the implantation parameters of Phosphorous and Boron doping with 6e15 and 5e15 ions/cm^2 respectively, at a fixed implantation energy of 20 keV. The influence of the post-implantation annealing conditions is discussed with experimental results, obtained on symmetrical test structures with thermal SiOx/doped poly-Si on each side. The best-obtained passivation result for n^+ -poly-Si contact was 728 mV at annealing conditions of 1050°C for 1 minute, while for the p^+ poly-Si contact at the same annealing conditions 699 mV is obtained. To enhance the passivation, PECVD deposited SiN_X capping layer and annealing in forming gas as hydrogenation processes are carried out. Then, FBC solar cells are fabricated to evaluate the electrical performances, in terms of passivation and carrier transport, of the poly-Si contacts structures, which are prepared with different annealing conditions, in terms of temperature and time. The results obtained from the FBC cells show that increasing the annealing temperature leads to an increase in the passivation thus the V_{OC}. The best-obtained V_{OC} was 706mV for the wafer annealed at 1050°C for 1 minute.

To enhance the optical properties of the IBC cells, the surface is textured and the influence of doping dose on passivation of the front surface field (FSF) is evaluated. Four different passivation stack layers SiN_X, AlO_X/SiN_X, a-Si/SiN_X, and double SiN_y /SiN_X are evaluated for FSF implanted with dose of 1e14 ions/cm^2. The best-obtained passivation result is from FSF sample passivated with a-Si/SiN_X. *It* shows excellent passivation property with iV_{OC} of 714 mV and a J_0 of 7.5 fA/cm^2. while the other stacks show lower passivation of iV_{OC} 708 mV for the AlO_X/SiN_X sample and iV_{OC}=686 mV for the SiN_y /SiN_X sample. The influence of FGA on the FSF passivation quality is also evaluated. The results show that the sample passivated with a-Si/SiN_X experienced a sharp decrease of 35 mV in the iV_{OC} after FGA due to the low thermal stability of the a-Si:H. On the other hand, other FSF samples with passivation stacks of SiN_X, AlO_X/SiN_X, and SiN_X /SiN_X show a positive influence upon the FGA on their passivation quality as a result of the extra hydrogen diffusion during the FGA which saturates more defects on the c-Si surface.

The implantation of the optimized thermal SiOx/ doped poly-Si structure and FSF with a-Si/SiN_X passivating layer into the IBC solar cells leads to high-efficiency IBC solar cells. The record cell has a conversion efficiency of 21.04% and 22.15% after the post metallization annealing, V_{OC} of 681 mV, and *FF* of 78,9 with J_{sc} of 37.5 mA/cm^2

CONTENTS

Nomenclature

Poly-SiO_X	Oxygen Alloyed Polycrystalline Silicon
Poly-Si	Polycrystalline Silicon
τeff	Minority Carrier Lifetime
Eg	Bandgap
η	Conversion efficiency
EC	Conduction Band
ρ_C	Specific Contact resistance
EV	Valance Band
a-Si	Amorphous Silicon
FBC	Front and Back Contacted
Ag	Silver
FF	Fill Factor
Al	Aluminum
FG	Forming Gas
ALD	Atomic Layer Deposition
FZ	Float Zone
ARC	Anti-reflection Coating
HF	Hydrofluoric Acid
B	Boron
HNO_3	Nitric Acid
BHF	Buffer Hydrofluoric Acid

iV_{OC}	Implied open-circuit voltage
c-Si	Crystalline Silicon
IBC	Interdigitated Back Contact
CSPC	Carrier Selective Passivating Contacts
ITO	Indium Tin Oxide
TMAH	Tetramethylammonium Hydroxide
J_0	Recombination Current Density
VOC	Open-Circuit Voltage
JSC	Short-circuit Current density
PECVD	Plasma Enhanced Chemical Layer Deposition
LPCVD	Low Pressure Chemical Vapor Deposition
PV	Photovoltaics
NAOS	Nitric Acid Oxidation of Silicon
Rs	Series Resistance
N_2	Nitrogen
Rshunt	Shunt Resistance
O_2	Oxygen
Cu	Copper
P	Phosphorous
ITO	Indium Tin Oxide
SEM	Scanning Electron Microscopy
J_0	Recombination Current Density
SRH	Shockley-Read-Hall
JSC	Short-circuit Current density
STC	Standard Test Conditions
SiH4	Silane
SiN_X	Silicon Nitride
TCO	Transparent Conducting Oxide

1

INTRODUCTION

Plants satisfied their energy needs by Photosynthesis with sunshine and we live in an era where humankind seeks to satisfy their growing demands of energy by the sun as well which has been forever providing the planet with free light, warmth, and even life.

Nevertheless, 13% of the world population do not have access to electricity according to The International Energy Agency in 2016, IEA still expects the energy consumption to rise 50% in 2050 compared to the energy consumption level in 2019 where this growth is driven by the main industrial Asian countries like China and, Taiwan [2], thus, providing clean energy that fulfills the growing energy demand is crucial nowadays to stop the climate change which is directly related to the excessive use of the conventional energy source like Coal, Oil, and gas. IEA claimed a considerable drop of 7% in global CO2 as a consequence of the lockdown and measurement associated with the Covid-19 pandemic [1], where the United Nations Climate Change Conference that is held in Paris need to reach a Zero green gas emission in 2050 to meet their goal of keeping the temperature of the globe “well below 2°C above preindustrial levels and pursuing efforts to limit the temperature increase to 1.5°C above pre-industrial levels”. Therefore, Solar energy comes in the center of the renewable energy sources to achieve the required shift to clean energy resources and meet the rapid energy demand. Due to the sharp decrease in the electricity generated by solar PV power plants where the LCOE reaches a record of 3.7ct€ / kWh, consistent rapid growth is witnessed in the cumulative PV installation globally to reach 584 GWP at the end of 2019[3]. China still leading the world in the solar market in both PV module production and PV plant installation with 36% of the PV global installed capacity.

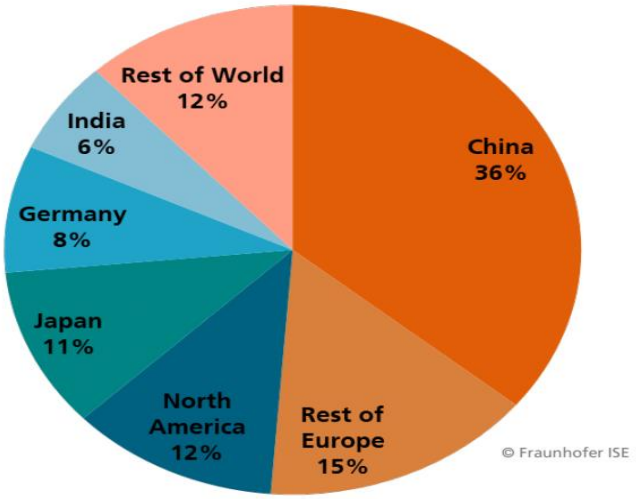


Figure1.1: The percentage of PV modules installed capacity per region [3].

As the solar industry is still scaling up it is associated with a decrease in the production cost of PV modules. The thin-film PV modules still have a low share in the market while the Mono-crystalline Si PV modules gain more share in the market with 65% to become the largest technology even though multi-crystalline PV modules rolled the solar market in the beginning. The main advantages of solar energy are based on the properties of Silicon material since Silicon is abundant, non-toxic, durable, and shows very good performance stability in the long term. Because of the domination of silicon-based solar cells in the market, it still gains attention in research to enhance its conversion efficiency. The lab record mono-crystallin Si-based solar cell shows efficiency of 26.7% while its multi-crystalline counterpart shows a conversion efficiency of 22.3% [3]. The gradual increase in the conversion efficiency is attributed to the improvement in the material used to fabricate the cells and the new approaches that are used to quench the recombination losses in the cell besides the advanced design of the optical properties [4].

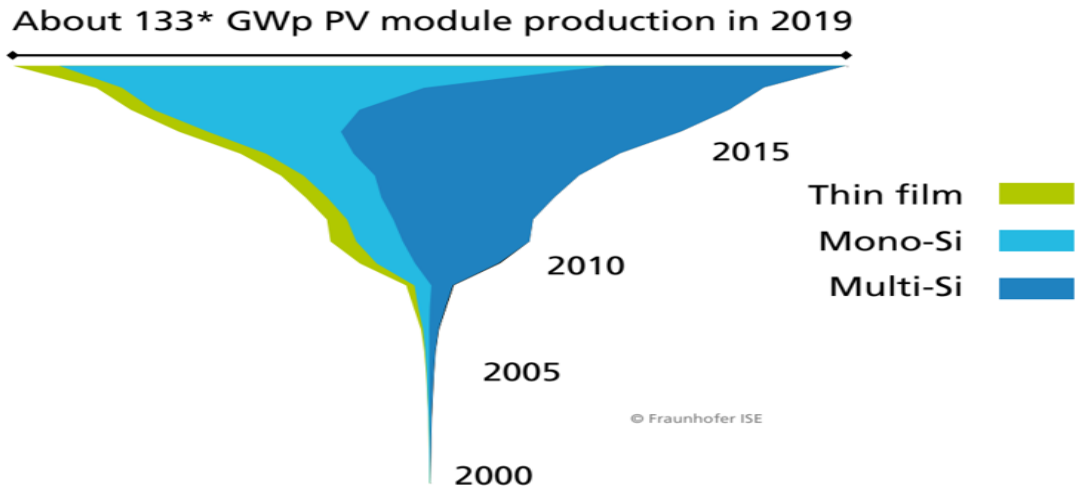


Figure1.2: The annual PV production by technology [3].

1.1The working principle of solar cells

Basically, a solar cell is a device that generates useful electrical energy when it is exposed to a light source. What is called a photovoltaic effect is the cornerstone notion of this energy conversion where electromagnetic radiation is directly converted into electricity. In the following, it is explained how electricity is generated in a simple PN junction.

Generation of mobile charge carriers occurs in the absorption layer when it is illuminated by a light source. The photons' energy should be greater than the energy of the semiconductor's bandgap to excite an electron-hole pair from the conduction band. In an indirect bandgap semiconductor like silicon, momentum should be provided additionally to enable this generation.

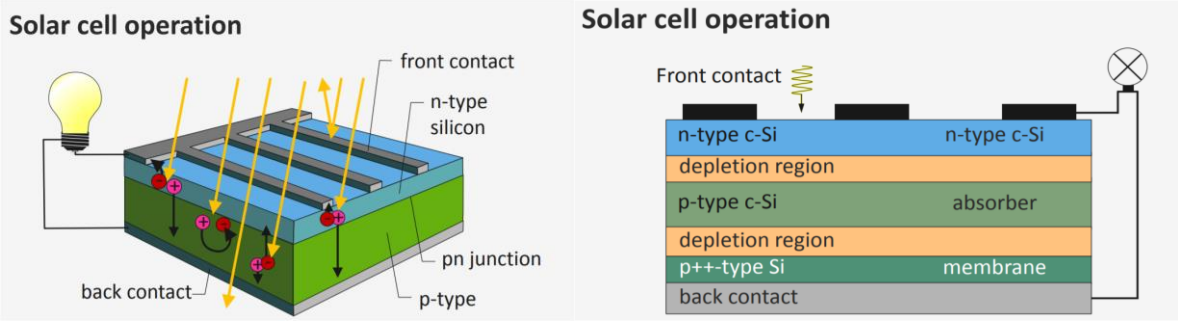


Figure1.3: A simplified representation of a silicon-based solar cell [5].

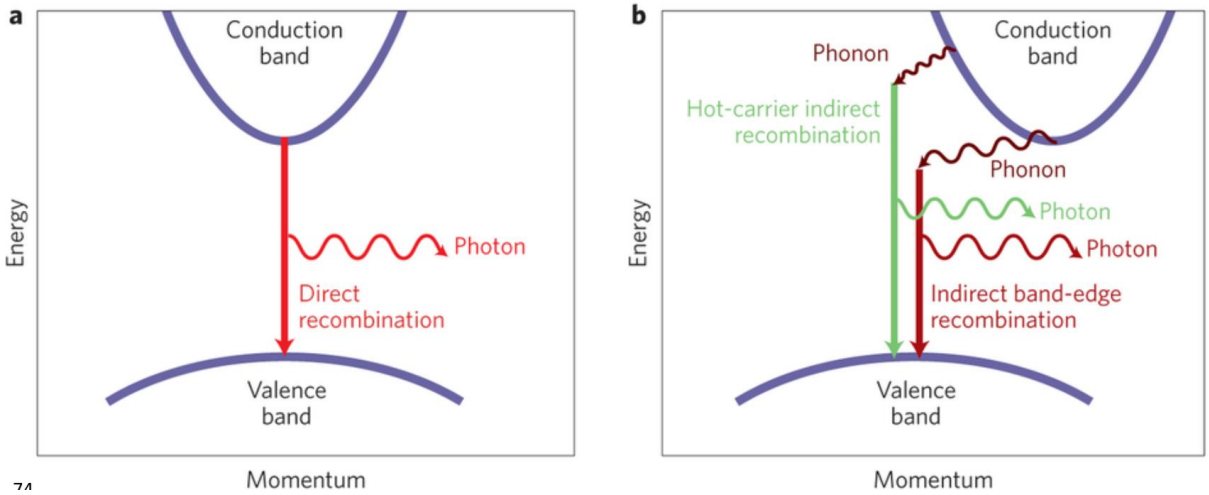


Figure 1.4: Illustration of the difference between (a) a direct bandgap semiconductor, and (b) an indirect bandgap semiconductor [6].

Separation of the free electron-hole pairs generated is crucial to make use of the absorbed energy, otherwise, these generated mobile charge carriers will recombine again and annihilate. The separation process is done by diffusion and drift current forming the transport mechanism over the depletion region in the P-N junction. After that, a collection process is required to build a useful electric current through an external circuit. A load is connected to the metal contacts of the solar cell where the collected electrons pass through one of the metal contacts to the external load and recombine with a hole at the other electrode.

1.2 Solar cell parameters

In order to define the performance of a solar cell, various properties of the cell have to be measured and characterized. The most important parameters are extracted from the JV-curve of an illuminated cell under standard test conditions which will be well defined in this section.

Standard test conditions: Researchers and manufacturers rate the output power and other parameters of a solar cell or a solar module at standard test conditions as following, cells temperature should be at 25 ^{O}C with no wind, while the light source simulator has to resemble a spectral shape similar to the AM1.5 air math spectrum and a total irradiance of 1000 W/m2.

Conversion efficiency: The conversion efficiency is the ratio between the output electric energy and the energy of incident light under standard test conditions which can be calculated by equation 1.1.

$$\eta = \frac{P_{max}}{P_{in}} = \frac{J_{sc}.V_{oc}.FF}{P_{in}} \qquad 1.1$$

Open circuit voltage (V_{oc}): The open-circuit voltage (V_{OC}) represents the maximum voltage a solar cell can generate since it is measured in the absence of the current flow through the cell and is given by equation 1.2

$$V_{OC} = \frac{k_B}{q} \ln \frac{J_{ph}}{J_0} + 1 \qquad 1.2$$

Where (J_{PH}) is the photogenerated current density, (J_0) is the saturation current density, and (q) is the elementary charge. The equation shows that higher irradiance increases the photogenerated current density (J_{PH}) which leads to higher open-circuit voltage, while higher temperature causes a larger leakage current (J_0) thus lower (V_{OC}). The dark saturation current (J_0) is related as well to the recombination rate in the cell therefore, the open-circuit voltage is a key factor to determine the passivation quality of the cell.

-Short circuit current (I_{SC}): The Short circuit current is measured at zero voltage; consequently, it is the maximum current that a solar cell can deliver. Generally, the short current density (J_{SC}) is used instead

of the short circuit current (I_{SC}) as it includes the unit area cm2 in its value. It is important to notice that photogenerated current (J_{PH}) is equal to the short circuit current in ideal conditions, hence the optical properties of the solar cell such as absorption and reflection strongly affect the values of the photogenerated current and the short circuit current respectively.

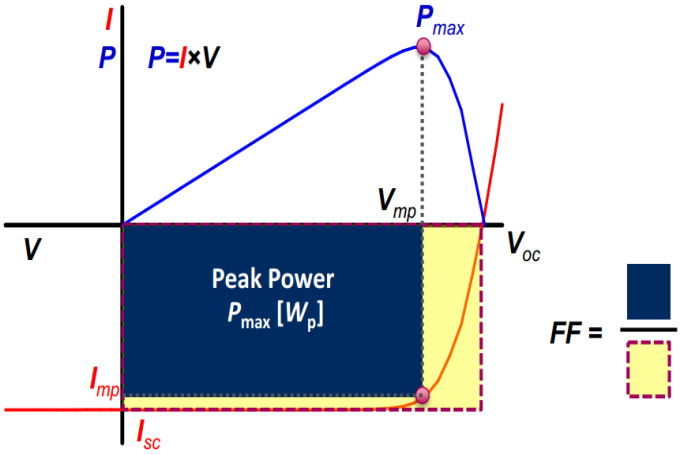


Figure 1.5: Illustration of IV curve of an illuminated solar cell.

Fill factor (FF): The fill factor represents the rate between the maximum output power calculated at short circuit conditions and the maximum power measured at the operation point. See figure1.2

Equation 1.1 shows that a higher fill factor causes higher conversion efficiency, as a result, it is commonly used to compare solar cells performance. To obtain a high fill factor, series resistance Rs should be minimized which consists of the silicon bulk resistance, the resistance of the metallic electrodes and, the resistance between the semiconductor and the metal. On the other hand, low shunt resistance deteriorates the value of the fill factor, which can be a result of a poor-quality wafer or a leakage current across the junction.

External Quantum efficiency (EQE): The external quantum efficiency is essential to analyze the optical properties of a solar cell and, determine the parasitic absorption. It represents the ratio between the number of collected charge carriers in the device to the number of the incident photons as shown in equation 1.3.

$$EQE = \frac{Electrons/sec}{Photons/sec} = \frac{I_{ph}(\lambda)}{e\Phi_{ph}(\lambda)} \qquad 1.3$$

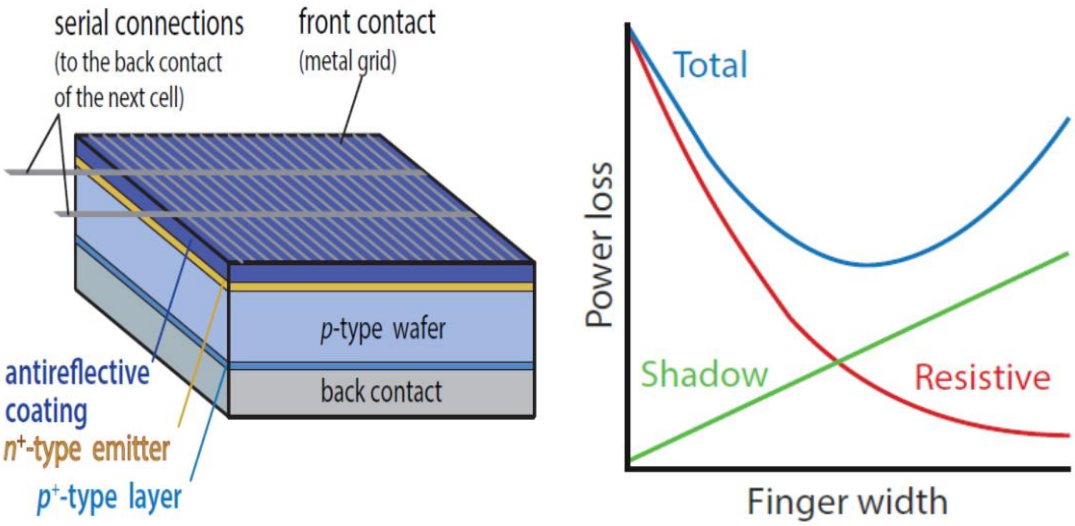
Determining the external quantum efficiency under short circuit conditions is a common way to calculate accurately the short circuit current density (JSC).

1.3 Loss mechanisms:

Understanding the loss sources in solar cells enables us to design advanced solar cells and maximize the conversion efficiency of the device. The loss sources in solar cells can be categorized into optical and electrical losses.

1.3.1 Optical losses:

Optical losses can be divided into two main categories, spectral mismatch, and additional losses. The spectral mismatch is considered the main reason behind the efficiency limitation of a solar cell. This mismatch between the energy of incident photons and the bandgap energy of the semiconductor appears in two cases. The first one is when the photons have lower energy than the semiconductor bandgap, therefore, these photons cannot be utilized to excite electrons from the valence band to the conduction band. On the other hand, when these photons have higher energy than the material bandgap Eg, electron-hole pairs will be promoted but the rest of the photon's energy will be lost in a thermalization process as heat.



Figuer1.6 (left) illustration of the metal grid in FBC solar cells. (Right) finding the optimum width of the metallic fingers.

The additional optical losses are attributed to shading, reflection, and parasitic absorption. A precise design is required to form the metallic grid of the solar cell contacts to achieve minimal shading and low electric resistance, see figure 1.4. Commercial solar cells include an antireflective coating to reduce the loss due to reflection, while advanced solar cells adopt novel approaches such as surface texturing and light management engineering to define the optimum parameters of the device's layers such as thickness and reflective index to minimize the reflection and the parasitic losses.

1.3.2 Electrical losses:

The failure to collect the generated charge carriers within the absorber layer leads to electrical loss which is mainly attributed to the recombination mechanisms in semiconductor materials. These mechanisms are surface recombination, radiative recombination, Shockley Read Hall (SRH) recombination, and Auger recombination.

Surface recombination is a major concern of researchers to increase the conversion efficiency of solar cells as it causes a significant drop in solar cell passivation. Surface recombination is based mainly on the dangling bond at the surface of the semiconductor which can be considered as localized defects that may trap a free charge carrier.

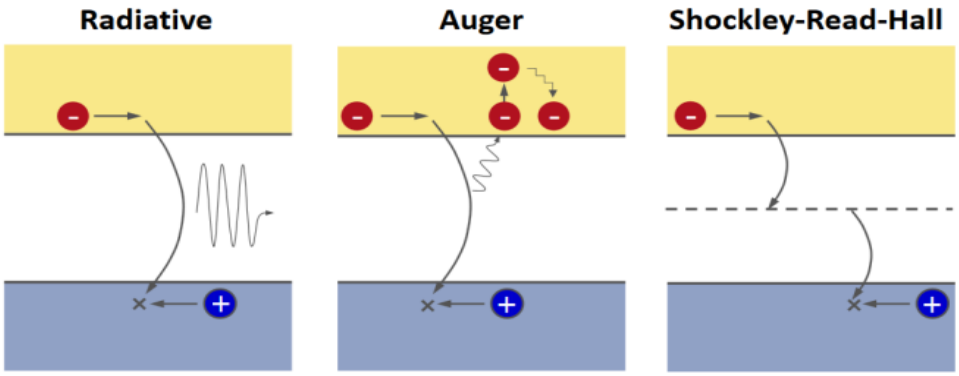


Figure 1.7 Illustration diagram of the recombination types [6].

Radiative recombination occurs when a recombined electron-hole emits a photon after an electron returns to its valance band, therefore, it can be seen as an opposite to the generation process. This type of recombination is rare in an indirect bandgap semiconductor material like silicon thus, it can be neglected in silicon-based solar cells.

Auger recombination is a three-particle process since the momentum and energy of a recombined electron-hole pair moves to a third particle which can be an electron or hole. Auger recombination is dominant in an indirect semiconductor material and it strongly depends on the charge carrier density; hence it becomes more important at high doping level.

Shockley Read Hall (SRH) recombination is facilitated by defects in the silicon bulks or impurity atoms which introduce trap-states within the forbidden gap and facilitate the recombination process. The recent technologies used in silicon production result in high-quality silicon wafers with low bulk defects. The defects formed at the grain boundary of polycrystalline silicon are the main reason for the low efficiency compared to the mono-crystallin silicon solar cells since they induce a higher rate of SRH recombination.

1.4 Surface passivation:

Silicon-based solar cells suffer strongly from surface recombination as mentioned in section 1.4. therefore, researchers have developed two techniques to overcome this problem and minimize this loss. The first technique used is chemical passivation where a thin layer of a suitable material is deposited on the surface of a silicon wafer, see figure 1.6. The dangling bonds at the surface form covalent bonds with the atoms of the passivating material deposited, thus decrease the defect density and reduce the likelihood of the surface recombination. Material like silicon oxide, a-Si, and Aluminum oxide show excellent passivation results and will be discussed extensively in chapter 5 [7].

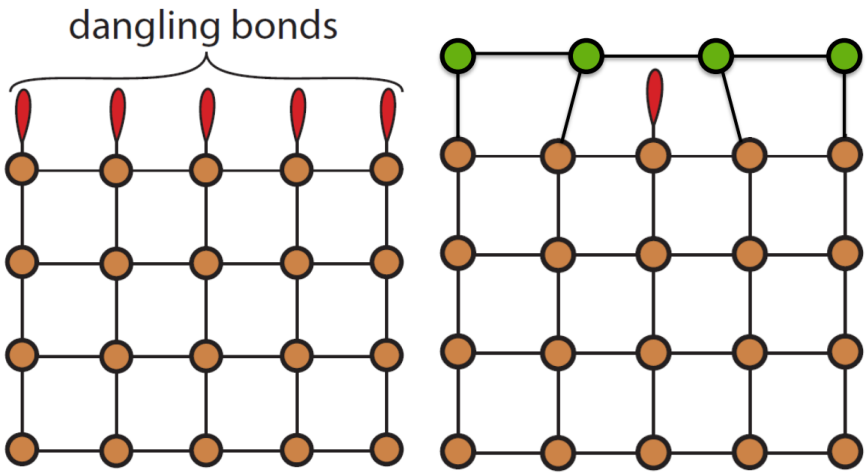


Figure 1.8 (a) Dangling bonds at the silicon surface. (b) covalent bonds after passivation.

Field-effect passivation is another used technique to reduce the loss caused by surface recombination. Introducing a heavily doped layer at the contact surface is a common practice to initiate an electric field that repels the minority charge carriers while allows the majority charge carriers generated to pass through.

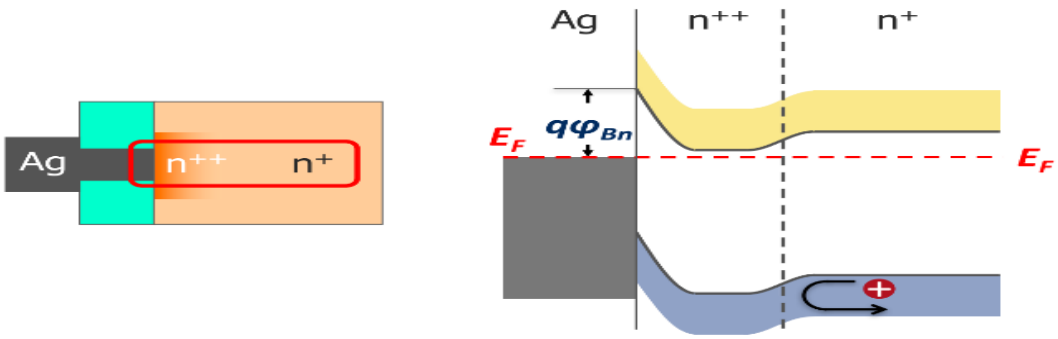


Figure 1.9: Sketch of a front selective emitter and its band diagram.

For example, in a p-type silicon wafer the generated holes nearby the emitter will recombine instantaneously with electrons at the metal interface thus, the recombination rate will be extremely high at the surface. Introducing a high concentration of phosphorus just under the contacts initiates a field effect that repels holes and allows only electrons to pass to the emitter, see figure 1.9. The same trick is used at the back contact to enhance the selectivity and reduce the recombination rate. This approach is applicable in interdigitated back contact solar cells, since their contacts in the backside, while a more complicated approach is required in front/back contacted solar cells to avoid Auger recombination caused by the high doping level nearby the surface.

1.5 Advanced design concepts in IBC solar cells:

Light management engineering and developing new solar cell structures led to a significant increase in the conversion efficiency of up to 26 % of silicon-based solar cells [8]. This efficiency increase is based on decreasing the optical and the electrical losses in the cell as will be explained in this section.

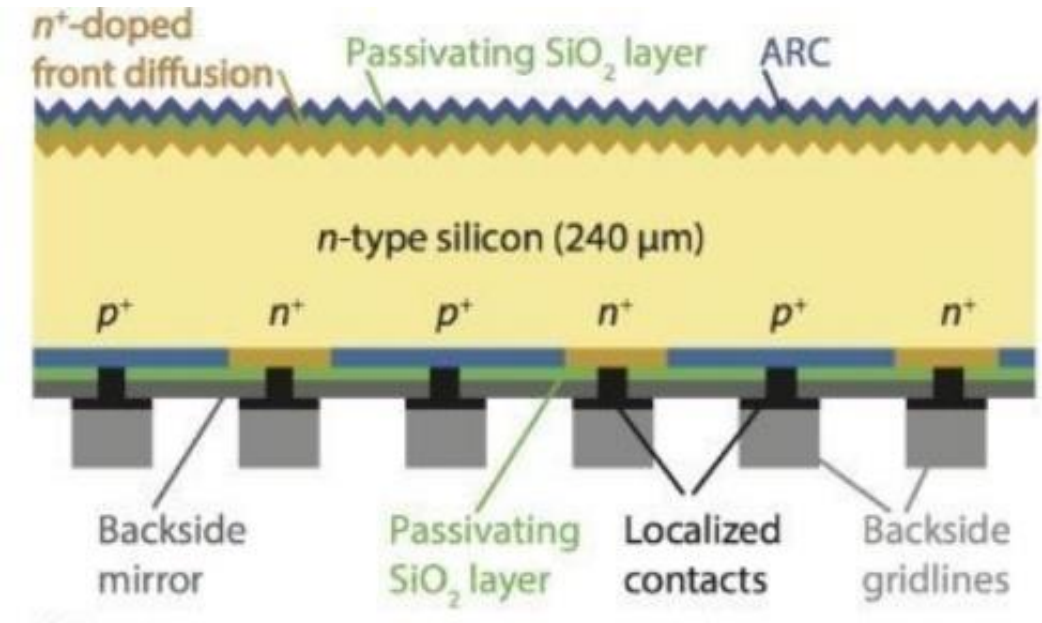


Figure1.10: Sketch diagram of an IBC solar cell with carrier selective contacts [6].

1.5.1 Minimizing the optical losses:

The main visual difference between conventional solar cells and interdigitated back contact solar cells (IBC) is moving the metal contacts grid to the backside of the module. Depositing the metal contacts at the backside is costly because it increases and complicates the production steps but it has valuable advantages such as decrease the shading, allowing thicker contacts which reduce contact resistivity and eliminate Auger recombination.

To enhance light absorption in the bulk, the surface is textured by a chemical etching process, and an anti-reflective coating layer is deposited on the surface. Usually, a silicon nitride layer is used as an anti-reflective coating with a thickness range from 50 to 100 nm. This layer is behind the common blue color of solar cells, and it is deposited through Plasma-enhanced chemical vapor deposition (PECVD) process at a certain temperature, and gas flow to achieve well-defined optical properties such as thickness, density, and refractive index.

1.5.2 Minimizing the electrical losses:

Beginning with the ohmic loss, contact resistivity plays a significant role in the series resistance of the solar cell and the Fill factor as a consequence. To reduce this resistance thicker metallic contacts are used without taking the shading effect into consideration since the contacts are in the backside in IBC solar cells. Aluminum is widely used in the mass production of solar cells thanks to price, whereas silver and copper have better conductivity thus lower loss but more expensive.

Carrier-selective passivating contacts (CSPCs) are becoming essential to overcome recombination loss at the contacts' interface. The fundamental characteristics of these contacts are providing effective carrier selectivity by creating sufficient band bending and introduce excellent interface passivation by treating the surface dangling bonds. Silicon oxide is a widely used material in the solar industry as a tunneling layer to provide chemical passivation and selectivity at the same time. It has a low fixed charge therefore it can be used in both n-type and p-type silicon wafers [9]. The growth condition of silicon oxides such as time and temperature is crucial to determine the thickness and the density of the created layer thus the passivation results. Generally, a hydrogenation step follows the deposition of the thermal silicon oxide by depositing a layer with a high hydrogen content to enhance the passivation during the annealing step. Materials like aluminum oxide (AlO_x) and amorphous silicon (a-Si) are typically used in the hydrogenation process which will be discussed in detail in the front surface field chapter.

1.6 Thesis objective:

The objective of this thesis is to fabricate high-efficiency IBC solar cells with thermal-SiOx/ (doped) poly-Si as passivating contacts. The main research questions are as follows:

1-investigating the passivation quality of the poly-Si selective passivating contacts by using dry thermal silicon oxide as a tunneling layer instead of wet oxidation.

2-evaluating the influence of high-temperature annealing on the dry thermal silicon oxide.

3-Evaluating the passivation of the front side of the cell by utilizing different doping doses and different passivation layers.

4- Optimizing the hydrogenation steps after evaluating the effect of the forming gas annealing (FGA) on the front surface field, and the passivated contacts.

The results of aim 1 and 2 will be applied first to produce front/back contacted solar cells (FBC), while the outcome of 3 and 4 will be implemented directly to produce IBC solar cells.

1.7 Thesis outline:

This thesis work consists of 6 main chapters, the second chapter provides a brief overview of the used technologies in the fabrication process and the measurement tools. In chapter 3 the theory behind the carrier selective contacts is first explained. then the fabrication process of the passivation test samples is detailed and results are discussed. The optimized poly-Si CSPCs in chapter 3 will be used to fabricate FBC solar cells. The fabrication process and the external parameters of these cells are measured and discussed in chapter 4. In chapter 5 the approach used to enhance the passivation of the front side of the cells is detailed and tested. while chapter 6 is assigned to explain the used flowchart to fabricate IBC solar cells and discuss the results. The report concludes with a discussion of the findings and recommendations to enhance the fabrication process and a road map to fabricate >23% IBC solar cells.

2

Experimental methods

This chapter aims to give a brief explanation of the main used technologies in the fabrication process to fabricate the IBC solar cells.

In this project, phosphorous (n-type) doped crystalline silicon (c-Si) wafers manufactured by TOP-SIL are used. The wafer material properties are presented in table 2.1. The reason behind the choice of n-type wafers is motivated by two crucial properties. First, n-type have a higher bulk minority carrier lifetime because it has lower sensitivity to recombination. Second, p-type material suffers from oxygen impurities due to wafer fabrication, therefore n-type are more used to avoid the boron-oxygen related light-induced [6].

Wafer properties:

In this work mono-crystalline, n-type silicon wafers manufactured by TOP-SIL are used during the fabrication process of the test samples and the IBC solar cells. The wafers properties are given in table 2.1. The choice of mono-crystalline silicon wafers is due to the absence of the grain boundary in the silicon to avoid the trap states at the edges which leads to a decrease in the lifetime of the carriers. The wafers are fabricated through the Float Zone process which is known for its low densities of impurities like oxygen and carbon. Phosphorous doped silicon wafer has desired advantages as they do not suffer from light-induced degradation like p-type wafers because of the absence of Oxygen and Boron, and also they are less sensitive to impurities like iron thus high-quality n-type silicon wafers are cheaper than their counterparts.

Table 2.1 c-Si material properties.

Parameter	Value
Doping	n-type
Thickness [µm]	260≃300
Orientation	<100>
Diameter [mm]	100 +/-2
Resistivity [ohm.cm]	1-5

Standard cleaning:

Standard cleaning is the first step in any fabricating process to remove any probable organic and inorganic contamination. They conducted a standard cleaning process in Else Kooi Laboratory (EKL), which consists of four steps. At the first step, the wafers are immersed in a 99% HNO_3 solution for ten minutes then they are moved to the rinsing bath for five minutes where an automatic rinsing process is performed with deionized water. Then the wafers are immersed in a 68 % HNO_3 solution at 100°C for 10 minutes and after that, the rinsing process is carried out again and followed by a dry step. To avoid the formation of a native oxide layer before the formation of the aimed silicon oxide an extra cleaning process (Marangoni) is performed. In this step the wafers are immersed in a 0.55% hydrofluoric acid (HF) solution until the surface becomes hydrophobic then the wafers are rinsed with deionized water to flush the HF and at the last minute, isopropyl alcohol (IPA) is added for drying.

Thermal Oxide Growth:

In this work, an ultra-thin layer of Thermal Oxide t-SiO_X is added as a tunneling layer. This layer is formed by dry thermal oxidation where the silicon wafers have entered a furnace at a temperature of 675°C for three minutes to enable the oxide growth with a thickness of 1.5 nm. The temperature and time are of significant importance to determine the thickness of the formed oxide. In this work, an Ellipsometry measurement is carried out to make sure that the formed oxide is in an acceptable thickness range between 1.4-1.5 nm. The formed Oxide is based on the reaction between the silicon and the Oxygen as shown in equation 2.1. This reaction takes place in a Tempress furnace where the chamber initially is filled with nitrogen with a gas flow of 6 SLM and when the furnace reaches the tuned value, Oxygen is added for a determined time duration with a gas flow of 0.6 SLM.

$$Si\ (s) + O2\ (g) \rightarrow SiO2\ (s)\ 2.1$$

To avoid any additional growth of the native oxide layer, the wafers are directly moved to the LPCVD furnace where the a-Si is deposited.

Low-pressure chemical vapor deposition (LPCVD):

In order to deposit a thick a-Si layer, the Low-pressure chemical vapor deposition (LPCVD) technique is used as it results in a pure and high uniformity deposited layer [10]. The process is carried out under low pressure (10 mTorr to 1 Torr) thus it is performed with minimal diffusion of the reactant gasses. Firstly, the tube is evacuated and when the pressure reaches the tuned value, the tube starts heating up to the deposition temperature to enable the precursor gas decomposition [11]. In the used recipe a 250 nm of a-Si is deposited at 580°C with a calculated deposition rate of 2.2 nm/min.

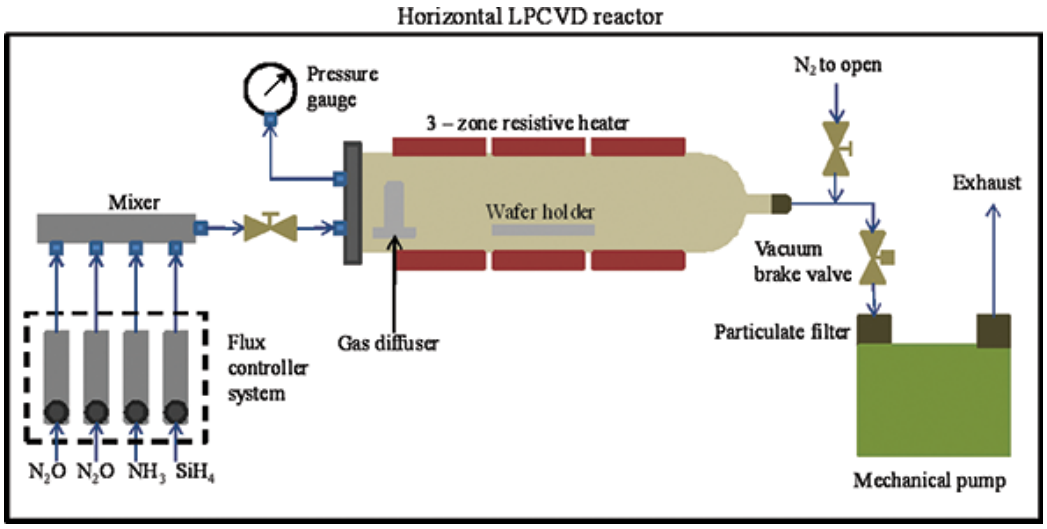


Figure 2.1 Schematic of an LPCVD reactor [12]

Ion Implantation:

To fabricate n^+ and p^+ poly-Si layers, ion-implantation technology is used to dope the a-Si with Phosphorous and Boron respectively. Varian ion implanter is used in this work which enables a wide control on the doped layer as we can tune the implantation energy to achieve the desired doping depth and the doping dose. The dopants are created by plasma and accelerated by a magnetic field towards the surface of the aimed wafer. The ions with high energy can cause a defect in the wafer's

surface which is a drawback of this technology. The used parameters in the implantation are illustrated in table 2.3 and the diagram of the implanter is sketched in figure

Table 2.3: the used implantation variables in the thesis.

Region	Ion type	Doping dose(ions/cm^2)	Implantation energy
Emitter	Boron	5e15	20 keV
BSF	Phosphorous	6e15	20 keV
FSF	Phosphorous	1e14 &3e14	20 keV

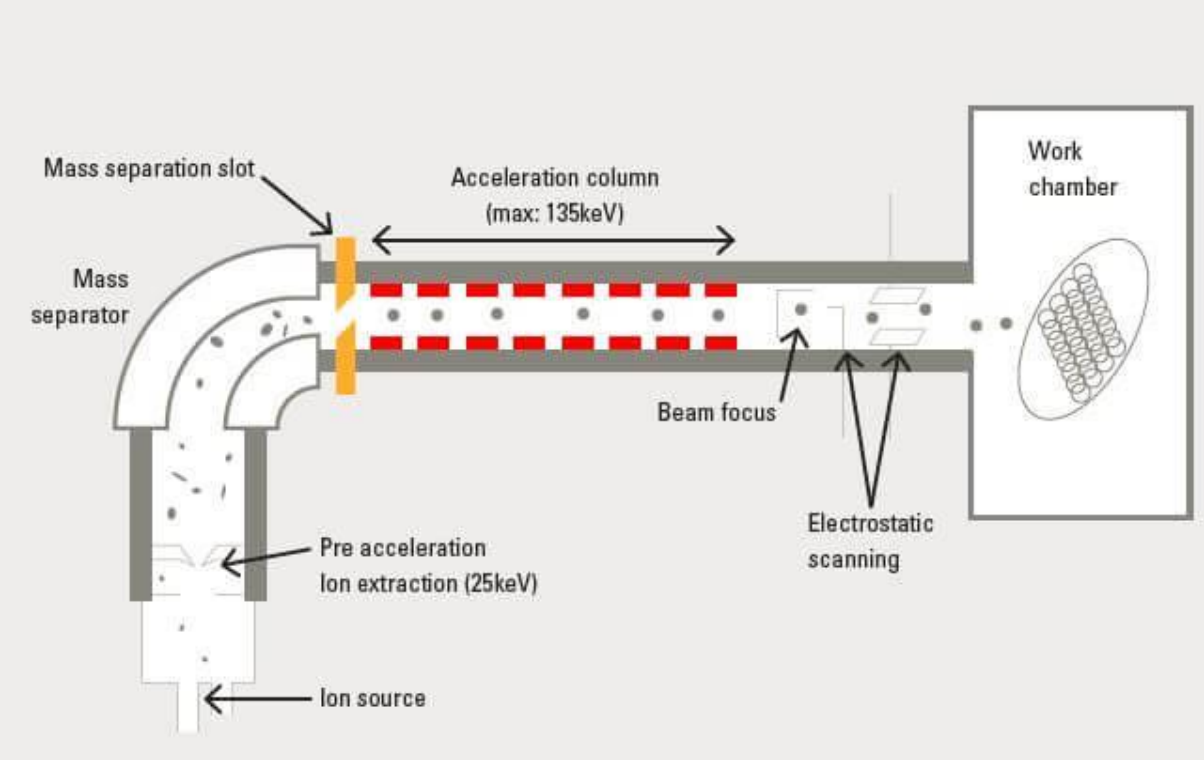


Figure:2.3 Schematic of the ion-implantation technology [13].

Plasma Enhanced Chemical Vapour Deposition:

Plasma Enhanced Chemical Vapour Deposition (PECVD) is commonly used to deposit a thin film of material from a gas state on a substrate as a solid-state. Passivating layers like a-Si and SiNX, which serve as anti-reflection coating and a capping layer for the hydrogenation treatment usually deposited through PECVD since it enables deposition at low temperature[14]. The machine chamber has two electrodes to create plasma when the Radiofrequency RF is on. To ignite the Plasma a highly energetic

field across the electrodes in both sides of the chamber is placed. For Silicon nitride deposition a mix of Silane and Ammonia gasses are existed as reactants to obtain the required six. In this work, we use this technology in order to deposit a thick SiNX layer to protect the rear side of the cell during texturing process. It is also used in order to passivate the front side of the cells with materials like a-Si and SiNX. A schematic sketch of the PECVD process is given in figure 2.4.

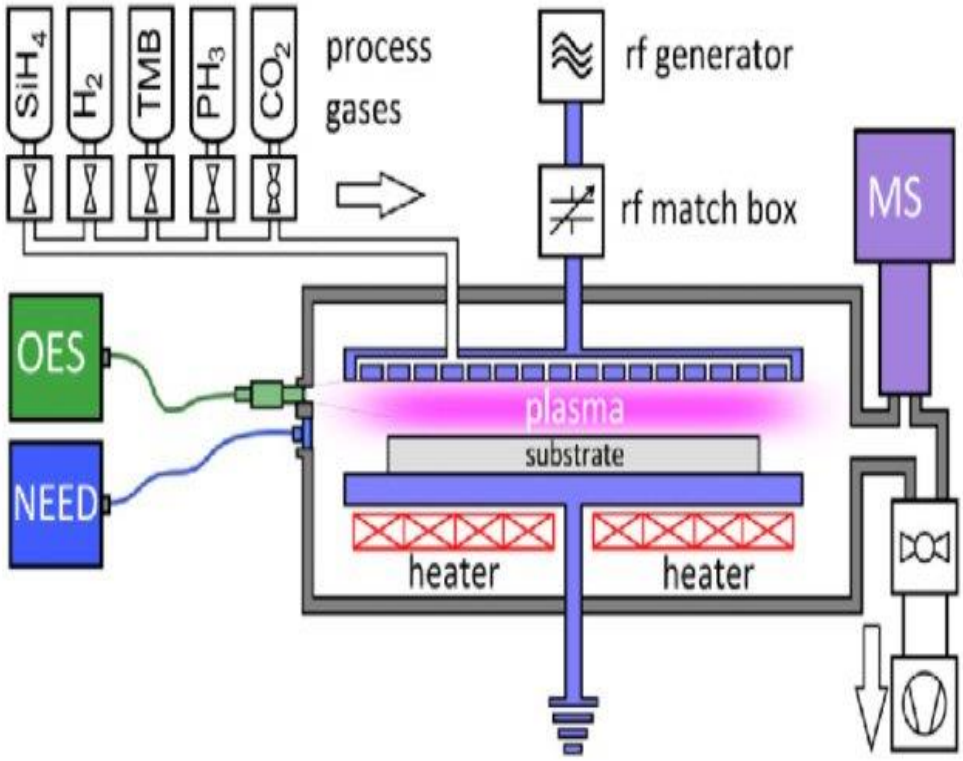


Figure 2.4 Scheme of the PECVD tool[15]

3

CARRIER SELECTIVE PASSIVATING CONTACT

In this chapter, the experimental details of fabricating and optimizing Carrier Selective Passivating Contacts (CSPC) are presented and explained. Firstly, the chemical passivation and the field-effect passivation are explained, then the influencing factors on each type are introduced and discussed. After that, the experimental process of the passivation test samples is detailed and sketched and followed by the results obtained at different annealing conditions. The Hydrogenation processes of FGA and SiN_X deposition used to enhance the passivation quality are introduced with the fabricating steps and followed by the passivation results discussion. Then the measurement steps of the contact resistivity used in this work are explained and the results are plotted for both the n^+ poly-Si and the p^+ poly-Si. Finally, the chapter concludes the results with a summary and the optimal findings to fabricate the poly-Si CSPC.

3.1 The passivation quality of poly-Si CSPC - a short review:

Carrier Selective Contacts can be made by several approaches such as introducing heavy doping region under the contacts, or by surface carrier modulation which is done by introducing a layer with large fixed charge density to function as an external potential source, or using a heterojunction between a silicon substrate and a wide bandgap material, etc.

The approach used to make Carrier Selective passivated Contacts in this work is to introduce an ultra-thin tunneling layer of thermal SiO_X (< 2 nm) as a tunneling layer with a heavily doped poly-Si for the emitter contact and the back surface field contact. There are different fabricating parameters of these layers that influence the surface recombination and the carrier's collectivity, which will be discussed, such as the parameters used in the growth of the t-SiO_X, the thickness of the poly-Si layers, the doping

dose for ion-implantation of poly-Si and the high-temperature annealing for activating/diffuse the dopants [16,17].

3.1.1 Chemical passivation:

Using SiO_X with doped poly-Si in the CSPCs plays an essential role to reduce the recombination current density, $J_{0,}$ and provide the required chemical and electric field passivation which leads to achieving a solar cell efficiency over 26% [18,19], The t-SiO_X layer has a chemical passivation function since it passivates the dangling bonds at the surface and minimizes the defect density at the c-Si/SiO_X interface. Silicon Oxide has another advantage to separate the doped poly-Si layer from the c-Si bulk and prevent the epitaxial growth of the poly-Si layer during the high-temperature annealing step[16]. The SiO_X layer can be formed in different ways such as using wet chemical oxidation like nitric acid [20,21] or by or UV/O_3 [16,23] or by dry thermal oxidation [16,22,23] as it is conducted in this work.

Silicon Oxide is a dielectric material; however, in the SiOx/doped poly-Si passivating contact structure, the charge carriers are transported from the c-Si to the poly-Si via two different transport mechanisms: tunneling, and through pin-holes as it provides direct pathways between the c-Si bulk and the poly-Si contacts [16,24]. The tunneling transport mechanism is effective and sufficient for ultra-thin SiO_X layer < 1.5 nm [24,25]. For thicker layer SiO_X (> 1.7 nm) the density of pin-holes in the oxide layer is vital and has to be optimized to achieve good conductivity, as insufficient pinholes density with poor tunneling transportation leads to high series resistivity (R_S) and poor solar cell fill factor (*FF*), while In the other hand too much transport through pin-holes (i.e when the possibility of transport through pinholes >10^{-3}) reduces the performance parameters of the solar cell such as *FF*, $V_{OC,}$ and J_{SC} significantly[24]. To conclude, the optimal thickness of the silicon oxide layer has to achieve an ideal balance between the carrier transportation and chemical passivation besides that the doped poly-Si/SiO_X stack has a positive impact to reduce the metallization-induced recombination[24].

3.1.2 Electric-field passivation:

Optimizing the Poly-Si layer has high importance to obtain an excellent passivation quality, therefore, many pieces of research were conducted to optimize its thickness, doping dose in case of ion implantation and the annealing temperature as these parameters together influence the doping profile of the n^+ and p^+ poly-Si passivating contacts since the field-effect passivation is based on this doping profile [21]. The doped poly-Si regions facilitate the electric field passivation by the band bending occurs at the poly-Si/SiO_X/c-Si interfaces as shown in figure (3.1). The formed high-doping regions decrease the conductivity and the mobility of the minority carriers as a result of reducing the equilibrium concentration of the minorities thanks to the introduced difference in chemical potential by the doping with respect to c-Si bulk. While in the other hand, the increase in the majority's concentration leads to an increase of the majority carrier conductivity consequently obtaining a low contact resistivity [26].

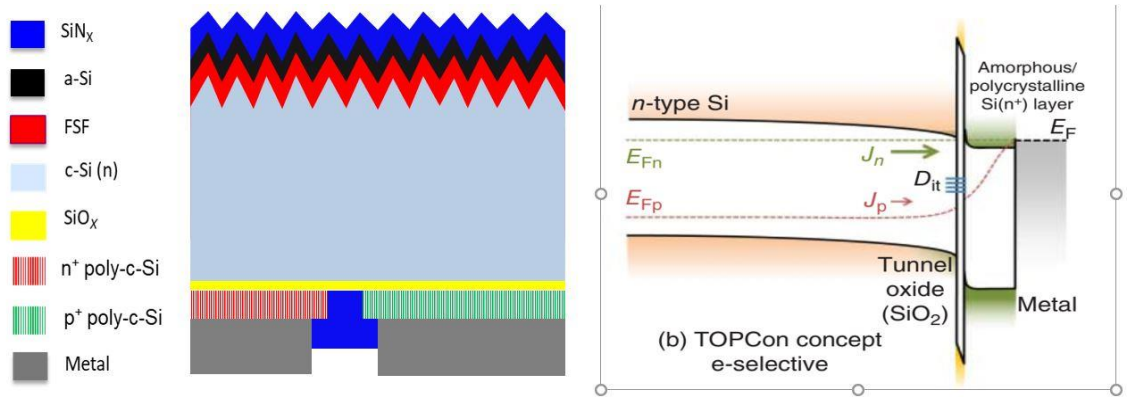


Figure 3.1: left: Schematic of a half-pitch IBC cell structure. Right: cell band diagram [36]

Generally, Electrochemical capacitance-voltage (ECV) is used to measure doping profiles in semiconductor layers where the measurement results show the carrier concentration and the profiling depth inside the materials [27]. The doping concentration increases with increasing the doping dose during the ion-implantation, and these implanted atoms will be activated and diffuse through the poly-Si in the annealing step at high temperatures. The annealing step is crucial to convert the deposited a-Si into poly-Si and to activate the dopants. This step is done usually in a furnace with a temperature range between 800 and 1050 °C. Besides the temperature parameters the annealing atmosphere also affects the passivation quality e.g., annealing in O_2 atmosphere shows better passivation results according to G. Yang et al. than annealing in a nitrogen one [21]. Figure (3.4) illustrates the doping profiles of phosphorous at fixed implantation energy and annealing conditions but for two different thicknesses of poly-Si. It is seen that for different thicknesses different minority carrier lifetime obtained and the maximum of 5.5ms obtained for 75 nm of poly-Si was prepared with an ion implantation dose of 2E15 cm^{-2} whereas, for a thicker layer of poly-Si like 250nm, a maximum lifetime of 8ms is obtained at a dose of 6E15 cm^{-2}. This behavior is attributed to the fact that the more migrated implanted atoms to the c-Si bulk the lower the passivation because of insufficient or no band bending at the interface of the poly-Si/c-Si. On the other hand, confining the majority of the dopants in the poly-Si region will lead to efficient field-effect passivation based on the strong established band bending at the poly-Si/c-Si interface.

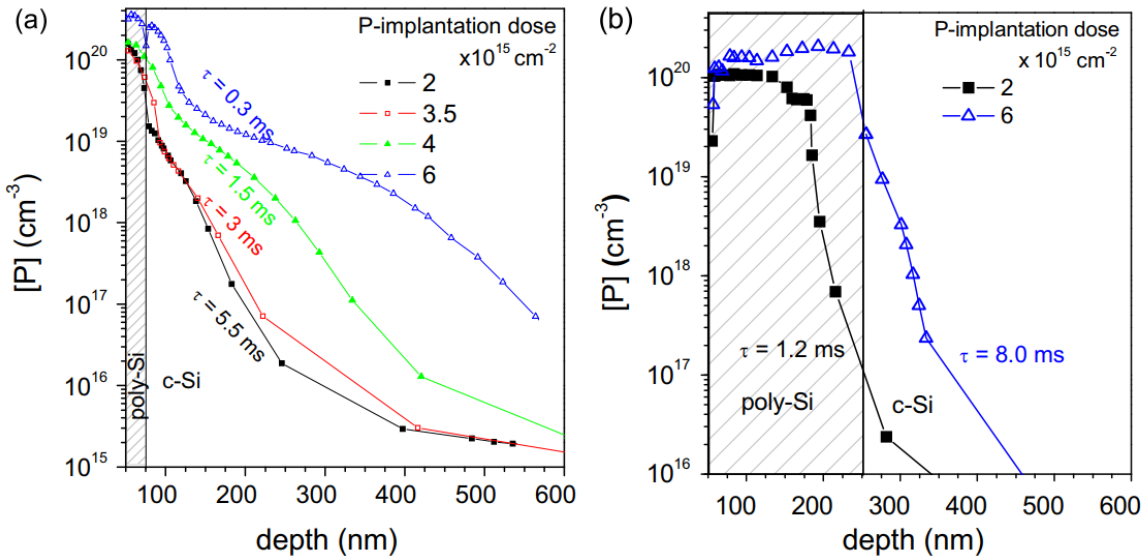


Figure 3.2: left: ECV measurement for P-doping profile for n^+ poly-Si passivating contacts with a thickness of 75 nm prepared with an implantation energy of 20 KeV but different doping dose, and annealed at 850°C for 90 min in N_2 at. Right: P-doping profile for poly-Si passivating contacts with a thickness of 250 nm prepared with an implantation energy of 20 KeV but different doping dose and annealed at 950°C for 5 min in N_2[21]

It is also important to give attention to the optical properties of the passivating material used in CSPC like SiO_X, Poly-Si, etc. Materials that have a close energy bandgap to c-Si like a-Si or poly-Si cause large absorption losses and lead to a decrease the J_{SC} and consequently the efficiency of the cell. Therefore, transparent passivating materials with wide-bandgap like SiN_X is stacked on AlO_X layer are usually used in the top side of the cell, whereas passivating materials with high absorption coefficients like poly-Si/SiO_X are used at the back side [26,28]. However heavily doped poly-Si result in a free-carrier absorption (FCA) nevertheless they are used in the rear side [28].

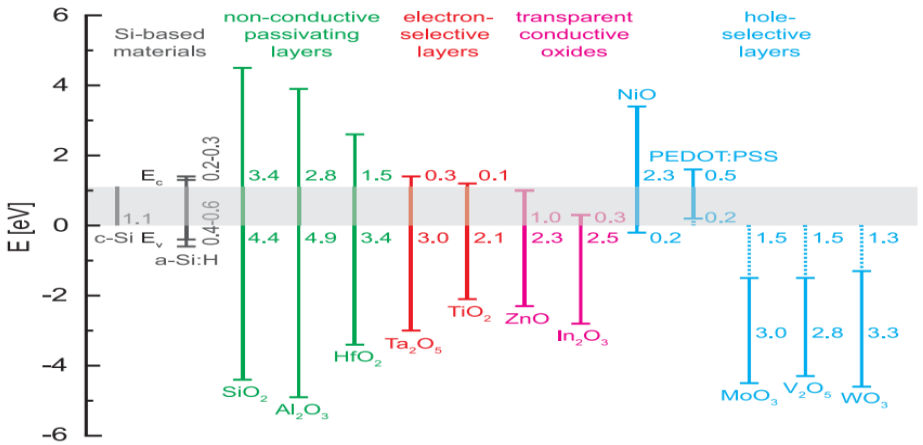


Figure 3.3: Conduction and valence band of various materials with respect to c-Si. [26]

3.2 Experimental details

This section aims to explain the fabrication process of the symmetrical samples that are used to measure the passivation quality of the poly-Si passivating contacts. The flowchart used is visualized for better understanding in Figure 3.4, and explained as follows:

The wafers used in this test are n-type float-zone (FZ) c-Si wafers, double-side polished with a thickness of 280 um and <100> oriented. Firstly, the wafers pass through a standard cleaning process to remove any contaminants, then the Marangoni cleaning process to remove the thin oxide layer on the silicon surface. The t-SiO_X is directly formed after Marangoni step by dry oxidation in the furnace at 675°C for three minutes, in an oxygen atmosphere. After that, a 250 nm thick intrinsic a-Si is deposited on both sides utilizing the Low-Pressure Chemical Vapor Deposition (LPCVD) technique. The next step is the ion implantation where Phosphorous and Boron are used to make the n^+ poly-Si and p^+ poly-Si layers with doping doses of 6e15 and 5e15(ions/cm^2) consequently at a fixed implantation energy of 20 KeV via Varian ion implanter E500HP. Another standard cleaning process is performed after the implantation to remove any contamination or impurities caused by the implanter.

The last step is the high-temperature annealing which is conducted at different temperatures and time duration to crystallize the amorphous silicon layers and activate the dopants to form the final n^+ poly-c-Si and p+ poly-c-Si passivating contacts. The annealing conditions used are 950 °C for 5 minutes, 1000 °C for 1 minute, and 1050 °C for 1 minute, and all samples are annealed in an O_2 atmosphere. It is worth mentioning that many optimized fabricating parameters such as doping dose, poly-Si thickness, etc. in this thesis project are token from previous projects at the PVMD group at TU-Delft, see table (3.1).

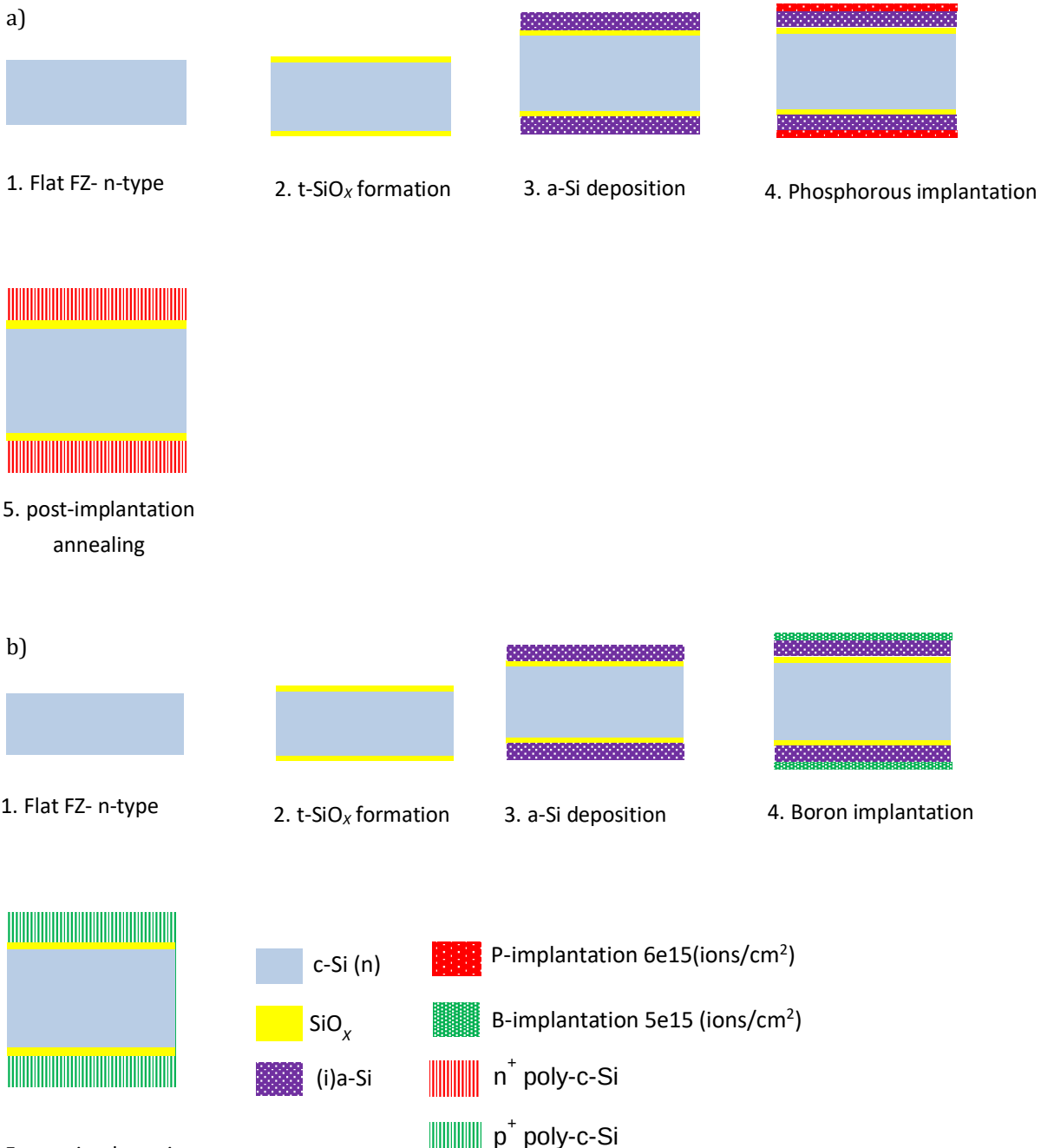


Figure 3.4: Schematic sketches of the steps used to process the passivation test samples: (a) n^+ poly-SiO_X test sample. (b) p^+ poly-SiO_X test samples.

Table 3.1 The, ion implantation parameters, and post-implantation annealing conditions [21] used for optimized the n-type and p-type poly-Si passivating contacts with NAOS SiO_X and different poly-Si thicknesses

Poly-Si			Implantation		Annealing/Oxidation			Passivation		
n-/p-type	Sample number	Thickness [nm]	Energy [keV]	Dose [$\times 10^{15}$ cm^{-2}]	Temperature [°C]	Time [min]	N_2/O_2	τ^b [ms]	J_0 [fA/cm^2]	iV_{OC} [mV]
n-type	1	70	~	~	850	90	N_2	0.03	1000	560
	2	75	20	2	850	90	N_2	5.5	9.5	706
	3	75	20	3.5	850	90	N_2	3	21.5	694
	4	75	20	4	850	90	N_2	1.5	51	684
	5	75	20	6	850	90	N_2	0.3	228	637
	6	250	20	2	950	5	N_2	1.2	48	679
	7	250	20	6	950	5	N_2	8	9	721
	8	**250**	**20**	**6**	**950**	**5**	**O_2^c**	**11.8**	**6**	**723**
p-type	12	200	5	5	950	5	N_2	1.8	25	695
	13	200	5	5	950	15	N_2	1.6	33	690
	14	200	5	5	950	30	N_2	1.1	65	677
	15	250	5	5	950	5	N_2	1.9	30	692
	16	**250**	**5**	**5**	**950**	**5**	**O_2^c**	**3.8**	**19**	**704**

3.3 the influence of annealing on the passivation quality

The best passivation quality achieved is 728mV for n^+ poly-Si contact at annealing conditions of (1050 °C for 1 minute) and 705mV for p^+ poly-Si contact at annealing condition of (950 °C for 5 minutes), whereas the p^+ poly-Si contact at (1050 °C for 1 minute) annealed condition has the lowest iV_{OC} with 6mV lower than the best p^+ poly-Si contact result obtained for the sample annealed at (950 °C for 5 minutes). However, the difference is greater than 60 mV for n^+ poly-Si contacts between the best and the lowest as a result of the differences between the doping profiles formed in each sample.

As all of the samples have the same chemical passivation layer. The difference in the passivation quality between the different samples annealed at different conditions is attributed mainly to the doping profile formed after the annealing step which did not provide a good field-effect passivation for the samples annealed at 950 °C for 5 minutes and at 1000°C for 1minute. Increasing the annealing temperature pushes the dopants to diffuse deeper in the c-Si surface as explained in section (3.1.2) which decreases the electrical field at the c-Si/SiOx/poly-Si interfaces and increases the Auger recombination at the c-Si surface. Thus, a balance should be found between the doping dose, the poly-Si thickness, and the annealing conditions to obtain the optimum doping profile for achieving the best field-effect passivation. It is noticeable that the passivation quality of the p^+ poly-Si contacts samples shows slighter variation than the n-type contacts samples. An ECV measurement would be very effective to analyze the doping profiles formed to evaluate the field-effect passivation at each annealing condition, however, this measurement was not available at the time of the project.

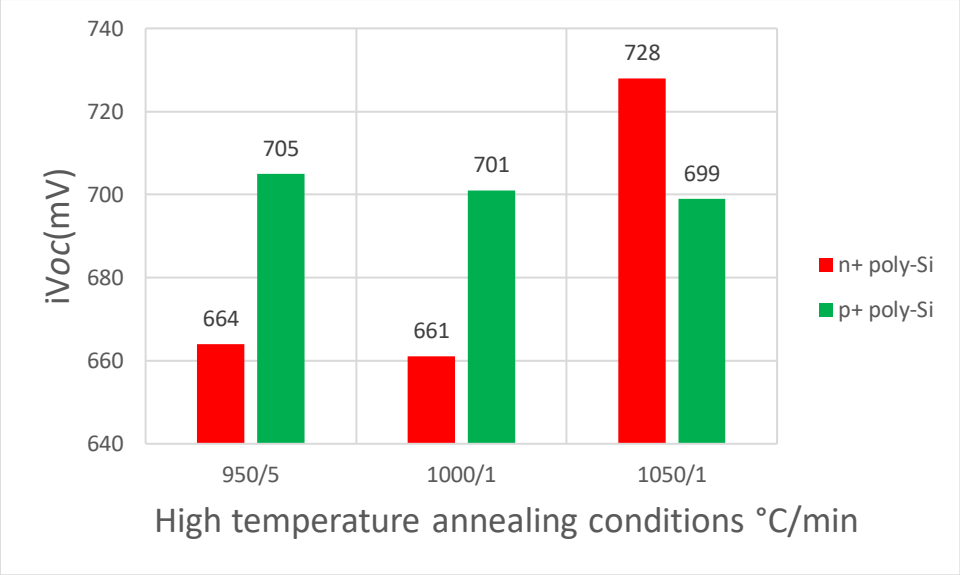


Figure 3.5: Passivation properties of symmetrical (n^+) poly-Si samples and (p^+) poly-Si samples after different annealing conditions.

3.4 The influence of hydrogenation on the passivation quality

In this section, the principles behind the hydrogenation processes that are used to enhance the passivation quality will be explained and the previously optimized fabrication parameters that influence the hydrogenation properties will be introduced and discussed. After that a schematic sketch of the symmetrical samples are used in the tests will be given and followed by the results of the hydrogenated p^+-poly-Si and the n^+-poly-Si contacts.

The hydrogen atoms included in a rich hydrogen content layer or available in the furnace atmosphere during a hydrogenating annealing step have a significant effect to increase the chemical passivation quality. Therefore, it can increase the iV_{OC} and the minority carrier's lifetime [29,30,31]. The deposited SiN_X layer can be considered as a hydrogen donor layer and the FGA step enables the Hydrogen atoms to diffuse in and passivate the dangling bonds of the silicon atoms at the c-Si surface that present trap states within the bandgap of the silicon at the bulk surface which could not be passivated by the SiO_X layer [32,33]. In this thesis work, to obtain the maximum passivation enhancement through hydrogenation, two processes are generally done. Firstly, the hydrogenation process through low-temperature annealing step in a furnace with a mixture of hydrogen and nitrogen atmosphere gases, at 400 °C for 30 minutes, which is normally referred to as forming gas annealing (FGA). after that, a capping layer of SiN_X has deposited through plasma enhanced chemical deposition (PECVD) technology, followed by another FGA step.

The samples used in this test are the same samples used to measure the passivation quality of the p^+ -poly-Si contacts and the n^+-poly-Si contacts after the high-temperature annealing step. The samples then enter the furnace for 30 minutes at 400 °C where these parameters are already optimized in previous work at the group and show that the temperature is of significant importance as increasing the annealing temperature result in a decrease in the measured iV_{OC}. This reduction is attributed to the diffused hydrogen from the capping layer, it is also shown that increasing the annealing temperature to exceed the one used in the t-SiO_X growth 700°C e.g. result in a dramatic decline in the iV_{OC}. The reported results for different annealing times show that the annealing time duration has almost no influence on the iV_{OC}, therefore it is decided to do the annealing at 400°C for 30 minutes which gives the highest obtained passivation quality [34]. After the FGA treatment, a 75 nm of SiN_X is deposited via (PECVD) at 400°C as well and followed with another FGA step as mentioned before.

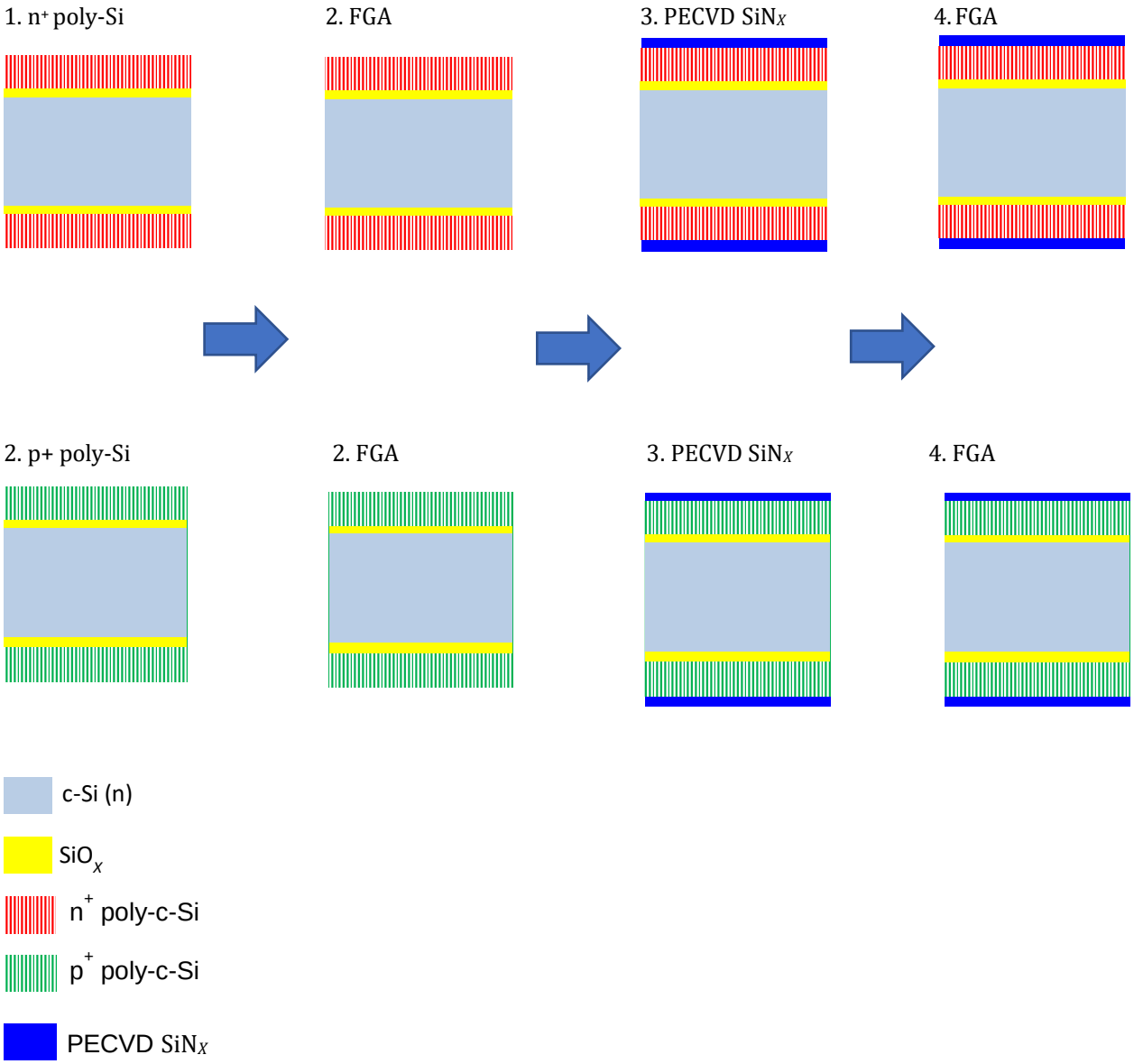


Figure 3.7: Schematic sketches of the hydrogenation treatment steps applied for n^+ poly-SiO_X test samples and p^+ poly-SiO_X test samples.

3.4.1 Hydrogenation tests results:

In the following figures the output passivation values for n^+ poly-SiO_X test samples and p^+ poly-SiO_X test samples which are sketched in figure 3.7, after the different hydrogenation steps are plotted.

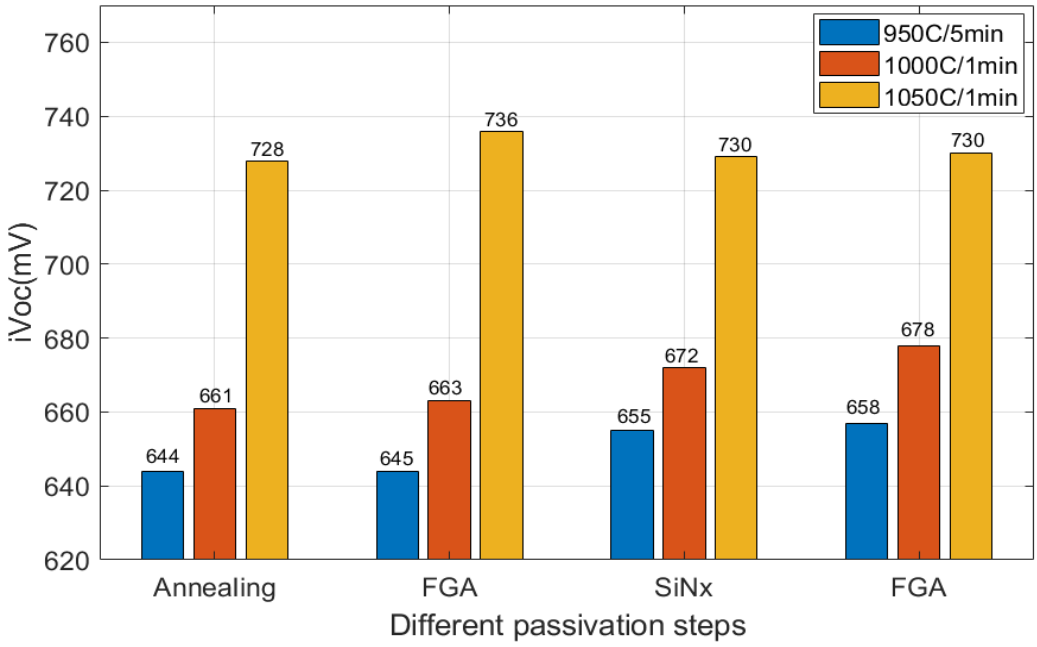


Figure 3.8: The passivation qualities of n^+ poly-Si test samples prepared with different annealing conditions (950°C/5min,1000°C/1min, 1050°C/1min) as a function of the hydrogenation steps.

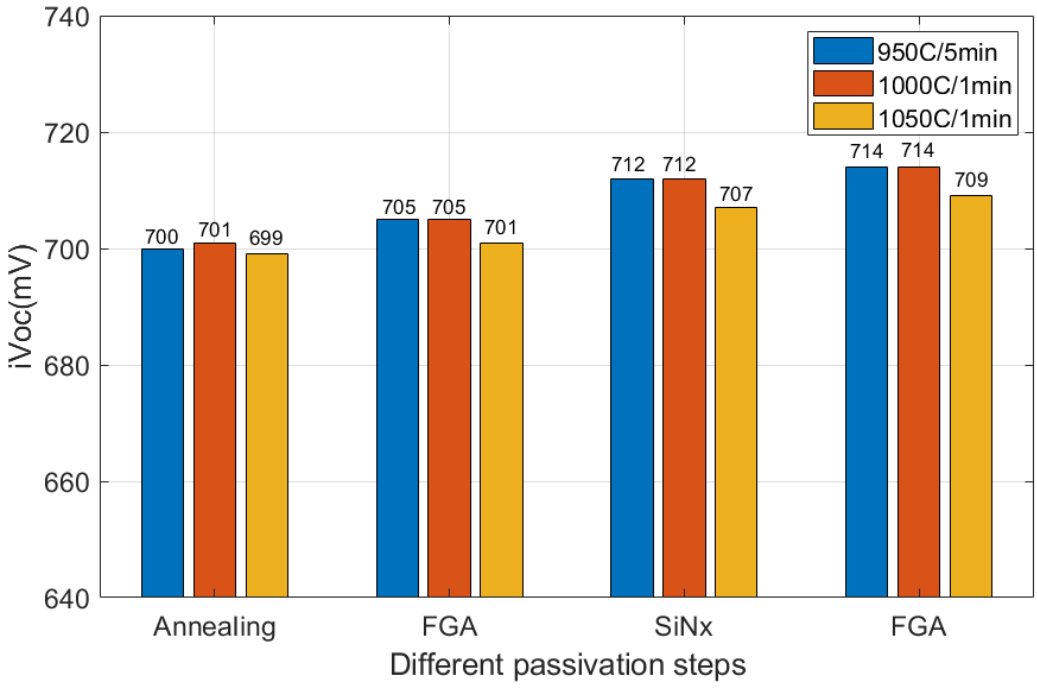


Figure 3.9 The passivation qualities of p^+ poly-Si test samples prepared with different annealing conditions (950°C/5min,1000°C/1min, 1050°C/1min) as a function of the hydrogenation steps.

The results shown in figure (3.8) illustrate that the hydrogenation treatment generally was not effective to enhance the passivation quality for the samples annealed at (950°C/5min and 1000°C/1min) to exceed the 700mV for the n^+ poly-SiO_X test samples. The passivation quality of the n^+ sample of the wafers annealed at 950°C/5min and 1000°C/1 min gradually enhanced through the SiN_X deposition and the second FGA step, whereas both of them show no change in iV_{OC} after the first FGA step. These results indicate that there was not enough hydrogen diffusion to passivate the trap states at SiO_X/c-Si interface which leading to slight passivation quality changes. After the SiN_X deposition both of them show an increase of around 10 mV in the iV_{OC} value as a result of the improvement in the chemical passivation, in the other hand the wafer annealed at 1050°C/1min shows 8mV increase in the iV_{OC} in by the first FGA step but negatively affected by the next two hydrogenation steps to reach at the end 730mV, this reduction can be caused by eventual contamination through the hydrogenation processes and needs further investigation.

The results of p^+ poly-Si visualized in figure (3.9) show a gradual improvement for all the samples as a result of the chemical passivation, the best passivation obtained is 714mV for samples that are annealed at (950°C/5min and 1000°C/1min), Whereas the sample annealed at 1050°C/1min reach 709mV.

The hydrogenation findings out of this work show that the samples annealed at 1050°C/1min are the best candidate to fabricate the aimed IBC solar cells yet. However, the passivation quality obtained can be further optimized by conducting more tests with different fabricating parameters in terms of poly-Si thicknesses and the doping dose of the ion implantation.

3.5 Contact resistivity:

Generally, the quality of the passivating contacts in c-Si solar cells is defined by the passivation quality which is evaluated usually by J_0 or iV_{OC}. The influence of such contacts on the solar cells' series resistance can be evaluated by measuring their contact resistivity, ρ_C. For high conversion efficiency solar cells, it comes of significant importance to reduce both parameters J_0 and ρ_C simultaneously for increasing the carrier selectivity. This will reduce the minority's conductivity thus reducing J_0, and raise the majority carrier's conductivity to minimize ρ_C at the same time [26].

3.5.1 Transfer Length Measurement (TLM) and samples preparation:

To conduct the TLM measurement we fabricated symmetrical samples as shown in figure (3.10). The sample preparation follows the same process as the samples are fabricated for the passivation test, see section3.2. The same t-SiO_X growth condition (675°C/3min) is used and the same deposition

parameters for the poly-Si of 250nm and implantation dose of 6e15(ions/cm2) for the P-doping and 5e15 (ions/cm2) for B-doping at a fixed implantation energy of 20keV, after that the samples divided to three groups to be annealed at three different annealing conditions (950°C/5min, 1000°C/1min and, 1050°C/1min) similar to the conditions used for the passivation test. The following process is metallization which is done by depositing 2um of Aluminum by e-beam evaporation technique using a hard musk to obtain metallic fingers with different spacing. A p-type bulk is used to measure the contact resistivity for the p^+poly-Si contacts to avoid the formation of a p-n junction that blocks the carrier's transportation through the t-SiO_X.

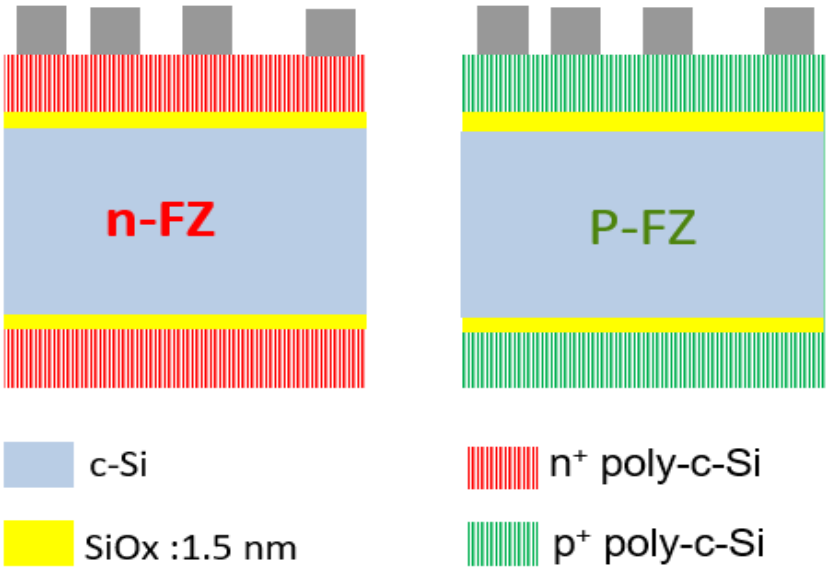


Figure 3.10: Schematic of the TLM sample to measure the resistivity of n^+-poly-Si and p^+-poly-Si

Table (3.2) metal pads geometry

Metal pad	width (um)	Length(um)
	250	1000
Spacing parameters	Metal pad label	Space(um)
	D1	650
	D2	100
	D3	1550
	D4	2000
	D5	2450
	D6	2900
	D7	3350

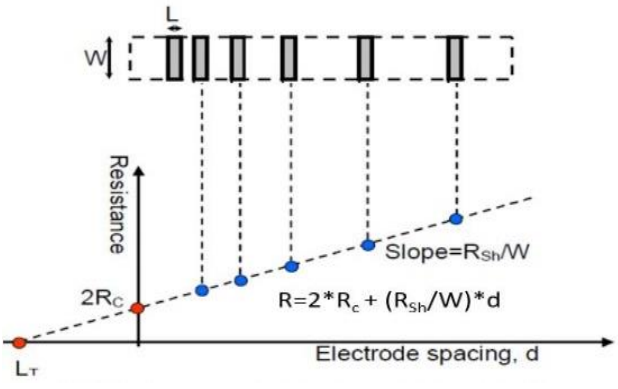


Figure 3.11: Illustration diagram of the TLM method.

The resistance is measured between each metal pad and the pad next to it, then the results are plotted against the spacing detailed in the table (3.2) to calculate R_C value which is twice the value of the intercept at the Y-axis, see figure (3.11) after that value calculated is used to find the contact resistivity ρ_C ($m\Omega.cm^2$)

The results presented in figure (3.12) show that p^+-poly-Si contacts have higher resistivity than n^+-poly-Si contacts, while the main finding is that increasing the annealing temperature from 950°C to 1050°C almost decrease the contact resistivity to the half for both p^+ and n^+ contacts. However, the minimum contact resistivity obtained was 13.5($m\Omega.cm^2$) for n^+ with an annealing condition of(1050°C/1min) which is still high compared to results achieved by using NAOS SiO_X instead of t-SiO_X [35]. The difference in the conductivity between the NAOS SiO_X and the t-SiO_X is attributed to the fact that t-SiO_X has a higher density than NAOS SiO_X thus the charge transport mechanisms through tunneling and pinholes in NAOS is more efficient. Our findings are consistent with the conclusion obtained by Z. Zhang et al [24]. that increasing the annealing temperature leads to form more pinholes thus, enable lower Rc. It worth to mention the structure of the samples used in the contact resistivity measurement is not 100% accurate, since part of the current will flow through the poly-Si layer. To obtain accurate contact resistivity of the poly-Si/bulk the poly-Si layer between the metals pad should be etched. For this project, the performed measurement gives acceptable results to indicate the influence of annealing temperature on the contact resistivity values.

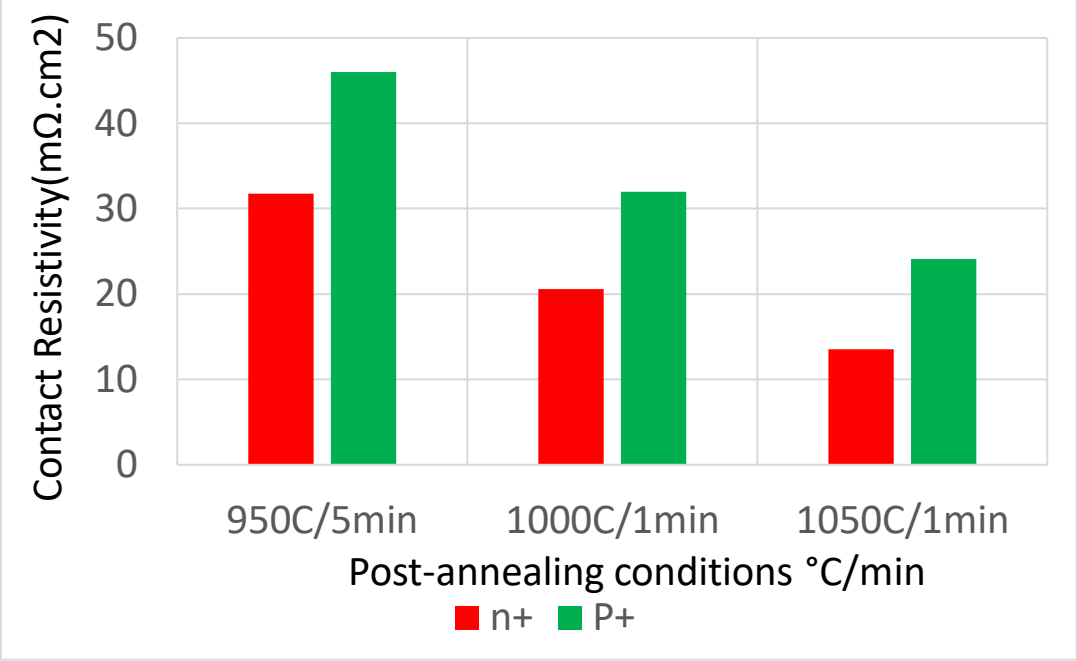


Figure 3.12: Contact resistivity values of Al/ doped poly-Si /t-SiO_X / c-Si at different annealing conditions in terms of temperature and duration.

3.6 Summary:

Initially, the fabricated test samples aim to optimize the n^+-poly-Si and p^+-poly-Si contacts' structure to enable effective field-effect passivation associated with chemical passivation from the deposited SiN_X and the FGA treatment. Three annealing conditions are tested: 950°C/5min,1000°C/1min, and 1050°C/1min, the sample annealed at 1050°C/1min condition show the best passivation quality for n^+-poly-Si contact. For p^+ samples, all samples show close values for the passivation quality with a slight advantage to the sample annealed at 950° for 5 minutes. After that hydrogenation, tests are carried out and all the tested samples show a gradual enhancement in terms of the passivation quality since hydrogen effectively saturates the dangling bond of the silicon atoms at the interface. The best-obtained iV_{OC} after the hydrogenation process are 730 and 709 mV for n^+ and p^+ contacts respectively for the wafer with post-implantation annealing condition of 1050°C/1min.

To evaluate the quality of the poly-Si contact for different annealing conditions, TLM measurement is carried out for both n^+ and p^+ contacts. The observed results show a decrease in the contacts' resistivity when increasing the annealing temperature since the high temperature forms more pinholes that improve the carrier transportation.

4

FRONT BACK CONTACTED SOLAR CELLS

In this chapter, the same fabricating parameters used in the symmetrical passivation tests are used to fabricate Front Back contacted solar cells (FBC) solar cells to evaluate the performance of the optimized poly-Si CSPCs in a simple structure before utilizing them in the complex IBC solar cell's structure. On the FBC cells, Suns-V_{OC} measurement is carried out and is followed by I-V measurement to characterize the external solar cell's parameters. The influence of different annealing conditions on the passivation quality is investigated and the difference between the pseudo fill factor and the fill factor is discussed. Silver and Aluminum as rear metal contacts are utilized respectively and the effect of the post-metallization annealing treatment is evaluated after the Aluminum deposition.

4.1 Experimental details:

The goal of FBC solar cells is to test the electrical performance of the optimized poly-Si passivating contacts with the fabricating parameters discussed in chapter 3, before using them in the fabrication of interdigitated back contacted solar cells (IBC), due to the simplicity of the flowchart of the FBC cells.

For this process n-type float-zone (FZ) c-Si wafers, double-side polished with a thickness of 280 um and <100> oriented are used as a bulk. Firstly, the new wafers are subjected to cleaning processes of standard cleaning and Marangoni cleaning process in HF to remove any contamination and avoid native oxide formation before the aimed thermal silicon oxide growth. After that, the wafers entered the furnace at 675°C to form the dry thermal oxidation tunneling layer on both surfaces for a time duration of three minutes. The step after that is to deposit a thick layer of 250nm of intrinsic a-Si on both sides by means of Low-Pressure Chemical Vapor Deposition (LPCVD) technique which takes 113 minutes as a deposition time while the whole process needs a few hours, then the wafers are ready for the ion implantation where the Phosphorous doped side forms the n^+-poly-Si contact at the front side while the Boron doped side forms the p^+-poly-Si contact at the rear side. The implantation parameters used are 6e15 and 5e15(ions/cm^2) for Phosphorous and Boron consequently at a fixed implantation energy of 20 KeV which are the same implantation parameters used in fabricating the

passivation quality test samples used in chapter 3. Post-implantation annealing step is carried out at three different time/temperature conditions of (950°C /5min,1000°C /1min and 1050°C /1min) to enable the a-Si conversion to poly-Si and activate the dopants, then two hydrogenation treatments are conducted, first, a deposition of SiN_X of 75nm by PECVD on both sides and followed with FGA at 400°C for 30 minutes. The wafer was then immersed in a BHF bath to remove the SiN_X layer to prepare for the metallization deposition, where photolithography and lift-off process was utilized to form the front metallization grid and the rear contacts with help of the e-beam evaporation technology (PROVAC)to deposit 1 um of Silver on the top and 2 um on the rear side of the cell to form the front and back contacts.For the front side of the cell, the mask used to define the metallization geometry of the cell is shown in figure (4.1), the mask has four sizes of cells with different metallization cover percentage as detailed in table (4.1)

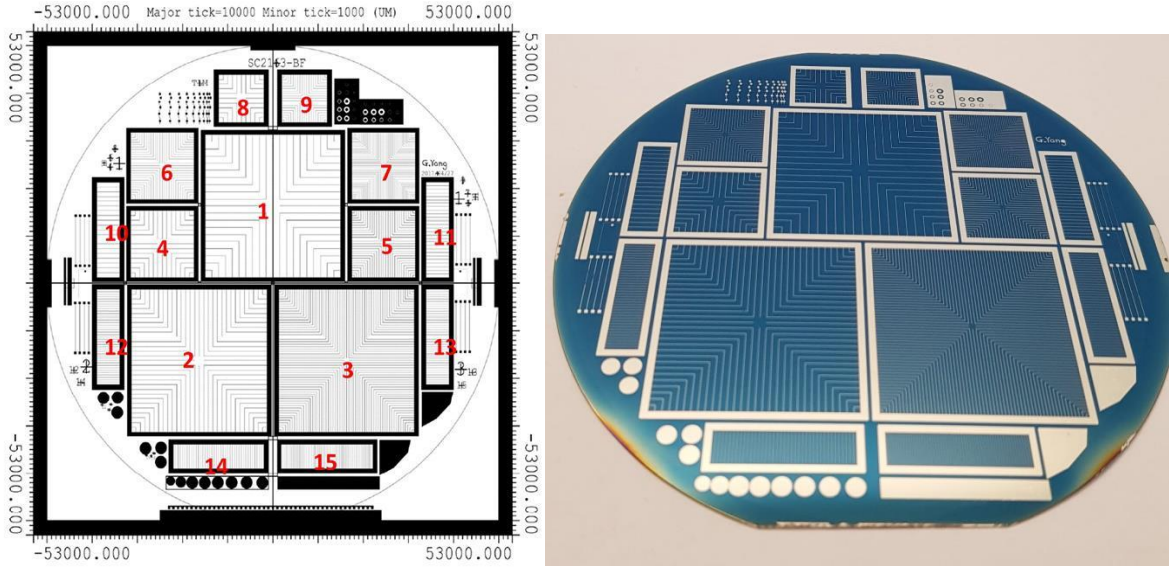


Figure 4.1 the mask used for the front side of the wafer and the wafer fabricated by this musk.

Table (4.1) Geometry specification of the lithography mask used to prepare metal grids for FBC cells

Cell number	Area(cm2)	Number of fingers	Metal coverage (%)
1	8.96	9	1.93
2	8.96	14	2.96
3	8.96	29	6.02
4	1.96	6	2.76
5	1.96	13	5.88
6	1.96	13	2.74
7	1.96	19	3.96
8	1	4	2.52
9	1	9	2.69
10	1	19	2.38
11	1	26	3.25
12	1	39	4.88
13	1	39	3.90
14	1	39	2.93
15	1	53	4.08

4.2 Cells' precursor performances:

Three wafers are fabricated according to the details explained in section 3.2, where the only difference between them is the post-implantation annealing conditions to prove our result on the quality of the passivating contact obtained in chapter 3. The iV_{OC} and *iFF* for the cell's precursors measurement are carried out by Sinton WCT-120 after the hydrogenation step. The plotted results in figure 4.2 show that the iV_{OC} values are in the range between 711 and 719mV where the iV_{OC} increases when the temperature of the post-annealing increases, which is consistent with our passivation quality tests performed in chapter 3, see figure (4.2).

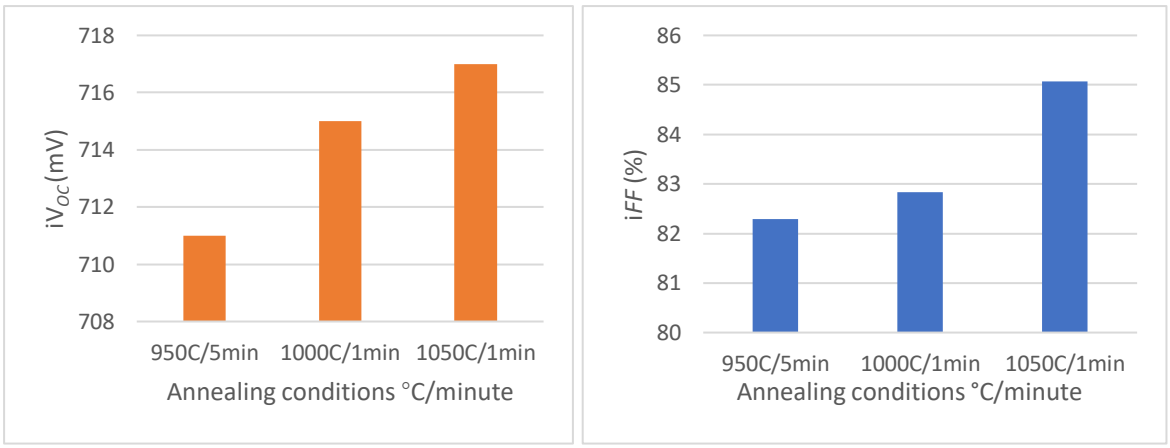


Figure (4.2) Passivation quality of the cell's precursor (iV_{OC} and *iFF*).

4.3 Suns-V_{OC} measurement:

Suns-V_{OC} measurement is also performed after the fabrication of the cells to compare it with V_{OC} results and evaluate the series resistance, see Figure (4.3) and (4.4). Firstly, Suns-V_{OC} measurement is carried out to make advantage of estimating the maximum V_{OC} and *FF* since this measurement excludes the effect of the series resistance, thus the difference between *pFF and -FF* represents a good indicator of the carrier transportation quality in terms of the series resistance [37]. Figures (4.3) and (4.4) illustrate the results obtained for cells 1, 2, and 3, and compare them to the same cells of the other wafers with the same metal gird fraction but annealed at different conditions. The output of the measurement shows that the highest Suns-V_{OC} obtained is 718 mV for cell number 3 annealed at

1050°C/1min condition whereas for the same cell at annealing condition of 950°C/5min it reaches 710 mV, the minimal value obtained was 708 mV for cell number 2 annealed at 950°C/5min. The outcomes show increasing in the Suns-V_{OC} by raising the annealing temperature which is consistent with the passivation quality test result performed in chapter 3. The pseudo fill factor measured reaches 83.1% for the cell number 2 annealed at 1050°C/1min while the lowest value was 80.5% for the cell number 1 annealed at 950°C/1min condition. It is noticeable that cells annealed at 950°C/5min and 1000°C/1min conditions have very close results while the samples annealed at 1050°C/1min show the best outcome and the maximum ΔFF does not exceed 3% between the top and lowest obtained p*FF* which is also consistent with the result of i*FF* of the cell's precursors shown in figure (4.2).

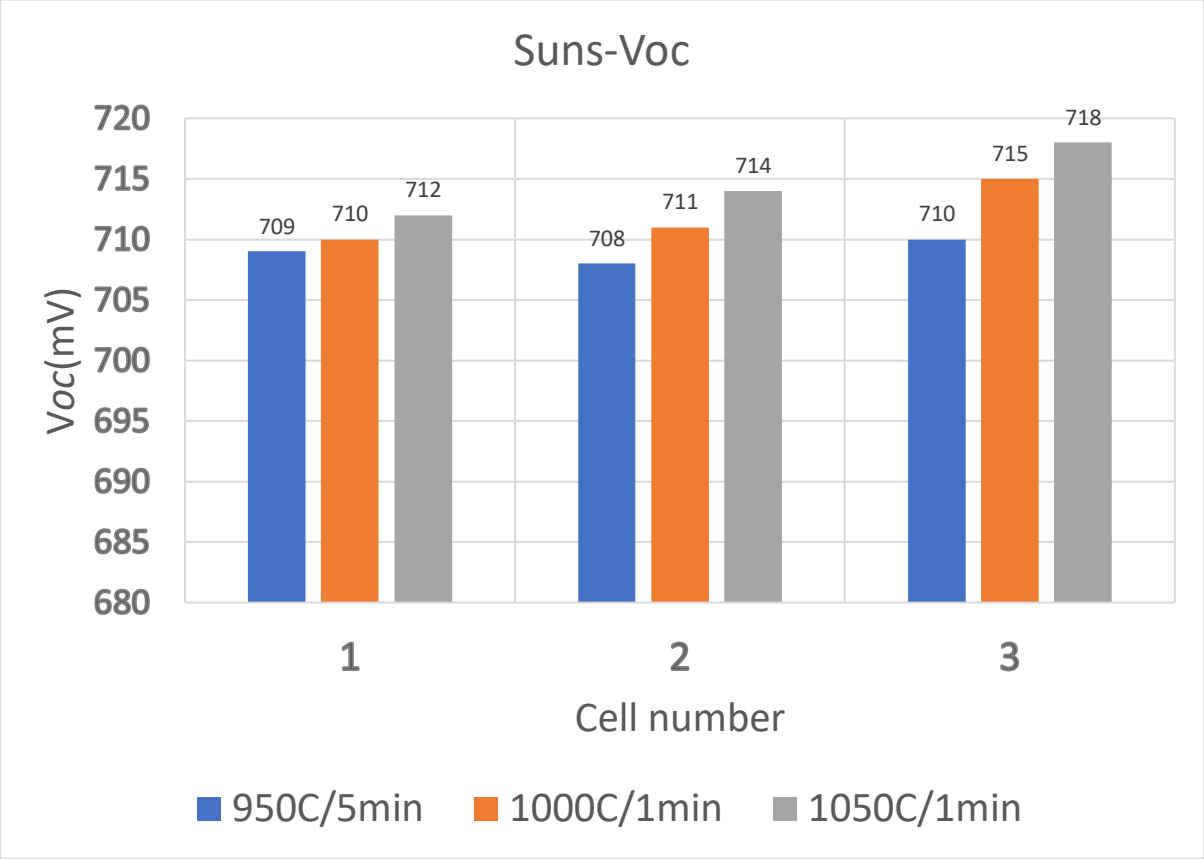


Figure (4.3) results of Suns-V_{OC} measurement, the V_{OC} for cells number(1,2,3) from three wafers annealed at different conditions(950°C/5min, 1000°C/1min, and 1050°C/1min).

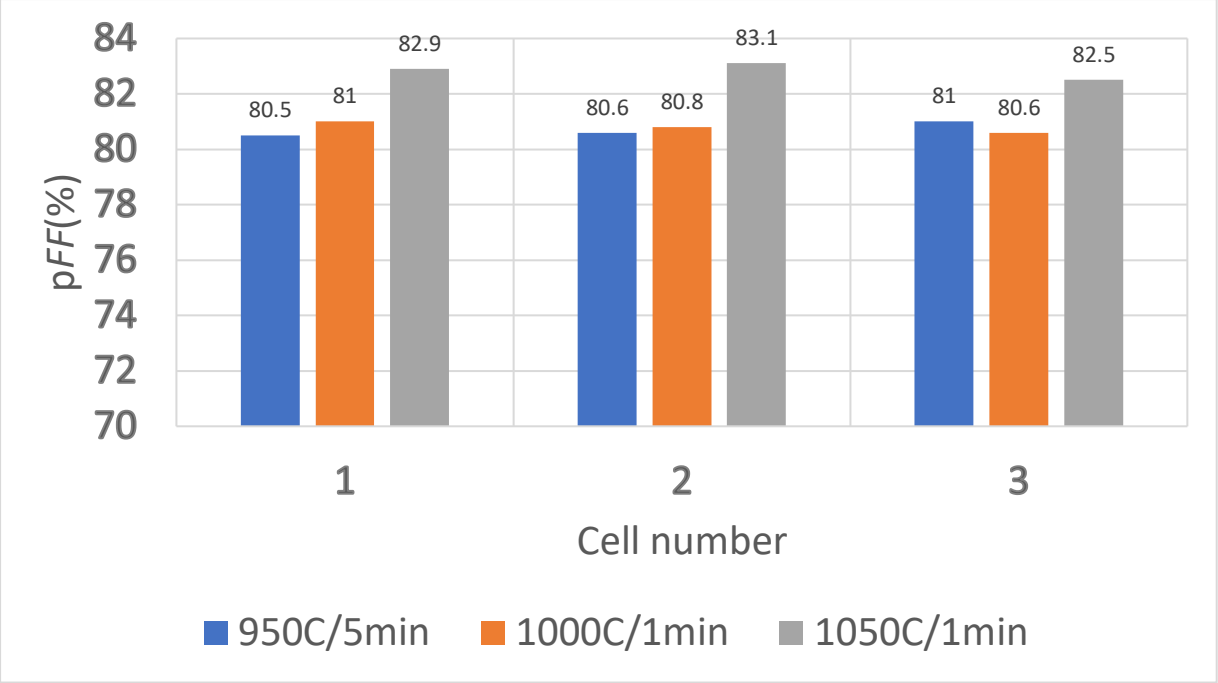


Figure (4.4) results of Suns-V_{OC} measurement, the p*FF* for cells number(1,2,3) from three wafers annealed at different conditions(950°C/5min, 1000°C/1min, and 1050°C/1min).

4.4 I-V measurement:

The next step was to measure the J-V curve to characterize the V_{OC} and the *FF* of the fabricated cells with Silver back contacts, the output is plotted in figures (4.5) and (4.6) consequently. The results obtained of V_{OC} values in a trend similar to the Suns-V_{OC} measurement. 706 mV of cell number 3 annealed at 1050°C/1min condition is the highest V_{OC} achieved whereas cells annealed at 950°C/5min and 1000°C/1minconditions record 702,704 mV consequently. Cells number 3 have a higher metal cover percentage than cells number 2 and 1 thus they have higher *FF* due to lower series resistance. Surprisingly, Cells number 3 also show higher V_{OC} even though they have higher metal coverage which causes more shading, but the result shows that they have higher J*sc* which can be attributed to more light absorption due to none-ideal coverage of the rest cells during the measurement since we cover the rest cells manually by black paper. However, designing the metal grid has an important influence on both *FF* and V_{OC} as many factors compete with each other,i.e increasing the metal width reduces the series resistance but on the other hand, it increases the shading, therefore, an optimal has to be found to achieve the highest conversion efficiency [6].

Comparing the values are obtained for the fill factor which is in the range between 56% and 64%, with the pseudo fill factor which is over 80%. A huge reduction in the fill factor is observed which indicates a large series resistance that hinders the current flow from the bulk to the metal contacts. The resistivity between the metals and the poly-Si is part of this resistance, remark was made by another

work in the group about poor adhesion of the thermally evaporated silver and the poly-Si [34]. Therefore, it is decided to remove the Silver and deposit Aluminium as rear contacts to determine the reason behind this large difference between p*FF* and *FF*. This process of removing the rear contacts metal by tape causes a drop in the measured V_{OC} and *FF* when carrying out the measurement again after the Aluminum deposition in place of the Silver, see figures (4.7) and (4.8). This reduction indicates degradation in the passivation due to performing more fabricating processes especially removing the Silver. The Fill factor values have also witnessed a drop in their values indicating that the large series resistance is not because of the resistance between the metals and the poly-Si. Observing the condition of forming the t-SiO_X, the aimed conditions to form the oxid is at 675°C for three minutes. The starting temperature of the recipe in the furnace is at 600°C, but the temperature can also be at 800°C depending on the previously used recipe in the furnace. The increasing of the starting temperature will lead to an increase in the thickness of the formed t-SiO_X and cause that large series resistance since SiO_X is a dielectric material. This conclusion is supported by the findings of Z. Zhang et al [24]. where they show that increasing the thickness of the t-SiO_X from 1.6 to 1.7 nm cause an increase in the contact resistivity by several orders of magnitude. The thick layer of t-SiO_X hinders the tunneling of the carriers from the bulk to the contact and causes a large reduction in the cell's fill factor.

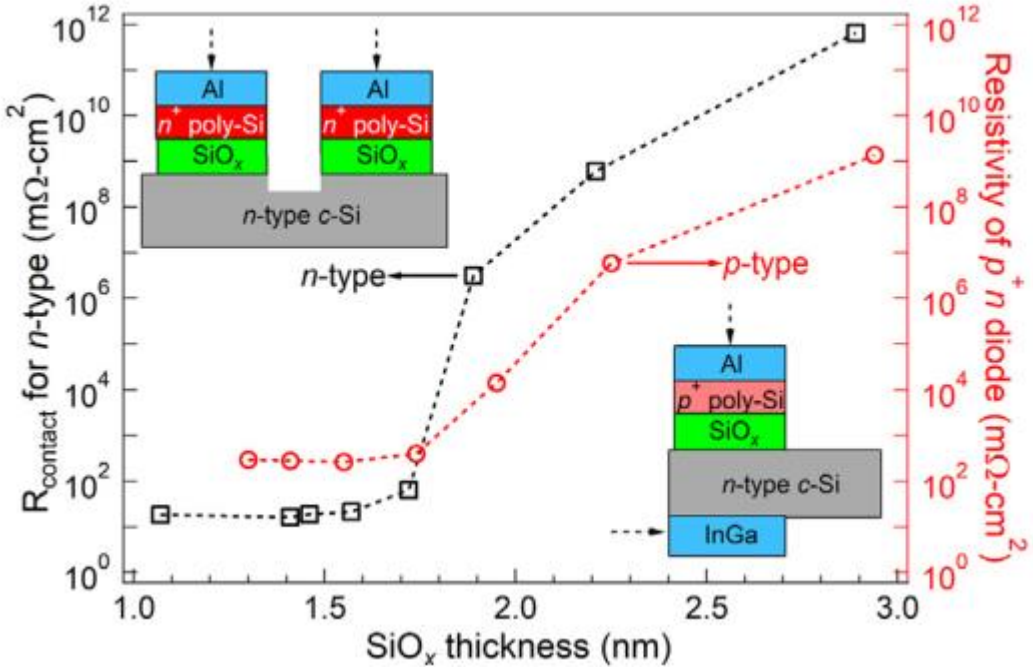


Figure 4.5: The effect of the t-SiOx thickness on the through contact resistivity of n^+ the contact (left axis), and p+n diode resistivity of the p^+ contact (right axis), on n-type c-Si wafer[24].

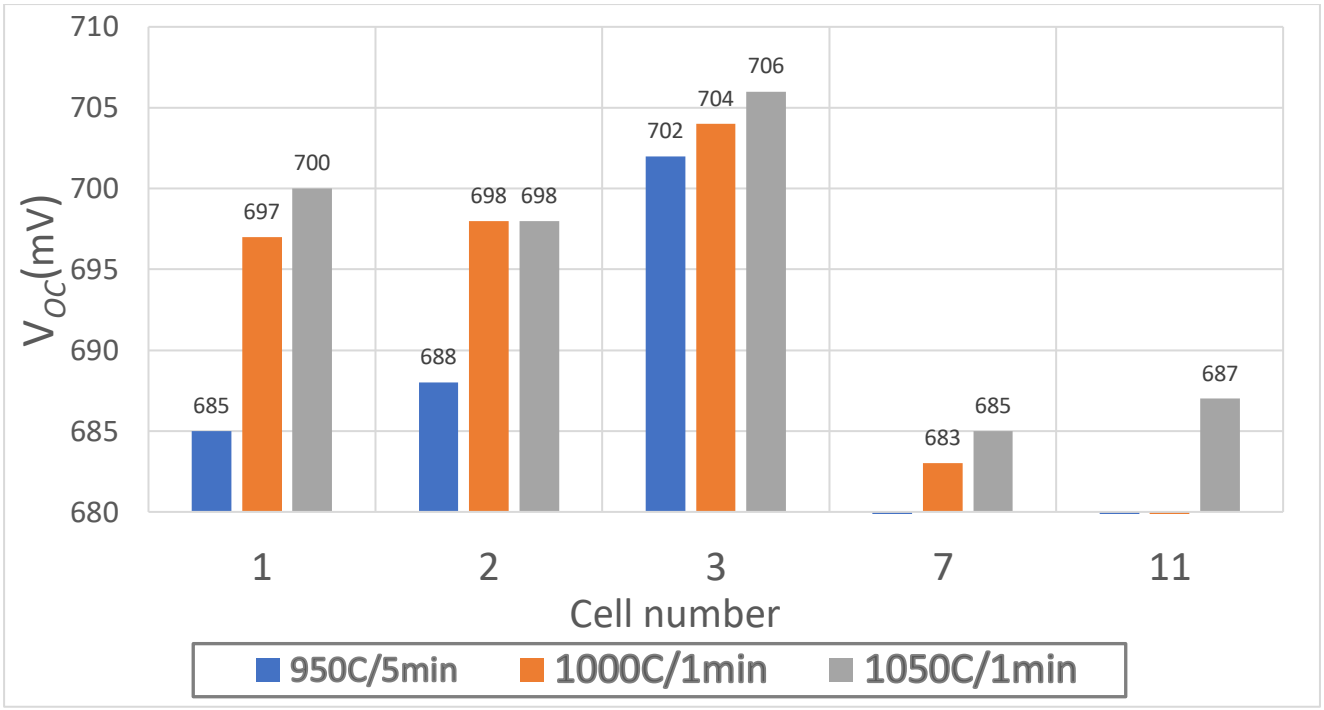


Figure (4.6) V_{OC} values obtained with I-V characterization for cells number(1,2,3) with Silver contacts at three different high-temperature annealing conditions of (950°C/5min, 1000°C/1min, and 1050°C/1min).

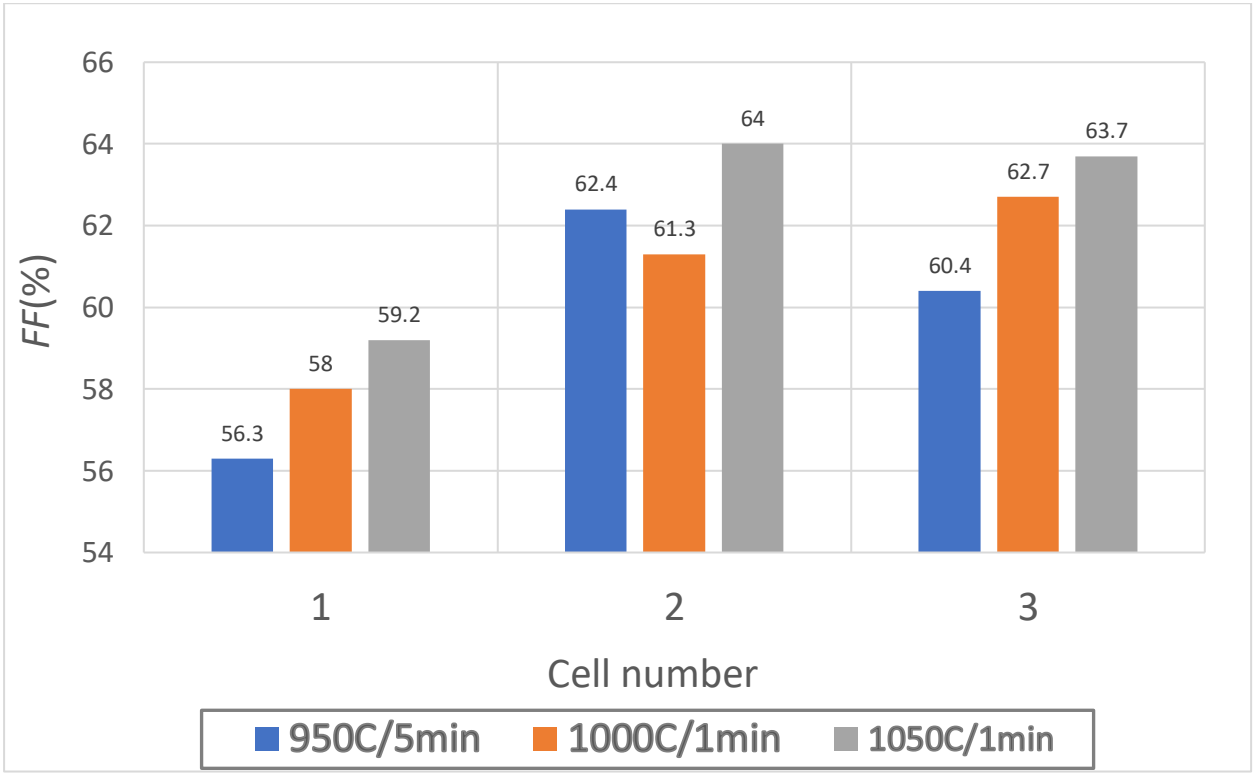


Figure (4.7) *FF* values obtained with I-V characterization for cells number(1,2,3) with Silver contacts at three different high-temperature annealing conditions of (950°C/5min, 1000°C/1min, and 1050°C/1min).

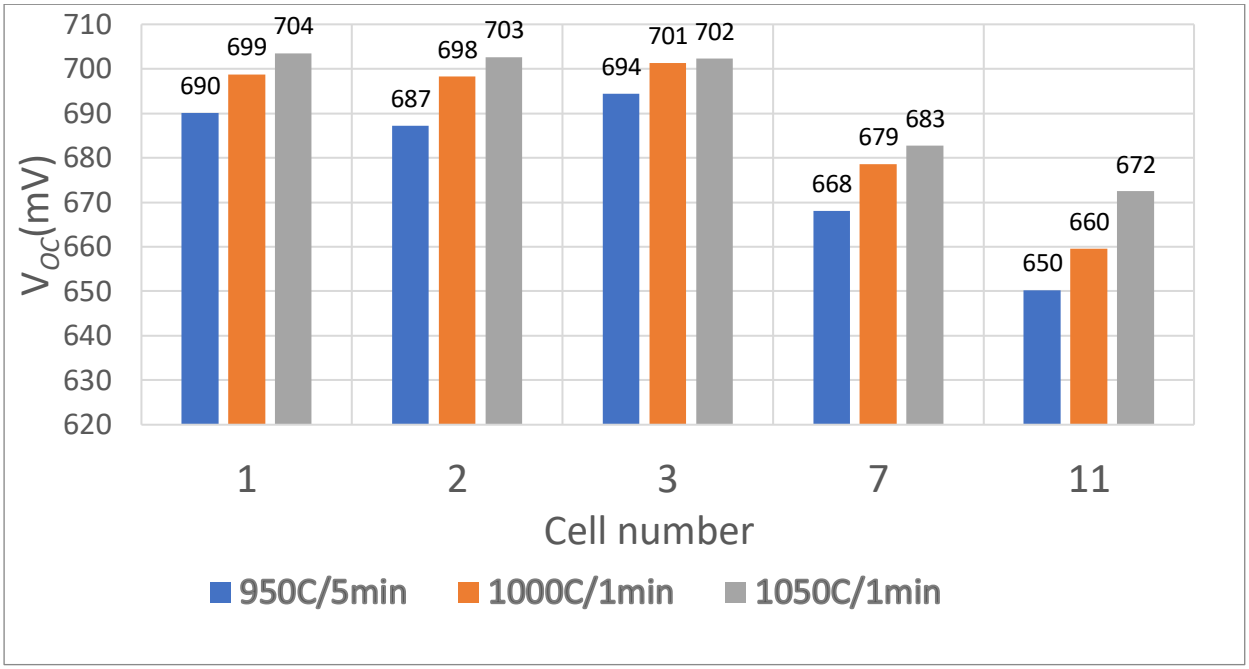


Figure (4.8) V_{OC} values obtained with I-V characterization for cells number(1,2,3) with Aluminum contacts at three different high-temperature annealing conditions of (950°C/5min, 1000°C/1min, and 1050°C/1min).

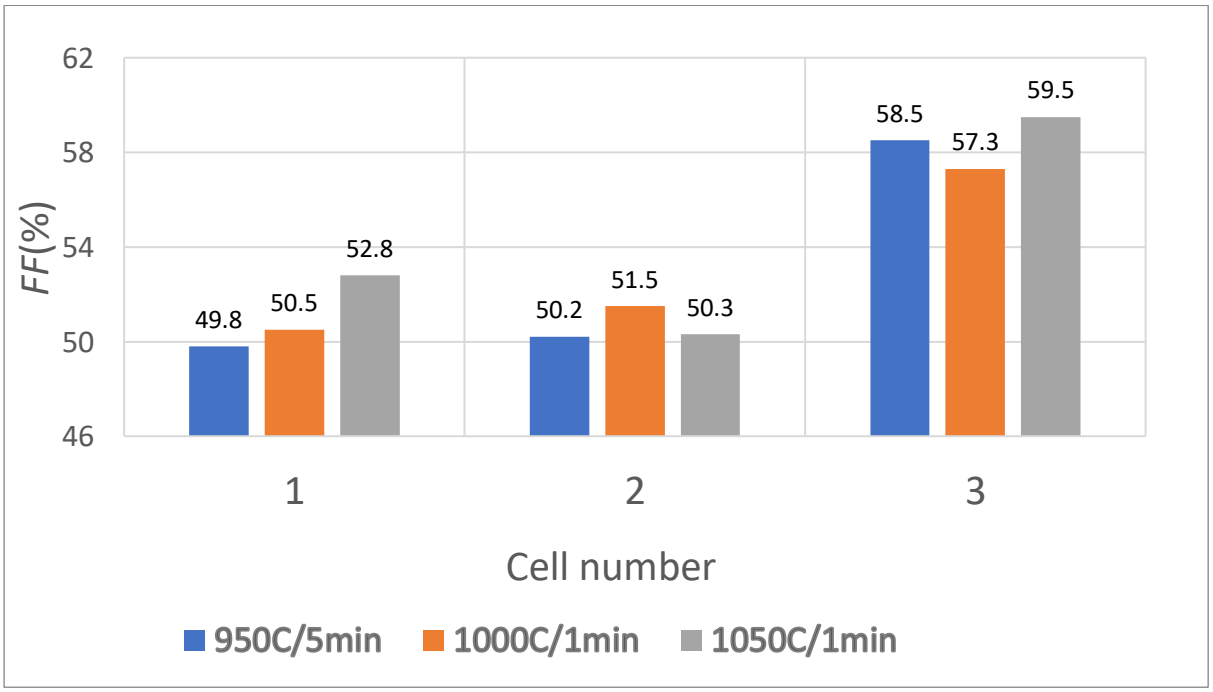


Figure (4.9) *FF* values obtained with I-V characterization for cells number(1,2,3) with Aluminum contacts at three different high-temperature annealing conditions of (950°C/5min, 1000°C/1min, and 1050°C/1min).

4.5 Post-metallization annealing effect:

The post-metallization annealing step was performed in another work in the PVMD group and it is proven to increase the FF particularly in case of TCO layers are deposited between the metal and the poly-Si [34]. This process decreases the contact resistance between the metal contacts and the poly-Si and the resistance of the electrodes themselves[39]. The post-annealing treatment is carried out by placing the wafer on a hotplate at a temperature between 300 and 550°C which is the limit of the hotplate device for different time duration. we measure the performance parameters of the cells after each annealing step. The annealing treatment effect is plotted for cell number 2 of wafer annealed at 1000°C/1min condition. The results plotted in figure (4.9) and (4.10) illustrate that the annealing steps performed do not have a remarkable influence on the passivation quality which is represented by V_{OC}. However, when the wafer was annealed for a time duration of 10 minutes at 550°C, the passivation quality decreases dramatically as a result of the hydrogen diffusion from the SiN_X layer. Thus, the annealing process did not go further. On the other hand, the fill factor dropped gradually through the first three steps where the temperature was under 500 °C, see figure 4.10. Raising the temperature further to a higher value like 500 °C and 550°C for a time duration of 4 or 6 minutes significantly increases the fill factor. the value of the fill factor is further enhanced after 10 minutes annealing time at 550°C to reach 64% but at the expense of decreasing the cell V_{OC} due to the decreasing of the passivation quality of the poly-Si passivating contacts as mentioned earlier. The large increase in the fill factor is attributed to the pinholes formed in the t-SiO_X layer which facilitate carriers transportation. This treatment is done also to another wafer and shows a similar trend.

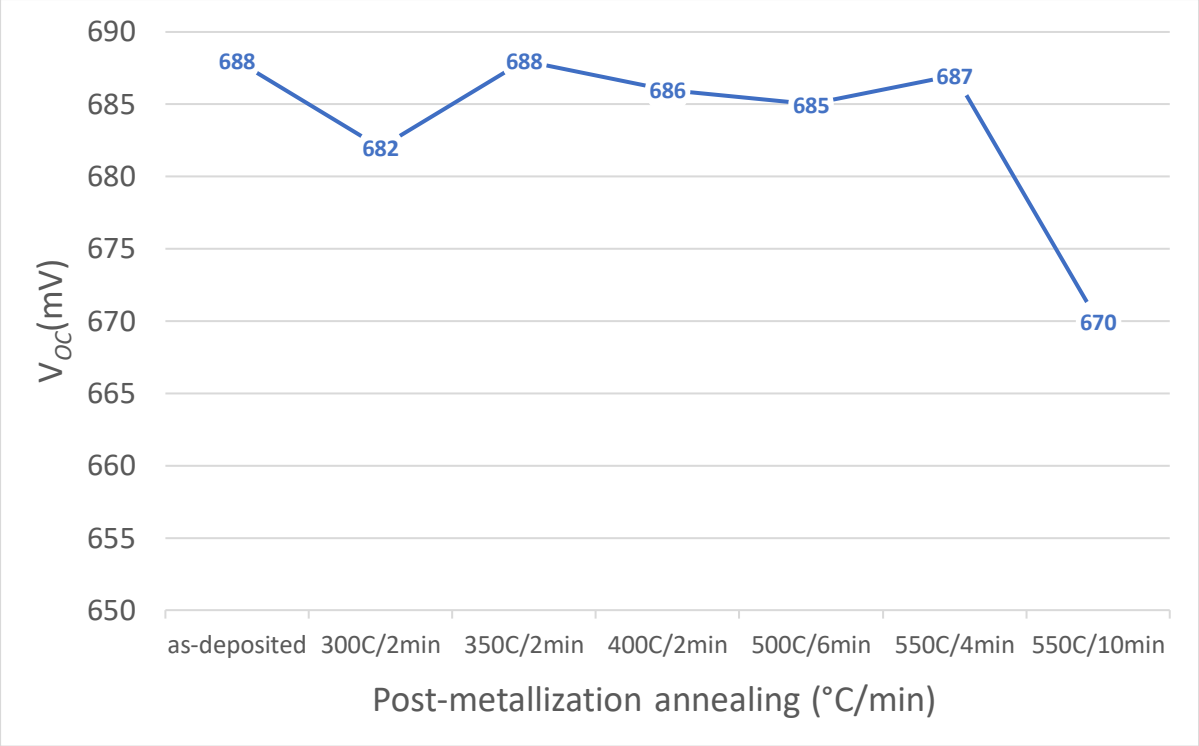


Figure (4.9) V_{OC} values obtained with I-V characterization for cell number1 of wafer 2 after post-metallization annealing with Al contacts.

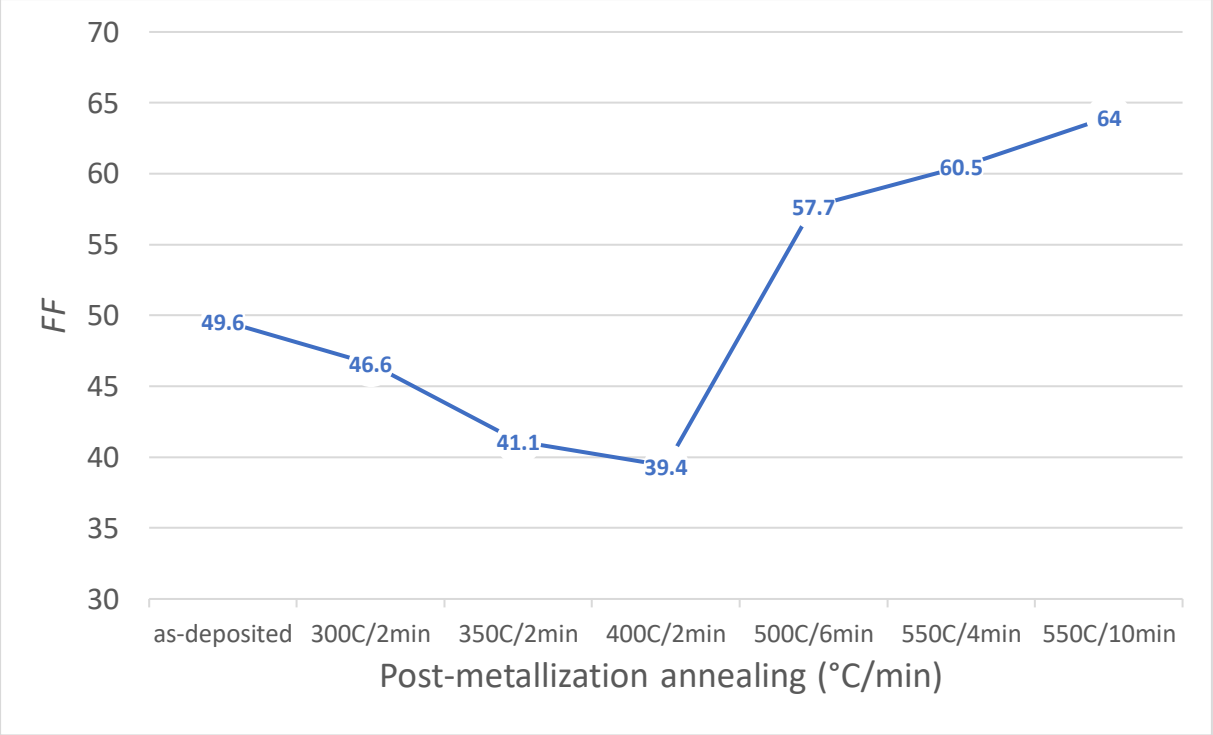


Figure 4.10: *FF* values obtained with I-V characterization for cell number1 of wafer 2 after post-metallization annealing with Al contacts.

4.6 Conclusion:

This chapter aimed to evaluate the optimized poly-Si passivating contacts in FBC solar cells due to the simplicity of their production steps, and try to understand the influences of fabricating parameters on the electrical performances of the FBC solar cells. Three wafers are fabricated with a tunneling layer of t-SiO_X with a thickness of around 1.5 nm and 250nm of poly-Si. The same doping dose of 6e15 and 5e15(ions/cm2) was used for Phosphorous and Boron implantation at a fixed implantation energy of 20keV, followed by a post-annealing step of 950°C/5min for wafer1 and, 1000°C/1min, and 1050° C/1min for wafer 2 and 3 respectively. The wafers are provided with the same antireflection coating of SiN_X which is used for the hydrogenation process as well followed by the FGA step. The metallization process is carried out by thermal evaporation of Silver firstly then Suns-V_{OC} measurement is performed. The results obtained show that the passivation quality of wafers annealed at higher temperature (1000°C/1min, and 1050°C/1min) conditions is better than the one annealed at 950° C/5min condition in terms of Suns-V_{OC} and p*FF,* the p*FF* values were above 80% and the highest Suns-V_{OC} was 718mV for the wafer annealed at 1050°C/1min conditions. Comparing these results with the results obtained from the V_{OC} and FF values obtained from I-V measurement, a large reduction in the fill factor is observed and attributed to large series resistance between the poly-Si and the bulk. The silver contacts have poor adhesion and tend to peel off during annealing, whereas Al with Si will form alloys that reduce the resistivity between Al and the poly-Si contacts therefore the Ag contacts are removed and Al contacts are deposited. The post-annealing aims to enhance the contact conductivity between the poly-Si contact and the bulk, on the other hand, it may enhance the poly-Si passivation which will benefit the cell V_{OC}. The post-metallization annealing process shows no improvement to restore the passivation quality V_{OC} while on the other hand a 10% of the increase is achieved for the *FF* after the post-metallization annealing as a result of the formed pinholes in the SiO_X layer.

5

IBC SOLAR CELL: FRONT SIDE OPTIMIZATION

In this chapter, a short theoretical introduction about the importance of optimizing the front side of the cells is explained. Then the effect of the P implantation doping dose and the annealing temperature on the sheet resistance of the front side c-Si surface is investigated. Different passivation layers for the front side are tested and the influence of the FGA treatment on the passivation quality of the front side is evaluated.

5.1 The importance of engineering the front side of the IBC cell:

An important characterization of IBC solar cells is that we can optimize the front and the backside of the cell separately, therefore to enhance the optical property of the cell it is decided to texture the front side to improve the light in-coupling in the cell. because the reflected light at a textured surface might be reflected at different angles and incident again on another point of the surface. in addition, the absorption path length within the c-Si bulk increases due to the scattered light at different angles than the normal to the wafer's surface which is important for wavelength above 900 nm, see Figure 5.1 [6].

The optical properties of the cells can be further enhanced by depositing an anti-reflection coating layer such as SiN_X which has a refractive index between 1.8 and 3 at a wavelength of 633 nm that can be manipulated by controlling the Si-content [40,41]. SiN_X has a passivation role as discussed in the hydrogenation section. Therefore it is widely used to enhance the optical and electrical properties of the cell.

The texturing process is realized by wet etching, where double side polished (DSP) n-type (FZ) c-Si wafers are immersed in the texturing mixture which is contained of Alka-Tex and Tetramethylammonium Hydroxide (TMAH) mixed with water at a ratio of 1:4 at a temperature of 80°C for approximately 15 minutes (until the surface is uniformly textured), the etching rate of the <100> crystal lattice orientation is much higher than its counterpart of <111> lattice orientation, therefore random pyramids are formed, which result in increasing the surface area[43]. The increasing area beside the pyramid's tips and edges form defect states which lead to a decrease in the passivation quality at the surfaces [44,45]. Two approaches are carried out to enhance the passivation quality after texturing, first is introducing a doped region at the front side through ion implantation to reduce the concentration of the minority carriers there which results in a reduction in the recombination. It is important to consider that increasing the doping dose leads to an increase in the Auger recombination at the c-Si surface doped region thus a trade-off between building an adequate potential barrier to initiate sufficient field-effect passivation and increase the recombination rate [46].

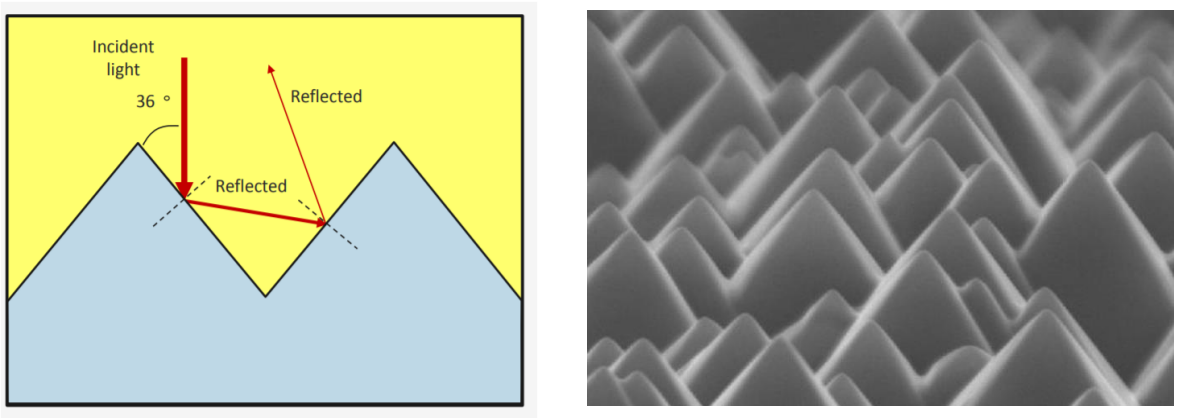


Figure 5.1(a): Light reflection at the textured surface. Figure 5.1(b): SEM picture of a textured surface.[6]

5.2 Sheet resistance:

Sheet resistance measurement is conducted by using a four-point probe method to realize the effect of the doping on the lateral conductivity for wafers with doping doses of 1e14 and 3e14(ions/cm^2) and annealed at different conditions in terms of time and temperature. The output results for each doping dose is reported in figure 5.2 show that generally for both doping doses, the sheet resistance shows a descending trend as we increase the annealing temperature, nevertheless, the first sample 950°C/5min annealed for a longer duration. The minimum obtained sheet resistance, R□, of samples with 1e14 (ions/cm^2) doping dose is above 240 (Ω/sq) for the sample annealed at 1050°C/1min while the highest value is around 266 (Ω/sq) for the sample annealed at 950°C/5min. On the other hand, sample annealed at 1050°C/1min but with doping dose of 3e14 shows a minimum R□ just below 200 (Ω/sq) and a maximum of 245(Ω/sq) for annealing condition of 950°C/5min. This outcome illustrates enhancement in the lateral conductivity for increasing the annealing temperature as a consequence of the increase in the carrier concentration, see figure 5.4, and the decrease in the trap density during the annealing process [47]. However, increase the doping dose further can reduce the sheet resistance further but will increase the Auger recombination rate near the surface [45].

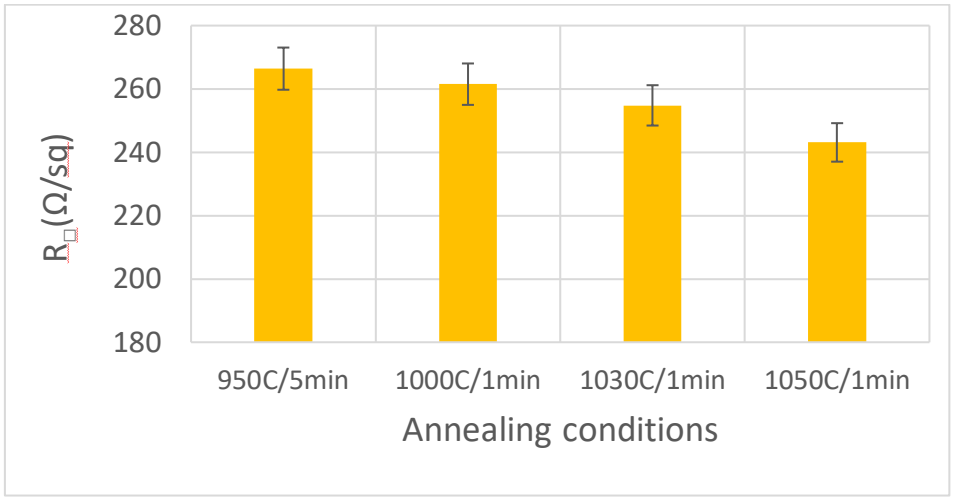


Figure 5.2 Sheet resistance results for samples with doping dose of 1e14 and implantation energy of 20 keV for different annealing conditions of 950°C/5min,1000°C/1min, and 1050°C/1min.

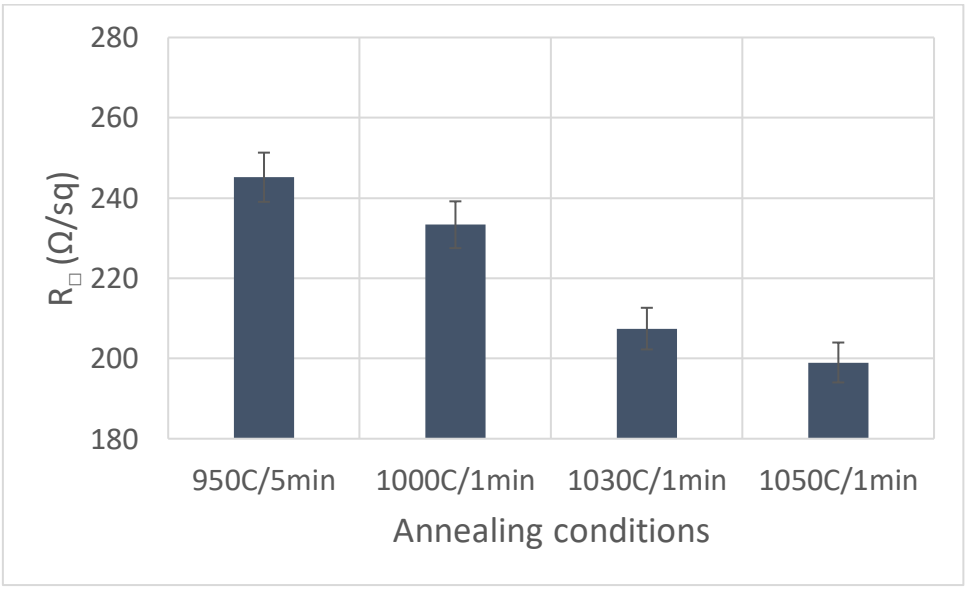


Figure 5.3 Sheet resistance result for samples with doping dose of 3e14 and implantation energy of 20 keV for different annealing conditions of 950°C/5min,1000°C/1min and 1050°C/1min.

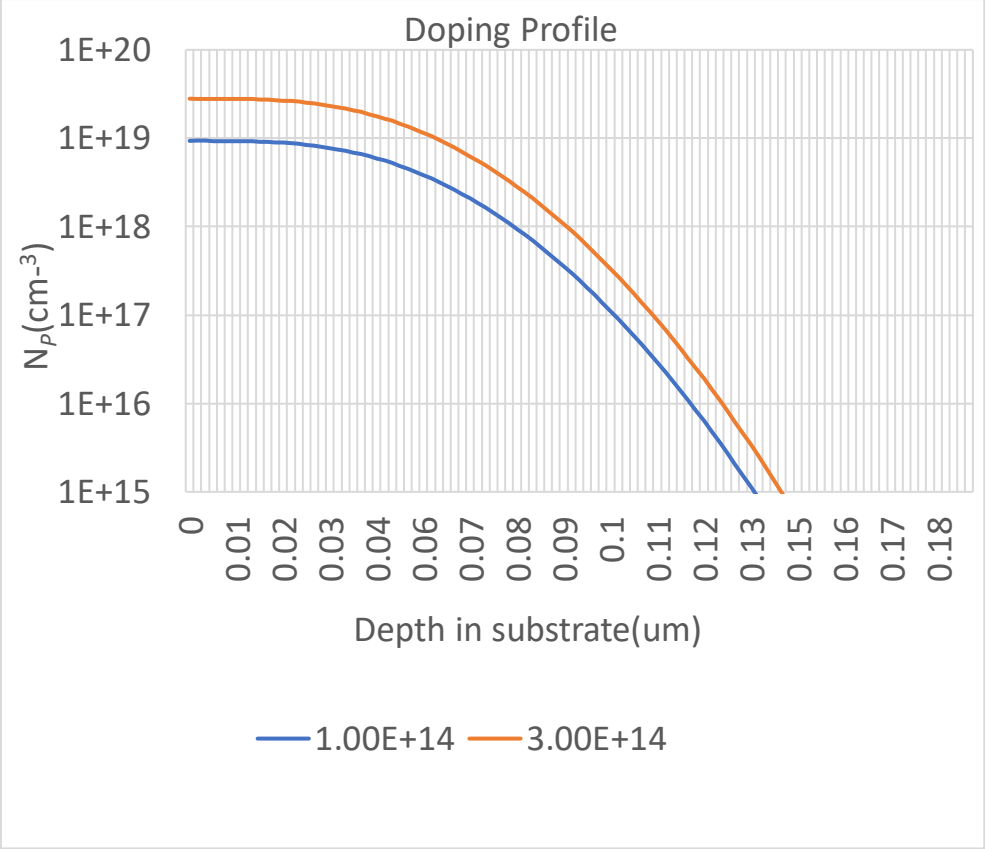


Figure 5.4: simulated doping profile of wafers annealed at 1050°C for 1 minute with phosphorous doping dose of 1e14 and 3e14 at 20 keV implantation energy. [48]

5.3 Front surface field Passivation:

Depositing a passivation layer on the front side of the cells is a commonly used approach in the fabrication of both FBC and IBC solar cells [49,50,51] to enhance the efficiency, this approach can be combined with doping the front side of the cell to maximize the passivation quality. Materials like SiO_X, AlO_X, a-Si:H, and SiN_X are extensively investigated and characterized in research publications, therefore it is decided in this work to evaluate the effect of different surface passivation layers on the passivation quality of the n^+ doped c-Si surface which acts as FSF for the IBC solar cells.

5.3.1 evaluating the effect of doping dose on the FSF passivation:

In this section, it is aimed to investigate the effect of the doping dose on the front side passivation quality since the initiated field-effect passivation is mainly based on the doping dose and the annealing conditions. Wafers with Two different doping doses and one sample without doping as reference are implemented. a stack of AlO_X/SiN_X as a passivating layer is used to test the passivation quality of this stack for different doping doses. Both aluminum oxide and silicon nitride are hydrogen-rich layers, therefore they are used individually or together as a capping layer for the hydrogenation treatment of the rear side poly-Si passivating contacts of the cell or the passivation of the cells' surface [52,53]. The fabricating parameters of the stacked AlO_X/SiN_X layers are already optimized in our group therefore it is decided to evaluate its performance on test samples to determine the passivation approach of the front side as a preparation step of fabricating IBC solar cells. The test samples are fabricating as follow:

1. Firstly, three double-side polished n-type c-Si FZ wafers with <100> surface orientation and a thickness of 280um are textured by immersing the wafers in an alkaline solution of Alka-Tex, and Tetramethylammonium Hydroxide (TMAH) as explained in section: (5.1).
2. After the texturing process, the wafers undergo the standard cleaning process where they are immersed in a 99% HNO3 solution followed by a rinsing step, then immersed again in a 68% HNO3 bath but at 110°C then moved to the rinsing bath, to clean the wafers from any contamination or residue from the texturing process.
3. Then, the wafers are dried by the drier, and two of them are moved to the implantation step, where they are implanted with phosphorous with a dose of 1e14 and 3e14 respectively at a fixed implantation energy of 20 keV.
4. A standard cleaning process is perfumed after the implantation of the two wafers than the three wafers are annealed at 1050°C for one minute in the furnace.
5. Then the three wafers are passed to the Marangoni cleaning process in 0.55% hydrofluoric acid (HF) to remove the native oxide before depositing the passivating layer.
6. At this point the samples are ready for the deposition where firstly a thin layer of 10 nm of AlOX is deposited through Atom layer deposition (ALD) technology which is done on the upper side then the wafer is flipped to deposit on the other side, the wafers then moved to the Oxford PECVD instrument where a layer of 75 nm is deposited on one side each process.
7. At the end of these steps, we have three symmetrical samples with AlOX/SiNX on both sides, where two of these samples are doped and undoped sample. See figure 5.5

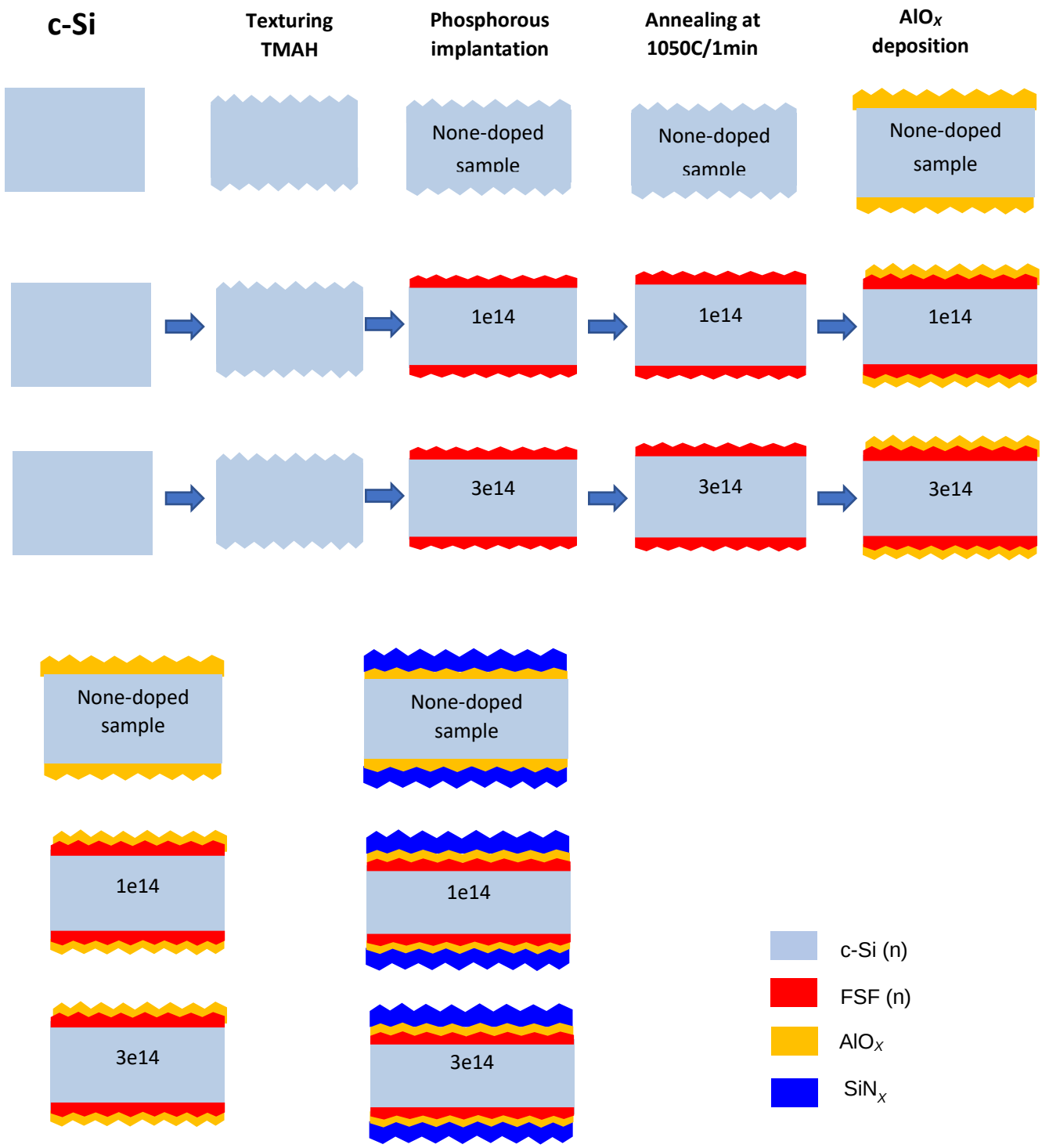


Figure:5.5 Sketch of the fabricating steps of the FSF passivation samples with AlO_X/SiN_X as passivating layers with different doping doses.

The obtained results of the passivation test reported in figure 5.6 show a significant difference in the iV_{OC} values between the sample with an implantation dose of 3e14 (ions/cm^2) and the other samples. 708 mV is the highest iV_{OC} measured for the sample with no FSF and the sample implanted with 1e14 (ions/cm^2). The lowest value of 594mV is attributed to the surface defects associated with the implantation and the increase in the recombination rate which is caused by Auger recombination as a result of the increase in the dopant concentration in c-Si near the surface. The function of the doping is to initiate a passivating electric field to further enhance the passivation quality of the passivation with help of the AlO_X/SiN_X passivating layer. The sample with 3e14 ions/cm^2 dose causes a high recombination rate near the surface. This is attributed to the high concentration of the dopants that diffuse deeper in the substrate at a higher implantation dose comparing to the sample with 1e14 ions/cm^2 as illustrated in the simulated doping profile of both samples in figure 5.3. Comparing the none doped sample with the sample doped with the 1e14 P-implanting dose, it is remarkable that there was almost no difference, this indicates that the field-effect initiated by the FSF compensates the losses in passivation quality that is attributed to defects caused through the implantation process.

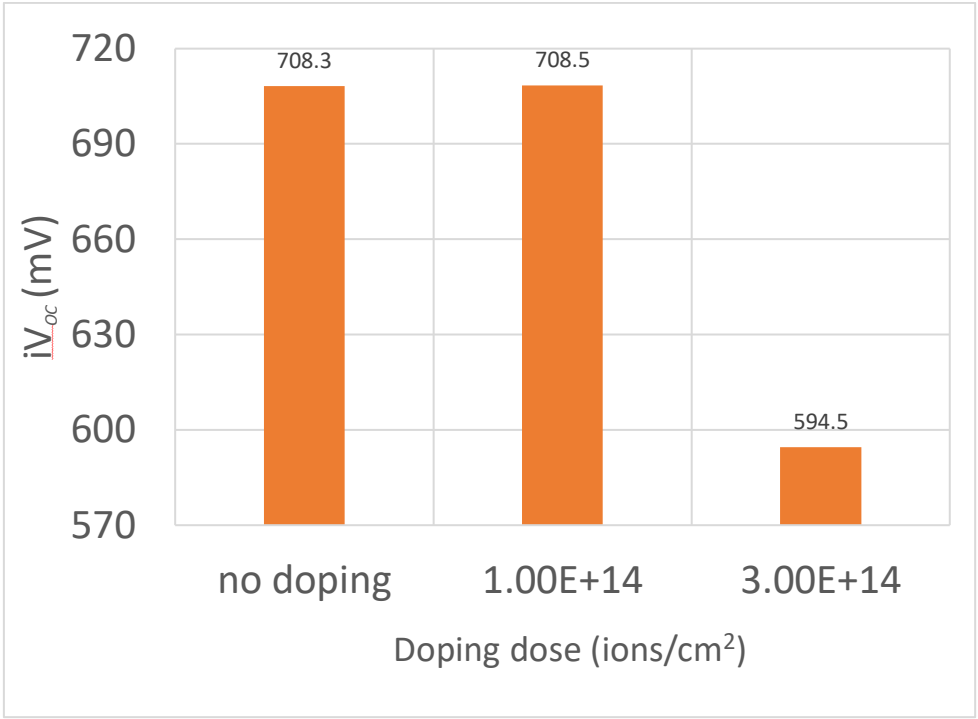


Figure 5.6 iV_{OC} for FSF test samples passivated with AlO_X/SiN_X layer for no doping, and doping dose of 1e14,3e14 at an implantation energy of 20 keV, and annealing condition of 1050°C/min.

5.3.2 Different passivating layers:

After evaluating the performance of the AlO_X/SiN_X passivating stack for passivation of FSF surface which prepared with different doping dose. another double stack layer such as a-Si/SiN_X and sole SiN_X layer are tested at a doping dose of 1e14 ions/cm^2 since these layers are widely used in FSF passivation and show a good passivation quality [36,42].

PECVD SiN_x passivation layer:

The test samples are fabricated in the same operation process as done in section (5.3.1), but with fixed implantation parameters but different passivating material, where both a-Si and SiN_X are deposited by PECVD technology. SiN_X layer is commonly used in the solar cells industry as ARC because it has a suitable refractive index [36], and taking its positive fixed charge Qf into account make it very desirable as passivating layer solely or stacked with another layer for n-type solar cells [54]. The hydrogen content effectively passivates the defects at the surface, however many things like the concentration and the type of the existing defects and impurities within the silicon, the electric field, and the temperature's deposition greatly affect the hydrogen diffusivity subsequently the passivation result [55]. The temperature of SiN_X deposition is crucial, since depositing the SiN_X layer at a lower temperature may prevent the hydrogen effusion from the layer. thus a 75 nm layer is deposited through PECVD technology at 400°C, as it gives the best passivation quality corresponding to the tool limitation [34]. The results of using solely SiN_X as a passivating layer for the textured surface are reported in figure 5.7. It shows poor passivation quality with iV_{OC} of 661mV, which indicates that the positive fixed charge of the SiN_X layer was not enough to initiate the required field-effect passivation and the hydrogen content could not effectively eliminate the surface and the bulk defects.

PECVD a-Si:H/SiN_X passivation stack

The second tested stack is SiN_X a-Si:H/SiN_X, the amorphous silicon when coupled with silicon nitride gives the best passivation and outperforms the other passivating tested layers with iV_{OC} of 714 mV. a-Si:H is well known as an excellent passivating layer due to its high hydrogen content of 12~18% [58] but is associated with a large optical loss when it is deposited at the front side of the cell. The parasitic absorption associated with the a-Si:H causes a reduction in the J_{SC} and consequently the cell's efficiency. To reduce the parasitic absorption, it is common to use a very thin layer of a-Si:H. Wan et al. claimed a high passivation quality for a sub-nm of hydrogenated amorphous silicon film coupled with silicon nitride [59]. However, in this work, a 10 nm of amorphous silicon deposited at 200°C capped with 75 nm layer of SiN_X as these parameters were already optimized in our group, and investigating different passivating layers is out the scoop of this work.

ALD-Al_2O_3/PECVD-SiN_x passivation stack

The third tested passivating material is AlO_X/SiN_X stack, a thickness of 10 nm of AlO_X is deposited through thermal ALD technology at 105°C and capped by 75nm of PECVD SiN_X deposited at 400°C. These stacked layers lead to high passivation quality with iV_{OC} of 708.5 mV and J_0 of 7 fA/cm^2 attributed to its high hydrogen content, the passivation provided by AlO_X/SiN_X is strongly dependent on the AlO_X thickness and its growth conditions as it determines the properties of the substrate interface such as the defect density and fixed charges density [60]. Nevertheless, the negative fixed charge of AlO_X makes it a suitable material to passivate p-type c-Si. it can provide effective passivation to n-type c-Si as well depending on the chemical passivation when the surface is lightly doped especially when it is capped by SiN_X as it reduces the AlO_X fixed charges density [36,61].

Finally, to enhance the passivation quality of the solely SiN_X passivating layer, an investigation of SiN_X composition is done by measuring the implied open-circuit voltage when depositing firstly a 10 nm of SiN_X at different gasses composition ratio then depositing the second layer of SiN_X of 75 nm at the default

deposition parameters. The samples are prepared according to the method explained in section (5.3.1). The ratio of SiH_4/NH_3 is manipulated within the limitation of the tool, see table 5.1. The obtained results are reported in figure 5.8. The results show that increasing the gasses ratio of SiH_4/NH_3 from its initial value of 20/20 to 20/10 leads to the enhancement of the passivation quality of the deposited SiN_X with iV_{OC} of 686,7mV. This enhancement is caused by the additional Siliconcoming from the increased proportion of Silane. Decreasing the SiH_4/NH_3 ratio by decreasing the SiH_4 gas flow leads to poorer passivation as shown in Figure 5.8.

Table 4.4 Gas mixture and gas ratios used for deposition of SiNx layers

SiH_4 (sccm)	**NH_3 (sccm)**	**SiH_4/NH_3 ratio**
20	20	1
20	10	2
20	2	10
15	20	0.75
10	20	0.5
5	20	0.25

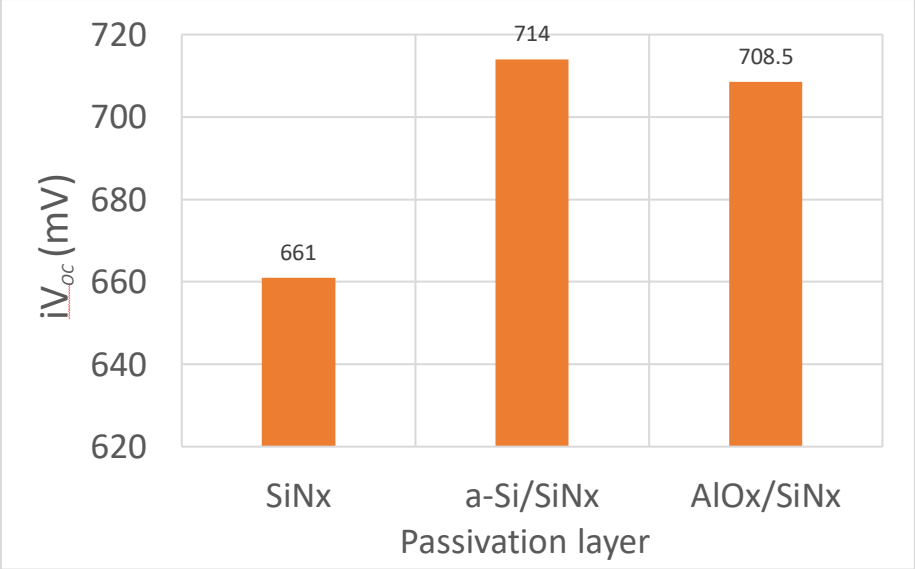


Figure 5.7 Passivation quality of FSF test samples with SiN_X, a-Si/ SiN_X, and AlO_X/SiN_X passivating stack layers. The FSF test samples were prepared with the conditions of doping dose of 1e14 and implantation energy of 20 keV, and annealing condition of 1050°C/min.

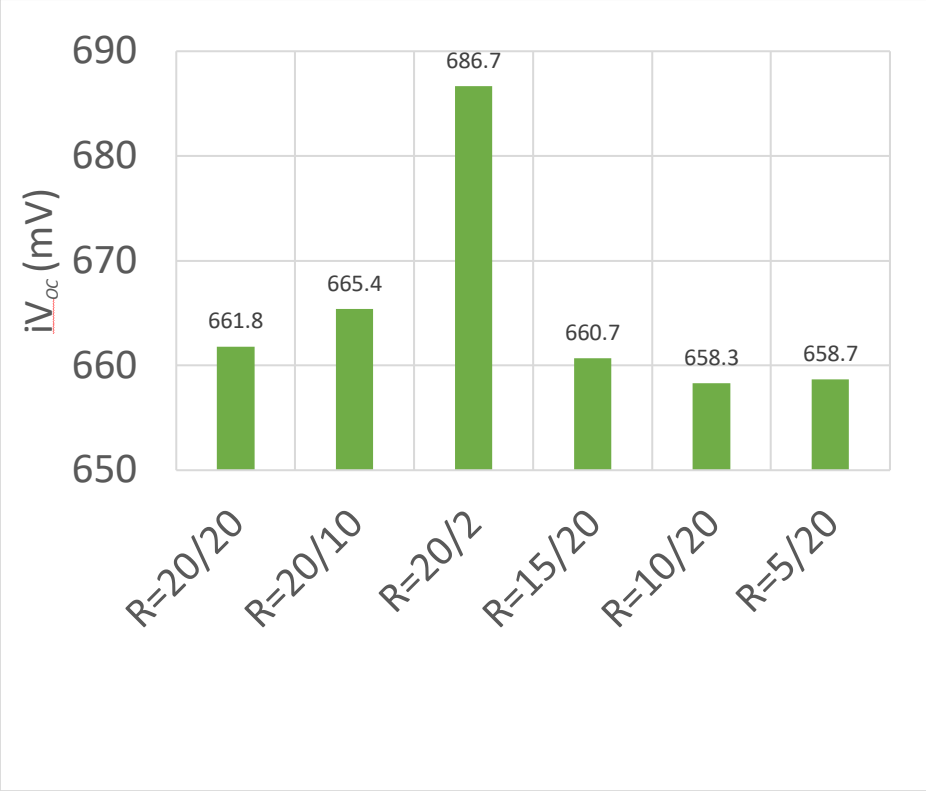


Figure 5.8 Passivation quality of FSF test samples with only SiN_X as a passivating layer for different SiH_4/NH_3 ratios at doping dose of 1e14 (ions/cm^2) and implantation energy of 20 keV, with annealing condition of 1050°C/1min.

5.3.3 The effect of FGA on the front surface passivation:

Finally, the effect of FGA on the surface passivation is evaluated, as the FGA process is used during hydrogenating the rear side poly-Si passivating contact when preparing IBC solar cells. The symmetrical samples with the tested passivating materials of AlOX/SiNX, a-Si/SiNX, SiNX/SiNX, and the sample with only SiN_X are subjected to the annealing process in forming gas at 400 °C for 30 minutes. The results are plotted in figure 5.9 illustrate that the sample with only SiN_X and the one with AlO_X/SiN_X show a considerable increase. This increase is owed to the extra hydrogen provided during the FGA which saturate more surface defects and the existing hydrogen at the interface that get more energy to diffuse and bond with the defects. It also indicates that these passivating layers were proofed to withstand the annealing temperature of 400°C for 30 minutes. On the other hand, the sample with a-Si/SiN_X as passivating layer experienced a sharp decrease in the passivation quality from 714 to 679 mV as a result of the low thermal stability of the amorphous silicon. It can be attributed to defects formation since the high temperature leads to crystallization of the a-Si [28]. a-Si:H is reported to provide effective passivation for both n-type and p-type c-Si but the main disadvantages related to it are the high blue light absorption and the low thermal stability. Therefore, the FGA treatment during hydrogenating the rear side poly-Si passivating

contacts should be done before passivating the front side of the cell, in case that is passivated by a-Si/SiN_X to avoid the deterioration in the passivation quality.

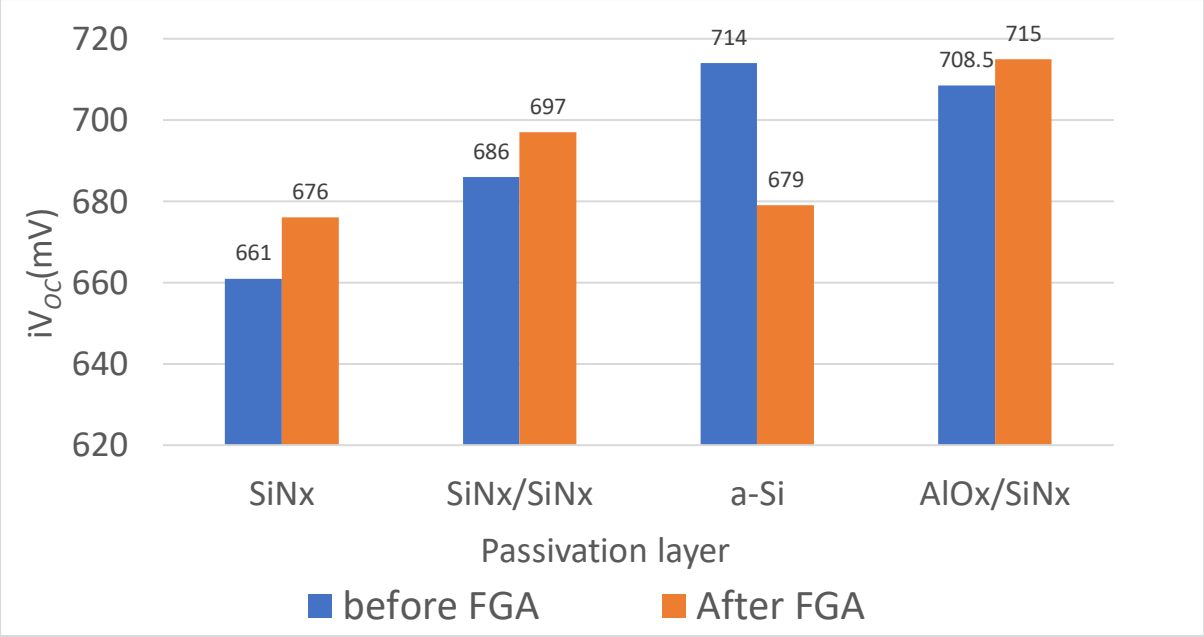


Figure 5.9 Passivation quality results before and after FGA process, the samples were prepared with a doping dose of 1e14 and implantation energy of 20 keV, and annealing condition of 1050°C/min.

5.4 Conclusion:

To achieve high-efficiency IBC solar cells, the performance of the different doping doses for FSF and different passivating materials are investigated. The sheet resistance of the FSF decreases when the annealing temperature is raised or by increasing the doping dose, and the minimum obtained R□ was just below 200 (Ω/sq) for the sample annealed at 1050°C/ for 1 minute. When the FSF is passivated by AlO_X/SiN_X stack, a close iV_{OC} for the non-doped sample and the lightly doped sample with 1e14 ions/cm^2. While the sample implanted with a higher dose of 3e14(ions/cm^2) shows poor passivation due to a high Auger recombination rate close to the surface.

The passivation quality with phosphorous FSF of 1e14(ions/cm^2) by four different passivation stack layers SiN_X, AlO_X/SiN_X, a-Si/SiN_X, and double SiN_X /SiN_X are evaluated. The double SiN*x*/SiN*x* stack is prepared with varying the SiH_4 to NH_3 flow ratio for the first 10nm of SiNx. The results show excellent passivation for

the sample passivated with a-Si/SiN_X with an iV_{OC} of 714 mV. However, this sample experienced a degradation in the passivation quality after it is subjected to annealing in forming gas at 400°C for 30 minutes due to the low thermal stability of the a-Si:H. The AlO_X/SiN_X passivated FSF sample showed lower passivation quality but higher thermal withstanding and experienced a further enhancement in the passivation quality from 708 mV to reach 715 mV after the FGA process. Whereas the sample that is passivated with SiN_X/SiN_X showed its best results of 697mV after the FGA process.

6

IBC SOLAR CELLS: FABRICATION AND RESULTS

The aim of this chapter is to fabricate high-efficiency IBC solar cells based on poly-Si passivating contacts with the optimized parameters from chapter 3 the IBC solar cells feature textured FSF to enhance the optical properties of the cells, while the FSF is passivated with the passivating layers evaluated in chapter 5.

Firstly, the implemented flowchart to fabricate the IBC cells is explained and associated with a detailed sketch of the fabricating steps. Then the external parameters of the cells are measured and discussed. In the end of the process, high conversion efficiency of 21.04% is obtained for the wafer provided with a-Si/SiN_X as FSF passivating layers and annealed at 1050°C for 1 min. After that several wafers are subjected to the post metallization annealing process in order to study the influences of post-annealing on the cell performances.

6.1 The flowchart for fabricating IBC solar cells:

The flowchart starts with 7 n-type FZ Silicon wafers with a thickness of 280um, double side polished (DSP)with <100> orientation. Marangoni cleaning by HF was used before starting the cell processes to fabricate the wafers as illustrated in table 6.1 following processing steps is done consequently.

Table 6.1: the aimed variables used to fabricate IBC solar cells

Wafer number	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Temperature of post-annealing	1000°C	1030°C	1050°C	1050°C	1050°C	1050°C	1050°C
Front side passivation	AlO_X/SiN_X	AlO_X/SiN_X	SiN_X/SiN_X	a-Si/SiN_X	AlO_X/SiN_X	AlO_X/SiN_X	AlO_X/SiN_X
FSF Doping dose (ions/cm^2)	1E+14	1E+14	1E+14	1E+14	1E+14	no	3E+14

1. Thermal silicon oxide formation: to prepare for this step, standard cleaning process with HNO3 and Marangoni cleaning process with HF are carried out to avoid any possible contamination and formation of native oxide on the wafers' surfaces before the formation of the t-SiOX which is done in a Tempress furnace at 675°C for three minutes in an atmosphere of N2:O2=6:0.6
2. Poly-Si deposition: the wafers directly moved to LPCVD furnace for the deposition of ~250 nm of a-Si with a deposition time of 1h53 min based on the deposition rate.
3. Alignment markers formation: this process is done through several steps, coating, exposure, and development to finish the shape of the photoresist to protect the area that should not be etched in the next step where the markers are etched in the c-Si bulk through plasma-etching tool Tepla. The alignment marker formation is a crucial process since the implantation steps and the metallization deposition are based on it.
4. Boron implantation: the photoresist left after the alignment marker etching is removed through plasma cleaning and followed by the standard cleaning process. Photolithography steps are carried out to define the Boron implanted area, then the wafers are implanted at an implantation energy of 20 keV and doping dose of 5e15 ion/cm2 by Varian implanter E00HP.
5. Phosphorous implantation: the left photoresist is etched through plasma again which is followed by standard cleaning and new lithography steps to define the Phosphorous implanted area. After the lithography, the wafers are implanted with phosphorous with a doping dose of 6e15 ion/cm2 in order to form the BSF.
6. Gap Formation between the emitter and the BSF: the aim of this process is to avoid shunting between the formed contacts, the rest photoresist is etched again and a new lithography process (coating, exposure and development) is carried out again to define the etched area between the contacts. The gap is etched then through plasma etching ~400 nm into the bulk.
7. Texturing the front side: the wafers undergo a standard cleaning process after that and a thick layer of SiNX ~250nm is deposited on the rear side of the wafers to protect the fabricated contacts

from etching during the texturing process. The texturing is carried out through wet etching by immersing the wafers in the Alkaline solution of TMAH as explained in chapter4. The wafers are cleaned after that through a standard cleaning process and dried out to be ready for doping on the Front side.

8. FSF implantation: the protection layer of SiNX at the rear side is etched away by immersing the wafers in BHF bath and this is followed by the standard cleaning process and 6 out of 7 wafers are then phosphorous implanted, one wafer implanted with 3e14 ions/cm2 while the rest are implanted with a dose of 1e14(ions/cm2) and the 7th wafers are kept with no doping.
9. Annealing: standard cleaning is always perfumed after any implantation step to avoid any contamination or remains caused by the implanter, then all the wafers are annealed as following: the first wafers with 1e14(ions/cm2) are annealed at 1000C for 1 minute and the second wafers with the same FSF are annealed at 1030C for 1 min, whereas the five wafers rest are annealed together at 1050C for 1 min.
10. Rear side hydrogenation: the wafers are ready for the hydrogenation process where all of them are subjected to a 75 nm SiNX layer deposition by PECVD technology. Because of the Covid-19 measurement, there were extra restrictions to enter Kavli lab therefore it is decided to perform the FGA process for all the wafers after hydrogenating the rear side nevertheless FGA shows a positive effect to passivating the front side when layers such as SiNX and AlOX/SiNX are used.
11. Front side passivation and ARC deposition: since AlOX/SiNX shows the best frontside passivation results after FGA it is chosen to make it the reference front passivation layer, thus one wafer annealed at 1050°C and with doping dose of 1e14 (ions/cm2) beside the wafers with special annealing condition or FSF doping dose such as wafers which annealed at 1000C, 1030C, no doping, and FSF of 3e14 all are passivated with AlOX/SiNX layer. Firstly 10 nm of AlOX layer is deposited by ALD technology followed by 75 nm of SiNX deposited via PECVD as explained in chapter 5. Two wafers remain are annealed at 1050C for 1 min and with doping dose for FSF of 1e14(ions/cm2), one of them is provided by a-Si/SiNX whereas the other is passivated by SiNX /SiNX as detailed in Chapter 5. An FGA step could not be done for the wafers with AlOX/SiNX, a-Si/SiNX, and SiNX/SiNX due to limited access to Kavli lab.
12. Opening the contact area: this step is important as the metal should be deposited directly on the poly-Si CSPC, therefore the SiNX should be removed from the place of the metal grid. Lithography steps include: coating exposure and development are done to define the contacts area, and the front passivated side is protected by photoresist since the wafers have to be immersed in BHF etching bath to remove the SiNX. The contacts area then is opened and the protective layer of the photoresist is stripped by immersing all the wafers in Acetone.
13. Metal deposition: again, photolithography steps are carried out after a cleaning process to determine the place of the metallic grid of the electrodes, and the front side is protected by photoresist layer then, the wafers are shortly dipped in a BHF to remove any oxide before the metallization process, then the wafers are directly moved to the metallic deposition through e-beam evaporation deposition where a 2nm of Aluminum is deposited. After the deposition, a liftoff step in Acetone is perfumed to remove the photoresist on the front side and the metal between the metallic fingers and the planned IBC solar cells are obtained, see figure 5,1.

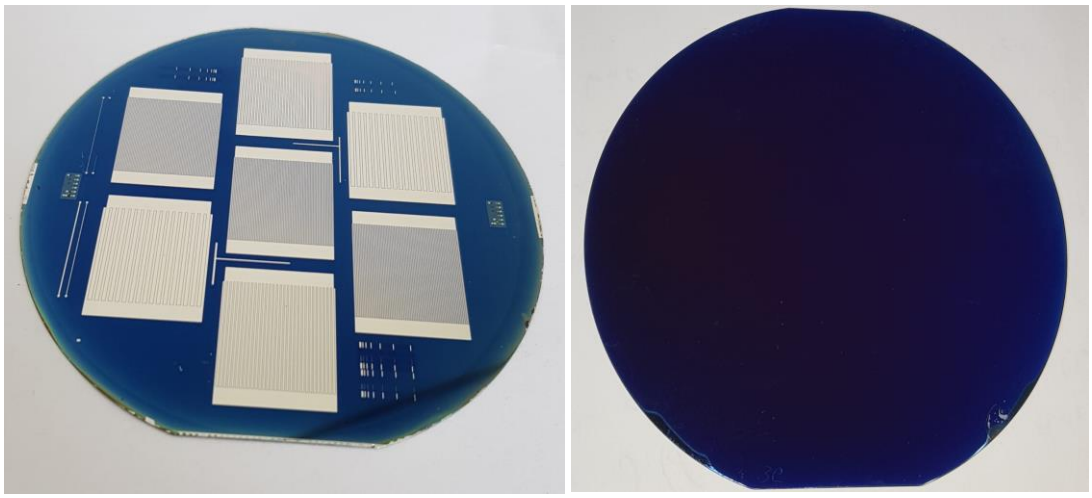
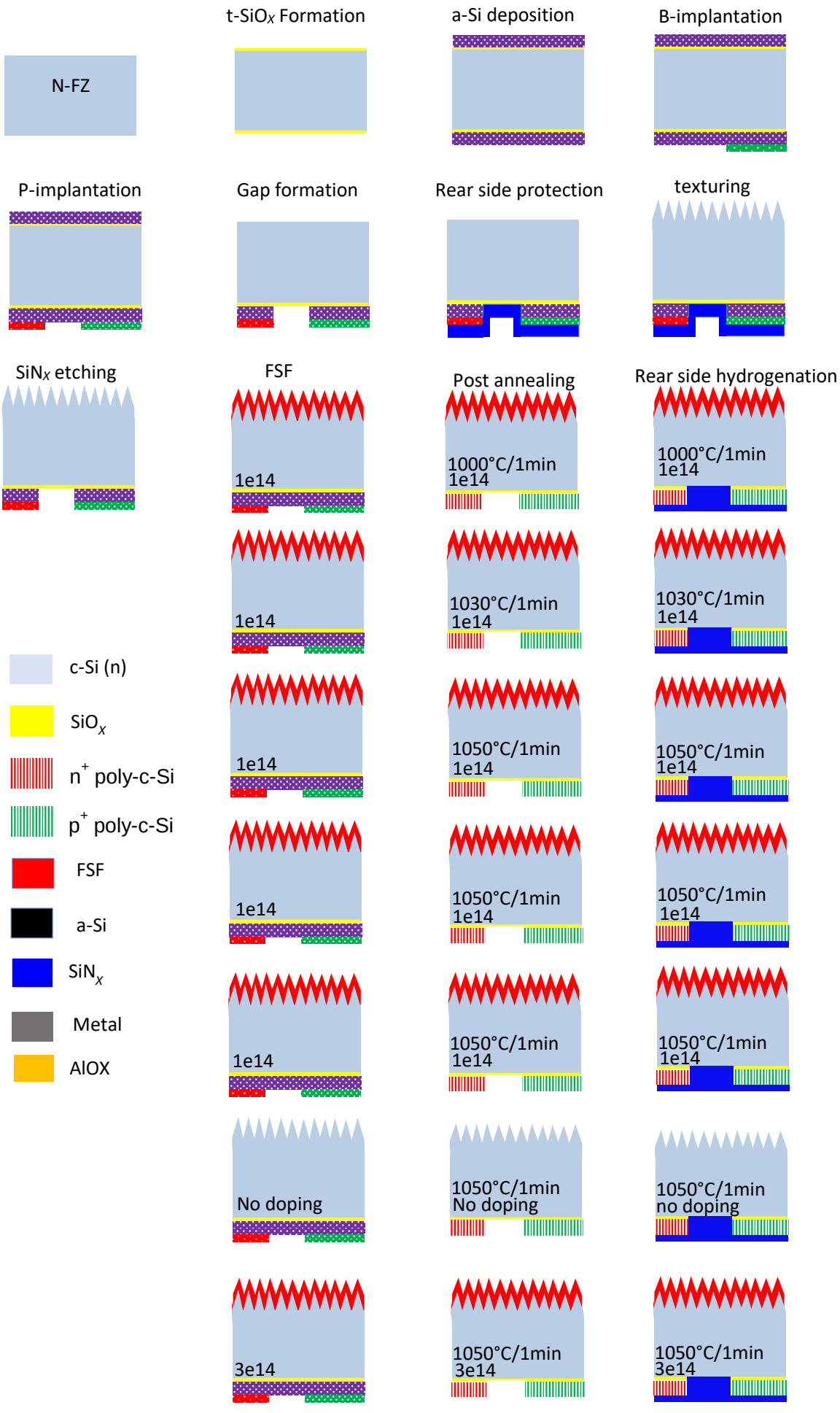
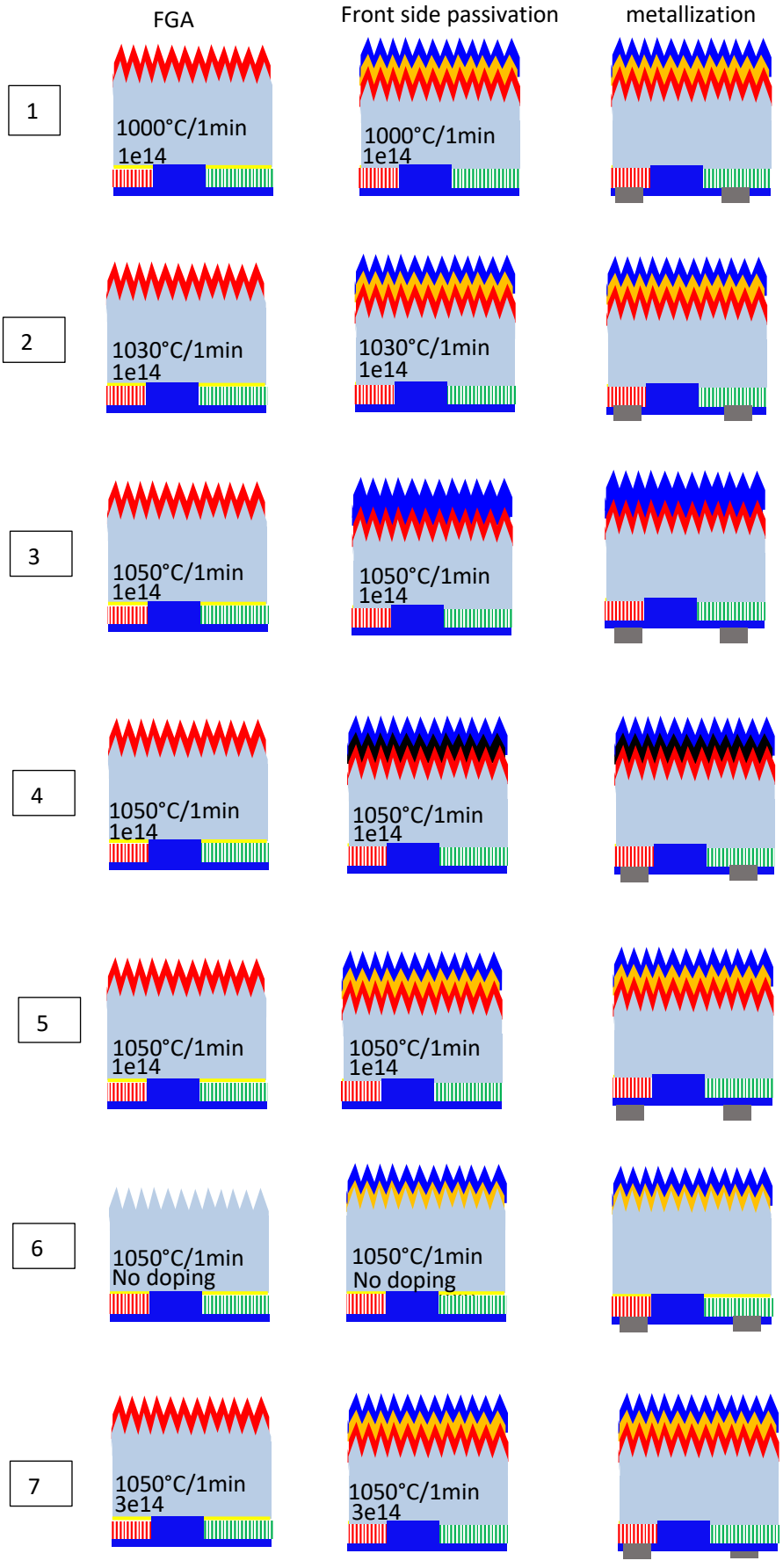


Figure 6.1: left: the rear side of the fabricated IBC solar cells after the metallization, right: the front textured passivated side.

Figure 6.2: Schematic sketches of the fabrication process of IBC solar cells.




FGA
Front side passivation
metallization
1
1000°C/1min
1e14
1000°C/1min
1e14
2
1030°C/1min
1e14
1030°C/1min
1e14
3
1050°C/1min
1e14
1050°C/1min
1e14
4
1050°C/1min
1e14
1050°C/1min
1e14
5
1050°C/1min
1e14
1050°C/1min
1e14
6
1050°C/1min
No doping
1050°C/1min
No doping
7
1050°C/1min
3e14
1050°C/1min
3e14

6.2 Results and discussion:

The fabrication process of IBC solar cells with poly-Si passivating contacts used in this section is aimed to evaluate the effect of three variables on the external solar cells' parameters represented in V_{OC}, *FF,* and the conversion efficiency. These variables including annealing temperature, the FSF doping dose, and the passivating layers of the front side, are listed in Table 6.1. The first variable is the post-implantation annealing temperature since the passivation quality tests are carried out in chapter 3, show that increasing the annealing temperature led to better fill factor and higher $V_{OC.}$ in addition, the sample annealed at 950°C for 5 minutes showed the poorest passivation quality thus, it is decided to replace it with annealing temperature of 1030°C for 1 minute. The best passivation in chapter 3 is obtained at 1050°C for 1 minute therefore it is fixed to be the reference annealing condition and 5 out of 7 wafers are annealed at this condition whereas wafer number 1 is annealed at 1000°C/1min and wafer number 2 annealed at 1030°C/1min for the comparison.

6.3 The influence of the annealing temperature on the cells' performance:

The three wafers are fabricated as shown in table 6.2 where all of them have the same FSF and front side passivating layer to evaluate the effect of the annealing temperature. Each wafer has 7 cells divided into 3 group according to the metallic grid design since the 7 cells show different performance which can be attributed to eventual contamination due to a large number of the fabricating steps besides the measurement deviation, therefore it is chosen to present the average values of cells 6 and 7 since they are in one group and has close values and the cell with the best performance will be reported.

Table 6.2: the compared fabrication variables of wafers number 5,6, and 7.

Wafer number	1	2	5
Annealing T	1000°C	1030°C	1050°C
FSF Doping dose (ions/cm^2)	1E+14	1E+14	1E+14
Front side passivation	AlO_X /SiN_X	AlO_X /SiN_X	AlO_X /SiN_X

Table: 6.2 the external parameters of the average values of cells 6 and 7 in wafers 1,2 and 5.

Wafer nr	***Annealing temperature [°C]***	**V_{OC} [mV]**	**FF [%]**	**Efficiency [%]**
1	1000	677	75	18.5
2	1030	682.5	75.8	19.7
5	1050	666	78.4	18.6

Firstly, the best-obtained cells in wafers 1, 2, and 5 are as follow: cell 6 in wafer 1 and wafer 2 have efficiencies of 19.3% and 20.5% respectively, while the best cell in wafer 5 shows efficiency of 19.4%. Looking at table 6.2 we can conclude that the cells of the wafer that is annealed at the highest temperature of 1050°C for 1 min show the highest fill factor of 78.4%. This trend is consistent for all the cells where the best-obtained fill factor was 79.3% of cell 6 wafer 5. The fill factor gradually decreases when decreasing the annealing temperature, which is attributed to the lower series resistance is caused by the lower contact resistivity and the sheet resistance as is illustrated in chapter 3. On the other hand, the V_{OC} of the cells in the three wafers, according to the results reported in table 6.2, indicates that the wafer annealed at 1030°C for 1 min has the highest V_{OC} at 682.5 mV thus the best passivation quality. Whereas the counterpart cells of the wafers are annealed at higher and lower temperatures show lower passivation. The passivation results are mainly attributed to rear side surface passivation at the poly-Si contacts interface with the bulk. Since the BSF contact is wider than the emitter contact because it is designed to collect the minorities (holes) which have a shorter lifetime, thus the passivation quality of the emitter is more significant. It is shown in chapter 3 that increasing the annealing temperature causes a reduction in the passivation quality of p-type contacts. However, this is not enough to explain the better V_{OC} obtained for cells in the wafer annealed at 1000°C for 1 min comparing with the wafer annealed at 1050°C which showed previously better passivation results in the passivation tests. This contradiction between the results obtained in the passivation tests and the result of the fabricated IBC cells might be attributed to the effect of the annealing temperature on the FSF which were not evaluated during the FSF optimization process since the tests are carried out for 1050C as it gives the best rear side passivation.

6.4 The influence of the surface passivating layer on the cells' performance:

Moving to the next group of the wafers, where the variable is the front side passivating layers. All the wafers are annealed at the same post-implantation annealing conditions of 1050°C for 1 min and have a doping dose for FSF of 1e14 (ions/cm^2). Three different double stacked layers of passivating materials are used, shown in table 6.3, as they are tested in chapter 5. The FGA could not be performed after passivating the front side as it is planned for the wafer with AlO_X/SiN_X and SiN_X/SiN_X for FSF passivation, due to access limitation to the lab. A fluctuation in the fill factor values of wafer number 3 with SiN_X /SiN_X is observed as a result of SiN_X remains after dipping the wafer in HF before the metallization, therefore the best cell in

each wafer in this group will be compared with its counterparts. The wafer with a-Si:H/SiN_X has the champion cell in all wafers with a conversion efficiency of 21.04% and a high fill factor of 79%, while the V_{OC} is at 681mV indicating room for further improvement. Wafer number 5 with AlO_X /SiN_X has the best conversion efficiency of 19,4% for cell 4 with V_{OC} of 673 mV, which can be further improved by subjecting the wafer for FGA after passivating the front side according to the findings in chapter 5. The fill factor of the cells in wafer 5 represents a small series resistance due to the high annealing temperature with an average of 78.5%. The cell in wafer 3 with SiN_X/SiN_X as passivating layer shows also acceptable efficiency of 17.6% with J_{SC} of 36,3 (mA/cm^2) comparing to 37,5 and 37 (mA/cm^2) of a-Si /SiN_X and AlO_X/SiN_X respectively. The results of this group of wafers show a promising performance of cells passivated by SiN_X /SiN_X and AlO_X /SiN_X especially when the FGA process is carried out after passivating both sides of the cells while the a-Si /SiN_X is still the best with no need for FGA after passivating the front side as it deteriorates the passivation quality of the a-Si.

Table 6.3: the compared fabrication variables of wafers number 3, 4, and 5.

Wafer number	3	4	5
Annealing T	1050C	1050C	1050C
Front side passivation	SiN_X /SiN_X	a-Si /SiN_X	AlO_X /SiN_X
FSF Doping dose	1E+14	1E+14	1E+14

Table: 6.4 the external parameters of the best cells in wafers 3, 4 and 5.

Wafer nr	***V*oc**	***FF***	**J_{SC}**	**Efficiency**
	[mV]	**[%]**	**[mA/cm^2]**	**[%]**
3	668	70	36.3	17.6
4	681	78.9	37.5	21.04
5	673	78.5	37	19.4

6.5 The optical performance of IBC solar cells:

In order to investigate the optical performances of the IBC solar cell with the three different passivating stacks : a-Si /SiN_X, SiN_X/SiN_X, and AlO_X/SiN_X ,the external quantum efficiency (EQE) measurement is carried out. The spectral response of the samples provided with AlO_X/SiN_X could not be obtained properly, due to the property of the AlO_X layer. The AlO_X on the front builds an inversion layer on the FSF surface, which sinks the carriers that reach the FSF. Therefore, the EQE was low for short-wavelength light, as this light will be absorbed within the first a few um of the bulk. But for long-wavelength light, the EQE show higher spectral response as they generally reach the rear side of the cell where the BSF and emitter are, see figure 5.3. The obtained results of the two cells from wafers with FSF passivation by a-Si/SiNX, SiNX/SiNX are plotted in figure 5.3. It is shown that both cells have a large room for improvement. Nevertheless, the textured sample provided with a-Si /SiNX layer has a better optical response than the textured wafer with SiN_X/SiN_X, the related EQE is still low and could not exceed 94% in the wavelength range 500 to 900 nm, which indicate a recombination loss where the generated charge carriers are recombined before they are collected. In chapter 5, it is mentioned that to enhance the passivation quality when using only SiN_X, double SiN_X is deposited where we increase the Silicon content by increasing the gas flow of Silane and reducing NH_3 for the first deposited layer which has a thickness of 10 nm. This Silicon causes a parasitic absorption for the short wavelength and the wafer with a-Si/SiNX also experiences parasitic absorption for the blue response as is shown in figure 5.4. The wafer passivated by SiN_X/SiN_X has a lower Jsc with 36.3 mA/cm2 for cell 2 compared to its counterpart in wafer 4 which is passivated by a-Si/ SiN_X which obtained 39.2 mA/cm2. This is because the lower EQE is attributed to the insufficient passivation of the front side by using only SiN_X/SiN_X as reported previously in chapter 5 where the tested sample without FGA has an iV_{OC} of 686 mV and J0 of 44 fA/cm2.

The used mask for the metallization deposition has three different contact geometry designs with three different pitch sizes, see table 6.5, therefore the EQE measurement is performed for one cell from each group in wafer 4 to evaluate the performance of each design. Cell number 2 has the lowest pitch size of 300nm thus, the highest contacts number within the cell's area, while cell number 4 has the medium pitch size with 650nm and cell number 6 with the highest pitch size with 1200nm thus, the largest metal fingers as shown in figure 5.1. The results plotted in figure 5.4 show a slight improvement when the pitch size is smaller and experience higher $J_{SC\ EQE}$ with 39.2mA/cm^2 for cell number 2 and 38.8, 37.5 for cells number 4 and 6 respectively. This enhancement in the EQE can be explained by better carrier collection as a consequence of the larger number of contacts within the same cell area thus lower recombination and higher EQE. It is also important to mention that the light spot for EQE measurement is about 1x2mm^2. Thus it is not large enough to cover as many pitches as possible to minimize the recombination of the generated carrier at the surrounding dark area, especially when the FSF is conductive enough to support to electrons to diffuse around, therefore the EQE can be underestimated.

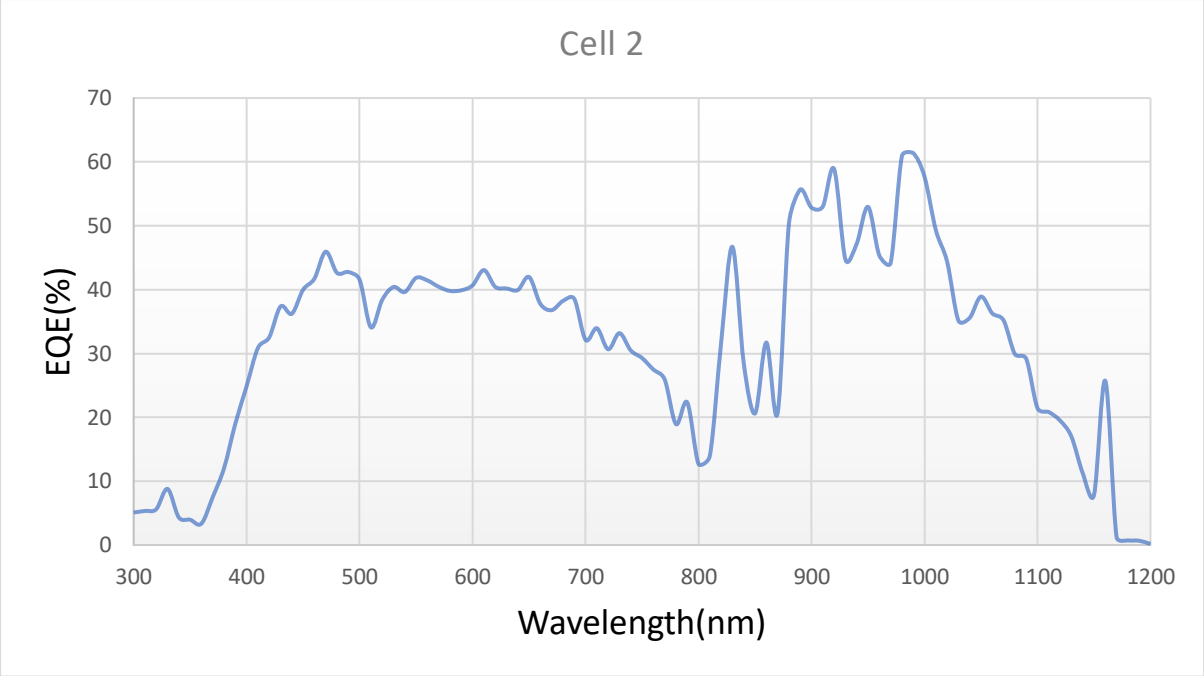


Figure 6.3: EQE measurement for cells number 2 of wafer 2 with AlO_X/SiN_X.

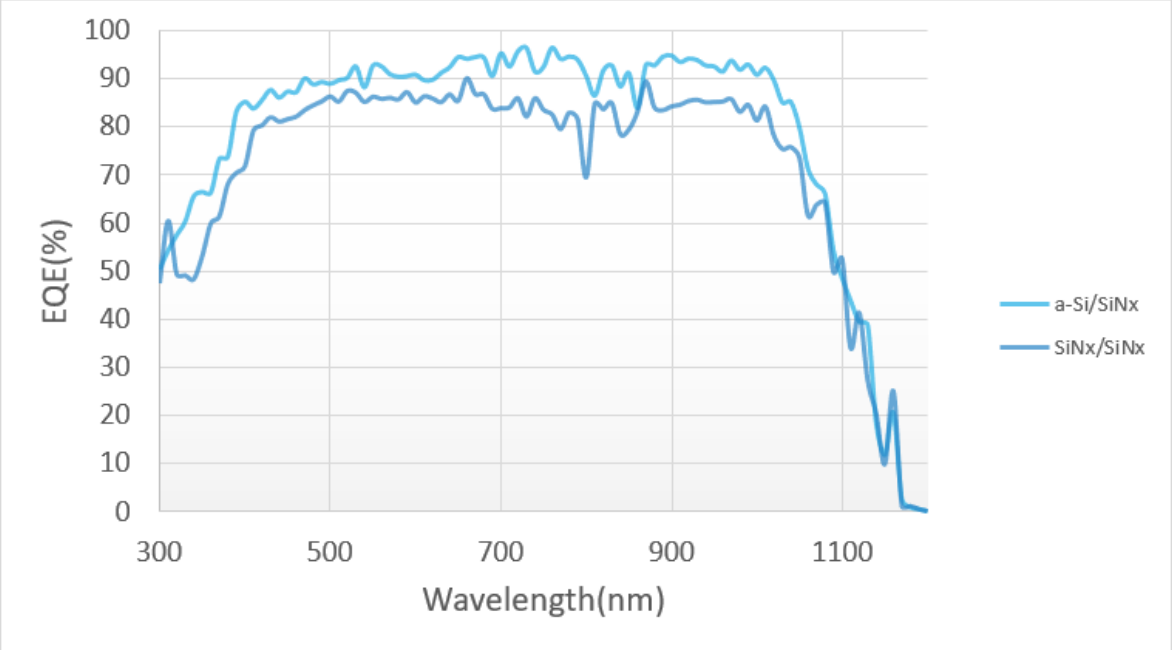


Figure 6.4: EQE measurement for cells number 2 of the wafer with a-Si/SiN_X and the wafer with SiN_X/SiN_X.

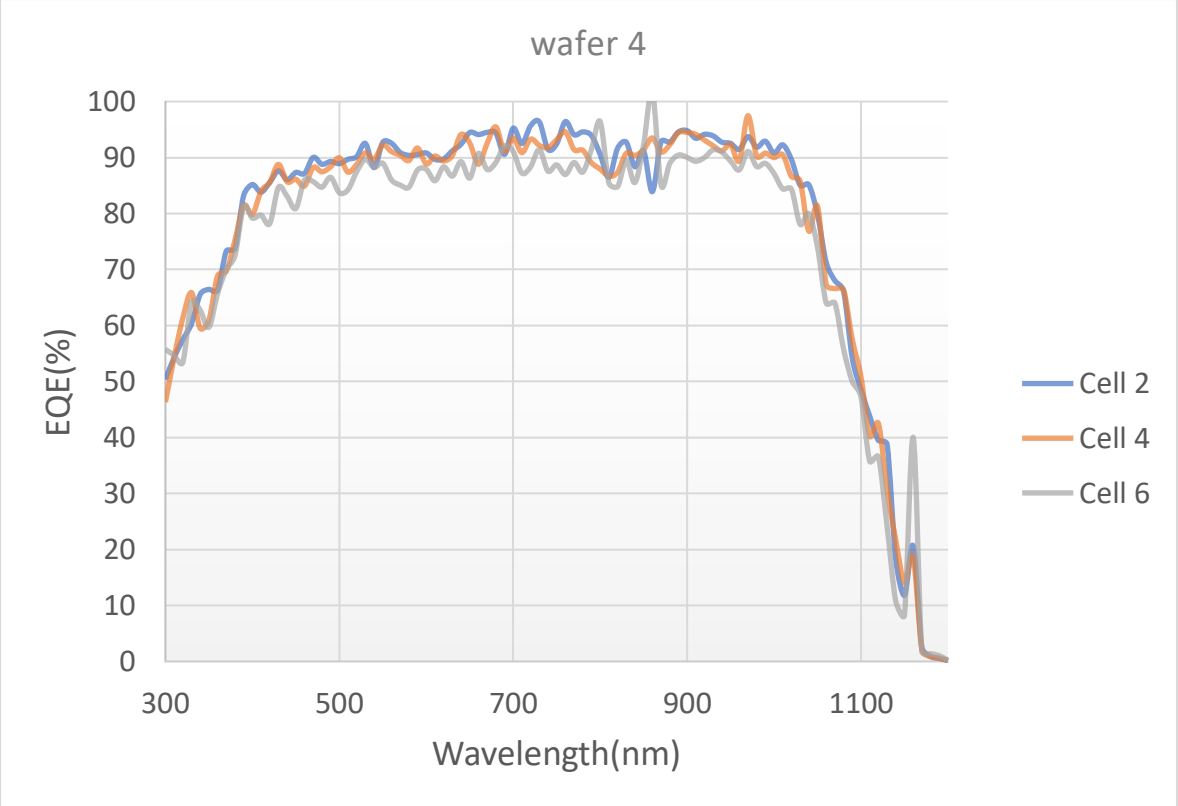


Figure 6.5: EQE measurement for cell 2,4 and 6 with pitch of xxx um from the wafer passivated by a-Si/SiN_X.

Table 6.5: Contacts geometry by cell type

Cell type	Type-A	Type-B	Type-C
Cell area (cm2)	4.04	4.09	4.18
Pitches	67.5	32.5	17.5
Pitch (um)	300	350	1200
Emitter width(um)	180	390	720
BSF width(um)	120	260	480

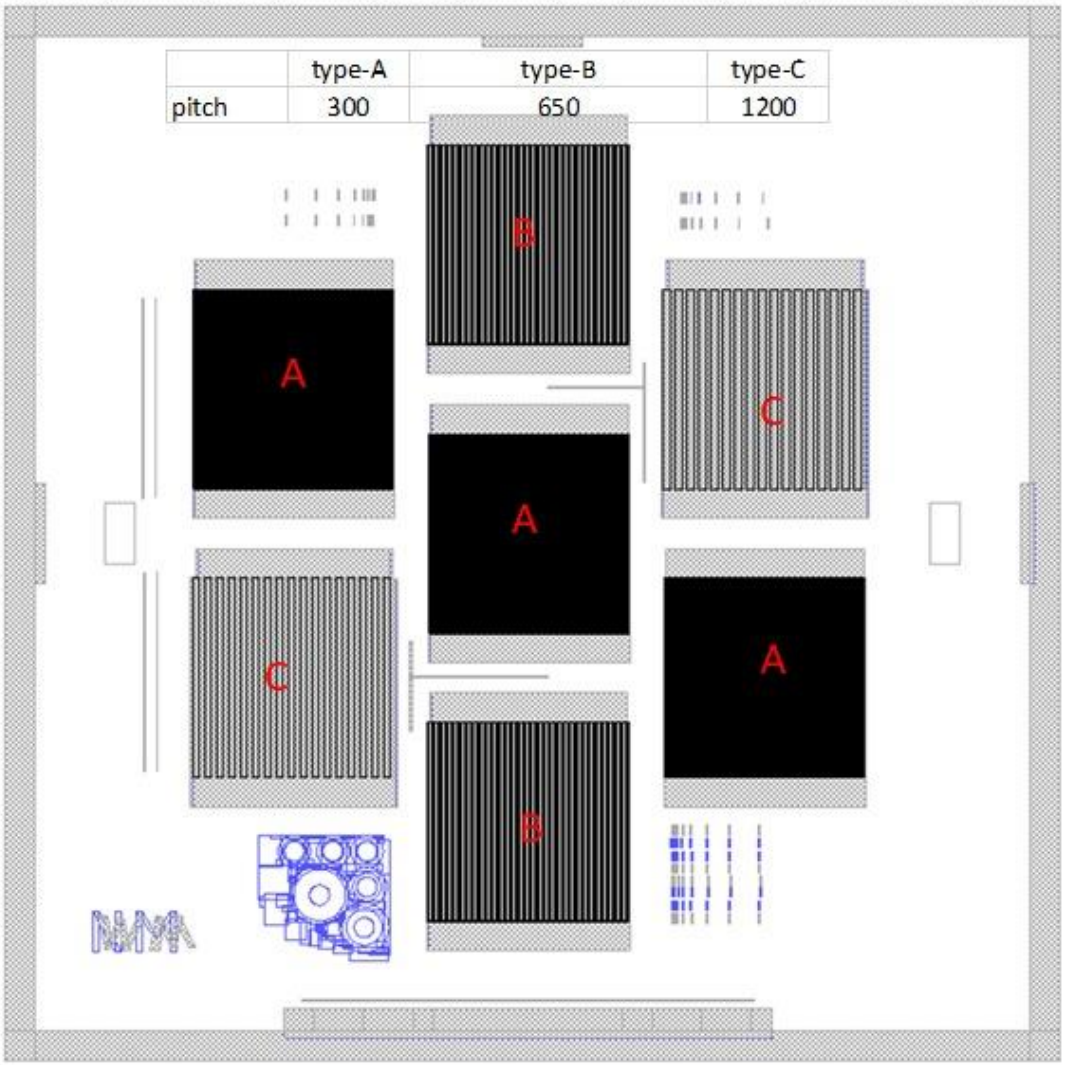


Figure6.6: Mask's geometry that is used to fabcricate the contacts

6.6 The influence of FSF on the performances of the cells:

The third group of wafers aimed to compare the effect of FSF on the cell's performance parameters. where one wafer is not doped and the other two wafers are doped with 1e14 and 3e14 respectively. Unfortunately, the wafer with a doping dose of 3e14(ions/cm2) is damaged during the fabrication and no output can be extracted from it. The rest two wafers show very close output as it is illustrated in table 6.6. The results show that cells with a doping dose of 1e14 exceed their counterparts in terms of V_{OC}. The doped

wafer experienced similar chemical passivation but assisted with an advantage of a slight field-effect passivation caused by light FSF doping comparing to the non-doped wafer. The filed effect passivation increases the J_{SC} as it repels the holes to the emitter thus reduce the recombination and more carriers reach the contacts. The blue response improved by the enhancement of the lateral conductivity associated with the doping. It is important to mention that a high level of doping dose increase Auger recombination near the surface thus reduce the passivation and the efficiency as a consequence.

Table 6.5: the compared fabrication variables of wafers number 5,6, and 7.

Wafer number	5	6	7
Annealing T	1050C	1050C	1050C
Front side passivation	AlO_X /SiN_X	AlO_X /SiN_X	AlO_X /SiN_X
FSF Doping dose	1E+14	no	3E+14

Table: 6.6 the external parameters of cells 2 in wafers 5, and 6.

Wafer nr	V_{OC} **[mV]**	***FF*** **[%]**	J_{SC} **[mA/cm^2]**	**Efficiency [%]**
5	673	77	36.5	18.9
6	667	76.7	35.7	18.2

6.7 Post metallization annealing:

The post-metallization annealing step that is tested in chapter 4 for the FBC cells showed that this process can enhance the fill factor of the cells as a result of enhancing the contact between the metals and the poly-Si contact thus enhancing the carriers transports. Therefore this process is also optimized in this section in order to increase the obtained IBC cell efficiency through enhancing the cell *FF.*

The process is carried out by placing the wafers on the hotplate with a temperature starts from 300°C to 550°C, the first few measurements after annealing at 300C and 400C for a short duration between 1 and 2 minutes did not show any enhancement which is consistent with the results obtained in chapter 4. When the temperature is raised to 450°C for the 1-minute duration the fill factor drops from 77.8 to 75.6, however, when repeating the step again for 2 minutes duration the fill factor recovers and starts increasing.

when the temperature is increased again to 550°C for 2-minute annealing duration the fill factor show a slight

improvement to reach in the end 78.8% for cell number 6 from wafer number 2 which has post-implantation annealed at 1030°C/1min. Regarding the open-circuit voltage, the performed annealing step did not cause any remarkable enhancement or degradation and the slight fluctuation can be attributed to the light exposure deviation during the IV measurement.

The same process is performed on other wafers like wafer number 5 and wafer number 4 which includes the cell with the highest obtained efficiency, both wafers show the same trend where just the fill factor could increase by 1% and thus the best-obtained cell reach a conversion efficiency of 22,15% with a fill factor of 79.7% , a V_{OC} at 680 mV and a J_{SC} at 37.5 mA/cm^2.

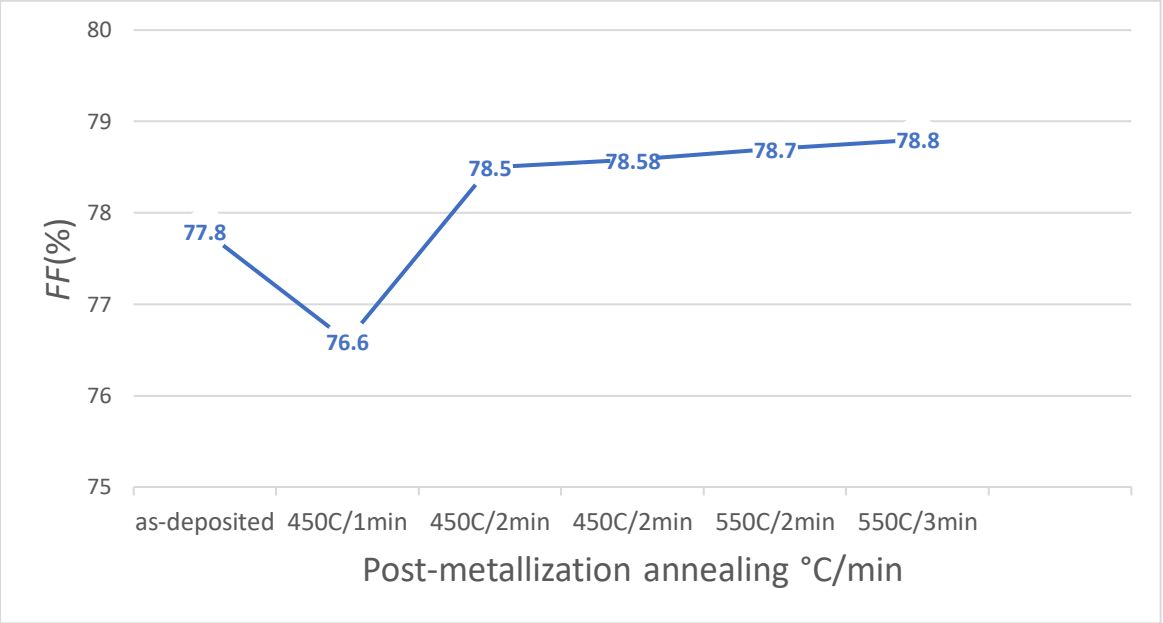


Figure 6.7: Fill factor of cell number6 of wafer 2 as a function of the post metallization annealing with a hotplate.

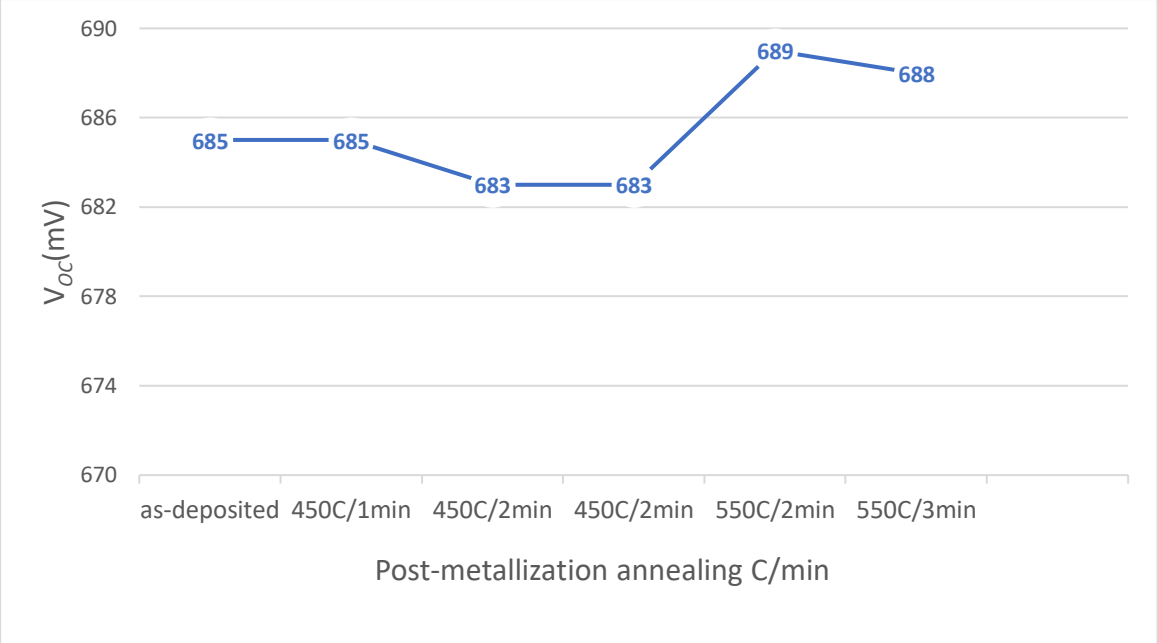


Figure 6.8: V_{OC} of cell number6 of wafer 2 as a function of the post metallization annealing with a hotplate.

6.8 Conclusion:

In this chapter, the fabricating flowchart of IBC solar cells is discussed and detailed. The IBC cells were prepared with the aim of study the influence of the following on the cells' performance: 1) the high-temperature annealing, 2) the surface's passivating structure, 3) the FSF implantation dose.

In the first group of IBC solar cells, for the research question (1) of the influence of the annealing temperature: three wafers are annealed for one minute at different temperatures 1000°C,1030°C, and 1050°C respectively. The obtained results show that increasing the post-implantation annealing temperature leads to enhance the fill factor as a result of the formed pinholes in the oxide layer. The pinholes facilitate carrier transportation thus decreasing the series resistance between the poly-Si and the c-Si. The best-obtained V_{OC} in this group was 685mV with a conversion efficiency of 20.5% for the cell number 6 on the wafer co-annealed at 1030°C for one minute, indicating that there is still a place for improvement and the passivating contacts should be further optimized.

The second group of IBC solar cells, for the research question (2): in order to investigate the influence of different front side passivating structures on the cell performances, double stacks as FSF passivation layers are tested: SiN_X/SiN_X, a-Si/SiN_X , and AlO_X/SiN_X. The passivated wafer with a-Si/SiN_X has the champion cell of all the wafers with a conversion efficiency of 21.4%, a V_{OC} of 681mV and a fill factor of 78.9%. while the wafer passivated with SiN_X/SiN_X shows lower output due to the ineffective passivation of the SiN_X/SiN_X to the FSF. whereas the one with AlO_X/SiN_X as passivating stack for FSF has an efficiency of 19.4% with a V_{OC} 673 mV. The

Moving to the third group, it is planned to evaluate the influence of the implantation dose of phosphorous to the front surface field on the IBC solar cells' performance. One wafer is doped with 1e14(ions/cm2) whereas the second wafer is undoped. The wafer with the FSF shows better output comparing to the undoped wafers since FSF suppresses the electrical shading and the doping reduces the sheet resistivity thus enhancing the lateral conductivity.

Finally, post metallization annealing treatment is carried out to study its effects on the fill factor. The conversion efficiency of the champion cell reaches 22.15% from 21.04% before annealing, as a result of the increase in the fill factor from 78.9% to 79.7%. and it is concluded that this process can slightly increase the fill factor when subjecting the wafers to a temperature higher than 400°C for a short time duration.

7

CONCLUSIONS AND OUTLOOK

This master project aims to fabricate high-efficiency IBC solar cells by utilizing thermal-SiO_X in ion-implanted poly-Si passivating contacts. To enhance the electrical properties of the cells effective passivation is needed to minimize the recombination loss, the optical properties are improved by texturing the surfaces of the cells and adapting an anti-reflection coating AR. In this section, the main conclusions of the performed work are presented and finally, recommendations are given for further enhancement of future works.

7.1 Conclusions:

Firstly, the performance of the poly-Si passivating contacts is evaluated for the following poly-Si contacts' structure: the thickness of 250 nm, fixed implantation energy of 20 keV, and implantation dose of phosphorous 6e14 ions/cm^2 for n^+ contacts (BSF) and Boron with 5e14 ions/cm^2 for p^+ contacts (emitter). An ultra-thin layer of 1.5 nm of t-SiO_X is introduced between the bulk and the poly-Si contacts as a tunneling layer. In this work, the poly-Si passivating contact structure with t-SiOx is tested with different annealing conditions of 950°C/5min, 1000°C/1min, and 1050°C/1min. The annealing time and temperature have significant importance as it activates and drives in the dopants inside the poly-Si, thus determining the doping profile. The doping profile of the poly-Si contacts is crucial for the passivation quality. It is based on the fabricating parameters in terms of the poly-Si thickness the implantation dose, the implantation energy, and the post-metallization annealing conditions. The high-temperature annealing is also critical on the t-SiO_X tunneling layer since the high-temperature forms pinholes, and the right amount of pinholes is required to achieve high passivation and low contact resistance at the same time. The results of the symmetrical passivation test samples show increasing in the passivation as the annealing temperature increase. An iV_{OC} of 728 mV is obtained for n^+ poly-Si contact at annealing conditions of 1050°C for 1

minute which was the best-obtained result, while for the p^+ poly-Si contact at the same annealing conditions 699 mV is obtained.

In order to fabricate high-efficiency solar cells, the front side of the cells has to be optimized. To achieve that in this work we utilize different concepts like texturing the surface to enhance the light absorption, FSF to increase the lateral conductivity and repels the holes to the emitter, and passivating the front side with different passivating stacks. The results of symmetrical tests samples show very good passivation for the sample passivated with a-Si/SiN_X stack with implantation dose of FSF at 1e14 ions/cm^2 with iV_{OC} of 714 mV and a J_0 of 7.5 fA/cm^2. The rest samples with AlO_X/SiN_X, and SiN_X/SiN_X show lower passivation quality with iV_{OC} of 708 mV and 686 mV respectively. The influence of the FGA on the surface passivating contacts is also carried out. A Positive impact of the FGA on the samples with AlO_X/SiN_X, and SiN_X/SiN_X is shown as they experienced an increase in the iV_{OC} with 7 and 9 mV respectively. The low thermal stability of a-Si:H leads to a decrease in the passivation with 35 mV.

Then three groups of IBC solar cells are fabricated to evaluate the annealing temperature, the surface passivating materials, and the implantation dose of the FSF. The findings of the first group show an increase in *FF* when increasing the annealing temperature and the best FF was 79.3% for the wafer annealed at 1050°C for 1 minute. This increase is attributed to the formed pinholes in the t-SiO_X layer which facilitate the carrier transportation thus decreasing the contact resistance.

The influence of the surface passivating materials obtains the best results for the wafer passivated with a-Si/SiN_X stack with an efficiency of 21.04% and J_{SC} of 37.5 mA/cm^2. The passivating materials of AlO_X/SiN_X, and SiN_X/SiN_X obtain conversion efficiency of 19.4% with J_{SC} of 37 mA/cm^2 for the AlO_X/SiN_X and 17.6% with J_{SC} of 36.3 mA/cm^2 for the SiN_X/SiN_X. This difference in the output is owed to the difference in the passivation quality as tested in chapter 5. The EQE measurement shows high parasitic absorption for the wafers passivated by a-Si/SiN_X and SiN_X/SiN_X as a result of the high absorption coefficient of silicon for short wavelength.

The last group of wafers is aimed to evaluate the role of the FSF on the cells' performance. The results obtained for the wafer with none-implanted surface were compared with the one that has surface P implantation with a dose of 1e14 ions/cm^2. THE FSF in the IBC cell structure leads to an increase in the conversion efficiency by suppressing the electrical shading. The sample with FSF has a slight better passivation, lead to increase the V_{OC}. The obtained values are V_{OC} of 673 mV for the doped wafer while the non-doped wafer has a V_{OC} of 666 mV.

7.2 Outlook :

Even though, IBC solar cell with efficiency as high as 22.15% is obtained, there is still a large room for further improvement. In this section, several insights are given to further enhance the conversion efficiency of the IBC cells.

1-The passivating contacts' structure: in this work the p^+ poly-Si contacts have considerably lower iV_{OC} than their counterparts of n^+ poly-Si contacts. Due to the long maintenance time of the implanter, it was not possible to test different Boron implantation doses or variable implantation energies. Finding the optimal implantation parameters associated with the poly-Si thickness is a key factor to obtain the best passivation. The poly-Si thickness, the implantation parameters, and the annealing conditions all together

define the doping profile, thus the passivation quality. Therefore, it would be very useful to initiate a database for the passivation tests conducted in the group to ease the efforts to reach the best passivation quality.

2-t-SiO_X growth condition: from the obtained results of the contacts resistivity measurement, it is shown that passivating contacts with t-SiO_X have higher contact resistivity than the ones provided with NAOS SiO_X [35]. Therefore, there is a need for further optimization of the tunneling layer to enhance the fill factor and maintain the high V_{OC} at the same time.

3-Short current density J_{SC}: the maximum measured J_{SC} by the EQE was 39.2 mA/cm^2 indicating a place for optimizing the front side of the cell in terms of the implantation dose of the FSF and the passivating materials. An optimum FSF should be found for each passivating material individually since the passivating materials have different types and amounts of fixed charge Qf. Material with a wide bandgap like SiO_X also should be evaluated to replace passivating layers with a high absorption coefficient like a-Si:H or utilizing a thinner film of a-Si:H to reduce the parasitic absorption.

4-In chapter 5, it is found that FGA can boost the FSF passivation quality with passivating stacks like AlO_X/SiN_X and SiN_X/SiN_X. However, in this work, the IBC cells were not subjected to the FGA after passivating the front side due to access limitation to Kavli lab. It is recommended to shift the FGA step when hydrogenating the backside to do it after passivating the front side with AlO_X/SiN_X and SiN_X/SiN_X. Performing the FGA at lower temperature or shorter time duration should be evaluated for a-Si/SiN_X stack to optimize the flow chart depending on the output.

5-Metallization: the metallization process is crucial to achieving a high fill factor, and since the metal grid in IBC cells is on the rear side, a thicker layer of metal can enhance the fill factor without compromise other parameters. Another approach would be to use material with higher conductivity than Al like electoral plated copper.

6-Fabricating at least two wafers for each IBC structure to compare in case of fluctuating cell performance due to contamination during the fabrication, or any other process mistake. It is also useful to avoid losing part of the results when the only wafer is damaged or broken during the fabrication process.

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