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A Transformer Isolated Driving Method for SiC MOSFETs with a Constant Negative Off Voltage

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***Abstract*—SiC MOSFETs have become more and more popular in recent years. Apart from its superior performance, attentions should be paid to its driving method. In this paper, an improved transformer driving circuit is proposed which can provide an almost constant negative turn-off voltage within a wide duty-cycle range. Both simulation and experimental results are given to verify the effectiveness of this method.**

***Index Terms*—SiC MOSFETs, Driving Transformer, Negative Off Voltage, MOSFETs in Series**

I. Introduction

Over the past 10 years, SiC power MOSFETs manufacturing technology has experienced a rapid development [1]. SiC MOSFETs have many advantages over Si MOSFETs like faster speed, higher breakdown voltage, lower on-resistance, high operation temperature and so on [2]. In commercial market of auxiliary power supply, e.g. for up to 200 W single or two switches Flyback or Forward based converter for the low voltage (LV) grid-connected application, the commonly used breakdown voltage for Si MOSFET is as high as 1.4 kV. A SiC MOSFET based power supply for this market can be constructed with 1.7 kV rated devices. Therefore, SiC MOSFET is becoming a more popular choice, particularly in the medium voltage (MV) markets. Although, SiC MOSFETs have many advantages, special attentions should be paid to its driving method. The threshold voltage of SiC MOSFETs tends to show a negative temperature coefficient which means a higher device temperature leads to a lower threshold voltage to turn device on [1], [3]. Therefore, a negative turn-off voltage is suggested. Besides, using negative turn-off voltage helps reduce the turn-off losses further since it enables faster charge extraction from the device parasitic capacitances [4].

In medium voltage applications, for example, when the DC bus voltage is 3 kV, several MOSFETs can be connected in series to make a high voltage switch. Compared with single MOSFET or IGBT switch with a high breakdown voltage, series-connected MOSFETs excel in aspects like lower equivalent on-resistance, lower equivalent output capacitance, and faster switching speed. Also, design and operation of a single switch in high voltage applications is quite challenging due to the high dV/dt [5]. Therefore, using several low voltage MOSFETs to make a high voltage switch is promising. However, when the MOSFETs are connected in series, some of the source terminals are not at common ground potential. Thus, in order to drive them successfully, a driving transformer can be selected as a suitable choice.

The main contribution of this paper is that an improved transformer isolated driving method is proposed which has a constant negative off voltage for SiC MOSFETs over a wide duty-cycle range. The paper is organized as follows, in section II, different transformer based driving methods will be summarized and analyzed. In section III, a proposed circuit will be given with analysis. In section IV, the simulation results are given. The simulation uses both a pure capacitor and LTspice model for simulation. Section V shows the experimental results of the proposed circuit. Finally, section VI concludes this article.

II. Different Transformer Based Driving Methods

A possible way to drive MOSFETs with a transformer is shown in Fig. 1 [6].

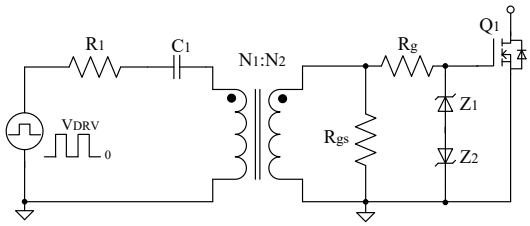

Fig. 1. Possible Driving Transformer Method

The capacitor C_1 is used to prevent the magnetic saturation of the driving transformer and R_1 is used to accelerate the transient process. However, the turn-on voltage of Fig. 1 will change with the duty-cycle. With a higher duty-cycle, the turn-on voltage will become smaller which is not desirable.

At steady state, the DC voltage across C_1 is dV_{DRV}. d is duty-cycle and V_{DRV} refers to the peak voltage of the unipolar pulse width modulation (PWM) at the input. Suppose the transformer is ideal without leakage inductance, then
The gate source turn-on voltage is:

$$V_{gs,H} = (1-d)V_{DRV}\frac{N_2}{N_1} \tag{1}$$

The gate source turn-off voltage is:

$$V_{gs,L} = -dV_{DRV}\frac{N_2}{N_1} \tag{2}$$

N_1 and N_2 are the turns number of the transformer's windings. Therefore, from (1), a higher duty-cycle leads to a lower turn-on voltage.

Fig. 2 shows an improvement with a DC restore capacitor at the transformer secondary side [6].

Due to the existence of C_2 and D_1, the gate source turn-off voltage is 0 V and the gate source turn-on voltage is:

$$V_{gs,H} = V_{DRV}\frac{N_2}{N_1} \tag{3}$$

However, it has a limitation that the gate source voltage V_{gs} has many oscillations when it turns on, i.e., superimposed voltage oscillations can cause aging of the MOSFET's gate oxide. Secondly, this driving voltage is non-negative when the MOSFET is off. Another point worth mentioning is that when the duty-cycle becomes smaller, the turn-off voltage tends to be slightly above zero. This is not recommended to the SiC MOSFETs which usually need a negative turn-off voltage to shut down robustly.

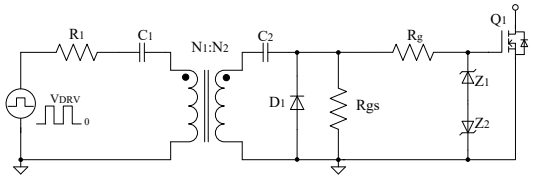

Fig. 2. Driving Transformer with a Secondary Side DC Restore Capacitor

Fig. 3 shows a driving circuit which can provide a negative turn-off voltage [7].

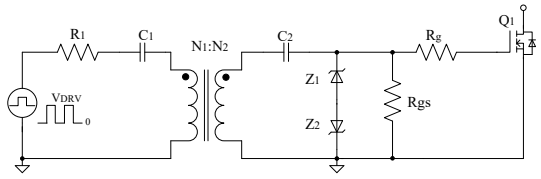

Fig. 3. Driving Method providing Negative turn-off voltage

The difference between the two circuits in Fig. 2 and Fig. 3 is that the diode D_1 at the secondary side is removed and replaced by two zener diodes. The minimum turn-off voltage in Fig. 3 is limited by the zener diode Z_2. Z_2 clamps the driving voltage when the duty-cycle becomes larger, thus ensuring enough turn-on voltage. Besides, the negative turn-off voltage guarantees the reliable shutdown of the SiC MOSFETs. However, the amplitude of the negative turn-off voltage will change with the duty-cycle especially at low duty-cycle situations when this value is actually not clamped by Z_2 and this value is expressed by (2) if the transformer is ideal without leakage inductance.

Reference [8] proposes an isolated gate driver for SiC MOSFETs with a constant negative off voltage. However, besides the driving transformer, another two series-connected transformers were also needed to comprise the duty-cycle compensation circuit. This increases the complexity of the driving circuit. An overview of gate driving circuits for SiC MOSFETs with a comparison of four different gate drivers was presented in [9].

III. Proposed Circuit and Analysis

The proposed driving circuit which can provide a constant negative turn-off voltage over a wide duty-cycle range and less gating voltage oscillations is shown in Fig. 4.

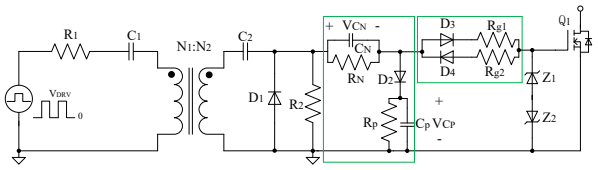

Fig. 4. Proposed Driving Circuit

The left encircled part is used to generate a negative turn-off voltage [10]. The main contribution of the proposed circuit is the combination of the driving transformer (C_2 and D_1 included) and this negative off voltage generation circuit.

The basic idea of the left encircled circuit is that when the PWM is on, diode D_2 conducts for a short time, so the voltage across C_P together with the input pulse will drive the MOSFETs on. When the gating signal turns off, the voltage across C_N will turn off the MOSFET which is a negative voltage.

The turn-on voltage is given by:

$$V_{gs,H} = V_{C_P} = \frac{R_P}{R_P + R_N}\frac{N_2}{N_1}V_{DRV} \tag{4}$$

The turn-off voltage is:

$$V_{gs,L} = -V_{C_N} = -\frac{R_N}{R_P + R_N}\frac{N_2}{N_1}V_{DRV} \tag{5}$$

The voltage drops of the diodes are neglected here.

The selection criteria for R_N, C_N, R_P, C_P can be found in [10], which is summarised as: $C_P \gg C_{gs}$, $C_N \gg C_{gs}R_P/R_N$, $R_NC_N \gg T_s$ and $R_PC_P \gg T_s$. Here, T_s is the switching period and C_{gs} represents the MOSFET input capacitance.

In [11], a similar technique is also proposed to generate a negative turn-off voltage which can be used to replace the left encircled part. However, from simulation, the negative turn-off voltage deviates from the idealized value when the duty-cycle changes.

The right encircled part is used to adjust the turn-on and turn-off speed. Besides, it can also help to attenuate the oscillations of the gate driving voltage quickly which will be shown by the simulation results in section IV.

IV. Simulation Results

The simulation result is first built in PLECS simulation software with a pure capacitor as its load. Simulation results of different circuits are compared. For the readers' convenience, the circuits are given in Fig. 6, Fig. 8, and Fig. 13

with corresponding parameters. Later, simulation results are also given in LTspice implementing a commercial accurate dynamic MOSFET spice model.

A. MOSFET model Using a Pure Capacitor

The MOSFET used here is the C2M1000170D with a gate capacitance of approximately 200 pF according to its datasheet [3]. Therefore, the load capacitor is set as 200 pF. A transformer model shown in Fig. 5 [12] is adopted for simulation. With a reference to [13], the magnetizing inductance L_m of the transformer is set as 1 mH with turns ratio 1:1. L_{r1} and L_{r2} are both set as 10 µH to act as the leakage inductance which will be explained in section V.

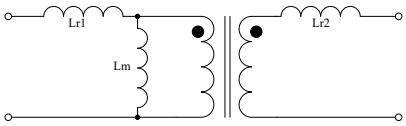

Fig. 5. Transformer model used in simulation

Firstly, the simulation results of Fig. 6 with and without two oscillation damping diodes are given in Fig. 7. V_F is the forward voltage drop of the diode, V_z is the breakdown voltage of the zener diode. The switching frequency f_s is 40 kHz.

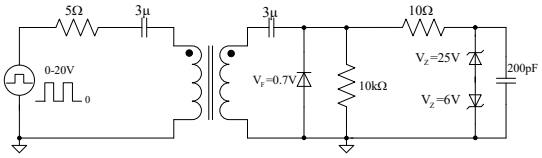

Fig. 6. Parameters of Driving Transformer with DC restore Capacitor

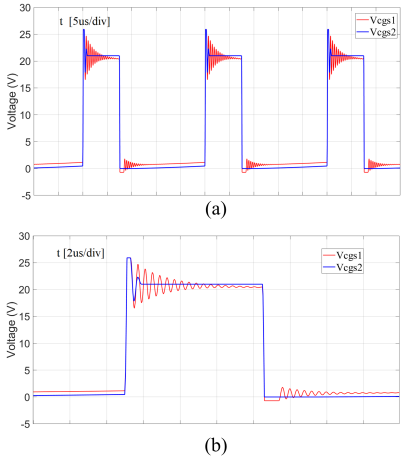

Fig. 7. (a) V_{cgs} under 0.3 duty-cycle. (b) Zoom-in of (a)

In Fig. 7, V_{cgs1} is the capacitor voltage obtained without implementing the gate diodes and V_{cgs2} is the capacitor voltage with the diodes. As it can be seen, the addition of the two diodes helps to damp the voltage oscillations more quickly.

Next, three different circuits are compared, they are: driving transformer circuit with a DC restore capacitor shown in Fig. 6, the proposed circuit shown in Fig. 4 without D_3 and D_4, and the final proposed circuit shown in Fig. 8.

The proposed circuit with parameters is shown in Fig. 8 with R_{g1} and R_{g2} both 10 Ω.

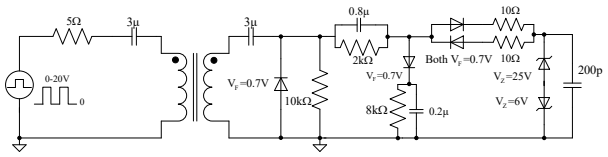

Fig. 8. Proposed Circuit with parameters

From Fig. 8, based on (4) and (5), the turn-on voltage is 16 V and turn-off voltage is -4 V.

Simulation results under 0.1, 0.3, 0.5 and 0.8 duty-cycle conditions are given in Fig. 9–Fig. 12. The switching frequency f_s is still 40 kHz. V_{cgs1} refers to the capacitor voltage of Fig. 6, V_{cgs2} refers to the capacitor voltage of the proposed circuit without diodes D_3 and D_4, V_{cgs3} refers to the capacitor voltage of the proposed circuit.

Fig. 9 shows the results under 0.1 duty-cycle. As can be seen from V_{cgs1}, the turn-off voltage is larger than 0 V and the oscillations at off transient may act as spurious triggering pulses.

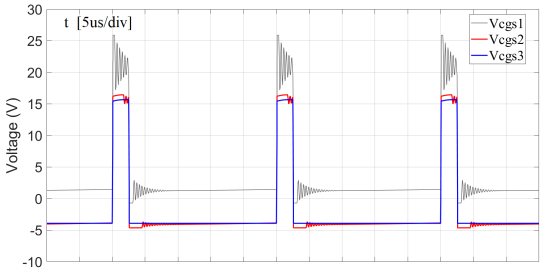

Fig. 9. V_{cgs} under 0.1 duty-cycle.

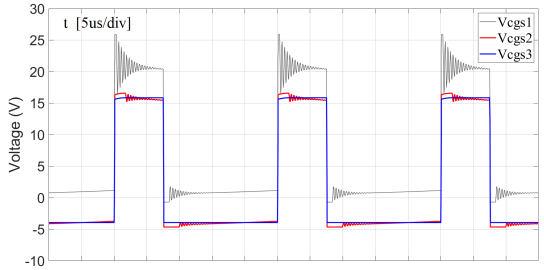

Fig. 10. V_{cgs} under 0.3 duty-cycle.

Based on the simulation results depicted in Fig. 9-Fig. 12, the proposed circuit achieves the goal of providing a constant turn-off voltage under a wide duty-cycle range. Although, the two diodes D_3 and D_4 help eliminate the oscillations, the main

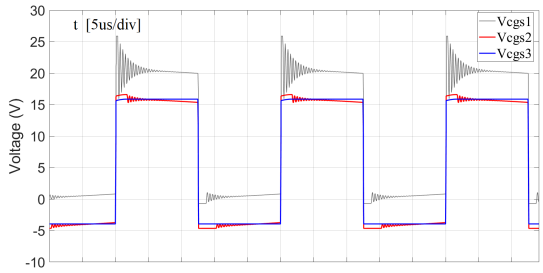

Fig. 11. V_{cgs} under 0.5 duty-cycle.

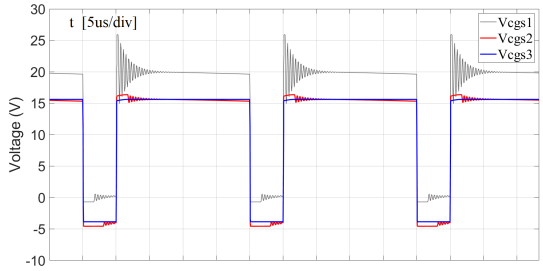

Fig. 12. V_{cgs} under 0.8 duty-cycle.

damping of the oscillations is achieved through the R_N, C_N, R_P, C_P part shown in Fig. 4.

Finally, the simulation result of Fig. 3 is also given. This simulation intends to show the possible spurious triggering pulses in low duty-cycle situations even when the steady off voltage level is below 0 V. The parameters of Fig. 3 is given in Fig. 13.

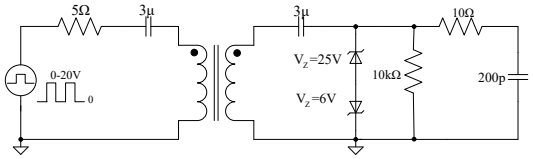

Fig. 13. Component parameters of Fig. 3

The simulation results are presented in Fig. 14 and Fig. 15 when the duty-cycle is 0.1 and 0.3.

In Fig. 14 and Fig. 15, V_{cgs1} is the capacitor voltage of Fig. 13, V_{cgs2} is the capacitor voltage of Fig. 13 with two damping diodes and V_{cgs3} is the capacitor voltage of the proposed circuit.

As mentioned in section II, low duty-cycles tend to generate spurious gate pulses at off transients more easily which can also be proved by the simulation results of Fig. 14 and Fig. 15.

Therefore, from the simulation results, the proposed circuit improved the driving voltage in mainly two aspects, firstly, it provides a constant negative turn-off voltage for reliable shutdown of the SiC MOSFET. Secondly, it reduces the oscillation greatly in a way without slowing down the switching speed. When there is no driving signal, the voltage on gate source capacitor can discharge through R_{g2}, D_4, R_N and R_2

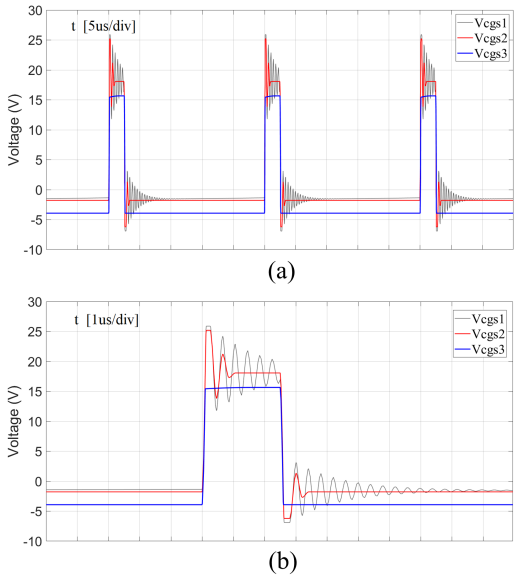

Fig. 14. (a) V_{cgs} comparison under 0.1 duty-cycle. (b) Zoom-in of the transients.

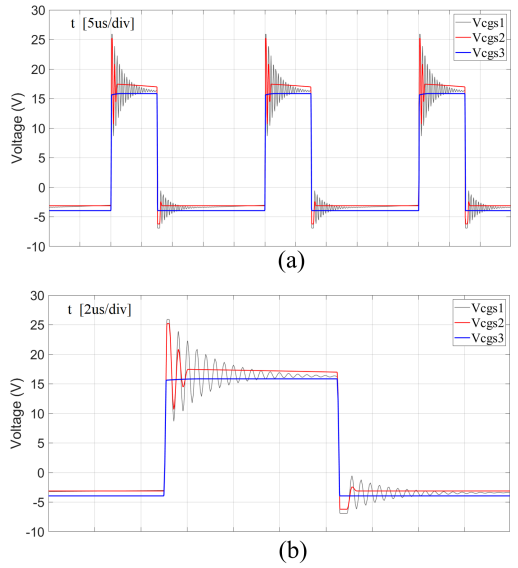

Fig. 15. (a) V_{cgs} comparison under 0.3 duty-cycle. (b) Zoom-in of the transients.

as shown in Fig. 4. Therefore, it will not turn on the MOSFET by default.

B. Using LTspice Model

In order to get a more accurate result, simulation was also done in LTspice. Here, only the proposed circuit is simulated. The LTspice model of C2M1000170D can be downloaded from the website of Cree [14]. The proposed circuit is simulated in a Flyback converter with the schematic and parameters shown in Fig. 16. Here, the transformer has two outputs which can drive two MOSFETs in series simultaneously and it can be used in MV applications. The experiment was also tested using two MOSFETs.

The results of gate source voltage are given in Fig. 17 when the duty-cycle is 0.3, 0.5 and 0.7. The inductance of the driving transformer is 1 mH:1.78 mH:1.78 mH which means the turns ratio is 1:1.33:1.33.

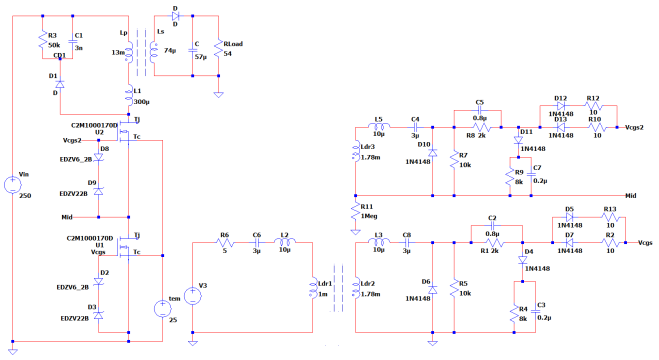

Fig. 16. Simulation Schematic in LTspice

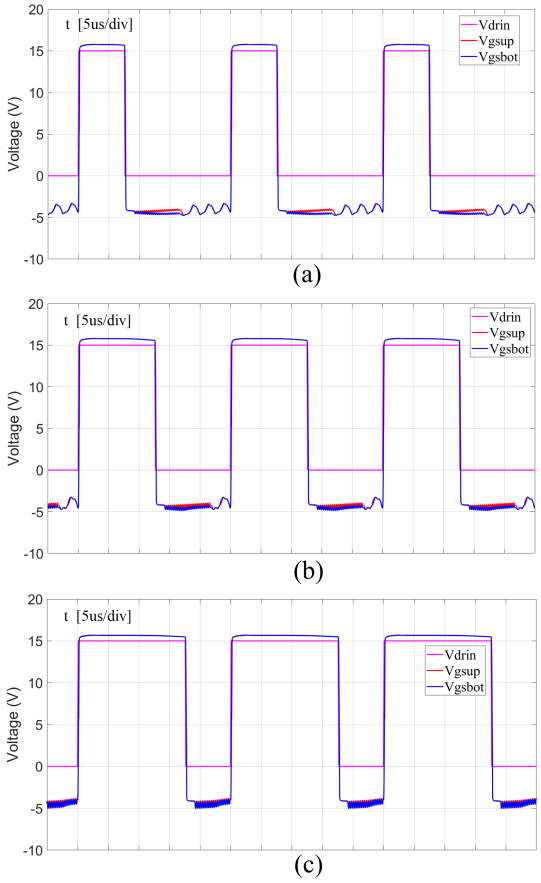

Fig. 17. LTspice simulation result. (a) 0.3 duty-cycle. (b) 0.5 duty-cycle. (c) 0.7 duty-cycle.

In Fig. 17, V_{drin} is the input driving voltage, V_{gsup} is the gate source voltage of the upper MOSFET, V_{gsbot} is the one of the lower MOSFET. The turns ratio 1.33:1 helps boost the driving voltage from 15 V to 20 V. From the simulation results in LTspice, the driving voltage has a constant turn-off voltage which is -4 V even when the duty-cycle changes. As for the oscillations in V_{gs} when it turns off, it happens when the MOSFET drain source voltage V_{ds} starts to oscillate which can be referred to Fig. 18, this oscillating voltage will result in a coupling current through C_{gd} between the drain and gate terminals of the MOSFET. This current will go back and forth through the diodes D_3 and D_4, therefore, there will be some oscillations of V_{gs}. However, the gate source voltage will also be clamped by diodes D_3 and D_4 which means the oscillation magnitude is around $2V_F$. For the turn-on voltage, there is no oscillations. During simulations, if extra gate source capacitances are added, there may exist a small overshoot at the very first beginning of the turn-on transient, however, it will not cause a problem.

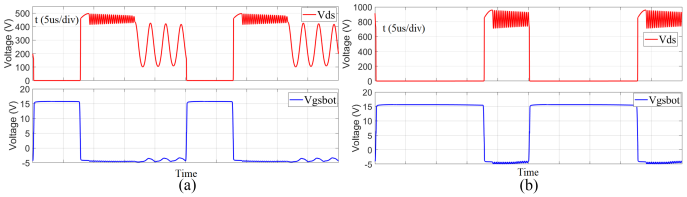

Fig. 18. V_{ds} and V_{gs} waveforms. (a) 0.3 duty-cycle. (b) 0.7 duty-cycle.

V. Experimental Verifications

A verification driving circuit based on Fig. 4 was built. The parameters are: $R_1 = 4.7\ \Omega$, $R_2 = 10$ kΩ, $R_N = 2$ kΩ, $R_P = 8.2$ kΩ, $R_{g1} = R_{g2} = 10\ \Omega$, $C_1 = C_2 = 4.7$ µF, $C_N = 1$ µF, $C_P = 0.22$ µF. The breakdown voltage of Z_1 and Z_2 are 22 V and 6.8 V respectively. All the diodes are 1N4148. The transformer was built with a toroidal ferrite core. The turns ratio of the transformer is 14:18:18 with measured inductance of 940.6 µH, 1559.9 µH and 1559.3 µH respectively at 10 kHz. The primary leakage inductance measured when shorting the two output windings is 18.8 µH which explains the value selection of leakage inductance for the simulation in section IV. The inductance is measured with Keysight U1733C LCR meter.

Fig. 19 shows the picture of the built driving circuit.

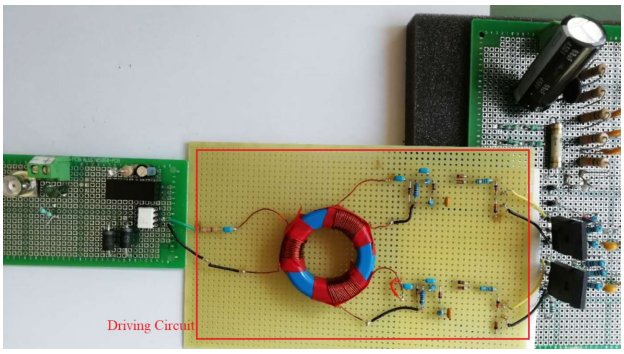

Fig. 19. Picture of the built driving circuit

This driving circuit was used to drive the two series connected MOSFETs in the Flyback converter. The picture of the experimental setup is shown in Fig. 20. The driving circuit

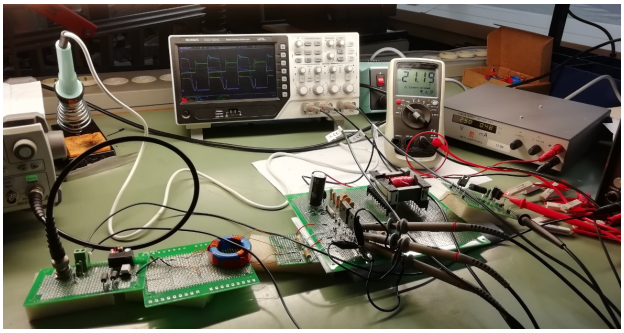

Fig. 20. Picture of the experimental setup

needs to be replaced by the one in Fig. 19 to achieve the results shown in Fig. 21.

The test condition is: Input voltage V_{in} is 250 V, load resistor is 54 Ω and switching frequency is 40 kHz.

The gate source voltage V_{gs} and V_{DRV} waveforms are tested and measured at different duty-cycles and the results are shown in Fig. 21.

In Fig. 21, V_{gs} is measured from the lower MOSFET. As can be seen from the experimental results, V_{gs} has almost a constant negative turn-off voltage under different duty-cycles which ensures a reliable shutdown of SiC MOSFETs.

VI. Conclusion

In this paper, an improved driving method using pulsed transformer is proposed. This circuit is benchmarked against state-of-art solutions by means of circuit simulations and the results show the proposed circuit has superior performance in terms of stable gate voltages and well attenuation capability for the ocillating voltages across the gate-to-source terminals of the device when different operational duty-cycles are considered. Finally, a prototype driving circuit was built to verify the idea. This driving circuit is used in a Flyback converter. The testing results show that the proposed circuit can provide a constant turn-on and turn-off voltage over a wide duty-clcle range. The results indicate that the proposed circuit is a good choice for driving the SiC MOSFETs with an electrical isolation and with a relatively low cost. Besides, more than one MOSFETs connected in series can be driven simultaneously with a driving transformer.

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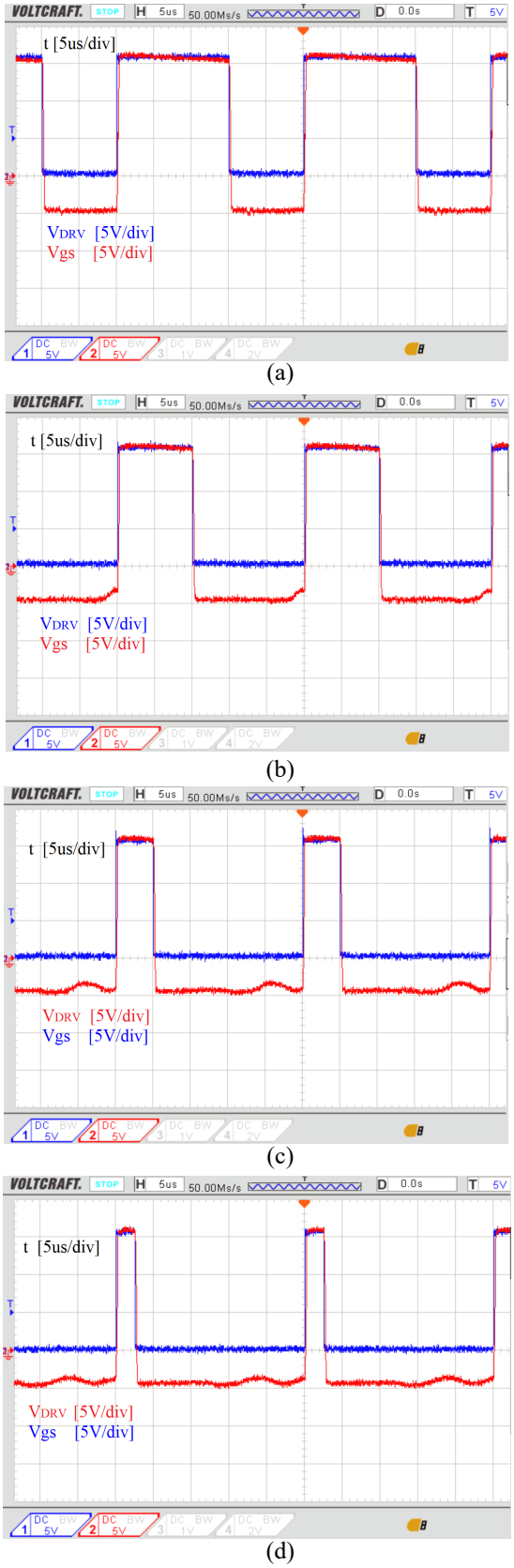

Fig. 21. V_{gs} and V_{DRV} experimental results. (a) 0.6 duty-cycle. (b) 0.4 duty-cycle. (c) 0.2 duty-cycle. (d) 0.1 duty-cycle.

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