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Optimized algorithm of active injection circuit to calibrate DC circuit breaker

L. Liu, S. Liu, M. Popov*

Faculty of Electrical Engineering, Mathematics, and Computer Science (EEMCS), Delft University of Technology, Mekelweg 4, 2628 CD Delft, The Netherlands

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ABSTRACT

The widely acknowledged high-voltage direct current (HVDC) technology has now been accepted as a solution of connecting renewable energy sources. However, this technology is vulnerable when facing DC-side faults; due to the low DC impedance, the fault current can rise to an extremely high value in a short time. In addition, when building a multi-terminal DC (MTDC) system, the fault can make a worse failure or blackout of the system when it is not cleared or isolated in time. The urgent need to ensure reliable mentioned HVDC power system can be realized by making use of DC circuit breaker (DCCB). The vacuum CB, which is one division of active DCCBs, has its own operational limit; it can interrupt fault currents when the di/dt of injected current is lower than a critical value, otherwise the arc may reignite. Therefore, the designing and testing of a DCCB must consider this feature. On the other hand, because of the complex configuration of an MTDC system, one DC-side fault can result in different fault currents at faulty line's terminals; thus, the DCCB needs to be calibrated based on its local fault information. This paper presents an algorithm to optimize the DCCB according to its critical di/dt and local fault current. Furthermore, the operational delay and chopping current of circuit breaker are also considered and modelled. The simulation results from PSCAD platform verify the effectiveness of the presented algorithm.

1. Introduction

The high-voltage DC (HVDC) technology based on voltage-source converter (VSC) is widely acknowledged due to its higher controllability, higher efficiency, and longer transferring distance when connecting offshore wind farms. So far, there have been numerous point-to-point VSC HVDC projects, and the multi-terminal HVDC (MTDC) network is a logical and possible step forward. Examples of this type of HVDC network are Nanao Multi-terminal VSC HVDC and Zhoushan Multi-terminal DC Interconnection in China, and the North Sea Transnational Grid (or even quoted as Super Grid) in Europe. Connecting offshore wind plants and other renewable energy resources with MTDC can further improve the trades and enhance the competition.

Currently, one of the most urgent topics in the HVDC domain is a reliable fault current interruption. Although the DC faults in a point-to-point HVDC link can be adequately isolated by conventional circuit breakers (CBs) on converter's AC side, this is not an option for the MTDC networks. Unlike that in the AC systems, the fault current in a DC system cannot naturally decrease to zero. In other words, it is inevitable to artificially create zero-crossing after DC-side faults occurrence, and this idea gives rise to the main concept of DCCB design. Besides the zero-crossing current, a successful fault interruption also requests a DCCB to be capable of dissipating the magnetic energy stored in DC system's inductors and withstanding the electrical strength of transient interruption voltage (TIV) [1].

There are DCCBs available for low- and medium-voltage applications, but only transfer and load current switches are in use in HVDC systems [2]. The CBs that are used for HVDC fault current interruption are not commonly available, or have limited ranges, e.g. the mechanical DCCB [3] and hybrid DCCB [4,5]. There are numerous concepts of DCCBs presented in articles and patents as well. And all these designs share similar configuration that contains a switching element in the nominal path to build the voltage withstand capability, a commutation path to create the current zero, and an absorber path to dissipate the stored energy [6]. For example, the switching elements are arcs between the contacts in mechanical CBs, and solid-state semiconductors in hybrid CBs; the absorbers are usually metal oxide surge arresters (MOSAs). All these designs and concepts have their own advantages and disadvantages, such as on-state losses and operating speed [5,7]. As the large amount of semiconductors in hybrid DCCBs require considerable investment, this paper only discusses the mechanical DCCBs, and its configuration is shown in Fig. 1. As illustrated in [5], a prototype of DC/DC converter can operate as DCCB, but it is not considered

* Corresponding author.
E-mail addresses: Lian.Liu@tudelft.nl (L. Liu), S.Liu-2@tudelft.nl (S. Liu), M.Popov@tudelft.nl (M. Popov).

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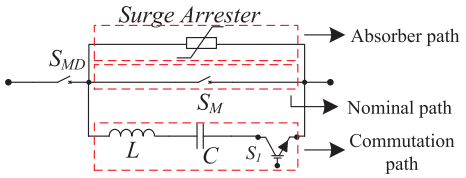

Fig. 1. Typical configuration of mechanical DCCB.

as it is out of the scope of this paper.

Because of the absence of practical HVDC test system, a DCCB is usually investigated in electromagnetic transient (EMT) software environment. The investigation always emphasizes the CB's performance on system level. Therefore, some elements' physical phenomena are neglected. Although the nature of arc in mechanical CBs can be modelled, its dynamic function is difficult to determine and is only valid under specific conditions [8]. The functionality of vacuum switches in mechanical DCCBs is influenced by the slope of injected current (di/dt) at the instant of fault current interruption [9]: the switch can only function well when this di/dt is lower than a critical limit. Because the derivate of sinusoidal injected current is a cosine function, it reaches a minimum at the interruption moment of the considered maximal fault current. Therefore, there would be a minimum fault current corresponding to the maximum di/dt determined by the nature of vacuum switch. Consequently, although the simulation test of a DCCB can be successful, it may fail to clear the arc in practice when the fault current is too low; the simulation results are insufficient to verify DCCB's practical performance. Additionally, when a fault occurs in an MTDC system, the current flowing through one terminal of the faulty transmission line (an overhead line (OHL) or a cable) can be several times larger than that flowing through the other one, because of different fault-current levels linked to this faulty line. Therefore, it is necessary to design and calibrate a DCCB based on its local fault information; a universal design would be inappropriate.

The DCCB is not only used in fault scenario to clear the fault current, but also can be used to disconnect transmission line during normal operation, e.g. serving for the maintenance purpose in an MTDC system. As the nominal current or load current of a transmission line is much lower than a fault current, a fault-interrupting-oriented LC circuit could not guarantee successful operation of vacuum switch because of the possible high di/dt. Hence, it is necessary to dimension the LC circuit from the system maintenance point of view. Due to that the injected current is determined by the LC resonant circuit. This paper presents an algorithm that optimizes the LC resonant circuit to enhance DCCB's practical reliability. The configuration of LC resonant circuit is upgraded accordingly based on the optimization.

The outline of the paper is as follows. The Section 2 introduces the factors that can influence the DCCB's operation, which are also modelled in the simulation. The Section 3 presents the algorithm in detail. The Section 4 describes the studied MTDC system and illustrates the fault currents that are required for the optimized algorithm. The DCCB's performances before and after optimization are compared and discussed in Section 5. Finally, the Section 6 draws the conclusion.

2. Factors influencing DCCB

As mentioned in last chapter, the system-level simulation of DCCB may omit or neglect some critical factors in practice.

2.1. The impact of di/dt

The impact of di/dt is very important in the AC circuit breaker, during the quenching of high-frequency current at its zero-crossings. The limit between interruption and reignition of the high-frequency current has been expressed as a critical di/dt value, beyond which no interruption occurs [10–12]. The same phenomenon can happen during

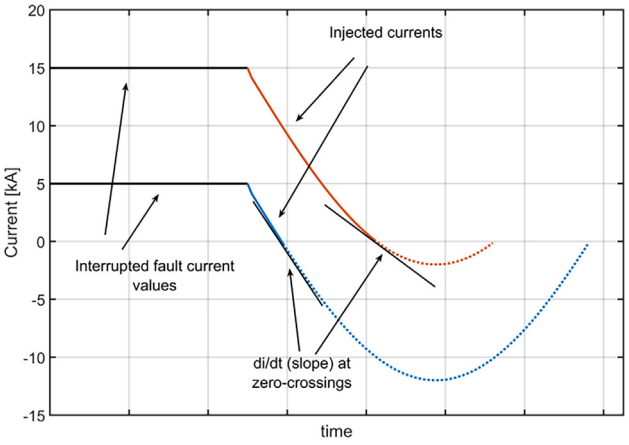

Fig. 2. DCCB interrupting different fault currents.

interruption of DC fault current, although the zero-crossing is created artificially based on LC circuit of DCCB. The Fig. 1 demonstrates one DCCB interrupting two DC fault currents: 5 kA and 15 kA. The di/dt (slope) of injected current at zero-crossing in each case is also marked in Fig. 2, and we can easily observe that the di/dt of 5 kA-scenario is much higher than that of 15 kA-scenario. In practice, the critical di/dt value of a vacuum switch is 150–1000 A/μs [13]. In an MTDC system, the range of fault current can be very large, and it depends on system configuration, e.g. number of terminals, topology of transmission system. Therefore, for the sake of a reliable DCCB, the applied LC circuit must be calibrated to meet the vacuum switch limits of di/dt, for the all possible fault current in DCCB's protection zone.

In addition, considering the purpose of maintenance, one should also disconnect an OHL or a cable during normal operation. However, an LC circuit is dedicated to interrupt fault current of high level, so it could fail to interrupt the nominal current. As the latter could be ten times lower than the former, the di/dt at the instant of interrupting nominal current could exceed the mentioned critical range. To improve this problem, it is quite necessary to design an auxiliary LC circuit for the maintenance.

2.2. The impact of chopping current

The chopping current is an important feature of vacuum switch. The arc in an vacuum can vanish directly when the current is lower than a certain value. In the AC systems, the chopping current can be approximated roughly [9]. This paper applies the value obtained from experience on material CuCr55 [14], which is the most common contact material used in high voltage vacuum interrupter. The chosen values will be demonstrated in Section 5.

2.3. The delay of switch opening

After sending a signal to trip a DCCB, there is always a time delay before the mechanical devices activate. However, because of aging and the physical system of a DCCB, this time delay can be random in a range in practice. As the DC fault current can increase in a very short period, this time delay can influence the actual current interrupted by the DCCB. In this paper, it is assumed that the actual activating time is random between 5 ms and 6 ms based on [3]. In addition, the delay is set to follow normal distribution.

3. DCCB operating principle

The structure of the mechanical HVDC circuit breaker with active current injection is given in Fig. 3 [3]. In the same figure, DCCB's typical performance of interrupting fault current is shown as well. The

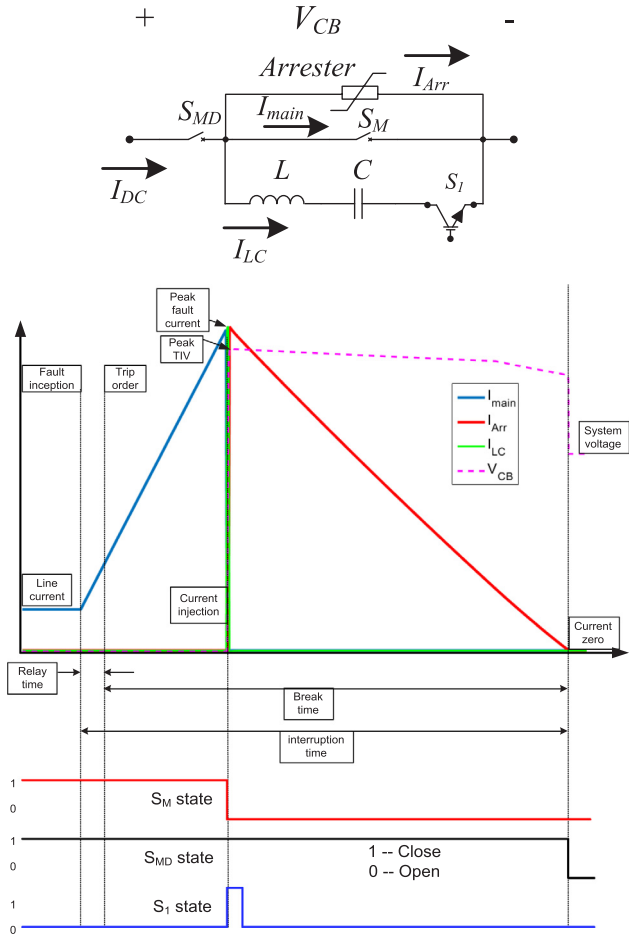

Fig. 3. Structure of DCCB and its typical performance.

breaker consists of a high speed mechanical vacuum interrupter (S_M), a switched parallel resonant branch (L, C, S_1) with a surge arrester and a residual current circuit breaker (S_{MD}).

After receiving a trip signal from protection relay, switch S_M begins to activate. When its contacts have separated to a sufficient distance (to withstand the transient voltage applied during interruption) the resonant circuit injects a counter-current, by turning on switch S_1. This generates a current zero within the interrupter (S_M) and all current now flows through the resonant branch, causing capacitor voltage to rise. When the clamping voltage of the arrester is reached, the current through the circuit breaker begins to rapidly decrease.

The energy stored in the system is then dissipated in the arrester. The time that arrester takes to dissipate energy is dependent on system conditions. When the DC breaker current passes through zero, the residual current circuit breaker S_{MD} becomes an open circuit, providing galvanic isolation of the circuit breaker from the rest of the network.

4. Optimized algorithm

Considering the aforementioned factors, we can obtain the ideal boundary of injected current slope when DCCB successfully interrupts a DC fault current at instant T_i, which is

$$0 \leqslant \frac{di_{LC}(T_i)}{dt} = \frac{U_C}{L}\cos\left(\frac{1}{\sqrt{LC}}T_i\right) \leqslant S_{\max} \tag{1}$$

$$0 < T_i \leqslant \frac{\pi\sqrt{LC}}{2} \tag{2}$$

In which, the $i_{LC}(t)$ represents the function of injected current in time domain, the U_C and $S_{\max}$ represent the voltage of capacitor and the desired di/dt (slope) at the instant of injection respectively, the L and C are the inductance and capacitance of resonant branch respectively.

And, it is worth pointing out that the interruption should always happen within the i_{LC}'s first quarter of a cycle; thus, the function of di_{LC}/dt is monotonically decreasing. Then, the maximum of C is

$$\frac{T_i^2}{L} < C \leqslant \frac{T_i^2}{L\arccos^2(LS_{\max}/U_C)} \tag{3}$$

In practice, (1) may not be equal to 0, in order to guarantee a successful interruption before i_{LC} reaching its maximum I_{LCmax}. If the assumption is that the inductor L, S_{max}, and U_C are pre-defined constants (U_C is always system voltage), the capacitor size is the function of the instant of interruption. However, the inductance and the capacitance can influence the interrupting instant T_i in return, so it is unlikely to find the required capacitor value explicitly; hence, an iteration process is necessary, and we propose the following steps:

First, according to (1), we can assume a minimum inductance $L_{\min}$ of LC circuit:

$$L = \frac{U_C}{S_{\max}} = L_{\min} \tag{4}$$

This equation is derived from the (1) based on the critical condition:

$$\cos\left(\frac{1}{\sqrt{LC}}T_i\right) \leqslant \frac{LS_{\max}}{U_C} \leqslant 1 \tag{5}$$

Then, based on maximum current $I_{\max}$ of a transmission line terminal, and a certain safety margin K, the range of capacitance C of LC circuit can be obtained:

$$C = \frac{(KI_{\max})^2 L}{U_C^2} \tag{6}$$

In (6), the L is a fixed value, so the C is proportional to $KI_{\max}$. The coefficient K determines the peak current that LC circuit can achieve. It could be set as 2 for 100% margin [15], then the circuit breaker has a higher rate to cope with unexpected situation, e.g. the unexpected extra time delay of main switch.

Then, with a given fault current I_{fault}, the instant of interruption T_i and slope S at this instant can be obtained respectively from (7) and (8):

$$T_i = \sqrt{LC}\arcsin\left(\frac{I_{fault}\sqrt{L/C}}{U_C}\right) \tag{7}$$

$$S = \frac{U_C}{L}\cos\left(\frac{1}{\sqrt{LC}}T_i\right) \tag{8}$$

When S from (8) is lower than $S_{\max}$ or the required limit, then according to (4) and (6), the range of natural frequency of LC circuit is obtainable

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{9}$$

When the frequency is within a preferred range, the calculated inductance and capacitance can meet the requirement.

Fig. 4 shows five sets of results obtained from the new algorithm. In addition, it is assumed to interrupt a 10 kA fault current in a ± 200 kV system, the $KI_{\max}$ of LC circuit is selected as 2 × 12 kA; the margin coefficient K is set to 2. Derived from (6), the largest chosen C is $(24^2 L_{min}/200^2)\mu F$. At the same time, the smallest C is $(10^2 L_{min}/200^2)\mu F$ that ensures the arcsine function in (7) is within domain (0,1], otherwise (7) has complex solutions. The figure clearly shows the di/dt at the instant of interruption for different values of L and C. It is noticeable that defining $L_{\min}$ from (4) can set a hard limit on the di/dt at the interruption instant. It is noted here that with the selected minimal inductances in Fig. 4, the mathematical upper limits of $S_{\max}$ are: 1000 A/μs, 571 A/μs, 154 A/μs, 100 A/μs, and 10 A/μs, when the $KI_{\max}$ is higher than 64 kA. Another boundary of this algorithm is the natural frequency

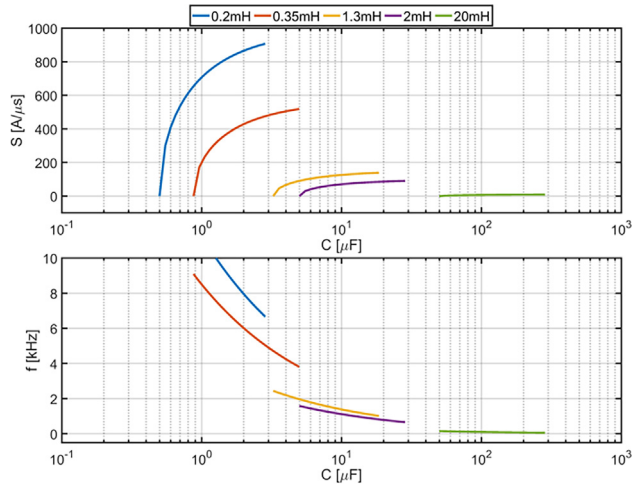

Fig. 4. Results of optimized algorithm with regard to capacitances under different L_{min}.

of corresponding LC circuit, which is also chosen within a range of 3 kHz–6.5 kHz.

5. Fault current ranges

The estimations of maximum and minimum current are two crucial inputs of the optimization algorithms, as they determine the LC circuit of a DCCB. In this paper, this range of fault current is obtained by DC-side fault simulations for a cable in a 4-terminal DC grid. In order to evaluate the critical pressure of DCCB, its adopts the topology similar to the one in [16]. The load flow is determined based on the test system DCS2 in [17].

5.1. Description of the studied system

The configuration of the studied MTDC system is shown in Fig. 5, which is a 4-terminal symmetric monopole HVDC system (± 200 kV). The converter Cm-F1 connects the offshore wind power plant, and Cm-E1 connects the offshore oil and gas platform. The rest of the onshore systems are modelled as infinite buses. The data of this system are provided in Table 1, and it is modelled in PSCAD environment. More details can be found in [17].

The fault is applied on the 200 km XPLE cable between DC bus Bm-B2 and Bm-B3. A 100 mH inductor is installed at each terminal of this cable, and two CBs are linked in this cable, i.e. DCCB1, DCCB2. In this work, the location of the DCCB is just chosen in order to show the performance of a model and may not related to a possible actual situation. The parameters of the studied cable are shown in Fig. 6, which is derived from [18]. Choosing this cable is because there is only contribution from converter Cm-B2 at the terminal of Bm-B2, while there is multiple contribution (three feeders) from terminal of Bm-B3. Multiple contribution is a representative feature of an MTDC grid; when a fault

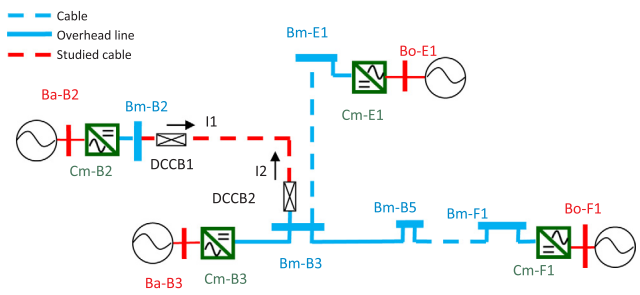

Fig. 5. Configuration of studied system.

occurs on the studied cable, the three healthy feeders at Bm-B3 may increase the fault current experienced by DCCB2.

5.2. Simulation of faults at different locations

A series of fault scenarios are simulated on studied cable: the fault is a permanent metallic pole-to-pole fault that is applied at different locations at 0.01 s. More details are listed in Table 2.

The I1 and I2 are the fault currents flowing through DCCB1 and DCCB2 respectively. The simulation results are demonstrated in Fig. 7.

It is noticeable that the fault location influences the amplitudes of fault currents I1 and I2: the closer the fault is to a DC bus, the higher the measured current would be at that bus. On the other hand, the three healthy feeders on Bm-B3 have obvious contribution to the I2: the highest fault current of I2 is almost twice higher than I1. Therefore, the rating of prospective DCCB2 should be higher than that of prospective DCCB1.

Assuming the fault can be detected instantly when it arrives the measuring unit at cable terminal, one can find the possible currents values that need to be interrupted by the DCCB. The random mechanical time delay and the time delay caused by travelling wave can be obtained from manufactures. In this paper, the fault detection applies the algorithm described in [19,20]. The time delay caused by traveling wave in the studied cable is around 1.015 ms (the velocity of the traveling wave is around 197 km/ms), which is computed by the Line Constants Program (LCP) in PSCAD. The estimated interruption time intervals are tabulated in Table 3 in the most and least severe fault cases; for the DCCB1, they are Fault A and Fault F, while for the DCCB2, they are Fault F and Fault A. The table also shows the range of fault currents corresponding to the time intervals.

6. Performance of DCCBs

6.1. Designing LC circuit without di/dt consideration

According to Table 3, the LC circuit of DCCB1 and DCCB2 can be seen in Table 4. The configuration of circuit breaker is shown in Fig. 3, which uses an IGBT (S_1) to control the current injection. It is assumed that the vacuum switch S_M cannot open when di/dt is higher than a critical value, which is 650 A/μs. The arrester's data are obtained from [21]: the rated voltage is 243 kV, and the maximum continuous operating voltage (MCOV) is 175 kV. The chopping currents of S_M and S_{MD} are defined as 32 A [14] and 10A [3] respectively. The control loop and logic of the DCCB are designed based on [13,22].

The performance of DCCB2 under Fault E is shown in Fig. 8. We can see that the injected current cannot interrupt the fault due to the high di/dt. In practice, it is highly possible that the arc in vacuum switch cannot vanish and it could reignite. As a result, the main current through the vacuum interrupter cannot commute into the energy absorption branch. In order to avoid this kind of failure, the designing of LC circuit must take its di/dt into account.

6.2. Optimizing LC circuit with di/dt consideration

Similarly, according to Table 3 and a pre-assumed maximal di/dt = 571 A/μs, the DCCB1 and DCCB2 are calibrated optimally. The results are shown in Table 5, in which the 'main' LC circuit is referred to distinguish the 'auxiliary' LC circuit discussed in the next paragraph. On the other hand, the maximum injected current I_{max} of LC circuit is higher than estimated maximum fault current, which is around 54% margin both for DCCB1 and DCCB2. Although in [15], it is recommended to make 100% margin, the margins for optimized DCCBs are enough.

As mentioned in Section 1, the DCCB can also be used to disconnect an OHL or a cable for the maintenance during nominal operation. Therefore, the auxiliary LC circuits for this aim are calibrated in

Table 1
Data of Study System.

AC system		DC system	
Bus name	RMS Voltage	Converter name	Control mode and setting points
Ba-B2	380kV	Cm-B2	P/V_{dc}; P_{ref}=400MW, V_{dc_ref}=±200kV, droop=0.2
			Q; Q_{ref}=0 MVAR
Ba-B3		Cm-B3	P/V_{dc}; P_{ref}=−800MW, V_{dc_ref}=±200kV, droop=0.2
			Q; Q_{ref}=0 MVAR
Bo-E1	145kV	Cm-E1	Island mode; V_{ac_ref}=145kV, frequency=50Hz
Bo-F1		Cm-F1	P; P_{ref}=500MW
			Q; Q_{ref}=0 MVAR

Table 6. As the nominal power (± 200 kV × 0.95 kA) flows from Bm-B2 to Bm-B3, the auxiliary LC circuits of DCCB1 and DCCB2 are chosen to inject current aligning with I1, which means the DCCB2 has to interrupt currents in opposite directions respectively under faulty and normal conditions. In fact, the DCCB with bi-directional in interruption capability is necessary for MTDC network [23], but it is not discussed in detail here because it is out of the scope in this paper.

6.3. Performance of optimized DCCBs

The optimized configuration of the DCCB is shown in Fig. 9. The main and auxiliary LC circuits are combined to share one inductor: when the switch S_C is closed, the conductance will be $C_1 + C_2$ which are used to interrupt fault current; when S_C is opened, the inductance will be only C_2 (As $C_2 = 2\,\mu F$, the C_1 of DCCB1 and DCCB2 is respectively 3 μF and 7 μF) which is used to interrupt nominal current. The switch S_C is controlled by another independent signal, e.g. a maintenance signal. Similar functionality is already realized in hybrid DCCB [24].

Particularly in this paper, the switches S_{A1} and S_{A2} are applied in DCCB2 to reverse the injection of current I_{LC}, because fault current and nominal current are in opposite directions. Normally, the S_{A1} and S_{A2} are opened and closed respectively, so the DCCB is always ready for interrupting a fault current. When there is a command to trip a healthy transmission line, a signal can be sent to S_{A1} for closing and S_{A2} for opening. Waiting for the signal to initialize S_1, the DCCB is now ready for interrupting the nominal current. In fact, the signal controlling S_{A1} and S_{A2} can cooperate with that controlling S_C. The chopping currents and the surge arrester apply the same values as described in Section 6.1.

Table 2
Simulated Fault Cases.

Fault scenario	Description
Fault A	Pole-to-pole fault, 0 km aways from Bm-B2.
Fault B	Pole-to-pole fault, 20 km aways from Bm-B2.
Fault C	Pole-to-pole fault, 80 km aways from Bm-B2.
Fault D	Pole-to-pole fault, 120 km aways from Bm-B2.
Fault E	Pole-to-pole fault, 180 km aways from Bm-B2.
Fault F	Pole-to-pole fault, 200 km aways from Bm-B2.

6.3.1. Interrupting fault currents

Figs. 10 and 11 demonstrate the successful fault interruption

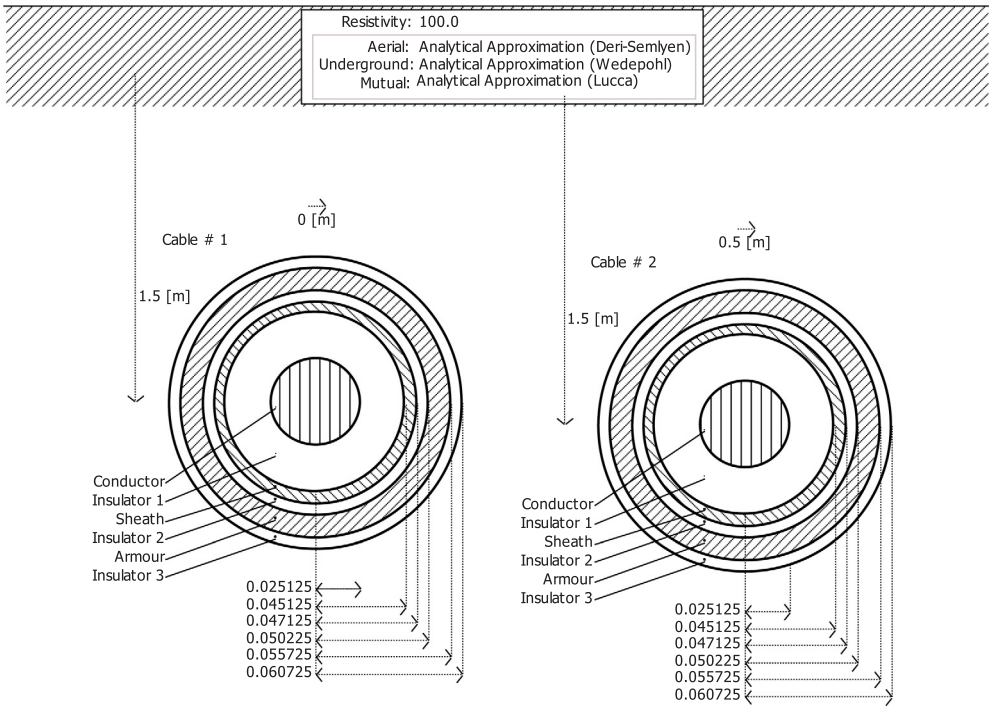

Fig. 6. Dimension of studied cable.

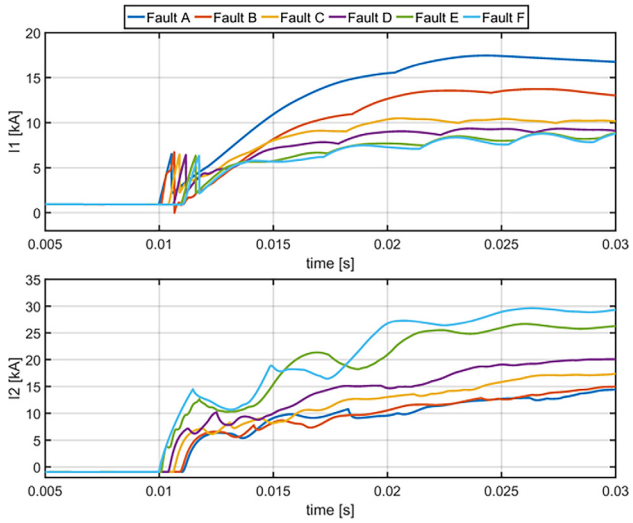

Fig. 7. Simulation results of fault currents at two terminals of the studied cable.

Table 3
Estimation of Fault Current Ranges.

Interrupting time interval		Interrupting current interval
DCCB1	[0.015 s 0.017015 s]	[5.8695 kA 12.516 kA]
DCCB2	[0.015 s 0.017015 s]	[7.873 kA 21.36 kA]

Table 4
DCCBs Configuration.

Parameter	DCCB1	DCCB2
Capacitor	7μF	
Inductor	0.2mH	
Frequency	3.97kHz	
U_C	200kV	
I_{max}	37.42kA	

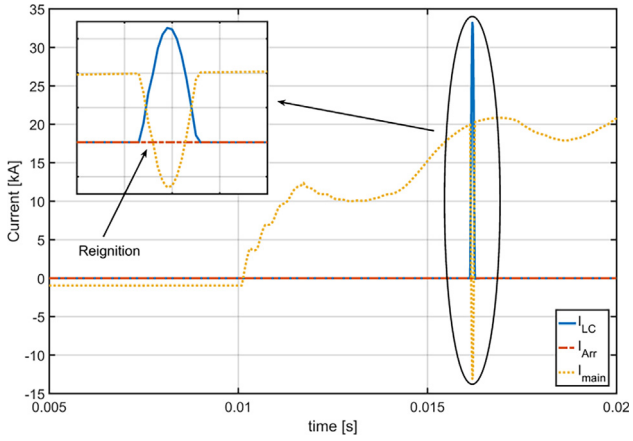

Fig. 8. Performance of DCCB2 before optimizing.

considering two circuit breakers, respectively. To be consistent with Section 5.2, the fault location is with respect to Bm-B2. In these two figures, only Fault A and Fault F are simulated here. Fault A is the most and least severe fault scenarios for DCCB1 and DCCB2 respectively, while vice versa holds for Fault F. It is noticeable that the considered faults can be cleared within 10 ms.

Table 5
DCCBs after Optimization: The Main LC Circuits.

Parameter	DCCB1	DCCB2
Capacitor	5 μF	9 μF
Inductor	0.35 mH	0.35 mH
Frequency	3.8 kHz	2.8 kHz
U_C	200 kV	200 kV
I_{max}	23.9 kA	32.1 kA
di/dt_{max}	571 A/μs	571 A/μs

Table 6
DCCBs after Optimization: The Auxiliary LC Circuits.

Parameter	DCCB1	DCCB2
Capacitor	2μF	
Inductor	0.35mH	
Frequency	6.0kHz	
U_C	200kV	
I_{max}	15kA	
di/dt_{max}	571A/μs	

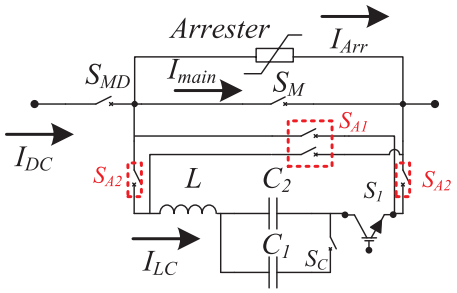

Fig. 9. Configuration of optimized DCCB.

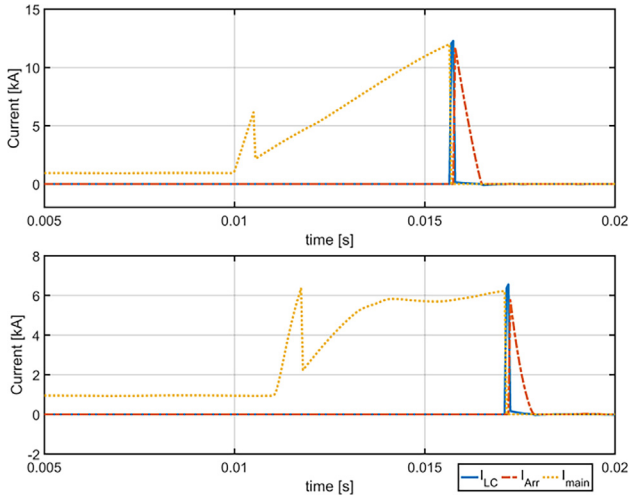

Fig. 10. Performance of DCCB1 after optimizing. Top: Fault A; bottom: Fault F.

6.3.2. *Interrupting nominal currents*

Fig. 12 depicts the successful nominal current (0.95 kA) interruption by DCCB1 and DCCB2: they received the signal at 0.01 s and interrupted the currents at around 0.0158 s. It is clear that the nominal current flows though DCCB2 in a negative direction, so the injected current has been reversed accordingly. The current can be neutralized in 3 ms, due to its low value and high natural frequency of LC circuit. In practice, disconnecting a transmission line is possible by: first opening either one DCCB linked on the line, then opening the other one after

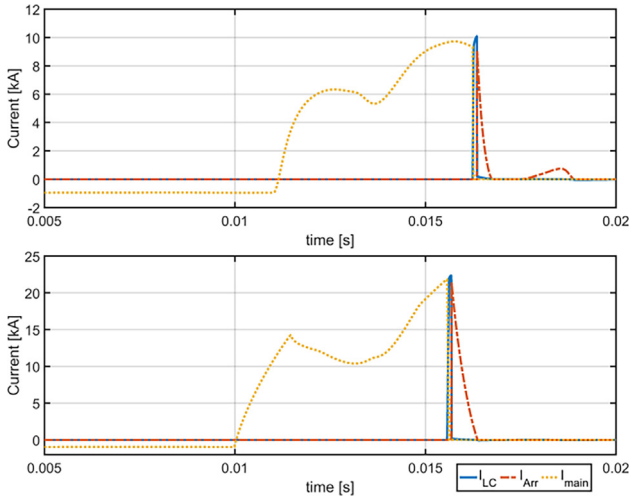

Fig. 11. Performance of DCCB2 after optimizing. Top: Fault A; bottom: Fault F.

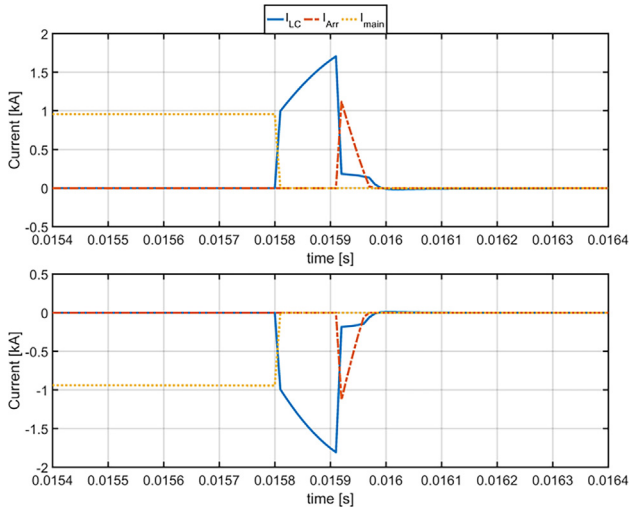

Fig. 12. Performance of circuit breaker interrupting nominal currents. Top: DCCB1; bottom: DCCB2.

current decreasing to zero. The simulation here demonstrates the DCCBs' functionality of interrupting nominal current (load current) after optimized calibration.

6.4. Discussion

Besides the scenarios in Table 2, other fault situations with different fault distances are simulated as well. The di/dt of two studied DCCBs at the current zero instant under each situation is recorded, which is shown in Fig. 13. It is noted here that the fault distance is calculated from Bm-B2 to fault location. According to the results, we can observe that they are well below the set critical di/dt = 650 A/μs, which can guarantee the successful vacuum switch operation, thus successful fault interruption. The simulation shows the effectiveness of the optimized DCCBs: after the optimization, the di/dt at the current zero instant can be in an acceptable level.

In addition, the slopes (di/dt) when interrupting nominal currents are also calculated and recorded in Fig. 14. It is obvious that the di/dt is close to the maximal value (571 A/μs). In practice, when designing and testing an LC circuit, it is better to consider a safe margin based on the critical di/dt of a vacuum switch, and choose a suitable inductor based on (4). Otherwise the vacuum switch would always work at its maximal limit when interrupting fault current.

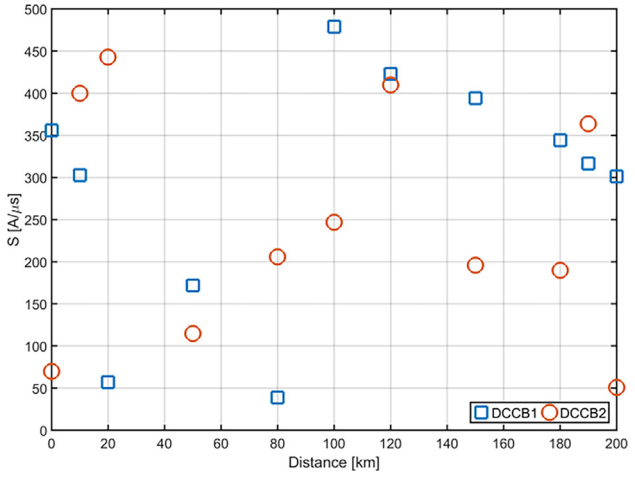

Fig. 13. Slope (di/dt) at interrupting instant under different located faults.

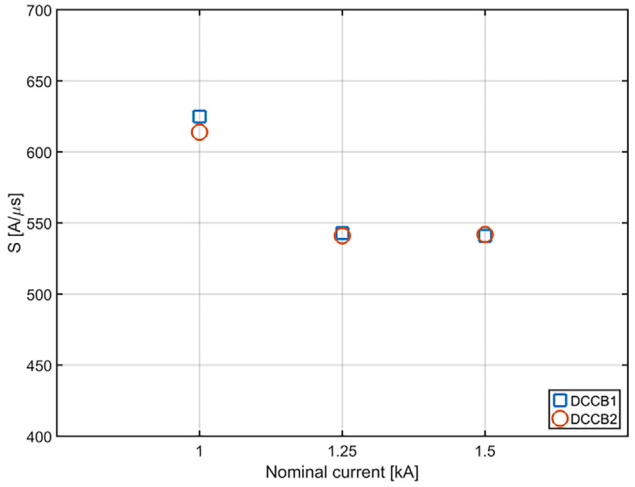

Fig. 14. Slope (di/dt) at interrupting instant under different nominal currents.

6.5. Limitation

In a real circuit breaker, the maximum quenching capability of di/dt of vacuum interrupter depends on the characteristic of vacuum bottle. The maximum value range is 150–1000 A/μs according to [13], this value is influenced by many factors, such as interruption current, gap distance, etc. In this stage, the maximum quenching capability of di/dt of vacuum interrupter under different fault current magnitude is neglected. In this paper, the fixed 650 A/μs is considered. In practice, the higher the interruption current is, the denser the residual plasma will be after current zero. As a result, the lower di/dt the vacuum contact can withstand [25]. In addition, the contacts separating dynamic and gap distance also influence the maximum quenching capability of di/dt. The reason is that the vacuum bottle can survive a higher di/dt when the gap distance between contacts is larger [25]. If the gap distance dynamic during operating contacts could be provided, the research could be more realistic.

7. Conclusion

This paper discusses a significant physical feature that can influence the functionality of a vacuum switch: the di/dt of injected current from *LC* circuit at interrupting instant. As the vacuum switch can extinguish an arc only when the di/dt is lower than a critical value, the di/dt must be considered when designing and calibrating a DCCB. The paper presents an algorithm to optimize a DCCB with the given critical di/dt.

The detailed algorithm is presented in the paper. Due to the internal correlation between inductance, capacitance, and interrupting instant, the optimal parameters should be obtained iteratively. Besides the algorithm, the configuration of DCCB is also upgraded accordingly, which can interrupt in both fault and nominal scenarios. The simulation performed in PSCAD environment shows that the algorithm can guarantee that the di/dt is within a safe limit during interruption. On the other hand, the results of di/dt when interrupting nominal currents reveal that choosing a safe margin of di/dt for designing *LC* circuit is advisable.

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