Delft University of Technology
Faculty of Electrical Engineering, Mathematics and Computer Science

Masters's thesis

Evaluation of advantageous modulation methods for a dual active bridge converter with a wide output voltage range

July 21, 2022

Author:
C.A Straathof

Student number:
4557352

Jury:
Prof.dr.ir. P. Bauer (Chair)
Dr.ir. Z. Qin (Supervisor)
Dr.ir. R. Santbergen

Daily supervisor:
Dingsihao Lyu

Abstract

In this thesis two new modulation methods are proposed for a wide output voltage range dual active bridge (DAB) converter for bidirectional EV charging application. The objective of the proposed modulation method is to maximize the number of ZVS events over the operating range, while maintaining low current stress. The first modulation method achieves this with fixed a switching frequency, while the second achieves full ZVS operation using a variable switching frequency combined with alternative charging profiles. The design of the modulation method is done through an analysis of the operating modes and the ZVS behaviour of the DAB converter. To verify the improvements to the ZVS behaviour of the proposed modulation method, the modulation method is implemented in a simulation and on an 11 kW prototype with an input voltage range of 640 to 840 V, and an output voltage range from 250 to 1000 V, to ensure compatibility with various types of EV's. A control system and a transient mitigation method are designed to facilitate the experimental verification. The proposed modulation method is compared to a peak current optimization for the DAB converter found in the literature. Measurements done on the 11 kW prototype confirm that the improvements in ZVS are achieved. These improvements in ZVS of the proposed modulation method also result in increased efficiency compared to the peak current optimization, especially in the low-power operating regions. The full power efficiency over the entire voltage range of the peak current optimization, the proposed fixed frequency, and the proposed variable frequency modulation are 97.895%, 97.879% and 97.964% respectively.

Acknowledgments

First of all, i would like to thank Yang for helping me find an interesting thesis topic after after my previously selected topic suddenly became unavailable. This brought me into contact with Dingsihao, who proposed this interesting topic. I enjoyed working with him and appreciate his supervision, especially during the testing period. His feedback in the writing process is also greatly appreciated. I would also like to thank my official supervisor Dr.ir. Zian Qin for making this thesis possible. I am also grateful to Thiago for having designed the PCB used for testing, and to Joris and Mladen for their assistance in creating a functional prototype.

Coen Straathof
July 2022

Contents

List of Abbreviations

Abbreviation	Explanation
DAB	Dual Active Bridge
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
CV	Constant Voltage
CC	Constant Current
MSCC	Multistep Constant Current
ESS	Energy Storage Systems
EV	Electric Vehicle
SPS	Single Phase Shift
EPS	Extended Phase Shift
DPS	Dual Phase Shift
TPS	Triple Phase Shift

Table 1

Chapter 1

Introduction

To reduce the effects of climate change, the need to reduce greenhouse gas emissions arises. In applications like transportation and heating of homes, which have a significant contribution to global greenhouse gas emissions, efforts are being made to replace fossil fuels with electricity as an energy source. In the field of transportation this is mainly done through electric vehicles (EV) and public transportation, while for heating, solutions like heat pumps, or usage of industrial waste heat are common.

Due to the intermittent nature of renewable energy sources, Energy storage systems (ESS) are required to stabilize the electricity grid. Battery energy storage, which has a rapid response time and good efficiency is a promising solution for dealing with the short term energy imbalance. To reduce the total amount of resources required for the ESS, EV batteries can be used to support the grid. This would introduce a large amount of additional energy storage that will be available for the majority of the day, as most EV's will only be used for a few hours each day.

To achieve this, both the EV charger and the EV itself need to be capable of bidirectional power transfer. For people to interact with the charger system safely, galvanic isolation is a necessary feature for the system. This is typically achieved through a transformer, working at 50 Hz, or at a higher frequency as part of a power converter. The higher frequency operation of the transformer in such converters allows for much smaller transformers at the same power rating, and is thus preferred over a 50 Hz transformer. Among different brands of EV's, battery voltage ranging from 320 to 800 V can be found [18]. To ensure that the charger is compatible with all vehicle types it should have a wide output voltage range.

To achieve bidirectional isolated DC/DC conversion, multiple converter topologies can be used. The dual active bridge (DAB) and CLLLC resonant DAB topologies are suitable for EV charging application, as they have high power density, efficiency [7, 24]. Given that correct control strategies are used, both converter types are capable of zero voltage and/or zero current switching, providing a significant reduction in switching losses compared to hard switched converters. When considering the DAB and resonant converter for EV charging application, in a design with a single DC-DC converter, the phase shift based DAB performs better as it can handle a wider voltage range and has a faster dynamic response than the CLLLC resonant converter [24]. Alternatively a design with two DC-DC stages could be used with either the DAB or resonant converter, where a buck or boost stage is added to extend the voltage range. However, as this increases the part count and design complexity, a single stage DAB is chosen for this application.

When charging a battery, the charging process can affect the useful life of the battery. The most basic charging method charges the battery using a constant current, until the battery voltage reaches an upper limit, after which the battery will be charged at a constant voltage (CC-CV) [14]. Alternatively the charging current can be reduced in steps (MSCC) [14], which

has the potential to achieve higher efficiency, as individual DC/DC converters can be shut down allowing the others to operate closer to their optimal operating region. Alternative methods like pulsed charging [14, 1] can also be used, providing a similar advantage as MSCC, where the converter can operate in its optimal operating region. Pulsed charging also offers benefits to battery life [1], however this method can also have a negative impact on the electricity grid [14].

1.1 Objectives & requirements

The goal of this thesis is to design a control system for a wide output voltage range DAB converter for EV charging application. The focus will be on the modulation, however other parts of the control system should also be considered. The control system should improve the ZVS behaviour and efficiency of the converter, which is mainly affected by the modulation method. It should also take into account the transient behaviour of the converter, as large DC offsets or saturation are not desirable. The requirements for the for the DAB converter are shown below:

- An input voltage range from 640 V to 840 V
- An output voltage range from 250 V to 1000 V
- A maximum output power of 11 kW
- A maximum DC current of 30 A
- Bidirectional power transfer

To verify whether the control system actually provides an improvement, it should be compared to a control system using an already existing modulation method to observe whether the ZVS behaviour and efficiency have improved. In addition to this, tests should be performed to observe the transient performance of the converter.

1.2 Thesis Structure

To start the design of the control system, first a literature study regarding the DAB converter and its modulation methods will be performed. This is discussed in chapter 2, together with the analysis of the ZVS requirements and transient behaviour. This chapter will also introduce the new modulation and transient mitigation methods proposed in this thesis, which improves the DAB converters ZVS behaviour over the operating range, while retaining low current stress.

Based on the theoretical analysis done for the control system, a simulation will constructed to verify the functionality of the control system. Problems arising from the simulation will be addressed when necessary. Chapter 3 will discuss the simulation and it's results.

In chapter 4, the practical implementation of the converter and its control system will be discussed. This includes the implementation of key parts of the control system on a TMS320F28379D microcontroller, the selection of the switches, and the design of the transformer and inductor. Specific details about the implementation of the control system on the microcontroller can be found in the appendix. Based on the designed hardware, and the control system, an estimate of the converters efficiency over the operating range is made.

Finally, the constructed converter will be used to test the proposed modulation methods and transient mitigation method. The results of these test are discussed in chapter 5.

Chapter 2

Analysis of DAB modulation methods

2.1 DAB converter operation

The DAB converter consists of two H-bridges, with a transformer that has a relatively large leakage inductance, as shown in figure 2.1. In this circuit the magnetizing inductance is neglected, as it is typically significantly larger than the leakage inductance thus limiting its influence on converter behaviour. Each half-bridge in the circuit operates at a 50% duty cycle. Below the parameters that can be manipulated to control the converter are listed.

- $-1 < \Phi < 1$, the normalised phase shift between the two H-bridges.
- $0 < D_1 < 1$, the effective duty cycle of the left H-bridge.
- $0 < D_2 < 1$, the effective duty cycle of the right H-bridge.
- T_s, the sample time, which equals $\frac{1}{f_s}$

Figure 2.2 shows the voltage waveform of a single switching period at 25 kHz to clarify the parameters listed above. The effective duty cycle D_1 and D_2, which can be observed in the output voltage waveforms of the primary and secondary H-bridge ($V1$ and $V2$), are implemented through the phase shift between the half bridges (V_{Qxx}) in the H-bridge. Φ, the phase shift between the primary and secondary H-bridge, and is defined from the centre of the voltage waveforms.

Φ is the main control parameter of the DAB converter, determining the direction of power flow and affecting its magnitude. By manipulating D_1 and D_2, the magnitude of the power flow can be altered, and the ZVS range can be extended. This is done in various modulation methods like extended (EPS), dual (DPS) and triple phase shift (TPS) modulation [15]. Finally there is the switching frequency, which has an inversely proportional relationship with the transferred power. It can potentially be used to optimize the performance at different voltage levels, or different loads.

2.2 modulation methods

In literature various modulation methods can be found. The most simple modulation method is single phase shift modulation, where only Φ is manipulated. At unity voltage gain, it provides ZVS over the most of the operating range. However at non-unity voltage ratio the ZVS

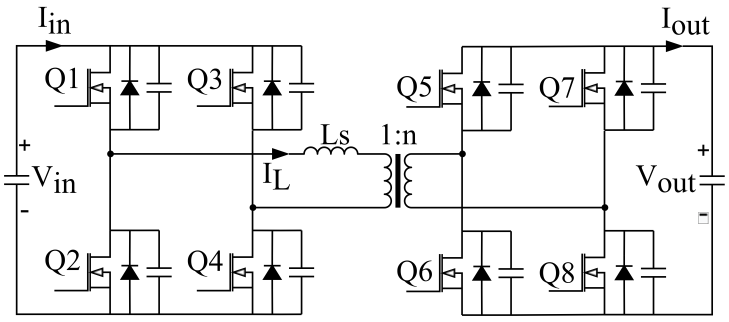


Figure 2.1: Circuit of the DAB converter

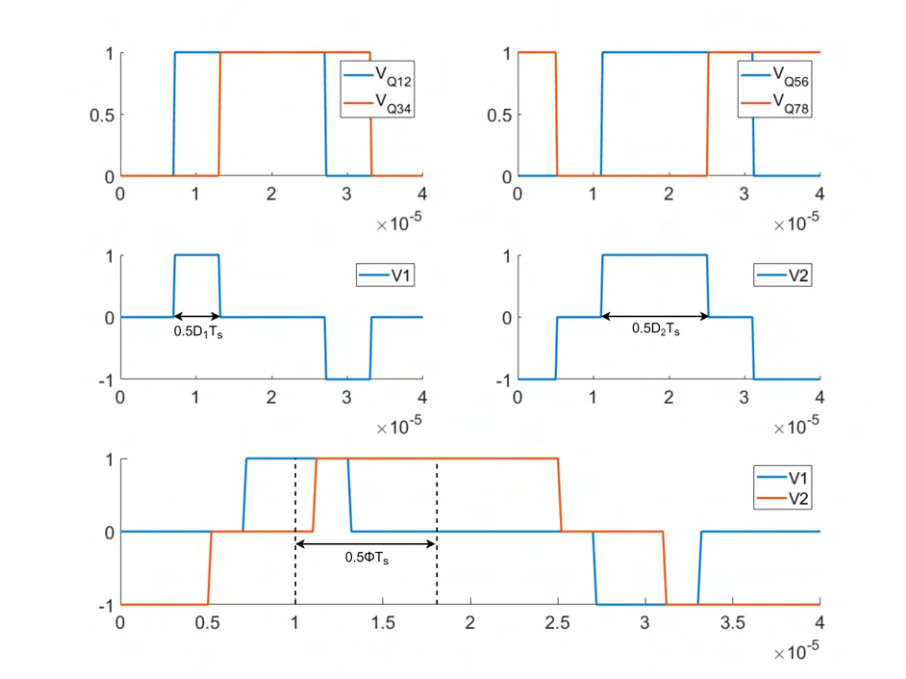


Figure 2.2: Voltage waveforms for $\Phi = 0.4$, $D_1 = 0.3$ and $D_2 = 0.7$

range is limited at lower loads, and current stress is high compared to more advanced modulation methods [15]. This makes it unsuitable for wide voltage range applications like EV charging.

2.2.1 EPS and DPS modulation

To improve the modulation, a second control parameter can be used, which is done in EPS modulation and DPS modulation. Here both Φ, D_1 and D_2 can be manipulated with some restrictions. In the case of EPS modulation, only D_1 or D_2 can be manipulated while the other is set equal to 1, depending on the voltage ratio. For DPS modulation D_1 is set equal to D_2. This limits the number of control variables to 2.

For both modulation types, the power range where ZVS applies is extended due to the additional control parameters, however they do not provide full range ZVS when considering the switch junction capacitors. Between EPS and DPS modulation, EPS modulation generally performs better as it has reduced current stress compared to DPS modulation [16]. The exception to this is at very low power, where the small duty cycle in both H-bridges occurring in DPS modulation reduces the reactive power in the inductor compared to EPS modulation where one H-bridge will operate a duty cycle of 1.

To resolve the issue regarding the limited ZVS range, in [22] and [20] for EPS modulation, and [13] for DPS modulation, the ZVS range is expanded to the full operating range by making use of the magnetizing current of the transformer. This is implemented by designing the transformer to have a smaller magnetizing inductance. When comparing the two modulation methods, EPS again has an advantage as it requires a much smaller magnetizing current compared to DPS modulation to obtain full ZVS range. The main cause of this difference is that the ZVS range of EPS modulation without magnetizing inductance only has a small non-ZVS gap in the power range when transitioning between operating modes [22], while DPS modulation loses ZVS in the entire low power operating range [13]. Modulation techniques that rely on magnetizing inductance are considered to be less desirable compared to other methods, as the additional magnetizing current results in more conduction losses.

Instead of using the magnetizing inductance, which results in additional conduction losses, it is also possible to manipulate the switching frequency to bridge the gap in power between the two ZVS regions [6]. Although the control complexity is higher compared to the magnetizing current method, it has the potential of achieving higher efficiency. The lowered switching frequency needed the low power switching region also has the advantage of decreasing the switching losses in this region.

In [25] a variation of EPS is discussed, where asymmetric pwm is used to reduce rms current and expand the ZVS range. Although such a method has the potential to extend the ZVS range, the DC offset is problematic, and requires a series capacitor to prevent saturation of the transformer. This is a disadvantage as a series capacitor results in additional conduction losses, and larger converter size.

2.2.2 TPS modulation

By allowing the duty cycle of both H-bridges to be controlled separately, it is possible to control the DAB converter in a more optimal way than when using EPS or DPS modulation, as EPS and DPS modulation in essence variants of TPS with certain restrictions applied to it for the purpose of reducing complexity. In [5] twelve operating regions are derived for TPS modulation. Removing mirrored operating modes, and the obsolete operating modes with $\Phi = \pm 1$, five operating modes remain [10, 19, 11]. Table 2.1 shows the boundaries of these operating modes. The waveforms corresponding to the operating modes are shown in figure 2.3, 2.4 and 2.5.

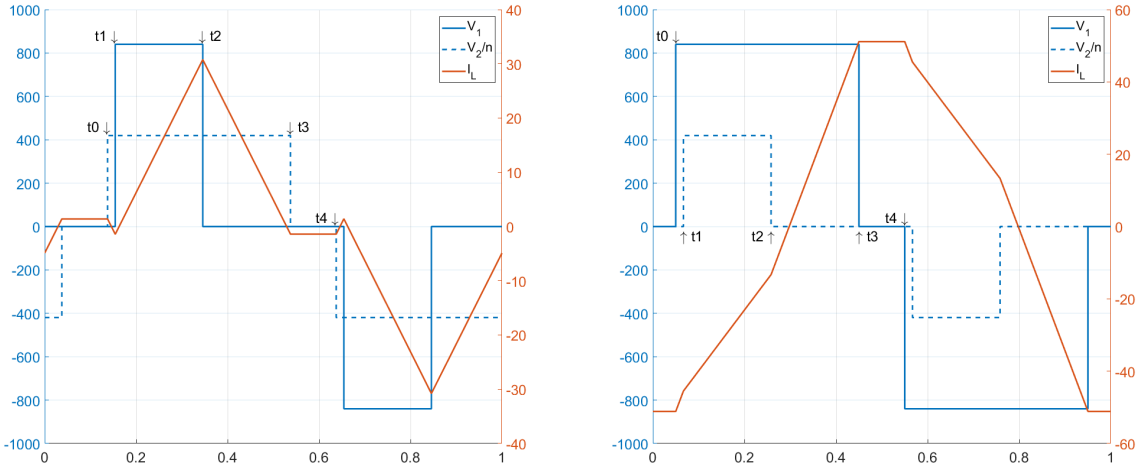
Mode	Condition 1	Condition 2	ZVS turn-on (max)
1	$\frac{\lvert D_2-D_1\rvert}{4} > \frac{\Phi}{2}$	$sign(D_2 - D_1) = sign(V_1 - V_2)$	8/8
2	$\frac{\lvert D_2-D_1\rvert}{4} > \frac{\Phi}{2}$	$sign(D_2 - D_1) = sign(V_2 - V_1)$	6/8
3	$\frac{\lvert D_2-D_1\rvert}{4} < \frac{\Phi}{2}$	$\frac{\Phi}{2} < \frac{D_2+D_1}{4} < \frac{1}{2} - \frac{\Phi}{2}$	6/8
4	$\frac{D_1+D_2}{4} > \frac{\Phi}{2}$	$\frac{D_1+D_2}{4} > \frac{1}{2} - \frac{\Phi}{2}$	8/8
5	$\frac{D_1+D_2}{4} < \frac{\Phi}{2}$	$\frac{D_1+D_2}{4} < \frac{1}{2} - \frac{\Phi}{2}$	6/8

Table 2.1: Limits of each operating mode

TPS optimization

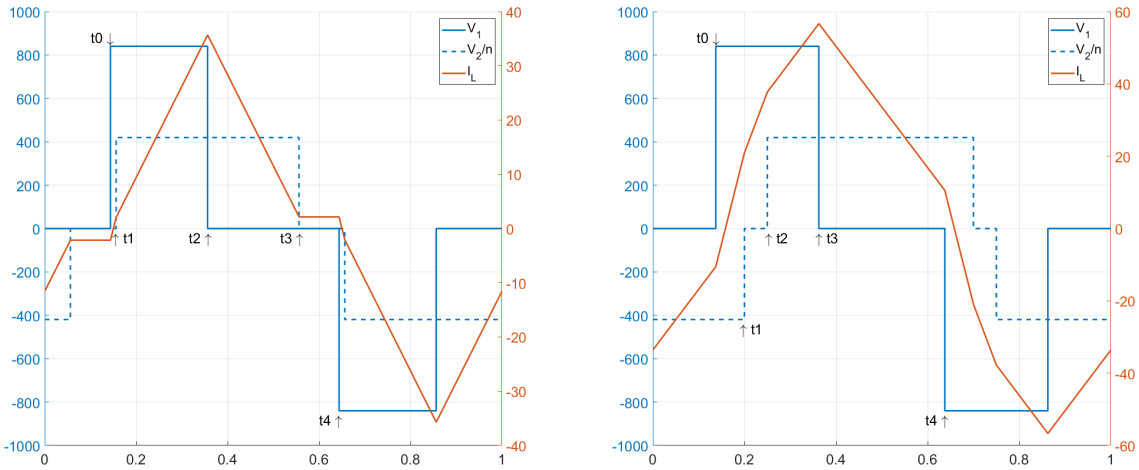
As the most flexible among the modulation methods, TPS modulation can be optimized for minimum peak or rms current or minimum reactive power. In [5] and [10] a minimum peak current optimization is done, this results in 2 operating regions, which naturally transition into each other.

At low power, the peak current has the lowest value when operating at the boundary between mode 1 and 3 of TPS, where the duty cycles are proportional to the voltage ratio. As the current



(a) (b)

Figure 2.3: TPS mode 1 & 2



(a) (b)

Figure 2.4: TPS mode 3 & 4

waveform resembles a triangular shape, it is also called ideal triangular modulation. At higher power, the peak current is minimized when operating with a duty cycle of 1 on the H-bridge with lower voltage, which is equivalent to EPS modulation. A similar modulation method is derived in [19], by first removing the non-ideal operating modes, and finding the minimum rms current through analytical means.

As discussed in [10] and [19], it is possible to achieve full soft-switching using these methods. While operating at higher power in the EPS region, full ZVS can be achieved. When the power is decreased, the converter will start to operate using ideal triangular modulation. As 6 out of 8 switching events will switch with zero current, ZVS will be lost for these switching events, in return ZCS is obtained, compensating the lack of ZVS to a certain degree.

A further improvement has been made to the soft switching in [11], where a slow control loop optimizes D_1 and D_2 for increased steady state efficiency with a peak current optimization

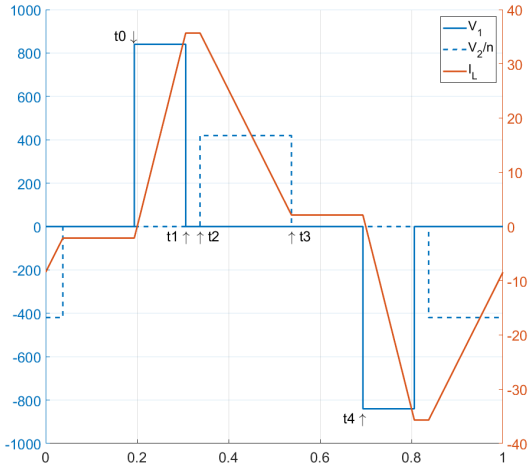


Figure 2.5: TPS mode 5

as a reference. As a result the triangular operation is shifted into the mode 1 TPS region at low power, as switching losses are reduced here due to increased number of ZVS events. Although this controller does maximize the efficiency, it has a slow dynamic response and its implementation is fairly complex. It also requires high speed voltage and current sensors on the input to measure the efficiency.

2.2.3 Hybrid modulation methods

Instead of following a complex optimization process, it is also possible to combine multiple different modulation techniques. The modulation techniques used are typically fairly simple in implementation, but not fully optimized for minimum current or ZVS.

The most basic hybrid modulation methods simply combine two different modulation techniques. For example in [23] and [26] a combination of SPS and a modified triangular modulation modulation with higher maximum power than normal triangular modulation is proposed. This allows the system to maintain soft switching in a relatively large part of the operating range. This comes at the cost of increased rms current, as the proposed modified triangular modulation has high circular current.

A more optimal hybrid modulation is proposed in [8], utilizing SPS in its ZVS range. Once the limit of the ZVS range has been reached, the duty cycle of the higher voltage bridge will decrease until the ratio between voltage and duty cycles is equal, this operating region can be implemented as a specific case of EPS modulation. The low power boundary of this region coincides with the maximum power of triangular modulation, which is used at even lower power. Although it doesn't provide full range ZVS, it does provide ZCS where ZVS is absent. Compared to the previously discussed TPS modulation methods, it has increased conduction and switching losses, but its implementation is very simple.

The efficiency of the above methods could be enhanced by providing a small duty cycle offset similar to what is done for trapezoidal modulation in [21]. This would provide more ZVS events compared to the original methods, although it does increase the complexity of the modulation techniques by a certain degree.

2.3 General ZVS conditions

To achieve ZVS in a DAB converter, the energy stored in the leakage inductance should be greater or equal to the energy required to fill or empty the junction capacitance of the switches, and the energy to overcome the voltage applied on L_s by the non-switching H-bridge. A similar ZVS analysis has been done for EPS modulation in [22] and [20], and for DPS modulation in [13]. However, as these are restricted to EPS and DPS modulation respectively, they do not cover all types of switching events. Given the variety of modulation techniques that will be considered, in this subsection, the general ZVS conditions with the minimum or maximum inductor current as the output value will be derived.

To simplify the calculation the voltage applied on the inductor by the input side H-bridge is defined as V_1, The voltage applied to the inductor by the output side H-bridge is defined as V_2. V_1 can be $\pm V_{in}$ or 0, V_2 can be $\pm V_{out}$ or 0, depending on the control signals sent to the switches of both H-bridges.

Different switching events can be considered. First is the single H-bridge, which can either be switched to or from a state where the output of the H-bridge is 0. This affects the contribution of the output of the non-switching H-bridge to the ZVS requirement. There is also the case where D_1 or D_2 is equal to one, where both half bridges in the same H-bridge switch at the same time. It is also possible to have multiple half bridges in a different H-bridge switch at the same time.

2.3.1 Single half bridge

The first two cases consider the switching of only a single half bridge, either entering or leaving the zero voltage state of the H-bridge. This can occur in all four half bridges, but the ZVS requirements use the same equations. Figure 2.6 shows the equivalent circuits for both cases of a single bridge switching. The calculations will assume the circuit is lossless, thus in practice some safety margin may be needed.

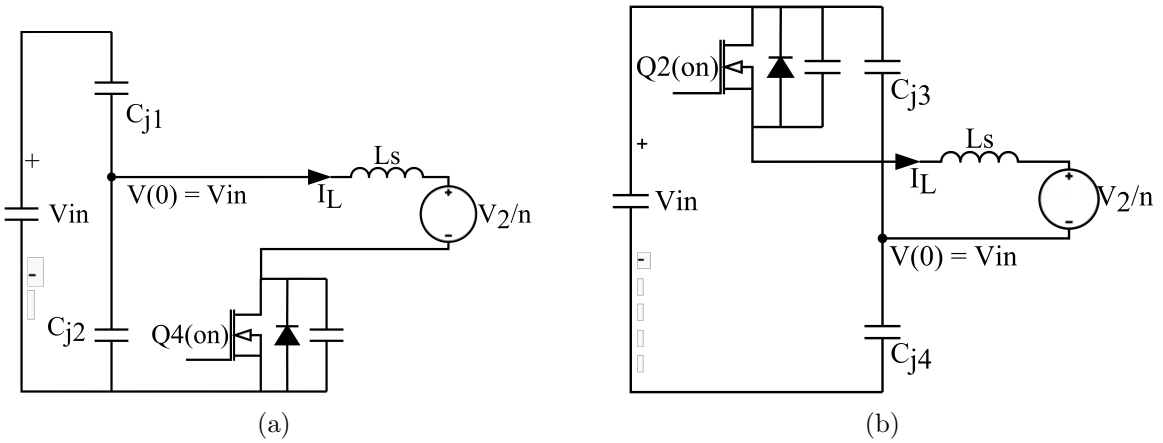


Figure 2.6: Equivalent circuits for transitions from V_{in} to 0 and from 0 to V_{in}

To derive the necessary inductor current, the energy stored in the capacitors and inductor, and the energy consumed by the secondary side voltage will be considered. When switching from a zero state to a positive or negative state, the inductor needs to provide energy for the capacitors, which may be reduced if the voltage applied by the non switching H-bridge also supplies energy.

The energy equation for the input bridge switching from the 0 to the positive V_{in} state is shown in 2.1, which results in equation 2.2 when solved for the inductor current. In these equations E_C represents the energy needed to change the capacitor voltage, while $E_V = Q_c V$ represents the energy provided by the non-switching H-bridge.

$$E_L = E_C - E_V = C_j V_{in}^2 - 2C_j V_{in} \frac{V_2}{n} \tag{2.1}$$

$$I_L = -V_{in}\sqrt{\frac{2C_j}{L}(1 - 2\frac{V_2}{nV_{in}})} \qquad \frac{V_2}{nV_{in}} < 0.5 \tag{2.2}$$

The same principle can be used for switching from a positive state to a 0 state of the H-bridge, however in this case the capacitor contains more energy initially compared to the final state, which leads to a different leads to a different ZVS requirement. The energy equation for this case is shown in equation 2.3, which results in equation 2.4 when solved.

$$E_L = E_V - E_C = 2C_j V_{in} \frac{V_2}{n} - C_j V_{in}^2 \tag{2.3}$$

$$I_L = V_{in}\sqrt{\frac{2C_j}{L}(2\frac{V_2}{nV_{in}} - 1)} \qquad \frac{V_2}{nV_{in}} > 0.5 \tag{2.4}$$

In the above calculations, only positive voltage switching has been considered in the input side H-bridge. In the output side H-bridge, the transformer turns ratio results causes some minor differences in the equation. The equations thus need to be modified to work for both polarities and for the secondary H-bridge, which is done using the same steps as for the above cases. The results of this process are shown in table 2.2. $\Delta V_{1/2}$ in these equations is the change in voltage of the switching H-bridge, which equals the DC voltage on the switching side multiplied by the switching direction. The voltage of the non switching side, $V_{1/2}$ is the output voltage of the secondary H-bridge, which can be either $\pm V_{in/out}$ or 0.

Bridge 1 switching (0 to $\pm V_{in}$)	
$\frac{V_2}{n\Delta V_1} < 0.5$	$I_{L-lim} = -\Delta V_1\sqrt{\frac{2C_j}{L}(1 - 2\frac{V_2}{n\Delta V_1})}$
$\frac{V_2}{n\Delta V_1} \geq 0.5$	$I_{L-lim} = 0$
Bridge 1 switching ($\pm V_{in}$ to 0)	
$\frac{V_2}{n\Delta V_1} > 0.5$	$I_{L-lim} = -\Delta V_1\sqrt{\frac{2C_j}{L}(2\frac{V_2}{n\Delta V_1} - 1)}$
$\frac{V_2}{n\Delta V_1} \leq 0.5$	$I_{L-lim} = 0$
Bridge 2 switching (0 to $\pm V_{out}$)	
$\frac{nV_1}{\Delta V_2} < 0.5$	$I_{L-lim} = \Delta V_2\sqrt{\frac{2C_j}{L}(1 - 2\frac{nV_1}{\Delta V_2})}$
$\frac{nV_1}{\Delta V_2} \geq 0.5$	$I_{L-lim} = 0$
Bridge 2 switching ($\pm V_{out}$ to 0)	
$\frac{nV_1}{\Delta V_2} > 0.5$	$I_{L-lim} = \Delta V_2\sqrt{\frac{2C_j}{L}(2\frac{nV_1}{\Delta V_2} - 1)}$
$\frac{nV_1}{\Delta V_2} \leq 0.5$	$I_{L-lim} = 0$

Table 2.2: ZVS conditions for single switching events

2.3.2 Both half-bridges

The other cases involve both half bridges in an H-bridge switching at the same time. This only occurs during EPS and SPS modulation when switching from the negative state of the H-bridge to a positive one, or reversed. the energy stored in the capacitors of the one H-bridge can flow

into the capacitors of the other H-bridge. Given that the capacitor energy is already present, the energy absorbed or delivered by the secondary side voltage is the only contributing factor to the ZVS conditions. The same energy equation as for the single half bridge switching events is used, as shown in equation 2.5, based on figure 2.7.

$$Q_c = 2V_1C_j \qquad E_{V2} = Q_c * \frac{V_2}{n} = 2V_{in}C_j\frac{V_2}{n} \qquad E_L = \frac{1}{2}L_sI_L^2 \tag{2.5}$$

Solving these equations for I leads to the minimum amplitude of the inductor current shown in table 2.3, the amplitude for the secondary side H-bridge is calculated using the same method from the secondary side of the transformer.

Bridge 1 switching	
$\Delta V_{in} * V_2 < 0$	$I_{L-lim} = \frac{V_2}{n}\sqrt{\frac{4C_j}{L_s}\lvert\frac{nV_{in}}{V_2}\rvert}$
$\Delta V_{in} * V_2 \geq 0$	$I_{L-lim} = 0$
Bridge 2 switching	
$\Delta V_{out} * V_1 < 0$	$I_{L-lim} = -nV_1\sqrt{\frac{4C_j}{L_s}\lvert\frac{V_{out}}{nV_1}\rvert}$
$\Delta V_{out} * V_1 \geq 0$	$I_{L-lim} = 0$

Table 2.3: ZVS condition when two half bridges in the same H-bridge switch at once

In case both half bridges in the same H-bridge turn on or off at the same time, ZVS is only possible in one of the two half-bridges, as both half bridges require a different current polarity to achieve ZVS. The conditions that apply to either of the half bridges are similar to those of the single switch case from the 0 to the positive or negative output state, as the non-ZVS switch will conduct through the diode as a result of the current polarity. This only occurs when the duty cycle of one of the H-bridges approaches zero, at which point it will be more optimal stop the H-bridge from switching to reduce losses.

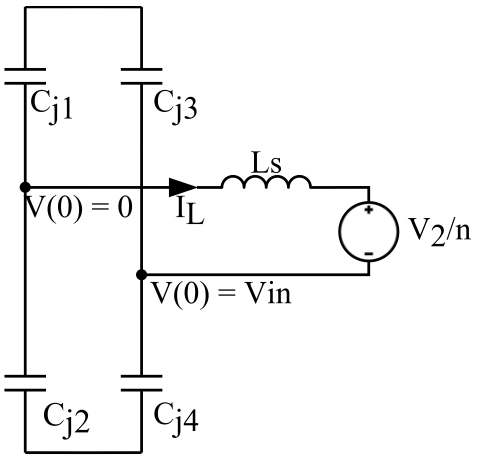


Figure 2.7: Equalvalent circuit when both half bridges switch at once

2.3.3 Cases involving both H-bridges

It is also possible for H-bridges on both sides to switch at the same time at the boundaries of the switching modes. If both H-bridges increase in voltage, similar to the previous non-ZVS case, only one H-bridge can have ZVS. This generally only occurs on the boundaries between switching modes, like on the boundary between TPS mode 1, mode 3 and mode 4. The switch

that gets ZVS is determined by the current direction in this case, where the inductor current will fill or drain the capacitors of the ZVS bridge, while the non-ZVS bridge will conduct through the diode of the switch that was previously on. The inductor current requirement can thus be calculated as if the ZVS bridge has a single switching event.

Alternatively the two H-bridges can switch in opposing directions, which will lead to decreased ZVS requirements. The part of the operation regions this occurs in is located at the boundary between TPS mode 3 and 5, and at the outer boundary of TPS mode 4. These events are not considered in the calculations as they occur in sub-optimal operating regions that suffer from high circular currents.

2.4 Proposed modulation method

While a peak current optimization based modulation provides low currents stress and full soft range soft switching, at low power where the converter operates using ideal triangular modulation, it only has 2 out of 8 ZVS switching events. To improve efficiency at low power, a new modulation method is proposed which maximizes the number of ZVS events in the operating range. As the modulation method is similar to that of the peak current optimization, it should still retain low current stress.

The proposed modulation method will operate in mode 1 TPS at low power and in EPS at high power, similar to what resulted from the efficiency optimizing control loop in [11]. This will increase low power efficiency compared to the peak current optimizations. The boundaries of the DAB converter operating modes are analysed and a transition region is added to maximize the number of ZVS events over the operating range.

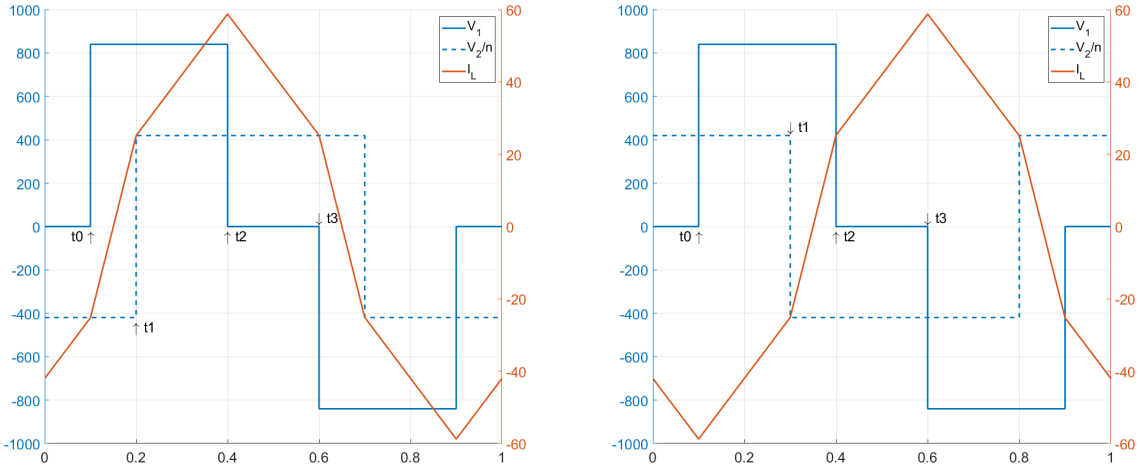
The control law will remain close to that of the optimizations for peak current done in [5], [10] and [19]. This is preferred over the rms current optimization in [22] for the high power EPS region, as the peak current optimization results in a linear, easy to implement modulation method, while the difference in rms current is rather small. The rms current optimization uses non-linear equations, including multiple square roots, which is not very suitable for implementation in a microcontroller.

In this section, firstly the ZVS constraints of EPS and mode 1 TPS modulation will be analysed. The ZVS conditions of a transition region which uses mode 1 EPS, a specific case of mode 1 TPS, will also be analysed. Based on this analysis a control law will be created, taking into account the ZVS analysis. In these equations k will be used to represent the voltage gain between the two sides of the converter, k is defined as $k = \frac{V_{out}}{nV_{in}}$.

2.4.1 EPS ZVS boundaries

EPS has two operating modes, mode 1 EPS is a specific case of mode 1 TPS, and mode 2 EPS a case of mode 4 TPS. Depending on whether $k > 1$ or $k < 1$ either D_2 or D_1 will be equal to 1, which is not the case for the TPS modes. Only mode 2 EPS will be discussed here as mode 1 EPS is a variation of mode 1 TPS, which will be covered at a later point. The forward and reverse power transfer voltage and current waveforms for mode 2 EPS are shown in figure 2.8.

The required current amplitude for ZVS depends on the conditions under which the switching occurs. The switching events at t_0 in figure 2.8a and the switching event at t_2 in figure 2.8b are symmetrical and will have the same current amplitude during switching. However due to the different voltages applied by the non-switching H-bridge, their ZVS requirements will be different. Similar differences can be found for the other switching events depending on the polarity of Φ and k.



(a) (b)

Figure 2.8: EPS case 2 in forward and reverse power transfer operation

To simplify the control system, the polarity of Φ with the worst case ZVS requirements will be used in the calculations. When considering a positive polarity of Φ for $k < 1$, the switching event at t_0 in figure 2.8 will have a larger ZVS requirement compared to its symmetrical point at t_2 for a negative polarity of Φ. For the switching event at t_1 this is reversed, having a larger ZVS requirement for a negative polarity of Φ.

For $k > 1$, the worst case polarities of Φ are reversed compared to $k < 1$ at the same points in the voltage and current waveform.

Solutions when $V_{in} > \frac{V_{out}}{n}$

The current values at the switching times are mirrored between the two conduction modes, where t_0 in forward mode corresponds to the current at t_2 in reverse mode. In these equations the absolute value of Φ is used assuming symmetry between forward and reverse power transfer. This leads to the inequalities based on forward power transfer in equation 2.6(t_0), 2.7(t_1) and 2.8(t_2), where k_w is the worst case value of k for the specific the ZVS requirements.

$$-\frac{T_s}{4L_s}(D_1(V_{in}+\frac{V_{out}}{n})+(2|\Phi|-2)\frac{V_{out}}{n}) < -V_{in}\sqrt{\frac{2C_{j1}}{L}(1+2k)} \qquad k_w = 1 \qquad (2.6)$$

$$\frac{T_s}{4L_s}(V_{out}/n+(2|\Phi|-1)V_{in}) > nV_{in}\sqrt{\frac{4C_{j2}k}{L}} \qquad k_w = 1 \qquad (2.7)$$

$$\frac{T_s}{4L_s}(D_1V_{in}+(2|\Phi|-D_1)V_{out}/n) > V_{in}\sqrt{\frac{2C_{j1}}{L}(2k-1)} \qquad k_w = 1 \qquad (2.8)$$

By filling in the the worst case values for k, and solving the inequalities, simplified boundary values for the ZVS region of mode 2 EPS can be derived. The solutions, which are valid in both directions of operation, and are shown in equation 2.9(t_1), 2.10(t_0) and 2.11(t_2). It can be seen that there are two ZVS requirements on D_1, these are both for a different half bridge. In practice the ZVS requirement in equation 2.11 is not relevant as it lies outside of the boundary

of EPS mode 2, with the exception of k being very close to 1. Under these circumstances the ZVS requirement on D_1 will only be effective for very small values of $|\Phi|$.

$$|\Phi| > 0.5 - 0.5k + \frac{2nL_s}{T_s}\sqrt{\frac{4C_{j2}}{L_s}} \tag{2.9}$$

$$D_1 > \frac{k(2-2|\Phi|) + \frac{4L}{T_s}\sqrt{\frac{6C_{j1}}{L}}}{1+k} \tag{2.10}$$

$$D_1 > \frac{-2k|\Phi| + \frac{4L}{T_s}\sqrt{\frac{2C_{j1}}{L}}}{1-k} \tag{2.11}$$

Solutions when $V_{in} < \frac{V_{out}}{n}$

Using the exact same method, a set of solutions for when V_{in} is smaller than $\frac{V_{out}}{n}$ can also be derived. Here equation 2.15 applies to the primary side H-bridge, while equation 2.16 and 2.17 apply to the half bridges of the secondary side H-bridge.

$$-\frac{T_s}{4L_s}(D_2(V_{in} + \frac{V_{out}}{n}) + (2|\Phi| - 2)V_{in}) < -V_{out}\sqrt{\frac{2C_{j2}}{L}(1 + 2k^{-1})} \qquad k_w = 1 \tag{2.12}$$

$$\frac{T_s}{4L_s}(V_{in} + (2|\Phi| - 1)\frac{V_{out}}{n}) > V_{out}\sqrt{\frac{4C_{j1}k^{-1}}{L}} \qquad k_w = 1 \tag{2.13}$$

$$\frac{T_s}{4L_s}(D_2(\frac{V_{out}}{n} - V_{in}) + 2|\Phi|) > V_{out}\sqrt{\frac{2C_{j2}}{L}(2k^{-1} - 1)} \qquad k_w = 1 \tag{2.14}$$

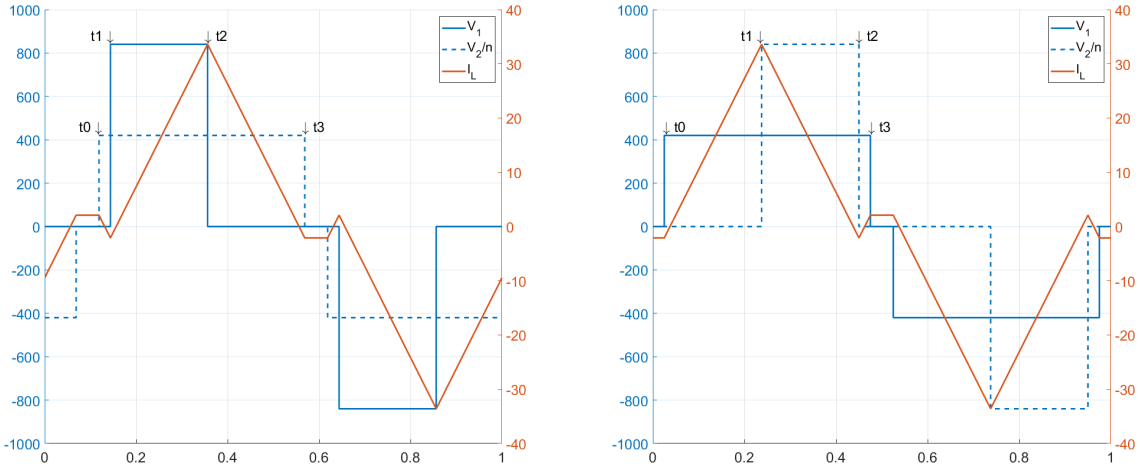
$$|\Phi| > 0.5 - 0.5k^{-1} + \frac{2L_s}{T_s}\sqrt{\frac{4C_{j1}}{L_s}} \tag{2.15}$$

$$D_2 > \frac{k^{-1}(2-2|\Phi|) + \frac{4nL}{T_s}\sqrt{\frac{6C_{j2}}{L}}}{1+k^{-1}} \tag{2.16}$$

$$D_2 > \frac{-2k^{-1}|\Phi| + \frac{4nL}{T_s}\sqrt{\frac{2C_{j2}}{L}}}{1-k^{-1}} \tag{2.17}$$

2.4.2 mode 1 TPS ZVS boundaries

The approach for mode 1 TPS will differ from the one in the EPS case, as in mode 1 TPS there are more control variables to take into account. Figure 2.9 shows the waveforms for mode 1 TPS operation. The H-bridge with the larger duty cycle, always switches with zero voltage applied by the non-switching H-bridge, making the switching events at t_0 and t_3 independent of k. The switching events at t_1 and t_2 are dependent on k. To simplify the equations a similar as used for EPS mode 2 is used, where worst case values of k are assumed. For the switching event at t_1, depending on the polarity of k $k_w = 0$ or $\frac{1}{k_w} = 0$ gives the worst case ZVS requirement, while for the switching event at t_2 this occurs at $k_w = 1$.



(a) (b)

Figure 2.9: Mode 1 TPS waveforms for $V_{in} > V_{out}$ and $V_{in} < V_{out}$

ZVS equations when $V_1 > \frac{V_2}{n}$

Below the ZVS inequalities for mode 1 TPS are shown.

$$\frac{T_s}{4L_s}(D_2\frac{V_{out}}{n} - D_1V_{in}) > V_{out}\sqrt{\frac{2C_{j2}}{L_s}} \qquad 0 < k < 1 \tag{2.18}$$

$$\frac{T_s}{4L_s}(2\Phi\frac{V_{out}}{n} + D_1(\frac{V_{out}}{n} - V_{in})) < -V_{in}\sqrt{\frac{2C_{j1}}{L}(1-2k)} \qquad worstcasek = 0 \tag{2.19}$$

$$\frac{T_s}{4L_s}(2\Phi\frac{V_{out}}{n} + D_1(V_{in} - \frac{V_{out}}{n})) > V_{in}\sqrt{\frac{2C_{j1}}{L}(2k-1)} \qquad worstcasek = 1 \tag{2.20}$$

This results in the following restrictions to the duty cycle:

$$D_2 > \frac{D_1}{k} + \frac{4nL_s\sqrt{\frac{2C_{j2}}{L_s}}}{T_s} \tag{2.21}$$

$$D_1 > \frac{2k\Phi}{1-k} + \frac{4L_s\sqrt{\frac{2C_{j1}}{L_s}}}{(1-k)T_s} \tag{2.22}$$

$$D_1 > -\frac{2k\Phi}{1-k} + \frac{4L_s\sqrt{\frac{2C_{j1}}{L_s}}}{(1-k)T_s} \tag{2.23}$$

This can be rewritten as:

$$D_1 > \frac{2k|\Phi|}{1-k} + \frac{4L_s\sqrt{\frac{2C_{j1}}{L_s}}}{(1-k)T_s} \tag{2.24}$$

$$D_2 > \frac{2|\Phi|}{1-k} + \frac{4L_s}{T_s}(\frac{\sqrt{\frac{2C_{j1}}{L_s}}}{k(1-k)} + n\sqrt{\frac{2C_{j2}}{L_s}}) \tag{2.25}$$

where $|\Phi_{TRG-lim}|$ in the equation below is the the maximum phase shift for full ZVS mode 1 TPS operation, as at which point $D_2 = 1$ and cannot be increased further.

$$|\Phi_{TRG-lim}| = 0.5 - 0.5k - \frac{2L_s}{T_s}(\frac{\sqrt{\frac{2C_{j1}}{L_s}}}{k} + n(1-k)\sqrt{\frac{2C_{j2}}{L_s}}) \tag{2.26}$$

ZVS equations when $V_1 < \frac{V_2}{n}$

When the When the voltage ratio k is bigger than 1, operation is changed slightly. In 2.27, 2.28 and 2.29 the modified ZVS equations for operations under these conditions are shown for t_0, t_1 and t_2 in 2.9b.

$$-\frac{T_s}{4L_s}(D_1V_{in} - D_2\frac{V_{out}}{n}) < -V_{in}\sqrt{\frac{2C_{j1}}{L_s}} \qquad 0 < k < 1 \tag{2.27}$$

$$\frac{T_s}{4L_s}(2\Phi V_{in} + D_2(\frac{V_{out}}{n} - V_{in})) > V_{in}\sqrt{\frac{2C_{j2}}{L_s}(1-2k^{-1})} \qquad worstcase k^{-1} = 0 \tag{2.28}$$

$$\frac{T_s}{4L_s}(2\Phi V_{in} + D_2(V_{in} - \frac{V_{out}}{n})) < -V_{in}\sqrt{\frac{2C_{j2}}{L_s}(2k^{-1}-1)} \qquad worstcase k^{-1} = 1 \tag{2.29}$$

Solving these equations, and merging the conditions for t_1 and t_2 in a similar way as was done for $k < 1$, results in the conditions in equation 2.30 and 2.31. The requirement for D_1 assumes operation on the boundary of D_2, as D_2 has been substituted in the equation for D_1. The phase shift boundary for ZVS is shown in equation 2.32.

$$D_2 > \frac{2k^{-1}|\Phi|}{1-k^{-1}} + \frac{4nL_s\sqrt{\frac{2C_{j2}}{L_s}}}{(1-k^{-1})T_s} \tag{2.30}$$

$$D_1 > \frac{2|\Phi|}{1-k^{-1}} + \frac{4nL_s}{T_s}(\frac{n\sqrt{\frac{2C_{j2}}{L_s}}}{k^{-1}(1-k^{-1})} + \sqrt{\frac{2C_{j1}}{L_s}}) \tag{2.31}$$

$$|\Phi_{TRG-lim}| = 0.5 - 0.5k^{-1} - \frac{2L_s}{T_s}(\frac{n\sqrt{\frac{2C_{j2}}{L_s}}}{k^{-1}} + (1-k^{-1})\sqrt{\frac{2C_{j1}}{L_s}}) \tag{2.32}$$

2.4.3 Resulting control law

The ZVS boundaries presented in this section can be used to construct a control law. The control law will consist of three regions, the (mode 2) EPS region at high power, the mode 1 TPS region at low power, and a transition region to connect both regions.

Values of D_1 and D_2 in the EPS region are determined by linear extrapolation between two points. The first point is located at $|\Phi| = 0.5$ and $D_1 = D_2 = 1$, where the converter power is maximized. The second point is determined by the intersection between the ZVS boundary on $|\Phi|$ for EPS mode 2 shown in equation 2.9 and 2.15, and the boundary between EPS mode 1 and 2, which occurs at $D_{1/2} = 1 - 2|\Phi|$. By choosing the boundary of the EPS region in this way, all ZVS requirements except for those in equation 2.10 and 2.16 are met. This ensures 6 out of 8 switching events can maintain ZVS in this operating mode.

The mode 1 TPS region, which will also be referred to as the triangular region, is defined by the duty cycle equations presented in the previous subsection. It starts at $\Phi = 0$, and ends at $\Phi_{TRG-lim}$, at which point either D_1 or D_2 will be equal to 1. At the boundary of this operation region, the converter will operate in mode 1 EPS.

By themselves, the EPS and triangular region are not connected, creating a discontinuity in the control law. To resolve this, a transition region is added in between. The values of D_1 and D_2 are calculated using linear extrapolation between the boundaries of the triangular and EPS region.

A special case of the control law occurs when k approaches 1. Here $|\Phi_{TRG-lim}|$, the boundary of the triangular region, becomes negative. This means that the system will not operate in the triangular region under these conditions. Instead the converter will operate in the transition

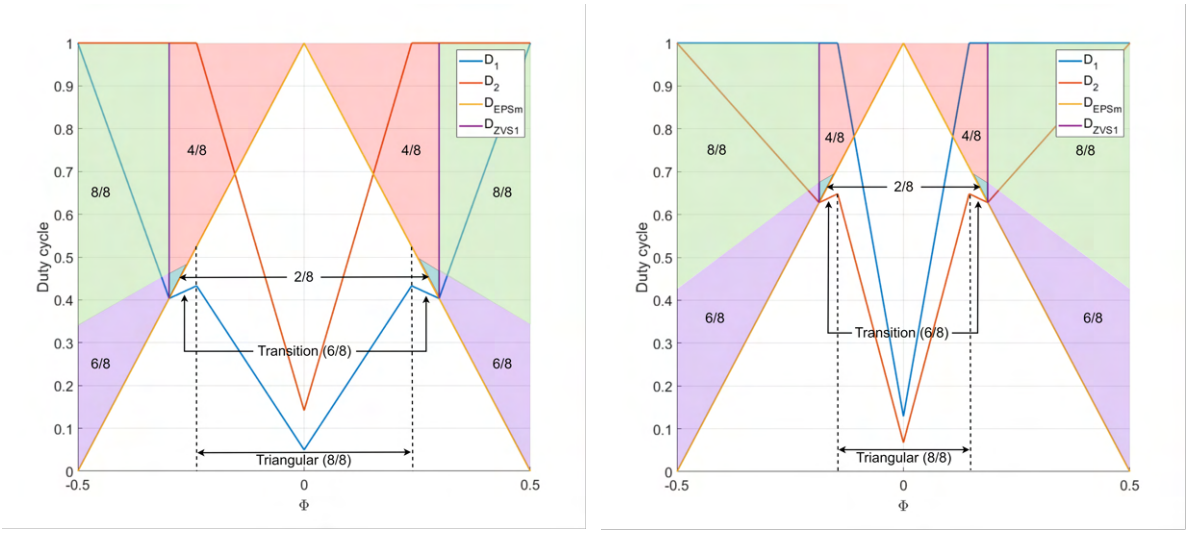
region at $\Phi = 0$. The boundary values for D_1 and D_2 can still be calculated using the negative value of $|\Phi_{TRG-lim}|$, however the ZVS requirements at t_1 and t_2 in Figure 2.9 will not be met. The ZVS requirements at t_0 and t_3 will still be met under these conditions, maintaining 4 out of 8 ZVS switching events.

Operation in the transition region occurs in mode 1 EPS, a special case of mode 1 TPS where depending on the voltage gain k either D_1 or D_2 is equal to 1. In this situation, only the ZVS conditions at t_0 and t_3 in figure 2.9 change compared to normal mode 1 TPS operation, as the t_0 and t_3 switching events now occur at the same time. Given that the voltage of the non-switching side is always zero when this occurs, the ZVS current requirement will also be zero, based on the values from table 2.3. In the case of $k < 1$ the ZVS requirement for D_2 changes to $D_2 > \frac{D_1}{k}$, while for $k > 1$ it changes to $D_1 > \frac{D_2}{k^{-1}}$.

In practice the current during the specified switching events will not be zero, as at the boundary of the mode 1 triangular and mode 2 EPS region, the currents will also be non-zero. The current during the t_0 and t_3 switching events will be in between that for the triangular and EPS operating regions. This means the ZVS conditions at t_0 and t_3 will always be met in the transition region. From the ZVS requirements that apply to t_1 and t_2, only one of the two will be met in the transition region if $|\Phi_{TRG-lim}| > 0$, if $|\Phi_{TRG-lim}| < 0$, neither will be met.

The resulting control law is shown in figure 2.10, here D_{EPS} marks the boundary between of EPS mode 1 and mode 2. D_{ZVS1} shows the ZVS boundary on $|\Phi|$ in the EPS region, which is used together with D_{EPS} to define the EPS region boundary point of the control law. In EPS mode 2, the number of ZVS events per region is shown. It also includes the triangular and transition regions, which are marked using arrows.

Figure 2.11 shows the control law at unity voltage gain. It can be observed that D_2 remains constant at a value of 1, never entering the triangular region where D_2 would be smaller than 1.



(a) Case: $V_{in} = 640$, $V_{out} = 250$, n = 0.875

(b) Case: $V_{in} = 640$, $V_{out} = 840$, n = 0.875

Figure 2.10: Duty cycle waveforms for $k < 1$ and $k > 1$ with ZVS regions

2.4.4 Overall ZVS performance

The proposed control law will provide full ZVS in most of the operating range except for the transition region, and a small part of the EPS operating region bordering the transition region,

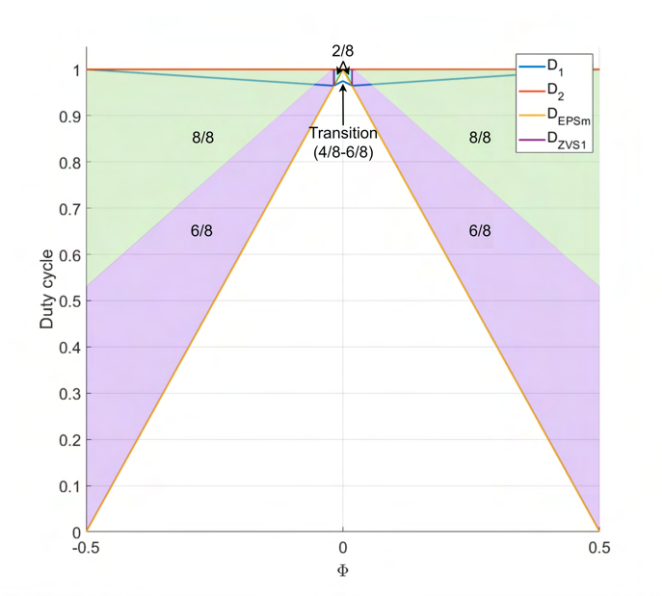


Figure 2.11: Duty cycle waveforms for $k = 1$

where 6/8 switches will have ZVS. When the voltage gain is close to one, the ZVS events in the transition region are reduced to 4/8. It is expected that this will increase the operating efficiency compared to the non-ZVS peak current optimizations in [5], [10] and [19].

2.5 Transient Behaviour

Given the application of the converter, which is EV charging, it is expected that the converter operation will be fairly static. However during the startup sequence, or during a load change this does not apply. In these situations, attention must be paid to the initial current at the start of each switching period. If a large change in output power is made without taking this into account, it can lead to a DC offset in the leakage inductance current and magnetizing current. The offset of the leakage inductance, which can be very significant, can obstruct ZVS, and cause additional conduction losses. The DC-offset of the magnetizing current mainly involves the risk of transformer saturation, which an in turn cause the transformer to overheat.

In [3] various methods of removing these transient DC offsets are discussed, utilizing transient states to transition between operating points of the converter. Various solutions are provided which can transition in less than half a cycle, while other need slightly less than a whole switching cycle. In [9] a general method that can be applied to all modulation types is proposed, it prevents a offset from occurring in both the leakage and magnetizing current, with a transition of less than a half cycle.

Although methods using a transient state do solve the transient issue, these methods have the disadvantage of increasing the control complexity. This increase in complexity is caused by the introduction of a variable length switching period every transition. It also requires a boundary for the minimum amount of change in power or voltage before something is considered a transition, otherwise it will be triggered unintentionally by noise on the voltage measurement. In this thesis an alternative method is proposed, where every switching cycle will starts and ends at a current of 0 A. This prevents a DC offset in the leakage inductor current from occurring during a change in power output, but does not prevent an offset in the magnetizing current. In return the proposed method is much simpler to implement as a fixed duty cycle can be used. To be able to start each switching period at 0 A, the zero current regions in the operating

waveforms need to be analysed.

2.5.1 Zero current regions

The system has two operating modes, mode 2 EPS and mode 1 TPS. In mode 1 TPS, there will always be a zero crossing during the time that the lower voltage side is one, while the high voltage side is 0. Whether the left or right side of the high voltage waveform is selected depends on the direction of the phase shift, and whether the voltage ratio is bigger or smaller than one.

To minimize the transition switching losses, similar switching states should be chosen as the start or end point of the period. When $V_{in} > \frac{V_{out}}{n}$ the switching state chosen is $V_2 = \frac{V_{out}}{n}$, with $V_1 = 0$ or $V_1 = -V_{in}$, depending on the operating mode. In mode 1 TPS this occurs to the left of t_1, or the right of t_2, depending on the polarity of the phase shift, as seen in figure 2.9. In mode 2 EPS this occurs around t_3 in forward conduction mode, and around $t_2 + 0.5T_s$ in reverse conduction mode, in figure 2.8.

Similar states can be found for when $V_{in} < \frac{V_{out}}{n}$, based on the input side voltage $V_1 = V_{in}$. Here the output side voltage on the inductor can be either $V_2 = 0$ or $V_2 = -\frac{V_{out}}{n}$.

The solution are calculated by taking one of the boundaries of the 0 current region, and adding a ΔI term that is equal to $\frac{V_{inductor}}{L}t$. The resulting equation is then solved for t. This gives a time offset relative to one of the boundaries of the 0 current region. By dividing this time offset by the sample time, it can be normalized in a range from 0 to 1.

An additional offset is required as the point at which the boundary of the zero current region is located is not at the start of a switching cycle. For the calculation of this term, it is assumed that the primary side voltage has a fixed phase shift, while the secondary voltage is shifted by Φ. The standard position can be observed in figure 2.8 and 2.9.

Mode 1 TPS solutions

In mode 1, there is a total of 4 possible cases. Φ bigger or smaller than 0, and V_{in} being bigger or smaller than $\frac{V_{out}}{n}$. The solutions for the offset D_{off} for the mode 1 cases are shown in table 2.5. D_{off} is the offset of the zero current switching point from the start of the period, and can vary from 0 to 1.

Voltage gain	Phase shift	D_{off}
$k < 1$	$\Phi > 0$	$0.5\lvert\Phi\rvert + \frac{D_1}{4}k^{-1} + 0.25$
$k < 1$	$\Phi < 0$	$-0.5\lvert\Phi\rvert + \frac{D_1}{4}k^{-1} + 0.25$
$k > 1$	$\Phi > 0$	$-\frac{D_2}{4}k + 0.25$
$k > 1$	$\Phi < 0$	$\frac{D_2}{4}k + 0.25$

Table 2.4: Transient conditions

Mode 2 EPS solutions

In mode 2 EPS there are 8 possible cases. Similar to the solutions for mode 1 TPS, they are separated by the polarity of Φ and the voltage ratio. In addition to this, the polarity of the current at the switching event around which the zero current region is found determines on which side of the switching event the zero current point is found. For $V_{in} > \frac{V_{out}}{n}$ the current is shown in equation 2.33, and for $V_{in} < \frac{V_{out}}{n}$ it is shown in equation 2.34.

$$I_{0-EPS_1} = \frac{Ts}{4L}(D1 * (k^{-1} + 1) + 2|\Phi| - 2) \tag{2.33}$$

$$I_{0-EPS_2} = \frac{Ts}{4L}(D2 * (1+k) + 2|\Phi| - 2) \tag{2.34}$$

$k < 1$	$\Phi > 0$	$I_{0-EPS-2} > 0$	$\frac{2\|\Phi\|-2}{4(k^{-1}+1)} + 0.75$
$k < 1$	$\Phi > 0$	$I_{0-EPS-2} < 0$	$\frac{\|\Phi\|}{2} + \frac{D_1}{4}k^{-1} + 0.25$
$k < 1$	$\Phi < 0$	$I_{0-EPS-2} > 0$	$-\frac{2\|\Phi\|-2}{4(k^{-1}+1)} + 0.75$
$k < 1$	$\Phi < 0$	$I_{0-EPS-2} < 0$	$1.25 - \|\Phi\|/2 - \frac{D_1}{4}k^{-1}$
$k > 1$	$\Phi > 0$	$I_{0-EPS-1} > 0$	$k\frac{2\|\Phi\|-2}{4(1+k)} + \frac{D_1}{4}$
$k > 1$	$\Phi > 0$	$I_{0-EPS-1} < 0$	$-\frac{D_2}{4}k + \frac{D_1}{4}$
$k > 1$	$\Phi < 0$	$I_{0-EPS-1} > 0$	$-k\frac{2\|\Phi\|-2}{4(1+k)} + \frac{D_1}{4}$
$k > 1$	$\Phi < 0$	$I_{0-EPS-1} < 0$	$\frac{D_2}{4}k + \frac{D_1}{4}$

Table 2.5: Transient conditions

2.5.2 Magnetizing current

Using these equation for transient behaviour results in the preservation of ZVS in transient cases, but it neglects the magnetizing current. While at positive Φ during steady state the magnetizing current at the start of a period will be positive, at negative Φ it will be negative. In the worst case scenario, if a transition from Φ to $-\Phi$ were to occur, a DC offset in the magnetizing current of 2x the $I_{mag-peak}$ can occur.

A smaller magnetizing current offset can be obtained if the initial states of the switches at the start of each switching period are neglected. Instead the converter will try to maintain an average negative (or positive) voltage during the first half of each switching period. This will result in a positive magnetizing current at the start of each period during steady state, regardless of the polarity of Φ, at the cost of ZVS during the transition. This limits the maximum DC offset to only 1x $I_{mag-peak}$. In the case of $k < 1$, for positive Φ the equations remain unchanged. For negative Φ a switching state where V_2 is negative can be implemented, by applying a normalized phase shift of 0.5 to the offset equations.

The option to reduce the peak magnetizing flux is preferred over the reduction in switching loss when a transition from positive to negative Φ occurs. This choice is made as the peak magnetizing flux has a larger impact on the circuit design than the occasional additional switching loss. It should be noted that a transition from positive to negative power is not something that is expected to occur often for EV charging application.

2.6 ZVS range extention

The proposed modulation method introduces improvements to the number of ZVS events compared to other modulation methods, but it still does not operate with full ZVS over the entire operating range. An example of this would be operation at higher output voltage, where operation will occur in the transition region at full power. As it is likely that the converter will operate at full power a majority of the time, operating with a reduced number of ZVS events at this operating point is undesirable.

Through variable frequency operation, and by using alternative charging profiles, it is theoretically possible to extend the ZVS range to the full operating range.

The primary idea behind the ZVS range extention is that variable frequency operation can be used to ensure the converter always operates in a mode with full ZVS while operating at

maximum power. By combining this with alternative charging profiles, that use the converter either at full power, or turn it off, full ZVS operation can be ensured.

Charging profiles suitable for this include pulsed charging, and the Multistep Constant Current (MSCC) charging profile when using multiple DAB converters connected in parallel [14]. For a pulsed charging profile, the converter operates at full power until a voltage limit is reached, at which point it shuts off for a certain time. For a parallel DAB converter configuration, one of the parallel converters is shut off every time the voltage limit is reached, reducing the power in steps.

2.6.1 Variable frequency operating modes

To obtain the desired full ZVS operation, the converter should always operate in the triangular region, or the full ZVS part of the EPS region. This can be achieved by increasing the switching frequency, which decreases the output power, requiring an increase in Φ to achieve the same power. As a result operation will shift towards the EPS region, where full ZVS can be achieved.

Similarly if the switching frequency is reduced, Φ needs to be reduced to maintain the same output power. The lower value of Φ will shift operation towards the triangular region.

Although various combinations of increased and decreased frequency are possible, a continuous switching frequency over the operating region is desired, to simplify implementation in a lookup table. A discontinuity would result in the lookup table selecting an in between value at the discontinuity, where the system does not operate with full ZVS. The lookup table could also be operated in a stepwise manner, instead of the default point-slope method, however an increase in resolution and would be required, increasing memory usage.

In table 2.6 the maximum and minimum frequencies are shown for various combinations of frequency changes. These are calculated by looping through Phi until the positive and negative maximum power is reached. Once this power is reached, the operating mode will be checked. When the system operates in an undesirable operating mode like the transition region or the non-ZVS part of the EPS region, the switching period is increased or decreased. The Power calculation is then repeated until the full power operating mode is as desired. The frequency values in 2.6 use a version of of the control equations that includes compensation for non-ideal converter behaviour, which will be discussed in chapter 3.

Continuous	Frequency	f_{min}	f_{max}	ratio($\frac{f_{max}}{f_{min}}$)
no	increase/decrease	11.8 kHz	71.4 kHz	6.07
no	increase	25 kHz	83.3 kHz	3.33
no	decrease	7.14 kHz	25 kHz	3.5
yes	increase	25 kHz	83.3 kHz	3.33
yes	decrease	0 kHz*	25 kHz	-

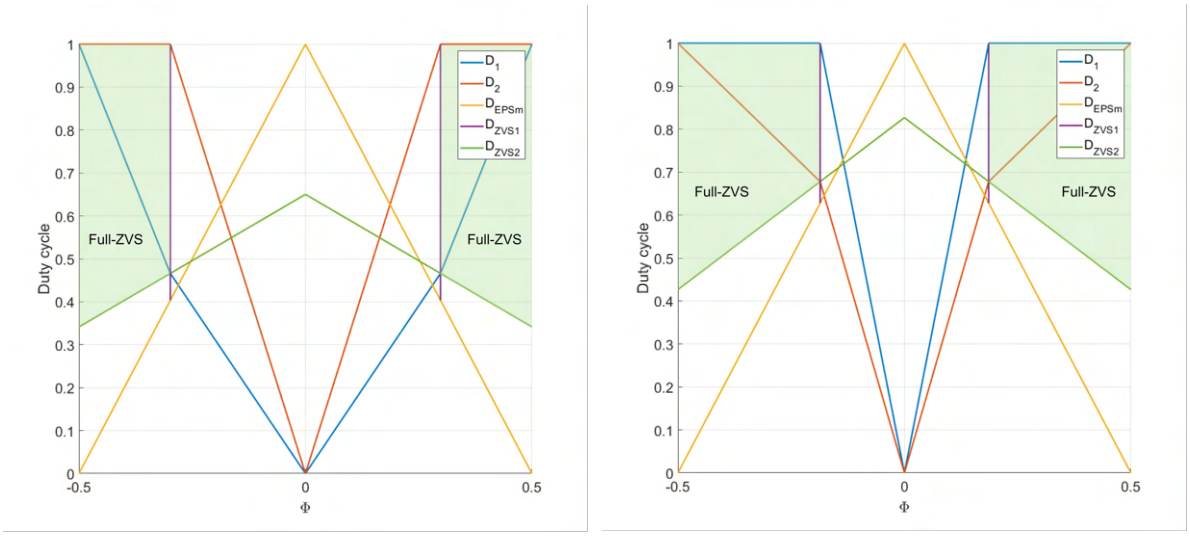
Table 2.6: Variable frequency results for L = 104.3 uH using the proposed control law

Among the options shown in table 2.6, the most viable option is based on a continuous frequency increase while operating only in the EPS region. An increase in frequency is less likely to affect the magnetic design in a negative way and will reduce peak flux density in the transformer core. It is also the only viable option that has a switching frequency continuous over the voltage range, as the alternative continuous approach of always operating in the triangular region fails when operating close to unity gain voltage gain.

2.6.2 Modified EPS modulation

While the Proposed modulation method maximizes the number of ZVS events over the entire operating range, it does not do so specifically for the EPS region. By modifying the control law for variable frequency operation, it is possible to reduce the minimum power while operating at full ZVS in the EPS region. This has the advantage of reducing the maximum switching frequency.

The ZVS range in the EPS mode 2 region can be used more optimally if instead of using the intersection of the EPS mode boundary and the ZVS boundary, the intersection between two EPS mode 2 ZVS boundaries is used to define the boundary of the high power operating region. The resulting control law is shown in 2.12. By using this modified control function, the maximum switching frequency can be reduced from 83.3 kHz to 66.7 kHz, which will reduce switching and inductor core losses.



(a) Case: $V_{in} = 640$, $V_{out} = 250$, n = 0.875

(b) Case: $V_{in} = 640$, $V_{out} = 840$, n = 0.875

Figure 2.12: Duty cycle waveform including the EPS mode 2 ZVS boundaries and mode boundary for variable switching frequency operation

The modified EPS modulation has a parts that operate without ZVS or in the mode 1 TPS region at lower values of Phi. This is only implemented to keep the modulation continuous for lower values of $|\Phi|$. A variable switching frequency will be used to maintain operation in the full ZVS part of the EPS region.

Chapter 3

Simulation

To test the control method that has been created in the previous chapter, a simulation is made using simulink. In this chapter, the simulink model of the DAB converter, the control system and the non-ideal behaviour of the DAB converter will be discussed.

3.1 Hardware modelling

The goal of the hardware model is to provide sufficient accuracy for the performance aspects that matter, like the ZVS behaviour of the converter, while minimizing its complexity. Among the system components the transformer and the MOSFETs are the only parts that affect ZVS behaviour. As semiconductor MOSFETs are temperature dependent, a thermal model should be included too. Parts like protection systems and gate drivers are not considered in the model.

3.1.1 Transformer and inductor model

The transformer of a DAB converter can be constructed in different ways, but generally a high leakage inductance is required. This high leakage inductance can be implemented in two ways, by adding an external leakage inductor, or by using a more complex transformer design.

Integrating the leakage inductance into the transformer offers a more compact solution, and can be achieved by placing the primary and secondary windings on separate transformer legs, while providing a flux path that does not go through the other winding. The air gap of this alternative flux path can then be tuned to provide the desired leakage inductance. Although this solution is compact, the design process for such a transformer will be more complicated.

As the focus of the thesis is on the modulation and control system design, and not on hardware optimization, instead an external leakage inductor and transformer will be used, as this allows for much simpler design.

As the simulation is focussed on verifying the modulation and control system operation, only elements useful to achieving this purpose should be included in the model. These include leakage and magnetizing inductance, and the series resistance of the windings. Other elements like the non-linear behaviour of transformer core materials are not modelled, as the modelling of these is fairly complex, without adding much value to the simulation.

Figure 3.1 shows the equivalent circuit of the simulation model, Here V1 and V2 are the voltage applied by the primary and secondary side H-bridge. Equation 3.1, 3.2 and 3.3 are used to model the transformer and inductor in simulink.

$$\frac{dI_{L1}}{dt} = \frac{V1 - I_{L1}R_{s1} - \frac{V2}{n} + (I_{L1} - I_m)R_{s2}}{L_s} \tag{3.1}$$

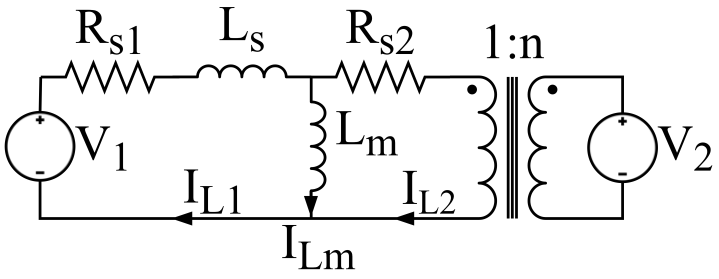


Figure 3.1: Equivalent circuit for the transformer model

$$I_{L2} = I_{L1} - I_{Lm} \tag{3.2}$$

$$\frac{dI_{Lm}}{dt} = \frac{\frac{V_2}{n} + (I_{L1} - I_m)R_{s2}}{L_m} \tag{3.3}$$

3.1.2 Mosfet model

The modelling of the MOSFET can be split up in two different parts, the electrical model, and the thermal model. The thermal model of the MOSFET also includes the model of the heatsink.

Electrical model

The MOSFET is a key part of the simulation, as the focus of the control system to be simulated is on achieving ZVS. To properly simulate the ZVS behaviour, the MOSFET should have an accurate model of the output capacitance. There are many types of models that can be used for this, like the level 1 to level 3 spice models, or the bsim model. In [12] two level 1 spice models are used to approximate the converter behaviour with accuracy similar to a level 3 model, but with reduced computational load compared to the higher level models. Although this approach works, the availability of these models depends on the manufacturer of the selected MOSFET, and is thus not a reliable method.

In [17] a simpler model is presented, which uses an ideal switch with a resistor value equal to R_{DS-on} of the MOSFET, in parallel with a simple diode model, and a variable capacitance. Figure 3.2 shows the schematic of this model.

Compared to the previously mentioned models it has two advantages, the model is very simple, which will increase the simulation speed, and the parameters of the model can be taken directly from the data-sheet. Being able to take the parameters for the model from the datasheet means that it can easily be implemented regardless of which parts are chosen.

The simplicity of this model does not come at the cost of the ZVS modelling, as the simplified model still models the variability of the output capacitance accurately.

One of the disadvantages of this model is that it does not perform well by itself in modelling the switching losses, as it uses an ideal switch in series with a resistor. This means that the only part of the switching loss that is modelled is the energy stored in the output capacitance when the MOSFET turns on. These values can be taken from the datasheet of the selected parts. As the capacitor energy loss during turn-on is already included in the model, it needs to be subtracted from the switching losses losses in the datasheet. This is done in the initialization file of the simulation.

The losses, which are taken as energy values from a lookup table, are spread out over a period equal to the rise or fall time of the MOSFET, the period during which switching losses would normally occur with a more accurate model. This has been done to more accurately

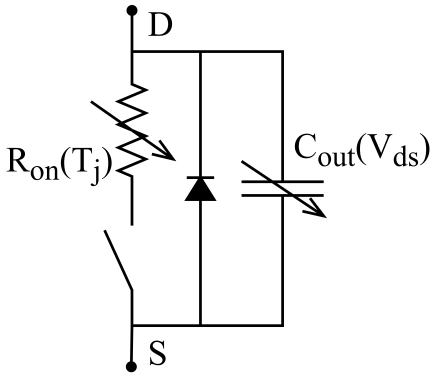


Figure 3.2: Simplified model of the MOSFET

model the ripple in junction temperature. The switching energy is determined by the switch voltage and inductor current at the rising or falling edge of the switching signal. Although this is not the most accurate way of modelling switching losses, it is deemed sufficient for estimating the losses and operating temperature of the system.

Thermal model

To estimate the operating temperature, a thermal model of the MOSFET's and heatsink is needed. All MOSFETs will be connected to a single fan cooled heatsink. Given the application in an EV charger, where the system operates at steady state for an extended period of time, the thermal resistance is the most important part of the model. The thermal capacitance at the MOSFET junction also plays an important role regarding temperature ripple due to the switching losses, however the thermal capacitance of the package and heatsink are not important for steady state application.

Figure 3.3 shows the heatsink and its dimensions. The heatsink will be mounted upside-down under the DAB converter PCB, with the MOSFETs of the primary H-bridge on one side, and the MOSFETs of the secondary H-bridge on the other side.

The thermal behaviour of the model can be made with varying complexity. The simplest model is shown in figure 3.4, where the heatsink is seen as a single unit with uniform temperature. Although this type of model works fine if each MOSFET has similar average losses, this condition is not met for the DAB converter. The possible use of different MOSFETs, differences in ZVS, and the turns ratio can cause can result in different losses in each half bridge.

Figure 3.5 and 3.6 show an improved model. It considers the heatsink to be structured out of four different elements, one for each half bridge. Between the four elements there is a thermal resistance, which can be estimated based on the thermal properties and dimensions of the heatsink material. The method used to calculate the thermal resistance converts the elements to "sheets" with a length, which represents the distance between the elements, and a width and thickness, which are used to calculate the surface area used for the conduction of heat. These dimensions are then used to calculate the thermal resistance.

For the resistance between the elements on the same side, the side surface, only $\frac{2}{3}$ of the width of the element is used. This is done as the width of the element is twice the length, while the switches are mounted approximately in the middle of the element. Due to the mounting position of the switches, the heat that travels through the outside of the elements will follow a longer path, increasing the effective thermal resistance. This results in an aluminium sheet of

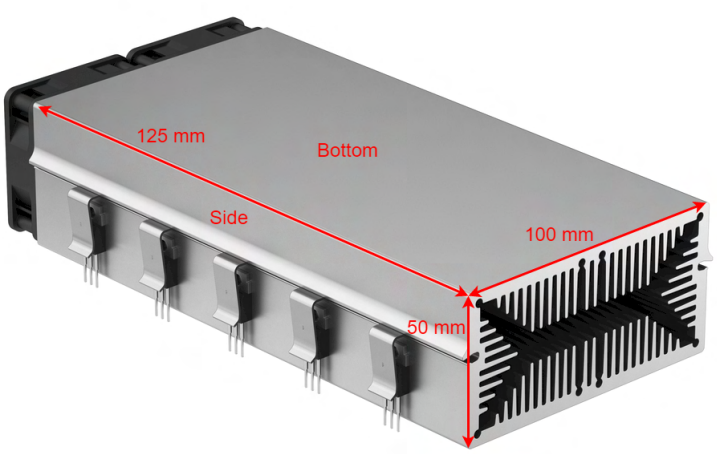


Figure 3.3: Heatsink used for the DAB converter with dimensions [4]

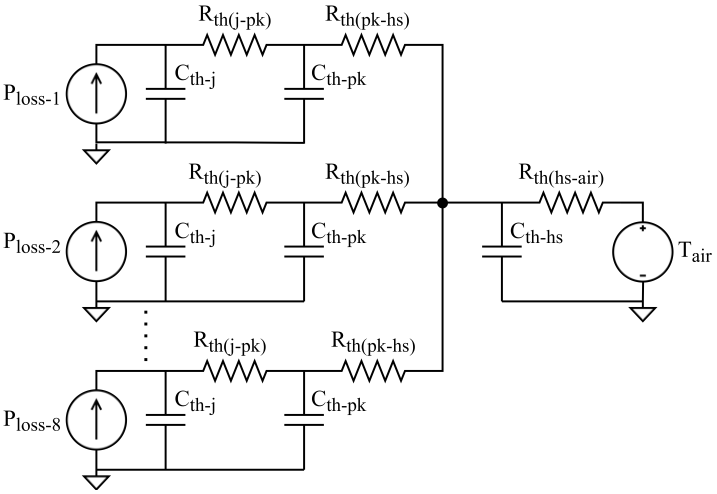


Figure 3.4: Thermal model of the MOSFET and heatsink

75 mm long, 4 mm thick and 100 mm ($\frac{2}{3} * 150$) wide. The resulting thermal resistance, assuming a thermal conductivity of $C_{alu} = 207\ W/m$, is then $R_{ab} = 0.905\ \frac{^\circ C}{W}$.

For the elements on opposing sides heat can be transferred over the bottom and the top of the heatsink, effectively doubling the thickness of the metal sheet. The length used to calculate the thermal resistance is now 150 mm, and the width only 62.5 mm. The resulting thermal resistance is equal to $R_{12} = 1.4493\ \frac{^\circ C}{W}$.

To verify the accuracy of the proposed model a more accurate lumped element model consisting of 30 elements has been constructed. Each element on the sides is 50 by 25 mm, of which there are 10. 8 of these side elements have a MOSFET connected to them. The remaining 20 elements are located at the top/bottom of the heatsink, and have a size of 25 by 25 mm. The top and bottom of the heatsink are considered in the same elements because of symmetry. The

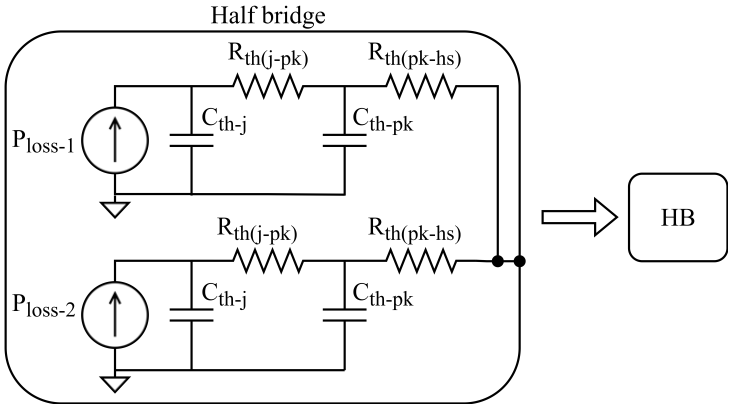


Figure 3.5: Thermal model of an ideal half-bridge

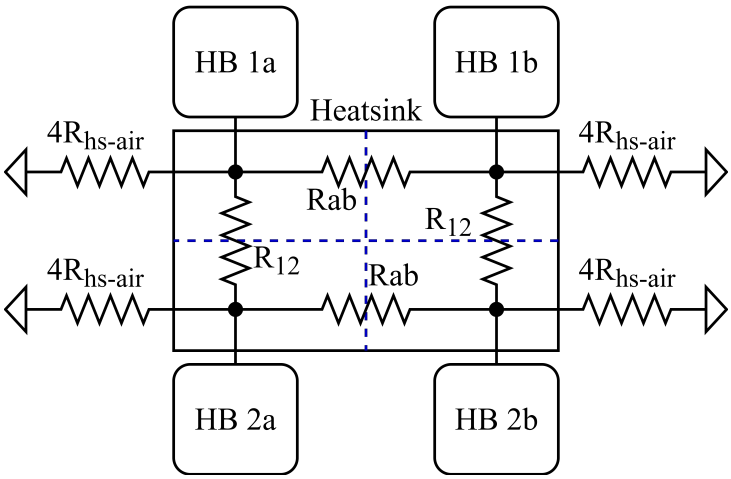


Figure 3.6: More advanced thermal model of the heatsink

half bridges are connected to the 4 side elements. Any further details are deemed unnecessary for confirming heatsink operation.

The maximum and minimum temperatures found in the proposed model are very similar to those of the lumped element model. The temperatures under unbalanced losses are shown in table 3.1. For the lumped model two temperatures are listed, for both MOSFETs in the half bridge. In all models an individual MOSFET junction to heatsink thermal resistance of 0.49 is present.

Since the proposed four element model is much simpler to implement in simulink, while still providing reasonably accurate results, it is used over the mode advanced lumped element model.

half bridge	1_a	1_b	2_a	2_b
Losses per MOSFET	10 W	20 W	30 W	40 W
Tj_{ideal}	$101.9°C$	$106.8°C$	$111.7°C$	$116.6°C$
Tj_{prop}	90.2	$104.7°C$	$113.8°C$	$128.3°C$
Tj_{lumped}	$89.5 - -90.5°C$	$105.6 - -105.9°C$	$110.9 - -114.59°C$	$126.4 - -130.6°C$

Table 3.1: Comparison of themral models

3.2 Controller

The controller is responsible for generating the PWM signals used to control each MOSFET. It does so by controlling the phase shift of each half bridge in the converter. In addition to this, it also needs to implement dead-time, which can vary with operating mode, operating voltage and the turns ratio of the transformer.

3.2.1 Duty cycle & offset calculation

An essential part of the controller is the generation of the effective duty cycles for each H-bridge. The effective duty cycle can be manipulated by changing the phase shift between the two half bridges in an H-bridge, where a phase shift of π results in a duty cycle of 1, and a phase shift of 0 in a duty cycle of 0. The relation between the internal phase shift and the duty cycle is linear, allowing for an easy conversion from duty cycle to internal phase shift.

The duty cycles are calculated using the equations derived in chapter 2 using a "function block" in simulink, which executes matlab code as part of the simulation. The function used to calculate the duty cycle checks whether the voltage gain k is bigger or smaller than 1, and which operating mode the system is in at a given phase shift Φ between the two H-bridges. It then applies the relevant equations for the duty cycles of both H-bridges as defined in chapter 2. It should be noted that these equations are modified to deal with the non-ideal behaviour of the converter, which is discussed in later in this section.

Based on the resulting duty cycles D_1 and D_2, and the phase shift Φ, a second function block will calculate the phase offset that that is required for the leakage inductor current to start at 0 each switching cycle. The implementation is done in a similar way to the calculation of D_1 and D_2. First D_1, D_2 and Φ are used to determine the operating mode of the converter, after which the phase offset equations introduced chapter 2 are applied for the current operating mode of the converter.

3.2.2 PWM generation

The C2000 series microcontrollers by Texas instruments have built-in ePWM modules. These modules are capable of up,down or up-down counting, and can be given an offset to implement a phase shift. This offset is applied when the ePWM module receives a synchronization signal, which can come from various sources. The Duty cycle of each PWM module will be a constant 50%.

To keep the PWM generation in the simulation similar to that in the microcontroller, a counter based system will be used to generate the PWM. The easiest way to implement this in simulink is by using an up counter that resets to a phase value when it receives a synchronization signal, using a "greater than or equal to" logic block to generate the output. The deadtime in the ePWM modules will be supplied by external input, and will be implemented as a variable turn-on delay on each PWM output.

Due to hardware constraints, the PWM implementation on the microcontroller is more complicated than what is used for the simulation. The microcontroller PWM implementation can be found in chapter 4.

3.2.3 Dead-time Calculation

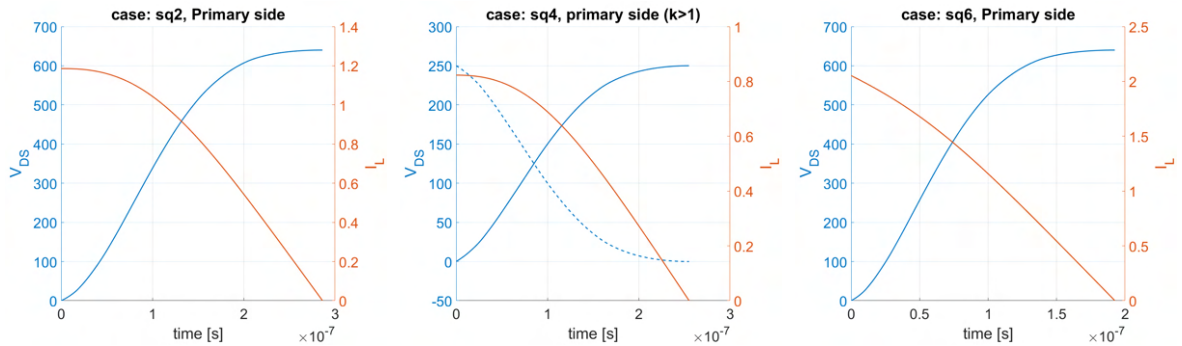
In the simulation a certain amount of time is required for the switch voltage to change as a result of the inductor current. In an ideal system the dead-time can be calculated as a function

of the capacitance and inductance, however the non-linear behaviour of the junction capacitance prevents this from being a valid option. The effect of the non-switching H-bridge can also be taken into account, although this would greatly increase complexity.

A more realistic approach to get the dead-time is through simulation of each of the worst case switching events. The resulting dead-time, which varies with switching voltage and side of the transformer switching occurs on, can be stored in a lookup table. The dead-time simulation includes three worst case scenarios, which can be applied to both sides of the transformer. The first case (SQ2) considers a single half-bridge switching, and will have the non-switching H-bridge apply 0 V to the inductor. This occurs in mode 1 TPS during t_0 and t_3 as shown in figure 2.9. The second case (SQ6) which also considers a single half-bridge switching, has the non-switching H-bridge apply a voltage of opposing polarity compared to the ΔV of the switching H-bridge, this occurs at t_0 in figure 2.8a. Finally the SQ4 case refers to a case with both half-bridges switching at the same time, where similarly to the SQ6 case the non-switching H-bridge opposes ZVS, this occurs at t_1 in figure 2.8b. The labels applied to these events are based on the factors in the square root term of the worst case minimum ZVS current for these events.

A simple code based simulation of a resonant LC system is used to obtain the dead-time, where the ΔI_L and ΔV_C are calculated stepwise manner based on the V_C and I_L of the previous step. Once I_L reaches 0, or V_C reaches the switching voltage, the simulation is stopped. The dead-time is then found by taking the maximum value of the time vector of the simulation. Figure 3.7 shows the switching waveforms of the primary side H-bridge under worst case conditions. The process of acquiring the dead-time is repeated over the voltage range of the converter, which allows it to be used in the simulation through a lookup table.

In the case where a reduction in dead-time is desired, it is possible to increase the current for the ZVS requirement. However this comes at the cost of increased rms current and reduced ZVS range. At the current switching frequency of 25 kHz this is not necessary, however at increased switching frequency where dead-time will take up a larger part of the switching period this option can be considered.



(a) (b) (c)

Figure 3.7: Switching waveforms for the dead-time calculations of the SQ2, SQ4 and SQ6 cases, of the primary H-bridge

Which case of dead-time should be applied depends on the operating mode of the converter. In the triangular region case SQ2 applies to all switching events, this is not the case in the transition and EPS region. In both the transition and EPS region the H-bridge the SQ4 case applies to the H-bridge with a duty cycle of 1. In the transition region the SQ2 case applies to the other H-bridge, while in EPS the SQ2 and SQ6 cases apply to individual half bridges in the

other H-bridge.

Given that each half-bridge is controlled by its own ePWM module, which has a separate dead-time input, the implementation of varying dead-time between different half-bridges is not problematic.

3.2.4 Outer Controller

Although modulation has already been discussed, the control itself has not. The outer control loop does not affect the efficiency of the converter directly, but it is required to manage the flow of power of the converter. For EV battery charging, either the DC battery current or the converter power can be controlled.

Controlling the battery current directly can be a desirable property, since it can be used as a form of battery protection. However it not expected to be necessary as the thermal capacity of the battery and ripple filter components should be capable of handling current overshoot that would occur during a transient in the output power of the converter.

Two methods for direct converter power control are considered:

- Measure the filter inductor current, and the dv/dt to get the exact converter power, which can be controlled using a PI controller that manipulates Φ. This includes a 2D lookup table containing the maximum Φ over the voltage range to maintain the power limit of the converter. This uses a fairly small amount of memory. This can also be done using the calculated power, although this requires more computational resources.
- Use a 3D lookup table to store the Φ needed to approximately obtain a certain power at a certain input and output voltage. The needed memory space varies with resolution, but it is expected to require a lot of memory as resolution is important.

Two indirect control methods are proposed:

- Use a cascaded control loop with Φ as the main control variable, used in a control loop with the capacitor voltage, which is in turn controlled as part of the inductor current control loop. Although the implementation needs very little memory, tuning will be rather difficult as the DAB converter is non-linear, and the sampling rate is low.
- Use a cascaded control loop, with a power lookup table to remove the non-linearity in $P(\Phi)$. Still has the same bandwidth issues. This could potentially be used with some form of predictive control on the capacitor voltage, which can increase the effective bandwidth. This option can use a current estimate based on the output capacitor dv/dt and the converter power in the lookup table, although a sensor is preferred.

Although the PCB design does have current sensors, they are not connected to the DC bus, but to the transformer and external leakage inductance. Due to limitations in controller speed these cannot be used to measure power or output current. Thus limitation in hardware exclude any options using a current sensor.

Given it's simple and sensor-less implementation, the power control at the converter using a lookup table is chosen for implementation. To generate a the required lookup table, first a lookup table containing the power at a given value of Φ, V_{in} and V_{out} is created in matlab. This is done with a very high resolution for Φ. For each combination of input and output voltage, the power vs Φ curve is sampled at fixed power values using the 1D interpolation function in matlab. These values of Φ are then stored in a 3D matrix used in the lookup table to determine Φ based on the converter power reference, the primary DC voltage and the secondary DC voltage. As

the resolution for the initial vector containing Φ is very high, the lookup table is expected to be accurate. It should be noted that high accuracy in the power lookup table is not required, as D_1 and D_2 are calculated using ZVS equations based on Φ.

In the practical implementation, the values of Φ in the table are multiplied by a factor 20000, and stored using the int16 datatype to reduce the amount of memory needed compared to storing the values as doubles.

3.3 Non-ideal converter behaviour

In the Analysis the ZVS conditions have been analysed under ideal circumstances, however in the simulation there are some causes of non-ideal behaviour. This section will analyse some of the sources of this non-ideal behaviour, and whether they provide a problem with the ZVS requirements. In the case where the non-ideal behaviour compromises the ZVS requirements, adjustments can be made to compensate for the non-ideal behaviour. Four main sources of non-ideal behaviour will be considered, which are listed below:

- Junction capacitor non-linearity
- Magnetizing current
- MOSFET on-resistance and transformer series resistance
- Dead-time & switch capacitance

3.3.1 Junction capacitor non-linearity

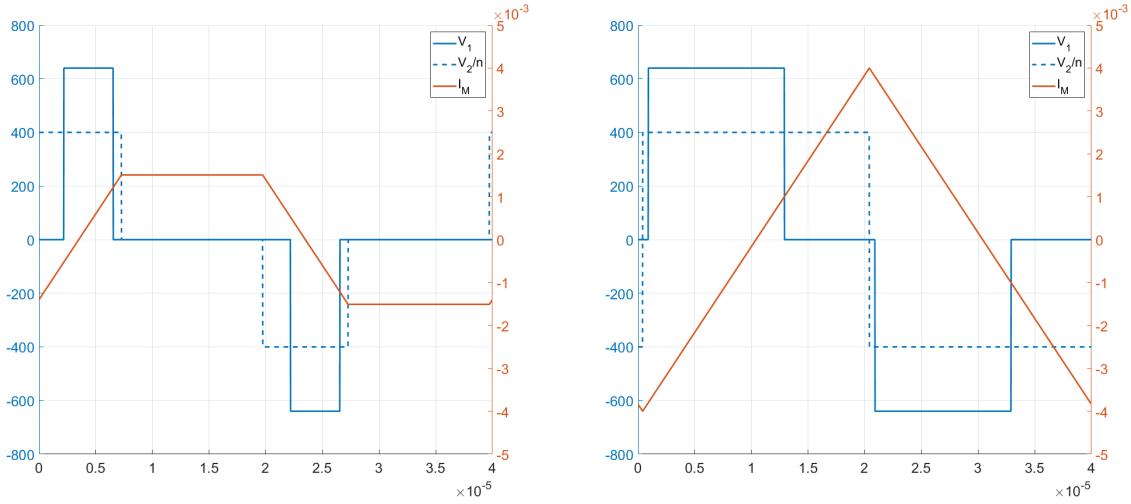
Unlike the ideal capacitor used in the calculations in chapter 2, the output capacitance of a MOSFET is non-linear. As observed from the data-sheets of various MOSFETs, the junction capacitance is typically larger at low drain-source voltage. As each half-bridge has two MOSFETs, the capacitance will be the the sum of that from both MOSFETs. During the dead-time of a half-bridge, when the voltage changes, this results in a varying capacitance. The non-linear behaviour means that the typical equation for capacitor energy, $E = 0.5CV^2$, does not work anymore. As this equation is the core of the ZVS requirements used in the calculation of D_1 and D_2, a solution must be found.

To resolve this, the capacitor energy of the non-linear half-bridge capacitance is calculated through discrete integration, this is done at various voltage levels. An equivalent energy linear capacitance is then calculated as $C = \frac{2E}{V^2}$. As the capacitance is under a square-root term in the ZVS equations, instead of storing the capacitance directly, the $\sqrt{C}$ term will be stored in a lookup table as an input for the function to calculate D_1 and D_2. This avoids having to calculate the square-root each switching cycle, saving computational effort.

3.3.2 Magnetizing current

In the proposed control system, the each switching period the current starts and ends at 0. Although this works for the leakage inductance current, it does not work for the magnetizing current. Figure 3.8 shows the magnetizing current a low and a higher power operating point. Here it can be observed that the initial magnetizing current at higher power of approximately -3.75 mA, while at lower power it is approximately -1.5 mA. If a transition between these two operating points were to occurs, a magnetizing current offset of approximately 2.25 mA would occur.

In the case of a startup event, where the magnetizing current is zero initially, this offset could even increase to 3.75 mA. The magnitude of the offset increases with increasing converter output voltage.



(a) $P_{ref} = -500\ W$, $L_M = 10.6mH$ (b) $P_{ref} = 5000\ W$ $L_M = 10.6mH$

Figure 3.8: Voltage and current waveforms in the triangular region

As shown in [22] and [13], magnetizing current can be used to extend the ZVS range. However this only applies to the AC part of the magnetizing current, a DC offset in the magnetizing current can hinder ZVS operation for half of the switching events.

To maintain Proper ZVS switching, this offset should be compensated. The maximum offset will be considered equal to the peak magnetizing current under worst case conditions at the measured voltage. This assumption is made as it is expected that the converter will operate at a fairly constant voltage, with significant variation in Φ, D_1 and D_2 remaining a possibility. Considering that the transformer is placed on the secondary side of the leakage inductor, it is assumed only the secondary side voltage affects the magnetizing current. Assuming worst case conditions, D_2 is set equal to 1, resulting in the peak magnetizing current shown in equation 3.4. The magnetizing current is calculated as if the magnetizing inductor is placed at the primary side of an ideal transformer, as shown in figure 3.1.

$$I_{m-peak} = \frac{TsV_2}{4nL_m}; \tag{3.4}$$

This equation does not consider that at a high output voltage, D_2 might not be equal to 1 at 11 kW. This is done intentionally as D_2 in the higher part of output voltage range depends on a large variety of factors, including the magnetizing current compensation itself. Since the increase in complexity is significant, and it's effect on the converters efficiency is expected to be negligible, the variability of D_2 is not considered.

The magnetizing current compensation is implemented by adding the calculated offset current to all ZVS requirements that apply to the secondary H-bridge.

3.3.3 MOSFET and transformer resistance

The resistance of the MOSFET and transformer have a small effect on the current, as the voltage second area over these resistances causes the inductor current to change slightly. This only affects the triangular and transition operating regions and its boundaries, where there is very little margin for the ZVS conditions. Operating points in the EPS region are calculated using linear extrapolation between the point [$\Phi = 0.5$, $D_1 = D_2 = 1$], and its boundary with the transition region. As all boundaries and operating points that depend on ZVS requirements

for their calculation are located in or at the boundary of mode 1 TPS, the EPS region does not have to be considered for the series resistance offset compensation.

To simplify the calculation of the offset, an approximation of the worst case scenario will be used. The worst case operating condition is considered the maximum power in the mode 1 TPS region, which occurs at the boundary between the transition and EPS region. As this boundary operating point is dependent on the series resistance offset, it would make the equations to calculate this compensation complicated. To simplify it, instead the maximum power of ideal triangular modulation is used, which will have a similar current waveform. This greatly simplifies the calculation of the offset compensation.

At the upper boundary of the power for ideal triangular modulation, the average current during a half period equals $\frac{V_2 T_s}{4L_s}(1-k)$ or $\frac{V_1 T_s}{4L_s}(1-k^{-1})$ depending on whether $k<1$ or $k>1$. When multiplied by the total series resistance $R_{eq} = (2+\frac{2}{n^2})R_{on} + R_{s1} + R_{s2}$, the average voltage is obtained as shown in equation 3.5 assuming $k<1$. Equation 3.6 shows the average voltage when $k>1$.

$$Vr_{av} = ((2+\frac{2}{n^2})R_{on} + R_{s1} + R_{s2})\frac{V_2 T_s(1-k)}{4L_s} \tag{3.5}$$

$$Vr_{av} = ((2+\frac{2}{n^2})R_{on} + R_{s1} + R_{s2})\frac{V_1 T_s(1-k^{-1})}{4Ls} \tag{3.6}$$

The average voltage can then be multiplied by $\frac{T_s}{2L_s}$ to obtain the ΔI. The resulting peak offset is then equal to $\frac{\Delta I}{2}$, as shown in equation 3.7 and 3.8 for $k<1$ and $k>1$.

$$I_{Loff} = ((2+\frac{2}{n^2})R_{on} + R_{s1} + R_{s2})\frac{V_2 T_s^2(1-k)}{16L_s^2} \tag{3.7}$$

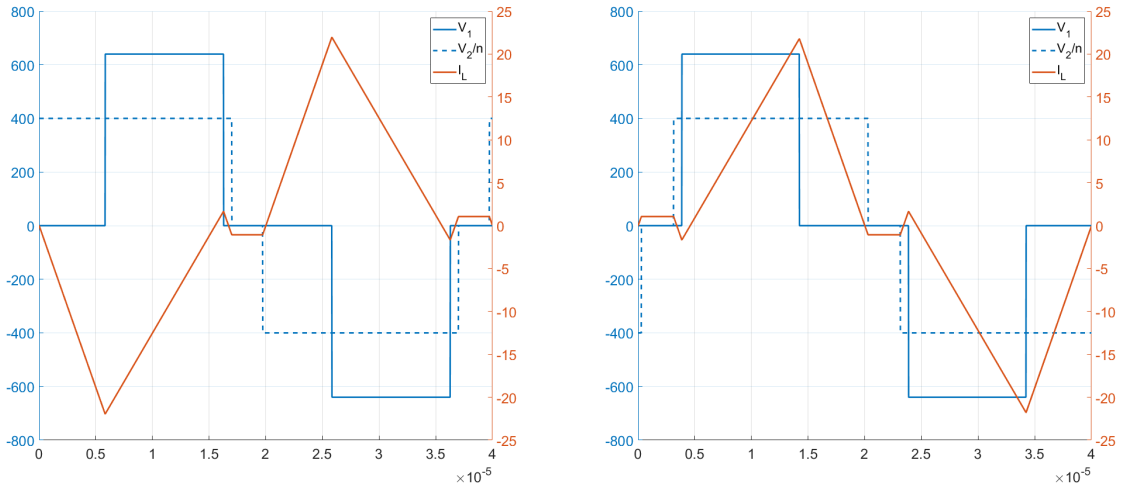
$$I_{Loff} = ((2+\frac{2}{n^2})R_{on} + R_{s1} + R_{s2})\frac{V_1 T_s^2(1-k^{-1})}{16Ls^2} \tag{3.8}$$

The simplest compensation method would be by adding a fixed current value to the ZVS requirements, similar to what is done to compensate for the magnetizing current offset. However as this error has a polarity, Compensation can be applied taking the polarity into account.

The polarity of the error depends on the polarity of the current, and the polarity of the ΔV. In or at the boundary of mode 1 TPS, where all the relevant operating mode boundaries are located, the polarity of the average current is mainly affected by the polarity Φ. A positive Φ will result in a positive current during the positive voltage half cycle, as shown in figure 3.9b. In the meantime a negative value of Φ will result in a negative current during the the positive voltage half cycle shown in figure 3.9a. This difference in the polarity of the average current will also result in a different polarity of the voltage error. k affects where the compensation is applied, however it does so not by changing the polarity, but by changing the order of switching events and as a result the ZVS equations. For example when $k<1$, and $\Phi>0$, the offset increases the switching current for the secondary H-bridge, and decreases it for the primary H-bridge. In this situation only the ZVS requirement for the primary H-bridge requires compensation. This compensation is applied in the equation for D_1, the equation for D_2 depends on D_1, and will thus also be modified. Table 3.2 shows an overview of where the compensation is required for each of the operating regions and modes.

3.3.4 Switch capacitance & dead-time

Although the switch capacitance does not directly cause any non-ideal behaviour when hard switching is used, the fairly long dead-time needed to achieve ZVS does. Depending on the current at the moment of switching, the time needed to charge or discharge the switch capacitance may vary. This can change the effective duty cycle, or the phase shift depending on the



(a) $P_{ref} = -3500\ W$ (b) $P_{ref} = 3500\ W$

Figure 3.9: Voltage and current waveforms in the triangular region

k	Phi	Mode 1 TPS	EPS
< 1	> 0	$D_1(\Phi)$	-
< 1	< 0	$D_2(D_1)$	$\Phi_{EPS-lim}$
> 1	> 0	$D_1(D_2)$	$\Phi_{EPS-lim}$
> 1	< 0	$D_2(\Phi)$	-

Table 3.2: Overview of the control variables which require compensation under various operating conditions

operating mode. The change to the phase shift or duty cycle can in turn negatively affect the ZVS behaviour.

When operating in the higher ends of the EPS region this is not problematic, since switching current exceeds the ZVS current in this region. In the triangular and transition region, switching events happen at the ZVS current limit, so small deviations can disrupt ZVS operation.

In the triangular region a disruption is caused by the half bridge switching at the peak current of the triangular waveform, which has a shorter effective dead-time. Depending on the polarity of the phase shift this can either increase or decrease the effective duty cycle of the higher voltage H-bridge. When entering the transition region, the dead-time effect of the non-ZVS switching event will be added to this. Similar to the resistance issue, this can be solved by implementing a phase shift dependent offset, corresponding to the length of the dead-time to the modulation function. This offset is equal to the dead-time of the H-bridge with the higher voltage, and is applied in the same equations as the resistance offset, as shown in table 3.2

Problems also occurred in the triangular region with the dead-time of the lower voltage side switches. A non ZVS switching event can cause an increase in the effective $|\Phi|$, which results in the higher voltage side ZVS condition, which is a function of $|\Phi|$ not being met. These are addressed by adding a compensation term to Φ in the ZVS equations, again dependent on the polarity of Φ.

These errors are also present at the boundary between the mode 2 EPS and transition regions. The ZVS equations at this boundary are also compensated using the same methods.

3.4 Modified control function

The generation of the primary and secondary side duty cycle D_1 and D_2 is still primarily based on the ZVS boundary equations presented in chapter 2 for each of the operating modes. However, in addition to the ZVS current requirements, current offsets are added to the ZVS requirements for the magnetizing current offset and resistor current offset compensation. The dead-time compensation is applied directly to the duty cycle equations. This section will discuss the modified control equations and the functionality of the control function.

It should be noted that some of the places where dead-time is compensated are not based on observed non ZVS events in the simulation, but on practical testing. These include the compensation added to Φ in triangular mode and the compensation added to the Φ_{EPS} to address observed non-ZVS switching events.

Initially the control function defines a few basic variables, as shown in the code below. Among these are the voltage gain k noted as kg in code, selection variables (a_1,a_2) used to apply the resistance and dead-time compensation only for the correct polarity of Φ, the absolute value of the phase shift, and the ratio between the leakage and magnetizing inductance. The dead-time relative to half the switching period is stored in the vector shown in equation 3.9 for the SQ2 and SQ6 and SQ4 switching events for both the primary and secondary sides.

$$dt = \frac{2}{Ts}[dt_{2-prim}\ dt_{2-sec}\ dt_{6-prim}\ dt_{6-sec}\ dt_{4-prim}\ dt_{4-sec}] \tag{3.9}$$

```
kg = V2/(V1*Nr);
if Phi>=0
        a1 = 1;
        a2 = 0;
else
        a1 = 0;
        a2 = 1;
end
Phi = abs(Phi);
mi = Ls/Lm;
```

It then checks the voltage gain k, which is crucial to determining D_1 and D_2. At this point the boundaries of the operating modes will be defined. In the case where $k < 1$ these boundaries are shown in equation 3.10, 3.11, 3.12 and 3.13. $C_{j-1/2}$ in these equations is variable, based on the previously discussed lookup table containing the square root of the effective capacitance.

$$\Phi_{EPS} = 0.5 - 0.5k + \frac{2L_s n}{T_s}\sqrt{\frac{4C_{j2}}{L_s}} + m_i k + a_2\frac{2L_s}{V_{in}T_s}I_{Loff} + a_2 dt(6) \tag{3.10}$$

$$D_{1-EPS} = 1 - 2\Phi_{EPS} - a_2(dt(1) + dt(3)) \tag{3.11}$$

$$\begin{aligned}\Phi_{TRG} = 0.5 - 0.5k - \frac{2L_s}{T_s}(k^{-1}\sqrt{\frac{2C_{j1}}{L_s}} + n(1-k)\sqrt{\frac{2C_{j2}}{L_s}} + \frac{I_{Loff}}{V_{in}}(a_2(1-k) + a_1 k^{-1})) \\ -(0.5 - 0.5k)(m_i + (a_1 + 2a_2)dt(1)k^{-1}) - a_2 dt(2)\end{aligned} \tag{3.12}$$

Based on these equations, it can be determined whether the system operates in triangular region, the transition region, or the in the EPS region. In the EPS and transition region, D_1 and D_2 are obtained using linear extrapolation between the boundary points. In the triangular region equation 3.13 and 3.14 are used to calculate D_1 and D_2.

$$D_{1-TRG} = \frac{2k(\Phi + a_2 dt(2))}{1-k} + \frac{4L_s}{T_s(1-k)}(\sqrt{\frac{2C_{j1}}{L_s}} + a_1\frac{I_{Loff}}{V_{in}}) + a_1 dt(1); \tag{3.13}$$

$$D_{2-TRG} = \frac{D_{1-TRG}}{k} + \frac{4L_s}{T_s}(n\sqrt{\frac{2C_{j2}}{L_s}} + a_2\frac{I_{Loff}}{V_{in}}) + m_i + 2a_2\frac{dt(1)}{k} \tag{3.14}$$

The control equations are also recalculated for the case $k > 1$. The boundary equations for this case are shown in 3.15, 3.16, 3.17. It can be observed that the compensation related terms are placed differently compared to the case of $k < 1$, as the circumstances in which they apply differ.

$$\Phi_{EPS} = 0.5 - 0.5k^{-1} + \frac{2L_s}{T_s}\sqrt{\frac{4C_{j1}}{L_s}} + a_1\frac{2nL_s}{V_{out}T_s}I_{Loff} + a_1 dt(5) \tag{3.15}$$

$$D_{1-EPS} = 1 - 2\Phi_{EPS} - a_1(dt(2) + dt(4)) \tag{3.16}$$

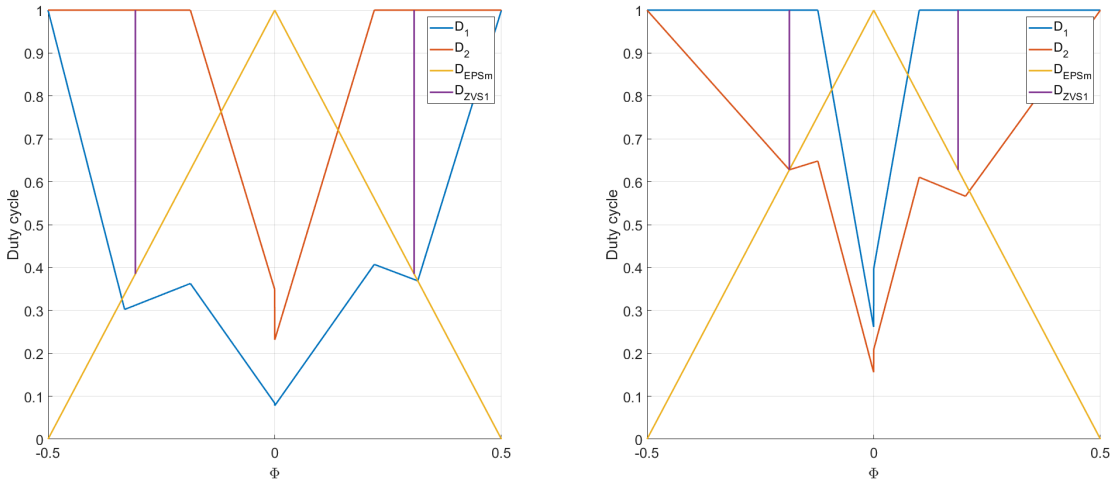
$$\begin{aligned}\Phi_{TRG} = 0.5 - 0.5k^{-1} - \frac{2L_s}{T_s}(nk\sqrt{\frac{2C_{j2}}{L_s}} + (1-k^{-1})\sqrt{\frac{2C_{j1}}{L_s}} \\ + \frac{nI_{Loff}}{V_{out}}(a_1(1-k^{-1}) + a_2k)) - (2a_1 + a_2)dt(2)k(0.5 - 0.5k^{-1}) - 0.5m_ik - a1 * dt(1)\end{aligned} \tag{3.17}$$

The equations describing D_1 and D_2 for triangular modulation are then shown in equation 3.13 and 3.14.

$$D_{2-TRG} = \frac{2k^{-1}(\Phi + a_1dt(1))}{1-k^{-1}} + \frac{4L_s}{T_s(1-k)}(n\sqrt{\frac{2C_{j2}}{L_s}} + a_2\frac{nI_{Loff}}{V_{out}}) + a_2dt(2) + \frac{m_i}{1-k^{-1}} \tag{3.18}$$

$$D_{1-TRG} = \frac{D_{2-TRG}}{k^{-1}} + \frac{4L_s}{T_s}(\sqrt{\frac{2C_{j1}}{L_s}} + a_1\frac{nI_{Loff}}{V_{out}}) + 2a_1\frac{dt(2)}{k^{-1}} \tag{3.19}$$

Based on these equations, the control law can be constructed for use in the microcontroller. Figure 3.10 shows the resulting control law when using the "G3R20MT12K" silicon carbide MOSFET for all switches. It also includes the boundary of mode 2 EPS (D_{EPS}). It can be observed that the duty cycle waveforms are not symmetrical, which is expected as the compensations are also non-symmetrical in nature.



(a) Case: $V_{in} = 640$, $V_{out} = 250$, n = 0.875

(b) Case: $V_{in} = 640$, $V_{out} = 840$, n = 0.875

Figure 3.10: Duty cycle waveforms for $k < 1$ and $k > 1$ including the compensation of non-ideal behaviour.

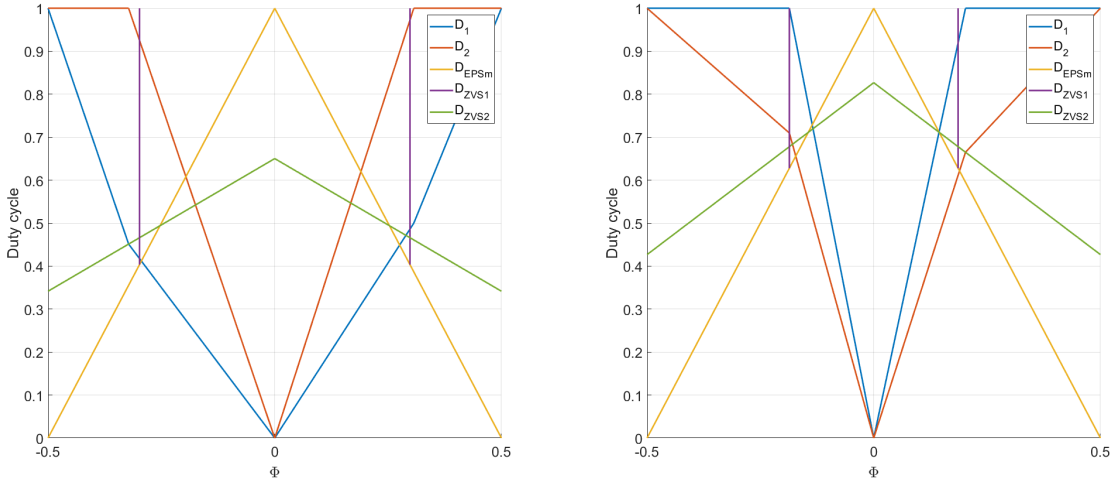
3.4.1 Variable frequency control modifications

Similar to the fixed frequency modulation method, the variable frequency method also requires some modifications to ensure ZVS. The modifications to the Φ_{EPS} boundary are exactly the same as the boundaries shown in equation 3.10 and 3.15 for the fixed frequency modulation method.

The modifications on the second ZVS boundary are shown in equation 3.20 and 3.21. Figure 3.11 shows the Duty cycle plot of the variable frequency modulation.

$$D_{1-EPS} > \frac{k(2-2\Phi_{EPS}) + \frac{4L}{T_s}\sqrt{\frac{6C_{j1}}{L}} + a_1\frac{I_{Loff}}{V_{in}}}{1+k} + a_1(dt(1)+dt(3)) \tag{3.20}$$

$$D_{2-EPS} > \frac{k^{-1}(2-2\Phi_{EPS}) + \frac{4nL}{T_s}\sqrt{\frac{6C_{j2}}{L}} + a_2\frac{nI_{Loff}}{V_{out}}}{1+k^{-1}} + a_2(dt(2)+dt(4)) \tag{3.21}$$



(a) Case: $V_{in} = 640$, $V_{out} = 250$, n = 0.875

(b) Case: $V_{in} = 640$, $V_{out} = 840$, n = 0.875

Figure 3.11: Duty cycle waveforms for $k < 1$ and $k > 1$ including the compensation of non-ideal behaviour.

3.5 Simulation results

When considering the control system, its basic behaviour like the voltage and current waveforms can easily be checked using the current equations and a simple ideal DAB model. More complex behaviour like the converter non-idealities and transient behaviour cannot be checked through those means, and must instead be done in the simulation. This section discusses the transient DC offset compensation system and the performance of the non-ideal behaviour compensation.

3.5.1 Transient behaviour

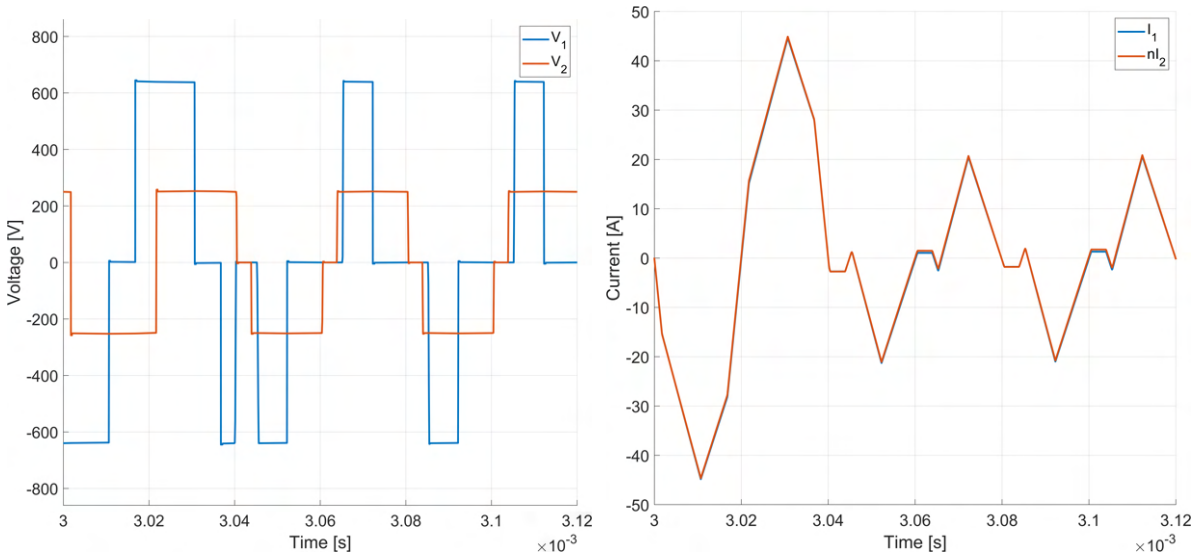
In chapter 2, a system to reduce transient DC offset by starting each switching cycle at a current of 0 A was introduced. The current starting at 0 A each switching period regardless of operating mode has been verified based on an ideal theoretical model considering only the input and output voltages, the control parameters, and the inductor. However its general behaviour should also be observed in a non-ideal model like the simulation. To observe the performance of the system, a step change in phase shift is applied. This step change will go from the EPS

region with positive Φ, to the triangular region with both positive and negative Φ. The voltage and current waveforms around this transient are shown in figure 3.12 and 3.13.

When observing the current directly after the change in power reference at $Time = 3.04\ ms$, in both cases a small negative DC offset can be found in the current. In the first case in figure 3.12, this offset is very small. In the second case in 3.13 the offset slightly larger. This difference in offset between the two cases is caused by the larger difference in initial state when a transition to negative power occurs. This results in different switching events which can affect the current through the dead-time.

It is likely that the series resistance offset also plays a role in this. The current in the half-cycle before the transient event is positive, and rather large in amplitude, which results in a negative series resistance offset. This offset, Just like the other non-ideal behaviour is not taken into account in the phase offset calculation discussed in chapter 2, which assumes an ideal converter.

It is deemed unnecessary to include the non-ideal behaviour in the phase offset calculation, as the error is fairly small and do not appear to last beyond the fist switching cycle after the transient. Compensating the non-ideal behaviour can also have disadvantages when the error is overcompensated, which would generate an error of opposite polarity. This is not an issue for the ZVS requirements, as being above the ZVS current limit does not affect the switching losses.



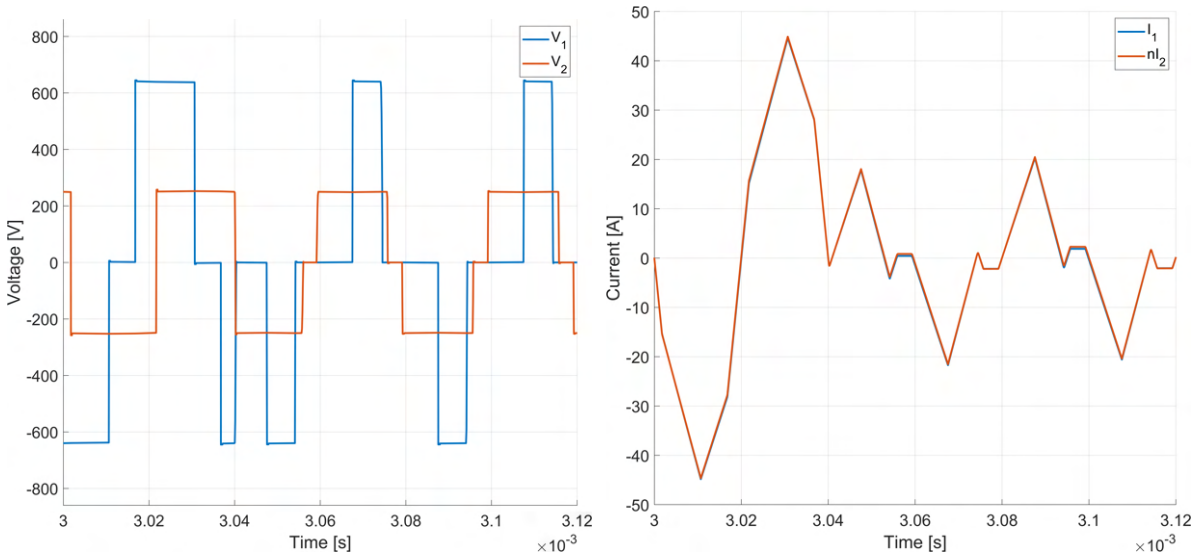
(a) (b)

Figure 3.12: Voltage and current waveforms for a transient from 10kW to 2kW

3.5.2 compensation effects

To verify the functionality of the compensation, a case where a ZVS condition is not met without compensation is considered. The waveforms under this condition will be compared with and without the compensation applied. A case close to the boundary of the triangular region is selected as it will provide a larger series resistance offset compared to a case with Φ close to 0.

Figure 3.14 shows the voltage and current waveforms with and without compensation when $V_{in} = 840\ V$ and $V_{out} = 250\ V$. It can be observed that when V_1 switches from a zero-voltage

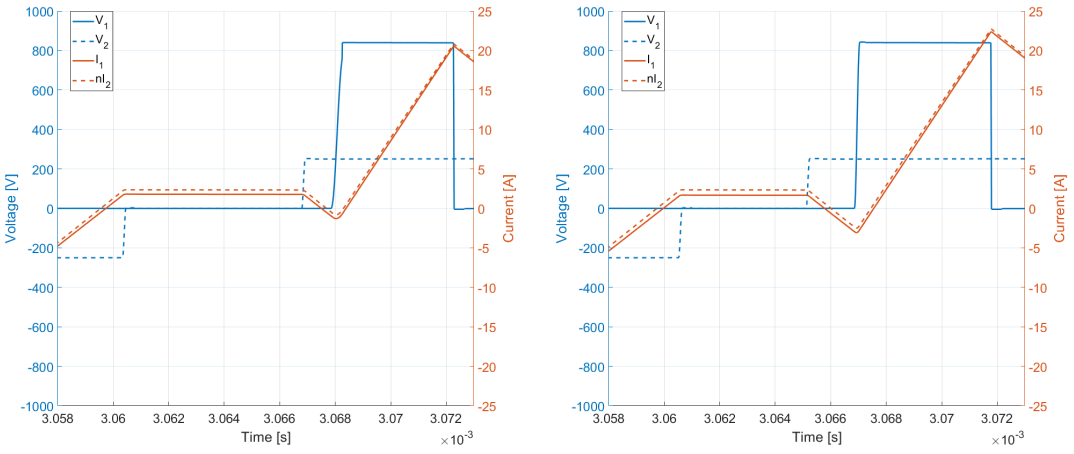


(a) (b)

Figure 3.13: Voltage and current waveforms for a transient from 10kW to -2kW

state to a $\pm V_{in}$ state, the turn-on occurs before the capacitors have been charged, indicating partial hard switching. This is caused by a combination of current offsets.

When comparing the current between the uncompensated and compensated cases, it can be observed that at the current at the non-ZVS switching event now has increased amplitude. This results in the switch capacitor being fully charged and starting to conduct through the diode, which is signified by the small increase in the voltage before the switch is turned on. This can be observed for the compensated case in 3.14, showing the functionality of the compensation. The current during the secondary side switching events remains mostly unchanged, as no compensation is needed for these switching events.



(a) Uncompensated (b) Compensated

Figure 3.14: Voltage and current waveforms without and with compensation for non-ideal behaviour

Chapter 4

Practical implementation

The practical implementation of the system can be split up in two parts, the implementation of the control system, and the implementation of the hardware.

The control system has to be implemented on a TI TMS320F28379D controlCARD, which will be done using the "C2000 Embedded Coder Support Package" Simulink. This simplifies the process of programming the controller significantly.

For the hardware of the system a pre-existing PCB design is used. The PCB is designed for operation up to 11 kW or a DC output current of 30 A. The intended usage of the PCB is over an input voltage range from 640 V to 840 V, and an output voltage range from 250 V to 1000 V. Figure 4.1 shows the assembled PCB. The PCB has isolated voltage measurement circuits on the primary and secondary side DC bus, which can be used for the controller. It also has hall effect current sensors on the primary and secondary side of the inductor and transformer connections, which are used for the overcurrent protection system implemented on the PCB.

As the PCB has already been designed, only the selection of the switches, and the design of the transformer and external leakage inductor have to be considered.

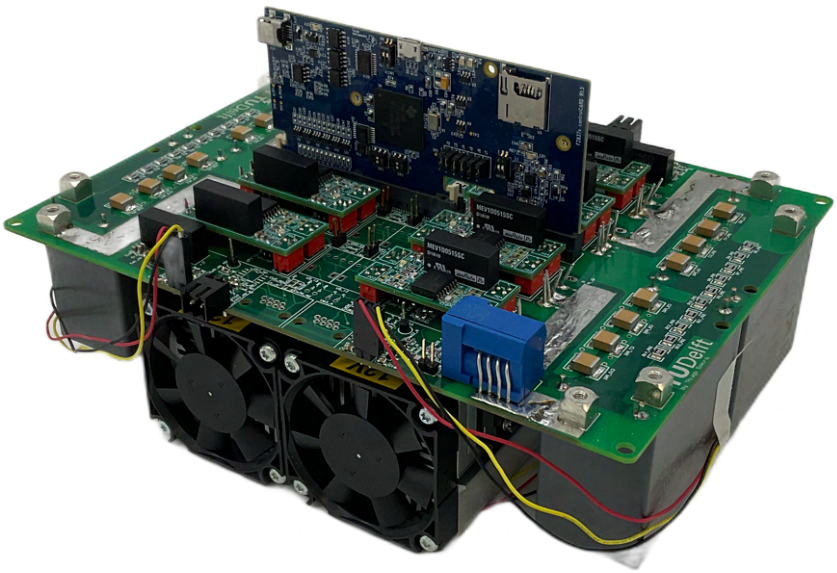


Figure 4.1: Assembled PCB of the DAB converter

4.1 Control system implementation

The control implementation on the TMS320F28379D is very similar to that of the simulation, using the same control equations and phase shift calculations and lookup tables. The main differences can be found in the implementation and synchronization of the PWM, and the interrupt structure of the controller, which was absent in the simulation. A digital PWM enable also needs to be implemented, as there is no hardware enable on the PCB, it is instead implemented through the trip-zone module of the controller. This section will discuss the practical implementation of these aspects of the controller.

4.1.1 System timer and interrupt routine

For the control system to work properly, it should perform its calculations periodically. To achieve this the start of a switching period is marked by a timer implemented on ePWM module 5, as the first four modules are reserved for the PWM outputs. Whenever the counter equals 0, an interrupt is generated which will trigger the ADC to take a primary side current measurement, after which voltage measurements are done sequentially on different channels of a single ADC. At the end of conversion of the last voltage measurement, an interrupt is generated to perform the control calculations. The control values are sent to the PWM registers, and implemented upon synchronization. Synchronization of the PWM modules is implemented based on ePWM module 5, which represents the system timer.

4.1.2 Enable implementation

To be able to shut down the converter through the controller dashboard, the control system needs to be able to shut down the PWM modules. This can be done through a software force input or the trip zone module. Using the trip zone module offers the advantage of not interfering with the PWM generation itself, as it is implemented after the PWM generation module. This is critical to achieve the correct initial state after the PWM is enabled.

The trip zone module is configured to work on a cycle by cycle basis. If the trip zone input becomes low, it will force the PWM outputs low immediately. If the input is changed to a high state, then the PWM outputs will be enabled during the next ZERO or PRD event of the PWM module. The trip zone signal is routed through a GPIO as it is not possible to control it by software in the embedded coder support package.

4.1.3 PWM implementation

The PWM implementation has to meet certain requirements to ensure proper behavior at all times. The requirements are listed below.

- Synchronization with the system timer
- A correct initial state after synchronization regardless of phase shift
- A constant 50% duty cycle
- A phase shift range from 0 to 2π.
- A ZERO or PRD event at the start of each period to reset the trip zone

The synchronization with the system timer is needed for the transient DC offset mitigation, which will apply an equal phase shift to each PWM module, thus preventing synchronization using ePWM module 1. The implementation of the synchronization can be done either through software synchronization of through an external GPIO, as it is not possible to synchronize

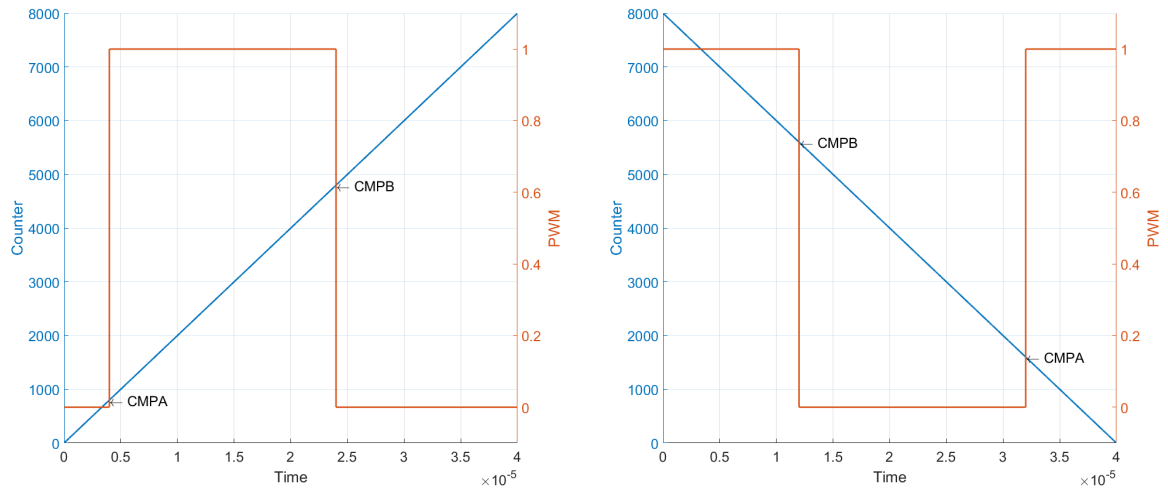
ePWM modules 1-4 with ePWM module 5 internally. Software synchronization has significant delays, making it unsuitable for this application. Because of this the only viable option is to have the system timer, ePWM module 5, output a pulse at the start of each period, which is in turn connected to the external synchronization of ePWM module 1, which passes it to ePWM module 2-4 through the synchronization daisy chain.

The PWM implementation is done through an up-down counter. Each period starts with the counter at ZERO or PRD, which is used to set the initial state, and reset the trip-zone module synchronously. The CMPA and CMPB compare events are set depending on phi to implement the phase shift. As CMPA and CMPB events are prioritized over the ZERO and PRD events, the PWM output will be correct even if a CMP and ZERO or PRD event occur at the same time. Table 4.1 shows an overview of the PWM compare values for different phase shift. Here θ_n is the phase shift normalized between 0 and 1.

	$0 <= \phi < \pi$	$\pi <= \phi < 2\pi$
PHS	ZERO	PRD
CMPA	$\theta_n PRD$	$PRD - \theta_n PRD$
CMPB	$\theta_n PRD + 0.5PRD$	$1.5PRD - \theta_n PRD$

Table 4.1: Values of the phase shift PHS, CMPA and CMPB

In figure 4.2 examples of the PWM generation for $\theta_n = 0.1$ and $\theta_n = 0.8$ are shown. It can be observed that the system works in up or down counting mode depending on the value of θ_n.



(a) (b)

Figure 4.2: Counter and PWM waveforms at PHS = 10% and PHS = 80%

4.2 Hardware considerations

There are three pieces of hardware that need to be designed or selected, the switching devices, the transformer, and the external leakage inductor. The first parameter to be addressed is the transformer turns ratio, which will influence the worst case RMS current and the size of the total leakage inductance. An estimate of the RMS current can then be used to make a selection of viable switching components which can be compared in more detail. A more detailed turns

ratio optimization for the turns ratio with the newly selected switch can then be performed. The resulting turns ratio, total leakage inductance and worst case current and voltage waveforms are then used to design the transformer and external leakage inductance.

4.2.1 Approximate turns ratio Optimization

To get an approximate value for the turns ratio, firstly an optimization that only considers conduction losses is considered, as conduction loss is expected to be the dominant loss in the switching components. This is done using equation 4.1, which shows the equivalent RMS current with an adjustment for the increase or decrease in secondary side current due to the turns ratio. Similar to the method presented in [2], the algorithm will cycle through various values for the turns ratio to find the turns ratio with the lowest average I_{rms-eq} over the input and output voltage range while operating at full power. Lower power is not considered as it is expected that the converter will operate at full power the majority of the time.

$$I_{rms-eq} = I_{rms-p}\sqrt{(0.5 + \frac{0.5}{n^2})}; \tag{4.1}$$

The optimization algorithm starts by determining the leakage inductance needed to achieve the maximum power under minimum voltage conditions, at the maximum value for $|\Phi|$. This is repeated for each turns ratio the algorithm loops through. The maximum value of $|\Phi|$ is based on figure 4.3, which shows the ratio between the power and RMS current at various output voltages. Above a certain $|\Phi|$, this ratio decreases. Since the maximum $|\Phi|$ only applies at the lowest input and output voltage, the maximum value of $|\Phi|$ is chosen around the peak of the curve for $V_{out} = 250V$. Further manual optimization resulted in a maximum phase shift value of $|\Phi| = 0.41$.

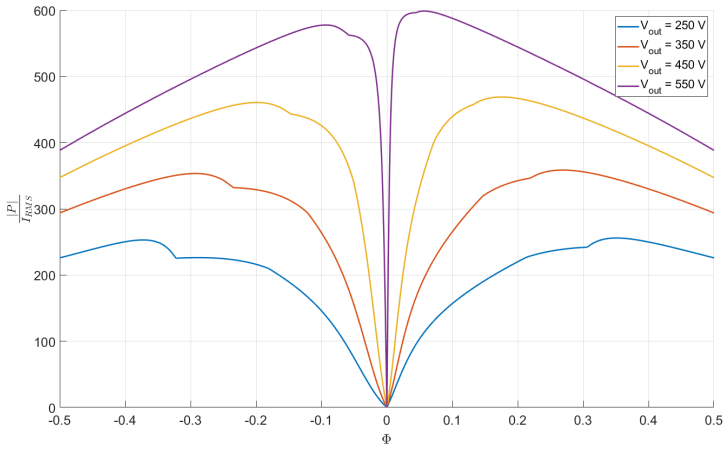


Figure 4.3: Ratio between the $|P|$ and I_{rms} at $V_{in} = 640\ V$, with n = 0.875

For the ZVS conditions, a fixed output capacitance of $C_j = 300\ pF$ will be used and the magnetizing inductance will be assumed infinite. The compensations added to the controller to address non-ideal converter behavior will not be included since no parts have been selected at this point.

By cycling through various values for the turns ratio in steps of 0.01, a minimum value of the averaged I_{rms-eq} is found at $n = 0.87$. This varies from the value of $n = 0.8333$ obtained in [2], since different modulation methods are used.

4.2.2 Transistor selection

As the transistors used in the DAB converter have to work up to 1000 V, either IGBT's or silicon carbide (SiC) MOSFETs can be used. Given the fairly high switching frequency of 25 kHz, and up to 66.7 kHz if the variable switching frequency implementation is considered, SiC mosfets are the better choice. SiC mosfets are capable of higher switching speeds and usually have lower switching loss and conduction losses compared to IGBT's. The main drawback of SiC MOSFETs is the price.

The MOSFET selection is done based on a maximum allowable value of R_{ds} of the MOSFET. At a turns ratio of $n = 0.87$, a worst case primary side RMS current of $I_{rms-p} = 30.51\ A$ is found at $V_{in} = 640\ V$ and $V_{out} = 355\ V$. The maximum junction temperature for the MOSFET is set to $125°C$. As switching losses are not considered here, conduction loss is only allowed to make up 67% of the total loss before this temperature is reached.

To get an estimate of the maximum junction temperature, it is assumed the heatsink has uniform temperature, with a junction to heatsink thermal resistance of $R_{j-hs} = 0.5°C/W$. The heatsink used is a "fisher elektronik LAM 5 D K 125 12", which has a thermal resistance to air of $R_{hs-a} = 0.37°C/W$. The resulting ΔT_j is shown in equation 4.2. Solving this equation for a ΔT_j, assuming an ambient temperature of $25°C/W$ leads to a maximum R_{ds} of $30m\Omega$.

$$\Delta T_j = R_{j-hs}(\frac{I_{rms-p}}{n})^2 R_{ds} + 2R_{hs-a}I_{rms-p}^2(1 + \frac{1}{n^2})R_{ds} \tag{4.2}$$

To be compatible with the PCB, the MOSFETs have to come in either a TO-247-3 or TO-247-4 package, and have to be compatible with a +15/-5V gate driver circuit. The voltage rating of the MOSFET is chosen to be 1200 V, as the availability of affordable 1700 V SiC MOSFETs with the correct package is poor. Assuming 20% derating this allows for safe testing up to 960 V, which is sufficient for testing the performance of the proposed modulation method. The R_{ds} limit is considered assuming a junction temperature of $125°C$, to prevent thermal runaway.

Among the selection of suitable MOSFETs are the G3R20MT12K, the UF3SC120016K3S and the C3M0021120K. All three MOSFETs have a comparable R_{ds} around 24 $m\Omega$ at a junction temperature of $125°C$. As the GeneSiC G3R20MT12K has the lowest output capacitance and switching loss among these, it is selected for this converter design.

4.2.3 Loss based optimization

To ensure the transformer turns ratio still minimzes the losses of the switching components when switching loss in included, the optimization will be repeated with the average converter losses over the entire voltage range as the outcome. Only full power operation is considered for this average, as this is expected to be the most likely operating condition in practice. It will also be used to check whether the junction temperatures will remain below the maximum value of $125°C$ with the inclusion of switching loss and the non-ideal heatsink model discussed in chapter 3.

The optimization follows the same steps as the approximate optimization, with some differences in the inputs. The modulation in the optimization now includes the non-linear capacitance specified by the datasheet of the G3R20MT12K, with deadtime adapted to this capacitance. Compensations for non-ideal behaviour are now also included.

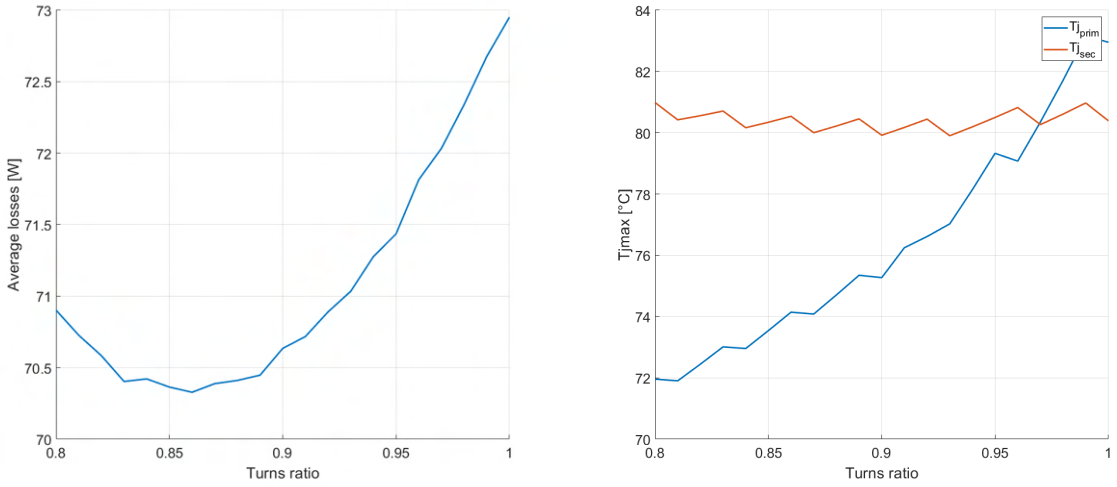
To implement the compensations for non-ideal behaviour some assumptions need to be made about the magnetic components, as these have not yet been designed. The magnetizing inductance needed for the magnetizing current compensation is estimated to be equal to 100 times the calculated leakage inductance. The series resistance of the transformer and external leakage

inductor is left out of the optimization. This does harm it's accuracy somewhat, but not to a problematic degree.

The calculation of the losses is split up in two parts, conduction loss and switching loss. The conduction loss is calculated using the series resistance of the MOSFETs, and the calculated I_{rms} through the switch at the operating point in question. The switching loss calculation is done based on the MOSFET datasheet. The turn-off losses are calculated uses the switching current equations discussed in chapter 2, which are used as an input for a lookup table extracted from the MOSFET datasheet. Turn-on losses are considered to be equal to 0 in full ZVS operating modes, and are assumed to be equal to the half bridge capacitor energy for any half bridge that does not have ZVS when operating outside of the full ZVS operating regions. This assumption is made as the switching current during non-ZVS events is expected to be close to 0.

Figure 4.4 shows the average losses and peak junction temperature for various turns ratio's. The minimum average losses are observed at $n = 0.86$, which differs from the conduction loss based estimate. It should be noted that although this turns ratio has the lowest average loss, the difference within the range of $0.83 < n < 0.89$ is negligible. As the transformer design script will not always be able to get the exact turns ratio this flexibility is beneficial. Given the maximum value of $|\Phi| = 0.41$, and the optimal turns ratio of $n = 0.86$, L_s will be equal to 110.5 μH.

It can also be observed that the maximum junction temperature in the entire operating range does not exceed $83°C$, which is well below the maximum temperature limit of $125°C$. This confirms the suitability of the G3R20MT12K SiC MOSFET.



(a) (b)

Figure 4.4: Average losses and maximum junction temperature

4.2.4 Magnetic design

Based on the turns ratio optimization, which gives a turns ratio of $n = 0.86$, and a leakage inductance of $L_s = 110.5$ μH, a transformer and external leakage inductor can be designed. As the size of the external inductor depends on the size of the transformer leakage inductance, the transformer has to be designed first. This is done with a transformer design script that attempts to find viable designs by cycling through various combinations of primary and secondary turn numbers, and the type and number of transformer cores. Only combinations that meet the flux and maximum ΔT requirements are shown as outputs.

For this process voltage and current data for two cases are provided, the case with the highest RMS current (30.64 A) at $V_{in} = 640\ V$ and $V_{out} = 350\ V$, and the case with the largest transformer flux linkage at $V_{in} = 840\ V$ and $V_{out} = 700\ V$. As E70/33/32 size transformer cores using N87 core material were already present, the design script will be adjusted to use these cores.

The resulting transformer design is shown in table 4.2, it has a turns ratio of $n = 0.875$, which differs slightly from the target but is still within the acceptable range. On the right the table shows the measured leakage and magnetizing inductance. The inductances are referred to the primary side of the transformer, and are obtained using short and open circuit test.

The total leakage inductance value paired with this turns ratio is equal to 108 μH, Thus the external leakage inductor should have a value of 91.8 μH.

part	N_p	N_s	N_{wire}	N_{cores}	l_{gap}	L_{s-p}	L_{m-p}
Transformer	16	14	2	5	0 mm	16.2 μH	5.533 mH
Inductor	9	-	2	3	1.422 mm	87.8 μH	-

Table 4.2: Outcome of the magnetic component design scripts and measured inductance

The external leakage inductor is designed using a script with a similar algorithm adapted for inductor designs. In the left part of table 4.2 the design values for the inductor are shown, while on the right the measured inductances are shown. Due to some inaccuracy with the spacers for the air gap, the air gap length had to be adjusted to get close to the desired inductance. The final air gap resulted in an inductance value of 87.8 μH.
To obtain a series resistance for the components, a simple DC measurement was performed under the assumption that the skin effect is negligible due to the use of very fine litz wire. For the transformer this results in a a primary side resistance of 31 $m\Omega$, and a secondary side resistance of 25 $m\Omega$. For the inductor this resulted in a resistance of 11 $m\Omega$. These values are used for the series resistance compensation, and to estimate the losses of the transformer and inductor.

4.2.5 Efficiency estimation

With the completed transformer and inductor design, it is possible to estimate the total converter loss over the operating range. The estimation of the inductor and transformer conduction loss can be done using the calculated RMS current data. The magnitude of the core loss will be estimated using equation 4.3, based on Steinmetz's equation. The value of k and $beta$ is derived from the core loss outputs of transformer and inductor design scripts, and the estimated flux values. The value α is estimated using the datasheet of the N87 core material. The resulting values are shown in table 4.3. The peak flux λ_p is calculated using the voltage and duty cycle on the primary side of the transformer, combined with a quarter of the switching period. For the inductor the calculation is done based on the peak current and the inductance as shown in table 4.2.

$$P_{core} = k(\frac{f_{sw}}{25000})^{\alpha}\lambda_p^{\beta} \tag{4.3}$$

The efficiency estimate is performed for the proposed modulation method and the variable switching frequency modulation method. The efficiency estimate for both modulations are shown in figure 4.5 and 4.6.

It can be observed that the efficiency of the converter at higher power is the largest when operating close to unity voltage gain, which is expected since the transformer current can be

Part	k_{ind}	α	β
Transformer	$2.392 * 10^6$	1.668	2.303
Inductor	$1.798 * 10^7$	1.668	2.303

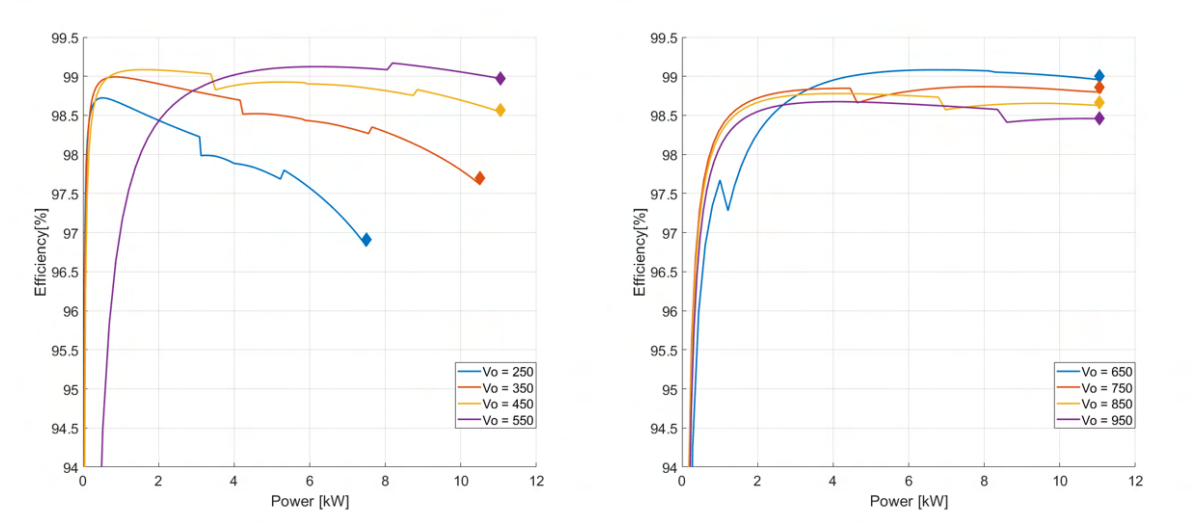
Table 4.3: Constants used in equation 4.3

minimized at the voltage ratio. This does come at the cost of lower efficiency at low power as at unity voltage gain, low power operation occurs in a special case of the transition region with only 4/8 ZVS switching events.

At voltage gains away from unity, the effect of the operating regions can be observed clearly, at low power operation occurs in the triangular region, where switching occurs at full ZVS. When power increases, a sudden drop in efficiency occurs due to operation in the transition region, where ZVS is limited to 6/8 switching events. Then when power increases further, the converter starts operating in the EPS region, ZVS is gained again and a step increase in efficiency occurs. In reality this will be more gradual as the switch will have still have partial ZVS switching close to the operating mode boundaries.

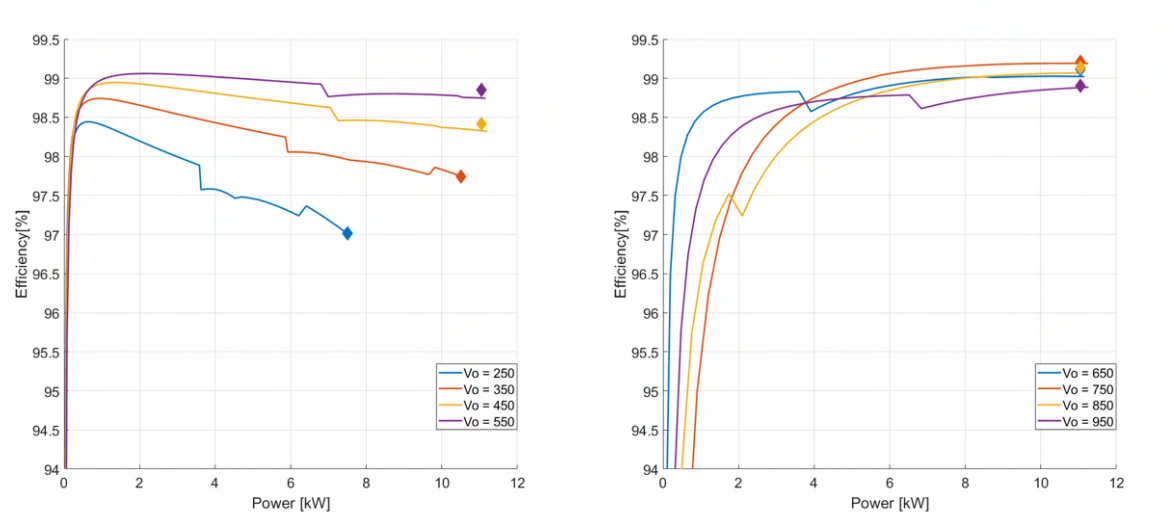
Overall, the estimated efficiency appears to be the highest while operating at higher voltages, as the RMS current to achieve full power is reduced at this operating point.

When comparing the Variable switching frequency operation, who's full power operating points are shown as $*$ in the figures, to the fixed frequency implementation, the efficiency appears very similar. The efficiency of the variable switching frequency implementation is either exactly the same, or higher by a very small margin. At low voltage these slight differences are caused by the difference in modulation between the fixed and variable switching frequency modulation, as the frequency change does not apply at lower voltages. At high output voltages where the frequency is increased, losses will also be affected by differences in ZVS and the frequency change.



(a) (b)

Figure 4.5: Estimated efficiency for the proposed and variable switching frequency modulation ($\diamondsuit$) at $V_{in} = 640\ V$



(a) (b)

Figure 4.6: Estimated efficiency for the proposed and variable switching frequency modulation ($\diamondsuit$) at $V_{in} = 840\ V$

Chapter 5

Test results

To verify performance of the system, the modulation and transient mitigation methods need to be tested. This is done on the DAB converter prototype discussed in chapter 4. The testing is focused on the ZVS performance of the modulation, the transient behavior, and the overall effects of ZVS on the efficiency.

To provide a better overview of the testing process, the experimental setup will be discussed first. After this the results of each part of the tests will be discussed in individual sections.

5.1 Test setup

The observation of the ZVS switching, the transient behavior, and the efficiency efficiency measurements of the converter are all done in the same experimental setup. Below the parts used in the test setup are listed.

- DAB converter PCB with transformer and external leakage inductance
- 2x Bidirectional DC power supply (Delta SM1500-CP-30)
- Power analyzer
- 4 channel oscilloscope with 2 current probes and 2 differential voltage probes

The two power supplies are connected to the primary and secondary DC busses of the converter through the power analyzer. This allows for the measurement of the input and output power of the converter, making it possible to calculate the efficiency of the DAB converter.

The voltage and current probes in the setup are connected to the output of the primary and secondary side H-bridges. The voltage probes show the voltage applied to the inductor and transformer, which can be used to observe ZVS behaviour and to verify the inductor current. The main function of the current probes is to verify the shape of the current waveform, and to check for DC or transient offsets.

5.2 ZVS Behavior

One of the improvements of the proposed modulation method is an increase in the number of ZVS switching events. To confirm whether this improvement is actually achieved, the switching waveforms for the ideal peak current optimization and proposed modulation will be compared.

Whether a switching event has ZVS is determined based on the slope and shape of the voltage waveform, combined with the polarity of the current. Table 5.1 shows the legend for the waveforms in the oscilloscope screenshots used in this chapter.

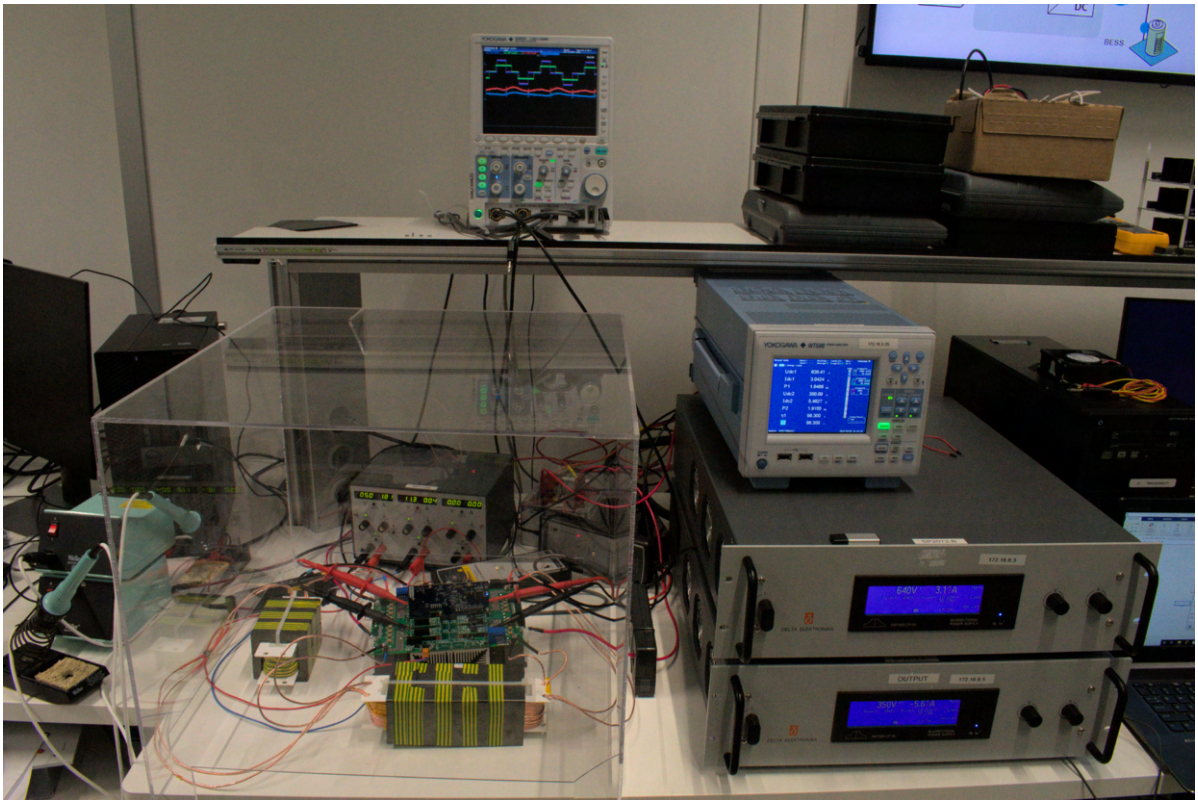


Figure 5.1: Overview of the test setup

Measurement	Description	Line colour
V_1	Primary side inductor voltage	
V_2	Secondary side transformer voltage	
I_1	Primary side inductor current	
I_2	Secondary side transformer current	

Table 5.1: Legend for the oscilloscope screenshots

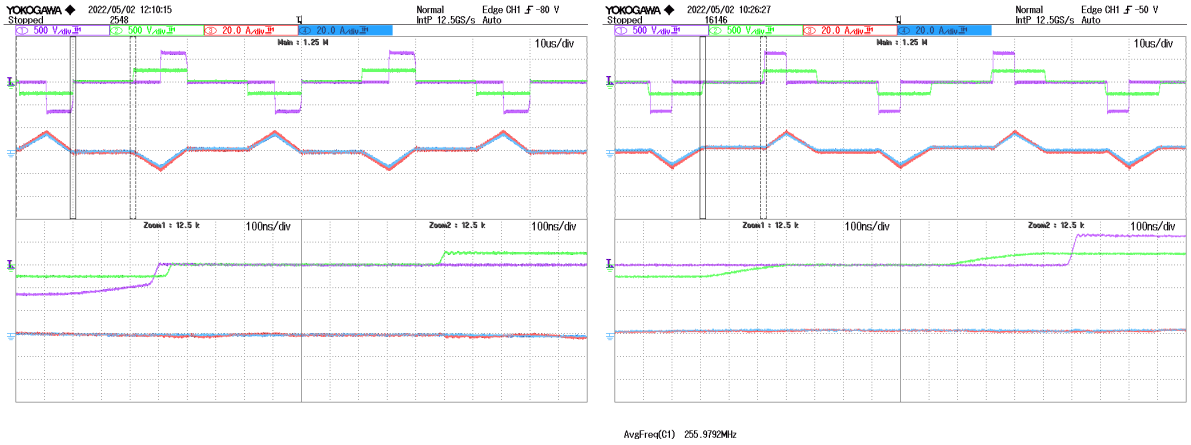
5.2.1 Comparison of the ideal and proposed triangular region

In figure 5.2 and 5.3 the triangular operating regions of the peak current optimization and the proposed modulation method can be seen. For the peak current optimization the expectation is that only 2/8 switching events will have ZVS in the triangular region, however due to offsets caused by dead-time and series resistance this is not always the case. For negative power these offsets cause partial ZVS for the primary side switching event (purple). For positive power the offset is opposite and causes the secondary side to have full ZVS, increasing the number of ZVS events to 6/8.

The peak current optimization as shown in figure 5.2 still has less ZVS events than the full ZVS operation that can be observed for the proposed modulation in figure 5.3, however the difference is smaller than initially expected because of the offsets in the current.

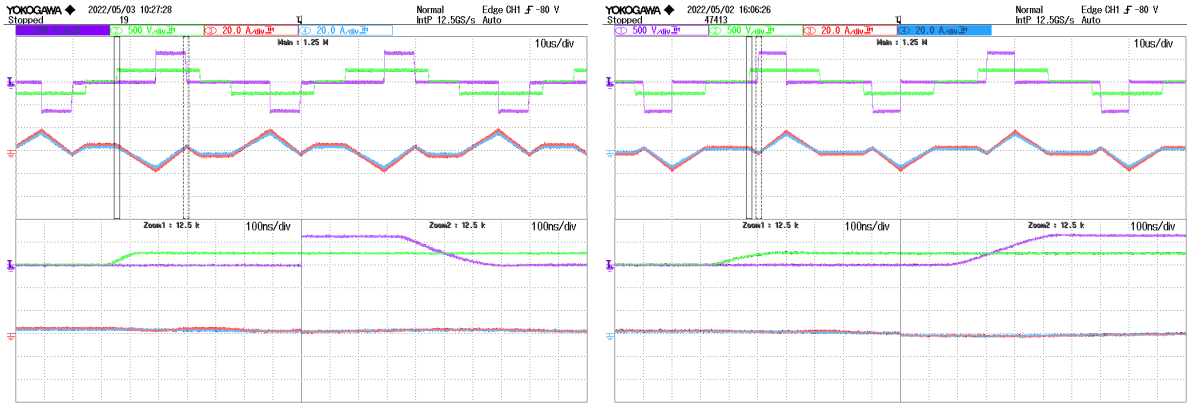
5.2.2 ZVS performance around the transition region

One of the goals of the proposed modulation method is to maintain a high number of ZVS events over the entire operating range. To achieve this the transition region was implemented such that 6/8 ZVS events can be maintained in this region, or 4/8 when operating at very low



(a) $P_{ref} = -1000W$ (b) $P_{ref} = 1000W$

Figure 5.2: Ideal triangular modulation at $V_{in} = 640\ V$ and $V_{out} = 250\ V$



(a) $P_{ref} = -1000W$ (b) $P_{ref} = 1000W$

Figure 5.3: Proposed triangular modulation at $V_{in} = 640\ V$ and $V_{out} = 250\ V$

power at unity gain. Figure 5.4 shows an overview of the approximate operating points used to confirm ZVS around the transition region.

In figure 5.5 and 5.6 the waveforms from the triangular region, transition region, the partial ZVS and full ZVS parts of the EPS region. In the transition from the triangular region (figure 5.5a) to the transition region (figure 5.5b), the switching events of the primary and secondary side voltage start to overlap. Switching current remains positive such that the secondary side switching events maintains ZVS, at the cost of ZVS for one of the primary side switching events. As the power is increased and the EPS region is entered (figure 5.6a), ZVS does not return immediately. After increasing the power further the full ZVS part of the EPS region is reached (figure 5.6b). This confirms that when not operating at unity gain, 6/8 ZVS events are maintained in all times.

5.2.3 Unity voltage gain behaviour

At unity voltage gain, the converter does not operate in the triangular region at low power. Instead it starts in the transition region. This also affects ZVS performance, as now only 4/8 switches are expected to have ZVS at very low power. This can be seen in figure 5.7, where the secondary side has full ZVS, and the Primary side no or only partial ZVS at 1000 W. When increasing the power further, the partial ZVS switching event gains full ZVS and operation with

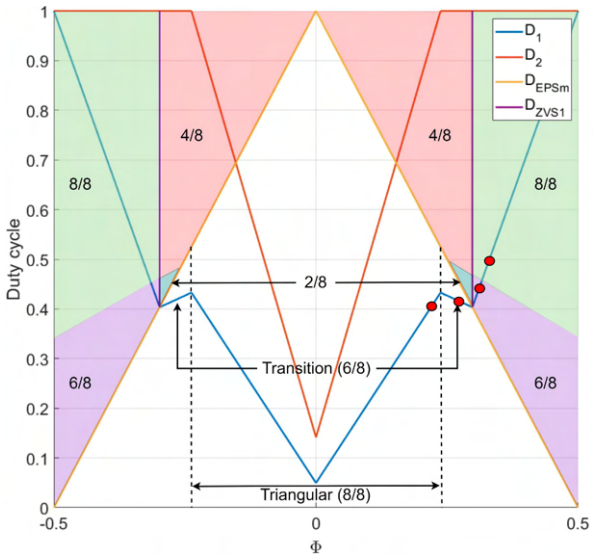
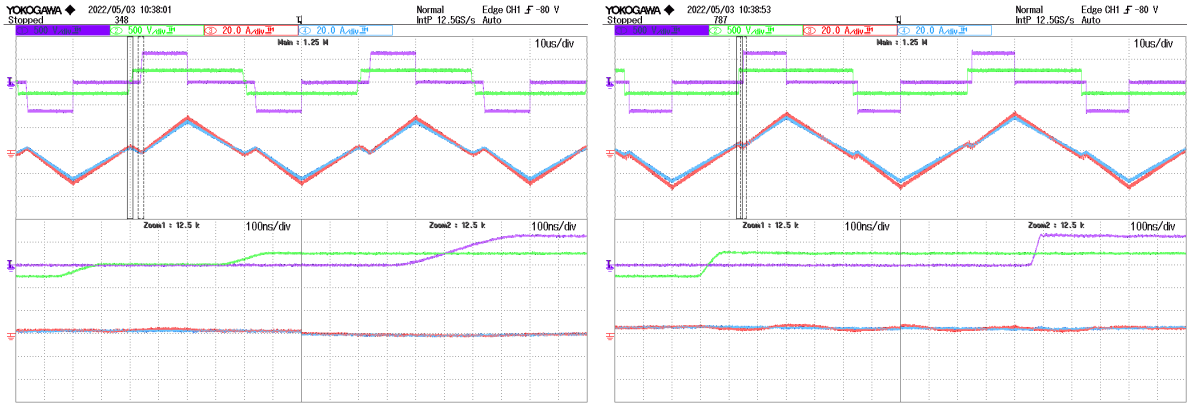
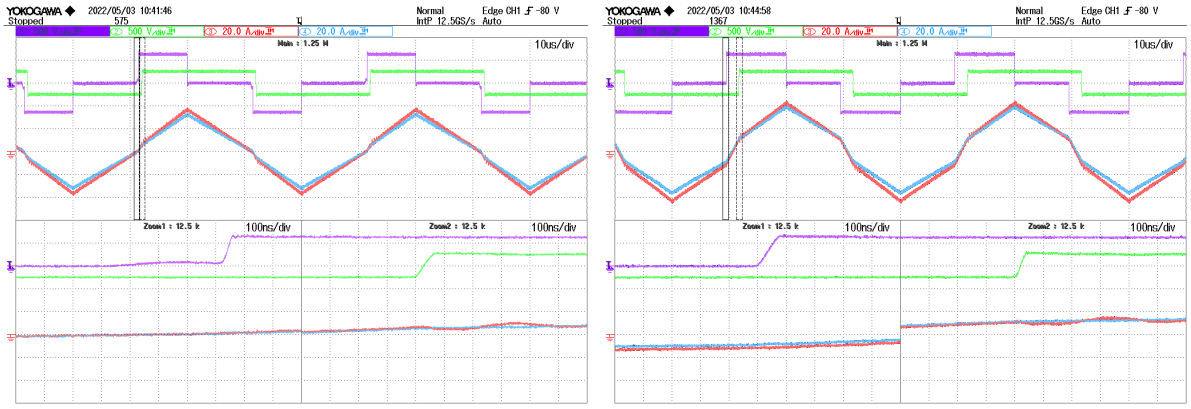


Figure 5.4: Overview of the operating points used to confirm ZVS in the transition region



(a) $P_{ref} = 3000W$ (b) $P_{ref} = 4000W$

Figure 5.5: Positive triangular and transition region at $V_{in} = 640\ V$ and $V_{out} = 250\ V$

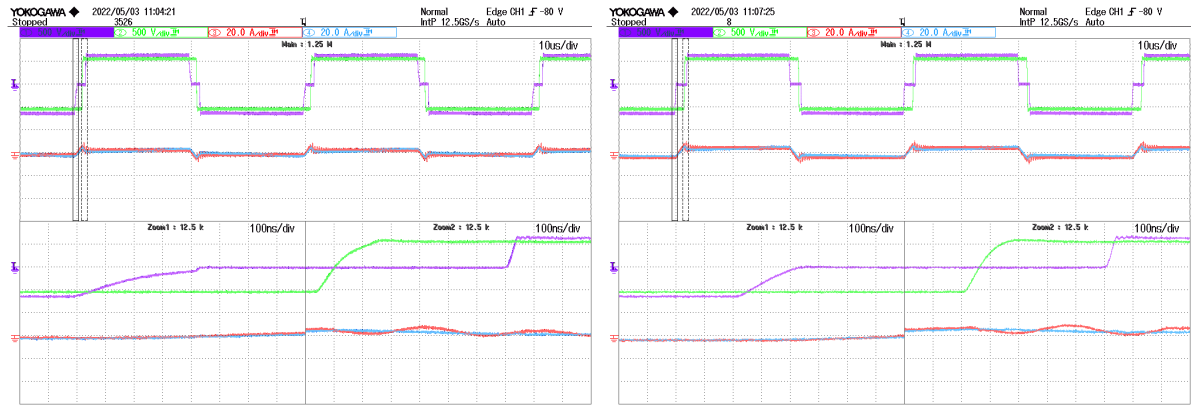


(a) $P_{ref} = 5000W$ (b) $P_{ref} = 6000W$

Figure 5.6: Positive non-ZVS and full ZVS part of the EPS region $V_{in} = 640\ V$ and $V_{out} = 250\ V$

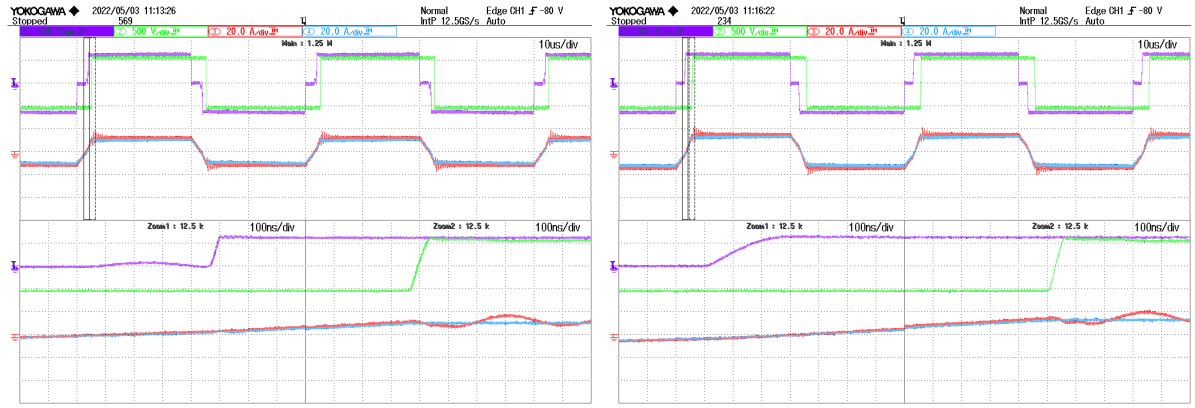
6/8 ZVS events resumes.

When power is increased further operation will shift to the EPS region where ZVS will be gained for the last pair of switches, as shown in figure 5.8.



(a) $P_{ref} = 1000\ W$ (b) $P_{ref} = 2000\ W$

Figure 5.7: Unity gain transition region at $V_{in} = 640\ V$ and $V_{out} = 550\ V$



(a) $P_{ref} = 6000\ W$ (b) $P_{ref} = 7000\ W$

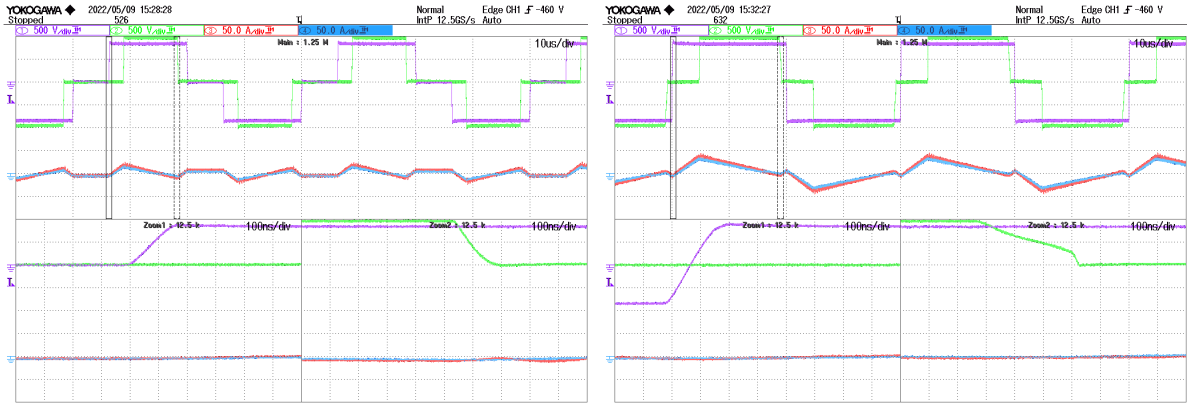
Figure 5.8: Unity gain EPS region at $V_{in} = 640\ V$ and $V_{out} = 550\ V$

5.2.4 High voltage operation

Figure 5.9 shows the DAB converter operation at the maximum tested input and output voltage. At this voltage operation mainly takes place in the triangular region, where full ZVS is observed. At maximum power the converter operates in the transition region with only 6/8 ZVS switching events.

5.2.5 Unexpected non-ZVS behaviour

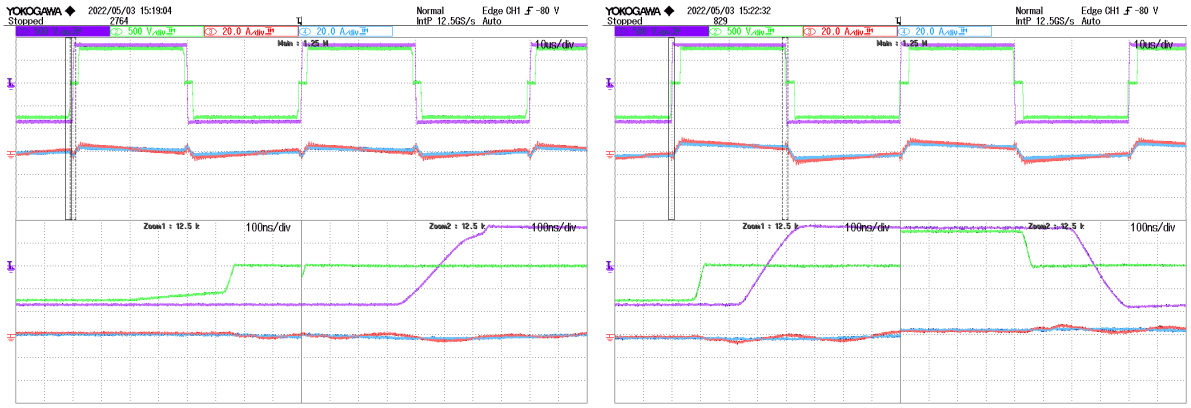
Figure 5.10 shows a case with a voltage close to unity gain at low power. At this voltage gain, the converter operates in the transition region from zero power. As the voltage gain is larger than 1, the primary side switches (purple) should have full ZVS. In 5.10 it can be seen that this is almost the case, as at 1000 W ZVS is not achieved completely. Possible causes could be not taking into account the transformer parasitic capacitance, however the error is very small it's



(a) $P_{ref} = 4000\ W$ (b) $P_{ref} = 11000\ W$

Figure 5.9: Triangular and Transition region operation at $V_{in} = 840\ V$ and $V_{out} = 950\ V$

effects on performance are inconsequential. The error appears to go away when increasing the power from 1000 to 2000 W.



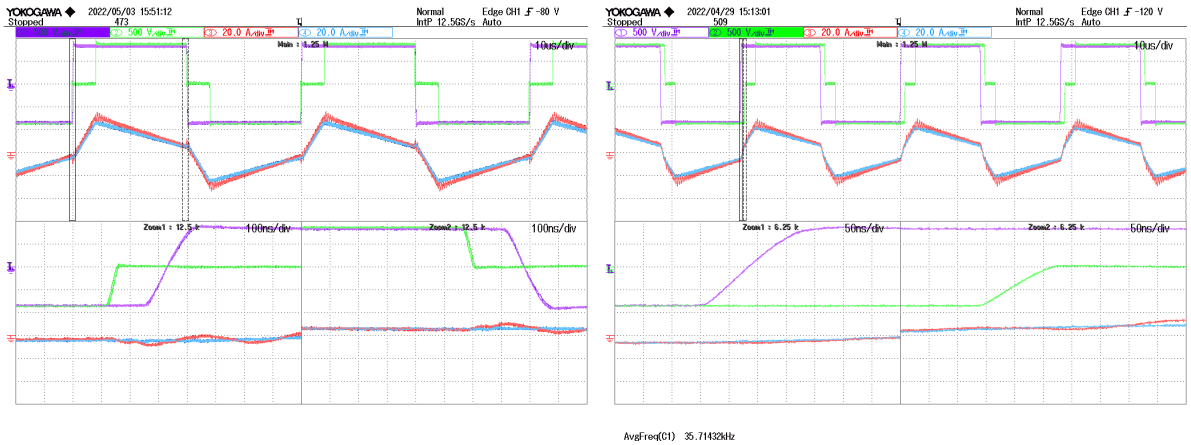
(a) $P_{ref} = 1000\ W$ (b) $P_{ref} = 2000\ W$

Figure 5.10: Unintended partial ZVS $V_{in} = 840\ V$ and $V_{out} = 750\ V$

5.2.6 Variable switching frequency modulation ZVS behaviour

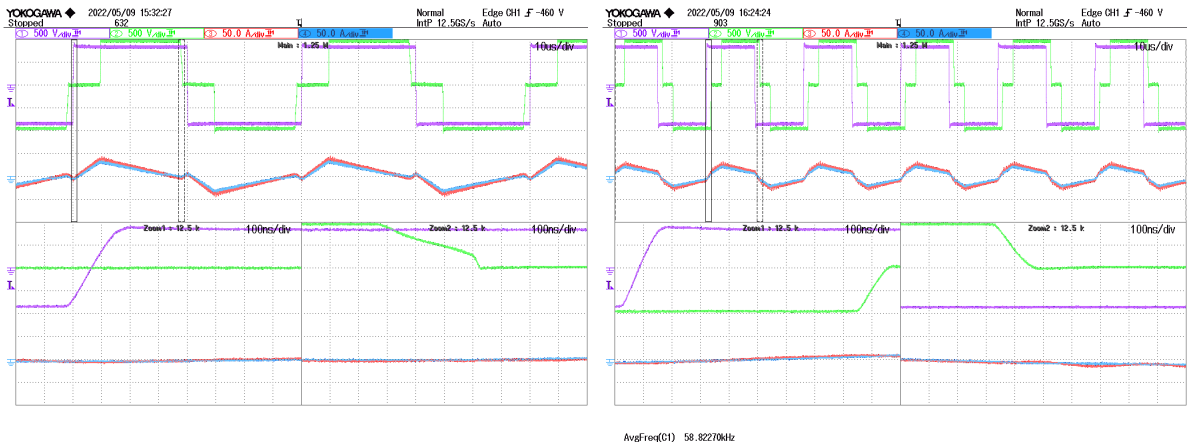
To see the effect of the variable switching frequency modulation, it is compared to the proposed fixed frequency modulation method. This is done at full power at an input voltage of $V_{in} = 840\ V$ and an output voltage of $V_{out} = 850\ V$ and $V_{out} = 950\ V$.

The measurements results are shown in figure 5.11 and 5.12. For the fixed frequency modulation, at $V_{out} = 850\ V$ only 6 out of 8 switching events have ZVS, as the converter operates in the transition region. At $V_{out} = 950\ V$, operation is closer to the triangular region, where partial ZVS is now achieved for the non-ZVS switching event. For the variable switching frequency implementation, full ZVS operation is achieved at the same operating voltage and power by increasing the switching frequency such that the operating point is shifted into the full ZVS part of the EPS region. At $V_{in} = 840\ V$ and $V_{out} = 850\ V$, a frequency of 35.7 kHz can be observed, while at $V_{out} = 950\ V$ the frequency is increased up to 58.8 kHz, compared to the base frequency of 25 kHz.



(a) Fixed switching frequency (b) Variable switching frequency

Figure 5.11: Fixed and variable frequency modulation at $V_{in} = 840\ V$ and $V_{out} = 850\ V$



(a) Fixed switching frequency (b) Variable switching frequency

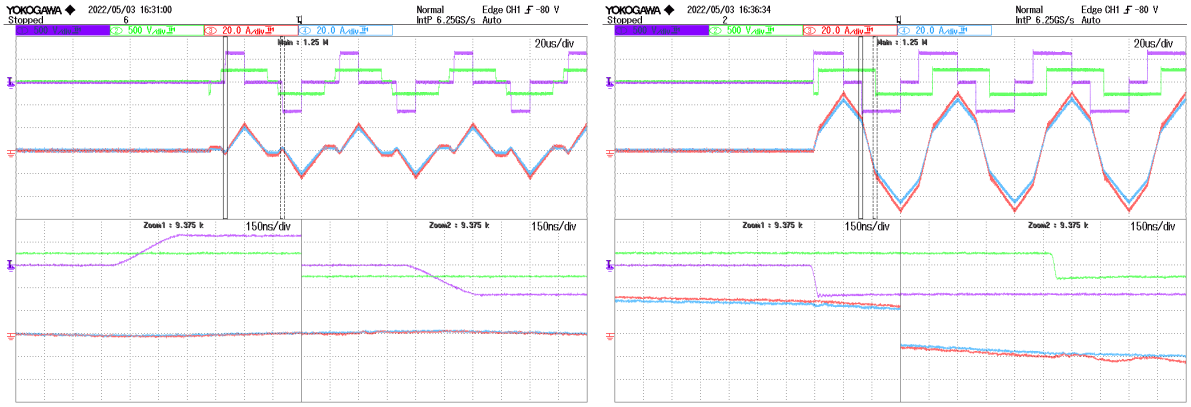
Figure 5.12: Fixed and variable frequency modulation at $V_{in} = 840\ V$ and $V_{out} = 950\ V$

5.3 Transient Behaviour

There are two parts involving the transient behaviour of the converter, the startup of the converter from its disabled state, and the transition between different levels of power.

Figure 5.13 shows the startup for the triangular and EPS regions. The transition region is not shown as it uses the same equations for transient mitigation as the triangular region. For both the triangular and EPS regions no noticeable offset is found after startup. This shows that the synchronized enable does work as intended.

For the transitions in power, transitions to different operating modes and to different power

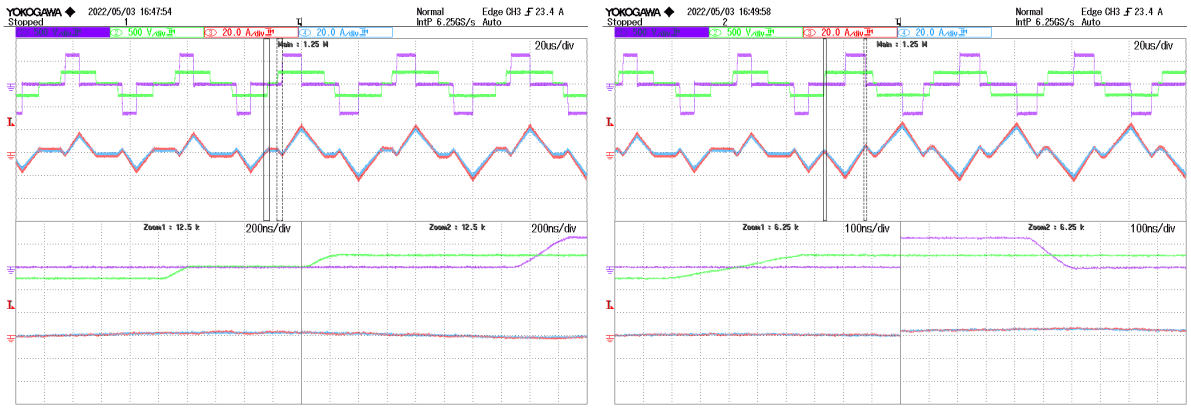


(a) 0 to 2000 W (b) 0 to 7500 W

Figure 5.13: Startup transient in the triangular and EPS region at $V_{in} = 640\ V$ and $V_{out} = 250\ V$

polarity will be discussed.

Figure 5.14 shows the positive and negative transition within the triangular region. Not only is there no noticeable offset, ZVS is also maintained during the transition. This is not the



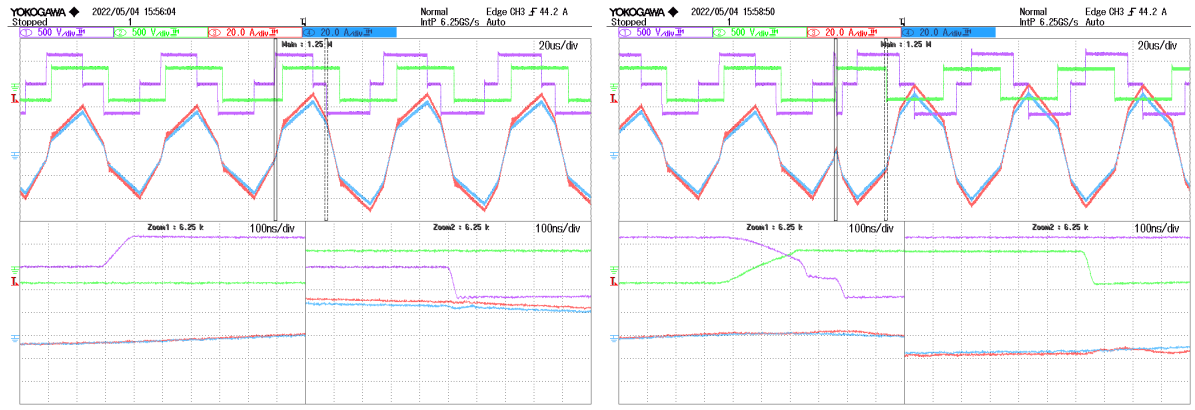
(a) 1000 to 2000 W (b) 1000 to -2000 W

Figure 5.14: Transitions within the triangular region at $V_{in} = 640\ V$ and $V_{out} = 250\ V$

case for transitions in the EPS region, as shown in figure 5.15. While the positive transition does maintain ZVS and has no noticeable offset, the negative transition does not have full ZVS during the transition and has a positive DC offset. This offset is likely caused by the difference in the initial state of the switches between positive and negative power. It should be noted that this transition is unlikely to occur in practice, as suddenly reversing the direction of power flow

in an EV charger does not make sense.

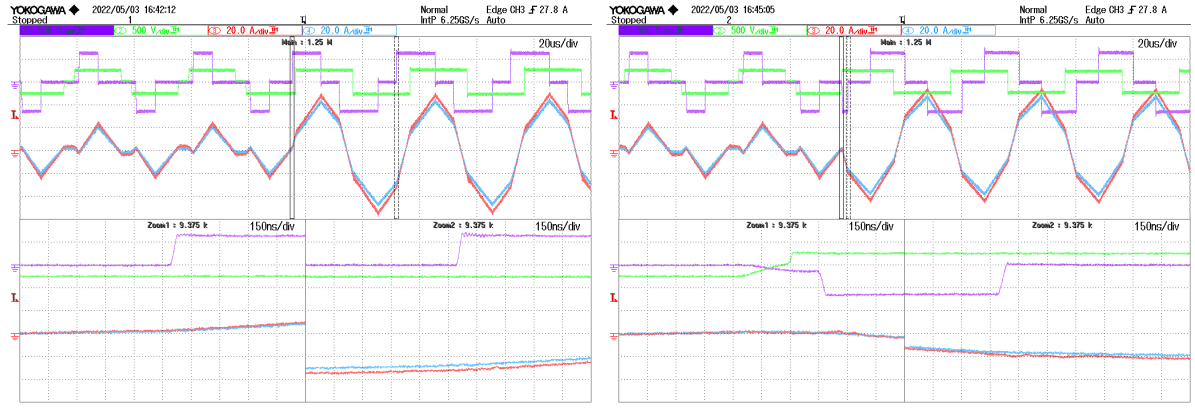
The transition from the triangular region to the EPS region in figure 5.15 shows a DC offset in for both directions of EPS power flow. For the positive to positive transition this is a fairly small offset, but for the positive to negative transition the offset is comparable to that of for the EPS to EPS transition. It is not expected that these offsets will cause problems with performance. In neither the positive nor the negative case is ZVS maintained during the transition.



(a) 8000 to 10500 W

(b) 8000 to -10500 W

Figure 5.15: Transitions within the EPS region at $V_{in} = 640\ V$ and $V_{out} = 350\ V$



(a) 2000 W to 7500 W

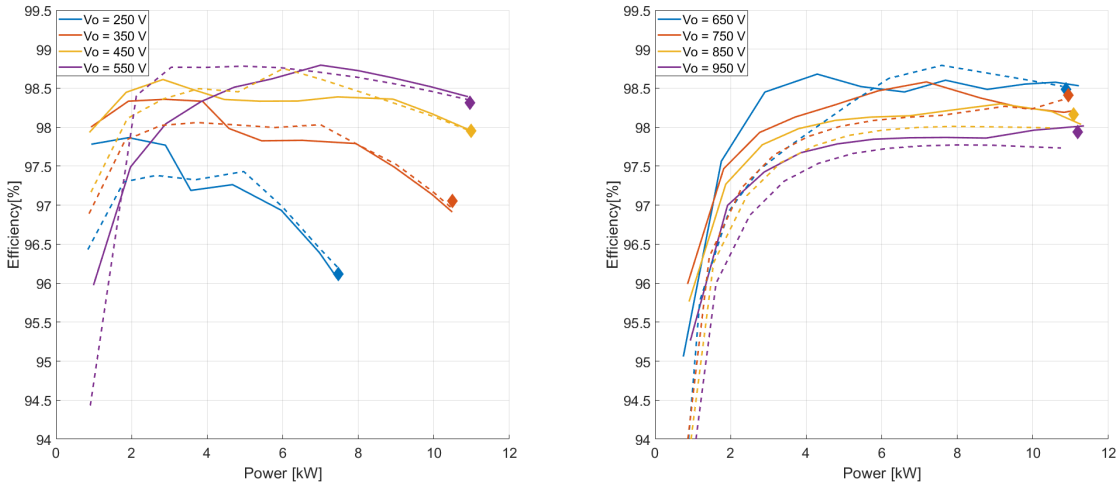
(b) 2000 W to -7000 W

Figure 5.16: Transitions from the triangular region to the EPS region at $V_{in} = 640\ V$ and $V_{out} = 250\ V$

5.4 Converter efficiency

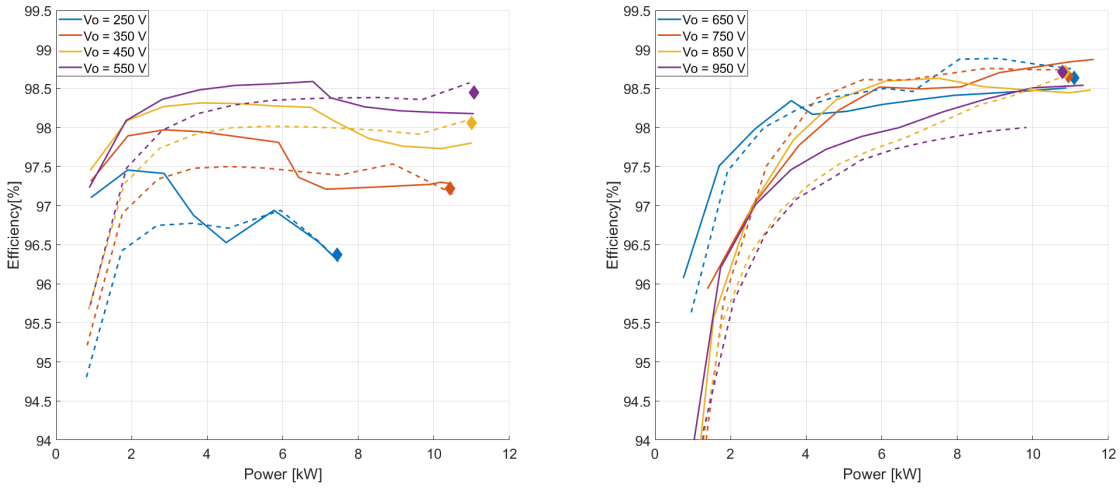
Compared to the peak current optimization based modulation, the proposed modulation has more ZVS switching events, especially at low power. On the other hand, the proposed modulation also has slightly increased RMS current. To observe the difference among the peak current optimization, the proposed modulation and the variable frequency modulation, efficiency data points have been collected at various points in the operating range.

This has been done at input voltages of 640 V and 840 V, with steps in output voltage of 100 V, and steps in power of 1000 W.



(a) (b)

Figure 5.17: Efficiency for the proposed modulation (—), peak current optimization (- -) and variable switching frequency modulation (◇) at $V_{in} = 640\ V$



(a) (b)

Figure 5.18: Efficiency for the proposed modulation (—), peak current optimization (- -) and variable switching frequency modulation (◇) at $V_{in} = 840\ V$

Figure 5.17 and 5.18 show the measured efficiency for each of the operating modes. First of all, it can be observed that the converter efficiency in practice is slightly lower that the theoretical efficiency shown in figures 4.5 and 4.6 in chapter 4. Possible causes for this could be inaccuracy in the modelling of the magnetic components, or inaccurate values for on resistance or switching loss in the datasheet. Since this does not affect the comparison between modulation methods, and no problematic temperatures were observed during testing, this difference will not be looked into further.

When comparing the proposed and peak current optimization based modulation methods, there are some noticeable differences in efficiency. These differences are particularly large at low power, where switching loss has a fairly large contribution to the total losses. The proposed modulation operates with full ZVS in its triangular region, while the peak current optimization based modulation will have limited ZVS in this region. The exception to this behaviour is around unity voltage gain, where the proposed modulation starts in the transition region.

At slightly larger power, the converter will start to leave the triangular region and enter the transition region. Here the efficiency of the proposed method drops slightly below that of the peak current optimization. This is likely the result of the proposed method having slightly larger RMS current than the peak current optimization, while losing some of its advantage in ZVS due to entering the transition region. In the case where the voltage gain is close to unity, at $V_{out} = 550$ for 5.17, and at $V_{out} = 750$ for 5.18, this starts at very low power as the proposed modulation method operates in the transition region from 0 power under these conditions. Because of this the peak current optimization shows better results at low to medium power if the voltage gain is close to unity.

At high power, In the EPS region for the lower output voltages, the efficiency is very similar between the proposed and peak current optimization based modulation methods. This is expected as both operate in the full ZVS part of the EPS region at this point. At higher output voltages the converter mainly operates in the triangular region and does not reach the EPS region. Because of this the peak current optimization will operate with 2/8 ZVS over almost the entire power range. This can also be observed in the efficiency of the peak current optimization, which is lower than that of the proposed method over the entire power range at higher output voltages.

When comparing the variable frequency modulation to the proposed modulation, the differences in efficiency at full power are fairly small. Table 5.2 shows the average full power efficiency, which is the average value of all the measured full power efficiency in both input voltages (640V and 840V) and all output voltages. Although the differences are small, the variable switching frequency modulation appears slightly more efficient. When low power efficiency is considered, the variable frequency modulation is intended to operate with a pulsed charging profile, which would have the same efficiency as at full power. As the efficiency of the proposed modulation method below maximum power is higher that of the variable frequency modulation method at full power, there are no real benefits to the variable frequency modulation when the efficiency is considered.

Modulation method	Average full power efficiency
Peak current optimization	97.895%
Proposed fixed frequency modulation	97.879%
Proposed variable frequency modulation	97.964%

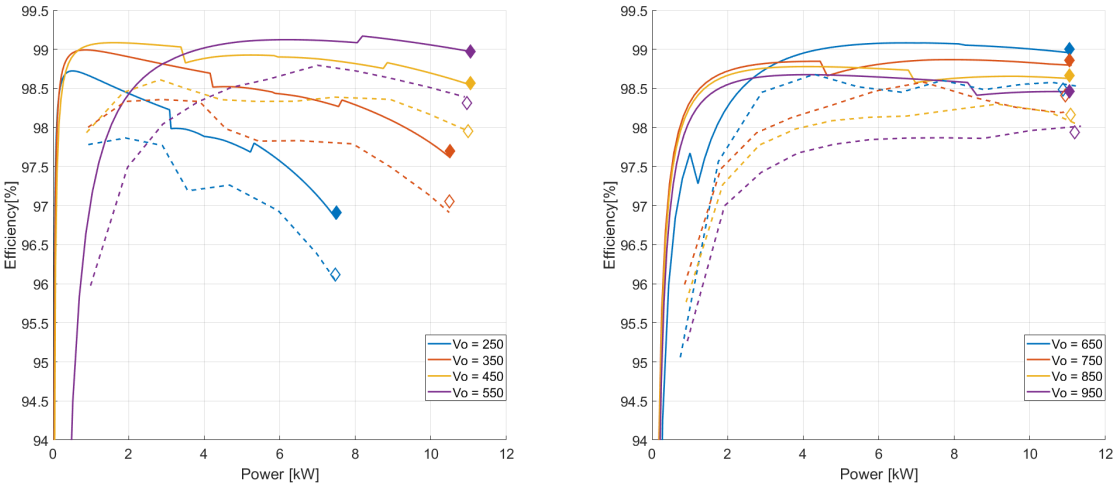
Table 5.2: Average full power efficiency of each modulation method

In the end the proposed modulation mainly improves performance in the triangular region, while being comparable to the efficiency of the peak current optimization in other operating modes. While operating at high voltage this affects the majority of the operating range, but at low voltage improvements to efficiency are limited to low power.

The converter operates most efficiently around unity voltage gain, where the RMS currents are the lowest. The least efficient operating point can be found at the lowest output voltage of 250 V. Here the maximum power is reduced due to the DC output current limit of 30 A, with

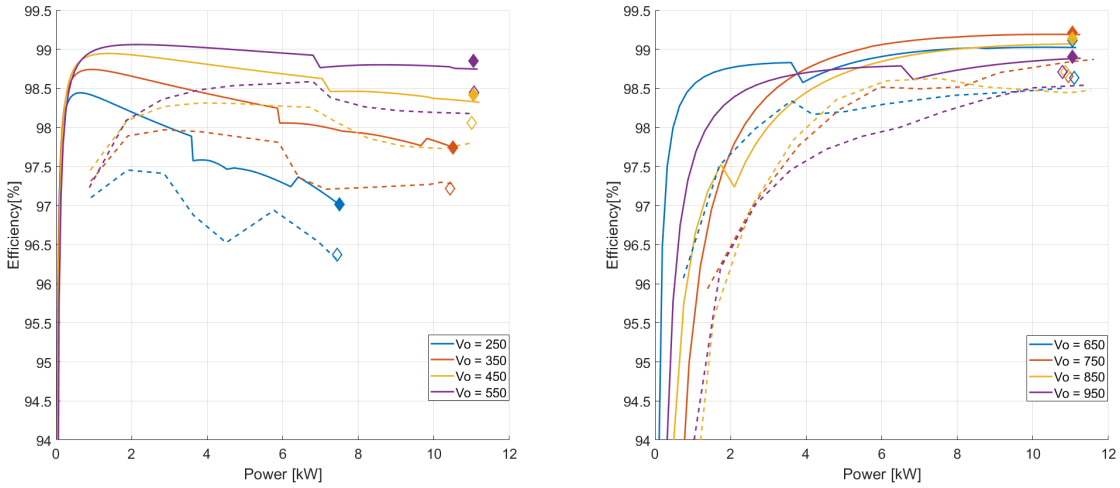
RMS currents in on the primary side of the transformer in the range of 30 A. This combination of high conduction loss and lower output power.

Figure 5.19 and 5.20 show the estimated and measured efficiency of the DAB converter. Overall the converter efficiency is slightly lower than the estimated efficiency provided in chapter 4. As no seperate measurements were taken for any of the converter components, the cause of this difference cannot be properly analysed. While the measured efficiency is slightly lower compared to the estimated efficiency, the measured efficiency does follow the general pattern seen in the estimated efficiency with respect to changes in voltage and power. To resolve the differences a more accurate models of the converter, inductor and transformer losses based on measured losses of the individual parts could be included. The effect of temperature, which can increase conduction loss, and reduces core loss can also be considered.



(a) (b)

Figure 5.19: Estimated (—) and measured (- -) efficiency of the proposed modulation method at $V_{in} = 640\ V$



(a) (b)

Figure 5.20: Estimated (—) and measured (- -) efficiency of the proposed modulation method at $V_{in} = 840\ V$

Chapter 6

Conclusion

The goal of this thesis is to design a beneficial modulation method that improves the ZVS behaviour and efficiency of a wide voltage range dual active bridge converter.

Among the various modulation techniques in literature, the peak current optimization based modulation method stands out as it achieves full range soft switching and comparatively low currents regardless of the input voltage, output voltage and output power of the converter. The main drawback of this method is that only 2/8 switches have ZVS at low power. To solve this a new method is proposed which uses the same operating modes as the peak peak current optimization, however with modifications based on the DAB converter's ZVS requirements that allow it to have full ZVS at low power. This modification to the low power region creates a discontinuity, for which a transition region is added in a way that allows 6/8 switches to maintain ZVS, with the exception of unity gain operation where only 4/8 switches can maintain ZVS at very low power. This should provide a noticeable improvement to efficiency while operating low power.

To achieve full ZVS over the entire operating range, an additional modulation method has been proposed. For this method the converter always operates at full power, which can be used in a pulsed or MSCC charging profile. The converter will always operate in the full ZVS part of the high power EPS region, and if it does not do so, the frequency is increased until it does.

In the simulation it was observed that switching events did non always have ZVS where they should. Using the simulation three main causes were found, magnetizing current offset, series resistance and dead-time. These sources of non-ideal behaviour caused offsets to the calculated switching current, which in turn prevents ZVS depending on the operating region. To address these compensations have been added to the switching where these offsets apply, ensuring that no unintentional loss of ZVS occurs.

In addition to the improved modulation methods, a control system has been designed. The control system uses a lookup table with reference power and the input and output DC voltages as its input and phase shift as its output. The phase shift is then used in the calculations for the modulation method. This type of control system does not require current sensing, and has a very fast transient response. This is combined with a new transient DC offset mitigation method. Compared to the methods proposed in literature, which use a variable length switching period to resolve both the leakage and magnetizing current offset, the proposed method is much simpler. It applies a phase shift to the entire voltage waveform such that the leakage current is 0 at the start of each period. Although it is simple to implement, it does have the possibility of a magnetizing current DC offset during a transient, which has to be taken into account in the transformer design.

To verify the proposed modulation methods, a DAB converter was constructed based on

an existing PCB design. For this design a turns ratio optimization is performed that reduces the average switching and conduction loss over the operating range. Based on the outcome a transformer and inductor were designed and built.

The assembled DAB converter was then used to perform measurements on the ZVS behaviour, transient behaviour and efficiency of the peak current optimization, the proposed modulation, and the variable switching frequency modulation.

Results show that the proposed modulation method does provide the number of ZVS events it should according to the calculations. This is also noticeable in the significant increase in the low power efficiency compared to the peak current optimization from literature. In the meantime, operation in the transition region appears slightly less efficient than that of the peak current optimization. At high power all modulation methods achieve fairly similar efficiency, with the exception of higher voltage operation where the proposed and variable switching frequency methods hold an advantage.

The measurements done on the transient mitigation method show the expected behaviour, a small offset or no offset at all during a transient. Transitions from positive power to a different value of positive power generally have the smallest offset, while transitions from positive to negative power show a slightly larger offset. The measured offsets are small enough to not form a problem for general operation, confirming the functionality of the transient mitigation method.

In conclusion, the proposed modulation method provides an advantage in wide voltage range application compared to peak current optimization in literature. The increase in ZVS switching reduces component stress and improves efficiency. Combined with a simple to implement but functional transient mitigation method, a practical and efficient control system has be designed for a DAB converter used in EV application.

6.1 future work

One of the disadvantages of wide voltage range operation is the large differences in current stress and efficiency in different parts of the voltage range. At low voltage high output current is needed and efficiency drops below 96.5%, while at unity voltage gain the current stress is low and efficiency reaches above 98.5%. As components have to be dimensioned for worst case conditions this leads to increased converter size.

A possible way to improve this would be by using two smaller DAB converters, that can have their outputs connected either in parallel or in series. This would reduce the required converter output voltage range from $250V < V_{out} < 1000V$ to $250V < V_{out} < 500V$, allowing for a more efficient and compact design.

Furthermore, a detailed optimization of the converter that includes the inductor and transformer design in its calculations could be considered. By including the magnetic components the overall converter size or efficiency can be minimized, instead of only the losses of the switching components.

Appendix A

Controller implementation

This chapter discusses the the simulink implementation of the controller. The simulink model is flashed onto the microcontroller using the embedded coder support package for TI C2000 microprocessors.

A.1 Simulink model

A.1.1 Communication

The communication between the computer and microcontroller is done using the serial protocol over USB with a baud rate of 9600. On the computer a dashboard is used as shown in figure A.1. The information received is sent from CPU 2 to CPU 1 through the internal communication channels of the microcontroller. This is done every switching period. the implementation of this system is shown in figure A.2.

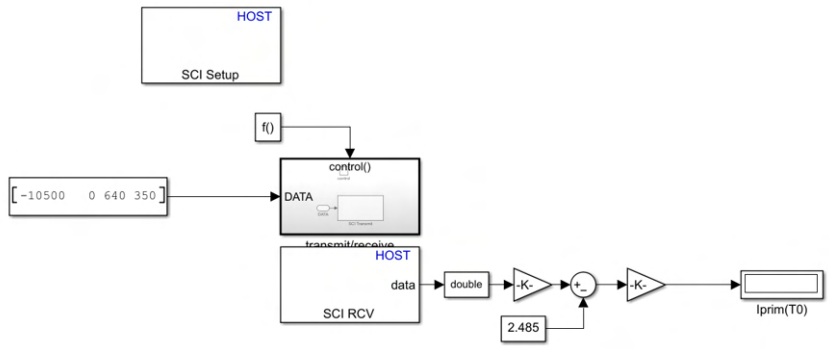


Figure A.1: Communication dashboard

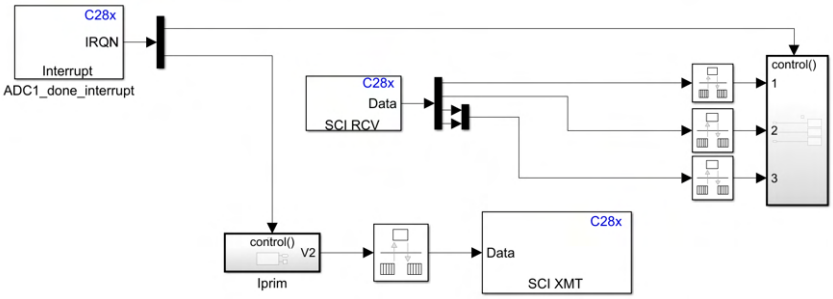


Figure A.2: Controller side implementation of the communication on CPU 2

A.1.2 Controller model

Figure A.3 shows an overview of the simulink model used to program the microcontroller. Outside of the internal communication channel receive submodules, it has the main controller and GPIO submodules. These are triggered using interrupts generated by the ADC end of conversion and ePWM 5 reset interrupts.

For the fixed frequency implementation the controller is shown in figure A.4. it uses the voltage

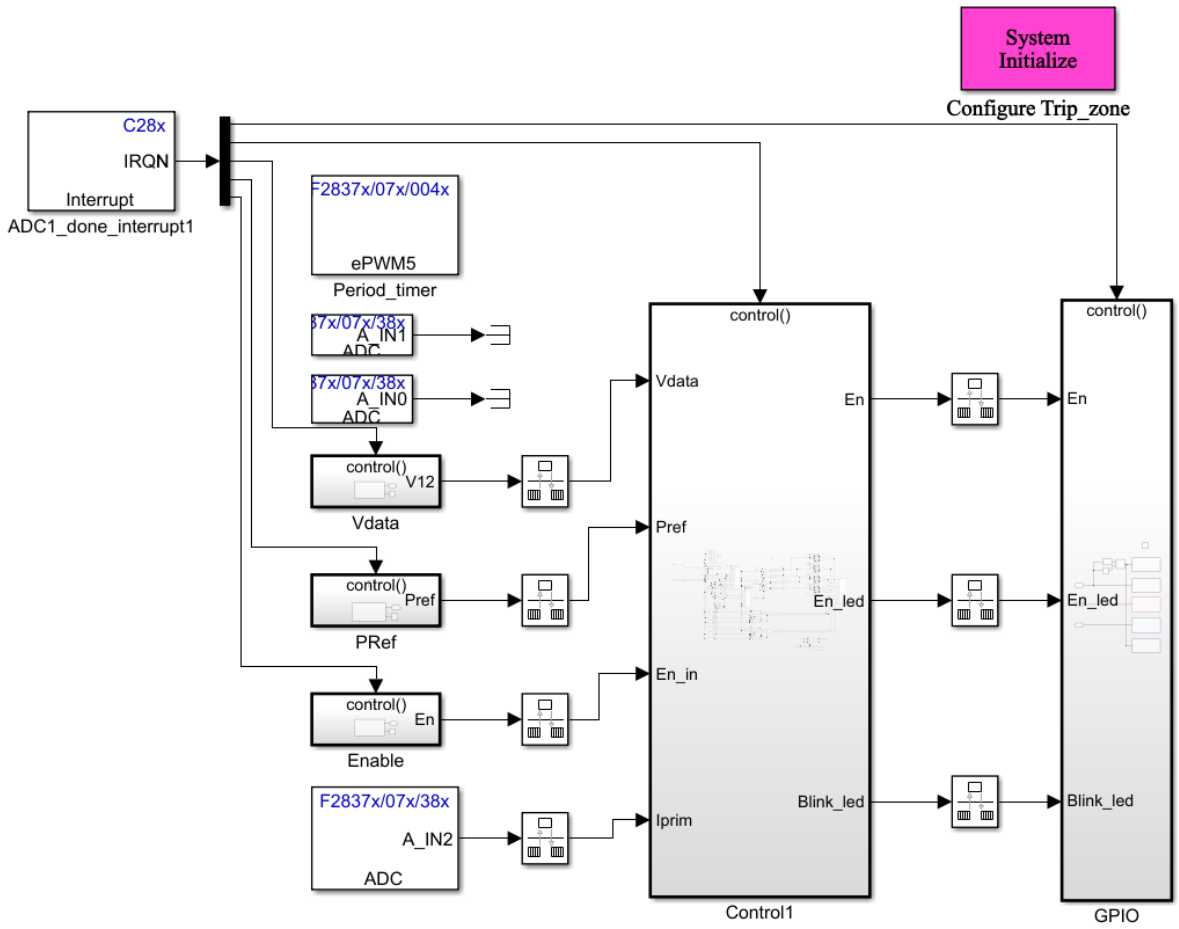


Figure A.3: Simulation overview

inputs and power reference it receives to calculate the dead-time, phase shift and needed ZVS current. These are then input into the control function block, which calculates D_1 and D_2. The offset calculation block uses these for transient mitigation. The outputs can then be used to calculate the phase shift of each module, and translated into compare values for the ePWM modules. A.5 shows the ePWM module's.

The variable frequency model is similar to that of the fixed frequency controller. There are some differences in the generation of the power reference, as it always operates at full power, and in the implementation of the variable switching frequency, which is done through a lookup table.

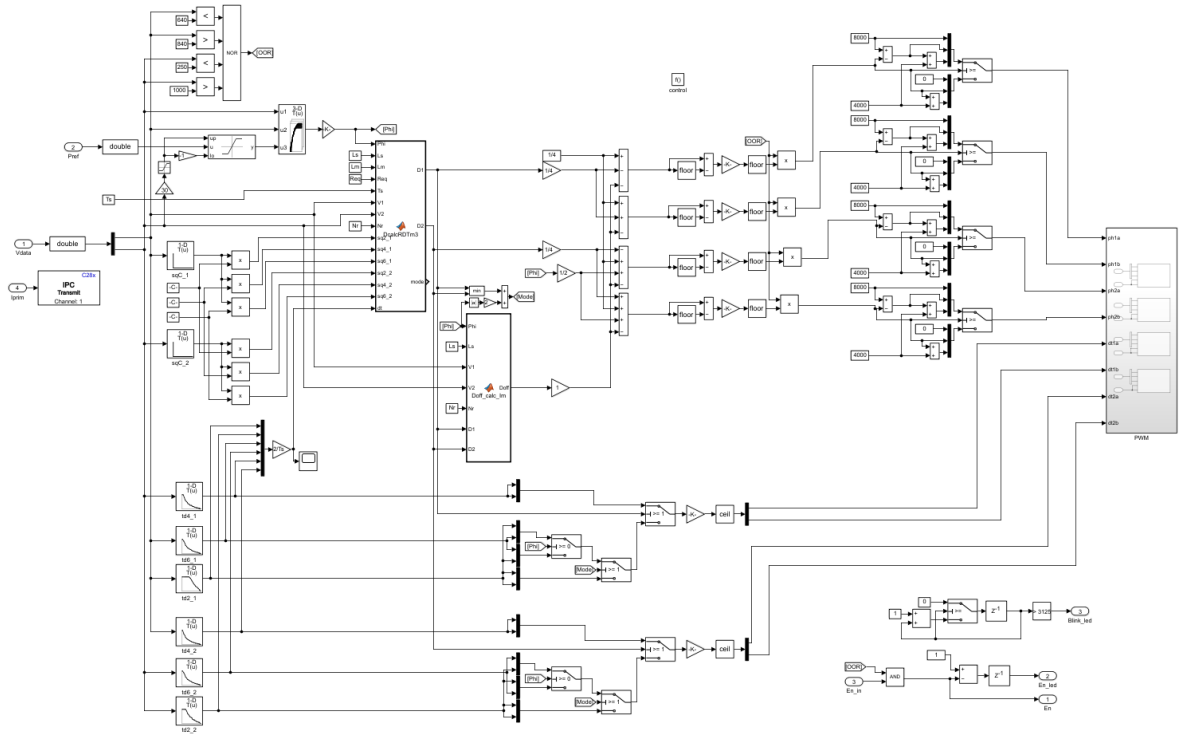


Figure A.4: Fixed frequency controller

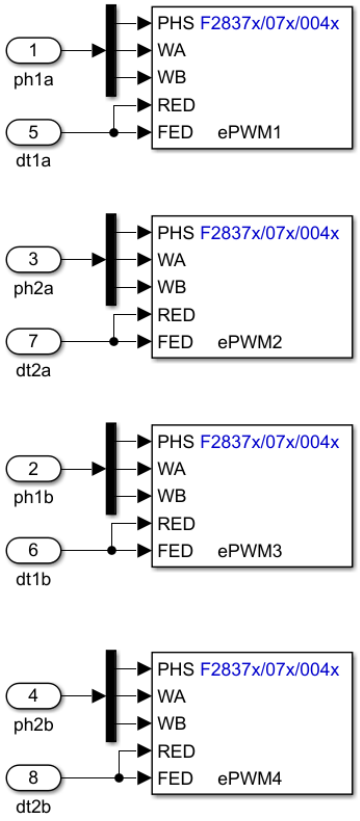


Figure A.5: PWM modules of the fixed frequency controller

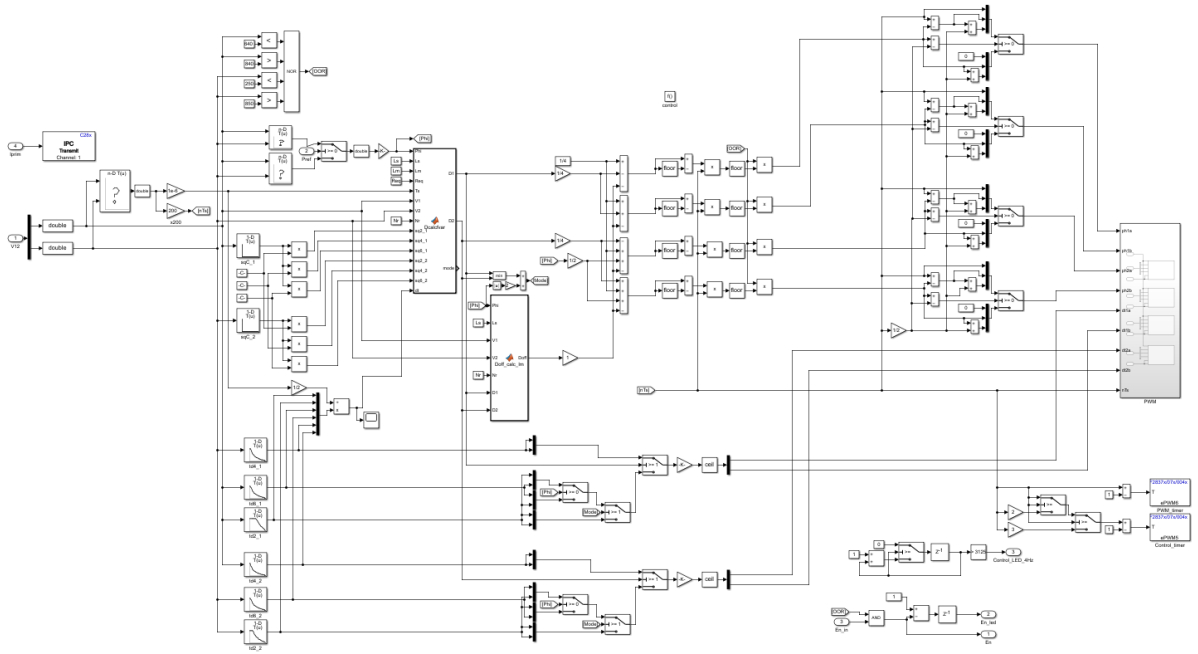


Figure A.6: Variable frequency controller

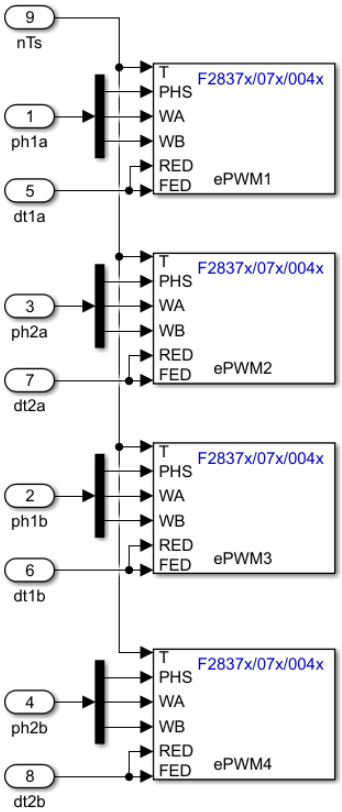


Figure A.7: PWM modules for the variable frequency controller

A.2 Offset calculation code

Code used in simulink to calculate the phase shift offset applied to all half bridges needed to start every switching period at $I_L = 0$.

```
function Doff = Doff_calc(Phi,Ls,V1,V2,Nr,D1,D2)
```

```
  kg = V2/(V1*Nr);
  ki = 1/kg;
  Phi_a = abs(Phi);

  if kg <= 1
    if D1>1-2*Phi_a % eps
      if Phi >= 0
        if D1*(ki+1)+2*Phi_a-2 > 0;
          Doff = (2*Phi_a-2)/(4*(ki+1))+0.25;
        else
          Doff = Phi_a/2+D1/4*ki+0.75;
        end
      else
        if D1*(ki+1)+2*Phi_a-2 > 0;
          Doff = -(2*Phi_a-2)/(4*(ki+1))+0.75;
        else
          Doff = 0.25-Phi_a/2-D1/4*ki
        end
      end
    else
      if Phi >= 0; % mode 1
        Doff = 0.5*Phi_a+D1/4*ki+0.75; % works
      else
        Doff = -0.5*Phi_a-D1/4*ki+0.25; %works
      end
    end
  elseif kg > 1
    if D2>1-2*Phi_a
      if Phi >= 0
        if D2*(1+kg)+2*Phi_a-2 > 0
          Doff = kg*(2*Phi_a-2)/(4*(kg+1))+D1/4;
        else
          Doff = -D2/4*kg+D1/4;
        end
      else
        if D2*(1+kg)+2*Phi_a-2 > 0
          Doff = -kg*(2*Phi_a-2)/(4*(kg+1))+D1/4+0.5;
        else
          Doff = D2/4*kg+D1/4+0.5;
        end
      end
    else
      if Phi >= 0;
        Doff = -D2*kg/4+0.25; %works
      else
        Doff = D2*kg/4-0.25; %works
      end
    end
  end
end
```

A.3 Control function code

This section contains the three control functions used in the simulation and for programming the microcontroller.

A.3.1 Control function for the peak current optimization

```
function [D1 D2 mode] = DcalcIdeal(Phi,V1,V2,Nr)
  kg = V2/(V1*Nr);
  Phi = abs(Phi);
  if kg <= 1
    kg = kg-1e-9;
    Phi_EPS = 0.5-0.5*kg;
    if Phi > Phi_EPS % EPS region
      D2 = 1;
      D1 = (Phi-Phi_EPS)*(1-kg)/(0.5-Phi_EPS)+kg;
      mode = 1;
    else  % Triangular modulation
      D2 = Phi/Phi_EPS;
          D1 = (Phi*kg)/(Phi_EPS);
          mode = 0;
    end
  else
    ki = 1/kg;
    Phi_EPS = 0.5-0.5*ki;
    if Phi > Phi_EPS % EPS region
      D1 = 1;
      D2 = (Phi-Phi_EPS)*(1-ki)/(0.5-Phi_EPS)+ki;
      mode = 1;
    else  % Triangular modulation
      D1 = Phi/Phi_EPS;
      D2 = (Phi*ki)/(Phi_EPS);
      mode = 0;
    end
  end
end
```

A.3.2 Control function for the proposed fixed frequency modulation

```
function [D1,D2,mode] = DcalcRDTm3(Phi,Ls,Lm,Req,Ts,V1,V2,Nr,
   sq2_1,sq4_1,sq6_1,sq2_2,sq4_2,sq6_2,dt)
   kg = V2/(V1*Nr);
   if Phi>=0
      a1 = 1;
      a2 = 0;
   else
      a1 = 0;
      a2 = 1;
   end
   Phi = abs(Phi);
   mi = Ls/Lm;
```

```
if kg <= 1
   kg = kg-1e-6;
   ILc = Req*(V2/Nr*Ts^2*(1-kg))/(16*Ls^2);
   comp = (4*Ls/Ts)*(ILc/V1); %Series resistance compensation.
   % Boundary calculations
   Phi_EPS = 0.5-0.5*kg+2*Ls*Nr*sq4_2/(Ts)+kg*mi+a2*comp/2+a2*
      dt(6);
   D_1_EPS = 1-2*Phi_EPS-a2*(dt(1)+dt(3));
   Phi_TRGlim = 0.5-0.5*kg-(2*Ls)/(Ts)*(sq2_1/kg+sq2_2*Nr*(1-
      kg))-(0.5-0.5*kg)*mi-comp*(a2*(0.5-0.5*kg)+0.5*a1/kg)-(
      a1+2*a2)*dt(1)/kg*(0.5-0.5*kg)-a2*dt(2);
   D_1_TRG = 2*kg*(Phi_TRGlim+a2*dt(2))/(1-kg)+sq2_1*(4*Ls/Ts)
      /(1-kg)+a1*comp/(1-kg)+a1*dt(1);
   if Phi > Phi_EPS % EPS region
     a = (1-D_1_EPS)/(0.5-Phi_EPS);
     b = D_1_EPS-a*Phi_EPS;
     D1 = a*Phi+b;
     D2 = 1;
     if D1 > (kg*(2-2*Phi)+(4*Ls/Ts)*(sq6_1+a1*ILc/V1))/(1+kg)
        +a1*(dt(1)+dt(3));
        mode = 3;
     else
        mode = 2;
     end
   elseif (Phi < Phi_EPS) && (Phi >= Phi_TRGlim) % transition
      region
     if  Phi_TRGlim < 0
        Phi_TRGlim = 0;
     end
     a = (D_1_EPS-D_1_TRG)/(Phi_EPS-Phi_TRGlim);
     b = D_1_TRG-a*Phi_TRGlim;
     D1 = a*Phi+b;
     D2 = 1;
     mode = 1;
   else  % Triangular modulation %%% increase lower D2/D1 DT
      comp (during transition an increase of 2 dt(1) is
      possible)
     D1 = 2*kg*(Phi+a2*dt(2))/(1-kg)+sq2_1*(4*Ls/Ts)/(1-kg)+a1
        *comp/(1-kg)+a1*dt(1);
     D2 = 2*(Phi+a2*dt(2))/(1-kg)+(4*Ls/Ts)*(sq2_2*Nr+sq2_1/(
        kg*(1-kg)))+mi+comp*(a2+a1/(kg*(1-kg)))+((a1+2*a2)*dt
        (1)/kg);
     mode = 0;
   end
else
   ki = 1/kg;
   ILc = Req*(V1*Ts^2*(1-ki))/(16*Ls^2);
   comp = 4*Ls*ILc*Nr/(V2*Ts);
   % Boundary calculations
   Phi_EPS = 0.5-0.5*ki+2*Ls*sq4_1/(Ts)+a1*comp/2+a1*dt(5);
   D_2_EPS = 1-2*Phi_EPS-a1*(dt(2)+dt(4));
```

```
        Phi_TRGlim = 0.5-0.5*ki-(2*Ls)/(Ts)*(Nr*sq2_2/ki+(1-ki)*
            sq2_1)-mi/(2*ki)-comp*(a1*(0.5-0.5*ki)+0.5*a2/ki)-((2*a1
            +a2)*dt(2)/ki)*(0.5-0.5*ki)-a1*dt(1);
        D_2_TRG = 2*ki*(Phi_TRGlim+a1*dt(1))/(1-ki)+sq2_2*Nr*4*Ls
            /((1-ki)*Ts)+mi/(1-ki)+a2*comp/(1-ki)+a2*dt(2);
        if Phi > Phi_EPS % EPS region
          a = (1-D_2_EPS)/(0.5-Phi_EPS);
          b = D_2_EPS-a*Phi_EPS;
          D2 = a*Phi+b;
          D1 = 1;
          if D2 > (ki*(2-2*Phi)+(4*Ls/Ts)*(sq6_2+a2*Nr*ILc/V2))/(1+
              ki)+a2*(dt(2)+dt(4));
              mode = 3;
          else
              mode = 2;
          end
        elseif (Phi < Phi_EPS) && (Phi >= Phi_TRGlim) % transition
            region
          if  Phi_TRGlim < 0
              Phi_TRGlim = 0;
          end
          a = (D_2_EPS-D_2_TRG)/(Phi_EPS-Phi_TRGlim);
          b = D_2_TRG-a*Phi_TRGlim;
          D2 = a*Phi+b;
          D1 = 1;
          mode = 1;
        else  % Triangular modulation
          D2 = 2*ki*(Phi+a1*dt(1))/(1-ki)+sq2_2*Nr*4*Ls/((1-ki)*Ts)
              +mi/(1-ki)+a2*comp/(1-ki)+a2*dt(2);
          D1 = 2*(Phi+a1*dt(1))/(1-ki)+4*Ls/(Ts)*(sq2_1+Nr*sq2_2/(
              ki*(1-ki)))+mi/(ki*(1-ki))+comp*(a1+a2/(ki*(1-ki)))
              +((2*a1+a2)*dt(2)/ki);;
          mode = 0;
        end
    end
end
```

A.3.3 Control function for the variable switching frequency modulation

```
function [D1 D2 mode] = Dcalcfvar(Phi,Ls,Lm,Req,Ts,V1,V2,Nr,sq2_1
    ,sq4_1,sq6_1,sq2_2,sq4_2,sq6_2,dt)
    kg = V2/(V1*Nr);
    if Phi>=0
        a1 = 1;
        a2 = 0;
    else
        a1 = 0;
        a2 = 1;
    end
    Phi = abs(Phi);
    mi = Ls/Lm;
```

```
if kg <= 1
   kg = kg-1e-6;
   ILc = Req*(V2/Nr*Ts^2*(1-kg))/(16*Ls^2);
   comp = (4*Ls/Ts)*(ILc/V1); %Series resistance compensation.
   % Boundary calculations
   Phi_EPS = 0.5-0.5*kg+2*Ls*Nr*sq4_2/(Ts)+kg*mi+a2*comp/2+a2*
      dt(6);
   D1_EPS = (kg*(2-2*Phi_EPS)+(4*Ls/Ts)*(sq6_1+a1*ILc/V1))/(1+
      kg)+a1*(dt(1)+dt(3));
   if D1_EPS>1
     D1_EPS = 1;
     Phi_EPS = (-1+kg+(4*Ls/Ts)*(sq6_1+a1*ILc/V1))/(2*kg)+(1+
        kg)/(2*kg)*a1*(dt(1)+dt(3));
   end
   if Phi>Phi_EPS
     a = (1-D1_EPS)/(0.5-Phi_EPS);
     b = D1_EPS-a*Phi_EPS;
     D1 = a*Phi+b;
     D2 = 1;
     mode = 3;
   else
     a = (D1_EPS)/(Phi_EPS);
     D1 = a*Phi;
     D2 = Phi/Phi_EPS;
     mode = 0;
   end
 else
   ki = 1/kg;
   ILc = Req*(V1*Ts^2*(1-ki))/(16*Ls^2);
   comp = 4*Ls*ILc*Nr/(V2*Ts);
   % Boundary calculations
   Phi_EPS = 0.5-0.5*ki+2*Ls*sq4_1/(Ts)+a1*comp/2+a1*dt(5);
   D2_EPS =(ki*(2-2*Phi_EPS)+(4*Ls/Ts)*(sq6_2+a2*Nr*ILc/V2))
      /(1+ki)+a2*(dt(2)+dt(4)); %eps bound 2
   if D2_EPS>1
     D2_EPS = 1;
     Phi_EPS = (-1+ki+(4*Ls/Ts)*(sq6_2+a2*Nr*ILc/V2))/(2*ki)
        +(1+ki)/(2*ki)*a2*(dt(2)+dt(4));
   end
   if Phi>Phi_EPS
     a = (1-D2_EPS)/(0.5-Phi_EPS);
     b = D2_EPS-a*Phi_EPS;
     D2 = a*Phi+b;
     D1 = 1;
     mode = 3;
   else
     a = (D2_EPS)/(Phi_EPS);
     D2 = a*Phi;
     D1 = Phi/Phi_EPS;
     mode = 0;
   end
```

```
    end
end
```

Bibliography

[1] Ahmed A Abdullah Al-karakchi, Gillian Lacey, and Ghanim Putrus. "A method of electric vehicle charging to improve battery life". In: *2015 50th International Universities Power Engineering Conference (UPEC)*. 2015, pp. 1–3. DOI: 10.1109/UPEC.2015.7339846.

[2] T.M Al. "Electric vehicle charger for future DC Grids". M.S. Thesis,TU delft, 2020. URL: http://resolver.tudelft.nl/uuid:a8ba9621-ee53-42ca-bb7c-b148eddf078c.

[3] Qinglei Bu et al. "A Comparative Review of High-Frequency Transient DC Bias Current Mitigation Strategies in Dual-Active-Bridge DC-DC Converters Under Phase-Shift Modulations". In: *IEEE Transactions on Industry Applications* (2021), pp. 1–1. DOI: 10.1109/TIA.2021.3136498.

[4] *Data sheet Product LAM 5 D K 125 12*. fisher elektronik. URL: https://www.fischerelektronik.de/web_fischer/en_GB/VA/LAM5DK12512/datasheet.xhtml?branch=heatsinks.

[5] Qing Gu et al. "Current Stress Minimization of Dual-Active-Bridge DC–DC Converter Within the Whole Operating Range". In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 7.1 (2019), pp. 129–142. DOI: 10.1109/JESTPE.2018.2886459.

[6] Xu Han, Yuan Tan, and Hao Ma. "The switching frequency optimization of dual phase shift control for dual active bridge DC-DC converter". In: *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*. 2017, pp. 1610–1615. DOI: 10.1109/IECON.2017.8216273.

[7] Peiwen He and Alireza Khaligh. "Comprehensive Analyses and Comparison of 1 kW Isolated DC–DC Converters for Bidirectional EV Charging Systems". In: *IEEE Transactions on Transportation Electrification* 3.1 (2017), pp. 147–156. DOI: 10.1109/TTE.2016.2630927.

[8] Jingxin Hu, Shenghui Cui, and Rik W. De Doncker. "Natural Boundary Transition and Inherent Dynamic Control of a Hybrid-Mode Modulated Dual-Active-Bridge Converter". In: *IEEE Transactions on Power Electronics* (2021), pp. 1–1. DOI: 10.1109/TPEL.2021.3119903.

[9] Jingxin Hu et al. "Generic Dynamic Phase-Shift Control for Bidirectional Dual-Active Bridge Converters". In: *IEEE Transactions on Power Electronics* 36.6 (2021), pp. 6197–6202. DOI: 10.1109/TPEL.2020.3039348.

[10] Jun Huang et al. "Unified Triple-Phase-Shift Control to Minimize Current Stress and Achieve Full Soft-Switching of Isolated Bidirectional DC–DC Converter". In: *IEEE Transactions on Industrial Electronics* 63.7 (2016), pp. 4169–4179. DOI: 10.1109/TIE.2016.2543182.

[11] Amit Kumar Jain and Rajapandian Ayyanar. "Pwm control of dual active bridge: Comprehensive analysis and experimental verification". In: *IEEE Transactions on Power Electronics* 26.4 (2011), pp. 1215–1227. DOI: 10.1109/TPEL.2010.2070519.

[12] Georgios Kampitsis et al. "An accurate Matlab/Simulink based SiC MOSFET model for power converter applications". In: *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2015, pp. 1058–1064. DOI: 10.1109/APEC.2015.7104479.

[13] Liting Li et al. “An Optimized DPS Control for Dual Active Bridge Converters to Secure Full Load Range ZVS with Low Current Stress”. In: *IEEE Transactions on Transportation Electrification* (2021), pp. 1–1. DOI: 10.1109/TTE.2021.3106130.

[14] Dingsihao Lyu, Thiago Batista Soeiro, and Pavol Bauer. “Impacts of Different Charging Strategies on the Electric Vehicle Battery Charger Circuit Using Phase-Shift Full-Bridge Converter”. In: *2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC)*. 2021, pp. 256–263. DOI: 10.1109/PEMC48073.2021.9432497.

[15] N. Noroozi, A. Emadi, and M. Narimani. “Performance Evaluation of Modulation Techniques in Single-Phase Dual Active Bridge Converters”. In: *IEEE Open Journal of the Industrial Electronics Society* 2 (2021), pp. 410–427. DOI: 10.1109/OJIES.2021.3087418.

[16] N. Noroozi, A. Emadi, and M. Narimani. “Performance Evaluation of Modulation Techniques in Single-Phase Dual Active Bridge Converters”. In: *IEEE Open Journal of the Industrial Electronics Society* 2 (2021), pp. 410–427. DOI: 10.1109/OJIES.2021.3087418.

[17] Zhi Qu et al. “Comprehensive power MOSFET model for LLC resonant converter in renewable energy applications”. In: *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*. 2016, pp. 1–5. DOI: 10.1109/PEDG.2016.7527095.

[18] Sebastian Rivera et al. “Electric Vehicle Infrastructure: From Grid to Battery”. In: *IEEE Industrial Electronics Magazine* 15.2 (2021), pp. 37–51. DOI: 10.1109/MIE.2020.3039039.

[19] Shuai Shao et al. “Optimal Phase-Shift Control to Minimize Reactive Power for a Dual Active Bridge DC–DC Converter”. In: *IEEE Transactions on Power Electronics* 34.10 (2019), pp. 10193–10205. DOI: 10.1109/TPEL.2018.2890292.

[20] Guo Xu et al. “Decoupled EPS Control Utilizing Magnetizing Current to Achieve Full Load Range ZVS for Dual Active Bridge Converters”. In: *IEEE Transactions on Industrial Electronics* (2021), pp. 1–1. DOI: 10.1109/TIE.2021.3078351.

[21] Guo Xu et al. “Fixed duty cycle compensation and magnetizing current design for DAB DC-DC converter with conventional trapezoidal modulation to achieve zero voltage switching”. In: *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*. 2016, pp. 433–438. DOI: 10.1109/IPEMC.2016.7512325.

[22] Guo Xu et al. “Optimized EPS Control to Achieve Full Load Range ZVS With Seamless Transition for Dual Active Bridge Converters”. In: *IEEE Transactions on Industrial Electronics* 68.9 (2021), pp. 8379–8390. DOI: 10.1109/TIE.2020.3014562.

[23] Yunpeng Yao et al. “Hybrid modulation scheme for dual active bridge converter that employs the triangular modulation and the single phase shift modulation”. In: *International Journal of Circuit Theory and Applications* 44.11 (2016), pp. 1982–2002. DOI: https://doi.org/10.1002/cta.2206. eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/cta.2206. URL: https://onlinelibrary.wiley.com/doi/abs/10.1002/cta.2206.

[24] Sheng-Yang Yu, Chris Hsiao, and Jack Weng. “A High Frequency CLLLC Bi-directional Series Resonant Converter DAB Using an Integrated PCB Winding Transformer”. In: *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2020, pp. 1074–1080. DOI: 10.1109/APEC39645.2020.9124521.

[25] Faizah Zahin, Alireza Abasian, and S. Ali Khajehoddin. “An Alternative Dual Active Bridge Modulation to Minimize RMS Current and Extend ZVS Range”. In: *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2020, pp. 5952–5959. DOI: 10.1109/ECCE44975.2020.9235374.

[26] Haihua Zhou and Ashwin M. Khambadkone. “Hybrid Modulation for Dual Active Bridge Bi-Directional Converter With Extended Power Range For Ultracapacitor Application”. In: *2008 IEEE Industry Applications Society Annual Meeting*. 2008, pp. 1–8. DOI: 10.1109/08IAS.2008.275.