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Fossum, Eric R.; Teranishi, Nobukazu; Theuwissen, Albert J.P.

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Eric R. Fossum,[1] Nobukazu Teranishi,[2] and Albert J.P. Theuwissen[3,4]

[1]Thayer School of Engineering, Dartmouth College, Hanover, New Hampshire, USA; email: eric.r.fossum@dartmouth.edu

[2]Research Institute of Electronics, Shizuoka University, Hamamatsu, Japan

[3]Department of Microelectronics, Delft University of Technology, Delft, The Netherlands

[4]Harvest Imaging, Bree, Belgium

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Keywords

image sensor, charge-coupled device, CCD, complementary metal oxide semiconductor image sensor, CMOS image sensor, CIS, quanta image sensor, QIS, photon-counting image sensor

Abstract

This article reviews nearly 60 years of solid-state image sensor evolution and identifies potential new frontiers in the field. From early work in the 1960s, through the development of charge-coupled device image sensors, to the complementary metal oxide semiconductor image sensors now ubiquitous in our lives, we discuss highlights in the evolutionary chain. New frontiers, such as 3D stacked technology, photon-counting technology, and others, are briefly discussed.

1. INTRODUCTION

Capturing images has been a human activity since prehistoric times, and camera capture has been a part of human culture for almost 200 years. Image sensors are the microelectronic silicon chips that sit at the heart of every digital camera and convert light into electrical signals suitable for transmission, storage, and processing by computers, for use by machines and humans alike. Image sensors have strongly affected human culture starting in the twenty-first century and possibly even earlier. Digital cameras were first implemented with a charge-coupled device (CCD) image sensor, and are currently implemented with a complementary metal oxide semiconductor (CMOS) image sensor (CIS). These cameras are applied widely in mobile smartphones, automobiles, web cameras, medical devices, security systems, defense technology, and space, among many other areas. The influence, for better and worse, of image-based social media, such as Facebook, Instagram, YouTube, and TikTok, on society can hardly be understated. However, an undisputed positive influence is that a camera in every pocket has aided social justice. Examples include video of the George Floyd event; the Arab Spring; and the capitol events of January 6, 2020, as well as videos that support law enforcement statements.

This review seeks to briefly summarize and contextualize key developments in the field. To do complete justice to the field would require a several-volume book, so our intent is to provide a skeletal guide to key breakthrough publications and review papers. The guide and references are imperfect, and many interesting side developments regrettably need to be passed by in this review.

2. HISTORICAL DEVELOPMENT MILESTONES OF THE TWENTIETH CENTURY

2.1. Camera-Image Pickup Cathode Ray Tube Technology

The concept of electronic camera-image pickup using cathode ray tube (CRT) technology dates to the early 1900s, in the predawn of the television age. In the pickup CRT, a focused-electron beam is raster-scanned across a photocathode surface, which is also illuminated with a focused optical image. Electrons liberated from the photocathode due to light and the scanning beam produce a current indicative of the instantaneous light intensity on that portion of the photocathode. It was quickly realized that, if the photocathode charge could be stored or integrated over a full raster-scan cycle and realized as photoconductive gain, then significantly more detector signal could be generated, and the tube would be much more sensitive.

Many different types of video camera tubes with improved performance were introduced over the decades up until the late 1980s and even the early 1990s, before the performance benefit of solid-state image sensors was fully realized for high-quality video applications (**https://en.wikipedia.org/wiki/Video_camera_tube**).

Many ideas for the practical implementation of camera-image pickup tubes were later reimagined or reinvented for solid-state imaging devices. These include raster-scan readout; in-pixel integration of photosignal to increase the signal-to-noise ratio (SNR); color filters for implementing color reproduction; and even sizing nomenclature for the image-pickup tube diameter dimension, which has been retained to refer to image sensor chip sizes despite its inaccuracy in that context.

2.2. 1960s Solid-State Image Sensors—A Beginning

The 1960s saw the real emergence of integrated semiconductor devices, and the light sensitivity of semiconductors was well-known by then. Some early devices included a photosensitive junction device by Honeywell (Morrison 1963), a scanistor array of n-p-n photosensitive junctions by IBM

(Horton et al. 1964), and a 50 × 50–element array of phototransistors by Westinghouse (Schuster & Strull 1966). The output signal of these devices was proportional to the instantaneous optical input signal without intentional integration, and thus, the signal was weak and required gain inside of the pixel for amplification. In essence, these were the first active-pixel sensors.

The leap to integrating the instantaneous optically induced signal in the pixel was made by Weckler (1967) at Fairchild using the intrinsic capacitance of the p-n junction photodetector. Visible-light photons generate photoelectrons with some quantum efficiency, which are collected and integrated on the junction capacitance as a charge. A 100 × 100 array of such silicon photodetectors was reported by Fairchild a year later (Dyck & Weckler 1968). The charge accumulated on the capacitance was read out passively through a switched-circuit network, resulting in a current or voltage pulse at the output as each pixel was selected. Such an architecture became known as a passive-pixel sensor.

At about the same time, Noble (1968) and Chamberlain (1969) at Plessey were exploring similar devices and self-scanned silicon image detector arrays. Their readout circuitry was more sophisticated than the Fairchild work and was implemented with charge-integration amplifiers to convert charge to a voltage at readout, or with an active source-follower in each pixel to convert the charge to a gate voltage and drive a voltage output signal from each pixel as an active pixel sensor.

Compared to imaging tubes, solid-state image sensors offered the advantages of smaller size, lower weight, higher reliability, and lower camera-system power. However, by 1970, solid-state image sensors delivered inferior image quality compared to tubes due to both fixed pattern noise (FPN) (due to variations caused by the pixel itself and from the pixel readout circuitry) and lower SNR (due to temporal noise from readout and a less responsive photodetector), and there was no significant market penetration of these devices into the video or still camera space.

In 1969, the CCD was invented at Bell Labs by Smith and Boyle. The CCD image sensor was relatively free from FPN issues and had lower readout noise when combined with correlated double sampling (CDS) (White et al. 1973). These features led to worldwide research and development (R&D) on CCD image sensors, with other metal-oxide-semiconductor (MOS) and bipolar approaches being mostly abandoned, with the exception of some MOS-image sensor efforts at Hitachi, Matsushita, and Reticon. Unfortunately, these efforts were unable to produce image sensors that competed with CCDs in performance due to residual FPN and temporal noise, along with lower resolution and higher manufacturing costs for larger-pixel devices.

2.3. Charge-Coupled Devices Dominate Solid-State Image Sensors (1970s–1980s)

The development and rise of CCDs as the solid-state image sensor of choice during the 1970s and 1980s is now discussed.

2.3.1. Charge-coupled devices. A CCD is a type of semiconductor charge-transfer device, which can transfer charge packets in a semiconductor by a sequence of pulses on MOS gate electrodes that control the electrostatic potential profile in the semiconductor (**Figure 1**). Just before the CCD was proposed in 1970 (Boyle & Smith 1970), the bucket-brigade device (BBD) was reported as a charge-transfer device (Sangster & Teer 1969, Sangster 1970). However, in principle, the CCD has superior charge-transfer efficiency compared to that of the BBD, which is essential for the good performance of charge-transfer devices. CCD charge packets can be generated electrically or optically. In the former case, the CCD acts as a delay line for signal processing, and in the latter case, the CCD can be used as an image sensor. A CCD image sensor can be used as both a photodetector array and a readout device (through sequential signal transfer). However, such a

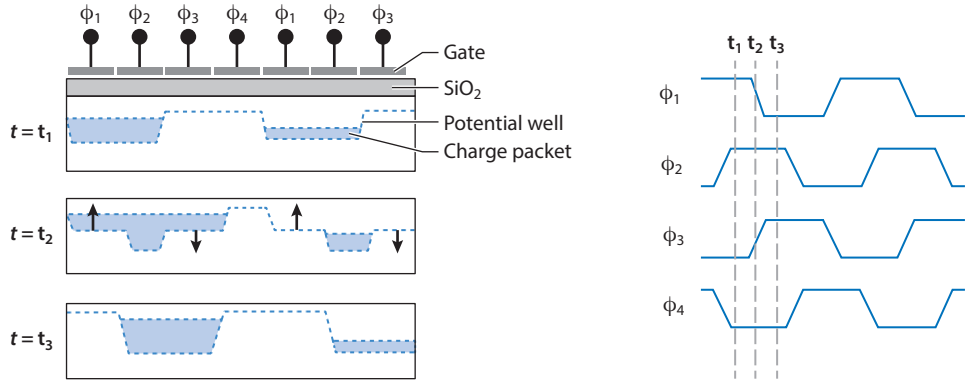

Figure 1

Illustration of a four-phase charge-coupled device diagram, a potential well diagram, and clock charts. As four clocks switch sequentially, the potential wells move rightward together with the charge packets.

full-frame CCD requires a mechanical shutter to block optical signal generation of carriers during readout to avoid smearing of the image. Therefore, the full-frame CCD was used for both digital still cameras and X-ray (burst) applications, but it was not convenient for video.

2.3.2. Frame-transfer charge-coupled device image sensor. To avoid such smear and to make a practical video camera, Tompsett and colleagues (Tompsett et al. 1971, Séquin et al. 1973) invented the frame-transfer (FT) CCD image sensor. It consists of an image area and a light-shielded (e.g., covered by metal) storage area. The FT CCD structure is relatively simple because there are only MOS capacitors, but it needs a larger chip size due to the storage area. The poly-crystalline silicon gate of the MOS capacitor absorbs light to some extent, and thus the sensitivity is limited, especially for blue light (Kosonocky & Carnes 1971). FT CCD production volume was smaller compared with the higher-performance and lower-cost interline-transfer (ILT) CCD image sensor invented a short time later.

2.3.3. Interline-transfer charge-coupled device image sensor. The ILT CCD was invented as an evolution of bilinear CCD image sensors. As shown in **Figure 2**, the ILT CCD pixel has a photodiode (PD) located between adjacent parallel shift registers (Amelio 1973, Walsh & Dyck 1973). This design allows the CCD shift registers to be covered with light-shielding material. During the exposure period, signal electrons are accumulated in the potential well at the PD. After the exposure period, the signal electrons are transferred to parallel vertical CCD (VCCD) shift registers and transferred to the output amplifier through the fast horizontal CCD shift register. The PD is used for signal-electron generation and integration, while the CCD shift registers are used only for signal-electron transfer and are covered with a light shield (e.g., metal). Therefore, the image smearing that occurred in the FT CCD is greatly reduced (Teranishi & Ishihara 1987). Since the PD charge is transferred simultaneously for all PDs, it acts like a global shutter, meaning that all pixel signals integrate simultaneously. A microlens and a color filter can be formed on top of each pixel to improve performance; these mechanisms are explained below.

At the output, the signal electrons are converted to a voltage signal by the floating diffusion amplifier (Carnes 1972). Additionally, to suppress the reset noise of the floating diffusion, CDS is applied.

CCDs initially suffered from blooming, i.e., electron overflow by a strong illumination from the PD to the VCCD and neighboring PDs. To resolve this, the lateral-overflow drain was proposed;

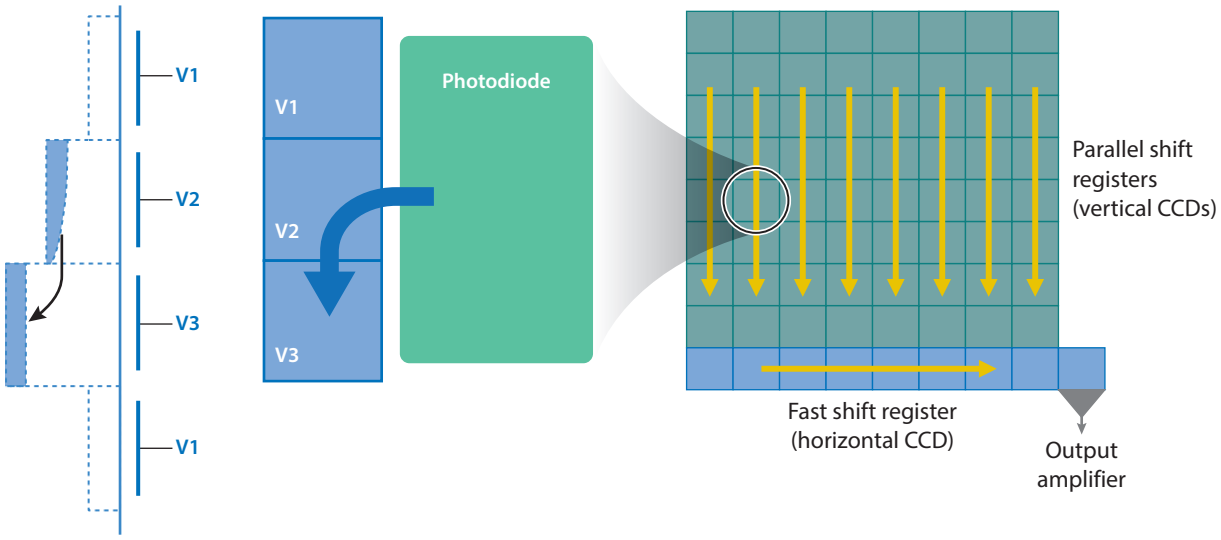

Figure 2

Illustration of a (three-phase) interline-transfer (ILT) charge-coupled device (CCD) showing (*left*) a unit cell with a photodiode (PD) and vertical CCD and (*right*) the entire ILT CCD image sensor. The photosignal moves from the PD into the vertical CCD, and then into the horizontal CCD to the sense node and output amplifier.

however, it consumes additional pixel area (Séquin 1972). To overcome this drawback, a vertical-overflow drain was invented (Ishihara et al. 1982).

2.3.4. Pinned photodiode. Pinned PD (PPD) technology (Teranishi et al. 1982, Fossum & Hondongwa 2014, Teranishi 2016) advanced CCD image sensor performance enough that CCDs successfully overtook conventional pick-up tubes. The PPD has two distinct features. The first is the p^+ pinning layer over the PD n-region, as shown in **Figure 3*a***. Although there are many generation-recombination (GR) centers at the silicon interface, the p^+ layer pins the Fermi level and prevents the interface from being depleted even when the PD n-region is completely depleted. Thus, GR centers are not active, and low dark current is achieved (Theuwissen 2006). In addition, the PD n-region storage well has larger capacitance and larger saturation because of the p-n junctions above and below it.

The second feature of the PPD is its complete charge transfer (**Figure 3*b***). The PD n-region potential, V_{dep}, when the PD n-region is completely depleted is designed to be lower than the channel potential of the transfer gate (TG) in the ON-state, V_{TG}. The potential difference, $V_{TG} - V_{dep}$, causes the driving force for electron transfer from the PD to the VCCD. The potential difference is needed especially at the final stage of the electron transfer. If there is no potential difference, some signal electrons might remain in the PD and image lag may occur.

PPD technology is used not only in ILT CCD image sensors, but also in CMOS image sensors, as described in Section 3. At present, almost all image sensors use a PPD.

2.3.5. Time delay and integration image sensor. A time delay and integration (TDI) image sensor transfers the photosignal integrating in the CCD stages at the same speed that the optical image is scanned across the surface of the image sensor, in a synchronized manner, allowing a longer effective integration time without motion blur (Barbe 1976, Farrier & Dyck 1980, Schlig 1986). TDI is important for many inspection systems, high-performance document and artwork scanning, and aerospace push-broom imaging.

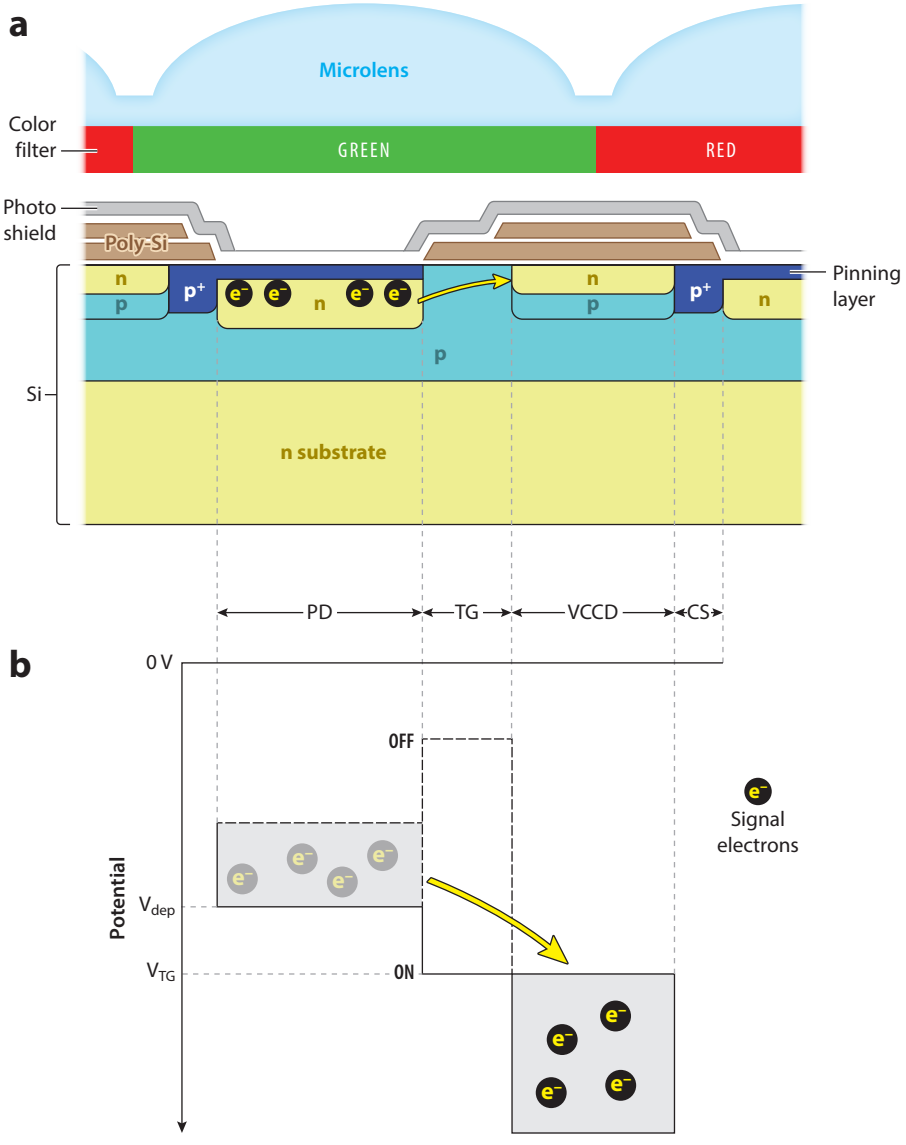

Figure 3

A pinned PD in an interline-transfer CCD with one phase of the CCD shift register (VCCD) shown. (*a*) A physical cross-section and (*b*) a potential diagram showing the electrons transferring from the PD to the VCCD. Abbreviations: CCD, charge-coupled device; CS, channel stop; PD, photodiode; TG, transfer gate; VCCD, vertical CCD.

2.3.6. Color filters and microlenses. A mosaic color filter array on an image sensor enables color signal. The most commonly used filter type for CCD image sensors and CMOS image sensors is the Bayer filter (Bayer 1976), which is a kernel comprising two green, one red, and one blue pixel filter. An on-chip color filter array was then developed (Aoki et al. 1980). Many other combinations have been explored to trade off some characteristics against others (**https://en.wikipedia.org/wiki/Color_filter_array**).

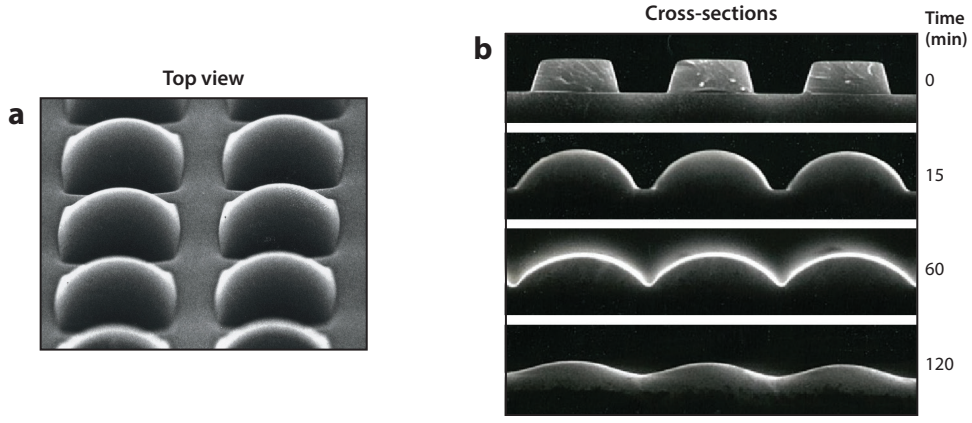

Figure 4

Microlenses to concentrate light on the photoactive area of a pixel. (*a*) Top view. (*b*) Cross-sections for different thermal-flow times. Images courtesy of NEC Corp.

To increase the effective aperture ratio and improve sensitivity, an on-chip microlens, as shown in **Figure 4**, was fabricated using resin thermal flow (Ishihara & Tanigaki 1983) that melts and rounds the resin. This method also enabled mass production. To increase the effective aperture ratio, a gapless microlens, the inner microlens, was developed (Sano et al. 1996). An additional inner lens is located nearby just above the silicon, allowing a larger numerical aperture so that light collection becomes more effective.

2.3.7. Stitching technology for large-area image sensors. Large- and/or long-image-area image sensors are sometimes required for specific applications, such as 35-mm full-size digital single-lens reflex cameras, astronomical telescopes, X-ray sensors, and linear image sensors. CCD image sensors and CMOS image sensors are fabricated using steppers and scanners for lithography. The exposure area of steppers and scanners is approximately 33 mm × 26 mm. Stitching technologies were invented to realize larger chip sizes than the maximum exposure dimensions of the lithography tool. Stitching involves using different parts of a mask to expose a large die in sequential steps, one region at a time, to build up an image layer that exceeds the single exposure area (Rominger 1988, Monma & Yuzurihara 1993, Kreider et al. 1995, Monma & Yuzurihara 1998).

When exposures are repeated sequentially, full image sensors are built up. Even very large full-wafer-size image sensors (CCD and CMOS) have been fabricated using this method (e.g., Lesser et al. 1997, Ay & Fossum 2006, Zacharias et al. 2007, Yamashita et al. 2011) (see **Figure 5**).

2.4. Some Issues with Charge-Coupled Devices (Circa 1990)

CCDs were known for their outstanding image quality, in part due to a very low leakage (or dark) current. Despite this, CCDs exhibited some problems, a few of which are briefly discussed below.

2.4.1. Charge-transfer efficiency. The basic working principle of CCDs is based on the transport of charge packets (Boyle & Smith 1970). These packets are generated in the pixel and need to be transferred to the output node, where the charge packet is converted into a voltage (or current). For example, in a 6-Mpixel CCD image sensor, in the worst case, the charge packet must undergo approximately 17,000 gate-to-gate transfers. Unfortunately, these transfers are not always perfect. Two major issues can limit the transfer efficiency: the finite time allowed for transportation

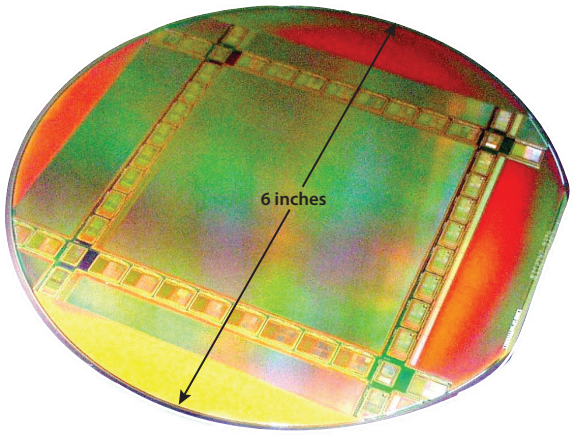

Figure 5

A 16-Mpixel stitched complementary metal oxide semiconductor image sensor on a 6-inch-diameter wafer. Figure reproduced from Ay & Fossum (2006).

and the charge trapping by surface or bulk states. If an overall charge transfer efficiency (CTE) of more than 98% is needed for 17,000 transfers, then each single charge transfer needs to be completed with an efficiency of 99.9999% ($0.999999^{17,000} \cong 0.983$), or losing 1 electron out of 1,000,000 electrons on average per transfer. The need to maintain high overall CTE gets more challenging as array sizes get larger (more transfers) or are operated at higher frame rates (less time per transfer), which results in scaling difficulties for CCDs (Theuwissen 1995).

CCDs were optimized for CTE by the introduction of an extra implantation in the CCD channel to form a buried-channel CCD (BCCD) (Walden et al. 1972). In a BCCD, the charge packets are no longer transported along the Si-SiO_2 interface, but instead in a channel located slightly deeper in the silicon. This modification results in (almost) no interaction between the charge packet and the interface states, as well as larger fringing fields to enhance the transfer speed of the charge packets. In space environments, radiation can increase surface and bulk states or traps over time, and the impact on CTE can be exacerbated by cooling the CCD to reduce dark current.

2.4.2. Readout rate. Maintaining high CTE can limit the rate at which charge packets can be transferred from one stage to the next, and increasing the clock voltages on the gates to speed charge transfer has practical limits due to silicon breakdown. CCD clocking rates reached 30–60 MHz in HDTV consumer devices, but the path to larger formats or faster frame rates was unclear, especially considering power consumption. Furthermore, increasing the output-amplifier speed also increases readout noise due to transistor white noise. A way to reduce the bandwidth requirement of the output stage is to make use of slower, parallel outputs (Lee et al. 1981), but this can introduce fixed-pattern noise issues due to offset and gain variation from output stage to output stage. On a practical basis, high-speed clocking can only be obtained by low-resistance gates and low-resistance interconnects to those gates. CCD gates equipped with tungsten straps achieve such goals, but at the cost of a complex and expensive fabrication process (Morimoto et al. 1992).

2.4.3. Power. In principle, a CCD is a collection of millions of MOS capacitors. These MOS capacitors are made by means of a poly-Si gate on top of a SiO_2(-Si_3N_4) gate dielectric. In the

previous example of the 3K × 2K pixel array, with 12-μm pixel pitch, the vertical transport phases can have a capacitance value of 2 nF/phase, while the horizontal transport phases can have a capacitance value of 150 pF/phase (Theuwissen et al. 1998). These capacitances need to be charged and discharged (e.g., for the vertical clocks between 0 V and 10 V and the horizontal clocks between 0 V and 5 V), which adds to the total energy cost. The transport-phase energy needed per frame will be [using the formula energy (E) = capacitance (C) × voltage (V^2)]

$$(2,048 \times 4 \times 2 \times 10^{-9} \times 10^2) + (2,048 \times 3,072 \times 3 \times 150 \times 10^{-12} \times 5^2) = 72\text{mJ/frame},$$

and the required clocking power is the energy per frame × frame rate. Increasing the frame rate will increase the consumed and dissipated power accordingly. It is important to note that this large amount of energy needs to be supplied through the external (off-CCD) drivers. The off-chip current-driver power requirement is even larger when considering settling time issues. The problem is exacerbated when the pixel count is increased and/or the frame rate is increased for the same size pixel.

2.4.4. Manufacturing yield. Yield, the ratio of the number of acceptable devices to the total manufactured devices, can severely impact manufacturing cost and profitability. Much effort is expended in semiconductor fabrication plants to maximize yield. The fabrication process and design are tuned over many manufactured parts to optimize yield. Compared to other electronics, CCDs were made both using an unusual process and at a relatively low volume. Both factors can negatively impact yield. Furthermore, the cost of fabrication equipment needs to be amortized over the volume of parts that are manufactured. Lower volume also increases amortization costs.

One source of less-than-perfect yield was the structures needed to ensure high CTE. To allow a smooth and efficient transport of charge packets, the MOS capacitors need to be closely spaced, and the gap between two neighboring capacitors needs to be as small as possible, preferably smaller than 0.25 μm. Larger gaps between the gates will introduce potential barriers that can hamper the charge transfer. At the time when CCDs were the first image sensor choice, it was not possible to etch gaps of 0.25 μm in a poly-Si layer of 0.5-μm thickness. For that reason, multiple poly-Si layers were used such that overlapping MOS capacitors could be realized. This resulted in a capacitor-to-capacitor gap with the thickness of the isolation layer on top of the poly-Si gate, typically 0.2 μm. Most CCDs use a triple poly-Si technology. Etching a first poly-Si layer is relatively easy, and in a four-phase transport system, phase 1 and phase 3 could be made out of this first poly-Si layer. Phase 2 would use the second poly-Si layer, and phase 4 would use the third poly-Si layer. In this way, only one phase is made in the second and third poly-Si layers. This is very beneficial for the manufacturing yield. Etching an overlapping poly-Si layer is not easy and can give rise to shorts. This can have a negative effect on the fabrication yield and, consequently, on the cost of the devices.

Additional issues can deteriorate the image quality, such as defective pixels, defective columns, fixed-pattern noise, dark current, and photoresponse nonuniformities. All of these factors could result in a non-yielding device. Currently, some of these issues can be corrected and hidden from the output image, but, taking all of the aforementioned issues into account, it should not be surprising that the manufacturing yield of CCDs was not high, thus making the CCD a relatively expensive device.

2.4.5. Integration. The CCD manufacturing technology was optimized primarily to fabricate high-quality image sensors. The focus in CCD process developments was on dark current reduction, yield optimization, and imaging performance. The CCD fabrication recipe was not well suited for the integration of additional electronics. Among a few others, Philips tried to implement CMOS peripheral circuitry on a CCD chip (Theuwissen et al. 1984). However, the CCD

design rules on one side did not match the CMOS design rules on the other. The CMOS part occupied too much space, which made the CCD chip unnecessarily large and (with the limited yield of the CCD part) too expensive. However, the Philips trial could be seen as a first attempt to create a standalone imager without the need for external peripheral driving circuitry (Theuwissen et al. 1985). The CCD technology can be seen as a special, dedicated technology developed and optimized for imaging with, coincidently, the option to implement some MOS transistors needed for the readout part of the imager. The invention of the CIS was partially predicated on answering the question of how to make a good image sensor with mainstream microelectronics technology.

2.5. Complementary Metal-Oxide Semiconductor Image Sensors (1990s)

The invention and development of the CIS in the 1990s are now discussed.

2.5.1. Brief history. By 1990, CCDs were firmly entrenched as the technology of choice for nearly all camera applications. Nearly all CCD design and production occurred in Japan, with companies such as Sony, Matsushita (Panasonic), Toshiba, Sharp, and NEC dominating CCD technology. Non-Japanese companies were few and included Philips, Thomson CSF, Kodak, and Texas Instruments. Additionally, there were some very-low-volume specialty companies such as Ford Aerospace, Tektronix, English Electric Valve, and others in the defense and aerospace arena. CCD-based cameras were relatively large and consumed significant power. CCD camcorders, for example, were bulky, and the brick-sized batteries lasted only 30 minutes or so. Space-borne scientific cameras were the size of a small refrigerator, had significant mass, and used substantial spacecraft power resources.

In the early 1990s, two separate efforts led to a resurgence in non-CCD image sensors using the CMOS technology platform. In fact, the efforts were probably unaware of each other at the time. The first involved creating highly functional single-chip imaging systems, with low cost as the primary concern. This effort had roots at two separate universities. At the University of Edinburgh in Scotland, a research group led by Denyer and Renshaw eventually spun out VLSI Vision, Ltd. (VVL), which produced inexpensive, lower-performance single-chip cameras for toys (e.g., the Barbie-Cam and the Intel Microscope) and other applications based on a passive pixel architecture. Another was rooted at Linköping University in Sweden, which spun out Integrated Vision Products (IVP), focused primarily on machine vision applications. IVP also employed a passive pixel architecture but also utilized the first column-parallel analog-to-digital converters (ADCs). The VVL and IVP passive pixel approaches were quite similar to the passive pixel approaches proposed by Weckler and Noble 25 years earlier but were aided by additional innovations and improvements in technology, such as the development of CMOS, which overtook n-channel metal-oxide-semiconductor (nMOS) technology in the 1980s (Fossum 1997).

2.5.2. Intrapixel charge transfer. The second effort stemmed from NASA's need for highly miniaturized, low-power, high-performance instrument imaging systems for next-generation interplanetary exploration and was led by the Jet Propulsion Laboratory (JPL) at Caltech in the United States (Fossum 2013a). This effort resulted in the invention of the CMOS active-pixel image sensor with intrapixel charge transfer and represented the opposite end of the performance spectrum compared to the focus of VVL and IVP. The first JPL device was demonstrated in 1993 (Mendis et al. 1994) and was soon integrated into a larger array (Mendis et al. 1997). A low-voltage PPD was developed in a JPL–Kodak collaboration (Lee et al. 1995). This invention built on the pixel elements of the CCD that made it work well, including complete charge transfer to eliminate lag and transfer noise, the PPD for high quantum efficiency, the floating-diffusion amplifier, and the enablement of CDS. Furthermore, it added additional circuits to suppress fixed-pattern

noise and provide other noise reduction. Essentially, the pixel was a single-stage micro-CCD including an output amplifier per pixel. Compared to CCDs with thousands of stages, an array of single-stage CCDs, each with its own output amplifier, eliminated the need for a 99.9999% CTE CCD structure. It could thus be implemented in a CMOS technology platform with low operating voltages and be more scalable to higher-resolution imaging and faster readout speeds. Intrapixel charge transfer is used in nearly all CIS devices today.

Intrapixel charge transfer meant that CDS could be used to suppress reset (also known as kTC) noise, just like in a CCD. The use of the CMOS technology platform meant that integration of CMOS circuits for timing, control, analog signal processing (ASP), ADC, and digital signal processing (DSP) would be relatively easy to implement and manufacture (Fossum 1993, 1997). The initial camera chips were all frontside illuminated (FSI). The major drawback of this approach was that the extra components within each pixel meant that the actual photosensitive area was relatively smaller than that of a CCD. However, just as in ILT CCDs, microlenses could help increase the effective pixel fill factor. Backside illumination was also recognized as a solution to the small photosensitive area, but at that time, it had only been used for low-volume, high-cost scientific CCDs (Fossum 1994). Backside-illuminated (BSI) CMOS image sensors eventually became mass produced when pixel shrinkage required pixels with a high fill factor that could gather more light (Rhodes et al. 2009).

A simplified block diagram of a generalized monolithic CIS is shown in **Figure 6*a***. The major blocks are (*a*) timing and control, including selection logic; (*b*) pixel array; (*c*) ASP; and (*d*) analog-to-digital conversion. Not shown is (*e*) DSP, including the image signal processing (ISP) block,

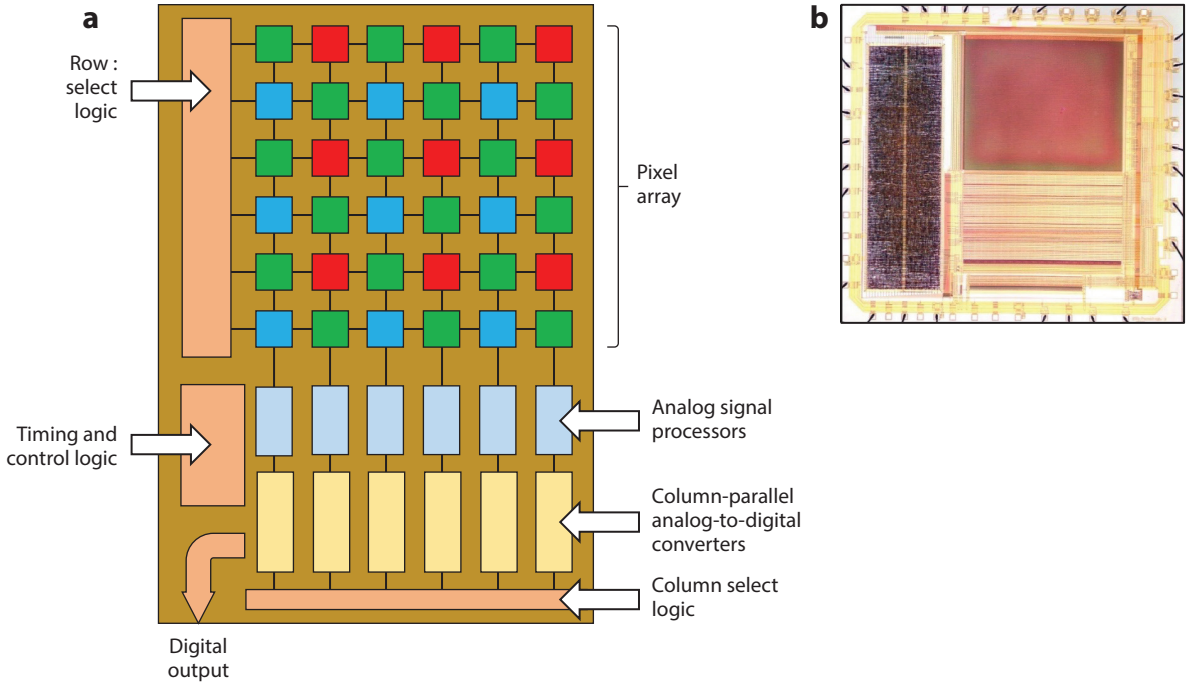

Figure 6

(*a*) Complementary metal oxide semiconductor (CMOS) image sensor block diagram. (*b*) Photograph of early Photobit CMOS image sensor chip for webcams. (*Left*) Digital logic for control and input-output (I/O) functions. (*Top right*) The pixel array. (*Bottom right*) The column-parallel analog signal processing and analog-to-digital converter (ADC) circuits. Photo courtesy of E.R.F.

which would be after the ADC digital output if included on-chip as a system-on-a-chip. An early webcam image sensor produced by the JPL spinoff Photobit is shown in **Figure 6*b***. More recent 3D stacked BSI CMOS image sensors might have pixels on one wafer layer and ASP, ADC, or digital logic on another wafer layer, with each wafer level fabricated in a specialized process (Oike 2022). Such stacking that includes more than two layers will enable new functions and improved performance of CMOS image sensors.

2.5.3. Pixel array. Many different types of CIS pixels have been explored over the years, but the most commonly used is the active pixel with intrapixel charge transfer that uses the PPD as the photodetection element (Lee et al. 1995, Guidash et al. 1997, Inoue et al. 1999, Yonemoto et al. 2000, Fossum & Hondongwa 2014). Because it requires four transistors in the general case, this pixel is often referred to as a 4-T pixel. Sharing some transistors and their function between adjacent pixels can reduce the average number of transistors per pixel to a number lower than four, even though the basic idea remains the same (McGrath et al. 2005).

A schematic of a 4-T pixel is shown in **Figure 7*a***. Photons strike the PPD and generate electron–hole pairs. Electrons are collected in the n-region of the PPD, as shown in **Figure 7*b***. For readout, the Select (SEL) transistor is selected, and the Reset (RST) gate is pulsed to reset the n^+ floating-diffusion (FD) sense node. The voltage on FD is then sensed by the source follower

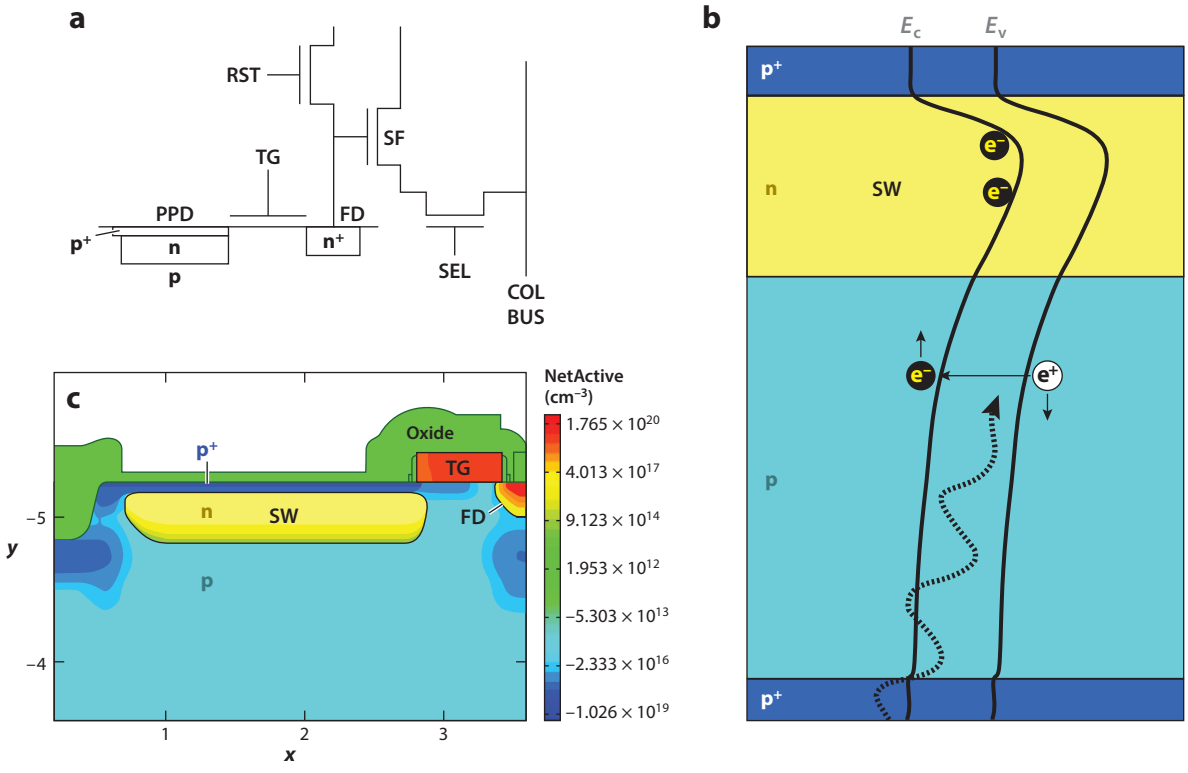

Figure 7

An illustrative PPD 4-T active pixel with intrapixel charge transfer. (*a*) A circuit schematic (Fossum & Hondongwa 2014). (*b*) A band diagram looking vertically through the PPD showing the photon, electron–hole pair, and SW. (*c*) A physical cross-section showing doping levels (Fossum 2023). Abbreviations: COL BUS, column bus line; FD, floating diffusion; PPD, pinned photodiode; RST, reset gate; SEL, select gate; SF, source-follower; SW, storage well; TG, transfer gate.

(SF) and driven onto the column bus to the ASP as the reset voltage. The TG is then pulsed, causing all of the electrons in the PPD to transfer to the FD and reduce its voltage by an amount proportional to the number of electrons, called the conversion gain (CG), in volts/electron, which is essentially the reciprocal of the total sense node capacitance. The new voltage on the FD is sensed by the SF and driven onto the column bus as the signal voltage. Using CDS, a voltage difference between the reset voltage and the signal voltage is created that is proportional to the number of photoelectrons integrated by the PPD, with FD reset noise, some 1/f noise from the SF, and the threshold voltage variation of the SF all suppressed. An illustrative cross-section of most of the pixel is shown in **Figure 7*c***.

In FSI pixels, optical elements above the pixel can help increase light-gathering capability and reduce crosstalk (Teranishi et al. 2012). In a BSI pixel, the sensor silicon wafer is mounted on a silicon carrier wafer, and the back of the sensor wafer is thinned and polished to a thickness of less than 10 μm and processed for passivation and optical properties, increasing the pixel factor to nearly 100% for improved quantum efficiency and low-light detection. The rest of the pixel structure remains similar to that described above, with the difference being that the light enters from the very-high-fill-factor backside instead of the frontside of the image sensor chip (Wuu et al. 2022).

The dynamic range of the pixel is determined by two factors: the readout noise of the pixel and the maximum (linear) charge storage capacity or readout capacity of the pixel. The input-referred readout noise, measured as a root-mean-square (r.m.s.) value, is typically 2–5 e^- r.m.s., and the noise is often dominated by the additive SF transistor noise in the pixel. Higher CG helps overcome the additive noise from the SF transistor and reduce input-referred read noise, thus improving low-light imaging performance (e.g., Venezia et al. 2018). Deep subelectron read noise (or noise less than 0.5 e^- r.m.s.) is expected in commercial devices within a few years and has already been demonstrated in R&D.

The charge-storage capacity depends on the physical design of the PPD, including doping concentrations, operating voltages, and the area and perimeter of the PPD. The readout capacity depends also on operating voltage and the capacitance of the sense node. Usually, the charge-storage capacity and readout capacity are matched. In a dual-CG pixel, often used for photography applications, an explicit extra capacitance in the pixel can be switched in to increase the readout capacity above the designed sense-node capacitance. Thus, one can choose (for the entire pixel array, typically) the CG to account for either low-light conditions or brighter illumination conditions and still maintain good SNR. A high dynamic range can also be achieved by combining different integration times (Yadid-Pecht & Fossum 1997).

2.5.4. Analog signal processing. The ASP typically performs CDS and programmable gain to improve SNR. Implementation of the ASP in a column-parallel configuration is challenging due to extreme circuit area constraints. Thus, there has been an excessive growth in the height of the ASP footprint to compensate for narrow width constraints. Some sharing of circuit elements between adjacent columns is used to ease these constraints. The overriding commandment in the design of the ASP is to not increase the input-referred read noise of the pixels. The programmable-gain amplifier helps achieve this goal by elevating the signal above the noise introduced by subsequent stages of the switched capacitor circuits. Recently, some parts of the ASP have been performed in the digital domain after the ADC (e.g., CDS and correlated multiple sampling).

2.5.5. Analog-to-digital converter. **Figure 6** illustrates a column-parallel ADC architecture that was adopted due to its lower power requirements compared to a high-speed global serial ADC, since the bandwidth of each of n ADCs is reduced by a factor of n, and the power is reduced superlinearly with n when settling time is considered (Jansson et al. 1993, Zhou et al. 1997). There

are many architectural approaches to on-chip ADC, including global; column-parallel (Kawahito 2018); pixel-parallel (Yang et al. 1999, Kleinfelder et al. 2001, Sakakibara et al. 2018); and, for 3D stacked structures, cluster-parallel (Masoodian et al. 2017) approaches. Furthermore, the type of ADC could be algorithmic, as in sigma-delta, successive approximation, and cyclic ADCs, or nonalgorithmic, as in single-slope and flash ADCs; all of these types have their own tradeoffs (Pain & Fossum 1994).

Today, on-chip ADC in a CIS is quite ubiquitous, but when the modern CIS was introduced by JPL, conventional wisdom stemming from the days of CCDs was that on-chip ADCs were undesirable due to the extra power dissipation and heating and the possible introduction of noise from the ADC into the analog pixel readout. In fact, when considering the power required to drive high-fidelity analog signals off the chip at high frequency, there may be a power advantage to doing analog-to-digital conversion on-chip. However, more importantly, on-chip ADCs open the door to on-chip DSP of the image and additional digital noise-reduction techniques and image quality improvements. Parallelism in the ASPs and ADCs can also reduce readout noise due to reduced transistor operating frequencies compared to CCDs. Column-parallel ADCs continue to be used in most sensors, with single-slope ADCs being preferred due to their chip-area efficiency and the fact that they have the fewest conversion artifacts, although they require the highest bandwidth comparators. For stacked structures, pixel-parallel and cluster-parallel ADCs are becoming popular. Improvement of the on-chip ADC continues to be an active area of research.

2.5.6. Digital signal processing/image signal processing. Additional DSP/ISP is used to perform many on-chip functions, including color signal processing (e.g., interpolation, white balance) and, depending on the application, functions such as image compression and signal formatting to meet communication standards. Additional functions could include recognition of faces or smiles or ensuring the security of the image data. Since the invention of the CIS, partitioning the imaging system for image capture and ISP has sometimes resulted in two-chip (or more) solutions. Since the ISP is highly application dependent, and well understood by the vision science community, additional information about it is not included in this review. However, the transfer of digital information off the image sensor chip to additional processors is often one of the most serious bottlenecks for future expansion of imaging capabilities, especially at high resolution and high frame rate. The use of 3D stacked image sensor technology with 3D interconnects for parallel transfer of data from the image sensor chip to a signal processing chip offers some relief for this problem.

3. TWENTY-FIRST-CENTURY ADVANCEMENTS

In the early 2000s, CMOS image sensors were very well-suited for the large, emerging camera-phone and smartphone market due to their power, size, and cost, and this drove the adoption and evolution of the CIS technology up until the present time. Smartphones were the killer application for CIS, meaning the low power and small form factor made them uniquely suitable for this high-volume application. Smartphone applications of CIS took the wind out of CCD evolution while supercharging CIS development. For example, in 2015, Sony announced the end of CCD production. CCDs continue to be used for a shrinking list of niche applications and represent a very small fraction of the total image sensor market share. Today, approximately 5-7 billion CMOS image sensors are manufactured each year; most are used for smartphones, and the rest are used in automotive, security, webcam, medical, and other applications. In 2021, the NASA Perseverance rover landed on Mars with approximately 20 CMOS cameras on board, fulfilling the promise of the early development of CMOS technology at the NASA JPL (Fossum 2023).

3.1. Manufacturing Advancements

In the intervening time between the advent of modern CMOS image sensors and today, additional manufacture advancements have further improved CIS performance.

3.1.1. Mass production of backside-illuminated image sensors. Since cameras have been installed in mobile phones and smartphones, the demand for small, high-resolution cameras has become high, and it has been necessary to further shrink the pixel size, reducing the light collection of the pixel for a given lens F-number. Backside illumination has been adopted from scientific use to allow for the shrinking of the pixel size without sacrificing the PD area ratio (Iwabuchi et al. 2006, Rhodes et al. 2009, Wuu et al. 2009). At present, many CMOS image sensors use the BSI scheme. **Figure 8** illustrates both FSI and BSI pixel cross-sections. The merits of backside illumination are its large fill-factor, the small stack height from the silicon to the microlens, and the freedom in the choice of the number of metal layers and metal layout. Thus, the pixel sensitivity is much improved.

The process of creating a BSI image sensor is as follows: (1) the frontside process, including wiring; (2) wafer bonding to a support wafer by direct bonding; (3) sensor wafer thinning; (4) backside treatment to suppress the dark current; (5) antireflection coating; (6) color filter application; (7) microlens application; and (8) bonding-pad opening. In the second step, both the sensor wafer and support wafer are flattened and cleaned; the surface is activated by plasma; and finally, both wafers are contacted and annealed. In the third step, to get accurate and uniform thickness in the final stage of the thinning process, chemical-mechanical polishing is adopted.

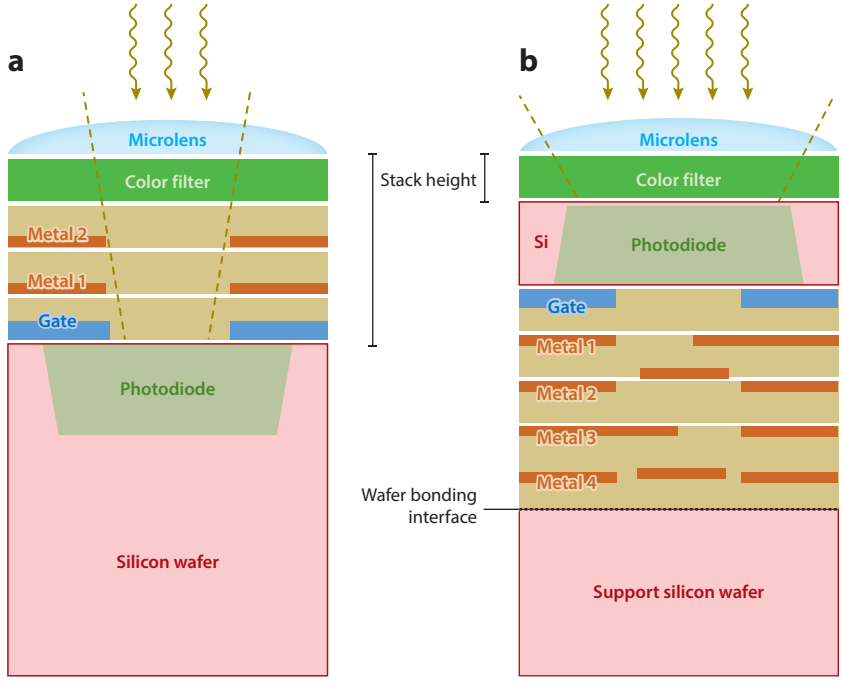

Figure 8

Illustrative example of (*a*) a frontside-illuminated pixel and (*b*) a backside-illuminated (BSI) pixel showing the better light gathering capability of the BSI pixel.

3.1.2. Deep trench isolation. The smallest pixel size possible today is approximately 0.5 μm, and the smallest practical silicon thickness for good visible-light absorption is approximately 4 μm. Thus, the aspect ratio of pixel size to silicon thickness is as large as 8, which causes both optical crosstalk and electron diffusion crosstalk. To reduce crosstalk, deep trench isolation (DTI) has been introduced (Park et al. 2007). Dielectric, polysilicon, and tungsten can be buried in the DTI. Electron diffusion crosstalk is blocked by the DTI. Metal-filled DTI perfectly suppresses the optical crosstalk, while DTI with dielectric and polysilicon reduces it to some extent.

DTI adopts the Bosch process for high-aspect trench etching (Roozeboom et al. 2015). To suppress dark current from the DTI interface, three approaches are applied. The first is to form the p^+ layer at the DTI surface by boron plasma doping (Moon et al. 2007). Many materials can be used as filler in this case. The second is to bury negatively charged dielectric material, which attracts holes to the interface. The third is to form a thin dielectric layer on the surface, which works as a gate dielectric, and to deposit polysilicon or tungsten as the gate. A negative bias is applied to the polysilicon or metal to accumulate holes (Kitamura et al. 2012, Ahn et al. 2014).

3.1.3. 3D stacking technology. 3D stacking technology allows functions including image processing to be integrated in CMOS image sensors to achieve small, high-performance smart cameras. The logic circuit wafer is a Cu-Cu hybrid bonded onto the image sensor wafer (Sukegawa et al. 2013, Oike 2022) (**Figure 9**). The two wafers are adhered physically by both SiO_2-SiO_2 and Cu-Cu and electrically connected at the peripheral area and/or pixel area (Kagawa et al. 2016). Appropriate fine process technology is applied to the logic wafer to achieve high-speed operation with low-power dissipation for various functions. A three-layer stack, consisting of an image sensor wafer, dynamic random access memory (DRAM) wafer, and logic wafer, was developed using through-silicon vias for electrical connections between the wafers (Haruta et al. 2017). The DRAM is connected, with a large bandwidth, to the image processor in the logic wafer.

3.2. Application-Specific Advancements

The list of potential applications of modern solid-state image sensors seems endless. Even today, new applications are being created almost daily. Although mobile imaging, to a large extent, drives

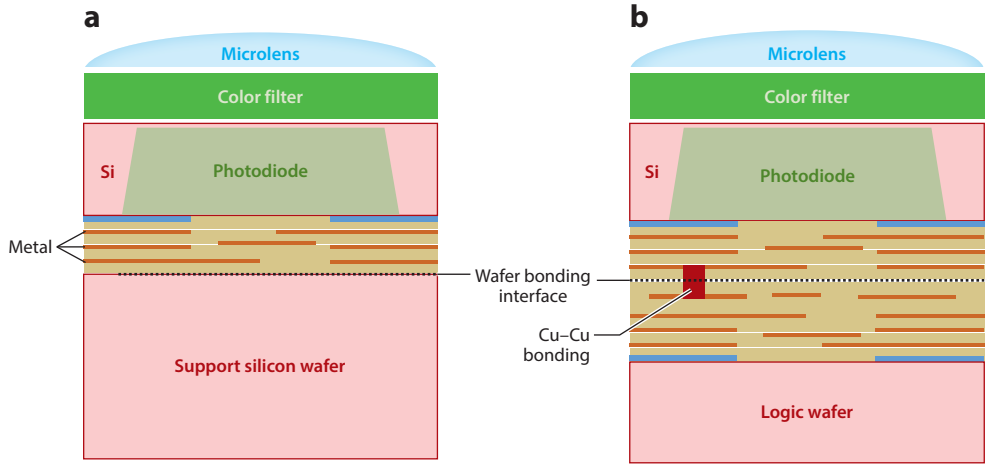

Figure 9

Illustrative cross-sectional comparison of (*a*) a backside-illuminated device and (*b*) 3D stacked image sensors where the lower layer is used for additional circuitry.

the technology of the CIS business, several specific applications require a dedicated design, layout, or fabrication technology for the devices that is different from the one applied for mobile imaging sensors. A few of these applications are discussed in this section.

3.2.1. Automotive high dynamic range. Business-wise, the automotive industry is one of the most promising upcoming and growing markets for CIS systems. While some performance parameters are not relevant for the automotive application, a key requirement is a high dynamic range. Consumer devices without special consideration can yield a dynamic range of up to 80–90 dB, but automotive imaging requires a minimum dynamic range of 120 dB. Several techniques are reported in the technical literature to increase the dynamic range of a CIS, but some of them suffer from motion artifacts, which need to be avoided for autonomous driving cars.

Another important issue in the automotive world is the demand for imaging parts that are insensitive to the LED flicker present in the light sources of cars and traffic signs. To mitigate LED flicker, sophisticated approaches are required (Takayanagi & Kuroda 2012).

An image sensor that can cope with the LED flicker, as well as creating a wide-dynamic-range output signal without motion artifacts, was announced by ST Microelectronics (Tournier et al. 2018). The device makes use of two PDs with chopped exposures. The first PD makes use of multiple long exposure times, and the photo-generated charges are accumulated on the first storage capacitor. The second PD relies on multiple shorter exposure times of which the photo-generated charges are accumulated on the second storage capacitor. The multiple long and multiple short exposure times are interleaved, such that the final result is a combination of both. This combination is characterized by a wide dynamic range without motion artifacts and without LED flicker issues.

3.2.2. Medical and capsule endoscopy. A typical requirement for endoscopes is a small form factor because the camera needs to pass through tiny openings in the human body. Image sensors with a small footprint can be realized by extended integration of the electronic circuits on a single piece of silicon with a minimum number of leads to the outside of the chip. For these types of applications, devices with no more than four I/O pins are required. These devices were available in the days of the CCDs, but the complete peripheral circuits for driving and reading out the CCD were not integrated on the chip; instead, they were located outside of the human body and attached by wires.

In the extreme case of capsule endoscopy, the pill camera is swallowed by the patient and passes through the complete gastroenterological channel (Iddan & Swain 2003). This means that not just the sensor with its ISP, but also the lens, light source, battery, and RF-transmission electronics (to transmit one frame every 8 seconds to the outside world), need to be inside of the capsule. Furthermore, the entire system has to be able to operate for many hours with a small, self-contained battery. A custom, very-low-power CIS was developed and produced by Photobit. This is an extreme and important example of the miniaturization achievable by using CMOS image sensors integrated along with other CMOS electronic components.

3.2.3. High speed. On-chip integration, in combination with stacking technology, is ideally suited for high-speed applications, as one can make optimum use of processing and handling signals in parallel. For instance, switching from a global ADC to a column-level ADC can increase the maximum frame rate of an image sensor, since the time-consuming conversion of a serial global ADC is reduced by the parallelism of column-level conversion. Note that one ADC can also serve multiple columns (Chen et al. 1990). Switching from a column-level ADC to a pixel-level ADC can further increase the maximum frame rate of the devices (Kleinfelder et al. 2001). In addition to the conversion time of the ADCs, which can be a limiting factor as far as speed is concerned,

another very important time constraint is set by getting all of the generated bits off-chip. Parallelism will be needed to output the digital code of multiple pixels at the same time. This will increase the number of pins on the package of the device and will increase the package cost accordingly. In some cases, the cost of packaging can be larger than the cost of the bare die.

From this discussion, the conclusion can be formulated that a pixel-level ADC would be the preferred choice for high-speed image sensors. However, having an ADC in every pixel will drastically lower the fill factor of the pixels. This problem can be overcome by switching to a stacked solution; the top layer will contain the image-sensing part, while the bottom layer will contain the ADCs (Takahashi et al. 2018). Image sensors with over 100-Mfps (burst mode) performance have been achieved with a specialized 3D stacked architecture (Kuroda et al. 2019).

3.2.4. Scientific imaging. The world of scientific imaging is extremely broad and includes many niche markets, e.g., space applications, astronomy imaging, high-energetic particle detection, and electron detection for scanning and transmission electron-beam microscope applications (SEM and TEM). A common parameter that plays an important role in all of these applications is the stringent requirement for low-noise performance. Noise not only determines the SNR and the dynamic range of an image sensor, but also defines the minimum input signal needed to make an acceptable output result.

Research on noise reduction started from the moment the very first CCDs were fabricated and is still a hot topic in the CIS community. Besides the introduction of new steps in the production process (e.g., optimized oxidation processes, dark current reduction steps), a lot of attention went to the design and layout of the pixels (e.g., PPDs, vertical TGs, passivation layers) and analog circuitry (e.g., CDS in the charge domain, correlated multiple sampling) (Chen et al. 2012, Ge & Theuwissen 2017). Once the read noise level is at 0.3 e^- r.m.s., or even as low as 0.15 e^- r.m.s., the electron number can be determined with good or excellent accuracy (Teranishi 2012, Fossum 2013b). In the early days of CMOS image sensors, noise levels of 40 e^- r.m.s. were not uncommon. These days, average read noise values below 0.20 e^- r.m.s. are being reported for room-temperature operation (Ma et al. 2021a, 2022a), enabling ultra-low-light imaging applications.

3.2.5. Dynamic vision sensors. In machine-vision video applications, a huge series of images are captured per unit of time. In many cases, these images contain a lot of information that does not change from image to image. However, independently of the image content, each frame generated by the sensors needs to be read out. In dynamic vision sensors (DVSs), the presence of redundant information from frame to frame is used to speed up the devices and/or to reduce the amount of output data. The concept of the DVS is relatively simple: Only variations between two consecutive images are presented at the output of the devices (Dickinson et al. 1995, Delbrück et al. 2010). Every pixel captures the information during the exposure time and compares the result with the output obtained during the previous exposure time. If there is no variation between two consecutive exposure times, then the pixel does not send out any information. If there is a variation (more than a particular threshold value) between two consecutive images, then the pixel becomes active and reports its location, the time at which the variation was noticed, and whether the difference between the two frames was positive (growing signal) or negative (decreasing signal). In other words, the pixel detects a variation in contrast from frame to frame. In most cases, pixels with a logarithmic response are used.

The output of a DVS is not a good-looking, nice image, but rather a stream of digital information indicating at which location and at which point in time a negative or positive change in light intensity was observed. Recently, there has been a trend of combining a DVS with a standard

RGB CMOS sensor; the output of the DVS device can be used to correct motion artifacts in the RGB data (Guo et al. 2023, Kodama et al. 2023).

3.2.6. Indirect time of flight ranging image sensors. Indirect time of flight (iToF) image sensors are being used to measure the 3D dimension (or distances) by means of a 2D imaging system. A near-infrared light pulse (e.g., with 50% duty cycle) is emitted by a light source, and the sensor tries to detect the returning light signal after the light pulse is reflected on an object. The distance between the camera and the object can be calculated using a simple calculation. The calculation is based on the ratio between the measurement of the amount of light that is detected by the sensor during the ON phase of the light source and the measurement of the amount of light that is detected by the sensor during the OFF phase of the light source (Kim et al. 2010). The shorter the distance between the camera and the object, the more signal will be collected during the ON phase. The longer the distance between the camera and the object, the more signal will be collected during the OFF phase. Because the speed of the light is very fast, the switch between the ON and OFF phases in the pixels needs to be fast as well. Pixels are operated with exposure times in the nanosecond range. Because the signals collected in these short exposure times will be very small, multiple measurements are accumulated in the pixels and are stored on an in-pixel capacitor (Kawahito 2021).

The operation mode of the iToF pixels requires a high-speed collection of photo-generated electrons, as well as an ultrafast transport of the charge packets from the PPDs toward the storage nodes. Extra drift fields (created by means of clever designs and layouts) are an absolute must to operate these pixels at modulation frequencies in the order of several hundreds of megahertz (Xu et al. 2016).

3.3. Quanta Image Sensors

A different approach for image sensors was proposed in 2005 in which single photons would be detected and counted by a large number of specialized yet tiny pixels (called jots) operating at a high frame rate (Fossum 2005).[1] Detection would be essentially binary: either 0 for no photon or 1 for a photon. Multiple frames of binary data could be used to recreate a gray-scale image, as illustrated in **Figure 10**. Single-photon sensitivity meant that one could image in the dimmest possible light. Initially called a digital-film sensor, the concept was later renamed a quanta image sensor (QIS) and extended to multibit operation (Fossum et al. 2016).

3.3.1. Quanta image sensor implementation using single-photon avalanche detectors. Single-photon avalanche detector (SPAD) devices, which are sensitive to single photons due to their use of high electric fields and impact ionization for carrier gain, have been in development for approximately 26 years, with rapid progress made recently. Using SPAD arrays, groups have begun to demonstrate the QIS concept and prove the imaging characteristics model (Dutton et al. 2015). In 2021, a 3.2-Mpixel SPAD array was reported for the first time with a 6.4-μm pixel pitch (Morimoto et al. 2021). Since the SPAD relies on avalanche multiplication for signal gain, it requires high internal electric fields and relatively large spacing between pixels to ensure isolation, and it may also typically have high dark count rates (dark current). Despite these issues, SPADs have been proven very useful for fast-photon-arrival timing applications such as 3D imaging. SPAD technology has also been exploiting technologies used for CMOS image sensors, such as 3D stacking (Ito et al. 2020) and low dark current structures.

[1]The text of Section 3.3 was adapted from Fossum (2023).

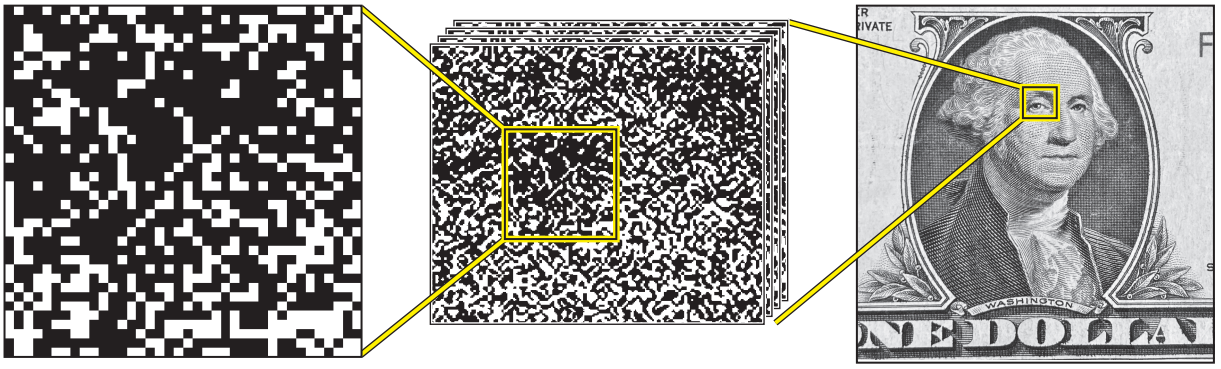

Figure 10

Quanta image sensor concept showing the spatial distribution of jot outputs (*left*), an expanded view of jot output bit planes at different time slices (*center*), and gray-scale image pixels formed from spatiotemporal neighborhoods of jots (*right*). Figure adapted from Ma et al. (2022a).

3.3.2. Complementary metal oxide semiconductor quanta image sensor. Work on realizing a CMOS QIS began at Dartmouth in 2012. At that time, a SPAD approach was rejected because SPAD pixels were very large, required high voltages, and had high dark current rates. Instead of using avalanche gain to detect single photoelectrons, the gain comes from using a very small sense-node capacitance yielding CG in the range of 300–500 $\mu V/e^-$. With intrapixel charge transfer, a single electron transferred to that capacitance can produce a discernible signal that is well above the input-referred noise floor (e.g., 0.2 e^- r.m.s. noise floor) and thus give a low error rate for detection of single photoelectrons. The detection process is slower than that for SPADs, although submicrosecond timing is achievable. Since the CMOS QIS does not need the high electric fields of SPADs, it enables smaller pixels or jots, as well as improved manufacturability, and thus enables lower cost per pixel and smaller optics. Power dissipation is also considerably smaller. The pump-gate jot device is illustrated in **Figure 11**. Experimental verification of room-temperature photoelectron-number resolution is presented in **Figure 12**.

In 2017, Dartmouth reported a room-temperature 1-Mpixel QIS device implemented in a nearly standard BSI CIS 3D stacked process with 1.1-μm pixel pitch, operating at 1,000 fps and dissipating approximately 20 mW of total power (Ma et al. 2017). The 1-Mpixel QIS was demonstrated more than two years earlier than the first 1-Mpixel SPAD array and with much smaller pixels. Approximately 34 CMOS QIS 1.1-μm pixels can fit into the area of one SPAD 6.4-μm pixel. Recently, CMOS image sensors that use QIS photon-counting technology have achieved high dynamic range and 163-Mpixel resolution (Ma et al. 2021b, 2022b). The applications of QIS technology are currently being explored and include low-light imaging for security, defense, science, and other applications. Both CIS QIS technology and SPAD QIS technology occupy important application areas (Ma et al. 2022a) and have inspired computational imaging research in the area of low-light image and video capture (e.g., ICCP 2023).

4. NEW FRONTIERS FOR SOLID-STATE IMAGE SENSORS

In this section, we discuss some emerging technologies that have caught the interest of the image sensor community.

3D stacking has enabled increased integration of sensors, allowing high-density focal-plane image processing and increasing throughput while reducing system power (Fossum 1989).

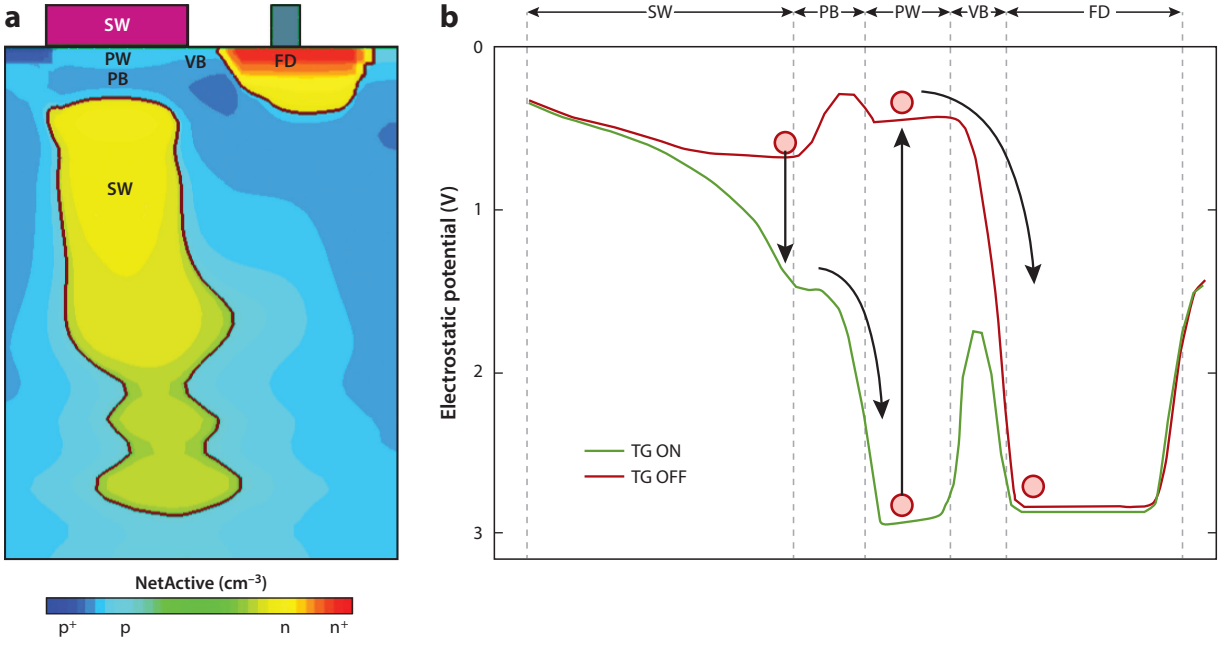

Figure 11

Pump-gate jot device with ultralow sense-node capacitance. (*a*) Cross-section of BSI pixel. (*b*) Electrostatic potential along the intrapixel charge transfer path. Panel adapted from Ma & Fossum (2015). Abbreviations: BSI, backside illuminated; FD, floating diffusion; PB, p-type bulk Si; PW, p-type well; SW, storage well; TG, transfer gate; VB, virtual barrier.

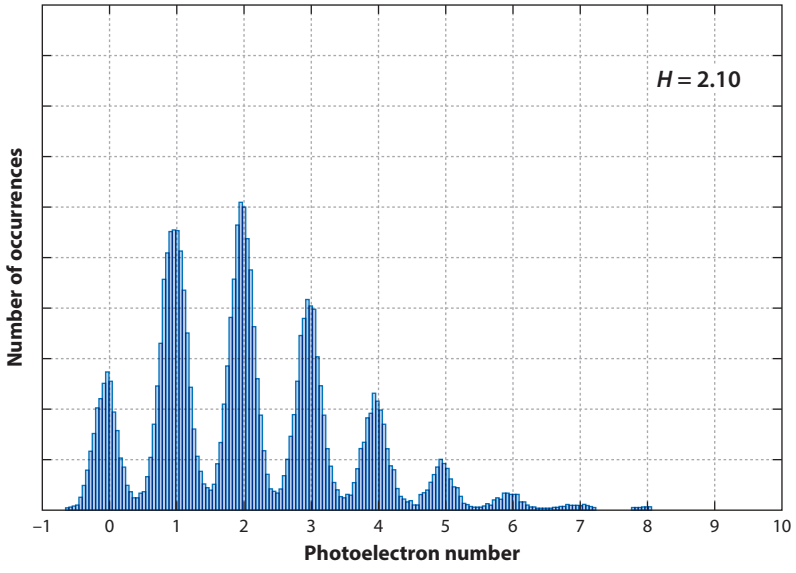

Figure 12

Measured photon-counting histogram (number of occurrences versus normalized readout voltage) showing clear quantization of photoelectrons. The peak heights correspond to the Poisson distribution for an average photoelectron arrival rate H of 2.1 e^-/sample, and the peak widths are related to residual readout noise. Figure adapted from Ma et al. (2017).

Computation that can be performed in a massively parallel manner will probably benefit the most from 3D stacking, and when considering connectivity, it is likely that local image processing benefits more than global image processing. The drive toward smart cameras with edge computing is being explored with 3D stacking technology (Eki et al. 2021).

Photon-counting image sensors have advanced rapidly in the past five years and have enabled new applications. The technology will likely be incorporated as part of mainstream CIS technology before long, enabling larger dynamic range and the ultimate performance in low-light imaging, especially when combined with computational imaging (Ma et al. 2022b).

Very-large-format video image sensors continue to be developed for specialized markets. For example, a 316-Mpixel, 120-fps sensor was implemented for use in the Las Vegas Sphere immersive theater (Agarwal et al. 2023).

Recently, thin-film transistor image sensors on silicon readout integrated circuits with quantum dot photodetectors have incorporated PPDs to improve their imaging performance. These sensors also permit better response than silicon detectors in the shortwave and near-infrared wavelength regimes (Kim et al. 2023).

An area of increasing concern is authentication of images, especially as society enters an age where photorealistic but fake images are easily generated using AI technology. More secure methods to ensure the integrity of original image data are being explored (Mansoorian & Fossum 2002, Fowler et al. 2023).

On the optical side, the possibility of moving from Bayer red, green, blue, green (RGBG) color-filter kernels to receiving R, G, and B signals for each pixel site (and thus avoiding color aliasing problems, long a dream of the image sensor community) seems to be nearing reality given the development of so-called perfect color routers (Catrysse et al. 2022). The related development of metalenses and their integration on-chip may simplify camera design and reduce the size and weight of cameras (Khorasaninejad & Capasso 2017).

5. CONCLUSION

Solid-state image sensors have evolved continuously and are ubiquitous in our daily lives. Not only can individuals enjoy photos and videos with their family and friends, but everyone can see them on social media. This affects markets, culture, education, and even politics. The market in which computers, rather than humans, see images, such as in machine vision, drones, barcode readers, biometrics, and gesture recognition, has also been growing. Some applications require the detection of X-rays, infrared light, and charged particles. Moreover, increasing capabilities for range measurement, polarization, and phase (wavefront) imaging enable new applications.

Like the proverbial double-edged sword, image-sensor-technology development also creates new social issues beyond the obvious social media concerns. These include facilitating criminal activity using cameras (e.g., peeping Toms, illicit video recording, identity theft); infringement on the right to privacy, including automatic facial recognition and tracking by autocratic government agencies; and exploitation of minors and sharing of illegal pornographic images. For a technology intended to benefit personal well-being and society at large with light and truth, it is indeed unfortunate that we must also reckon with, and control, the dark edge of the sword.

DISCLOSURE STATEMENT

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LITERATURE CITED

Agarwal A, Hansrani J, Bagwell S, Rytov O, Shah V, et al. 2023. A 316MP, 120FPS, high dynamic range CMOS image sensor for next generation immersive displays. *Sensors* 23(20):8383

Ahn JC, Lee K, Kim Y, Jeong H, Kim B, et al. 2014. A 1/4-inch 8Mpixel CMOS image sensor with 3D backside-illuminated 1.12μm pixel with front-side deep trench isolation and vertical transfer gate. In *Proceedings of the 2014 IEEE International Conference on Solid-State Circuits (ISSCC), San Francisco, CA, Feb. 9–13*, pp. 124–25. Piscataway, NJ: IEEE

Amelio GF. 1973. *Physics and applications of charge-coupled devices*. Intercon Tech. Pap., IEEE, Piscataway, NJ

Aoki M, Ohba S, Takemoto I, Nagahara S, Sasano A, et al. 1980. MOS color imaging device. In *Proceedings of the 1980 IEEE International Conference on Solid-State Circuits (ISSCC), San Francisco, CA, Feb. 13–15*, pp. 26–27. Piscataway, NJ: IEEE

Ay S, Fossum ER. 2006. A 76 × 77mm/sup 2/, 16.85 million pixel CMOS APS image sensor. In *Proceedings of the 2006 Symposium on VLSI Circuits, Honolulu, HI, June 15–17*, pp. 19–20. Piscataway, NJ: IEEE

Barbe D. 1976. Time delay and integration image sensors in solid state imaging. In *Solid State Imaging*, ed. P Jespers, F van de Wiele, MH White, pp. 659–671. Berlin: Springer

Bayer B. 1976. *Color imaging array*. US Patent 3,971,065

Boyle WS, Smith GE. 1970. Charge coupled semiconductor devices. *Bell Syst. Tech. J.* 49(4):587–93

Carnes JE. 1972. Noise sources in charge-coupled device. *RCA Rev*. 33:327–43

Catrysse P, Zhao N, Jin W, Fan S. 2022. Subwavelength Bayer RGB color routers with perfect optical efficiency. *Nanophotonics* 11(10):2381–87

Chamberlain SG. 1969. Photosensitivity and scanning of silicon image detector arrays. *IEEE J. Solid-State Circuits* 4(6):333–42

Chen K, Afghani M, Danielsson PE, Svensson C, et al. 1990. PASIC: a processor-A/D converter-sensor integrated circuit. In *Proceedings of the 1990 IEEE International Symposium on Circuits and Systems (ISCAS), New Orleans, LA, May 1–3*, Vol. 3, pp. 1705–8. Piscataway, NJ: IEEE

Chen Y, Xu Y, Chae Y, Mierop A, Wang X, et al. 2012. A 0.7e^- r.m.s.-temporal-readout-noise CMOS image sensor for low-light-level imaging. In *Proceedings of the 2012 IEEE International Conference on Solid-State Circuits (ISSCC), San Francisco, CA, Feb. 19–23*, pp. 384–86. Piscataway, NJ: IEEE

Delbrück T, Linares-Barranco B, Culurciello E, Posch C. 2010. Activity-driven, event-based vision sensors. In *Proceedings of the 2010 IEEE International Symposium on Circuits and Systems, Paris, May 30–June 3*, pp. 2426–29. Piscataway, NJ: IEEE

Dickinson A, Ackland B, Eid E-S, Inglis D, Fossum ER. 1995. A 256/spl times/256 CMOS active pixel image sensor with motion detection. In *Proceedings of the 1995 IEEE International Conference on Solid-State Circuits (ISSCC), San Francisco, CA, Feb. 15–17*, pp. 226–27. Piscataway, NJ: IEEE

Dutton NAW, Parmesan L, Gnecchi S, Gyongy I, Calder N, et al. 2015. Oversampled ITOF imaging techniques using SPAD-based quanta image sensors. In *Proceedings of the 2015 International Image Sensor Workshop (IISW)*, pp. 170–73. N.p.: Int. Image Sensors Soc. **https://imagesensors.org/papers/10.60928/om9n-1s8e**

Dyck RH, Weckler GP. 1968. Integrated arrays of silicon photodetectors for image sensing. *IEEE Trans. Electron Devices* 15(4):196–201

Eki R, Yamada S, Ozawa H, Kai H, Okuike K, et al. 2021. A 1/2.3inch 12.3Mpixel with on-chip 4.97TOPS/W CNN processor back-illuminated stacked CMOS image sensor. In *Proceedings of the 2021 IEEE International Conference on Solid-State Circuits (ISSCC), San Francisco, CA, Feb. 13–22*, pp. 154–56. Piscataway, NJ: IEEE

Farrier MG, Dyck RH. 1980. A large area TDI image sensor for low light level. *Imaging IEEE J. Solid-State Circuits* 15(4):753–58

Fossum ER. 1989. Architectures for focal plane image processing. *Opt. Eng.* 28(8):288865

Fossum ER. 1993. Active pixel sensors: Are CCDs dinosaurs? In *Proceedings of the IS&T/SPIE Symposium on Electronic Imaging: Science and Technology, San Jose, CA, Jan. 31–Feb. 5*. Bellingham, WA: SPIE. **https://doi.org/10.1117/12.148585**

Fossum ER. 1994. Assessment of image sensor technology for future NASA missions. In *Proceedings of the IS&T/SPIE 1994 International Symposium on Electronic Imaging: Science and Technology, San Jose, CA, Feb. 6–10*. Bellingham, WA: SPIE. **https://doi.org/10.1117/12.172771**

Fossum ER. 1997. CMOS image sensors: electronic camera-on-a-chip. *IEEE Trans. Electron Devices* 44(10):1689–98

Fossum ER. 2005. What to do with sub-diffraction-limit (SDL) pixels? A proposal for a gigapixel digital film sensor (DFS). In *Program of the 2005 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, Karuizawa, Jpn., June 9–11*, pp. 214–17. Piscataway, NJ: IEEE

Fossum ER. 2013a. Camera-on-a-chip: technology transfer from Saturn to your cell phone. *Technol. Innov.* 15(3):197–209

Fossum ER. 2013b. Modeling the performance of single-bit and multi-bit quanta image sensors. *IEEE J. Electron Devices Soc.* 1(9):166–74

Fossum ER. 2023. The invention and development of CMOS image sensors: a camera in every pocket. In *75th Anniversary of the Transistor*, ed. A Nathan, SK Saha, RM Todi, pp. 281–91. New York: Wiley

Fossum ER, Hondongwa DB. 2014. A review of the pinned photodiode for CCD and CMOS image sensors. *IEEE J. Electron Devices Soc.* 2(30):33–43

Fossum ER, Ma J, Masoodian S, Anzagira L, Zizza R. 2016. The quanta image sensor: Every photon counts. *Sensors* 16(8):1260

Fowler B, Chen W, Johnson K. 2023. Cyber security for CMOS image sensors. In *Proceedings of the 2023 International Image Sensor Workshop, Crieff, Scotl., UK, May 21–25*, pap. 16. N.p.: Int. Image Sensor Soc.

Ge X, Theuwissen AJP. 2017. A $0.5e_{rms}^-$ temporal noise CMOS image sensor with Gm-cell-based pixel and period-controlled variable conversion gain. *IEEE Trans. Electron Devices* 64:5019–26

Guidash RM, Lee TH, Lee PPK, Sackett DH, Drowley CI, et al. 1997. A 0.6 /spl μm CMOS pinned photodiode color imager technology. In *Proceedings of the 1997 IEEE International Electron Devices Meeting (IEDM), Washington, DC, Dec. 10*, pp. 927–29. Piscataway, NJ: IEEE

Guo M, Chen S, Gao Z, Yang W, Bartkovjak P, et al. 2023. A 3-wafer-stacked hybrid 15 MPixel CIS + 1 MPixel EVS with 4.6GEvent/s readout, in-pixel TDC and on-chip ISP and ESP function. In *Proceedings of the 2023 IEEE International Conference on Solid-State Circuits (ISSCC), San Francisco, CA, Feb. 19–23*, pp. 90–92. Piscataway, NJ: IEEE

Haruta T, Nakajima T, Hashizume J, Umebayashi T, Takahashi H, et al. 2017. A 1/2.3 inch 20Mpixel 3-layer stacked CMOS image sensor with DRAM. In *Proceedings of the 2017 IEEE International Conference on Solid-State Circuits (ISSCC), San Francisco, CA, Feb. 5–9*, pp. 76–77. Piscataway, NJ: IEEE

Horton JW, Mazza RV, Dym H. 1964. The scanistor—a solid-state image scanner. *Proc. IEEE* 52(12):1513–28

ICCP. 2023. *Proceedings of the 2023 IEEE International Conference on Computational Photography (ICCP), Madison, WI, July 28–30*. Piscataway, NJ: IEEE

Iddan GJ, Swain CP. 2003. History and development of capsule endoscopy. *Gastrointest. Endosc. Clin. N. Am.* 14(1):1–9

Inoue I, Nozaki H, Yamashita H, Yamaguchi T, Ishiwata H, et al. 1999. New LV-BPD (low voltage buried photo-diode) for CMOS imager. In *Proceedings of the 1999 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, Dec. 5–8*, pp. 883–86. Piscataway, NJ: IEEE

Ishihara Y, Oda E, Tanigawa H, Teranishi N, Takeuchi E, et al. 1982. Interline CCD image sensor with an anti-blooming structure. In *Proceedings of the 1982 IEEE International Conference on Solid-State Circuits (ISSCC), San Francisco, CA, Feb. 10–12*, pp. 168–69. Piscataway, NJ: IEEE

Ishihara Y, Tanigaki K. 1983. A high photosensitivity IL-CCD image sensor with monolithic resin lens array. In *Proceedings of the 1983 IEEE International Electron Devices Meeting (IEDM), Washington, DC, Dec. 5–7*, pp. 497–500. Piscataway, NJ: IEEE

Ito K, Otake Y, Kitano Y, Matsumoto A, Yamamoto J, et al. 2020. A BSI 10μm SPAD pixel array comprising full trench isolation and Cu-Cu bonding with over 14% PDE at 940nm. In *Proceedings of the 2020 IEEE International Electron Devices Meeting (IEDM)*, *San Francisco*, *CA*, *Dec. 12–18*, pp. 347–50. Piscataway, NJ: IEEE

Iwabuchi S, Maruyama Y, Ohgishi Y, Muramatsu M, Karasawa N, et al. 2006. A back-illuminated high-sensitivity small-pixel color CMOS image sensor with flexible layout of metal wiring. In *Proceedings of the 2006 IEEE International Conference on Solid-State Circuits (ISSCC)*, *San Francisco*, *CA*, *Feb. 6–9*, pp. 302–3. Piscataway, NJ: IEEE

Jansson C, Ingelhag P, Svensson C, Forchheimer R. 1993. An addressable 256×256 photodiode image sensor array with an 8-bit digital output. *Analog Integr. Circuits Signal Proc.* 4:37–49

Kagawa Y, Fujii N, Aoyagi K, Kobayashi Y, Nishi S, et al. 2016. Novel stacked CMOS image sensor with advanced Cu2Cu hybrid bonding. In *Proceedings of the 2016 IEEE International Electron Devices Meeting (IEDM)*, *San Francisco*, *CA*, *Dec. 3–7*, pp. 208–11. Piscataway, NJ: IEEE

Kawahito S. 2018. Column-parallel ADCs for CMOS image sensors and their FoM-based evaluations. *IEICE Trans. Electron.* 101.C(7):444–56

Kawahito S. 2021. Multi-tap time-resolved CMOS image sensors and their applications. In *Proceedings of the 26th Microoptics Conference (MOC)*, *Hamamatsu*, *Jpn.*, *Sept. 26–29*, pp. 1–2. Tokyo: Jpn. Soc. Appl. Phys.

Khorasaninejad M, Capasso F. 2017. Metalenses: versatile multifunctional photonic components. *Science* 358(6367):eaam8100

Kim JH, Berghmans F, Siddik AB, Sutcu I, Monroy IP, et al. 2023. A thin-film pinned-photodiode imager pixel with fully monolithic fabrication and beyond 1Me⁻ full well capacity. *Sensors* 23(21):8803

Kim SJ, Han SW, Kang B, Lee K, Kim JDK, et al. 2010. A three-dimensional time-of-flight CMOS image sensor with pinned-photodiode pixel structure. *IEEE Electron Device Lett.* 31(11):1272–74

Kitamura Y, Aikawa H, Kakehi K, Yousyou T, Eda K, et al. 2012. Suppression of crosstalk by using backside deep trench isolation for 1.12 μm backside illuminated CMOS image sensor. In *Proceedings of the 2012 IEEE International Electron Devices Meeting (IEDM)*, *San Francisco*, *CA*, *Dec. 10–13*, pp. 537–40. Piscataway, NJ: IEEE

Kleinfelder S, Lim S, Liu X, El Gamal A. 2001. A 10000 frames/s CMOS digital pixel sensor. *IEEE J. Solid-State Circuits* 36(12):2049–59

Kodama K, Sato Y, Yorikado Y, Berner R, Mizoguchi K, et al. 2023. 1.22μm 35.6Mpixel RGB hybrid event-based vision sensor with 4.88um-pitch event pixels and up to 10K event frame rate by adaptive control on event sparsity. In *Proceedings of the 2023 IEEE International Conference on Solid-State Circuits (ISSCC)*, *San Francisco*, *CA*, *Feb. 19–23*, pp. 92–94. Piscataway, NJ: IEEE

Kosonocky WF, Carnes JE. 1971. Charge-coupled digital circuits. *IEEE J. Solid-State Circuits* 6(5):314–22

Kreider G, Bosiers J, Dillen B, van der Heijden J, Hoekstra W, et al. 1995. An mK/spl times/nK modular image sensor design. In *Proceedings of the 1995 IEEE International Electron Devices Meeting (IEDM)*, *Washington*, *DC*, *Dec. 10–13*, pp. 155–158. Piscataway, NJ: IEEE

Kuroda R, Suzuki M, Sugawa S. 2019. Over 100 million frames per second high speed global shutter CMOS image sensor. In *Proceedings of the 32nd International Congress on High-Speed Imaging and Photonics*, *Enschede*, *Neth.*, *Oct. 8–12*, art. 110510B. Bellingham, WA: SPIE. **https://doi.org/10.1117/12.2524492**

Lee PPK, Gee RC, Guidash RM, Lee T-H, Fossum ER. 1995. An active pixel sensor fabricated using CMOS/CCD process technology. In *Program of the 1995 IEEE Workshop on CCDs and AIS*, *Dana Point*, *CA*, pp. 115–18. N.p.: Int. Image Sensor Soc.

Lee TH, Tredwell TJ, Burkey BC, Hayward JS, Kelly TM, et al. 1981. A novel solid-state image sensor for image recording at 2,000 frames per second. In *Proceedings of the 1981 IEEE International Electron Devices Meeting (IEDM)*, *Washington*, *DC*, *Dec. 7–9*, pp. 475–78. Piscataway, NJ: IEEE

Lesser M, Ouellette D, Theuwsissen AJP, Kreider GL, Michaelis H. 1997. Packaging and operation of Philips 7Kx9K CCDs. In *Program of the 1997 IEEE Workshop on CCDs and AIS*, *Bruges*, *Belg.*, pp. 5–7. N.p.: Int. Image Sensor Soc.

Ma J, Chan S, Fossum ER. 2022a. Review of quanta image sensors for ultra-low-light imaging. *IEEE Trans. Electron Devices* 69(6):2824–39

Ma J, Fossum ER. 2015. A pump-gate jot device with high conversion gain for a quanta image sensor. *IEEE J. Electron Devices Soc.* 3(2):73–77

Ma J, Masoodian S, Starkey D, Fossum ER. 2017. Photon-number-resolving megapixel image sensor at room temperature without avalanche gain. *Optica* 4(12):1474–81

Ma J, Zhang D, Elgendy O, Masoodian S. 2021a. A 0.19e⁻ r.m.s. read noise 16.7Mpixel stacked quanta image sensor with 1.1 μm-pitch backside illuminated pixels. *IEEE Electron Device Lett.* 42(6):891–94

Ma J, Zhang D, Elgendy O, Masoodian S. 2021b. A photon-counting 4Mpixel stacked BSI quanta image sensor with 0.3e⁻ read noise and 100dB single-exposure dynamic range. In *Proceedings of the 2021 Symposium on VLSI Circuits, Kyoto, Jpn., June 13–19*, pp. 1–2. Piscataway, NJ: IEEE

Ma J, Zhang D, Robledo D, Anzagira L, Masoodian S. 2022b. Ultra-high-resolution quanta image sensor with reliable photon-number-resolving and high dynamic range capabilities. *Sci. Rep.* 12:13869

Mansoorian B, Fossum ER. 2002. *Semiconductor imaging sensor with on-chip encryption*. US Patent 6,400,824

Masoodian S, Ma J, Starkey D, Yamashita Y, Fossum ER. 2017. A 1Mjot 1040fps 0.22e⁻r.m.s. stacked BSI quanta image sensor with cluster-parallel readout. In *Proceedings of the 2017 International Image Sensor Workshop (IISW)*, pp. 230–33. N.p.: Int. Image Sensor Soc.

McGrath D, Fujita H, Guidash RM, Kenney TJ, Wu X. 2005. Shared pixels for CMOS image sensor arrays. In *Program of the 2005 IEEE Workshop on CCDs and AIS, Karuizawa, Jpn.*, pp. 9–12. N.p.: Int. Image Sensor Soc.

Mendis S, Kemeny SE, Fossum ER. 1994. CMOS active pixel image sensor. *IEEE Trans. Electron Devices* 41(3):452–53

Mendis SK, Kemeny SE, Gee RC, Pain B, Staller C, et al. 1997. A 128 × 128 CMOS active pixel image sensors for highly integrated imaging systems. *IEEE J. Solid-State Circuits* 32(2):583–86

Monma G, Yuzurihara H. 1993. *Method of manufacturing semiconductor devices*. Jpn. Patent Publ. JP-A-5-6849

Monma G, Yuzurihara H. 1998. *Method of manufacturing semiconductor devices.* US Patent 5,731,131

Moon CR, Jung J, Kwon DW, Yoo J, Lee DH, et al. 2007. Application of plasma-doping (PLAD) technique to reduce dark current of CMOS image sensors. *IEEE Electron Device Lett.* 28(2):114–16

Morimoto K, Iwata J, Shinohara M, Sekine H, Abdelghafar A, et al. 2021. 3.2 Megapixel 3D-stacked charge focusing SPAD for low-light imaging and depth sensing. In *Proceedings of the 2021 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, Dec. 13–15*, pp. 20.2.1–4. Piscataway, NJ: IEEE

Morimoto M, Orihara K, Mutoh N, Toyoda A, Ohbo M, et al. 1992. A 2 M pixel HDTV CCD image sensor with tungsten photo-shield and H-CCD shunt wiring. In *Proceedings of the 1992 IEEE International Conference on Solid-State Circuits (ISSCC), San Francisco, CA, Feb. 19–21*, pp. 172–73. Piscataway, NJ: IEEE

Morrison SR. 1963. A new type of photosensitive junction device. *Solid-State Electron.* 6(5):485–94

Noble PJW. 1968. Self-scanned silicon image detector arrays. *IEEE Trans. Electron Devices* 15(4):202–9

Oike Y. 2022. Evolution of image sensor architectures with stacked device technologies. *IEEE Trans. Electron Devices* 69(6):2757–65

Pain B, Fossum ER. 1994. Approaches and analysis for on-focal-plane analog-to-digital conversion. In *Proceedings of Infrared Readout Electronics II, Orlando, FL*, pp. 208–18. Bellingham, WA: SPIE. **https://doi.org/10.1117/12.178483**

Park BJ, Jung J, Moon CR, Hwang SH, Lee YW, et al. 2007. Deep trench isolation for crosstalk suppression in active pixel sensors with 1.7 μm pixel pitch. *Jpn. J. Appl. Phys.* 46(4B):2454–57

Rhodes H, Tai D, Qian Y, Mao D, Venezia V, et al. 2009. The mass production of BSI CMOS image sensors. In *Proceedings of the 2009 International Image Sensor Workshop (IISW), Bergen, Norway, June 26–28*, pap. 006. N.p.: Int. Image Sensor Soc. **https://imagesensors.org/papers/10.60928/vcrm-fzu8/**

Rominger JP. 1988. Seamless stitching for large area integrated circuit manufacturing. In *Proceedings of the 1988 Santa Clara Symposium on Microlithography*. Bellingham, WA: SPIE. **https://doi.org/10.1117/12.968412**

Roozeboom F, van den Bruele F, Creyghton Y, Poodt P, Kessels WMM. 2015. Cyclic etch/passivation as an all-spatial concept toward high-rate room temperature atomic layer etching. *ECS J. Solid State Sci. Technol.* 4(6):N5067

Sakakibara M, Ogawa K, Sakai S, Tochigi Y, Honda K, et al. 2018. A 6.9-μm pixel-pitch back-illuminated global shutter CMOS image sensor with pixel-parallel 14-bit subthreshold ADC. *IEEE J. Solid-State Circuits* 53(11):3017–25

Sangster F. 1970. Integrated MOS and bipolar analog delay lines using bucket-brigade capacitor storage. In *Proceedings of the 1970 IEEE International Conference on Solid-State Circuits (ISSCC), Philadelphia, PA, Feb. 18–20*, pp. 74–75. Piscataway, NJ: IEEE

Sangster FLJ, Teer K. 1969. Bucket-brigade electronics: new possibilities for delay, time-axis conversion, and scanning. *IEEE J. Solid-State Circuits* 4(3):131–36

Sano Y, Shigeta Y, Ichikawa M, Aoki Y, Umeda T, et al. 1996. On-chip inner-layer lens technology for an improvement in photo-sensitive characteristics of a CCD image sensor. *J. Inst. Telev. Eng. Jpn.* 50(2):226–33

Schlig ES. 1986. A TDI charge-coupled imaging device for page scanning. *IEEE J. Solid-State Circuits* 21(1):182–86

Schuster MA, Strull G. 1966. A monolithic mosaic of photon sensors for solid-state imaging applications. *IEEE Trans. Electron Devices* 13(12):907–12

Séquin CH. 1972. Blooming suppression in charge coupled area imaging devices. *Bell Syst. Tech. J.* 51(8):1923–26

Séquin CH, Sealer DA, Bertram WJ, Tompsett MF, Buckley RR, et al. 1973. A charge-coupled area image sensor and frame store. *IEEE Trans. Electron Devices* 20(3):244–52

Sukegawa S, Umebayashi T, Nakajima T, Kawanobe H, Koseki K, et al. 2013. 1/4-Inch 8Mpixel back-illuminated stacked CMOS image sensor. In *Proceedings of the 2013 IEEE International Conference on Solid-State Circuits (ISSCC), San Francisco, CA, Feb. 17–21*, pp. 484–85. Piscataway, NJ: IEEE

Takahashi T, Kaji Y, Tsukuda Y, Futami S, et al. 2018. A stacked CMOS image sensor with array-parallel ADC architecture. *IEEE J. Solid-State Circuits* 53(4):1061–70

Takayanagi I, Kuroda R. 2012. HDR CMOS image sensors for automotive applications. *IEEE Trans. Electron Devices* 69(6):2815–23

Teranishi N. 2012. Required conditions for photon-counting image sensors. *IEEE Trans. Electron Devices* 59(8):2199–205

Teranishi N. 2016. Effect and limitation of pinned photodiode. *IEEE Trans. Electron Devices* 63(1):10–15

Teranishi N, Ishihara Y. 1987. Smear reduction in the interline CCD image sensor. *IEEE Trans. Electron Devices* 34(5):1052–56

Teranishi N, Kohono A, Ishihara Y, Oda E, Arai K. 1982. No image lag photodiode structure in the interline CCD image sensor. In *Proceedings of the 1982 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, Dec. 13–15*, pp. 324–27. Piscataway, NJ: IEEE

Teranishi N, Watanabe H, Ueda T, Sengoku N. 2012. Evolution of optical structure in image sensors. In *Proceedings of the 2012 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, Dec. 10–13*, pp. 24.1.1–4. Piscataway, NJ: IEEE

Theuwissen AJP. 1995. *Solid-State Imaging with Charge-Coupled Devices*. Berlin: Springer

Theuwissen AJP. 2006. The hole role in solid-state imagers. *IEEE Trans. Electron Devices* 53(12):2972–80

Theuwissen AJP, Beenhakkers M, Dillen B, Folkerts HO, Heyns H. 1998. Versatile building-block architecture for large area, high performance CCD imagers. In *Proceedings of the 28th European Solid-State Devices Research Conference, Bordeaux, France*, pp. 56–61. Piscataway, NJ: IEEE

Theuwissen AJP, Weijtens CHL, Cox JNG. 1985. The accordion imager: more than just a CCD sensor. In *Proceedings of the 1985 Electronic Imaging Symposium, Boston*, pp. 87–90. Bellingham, WA: SPIE

Theuwissen AJP, Weijtens CHL, Esser LJM, Cox JNG, Duyvelaar HTAR, Keur WC. 1984. The accordion imager: an ultra high density frame transfer CCD. In *Proceedings of the 1984 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, Dec. 9–12*, pp. 40–43. Piscataway, NJ: IEEE

Tompsett MF, Amelio GF, Bertram WJ, Buckley RR, McNamara WJ, et al. 1971. Charge-coupled imaging devices: experimental results. *IEEE Trans. Electron Devices* 18(11):992–96

Tournier A, Roy F, Cazaux Y, Lalanne F, Malinge P, et al. 2018. A HDR 98dB 3.2μm charge domain global shutter CMOS image sensor. In *Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, Dec. 1–5*, pp. 10.4.1–4. Piscataway, NJ: IEEE

Venezia VC, Hsiung AC-H, Ai K, Zhou X, Lin Z, et al. 2018. 1.5μm Dual conversion gain, backside illuminated image sensor using stacked pixel level connections with 13ke-full-well capacitance and 0.8e-noise. In *Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, Dec. 1–5*, pp. 10.1.1–4. Piscataway, NJ: IEEE

Walden RH, Krambeck RH, Strain RJ, McKenna J, Schryer NL, et al. 1972. The buried channel charge coupled device. *Bell Syst. Tech. J.* 51(7):1635–40

Walsh L, Dyck R. 1973. A new charge-coupled area imaging device. In *Proceedings of the 1973 CCD Applications Conference*, pp. 21–22. N.p.: Int. Image Sensor Soc.

Weckler GP. 1967. Operation of p-n junction photodetectors in a photon flux integrating mode. *IEEE J. Solid-State Circuits* 2(3):65–73

White M, Lampe D, Mack I, Blaha F. 1973. Characterization of charge-coupled device line and area-array imaging at low light levels. In *Proceedings of the 1973 IEEE International Conference on Solid-State Circuits (ISSCC), Philadelphia, PA, Feb. 14–16*, pp. 134–35. Piscataway, NJ: IEEE

Wuu SG, Chen HL, Chien HC, Enquist P, Guidash RM, et al. 2022. A review of 3-dimensional wafer level stacked backside illuminated CMOS image sensor process technologies. *IEEE Trans. Electron Devices* 69(6):2766–78

Wuu SG, Wang CC, Yaung DN, Tu YL, Liu JC, et al. 2009. A manufacturable back-side illumination technology using bulk-Si substrates for advanced CMOS image sensor. In *Proceedings of the 2009 International Image Sensor Workshop (IISW)*. N.p.: Int. Image Sensor Soc. **https://doi.org/10.60928/5m7f-fo4h**

Xu Y, Ge X, Theuwissen APJ. 2016. A potential-based characterization of the transfer gate in CMOS image sensors. *IEEE Trans. Electron Devices* 63(1):42–48

Yadid-Pecht O, Fossum ER. 1997. Wide intrascene dynamic range CMOS APS using dual sampling. *IEEE Trans. Electron Devices* 44(10):1721–23

Yamashita Y, Takahashi H, Kikuchi S, Ota K, Fujita M, et al. 2011. A 300mm wafer-size CMOS image sensor with in-pixel voltage-gain amplifier and column-level differential readout circuitry. In *Proceedings of the 2011 IEEE International Conference on Solid-State Circuits (ISSCC), San Francisco, CA, Feb. 20–24*, pp. 408–10. Piscataway, NJ: IEEE

Yang DXD, Fowler B, El Gamal A. 1999. A Nyquist-rate pixel-level ADC for CMOS image sensors. *IEEE J. Solid-State Circuits* 34(3):348–56

Yonemoto K, Sumi H, Suzuki R, Ueno T. 2000. A CMOS image sensor with a simple FPN-reduction technology and a hole accumulated diode. In *Proceedings of the 2000 IEEE International Conference on Solid-State Circuits (ISSCC), San Francisco, CA, Feb. 9*, pp. 102–3. Piscataway, NJ: IEEE

Zacharias N, Dorland B, Bredthauer R, Boggs K, Bredthauer G, et al. 2007. Realization and application of a 111 million pixel backside-illuminated detector and camera. In *Focal Plane Arrays for Space Telescopes III, San Diego, CA*, ed. TJ Grycewicz, pp. 72–79. Bellingham, WA: SPIE. **https://doi.org/10.1117/12.736961**

Zhou Z, Pain B, Fossum ER. 1997. CMOS active pixel sensor with on-chip successive approximation analog-to-digital converter. *IEEE Trans. Electron Devices* 44(10):1759–63