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A Cryo-CMOS Controller With Class-DE Driver and DC Magnetic-Field Tuning for Quantum Computers Based on Color Centers in Diamond

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***Abstract*— Striving toward a scalable quantum processor, this article presents the first cryo-CMOS quantum bit (qubit) controller targeting color centers in diamond. Color-center qubits enable a modular architecture that allows for the 3-D integration of photonics, cryo-CMOS control electronics, and qubits in the same package. However, performing quantum operations in a scalable manner requires large currents in the driving coils due to low coil-to-qubit coupling. Moreover, active calibration of the qubit Larmor frequency is required to compensate inhomogeneities of the bias magnetic field. To overcome these challenges, this work proposes both a cryo-CMOS alternating current (AC) controller consisting of a class-DE series-resonant driver and a DC current regulator (DC CR) that uses a triode-biased H-bridge for scalable low-power qubit operations. By experimentally validating the cryo-CMOS performance with a nitrogen-vacancy (NV) color-center qubit, the AC controller can drive a Rabi oscillation up to 2.5 MHz with a supply draw of 6.5 mA, and the DC CR can tune the Larmor frequency by ±9 MHz while driving up to ±20 mA in the bias coil. T_2^* coherence times up to 5.3 μs and single-qubit gate fidelities above 98% are demonstrated with the cryo-CMOS control using Ramsey experiments and gate set tomography (GST), respectively. The results demonstrate the efficacy of the proposed cryo-CMOS chips and enable the development of a modular quantum processor based on color centers.**

***Index Terms*— Calibration, class-DE, cryo-CMOS, DC magnetic field biasing, H-bridge, Larmor frequency, low-power DC current regulator (DC CR), microwave driver, nitrogen-vacancy (NV) center, output stage, quantum computing, resonator, switch-mode amplifier, system engineering, triode.**

I. Introduction

A PRACTICAL computational breakthrough with quantum computing requires a substantial scale-up of the number of quantum bits (qubits). Current advancements are spread over multiple qubit platforms, mostly led by superconducting transmons qubits, which can achieve a good coherence time (>10 µs) and gate fidelity (>99.9%) [1], [2], [3], [4], [5]. To achieve this performance, transmons must operate inside a dilution refrigerator at ∼10-mK temperatures, with each qubit individually wired to its control electronics operating at higher temperatures. Cryo-CMOS circuits have been proposed to keep most of the wiring compact within the cryostat [6], [7], [8], [9], [10]. Such electronics are typically placed at the 4-K stage due to the limited cooling power of the cryostat at lower temperatures [11]. However, this still requires significant bulky interconnects between the 4-K and the mK stage and thereby poses a scalability challenge. As an alternative qubit platform, qubits based on color centers in diamond, such as the nitrogen-vacancy (NV) center [12], can overcome those limitations as they can operate at much higher temperatures (>1 K) while reaching similar coherence times and fidelities [13], [14], [15]. Furthermore, their photonic interface has allowed entanglement generation over long distances (>1.3 km) using conventional fibers, enabling a large quantum computer to be formed through a network of smaller quantum processors [16], [17], [18]. The higher operating temperature of color centers enables co-integrating the qubits with cryo-CMOS control

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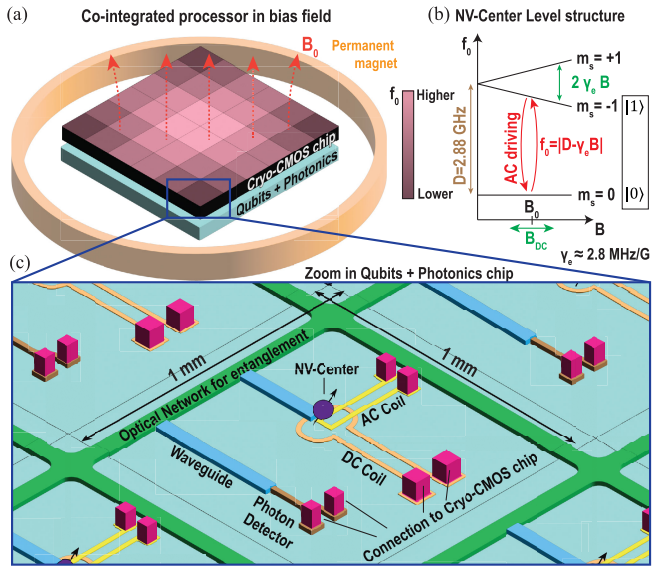

Fig. 1. Envisioned color-center-based quantum processor. (a) 3-D-integrated cryo-CMOS, photonics, and qubits that are biased in a permanent magnetic field. (b) Level structure of the NV-center's electron spin qubit. (c) Components on the Qubits + Photonics chip.

electronics at the same temperature stage, thereby solving the interconnection bottleneck and improving the scalability, but also requiring more research toward thermal management [14], [19], [20]. Previous efforts toward integrating CMOS with color centers have already been shown for sensing purposes [21], [22] and potential cryogenic architectures have been described [23], yet no cryogenic operated qubit controller for color centers has been demonstrated.

Fig. 1 shows a scalable color-center-based quantum processor, where color centers and photonics are 3-D-integrated with a cryo-CMOS chip in a unit-cell architecture, as proposed in [24]. All the required photonic signals for qubit initialization and readout, and the electronic signals for qubit control are generated within each unit cell, which is expected to occupy an area of approximately 1 × 1 mm to fit all the photonic components. Increasing the number of qubits in the quantum processor can be achieved in multiple ways: each unit cell can host one color-center qubit with multiple nuclear spin qubits, and unit cells can be combined to create a larger quantum processor, i.e., in this work, we assume 10 × 10 unit cells, and quantum processors can be combined through photonic links. Initialization and readout of the color-center qubit can be achieved by exciting the color center with a photon, and detecting if any photons are emitted by the color center using a single photon detector, while the frequency of the emitted photon can by tuned by applying strain or an electric field, depending on the color center used [25], [26]. Details about the readout, tuning, and their implementation are out of the scope of this work. Color-center-qubit operations are performed through alternating current (AC) magnetic fields, requiring an AC controller that drives currents through the AC coil, which is bonded off-chip in each unit cell, located close to the color center [see Fig. 1(c)]. The ∼1-mm spacing between unit cells inherently reduces the crosstalk of the magnetic fields. Consequently, frequency spacing schemes, e.g., frequency-division multiple access (FDMA) [9], are not required, enabling all cells to operate at the same Larmor frequency f_0, which is favorable to reduce the total system complexity and power consumption by adopting the same clock distributed among all cells. Still, distributing the same clock and supplies among multiple unit cells can be difficult and warrants additional research.

Moreover, moving toward a scalable color-center-based quantum processor, two open challenges in the unit cells must be addressed. First, due to the hybrid co-integration [19], [24], it is physically difficult to place the coils generating the AC magnetic field close to the color centers, requiring the efficient generation of significant current amplitudes (>10 mA_p) for driving qubit operations. Second, while the Larmor frequency of a 10 × 10 unit cell quantum processor can be set by a global permanent magnet, the inhomogeneity of the permanent magnet and integration inaccuracies can cause a significant deviation in Larmor frequency f_0 (>13 MHz), leading to infidelity when driving qubit operations. In [27], both challenges are overcome by: 1) introducing an AC controller with a class-DE switch-mode driver that efficiently delivers large AC to a low-impedance coil via a series resonator and 2) accurately correcting for deviations in f_0 using a DC current regulator (DC CR) that locally tunes the static magnetic field by driving a DC coil close to the color center.

This article sets out to extend on [27] by defining the requirements for high-fidelity operations on color-center-based qubits (Section II), providing circuit design procedures for the AC controller (Section III) and DC CR (Section IV), respectively, and showing extended characterization to quantify the system's performance with an NV-center qubit (Section V). Conclusions are drawn in Section VI.

II. Requirements for Driving Color-Center Qubits

Since the electronics driving the color-center qubits must ensure that the infidelity introduced during operation and idling is limited, this section presents the requirements for the AC and DC signals to meet 99.9% average gate fidelity for operations and idling, which are summarized in Table I, where each AC signal and each DC signal component contribute to 125×10^{-6} and 250×10^{-6} infidelities, respectively. In this work, 99.9% fidelity is targeted as a first proof of concept. The specification of future drivers can be tuned for more specific target fidelities and optimized for power dissipation.

To perform single-qubit operations on the adopted NV center, the control electronics must drive an AC magnetic field resonant with the Larmor frequency (f_0) perpendicular to the bias field, with f_0 determined by the applied bias field, as shown in Fig. 1(b). This work targets a typical permanent magnetic field range from approximately 1900 to 2000 G, as used in network experiments [17], leading to an f_0 range from 2.44 to 2.72 GHz for transitions between the $m_s = 0$ and $m_s = -1$ energy levels, as shown in Fig. 1(b). The SNR on the AC magnetic field driving operations needs to be >40 dB to meet the infidelity requirement [29], while the amplitude of the signal determines the Rabi frequency, f_r, and thus the speed of the operations. For an f_r of 5 MHz that drives a π rotation in $T_{op} = 100$ ns, a magnetic field amplitude

TABLE I
SPECIFICATIONS FOR THE AC AND DC MAGNETIC FIELDS*

AC Signal Requirement	99.9 % Fidelity
Larmor Frequency	2.7 GHz
Signal Amplitude	2.5 G
Frequency Inaccuracy	56 kHz
Frequency Noise	56 kHz_{rms}
Signal Inaccuracy	17 mG
Amplitude Noise	17 mG_{rms}
Timing Resolution	712 ps
Timing Jitter	712 ps_{rms}
Phase error	0.64°
Wide-band Additive Noise	10.7 mG_{rms}
DC Signal Requirement	**99.9 % Fidelity**
Tuning range	4.8 G
Tuning step	18 mG
Noise	18 mG_{rms}

*For 99.9%-fidelity π-rotations on the NV center's electron spin qubit, assuming the qubit is a two-level system [24], [28].

of 2.5 G_{pk} is required. This signal amplitude, together with the SNR requirement to achieve high fidelity, leads to a rms noise requirement of less than 17 mG_{rms} over a 5-MHz bandwidth, equivalent to a power spectral density (PSD) of 57 pG^2/Hz assuming white noise [28]. The controller has additional requirements for the allowed phase error between the x- and y-gate signals (which have a phase difference of 90°): the error must be below 0.64° for an infidelity of 125×10^{-6}. Furthermore, the AC signal envelope needs to have a time resolution better than 712 ps and a duration jitter below 712 ps_{rms} for both components to contribute less than 125×10^{-6} infidelity for the targeted operation time T_{op}.

Since each AC controller drives a qubit defined by the $m_s = -1$ and $m_s = 0$ state [Fig. 1(b)], no strict spurious free dynamic range (SFDR) requirements are placed on the design as only a single qubit is driven and the $m_s = +1$ can typically be planned far away from the driving tone and its harmonic contents [15], [30]. Additionally, the crosstalk of the driving signal to a neighboring unit cell is attenuated by more than 64 dB, causing less than 2×10^{-6} infidelity for the current unit cell size [24]. When making the unit cells smaller, e.g., due to the reduced size of photonic components, crosstalk may become a more prominent source of infidelity to consider. While the budget for crosstalk-induced infidelity may depend on specific system-design choices, a contribution to the infidelity below 2×10^{-5}, i.e., negligible compared to the contribution listed in Table I, would require a crosstalk lower than 54 dB between unit cells, which could be obtained, for instance, with a cell pitch of 0.6 mm. For the given Rabi frequency, also the allowed frequency inaccuracy and frequency noise can be derived [28], posing requirements on the clock source that can be readily achieved by the cryogenic phase-locked loop (PLL) in [31].

To enable tuning of f_0, each unit cell needs a locally tunable DC magnetic field parallel to the bias field, which can be achieved by using a DC CR driving a current through the DC coil [see Fig. 1(c)]. Here, the deviation of f_0 is assumed to originate from the inhomogeneity of the permanent magnet, which has a simulated variation of 0.24% across a 1×1 cm area [24], requiring a range of 4.8 G to be compensated for the target 2000-G bias field. Based on the target infidelity

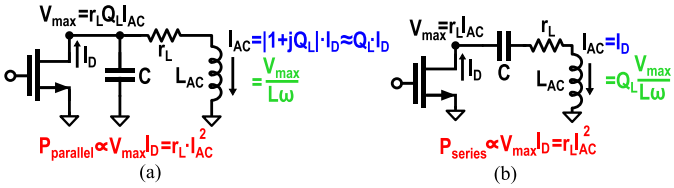

Fig. 2. Different options for driving a resonator: (a) parallel resonator with current-mode driving and (b) series resonator with voltage-mode driving.

and assuming the idling time is equal to T_{op}, the magnetic field needs to be set with a resolution <18 mG to sufficiently limit infidelity due to detuning, i.e., the frequency difference between f_0 and the AC magnetic field frequency f_{mw} [24]. The allowed noise on the magnetic field is similar to the resolution requirement, requiring an integrated noise below 18 mG_{rms}. The qubit idling time T_{op} determines upper limit of the integration bandwidth ($1/(2T_{\text{op}}) = 5$ MHz) and gain ($T_{\text{op}}^2/4$) of the noise contributing to the infidelity. Assuming no echoing sequences are performed, the lower limit of the bandwidth is determined by the experimental duration and is set to 1 Hz in this work [28], [32], [33]. Consequently, the PSD of the noise can consist of $1/f$ noise and white noise, as long as the integrated noise requirement is met.

III. AC CONTROLLER

Based on the requirements given in Section II, this section will provide the procedures for designing a microwave AC controller to drive an NV-center qubit efficiently. Considering the worst-case experimental scenario where the NV center is located ~20 μm away from the coil, see Section V-C, the estimated coupling factor from the microwave coil to the NV center is 50 G/A for near term experiments.[1] Hence, to drive a Rabi of $f_r = 5$ MHz, an AC amplitude (I_{AC}) of 50 mA is required, which is increased to $I_{\text{AC}} = 70$ mA to consider some margin.

Generating this large current amplitude using cryo-CMOS qubit controllers [6], [7], [8], [9] that drive a 50-Ω transmission line into a 50-Ω load would require a large impedance transfer ratio and consume significant power. However, in the proposed 3-D-integrated package (Fig. 1), the driver is located much closer to the qubits; hence, long lines can be omitted, and the amplifier can directly drive a resonator consisting of a capacitor and an inductor (L_{AC}) with a quality factor of Q_L and a series resistance

$$r_L = \frac{\omega L_{\text{AC}}}{Q_L} \tag{1}$$

where $\omega = 2\pi f_0$ is the tank's angular resonant frequency. Since the driver must now provide the required current to a low-ohmic resistor instead of 50 Ω, power consumption is significantly reduced.

Fig. 2 illustrates the two primary options for resonant driving: (1) a parallel-resonant tank with a current-mode driver, and (2) a series-resonant tank with a voltage-mode driver. Considering the theoretical scenario where the parallel- and series-resonator are driven with an ideal current or voltage

[1]In the envisioned integrated unit-cell architecture (Fig. 1), the coupling from the coil to the color center is expected to increase to 290 G/A, lowering the required I_{AC} to 9 mA.

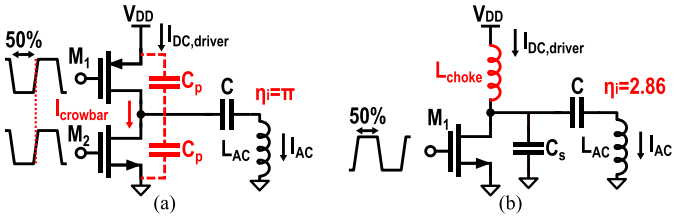

Fig. 3. Different options for switching voltage-mode driver: (a) class-D driver and (b) class-E driver.

source, respectively, both would consume the same power, $r_L I_{\mathrm{AC}}^2$, determined only by the required current and inductor loss. However, in a practical scenario, i.e., where the ideal sources are replaced with a transistor either working in saturation for linear signal amplification or in cut-off and triode for switch mode amplification, the power consumption is also limited by the transistor drain current and required voltage overhead. As can be gathered from Fig. 2, the drain current in the parallel structure is Q_L times lower than in the series one to generate the same coil current. Consequently, for the same transistor minimum drain-source voltage or on-resistance, the parallel option wastes less power and seems advantageous at first glance. However, for the same coil current, the maximum voltage swing ($V_{\max}$) across the current source in the parallel configuration is Q_L times larger than that of the voltage source in the series structure, requiring a Q_L times larger supply voltage as depicted in Fig. 2. Hence, to avoid reliability issues due to time-dependent dielectric breakdown (TDDB) and hot carrier injection (HCI) [34], the maximum voltage swing across gate-drain terminals needs to be limited by using cascode devices. These additional cascode devices consume more supply headroom, increasing the total power consumption (PDC) and making the $I_{\mathrm{AC}}/P_{\mathrm{DC}}$ advantage of the parallel tank only marginal. As a result, in this design, we opt for the voltage-mode series-resonant configuration to avoid using an excessively large supply voltage and cascode devices, while enjoying Q_L times higher coil current for the same $V_{\max}$.

Among different flavors of voltage-mode drivers, we are looking for the one offering the best current efficiency, i.e., $\eta_i = I_{\mathrm{AC}}/I_{DC,\mathrm{driver}}$ to achieve a lower power dissipation at a fixed supply voltage (V_{DD}) and work reliably. Since the distance between unit cells is sufficiently large to suppress crosstalk and spectral leakage, the out-of-band emission requirement on the AC controller is relaxed compared to other qubit platforms. Consequently, a switched-mode driver is preferred over a linear driver as it offers better efficiency and draws no power when idle, which are essential to reducing the controller's power dissipation. The first option is to employ a class-D switch-mode driver [see Fig. 3(a)], operating with 50% duty-cycle input square wave achieving $\eta_i = \pi$ [35]. However, this structure has two problems. First, to achieve a large current amplitude, the ON-resistance of the switches needs to be minimized. Consequently, the power efficiency is reduced at higher frequencies as the charge stored in the large parasitic output capacitance (C_p) of the transistors is dissipated once in every cycle. Second, any overlap in the 50% duty-cycle input pulses due to timing mismatches or slow

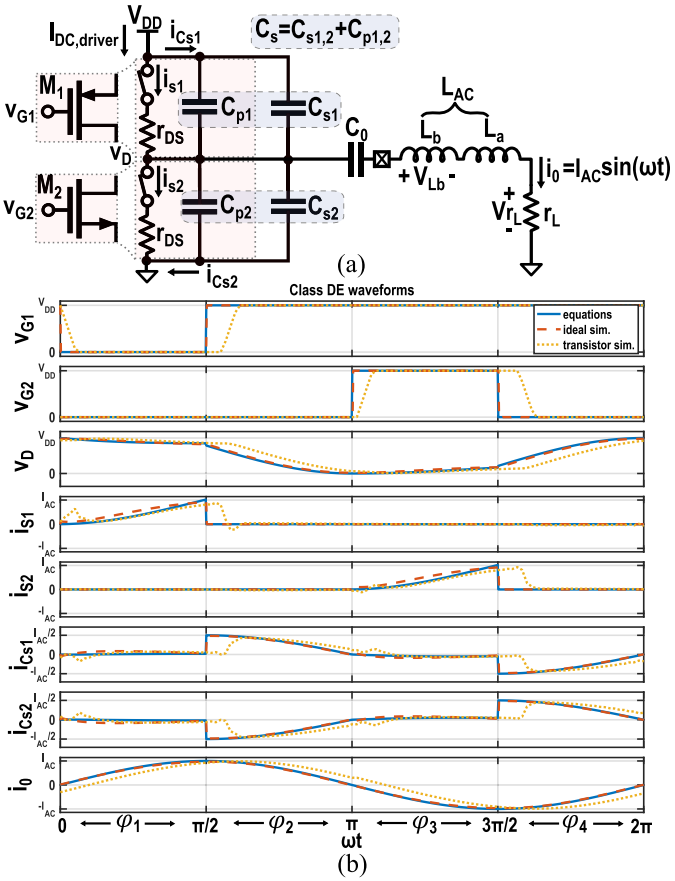

Fig. 4. Class-DE circuit analysis for finite ON-resistance (a) circuit diagram and (b) waveform comparison of derived equations, simulation with ideal switches, and real devices with identical ON-resistance r_{DS}. Simulations are done at 300 K.

voltage crossings could result in crowbar currents [36]. The sensitivity to overlapping pulses due to timing mismatches is mostly independent of temperature. Thus, this effect is also present at cryogenic temperature (CT). Furthermore, due to the choice of low threshold-voltage (LVT) devices to achieve lower ON-resistance and higher current driving capability, the crowbar currents will still be present at CT, even with the increased threshold voltage [37].

An alternative is the class-E driver shown in Fig. 3(b). This topology uses a shunt capacitance C_s to achieve zero-voltage switching (ZVS) and zero-derivative voltage switching (ZDS) operation, improving power efficiency at higher operating frequencies but achieving a lower $\eta_i = 2.86$ [38], [39]. The drawbacks of a class-E amplifier are its large-size choke inductor and the considerable voltage stress on the drain node (i.e., $3.56V_{\mathrm{DD}}$) [40], limiting its reliability. In this work, the advantages of both the class-D and class-E drivers are combined by adopting a class-DE topology, offering both good current efficiency, reliable operation, and absorbing the transistors' parasitic capacitances in the resonator network to satisfy ZVS and ZDS criteria [35], [41].

A. Class-DE Circuit Analysis

Fig. 4 shows the schematic of the class-DE circuit, in which PMOS and NMOS devices (M_1 and M_2) drive a series resonant load $L_{\mathrm{AC}} - C_0 - r_L$. In this analysis, the inductor L_{AC} is split

into two equivalent inductances, L_a and L_b. L_a resonates with the series capacitance (C_0) at the desired operating frequency ω, while L_b, together with shunt capacitor C_s, provides an additional impedance needed to satisfy the ZVS and ZDS criteria. Previous work has primarily focused on analyzing the class-DE operation, assuming ideal switches with zero ON-resistance [35], [41]. In contrast, this work takes a more practical approach. We model the transistors $M_{1,2}$ as ideal switches with open circuit in the OFF-state and a constant equivalent ON-resistance ($r_{\rm DS}$) when turned on. Therefore, this approach, which also models the transistor's equivalent parasitic output capacitances as constant shunt capacitors ($C_{p1,2}$), can provide a better understanding of the design considerations and achieve more accurate estimations of the component values. To achieve this result, a closed-form equation for the $M_{1,2}$ drain node $v_D(\omega t)$ is obtained, as the voltages and currents of the other branches can be readily derived from that.

The circuit operates in four distinguished intervals φ_{1-4} by applying 25% duty-cycle non-overlapping square pulses at $M_{1,2}$ gates. In this analysis, the loaded quality factor of the resonator is assumed to be sufficiently high[2] so that the load current has a purely sinusoidal solution

$$i_o(\omega t) = I_{\rm AC}\sin(\omega t + \phi) \tag{2}$$

where the phase must be $\phi = 0$ to satisfy the ZDS conditions, i.e., $(d(v_D(\omega t))/d(\omega t))|_{\omega t=0,\pi} = 0$ [35].

Interval $\varphi_1 : [0, (\pi/2))$ starts at $\omega t = 0$, at which M_1 is *on* and M_2 is *off*. Hence, there is no current through M_2, $i_{s2} = 0$, and the required current is sourced from the supply through M_1 (i_{S1}) and by the shunt capacitors, i.e., $i_{Cs1,2} = 2\omega C_s(d(v_D(\omega t))/d(\omega t))$. By writing KCL at the drain node, one can obtain the following ordinary differential equation (ODE):

$$v_{D\varphi_1}(\omega t) = V_{\rm DD} - r_{\rm DS}\cdot\left(I_{\rm AC}\sin(\omega t) + 2\omega C_s\frac{d(v_D(\omega t))}{d(\omega t)}\right). \tag{3}$$

Solving the above equation and imposing the ZVS condition, i.e., $v_D(0^+) = V_{\rm DD}$, gives

$$v_{D\varphi_1}(\omega t) = e^{-2\omega C_s r_{\rm DS}\,\omega t}\left(V_{\rm DD} + \frac{r_{\rm DS}I_{\rm AC}}{(2r_{\rm DS}C_s\omega)^2+1}\right) - \frac{r_{\rm DS}I_{\rm AC}(\cos(\omega t) - 2\,r_{\rm DS}C_s\omega\sin(\omega t))}{(2r_{\rm DS}C_s\omega)^2+1}. \tag{4}$$

In interval $\varphi_2 : ((\pi/2), \pi]$, both $M_{1,2}$ are *off*, and the output current is only provided by shunt capacitors. Therefore,

$$-2C_s\omega\cdot\frac{v_D(\omega t)}{d\omega t} = I_{\rm AC}\sin(\omega t). \tag{5}$$

Solving this ODE and imposing the ZVS condition, i.e., $v_D(\pi^-) = 0$, gives

$$v_{D\varphi_2}(\omega t) = \frac{I_{\rm AC}}{2C_s\omega}(\cos(\omega t) + 1). \tag{6}$$

The component values need to be sized such that the drain voltage waveform remains continuous when switching from one operation phase to another. As a result, the load current can be estimated by ensuring a continuous drain voltage waveform at $\omega t = \pi/2$, i.e., $v_{D\varphi_1}((\pi/2)) = v_{D\varphi_2}((\pi/2))$

$$I_{\rm AC} \approx \frac{2C_s\omega V_{\rm DD}\left((2r_{\rm DS}C_s\omega)^2+1\right)}{e^{\pi r_{\rm DS}C_s\omega} - 2\,r_{\rm DS}C_s\omega}. \tag{7}$$

Since the waveform is symmetrical, a similar analysis can be done to find an expression of the drain voltage for intervals $\varphi_3 : [\pi, (3\pi/2))$, where M_1 is *off* and M_2 is *on*, and $\varphi_4 : ((3\pi/2), 2\pi]$, where both transistors are *off*. The resulting waveform equations plotted in Fig. 4(b) show that the drain voltage is continuous and matches the harmonic balance simulation of the equivalent circuit.

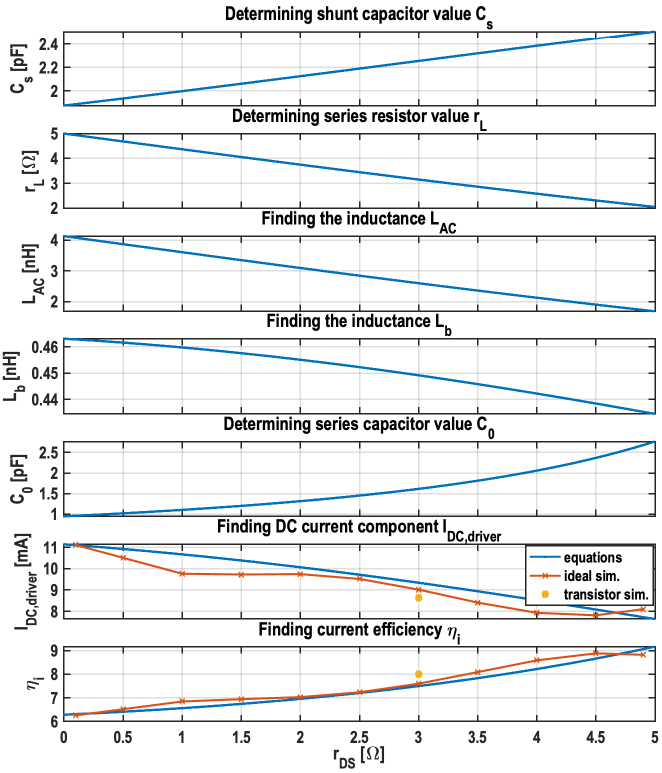

Fig. 5. Class-DE component values and performance based on the design equations for fixed output current ($I_{\rm AC} = 70$ mA) over variable ON-resistance ($r_{\rm DS}$).

B. Class-DE Design Procedure

Based upon the circuit analysis, this section develops a design guide to determine the components' values (i.e., C_s, r_L, $L_{\rm AC}$, L_b, C_0, and $r_{\rm DS}$) and to estimate the performance (i.e., η_i) of the class-DE driver. Initially, to derive the components' values, given the targeted current amplitude $I_{\rm AC}$, the design equations are developed step-by-step, and different components' values are plotted versus $r_{\rm DS}$ in Fig. 5. At the end of this section, $r_{\rm DS}$ is determined based on practical limitations, and all components' values can be found accordingly.

The first step is to find the required shunt capacitor value C_s, which can be extracted from (7) for a known $I_{\rm AC}$, and $r_{\rm DS}$. By increasing $r_{\rm DS}$, the transistor current $i_{s1,2}$ reduces, and consequently, a larger C_s value is needed to provide the output current to the load. Next, the required parasitic series resistance of the inductor, r_L, is determined by dividing the

[2]In practice, the quality factor should be larger than 3 to ensure a nearly sinusoidal load current. Otherwise, the performance of the class-DE is strongly affected due to the presence of more harmonic components at the output [42], [43].

magnitude of the in-phase component of the drain node voltage by the required load current

$$r_L = \frac{V_{r_L}}{I_{\mathrm{AC}}} = \frac{\frac{1}{\pi}\int_0^{2\pi} v_D \sin(\omega t)\ \mathrm{d}(\omega t)}{I_{\mathrm{AC}}}. \tag{8}$$

Accordingly, L_{AC} can be calculated using (1), assuming a maximum implementable quality factor of ∼14. As can be gathered from Fig. 5, for larger r_{DS}, the load resistance and, subsequently, the inductance value decreases to keep I_{AC} constant. Of course, since r_L cannot become negative, the results are only plotted for a small range of r_{DS} up to 5 Ω.

Furthermore, since L_a and C_0 should resonate at the design frequency ω, L_b can be calculated by dividing the fundamental quadrature component of v_D over the output current

$$L_b = \frac{V_{Lb}}{\omega I_{\mathrm{AC}}} = \frac{\frac{1}{\pi}\int_0^{2\pi} v_D \cos(\omega t)\ \mathrm{d}(\omega t)}{\omega I_{\mathrm{AC}}}. \tag{9}$$

Now, one can find the required series capacitance to resonate with the virtual inductance L_a

$$C_0 = \frac{1}{\omega^2 L_a} = \frac{1}{\omega^2 (L_{\mathrm{AC}} - L_b)} = \frac{1}{\omega r_L \left(Q_L - \frac{V_{Lb}}{V_{r_L}}\right)}. \tag{10}$$

Since the DC provided by the shunt capacitors in the steady state must be zero, and i_{S1} only draws current from the supply during the first interval φ_1, the driver's DC can be calculated by

$$I_{DC,\mathrm{driver}} = \frac{1}{2\pi}\int_0^{\frac{\pi}{2}} i_{S1}(\omega t)\ \mathrm{d}(\omega t). \tag{11}$$

A larger r_{DS} results in a higher voltage drop over the transistor during the initial phase, which increases the voltage variation across the shunt capacitors and causes them to deliver more current to the load. Since I_{AC} is constant, M_1 then delivers less current to the load, thus reducing the driver DC and improving its current efficiency from 2π to 8.75 when r_{DS} increases from 0 to 5 Ω (see Fig. 5). Consequently, at first glance, it seems that one should use a larger r_{DS} to achieve better current efficiency and power consumption.

However, r_{DS} cannot be chosen arbitrarily large for two reasons. First, as can be gathered from Fig. 5, one may need to reduce the inductor's number of turns to realize a smaller L_{AC}. Hence, the inductor's current-to-magnetic-field coupling factor drops, and therefore, to achieve the same magnetic field amplitude, the driver has to deliver more current to the resonator, increasing its power consumption. Second, the current driving capability of the transistor reduces at a larger r_{DS}, which means the transistors may not be able to provide the required peak current. For example, in our 40-nm CMOS technology, a minimum length NMOS transistor can only offer around 0.3 mA/μm in triode with a 200-mV drain–source voltage. To ensure that the required peak current of 70 mA can be provided, M_2 width (W_n) should be larger than 233 μm. Considering some margin, M_2 size is chosen (W_n/L_n) = (250 μm/40 nm). Due to the lower mobility of PMOS devices, the M_1 size (W_p/L_p) is 2.25× larger (562.5 μm/40 nm) to achieve the same peak current. As a result, the r_{DS} of both devices is approximately 3 Ω in this design.

In terms of noise, M_1 and M_2 transistors only add thermal noise when they are on for 25% of the clock period. With the large output current swing and the narrow bandpass filter at the output, the simulated SNR is >50 dB over the full design range of r_{DS} from 0 to 5 Ω. Consequently, the SNR requirement in Table I is always satisfied.

After determining r_{DS} and by employing Fig. 5, the values of other components can be found accordingly: $L_{\mathrm{AC}} = 2.6$ nH, $r_L = 3.15\,\Omega$, $C_s = 2.25$ pF, and $C_0 = 1.6$ pF. Moreover, based on simulation results, the effective parasitic output capacitance of the NMOS and PMOS device is approximately $\overline{C_p} \approx 0.5$ fF/μm. Therefore, the shunt capacitance values can be found by $C_{s1} = C_s - \overline{C_p} W_n = 2.13$ pF and $C_{s2} = C_s - \overline{C_p} W_p = 2.0$ pF. These values are taken as a guideline for the implemented driver and inductor design. In practice, due to assembly and fabrication variations and limitations (e.g., the bond-wire length), the inductance and quality factor values can vary, resulting in a deviation of the resonance frequency and current efficiency.

C. Controller Implementation

Fig. 6 shows the block diagram of the controller implementation. To optimize the class-DE driver performance across an f_0 range of 2.6–3 GHz, and counteract fabrication and assembly variations, the shunt and series capacitors have 2-bit tuning. In the series resonator, the maximum voltage across the series capacitor is significantly higher than the drain voltage. To reduce voltage stress on the tuning switches, C_0 is realized by a series connection of a fixed capacitor (C_1) and a tunable capacitor consisting of C_2 with two parallel switched capacitors (C_3 and C_4).

The AC controller only generates constant-amplitude rectangular pulses and is optimized to operate efficiently at the nominal supply voltage and the maximum required f_R. Although the rotation speed is fixed at a certain supply voltage, the operation time (T_{op}) can be adjusted to achieve any desired rotation angle, thereby enabling the implementation of any qubit gate. Additional pulse shaping is not necessary for this platform where there are no strict SFDR requirements and interference to neighboring qubits is negligible due to the physical spacing, as mentioned in Section II.

In order to control the rotation axis of the qubit, quadrature clock phases are needed. Hence, a divide-by-2 circuit is employed to produce the required 50% duty-cycle phases (φ_{0-3}) from an off-chip clock. As shown in the table in Fig. 6, based on the rotation axis of the desired qubit gate (i.e., $\pm x$ and $\pm y$), a de-multiplexer-based phase rotator then directs the appropriate overlapping φ_{0-3} phases to AND gates to generate the required 25% duty-cycle pulses for class-DE operation. Following this, an (N)AND gate combines the enable signal (EN) from the digital controller with the desired clock phase to trigger the driver to generate a rectangular pulse. It is important to note that the clock generation blocks, which consist of the divider, phase selectors, and AND gates for generating a 25% duty-cycle clock, remain active between pulses to ensure that the generated phases remain coherent while running different instructions. However, when not driving the

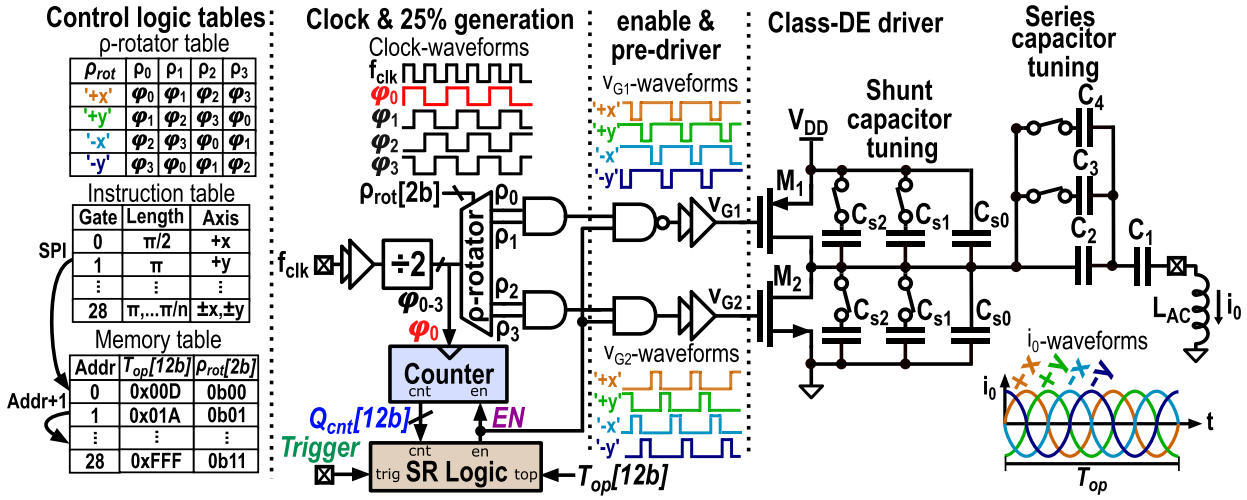

Fig. 6. Block diagram of the AC controller implementation, illustrating the control logic tables, the phase and pulselength controller, quadrature clock and 25% non-overlap generation, pre-driver, and class-DE driver with capacitor tuning.

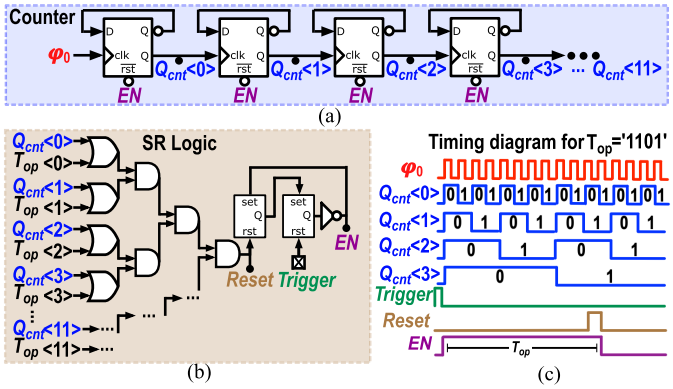

Fig. 7. Digital circuits (a) counter circuit (simplified to 4 bit), (b) set–reset logic circuit, and (c) timing diagram of pulselength control, enabling the output for $T_{\rm op} = 13$ counts.

qubit, the clock leakage to the output should be negligible, as the EN signal disables the pre-driver and driver.

Fig. 7 shows the simplified block and timing diagrams of the pulselength controller. It uses a 12-bit counter driven by the divided clock φ_0 to control the pulselength, $T_{\rm op}$, with a timing resolution of 370 ps and a maximum gate duration of 1.5 µs, thus meeting the required 712-ps resolution and 100-ns gate duration mentioned in Section II with enough margin. The counter is constructed using a divide-by-2 chain, which minimizes the circuit to just 12 flip-flops for a 12-bit counter.

When an external trigger is received, the EN is set high, activating the output driver and starting the counter. Once the stored $T_{\rm op}$ value and counter value ($Q_{\rm cnt}$) are equal (i.e., $T_{\rm op}\langle 0{:}11\rangle = Q_{\rm cnt}\langle 0{:}11\rangle$), the EN signal is reset using the internal reset signal. This action turns off the output, resets the counter, and retrieves new $T_{\rm op}$ value and phase rotator selection bits ($\rho_{\rm rot}$) from the instruction memory, which will be used at the next trigger. The memory can, in total, store 28 sequential gates to program the required gate sequences for qubit experiments.

IV. DC Current Regulator

By assuming a DC-coil current-to-field coupling of 710 G/A [24], the tuning range specification in Table I translates into a current range of 6.8 mA, as required to compensate the magnetic field inhomogeneity. Similarly, the tuning step translates to a step size of 25 µA, required to set a sufficiently accurate Larmor frequency, thus setting the specifications for the DC CR (Fig. 8). To support a wider range for the coil–qubit coupling and thus be compatible with more fabrication options, the target range is extended to 24 mA and the step size is lowered to 8 µA. Since each unit cell in the quantum processor will require an always-on DC CR, each regulator should consume less than 1 mW.[3]

To minimize the power, an H-bridge structure is adopted to allow positive and negative currents in the coil, thus shifting the required range of the coil current $I_{\rm DC}$ from 0 to 24 to −12 to 12 mA at the expense of two additional switches and, hence, more area. As a result, the power dissipation in the switches reduces by 2× compared to a single switch in series with the coil, i.e., from $I_{\rm DC}^2 r_{o4}$ to $((I_{\rm DC}/2))^2 \cdot 2r_{o4}$, assuming the same drain-to-source resistance r_{o4} for the NMOS switches $M_{4a,b}$ and $M_{5a,b}$. For a given coil current, the power dissipation can only be reduced by lowering the supply voltage. Although operating the H-bridge switches in saturation would make the circuit robust against variations of the supply and the coil resistance $R_{\rm coil}$, it would require excessive headroom,[4] thus forcing a biasing in the triode region. Generally, such low supply voltage can be accurately delivered by remote sensing, still sufficient power supply rejection (PSR) must be present when multiple DC CRs in the quantum processor are connected in parallel. Since up to 100 current regulators turning on or off in a quantum processor can change the current (∼1 A) in the interconnect ($R_{\rm ic} \approx 12.5\,{\rm m}\Omega$ for 10 × 10 unit cells [24]), the supply can be modulated by roughly 10 mV. To prevent crosstalk from this, $I_{\rm DC}$ should not vary more than an LSB step, i.e., 8 µA, requiring PSR $> (0.8\ {\rm mA/V})^{-1}$.

[3]The AC controller will likely dissipate more power when driving gates, but power dissipation can be reduced, e.g., by clock gating during readout when no gates are driven.

[4]With $V_{\rm DSat} > 100$ mV over a single H-bridge switch, the dissipation would be >1.2 mW.

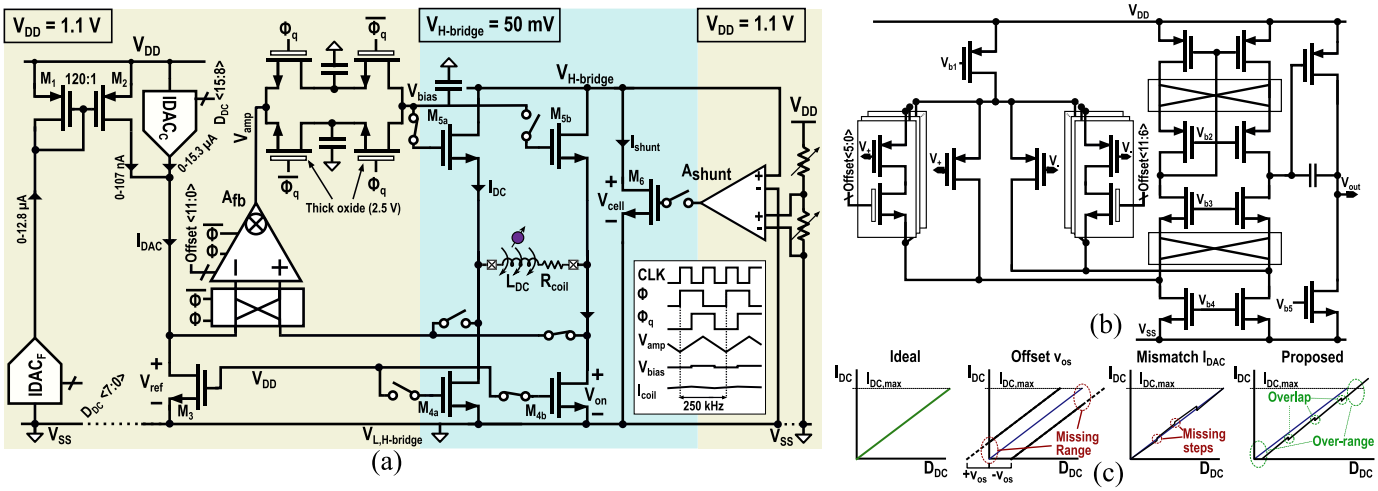

Fig. 8. (a) Schematic of the DC CR consisting of an H-bridge operating with a reduced supply (blue), a feedback loop operating with the nominal supply of 1.1 V (yellow) to accurately set the current in the coil and a shunt path that allows modulating the H-bridge supply (when multiple H-bridges are arranged in series). When multiple H-bridges are voltage-stacked, $V_{\text{L,H-bridge}}$ is not shorted to V_{SS}. (b) Two-stage Miller amplifier with rail-to-rail output with a trimmable input pair and thick-oxide chopping switches used to implement A_{fb} in (a). (c) Transfer from D_{DC} to I_{DC}; from left to right: ideal transfer; transfer in the presence of offset in A_{fb}, causing a reduction of the output range; transfer in the presence of mismatch in the digital-to-analog converter (DAC), causing missing codes; the proposed transfer, in which the effect of non-idealities is mitigated by introducing overlap between various DAC transitions and having over-range to allow for some residual offsets.

A. Current Regulation Loop

To improve the supply rejection and to accurately set the current in the coil independently of variations in r_{o4} and R_{coil}, the reference current I_{DAC} is generated and mirrored into the H-bridge by the feedback loop comprising the amplifier A_{fb} and $M_{5a,b}$, as shown in Fig. 8. A_{fb} senses the drain voltage of transistors M_3 and $M_{4a,b}$, both in deep triode, and tries to equalize the two voltages by regulating the gate of $M_{5a,b}$. As a result, the current in the coil is $I_{\text{DC}} \approx (W_4/W_3)I_{\text{DAC}}$, since $L_3 = L_4$. Although the feedback loop could alternatively have regulated the gate of $M_{3,4}$, this would have changed the operation of $M_{3,4}$ from weak to strong inversion over the I_{DAC} range, thus resulting in a varying mismatch between M_3 and M_4 [44] and, hence, in additional non-linearities. Instead, biasing $M_{3,4}$ in deep triode with a fixed $V_{\text{gs3,4}} = V_{\text{DD}}$ ensures: 1) minimum sizing of M_4, reducing area; 2) a fixed mismatch between M_3 and M_4 over the whole I_{DAC} range, resulting in a fixed gain error; and 3) the improved matching between M_3 and M_4 by biasing in strong inversion, even at CTs [44]. To size the circuit for minimum power while meeting the noise and accuracy requirements, the design equations describing the accuracy, PSR, noise, and power dissipation of the DC CR are derived [45].

The DC transfer of the regulation loop assuming M_3 and M_4 are in deep triode is given by

$$I_{\text{DC}} = \frac{r_{o3} I_{\text{DAC}} + v_{\text{os}}}{r_{o4} + \frac{R_{\text{coil}}+r_{o4}}{A_{\text{fb}}} + \frac{1}{g_{m5}\alpha A_{\text{fb}}}} \tag{12}$$

where g_{m5} is the transconductance of $M_{5a,b}$, r_{oi} is the small signal drain-to-source resistance of M_i (which equals the large signal drain-to-source resistance since M_3, $M_{4a,b}$, and $M_{5a,b}$ are biased in triode), $\alpha = [r_{o5}/(r_{o5} + r_{o4} + R_{\text{coil}})]$, A_{fb} is the DC gain of the feedback amplifier, and v_{os} is the offset of the amplifier. I_{DC} affects both g_{m5} and r_{o5} across the target range. For low I_{DC}, $M_{5a,b}$ will be in weak inversion, resulting in both $r_{o5} \gg R_{\text{coil}} + r_{o4}$ causing $\alpha \approx 1$ and a small g_{m5}. For high I_{DC}, $M_{5a,b}$ is biased in strong inversion with r_{o5} approaching r_{o4} reducing $\alpha \leq 0.5$, while g_{m5} is larger and depends on $V_{DS,5}$. In any case, A_{fb} must then be large enough to avoid poor accuracy in setting the coil current. Similarly, the PSR is given by

$$\text{PSR} = \left(\frac{dI_{\text{DC}}}{dV_{\text{H-bridge}}}\right)^{-1} = r_{o5}g_{m5}[R_{\text{coil}} + r_{o4}(A_{\text{fb}} + 1)] + r_{o5} + R_{\text{coil}} + r_{o4} \tag{13}$$

which may be degraded for large I_{DC} where r_{o5} is small, thus requiring a large A_{fb}.

The low-frequency PSD of the noise in the coil current can be described as

$$i^2_{n,DC} = \frac{i^2_{n,M5}r^2_{05} + i^2_{n,M4}[r_{o4} + g_{m5}r_{o5}r_{o4}(H_{Afb}+1)]^2}{\left\{g_{m5}r_{o5}[r_{o4}(H_{Afb}+1) + R_{\text{coil}}] + \frac{r_{o5}}{\alpha}\right\}^2} + \frac{v^2_{n,\text{amp}} + r^2_{o3}\left(i^2_{n,\text{DAC}} + i^2_{n,M3}\right)}{\left(r_{o4} + \frac{R_{\text{coil}}+r_{o4}}{H_{Afb}} + \frac{1}{g_{m5}\alpha H_{Afb}}\right)^2} \tag{14}$$

where $i^2_{n,Mi}$ is the PSD of the noise of transistors M_i, H_{Afb} is the amplifier open loop gain with input referred noise PSD $v^2_{n,\text{amp}}$, and $i^2_{n,\text{DAC}}$ is the noise PSD on the reference current I_{DAC}. The amplifier loop attenuates $i^2_{n,M5}$, making $v^2_{n,\text{amp}}$, $i^2_{n,\text{DAC}}$, $i^2_{n,M4}$, and $i^2_{n,M3}$ the dominant noise sources at low frequencies, while outside the loop bandwidth $i^2_{n,M4}$ and $i^2_{n,M5}$ will dominate the PSD until they are attenuated by parasitic capacitances, which is not shown in the equation.

Finally, the power dissipation of the DC CR is given by

$$P_{\text{DC}} = I^2_{\text{DC}}[r_{o4}(1+\alpha_5) + R_{\text{coil}}] + \alpha_{\text{DAC}} V_{\text{DD}} I_{\text{DC}} \frac{r_{o4}}{r_{o3}} + P_{\text{amp}} \tag{15}$$

where $\alpha_5 = (r_{o5}/r_{o4})$ when both are fully turned on, P_{amp} is the dissipation of the amplifier, and α_{DAC} is an efficiency

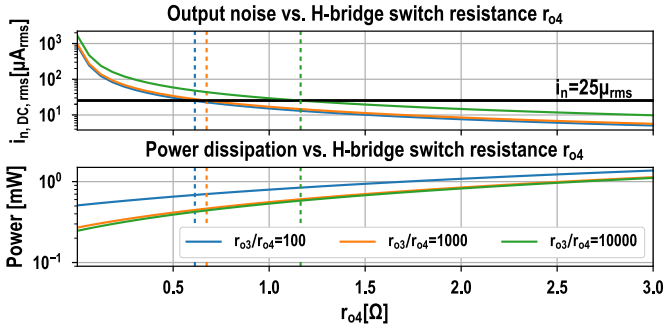

Fig. 9. Sweeping noise and power as a function of r_{o4} and r_{o3}/r_{o4}, the black line indicates the allowed noise for 99.9% fidelity and the colored dashed lines indicate the r_{o4} for which the noise requirement is met.

factor for generating the I_{DAC} current given by $\alpha_{\mathrm{DAC}} = (\max(I_{\mathrm{DACgen}})/\max(I_{\mathrm{DAC}}))$, with I_{DACgen} being the total current dissipated in the DAC to generate I_{DAC}.

The following parameters are used in the following analysis: $R_{\mathrm{coil}} = 1\,\Omega$, $\alpha_{\mathrm{DAC}} = 2$ (as justified later by the adopted topology), and $\alpha_5 = 1$ with equally sized $M_{4a,b}$ and $M_{5a,b}$. α_5 could be reduced for smaller power dissipation, i.e., $r_{o5} < r_{o4}$, but that comes at the expense of a larger area and an excessive load capacitance for the amplifier.

For the amplifier, lowering the bandwidth generally will help to reduce both its power and its noise but at the cost of a worse suppression of supply noise. In this work, the amplifier is designed to dissipate a maximum $P_{\mathrm{amp}} = 100\ \mu\mathrm{W}$ and to achieve the PSR specifications at DC while still improving the PSR up to 30 kHz, beyond which on-chip and off-chip filtering will further attenuate the supply noise. In this amplifier bandwidth, $1/f$ noise sources are dominant, and, based on simulated typical values, the integrated (1 Hz–30 kHz) noise contributions are assumed $v_{n,\mathrm{amp}}^2 = 225\ \mathrm{pV}_{\mathrm{rms}}^2$ and $i_{n,\mathrm{DAC}}^2 + i_{n,M3}^2 = (r_{o4}/r_o3) \cdot 64\ \mathrm{fA}_{\mathrm{rms}}^2$, where the factor (r_{o4}/r_{o3}) follows from assuming that M_3 and the DAC have a fixed bias point, causing the SNR on I_{DAC} to change if larger I_{DAC} currents are needed, i.e., due to smaller (W_4/W_3) ratios. For $i_{n,M4}$ and $i_{n,M5}$ only thermal noise,[5] i.e., $i_{n,Mx,\mathrm{th}}^2 = (4kT/r_{\mathrm{ox}})$, up to the upper limit of the qubit noise bandwidth (5 MHz) is added.

Fig. 9 shows the tradeoff in the choice of r_{o4}: a lower resistance would excessively amplify the amplifier and the DAC-branch noise, while a higher resistance would lead to a too high power dissipation. Similarly, a higher gain $(I_{\mathrm{DC}}/I_{\mathrm{DAC}}) = (r_{o3}/r_{o4})$ would amplify the DAC-branch noise, while a low gain would increase the DAC branch power dissipation since it requires larger I_{DAC} currents. In this work, the gain $(r_{o3}/r_{o4}) = 1000\times$ is chosen, requiring $r_{o4} \geq 0.6\,\Omega$ to meet the noise requirement. To have some extra margin for the noise in the prototyped design, r_{o4} is nominally designed to be $1\,\Omega$ at 300 K with $(W_4/L_4) = 1000\times(480\ \mathrm{nm}/40\ \mathrm{nm})$, and (W_4/L_4) is made programmable to account for reduced resistance at 4.2 K [46]. With r_{o4} known, the minimum required supply to meet the current range is $V_{\text{H-bridge}} \geq I_{\mathrm{DC}}[r_{o4}(1+\alpha_5) + R_{\mathrm{coil}}]$, leading to a power dissipation of 600 μW in the H-bridge when choosing $V_{\text{H-bridge}} = 50$ mV.

For the amplifier, $A_{\mathrm{fb}} > 90$ dB follows from (13) to achieve a DC PSR $> (0.8\ \mathrm{mA/V})^{-1}$ and a 2-MHz unity-gain bandwidth is chosen to achieve the PSR improvement up to 30 kHz. A two-stage Miller amplifier [Fig. 8(b)] is then adopted, with a folded-cascode first stage to provide enough gain and a rail-to-rail output stage ensuring that $M_{5a,b}$ can be biased from weak to strong inversion, such that the full range of I_{DC} from 0 mA to ±12 mA can be covered. Since the amplifier offset can lead to dead codes [Fig. 8(c)], the input pair of the amplifier is trimmable to allow reducing the offset to below 400 μV. With the target bandwidth, an integrated noise on I_{DC} of 15 $\mu\mathrm{A}_{\mathrm{rms}}$ is achieved with an amplifier and DAC power dissipation of 80 and 31 μW, respectively, resulting in a total power dissipation of the regulation loop of 111 μW.

Due to the $1000\times$ gain between I_{DAC} and I_{DC}, an I_{DAC} range of more than 0–12 μA and an 8-nA step size need to be implemented. To avoid missing codes while also consuming little area, I_{DAC} is generated by two coarse/fine 8-bit binary-weighted cascoded current DACs, $\mathrm{IDAC_C}$ and $\mathrm{IDAC_F}$, leading to $\alpha_{\mathrm{DAC}} = 2$. The $\mathrm{IDAC_F}$ current is scaled down by the $M_{1,2}$ current mirror before summation with the $\mathrm{IDAC_C}$ current to prevent impractically small unit currents in $\mathrm{IDAC_F}$, which otherwise would result in excessive size or in poor matching due to weak-inversion operation. As $M_{1,2}$ operate in weak inversion due to the low current range in M_2 (0–107 nA), the expected mismatch at CTs can be limiting [37]. As a workaround, overlaps between the MSB, MSB-1, and MSB-2 of both $\mathrm{IDAC_C}$ and $\mathrm{IDAC_F}$ and between $\mathrm{IDAC_F}$'s maximum range and the $\mathrm{IDAC_C}$ LSB step are included. Also, extending the I_{DAC} range to 0–15.3 μA ensures that the required coil current can be set even if the gain from I_{DAC} to I_{DC} is lower due to the mismatch between M_3 and M_4 or if the amplifier offset introduces dead codes [see Fig. 8(c)]. Since I_{DAC} only needs to be programmed once during the calibration of the qubit f_0, the overlap will not affect the operation and ensures that f_0 can be set with sufficient accuracy.

B. Chopper Stabilization

The noise sources in (14) are dominated by the $1/f$ noise of the amplifier and the I_{DAC} branch, where we assume that the gate-referred transistor flicker noise at 4.2 K remains approximately the same as 300 K for the given bias point [47]. Although the circuit is sized to achieve the noise specifications in the presence of such $1/f$ noise, exploring the chopping of the amplifier is interesting, as it could lead to a lower power dissipation by enabling a lower r_{o4}. Thus, chopper switches are implemented in the feedback loop and the amplifier, as shown in Fig. 8. The chopping ripple originating from v_{os} needs to be well below the stochastic noise requirement of the magnetic field, as shown in Table I. While v_{os} can be somewhat reduced by trimming the offset, further reduction of the chopping ripple is achieved by using a switched-capacitor notch filter (SC-filter) that samples the amplifier output at the quadrature clock phases Φ_q and attenuates the residual tone by >50 dB [48]. Thick-oxide switches are used for the chopper and the

[5] $M_{4,5}$ are large and biased in triode, making their $1/f$ noise low.

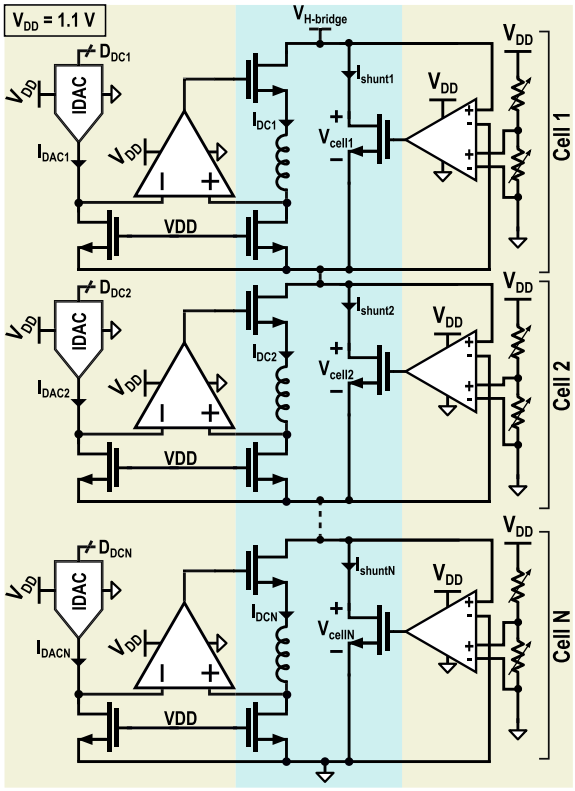

Fig. 10. DC CR with shunt path that enables recycling the current to reduce the interconnect current. For simplicity, only half of the H-bridge is drawn.

SC-filter to prevent any increased ON-resistance that could occur when V_{amp} and V_{bias} are around mid-rail at CTs [46]. To ensure stability of the feedback loop and proper $1/f$ noise cancellation, the chopping frequency must be larger than the loop bandwidth and the $1/f$ noise corner, i.e., f_{chop}>200 kHz for the parameters of Section IV-A. An added benefit of chopper stabilization is that offset v_{os} will be further attenuated, limiting the missing ranges of I_{DC} when R_{on} is small [see (12)].

C. Stacking DC CRs

Since the DC CR is to be used in a scalable quantum processor, operating multiple regulators in parallel needs to be considered. For the full quantum processor, the power dissipation normalized by the number of unit cells N is given, as an extension of (15), by

$$P_{DC} = I_{DC}^2[r_{o4}(1+\alpha_5) + R_{coil} + N R_{ic}] + P_{reg} \qquad (16)$$

where R_{ic} is the interconnect resistance due to metal routing and bond wires, estimated to be ~12.5 mΩ for a 10 × 10 mm quantum processor with $N = 100$ [24], and P_{reg} is the power of the amplifier and DAC. The N term in (16) can limit scalability and originates from DC CRs operating in parallel, drawing current from the same supply, causing the combined current to flow through the interconnect and possibly dominating the total power dissipation as N grows large [24]. To reduce the interconnect current, multiple H-bridges can be connected in series to allow for current re-use and to minimize the power dissipation in R_{ic}, as shown in Fig. 10, which also enables using a larger $V_{H\text{-}bridge}$ that may be easier to generate. To enable setting the H-bridge current independently in each unit cell, an additional feedback loop is introduced that regulates the voltage drop across the H-bridge, as shown in Fig. 8(a), and allows for an alternative current path I_{shunt}.

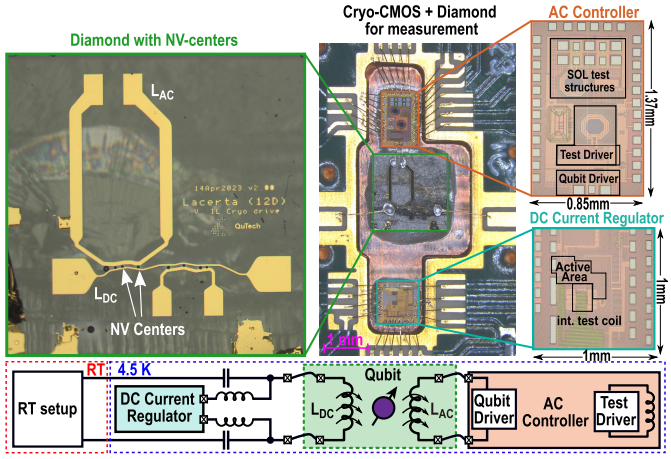

Fig. 11. Integrated cryo-CMOS and NV-center SIL sample. Two gold striplines, L_{AC} and L_{DC}, are patterned on the diamond. L_{DC} is bonded to a bias-T, which combines the DC CR and the RT setup. L_{AC} is directly bonded to the AC controller. The AC controller chip also hosts a test driver with an on-chip coil and short-open-load (SOL) test structures to characterize the driver and on-chip coil.

The feedback loop drives a transistor M_6 that shunts the residual current not used to drive the coil. Hence, this transistor needs to have a sufficiently low ON-resistance, such that a maximum current of 12 mA can be shunted with a maximum drop equal to $V_{H\text{-}bridge}$ to avoid an increase in power dissipation. The shunt transistor is driven by a differential difference amplifier, implemented as a folded-cascode amplifier consuming 3 μW with a gain bandwidth (GBW) of 200 kHz. The two input branches compare the voltage drop across the H-bridge to a reference voltage and the gate of M_6 is regulated to equalize the two. At low frequencies, the current regulation loop discussed in Section IV-A determines the supply rejection and the noise at lower frequencies. As a result, the voltage regulation does not require high accuracy and only noise at higher frequencies could be introduced due to the regulator. It is expected that up to ten cells can be stacked with V_{cell} voltages between 30 and 50 mV, which enables reducing interconnect dissipation significantly due to the I_{DC}^2 term of (16). The amount of H-bridges that can be stacked is limited since for H-bridges that are close to the supply side, i.e., cell 1 in Fig. 10, the fixed V_{DD} of 1.1 V limits the overdrive voltage on the transistors, increasing the resistances and power dissipation.

V. Measurement Results

This section summarizes the electrical results and qubit measurements with the AC controller and DC CR at CT and room temperature (RT). Both chips were fabricated in a commercial 40-nm CMOS process. For the DC CR, a single cell, as shown in Fig. 8, has been implemented on chip. The chips' die micrographs and their integration with the NV-center qubit sample are shown in Fig. 11. The measurement data and analysis files are found in [49].

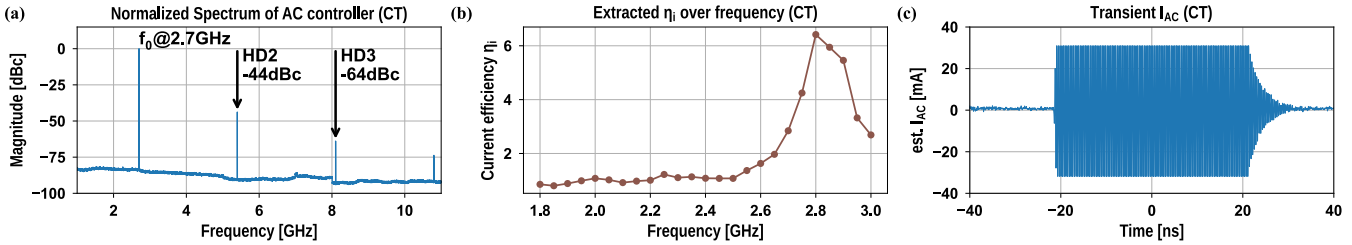

Fig. 12. Electrical characterization of the AC controller: (a) normalized spectrum measured with the magnetic probe; (b) extracted current efficiency $\eta_i = I_{\mathrm{AC}}/I_{DC,\mathrm{driver}}$ over frequency; and (c) transient waveform of I_{AC} extracted with the magnetic probe.

A. AC Controller Characterization

The AC controller chip hosts two replica class-DE drivers, as shown in Fig. 11: 1) a test driver employing an on-chip three-turn coil for standalone electrical characterization and 2) a qubit driver that is bonded to an off-chip coil for qubit measurements. To characterize the magnetic field generated by the chip, a magnetic-field probe [50] was placed roughly ∼100 µm above the center of the on-chip test coil within a cryogenic probe station cooled close to 4.2 K. The magnetic field at different frequencies was de-embedded using the manufacturer's calibration file. To estimate the current amplitude, the coupling factor of the three-turn coil at the distance of ∼100 µm was estimated by simulations to be around 70 G/A. The AC controller performance over frequency shown in Fig. 12(a) and (b) has been characterized with an R&S FSW 40-GHz spectrum analyzer. At CT, the best current efficiency is achieved at 2.8 GHz, where the measured magnetic flux density is 2.09 G, corresponding to an extrapolated current I_{AC} of 29.5 mA_p,[6] while drawing a 4.6-mA DC from a 1.1-V supply. Over the 2.6–3.0-GHz range, an SNR of >47 dB[7] for a 5-MHz bandwidth is achieved. Moreover, when the driver is disabled, no clock leakage is detectable at the output, as it falls below the measurement setup's noise level.

The AC controller's transient waveforms are shown in Fig. 12(c) at CT measured with the magnetic-field probe and in Fig. 13 at RT with a voltage probe, each captured in a single acquisition using a Teledyne LeCroy WaveMaster 40-GS/s oscilloscope. These waveforms demonstrate the digital controller's functionality in applying different qubit gate pulses, controlling the pulselength, and generating the four quadrature phases. For Fig. 13, the chip was programmed to produce a sequence of pulses alternating among the four quadrature phases to emulate the $\pm x$ and $\pm y$ gates for qubit control. By capturing and utilizing the input clock as the reference, the generated quadrature pulses are manually shifted and overlayed, allowing all pulses to be combined in a single plot in Fig. 13(b) and (c). While Fig. 13(b) and (c) demonstrates the chip's capability to generate $\pm x$ and $\pm y$ gate pulses, it cannot accurately determine the controller's quadrature phase inaccuracy due to the limited time resolution of the oscilloscope and coarse synchronization. Hence, the phase error will be determined later from the qubit measurements in Section V-C.

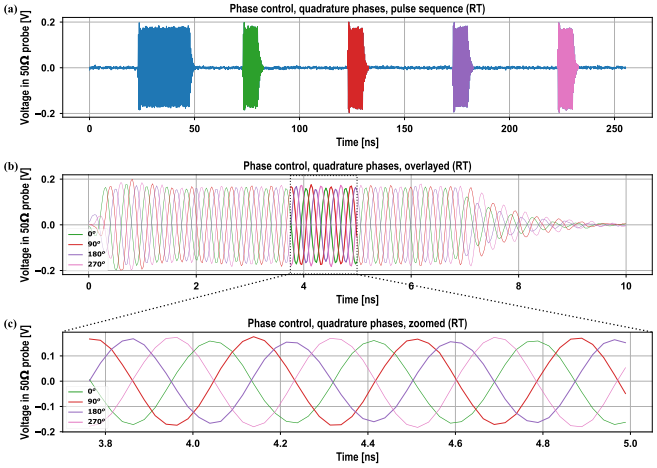

Fig. 13. Transient waveforms of quadrature phase control: (a) pulse sequence of one marker pulse and four quadrature pulses; (b) overlayed quadrature pulses; and (c) zoomed-in view quadrature pulses.

The overall power consumption of the AC controller is 16.8 mW when the electron spin is actively controlled at 2.7 GHz. The majority of this power is used by the class-DE driver, which consumes 7.2 mW, followed by the pre-driver and 25% duty-cycle generation at 6.1 mW, and the clock buffer and divider at 3 mW. The digital controller only consumes 0.5 mW. In a practical algorithm, active control of the electron spin takes up less than 5% of the algorithm time, as the remaining time is allocated for nuclear spin control and readout [24], [51]. By integrating the AC coil more closely to the qubit in the envisioned architecture and implementing this digitally friendly architecture in more advanced technology nodes, the power consumption could be further reduced.

B. DC CR Characterization

The performance of the DC regulator at both RT and CT (4.2 K) is shown in Fig. 14 and is summarized in Table II. During the measurements at 4.2 K, a printed circuit board (PCB) with the DC CR is mounted on a dipstick and submerged in liquid helium. By using an H-bridge that is connected to pads, either an external coil for biasing the NV center or a shunt resistance for measuring the current can be used. For the reported electrical characterization, the current is measured across a 1-Ω shunt resistance with a $V_{\text{H-bridge}}$ of 50 mV and a V_{DD} of 1.1 V.

[6]The measured output current is lower than the design simulations for two reasons: 1) due to use of an on-chip multi-turn inductor, the loss of the tuning switches, and interconnect, the effective quality factor of the fabricated amplifier is lower than the simulated Q_L of 14 and 2) due to the coupling between the on-chip coil and the magnetic field probe, an additional load impedance is coupled into the system, resulting in a larger loss.

[7]The reported SNR is likely limited by the noise of the active magnetic-field probe. Unfortunately, measuring and de-embedding the noise of the active probe were not possible within the cryogenic environment.

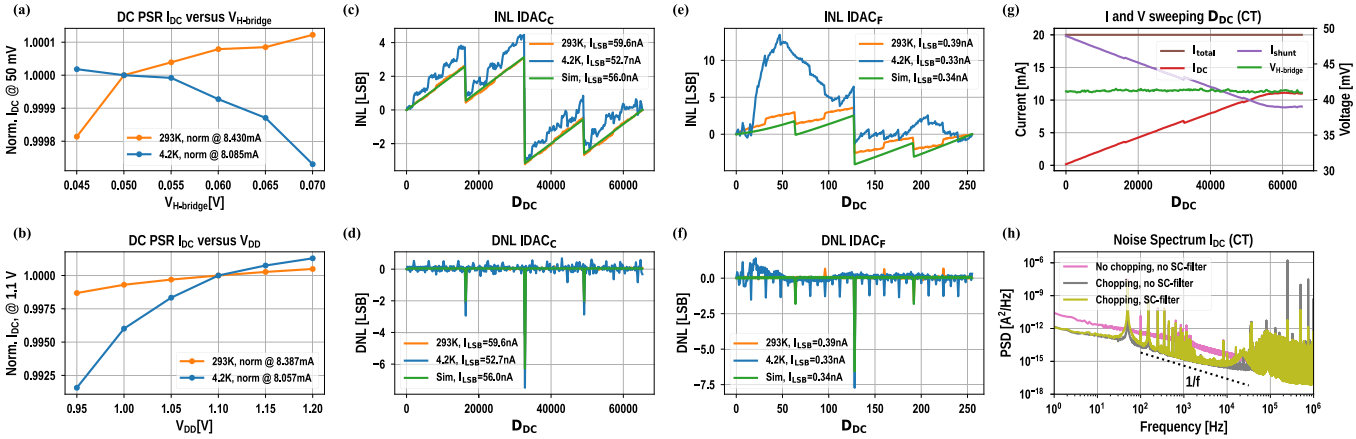

Fig. 14. Electrical characterization of the DC CR at RT (293 K) and CT (4.2 K). (a) and (b) show the DC PSR versus VH-bridge and V_{DD}. (c) and (d), and (e) and (f) show the INL and DNL of the IDAC$_C$ and IDAC$_F$, respectively. (g) shows the operation of the DC CR with shunt path enabled. (h) shows the noise PSD at CT. Simulations are done at 300 K

TABLE II
PERFORMANCE OF THE DC CR**

Specification	RT	4.2 K
V_{DD} [V]	1.1, 2.5	1.1, 2.5
$V_{H\text{-}bridge}$ [V]	50 mV	50 mV
Max I_{DC} [mA]	10.5	12.5
Average ΔI_{DC} [nA]	341	310
IDAC$_C$ Max/min ΔI step [nA]	70.7/-318.4	88.9/-342.3
IDAC$_F$ Max/min ΔI step [pA]	648.9/-2020	787/-2205
$V_{H\text{-}bridge}$ rejection ([μA/V])$^{-1}$	$(88.5)^{-1}$	$(-87.4)^{-1}$
V_{dd} rejection ([μA/V])$^{-1}$	$(58)^{-1}$	$(297)^{-1}$
PSD 10 Hz No Chopping [A^2/Hz]	462×10^{-15}	2400×10^{-15}
PSD 10 Hz Chopping [A^2/Hz]	25×10^{-15}	305×10^{-15}
P_{VDD} No Chopping [μW]	154	134
P_{VDD} Chopping [μW]	287	281
$P_{H-bridge}$ [μW]	525	625
Active Area [mm^2]	0.13	0.13

**Chopping is enabled with f_{chop}=250 kHz unless otherwise specified.

The power supply rejection of the DC CR for the $V_{\text{H-bridge}}$ and V_{DD} supply is plotted in Fig. 14(a) and (b), demonstrating an (87.4 μA/V)$^{-1}$ and (297 μA/V)$^{-1}$ for the $V_{\text{H-bridge}}$ and V_{DD} supply at CT, respectively.

Fig. 14(c)–(f) show the integral nonlinearity (INL) and differential nonlinearity (DNL) of the IDAC$_C$ and IDAC$_F$, which are measured on the I_{DAC} branch of Fig. 8 by connecting the node to an external pad and sweeping the values $D_{DC}\langle 15:8\rangle$ and $D_{DC}\langle 7:0\rangle$ [see Fig. 8(a)] for the coarse and fine DACs, respectively. The INL and DNL show the designed overlap between the MSB, MSB-1, and MSB-2 transitions, with a measured maximum step of 787 pA (88.8 nA) for IDAC$_F$ (IDAC$_C$). Combined with the 84.0 nA (13.5 μA) range of IDAC$_F$ (IDAC$_C$), the DAC covers the full range from 0 to 13.5 μA with a maximum step of 4.8 nA (limited by the overlap between IDAC$_F$ and IDAC$_C$), thus meeting the I_{DAC} requirement. The INL of IDAC$_F$ at 4.2 K clearly exhibits a large error at lower codes, which originates from sub-threshold bumps of transistors M_1 and M_2 operating in the sub-threshold regime at low D_{DC} due to the low current levels [37].

The operation of the DC CR with the shunt path is shown in Fig. 14(g). In this measurement, both the shunt regulation is set to a fixed value D_{shunt} and the total current into the DC CR I_{total} is kept at a constant 20 mA and measured by a source measurement unit (SMU), while also the voltage drop across the H-bridge and the output current are measured as D_{DC} is swept. I_{shunt} is then calculated by subtracting I_{DC} from I_{total}. The measurement demonstrates the functionality of the shunt regulation loop since the DC CR can independently set the current in I_{DC} across the various D_{DC}, while keeping the voltage drop across the H-bridge fixed to 41 mV due to the used $D_{\text{shunt}} = 32$ code. I_{DC} clips for high D_{DC} due to the limited $V_{\text{H-bridge}}$ that is set combined with finite H-bridge and coil resistance. Since the test chip only contains a single cell, stacking, as shown in Fig. 10, would require multiple chips and significantly complicates the measurement setup. To circumvent such a difficulty, similar shunt regulation behavior has been measured by inserting a resistor in the ground return path, effectively raising $V_{\text{L,H-bridge}}$ [Fig. 8(a)] to 150 mV.

Fig. 14(h) shows the noise PSD at CT, where the SC-filter attenuates the chopping tone by 54.5 dB and the 50-Hz tones in the spectrum originate from the SMU that is used to generate a reference current [49]. RT noise measurements up to 10 kHz match well with the simulations, and the integrated noise should contribute a sufficiently low 2×10^{-4} infidelity for $T_{\text{idle}} = 100$ ns.

C. Qubit Measurements

The AC controller and the DC CR are combined with a diamond sample that contains solid immersion lenses (SILs) [51] with NV centers, as shown in Fig. 11. The ensemble is mounted on a copper backplate and placed in a Montana Instruments Cryostation S50 [52], which cools the sample to 4.3 (cryo-CMOS off) and 4.5 K (cryo-CMOS on) during the experiments. The AC controller is directly bonded to the L_{AC} coil. This patterned strip line, together with the bond wires, was designed with a similar inductance as the on-chip test coil. As confirmed by electromagnetic (EM) simulations, the total inductance (including bond wires) is 2.6 nH, and the quality factor is 6.3.[8] The DC CR is connected to the L_{DC}

[8]The quality factor was limited by the patterned gold stripline, which has a maximum thickness of 200 nm. In the envisioned architecture in Fig. 1, this can be improved by enhancing the metal thickness on the diamond substrate or even implementing a superconducting coil.

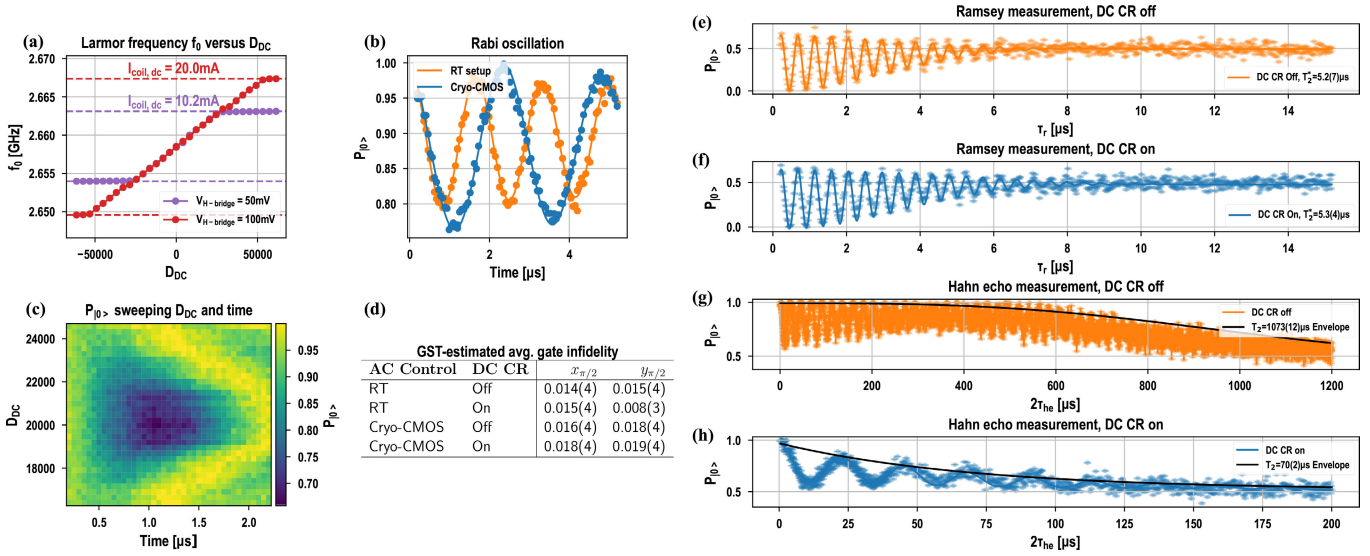

Fig. 15. Measurements of the NV center with the cryo-CMOS AC controller and DC CR, with uncertainties reported in the concise uncertainty notation. (a) Larmor frequency of the NV center as a function of D_{DC} of the DC CR. (b) Rabi oscillation versus time driven by both the AC controller and the RT setup. (c) Calibration plot with both cryo-CMOS chips enabled for a fixed f_{clk} of the AC controller, both time (x-axis) and DC CR code (y-axis) are swept to find the maximum contrast of the Rabi oscillation, resulting in the expected Chevron pattern. (d) GST results using both RT electronics and the AC controller with various settings where the DC CR is disabled and enabled ($\Delta f_0 = +0.6$ MHz), showing fidelities >98% for all settings. (e) and (f) T_2^* measurements with the DC CR disabled and enabled ($\Delta f_0 = +5$ MHz) are shown. (g) and (h) T_2 measurements for the same settings.

coil through a bias-T that combines the DC regulator output with signals from the RT setup (used for comparison). The optical setup used in the qubit measurements is the same as the one described in [53]. The sample is biased with a weak magnetic field of 80 G perpendicular to the surface of the diamond and aligned to the NV axis, resulting in Larmor frequencies similar to the 2000-G magnetic field. The coils are patterned with gold around the SILs on the surface of the diamond, resulting in striplines with a thickness of 200 nm and designed widths of 25 (L_{AC}) and 10 µm (L_{DC}) close to the SILs. The striplines have approximately 10-μm vertical and horizontal spacings to the center, meaning that both coils introduce parallel and perpendicular magnetic fields. While the used sample can demonstrate the functionality of the cryo-CMOS with the qubit, the current-to-magnetic-field couplings of L_{AC} and L_{DC} will be further improved in the envisioned 3-D-integrated processor of Fig. 1.

The experimental results demonstrating functionality with the qubit are plotted in Fig. 15. Fig. 15(a) shows the functionality of the DC CR plotting the qubit Larmor frequency as a function of the code D_{DC}, with the sign of D_{DC} indicating the current direction in the H-bridge. The Larmor frequency is measured by weakly driving (i.e., with low f_r) a specific microwave frequency with the RT electronics, and observing if this inverts the state of the qubit. Afterward, the dips originating from the hyperfine interaction with different nitrogen states can be fit to extract f_0 [54].[9] Both measurements with an H-bridge supply of 50 and 100 mV are plotted. The supply has been increased to compensate for the additional resistive losses due to the bias-T, such that the required current range is met. A tuning range of 9 (3.2 G) and 18 MHz (6.4 G) is demonstrated, meeting the targeted tuning range even with the unoptimized coil.

Fig. 15(b) shows the comparison of a Rabi oscillation driven by the AC controller with the one driven by the RT setup. The plotted oscillation has a low f_r due to the reduced supply ($V_{\mathrm{DD}} = 0.65$ V) of the AC controller output stage, allowing the AC controller to drive a single nitrogen state and resulting in a single clean oscillation with (1/3) maximum amplitude.[10] For all other experiments, the AC controller is operated at the nominal supply voltage ($V_{\mathrm{DD}} = 1.1$ V) and Rabi oscillations with a speed of 2.5 MHz can be achieved, while RT setup can drive larger currents than the cryo-CMOS, resulting in Rabi frequencies up to 27 MHz [15]. Furthermore, a linear relation between the current draw of the output stage and the resulting Rabi frequency was observed [27].

In Fig. 15(c), both cryo-CMOS chips are enabled to demonstrate that the NV center's Larmor frequency can be tuned to the f_{mw} of the AC controller. In this plot, both the AC controller pulse duration (x-axis) and the magnetic field introduced by the DC CR (y-axis) are swept. For certain magnetic fields (i.e., $D_{\mathrm{DC}} < 18\,000$ and $D_{\mathrm{DC}} > 23\,000$), there is barely any Rabi oscillation visible, meaning that the f_0 is too far detuned from f_{mw}. However, for $D_{\mathrm{DC}} \approx 20\,200$, an oscillation with the highest amplitude is measured. This indicates that the f_0 is tuned to f_{mw} at this magnetic field and demonstrates that inhomogeneities in f_0 can be calibrated with the DC CR.

To see the effect of noise from the generated magnetic field on the qubit, Ramsey experiments are plotted in Fig. 15(e) and (f), and Hahn-echo experiments are shown in Fig. 15(g) and (h). For the Ramsey experiment ($x_{\pi/2}$–τ_r–$x_{\pi/2}$),

[9]The Larmor frequency of the electron spin changes based on the NV centers ^{14}N spin state ($S = 1$), resulting in three dips. By initializing the nitrogen spin, a two-level system with a single dip would be created [51].

[10]The ^{14}N spin state is not initialized in this measurement. As a result, a Rabi frequency between 1 and 3 MHz can drive one nitrogen state resonantly and two transitions with a detuning, resulting in one slower oscillation with large amplitude and two faster oscillations with smaller amplitude.

TABLE III
BENCHMARK OF THE PROPOSED AC CONTROLLER WITH PRIOR ART

AC controllers	**This work**	[6]	[7]	[8]	[9]	RT
Qubit type	NV	Transmon	Transmon	Spin	Transmon & spin	NV
Qubit temperature	4.5 K	20 mK	20 mK	20 mK	20 mK	4.5 K
Impedance [Ω]	<1	50	50	50	50	50
Cryo-CMOS temp. [K]	4.5	3	3	3	3	N.A.
AC driver Class	DE	A(B)†	A(B)†	A	A	A
Frequency range [GHz]	2.6-3	4-8	4.5-5.5	11-17	2-15	0.7-6
Maximum I_{AC} [mAp]	30.1	N.A.	0.6*	4.0*	1.1*	1000
SNR [dB]	>47	N.A.	N.A.	>44	48	N.A.
Rabi frequency [MHz]	2.5	91‡	23.5‡	N.A.	1.2	>27
1-Qubit Gate fidelity	>98% (GST)	>99.6% (RB)	99.2% (RB)	N.A.	>99.7% (RB)	>98% (GST)
Active Area [mm^2]	0.092	7#	1.6	∼4	4	N.A.
Technology	40-nm Bulk	28-nm Bulk	14-nm FinFET	22-nm FinFET	22-nm FinFET	N.A.
Power per qubit, active control	16.8 mW	<4 mW	23 mW	90 mW∞♡	192 mW♡	>200W

†Derived from schematic, depends on bias point
*Assuming Pout with 50Ω
‡Based on reported gate duration
#Active area not explicitly mentioned
∞Estimated
♡FDMA allows for simultaneous control of 2 qubits

the time τ_r is swept so that the dephasing time T_2^* can be derived from the decay.[11] Without the cryo-CMOS controller introducing a DC magnetic field, this results in a T_2^* of 5.2(7) µs, while with the cryo-CMOS, a T_2^* of 5.3(4) µs is measured. This illustrates that the cryo-CMOS control, without chopping enabled, does not degrade the T_2^* when reducing the magnetic field at the NV center and introducing a Δf_0 of +5 MHz. The measured T_2^* should contribute less than 1×10^{-3} to the gate infidelity both when idling and during operations, according to [28]. For the Hahn echo experiment ($x_{\pi/2}$–τ_{he}–x_{π}–τ_{he}–$x_{\pi/2}$), the time τ_{he} is swept, showing visible collapse and revival of the signal due to interaction with the nuclear spin bath. T_2 is fit to the exponential decay of the revivals [56]. Without any additional DC bias, the spin bath only contributes low-frequency noise that can effectively be decoupled using a Hahn echo, resulting in a T_2 of 1.07(1) ms. With the DC magnetic field enabled, higher frequency noise above 1 kHz is added, which results in a reduced T_2 of 70(2) µs [57]. Consequently, while the introduced DC magnetic field affects the electron coherence time that can be achieved through dynamical decoupling, which, if needed, can be improved by reducing higher frequency noise at the expense of increased power dissipation [58], it does not reduce the T_2^* and does not affect the gate fidelity of the electron spin qubit.

The AC controller chip has a memory in which 28 instructions can be stored, resulting in randomized-benchmarking (RB) sequences with a maximum Clifford gate depth of 6, limiting the ability to observe a clear decay and leading to inconclusive fidelity estimates [59]. Hence, gate set tomography (GST), a self-consistent tomography method [60] that allows for the reconstruction of a set of gates, has been used. With GST, the infidelity for the characterized gates $x_{\pi/2}$ and $y_{\pi/2}$ (with T_{op}=135 ns) are provided separately, and a decomposition of the errors, such as stochastic (e.g., white noise) or coherent (e.g., over-rotation) errors can be extracted. During the characterization sequences, the nitrogen state was initialized using measurement-based initialization to create a two-level system. The GST sequences were run with a maximum gate length of 4. The resulting reports shown in Fig. 15(d) indicate a gate fidelity of >98% for both the RT and the cryo-CMOS controller, with and without the cryo-CMOS DC bias field enabled [49]. The remaining infidelity is similar for the various controller and magnetic field settings and is dominated by stochastic errors. These errors could originate from the shallow GST circuit depth, limited by what amount of gate errors can be amplified and distinguished [60]. With an extended instruction memory in a future system, more accurate RB and GST results can be naturally achieved [15]. The next limiting factor in the GST gate decompositions is the phase error, which was found to be ∼5° between the axis angles of the $x_{\pi/2}$ and $y_{\pi/2}$ gates for the cryo-CMOS controller, limiting the gate fidelity to 99.2%. This phase error is attributed to device mismatch that increases at CT [44], layout mismatches among the four clock phases due to the routing constraint, and phase imbalance of the off-chip balun [61]. Therefore, to enhance the quadrature phase accuracy in the next iteration, it is recommended to calibrate the phase and duty cycle of the differential input clock [62] and retime the 25% non-overlapping signals with the reference clock.

VI. CONCLUSION

This article presents the first cryo-CMOS controller targeting color-center-based quantum processors. This article discusses the unique challenges that color-center-based quantum processors face, and the requirements for achieving high-fidelity gates. It also provides a design guide for a novel AC controller with a class-DE output stage, which achieves high AC levels with excellent current efficiency, as summarized in Table III. The controller uses simple digital circuits for time and phase control of rectangular pulses. Similarly, the design of a new DC CR based on a triode-biased H-bridge is explained, which is used to drive large currents through a coil to actively tune the Larmor frequency into the resonance of the AC controller, without introducing observable infidelity. Both circuits have been extensively characterized with an NV-center qubit, showing no significant degradation in qubit performance introduced by the cryo-CMOS control, as intended with the target circuit specifications. The proposed

[11] A π-rotation on all three nitrogen states is driven. The exponential decay is present on all states, but two-third of the population is detuned with ∼2 MHz due to the nitrogen splitting, causing the visible oscillation between 0 and 2/3 [55].

circuits will enable more efficient qubit control in future 3-D-integrated color-center-based quantum processors, propelling the scaling of quantum computers toward a practical computational breakthrough.

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REFERENCES

[1] F. Arute et al., "Quantum supremacy using a programmable superconducting processor," *Nature*, vol. 574, no. 7779, pp. 505–510, 2019.

[2] Y. Kim et al., "Evidence for the utility of quantum computing before fault tolerance," *Nature*, vol. 618, no. 7965, pp. 500–505, Jun. 2023.

[3] Z. Li et al., "Error per single-qubit gate below 10–4 in a superconducting qubit," *NPJ Quantum Inf.*, vol. 9, no. 1, pp. 1–6, Nov. 2023.

[4] R. Barends et al., "Coherent Josephson qubit suitable for scalable quantum integrated circuits," *Phys. Rev. Lett.*, vol. 111, no. 8, Aug. 2013, Art. no. 080502.

[5] R. Barends et al., "Superconducting quantum circuits at the surface code threshold for fault tolerance," *Nature*, vol. 508, no. 7497, pp. 500–503, 2014.

[6] J. Yoo et al., "Design and characterization of a <4-mW/Qubit 28-nm cryo-CMOS integrated circuit for full control of a superconducting quantum processor unit cell," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 3044–3059, Nov. 2023.

[7] D. J. Frank et al., "A cryo-CMOS low-power semi-autonomous qubit state controller in 14nm FinFET technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2022, pp. 360–362.

[8] J. Park et al., "A fully integrated cryo-CMOS SoC for state manipulation, readout, and high-speed gate pulsing of spin qubits," *IEEE J. Solid-State Circuits*, vol. 56, no. 11, pp. 3289–3306, Nov. 2021.

[9] B. Patra, J. P. van Dijk, and S. Subramanian, "A scalable cryo-CMOS 2-to-20 GHz digitally intensive controller for 4×32 frequency multiplexed spin qubits/transmons in 22nm FinFET technology for quantum computers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 304–306.

[10] B. Prabowo et al., "29.3 A cryo-CMOS receiver with 15K noise temperature achieving 9.8dB SNR in 10μs integration time for spin qubit readout," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 474–476.

[11] S. Krinner et al., "Engineering cryogenic setups for 100-qubit scale superconducting circuit systems," *EPJ Quantum Technol.*, vol. 6, no. 1, pp. 1–29, Dec. 2019.

[12] M. W. Doherty, N. B. Manson, P. Delaney, F. Jelezko, J. Wrachtrup, and L. C. L. Hollenberg, "The nitrogen-vacancy colour centre in diamond," *Phys. Rep.*, vol. 528, no. 1, pp. 1–45, Jul. 2013.

[13] S. Pezzagna and J. Meijer, "Quantum computer based on color centers in diamond," *Appl. Phys. Rev.*, vol. 8, no. 1, pp. 011308-1–011308-17, Mar. 2021.

[14] M. Ruf, N. H. Wan, H. Choi, D. Englund, and R. Hanson, "Quantum networks based on color centers in diamond," *J. Appl. Phys.*, vol. 130, no. 7, pp. 070901-1–070901-20, Aug. 2021.

[15] H. P. Bartling et al., "Universal high-fidelity quantum gates for spin-qubits in diamond," 2024, *arXiv:2403.10633*.

[16] B. Hensen et al., "Loophole-free bell inequality violation using electron spins separated by 1.3 kilometres," *Nature*, vol. 526, no. 7575, pp. 682–686, 2015.

[17] S. Hermans, M. Pompili, H. Beukers, S. Baier, J. Borregaard, and R. Hanson, "Qubit teleportation between non-neighbouring nodes in a quantum network," *Nature*, vol. 605, no. 7911, pp. 663–668, 2022.

[18] S. Storz et al., "Loophole-free bell inequality violation with superconducting circuits," *Nature*, vol. 617, no. 7960, pp. 265–270, May 2023.

[19] R. Ishihara et al., "3D integration technology for quantum computer based on diamond spin qubits," in *IEDM Tech. Dig.*, Dec. 2021, pp. 14.5.1–14.5.4.

[20] I. Filippov et al., "Superconducting TSV contact for cryoelectronic devices," *Superconductor Sci. Technol.*, vol. 37, no. 1, Jan. 2024, Art. no. 015018.

[21] M. I. Ibrahim, C. Foy, D. R. Englund, and R. Han, "High-scalability CMOS quantum magnetometer with spin-state excitation and detection of diamond color centers," *IEEE J. Solid-State Circuits*, vol. 56, no. 3, pp. 1001–1014, Mar. 2021.

[22] J. Wang, I. B. Harris, X. Chen, D. R. Englund, and R. Han, "A CMOS-integrated color center pulse-sequence control and detection system," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2024, pp. 1–2.

[23] M. I. Ibrahim and R. Han, "Cryo-CMOS controller for solid-state color-center qubits towards scalable quantum processors," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2021, pp. 1–2.

[24] L. Enthoven, M. Babaie, and F. Sebastiano, "Optimizing the electrical interface for large-scale color-center quantum processors," *IEEE Trans. Quantum Eng.*, vol. 5, pp. 1–17, 2024.

[25] S. Meesala et al., "Strain engineering of the silicon-vacancy center in diamond," *Phys. Rev. B, Condens. Matter*, vol. 97, no. 20, 2018, Art. no. 205444.

[26] L. C. Bassett, F. J. Heremans, C. G. Yale, B. B. Buckley, and D. D. Awschalom, "Electrical tuning of single nitrogen-vacancy center optical transitions enhanced by photoinduced fields," 2011, *arXiv:1104.3878*.

[27] L. Enthoven et al., "29.2 A cryo-CMOS controller with class-DE driver and DC magnetic-field tuning for color-center-based quantum computers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 472–474.

[28] J. P. G. van Dijk et al., "Impact of classical control electronics on qubit fidelity," *Phys. Rev. Appl.*, vol. 12, no. 4, p. 1, Oct. 2019.

[29] J. P. G. van Dijk, B. Patra, S. Pellerano, E. Charbon, F. Sebastiano, and M. Babaie, "Designing a DDS-based SoC for high-fidelity multi-qubit control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 5380–5393, Dec. 2020.

[30] M. S. Everitt, S. Devitt, W. J. Munro, and K. Nemoto, "High-fidelity gate operations with the coupled nuclear and electron spins of a nitrogen-vacancy center in diamond," *Phys. Rev. A, Gen. Phys.*, vol. 89, no. 5, May 2014, Art. no. 052317.

[31] J. Gong, E. Charbon, F. Sebastiano, and M. Babaie, "A cryo-CMOS PLL for quantum computing applications," *IEEE J. Solid-State Circuits*, vol. 58, no. 5, pp. 1362–1375, May 2023.

[32] W. Yang, W.-L. Ma, and R.-B. Liu, "Quantum many-body theory for electron spin decoherence in nanoscale nuclear spin baths," *Rep. Prog. Phys.*, vol. 80, no. 1, 2016, Art. no. 016001.

[33] T. J. Green, J. Sastrawan, H. Uys, and M. J. Biercuk, "Arbitrary quantum control of qubits in the presence of universal noise," *New J. Phys.*, vol. 15, no. 9, Sep. 2013, Art. no. 095004.

[34] M. Babaie and R. B. Staszewski, "An ultra-low phase noise class-F 2 CMOS oscillator with 191 dBc/Hz FoM and long-term reliability," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 679–692, Mar. 2015.

[35] M. K. Kazimierczuk, "Class DE RF power amplifier," in *RF Power Amplifiers*. Hoboken, NJ, USA: Wiley, 2014, pp. 322–339.

[36] S.-M. Yoo, J. S. Walling, E. C. Woo, B. Jann, and D. J. Allstot, "A switched-capacitor RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2977–2987, Dec. 2011.

[37] P. A. 't Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Subthreshold mismatch in nanometer CMOS at cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 797–806, 2020.

[38] N. O. Sokal and A. D. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. SSC-10, no. 3, pp. 168–176, Jun. 1975.

[39] F. Raab, "Idealized operation of the class e tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. CS-24, no. 12, pp. 725–735, Dec. 1977.

[40] M. Kazimierczuk, "Collector amplitude modulation of the class E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. CS-31, no. 6, pp. 543–549, Jun. 1984.

[41] S.-A. El-Hamamsy, "Design of high-efficiency RF class-D power amplifier," *IEEE Trans. Power Electron.*, vol. 9, no. 3, pp. 297–308, May 1994.

[42] A. Grebennikov, N. Sokal, and M. Franco, *Switchmode RF Power Amplifiers*. (Communications Engineering Series). Amsterdam, The Netherlands: Elsevier, 2011.

[43] M. Albulet, "An exact analysis of class-DE amplifier at any output Q," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 46, no. 10, pp. 1228–1239, Oct. 1999.

[44] P. A. T. Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and modeling of mismatch in cryo-CMOS," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 263–273, 2020.

[45] K.-H. Chen, *Power Management Techniques for Integrated Circuit Design*, 1st ed., Singapore: Wiley, 2016, pp. 28–121. https://doi.org/10.1002/9781118896846.ch2

[46] R. W. J. Overwater, M. Babaie, and F. Sebastiano, "Cryogenic-aware forward body biasing in bulk CMOS," *IEEE Electron Device Lett.*, vol. 45, no. 2, pp. 152–155, Feb. 2024.

[47] G. Kiene, S. Ilik, L. Mastrodomenico, M. Babaie, and F. Sebastiano, "Cryogenic characterization of low-frequency noise in 40-nm CMOS," 2024, *arXiv:2405.17685*.

[48] G. Ge, C. Zhang, G. Hoogzaad, and K. A. Makinwa, "A single-trim CMOS bandgap reference with a 3σ inaccuracy of $\pm$0.15% from 40 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2693–2701, Oct. 2011.

[49] N. Fakkel et al., "Data underlying the publication: A cryo-CMOS controller with class-DE driver and DC magnetic-field tuning for quantum computers based on color centers in diamond," Delft Univ. Technol., Delft, The Netherlands, Tech. Rep., 2024, doi: 10.4121/697f7796-ba50-424f-bc08-1e14ac41f003.

[50] *Langer EMV-ICR HH100-6 Set, Near-Field Microprobe 2.5 MHz-6 GHz*. Accessed: Apr. 15, 2024. [Online], Available: https://www.langer-emv.de/en/product/near-field-microprobe-sets-icr-hh-h-field/133/icr-hh100-6-set-near-field-microprobe-2-5-mhz-6-ghz/758

[51] C. E. Bradley et al., "A ten-qubit solid-state spin register with quantum memory up to one minute," *Phys. Rev. X*, vol. 9, no. 3, Sep. 2019, Art. no. 031045.

[52] *System User Manual Cryostation S-Series*, Version 3.7, Montana Instruments, Bozeman, MT, USA, Oct. 2023.

[53] C. E. Bradley et al., "Robust quantum-network memory based on spin qubits in isotopically engineered diamond," *NPJ Quantum Inf.*, vol. 8, no. 1, p. 122, Oct. 2022.

[54] W. Pfaff, "Quantum measurement and entanglement of spin quantum bits in diamond," Ph.D. thesis, Dept. Quantum Nanosci., Appl. Sci., Delft Univ. Technol., Delft, The Netherlands, Dec. 2013, doi: 10.4233/uuid:62208a4a-72c6-45b5-af51-1a8e8f8bfdd8.

[55] Y. Yang et al., "Observing hyperfine interactions of NV-centers in diamond in an advanced quantum teaching lab," *Amer. J. Phys.*, vol. 90, no. 7, pp. 550–560, Jul. 2022.

[56] L. Childress et al., "Coherent dynamics of coupled electron and nuclear spin qubits in diamond," *Science*, vol. 314, no. 5797, pp. 281–285, Oct. 2006.

[57] B. J. Shields, Q. P. Unterreithmeier, N. P. de Leon, H. Park, and M. D. Lukin, "Efficient readout of a single spin state in diamond via spin-to-charge conversion," *Phys. Rev. Lett.*, vol. 114, no. 13, Mar. 2015, Art. no. 136402.

[58] M. H. Abobeih et al., "One-second coherence for a single electron spin coupled to a multi-qubit nuclear-spin environment," *Nature Commun.*, vol. 9, no. 1, p. 2552, Jun. 2018.

[59] J. Helsen, I. Roth, E. Onorati, A. H. Werner, and J. Eisert, "General framework for randomized benchmarking," *PRX Quantum*, vol. 3, no. 2, Jun. 2022, Art. no. 020357.

[60] E. Nielsen, J. K. Gamble, K. Rudinger, T. Scholten, K. Young, and R. Blume-Kohout, "Gate set tomography," *Quantum*, vol. 5, p. 557, Oct. 2021.

[61] *Mini-Circuits, NCR2-113+ Datasheet*. Accessed: Jun. 5, 2024. [Online], Available: https://www.minicircuits.com/pdfs/NCR2-113+.pdf

[62] Z. Toprak-Deniz et al., "A 128-Gb/s 1.3-pJ/b PAM-4 transmitter with reconfigurable 3-tap FFE in 14-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 1, pp. 19–26, Jan. 2020.

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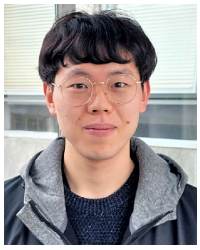

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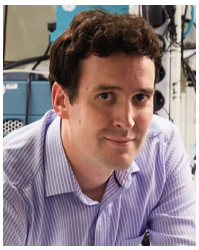

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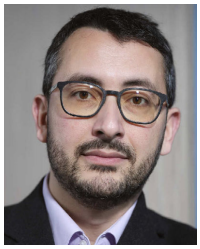

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