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A $\pm$36A Integrated Current-Sensing System with 0.3% Gain Error and 400μA Offset from -55°C to $+85$°C

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Abstract

This paper presents an integrated shunt-based current-sensing system (CSS) capable of handling $\pm$36 A currents, the highest ever reported. It also achieves 0.3% gain error and 400 μA offset, which is significantly better than the state-of-the-art. The heart of the system is a robust 260 $\mu\Omega$ shunt resistor made from the lead-frame of a standard HVQFN plastic package. The resulting voltage drop is then digitized by a precision $\Delta\Sigma$ ADC and a bandgap reference (BGR). At the expense of current handling capability, a $\pm$5 A version of the CSS uses a 10 mΩ on-chip metal shunt to achieve just 4 μA offset. Both designs are realized in a standard 0.13 μm CMOS process and draw 13 μA from a 1.5 V supply. Compensation of the spread and non-linear temperature dependency of the shunt resistor R_{shunt} is accomplished by the use of a fixed polynomial master curve

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and a single room-temperature calibration. This procedure also effectively compensates for the residual spread and non-linearity of the ADC and the BGR.

Index Terms

Current-sensing system (CSS), lead-frame shunt resistor, dynamic bandgap reference (BGR), temperature compensation, temperature sensor.

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I. Introduction

Current-sensing systems (CSS) are widely used in many industrial applications, such as motor controllers, battery fuel gauges, and energy monitoring systems [1]–[15]. Inductive sensors (e.g., Rogowski coils and current transformers) and magnetic field sensors (based on magneto- resistances, on fluxgates, or on Hall effect) [1]–[7] provide galvanic isolation and can safely operate in high-voltage environments. However, inductive sensors cannot sense DC currents, and both inductive and magnetic field sensors are substantially more complex than shunt-based sensors, which sense current by measuring the voltage drop across a shunt resistor R_{shunt} [9]–[15]. Their simplicity results in greater accuracy and resolution, and makes them amenable to integration [1], [15].

However, existing systems based on *integrated* shunt resistors typically exhibit more than 3% gain error and several milliamperes of offset [10]–[14]. Their gain error is mainly due to inadequate compensation of the shunt resistor's spread and temperature coefficient of resistance (TCR), while their current offset is limited by the readout electronics. By means of precision readout electronics and an on-chip metal shunt, we recently demonstrated a $\pm$5A CSS achieving a $\pm 0.35\%$ gain error and 16 μA offset [15]. However, in order to reliably handle currents of up to 5 A, the metal shunt was quite wide (700 μm) and occupied significant die area (0.4 mm^2). Furthermore, as shown in Fig. 1, it exhibits significant (0.1%) drift after long-term (24 day) testing at high temperatures ($+85$°C) and currents (5 A DC). This is due to electromigration, and can thus be mitigated by reducing the current-density and temperature of the shunt [16], [17], either by increasing its area, or by reducing its maximum operating current and/or temperature.

An alternative approach is to use the lead-frame of a package to implement the shunt resistor [10], [18], [19]. This costs no extra die area and increases both the shunt's current range and robustness since typical lead-frames are orders of magnitude thicker than on-die metal layers. In [10], [19], the effect of the lead-frame's large TCR ($\sim 0.335\%$/°C), is addressed by amplifying the voltage

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across the shunt V_{shunt} with a gain that has an equal-but-opposite temperature coefficient. However, the resulting gain error is still significant ($\pm 3\%$ over a ± 15 A current range) [10].

Rather than designing a precise temperature compensation scheme, yet another approach is to make the lead-frame from low-TCR (< 20 ppm/°C) alloys, such as Constantan, Manganin, or Evanohm [20], [21]. A design employing a low-TCR in-package shunt [9] achieves an offset of 50 mA and gain error of $\pm 0.75\%$ over a ± 10 A current range. However, a custom package is needed to accommodate the shunt, which increases production costs.

We recently presented a CSS [22] that achieved much better accuracy while still using a proof-of-concept lead-frame shunt made from the heatsink of a standard QFN package. Its block diagram is shown in Fig. 2. It contains a bandgap reference (BGR) and two switched-capacitor (SC) 2^{nd}-order $\Delta\Sigma$ ADCs; ADC_I digitizes V_{shunt} with respect to the BGR voltage V_{Ref}, and ADC_T uses the BGR's PNPs to sense the shunt's temperature *T*.

Compared to our previous work [15], in which a single ADC was time-multiplexed between current and temperature measurements, this work uses two separate ADCs. This enables continuous current and temperature sensing, leading to a faster and more accurate response to large current transients. In addition, by using an energy-efficient design methodology and fringe capacitors, its power consumption and area are reduced by about $4\times$ and $2\times$ compared to [15], for the same performance. Finally, it uses a significantly simpler calibration scheme, while preserving accuracy.

The rest of the paper is organized as follows. The implementation details of the shunts and of the readout electronics are presented in Section II and III, respectively. Section IV describes the calibration scheme, while Section V demonstrates how several errors in the readout circuitry are absorbed in the calibration process and significantly reduced. Experimental results are presented in Section VI. Section VII concludes the paper.

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II. Shunt Resistor

Inserting a shunt resistor into a current path inevitably gives rise to extra resistance and thus power loss. Choosing the value of R_{shunt} then involves a compromise between power loss and the magnitude of the voltage drop V_{shunt}, and hence, between current-sensing offset and resolution. The value of R_{shunt} is typically chosen to be of the same order of magnitude as the wiring resistance, which, depending on the application, ranges from sub-mΩ values in [1] to a few [9]–[12] or even tens of mΩ in [13], [14].

As described in Section I, the main limitations of an on-chip metal shunt are its large area and long-term drift. The latter can be alleviated by reducing the current range and/or the maximum operating temperature. Although this is acceptable for some applications, a superior solution is to use a lead-frame shunt. This extends current-sensing range without increasing die area. This section describes the design of the lead-frame and on-chip shunts used in this work.

A. *Lead-frame Shunt*

As shown in Fig. 3, the lead-frame shunt is implemented by using the heatsink of a small (3 $\times$ 6 $\times$ 0.85 mm^3) thermally enhanced 32-pin QFN plastic package (HVQFN32). The die is glued to the lead-frame and senses the voltage drop V_{shunt} between the Kelvin-contacted points S1 and S2. This approach avoids the costs associated with the design of a custom lead-frame shunt at the expense of a fixed resistance. The resulting shunt has a nominal value of 260 $\mu\Omega$ at room temperature, whose spread (due to, e.g., spread in the lead-frame thickness or in the location of the Kelvin-contacted points) is corrected by a room-temperature calibration.

Compared to an on-chip shunt, whose maximum current is limited by electromigration, the lead-frame shunt is quite thick and so its maximum current is mainly limited by the maximum allowable die temperature. Measurements show that passing a 36 A current through the lead-frame

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shunt results in a temperature rise of $\sim 50°C$[1], which translates into a maximum die temperature of 135°C at the maximum ambient temperature of 85°C. This results in a significant measurement error, since the shunt has a TCR of about 0.3%/°C. This effect is counteracted by a digital temperature compensation scheme, which involves measuring the shunt's temperature and then correcting for its known TCR in the digital domain (Fig. 2).

At a temperature T, the resistance of the shunt R_{shunt} can be approximated as:

$$R_{\text{shunt}}(T) = R_{\text{shunt}}(T_0) \cdot \left(1 + \alpha_1 \cdot (T - T_0) + \alpha_2 \cdot (T - T_0)^2\right) \tag{1}$$

where α_1 and α_2 are the resistor's 1^{st}- and 2^{nd}-order temperature coefficients, and T_0 is the temperature at which the shunt is calibrated. Since T_0 is also measured by the on-chip temperature sensor, this calibration does not need to be performed in a temperature-stabilized environment, thus reducing the calibration time and cost. Section IV describes the calibration process in detail.

It should be noted that, in this prototype, shifts in the orientation of the heatsink on the PCB, and thus in the exact locations where current enters and leaves the shunt, may cause small changes in $R_{\text{shunt}}(T_0)$. Like its spread, this is corrected by room-temperature calibration. However, this implies that the end user must calibrate the sensor after it has been soldered to the PCB, which may not be desirable. A custom lead-frame design would avoid this issue by ensuring that its sensing section, i.e. the section between the Kelvin contacts, is located some distance away from the actual soldering pins of the package, [7].

Good thermal coupling between the shunt and the temperature sensor is essential to accurately measure and thus compensate for the shunt's Joule heating. To investigate this, electro-thermal simulations were carried out in COMSOL. The simulation setup, including the dimensions of the various elements, is shown in Fig. 4. For the sake of simplicity, only the shunt, silicon die and the current-conducting PCB traces are included in this model. The die was assumed to have a thickness

[1]Some of this self-heating arose in our test PCB and could be improved by a better thermal design.

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of $\sim$ 200 μm after being back ground to fit into the HVQFN package. A coefficient h = 5 W/m^{2}K of convective heat transfer was used for the top surface of the PCB traces, which are assumed to be in perfect thermal contact with the lead frame, and whose far ends were assumed to be at room temperature.

The simulated temperature rise on the upper surface of the shunt at I = 36 A is illustrated in Fig. 5(a), while the temperature profile along the AA$'$ axis is shown in Fig. 5(b). The simulations predict an average temperature rise of about 43°C, which is in good agreement with measurement results. As expected, the self-heating peaks in the middle of the shunt and tapers off towards the points where it is attached to the PCB trace. The simulations also show that the difference between the average temperature of the shunt and that of the PNPs is only about 0.4°C, corresponding to a negligible 0.1% current-sensing gain error. As shown in Fig. 6, even though the shunt's temperature rise and its relative curvature are influenced by the dimensions of the PCB trace, its overlap with the lead-frame, and its ability to conduct heat away from the chip, these factors hardly affect the temperature difference between the shunt and the PNPs. These results indicate that a custom lead-frame shunt can be used as a low-cost and robust shunt in high-current sensing applications.

B. On-chip Metal Shunt

A $\pm$5A version of the CSS based on a 10 mΩ on-chip metal shunt (Fig. 7) was also implemented. This shunt is quite similar to that used in our previous work [15]. However, in [15] the insulating oxide between the metal shunt and the substrate-PNPs gave rise to errors in the estimated T, which were then corrected by an extra calibration step. In this work, thermal vias between the shunt and the gates of dummy PMOS devices improve (by $\sim 2\times$) the thermal coupling between the shunt and the substrate and reduce shunt self-heating, while preserving galvanic isolation. The result is better accuracy with a simpler calibration procedure.

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III. Readout Electronics

In this section, the readout electronics, which consists of a BGR and two ADCs (Fig. 2), is described. The digital backend was implemented off-chip.

A. Bandgap Reference

The bandgap reference (BGR) provides the ADCs' reference voltage V_{Ref} and senses the shunt's temperature *T*. As shown in the simplified circuit diagram of Fig. 8, it consists of a bias circuit and a bipolar core. The bias circuit generates a PTAT current *I* = 260 nA (at 27°C) with the help of an opamp and two auxiliary PNPs biased at a 1:*p* (= 10) current-density ratio. This current is then mirrored (1:8) to the bipolar core, and used to bias two other PNPs also at 1:10 current density ratio to generate V_{BE} and ΔV_{BE} [15], [23], [24] as

$$V_{\mathrm{BE}} = V_{g0} - \lambda T, \tag{2}$$

$$\Delta V_{\mathrm{BE}} = \frac{kT}{q}\ln(p), \tag{3}$$

in which, V_{g0} ($\approx$ 1.2V) is the silicon bandgap voltage, λ is the V_{BE} temperature coefficient, *k* is Boltzmann's constant, *T* is the absolute temperature, and *q* is the electron charge. These voltages are then sampled and linearly combined in the $\Delta\Sigma$ ADCs to generate a dynamic reference voltage

$$V_{\mathrm{Ref}} = \Delta V_{\mathrm{BE}} + \frac{V_{\mathrm{BE}}}{\alpha} \approx \frac{V_{g0}}{\alpha} = V_{\mathrm{Ref0}}, \tag{4}$$

where the ratio α (= 10) is realized by the ADCs' sampling capacitors [24]. In order to obtain a constant V_{Ref} over temperature, it is ensured that $\lambda = \alpha\frac{k}{q}\ln(p)$. The shunt's temperature is measured by digitizing ΔV_{BE} with respect to V_{Ref}.

To decrease the spread in *I*, and hence in V_{BE}, the opamp's offset is reduced by chopping, while ΔV_{BE} is made accurate by dynamically matching both the current sources and the PNPs [15], [25]. In order to prevent the voltage drop across the DEM switches ($\mathrm{SW_{DEM}}$) from corrupting V_{BE} and ΔV_{BE} and then causing significant errors in V_{Ref} and *T*, Kelvin-connected switches are used [15].

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Another source of error is the spread in the PNP's saturation current $I_{\rm sat}$, which leads to a $\pm 1\%$ PTAT spread in $V_{\rm BE}$ and hence in $V_{\rm Ref}$ [27], [28]. Also, since $V_{\rm BE}$ has a nonlinear temperature characteristic or curvature, $V_{\rm Ref}$ exhibits a corresponding curvature error of about $\pm 0.2\%$ [28], [29]. Taking these non-idealities into account, $V_{\rm BE}$ can be expressed as [23]

$$V_{\rm BE} = V_{g0}(1 + \delta\frac{T}{T_c}) - \lambda T + c(T) - c(0), \tag{5}$$

in which, δ represents its PTAT error term measured at a temperature T_c, and $c(T)$ is its curvature. By combining (4) and (5), the reference voltage can then be written as

$$V_{\rm Ref}(T) = V_{\rm Ref0}\Big(1 + \delta\frac{T}{T_c}\Big) + \frac{c(T) - c(0)}{\alpha}. \tag{6}$$

Sections IV and V describe how the effect of these non-idealities on CSS performance are mitigated.

B. ADC

The CSS employs two $2^{\rm nd}$-order SC feed-forward $\Delta\Sigma$ ADCs; $\rm ADC_{\mathit{I}}$ digitizes $V_{\rm shunt}$ and $\rm ADC_{\mathit{T}}$ digitizes *T*. Fig. 9 shows a simplified diagram of $\rm ADC_{\mathit{I}}$, in which capacitor C_{S1} (= 3 pF) samples $V_{\rm shunt}$, while capacitors C_{S2} (= 3 pF) and C_{S3} (= 300 fF), sample and accurately combine $\Delta V_{\rm BE}$ and $V_{\rm BE}$, respectively, to generate $V_{\rm Ref}$ [22]. The modulator's feedback is established by using the output bitstream $\rm bs_{\mathit{I}}$ to control the polarity of the feedback voltages $\pm\Delta V_{\rm BE}$ and $\pm V_{\rm BE}$. This conversion results in an output bit-stream $\rm bs_{\mathit{I}}$ with an average value

$$\mu_I = \frac{C_{S1}\cdot R_{\rm shunt}(T)\cdot I}{C_{S2}\cdot\Delta V_{\rm BE} + C_{S3}\cdot V_{\rm BE}} = \frac{R_{\rm shunt}(T)\cdot I}{V_{\rm Ref}} = \frac{V_{\rm shunt}}{V_{\rm Ref}}. \tag{7}$$

The leakage current of $\rm ADC_{\mathit{I}}$'s input sampling switches can be added to $V_{\rm shunt}$ and cause a large error ($> 0.5\%$) in current sensing at high temperatures and negative currents [15]. To tackle this issue, the input switches were realized as low-leakage high-$V_{\rm th}$ NMOS transistors. In addition the gates of the "off" switches are driven by the lowest available voltage, i.e. by ground when $I > 0$, and by ${V_{\rm shunt}}^{+}$ when $I < 0$ [15]. Simulations show that this scheme reduces the worst-case gain error due to $I_{\rm leak}$ by more than 60 times: to $< 0.01\%$.

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Fig. 10 shows a simplified diagram of ADC_T, in which T is digitized by charge-balancing ΔV_{BE} against $-V_{\mathrm{BE}}/10$. When bs_T is 0, C_{S4} (= 1 pF) samples $+\Delta V_{\mathrm{BE}}$ and when bs_T is $+1$, C_{S5} (= 100 fF) samples $-V_{\mathrm{BE}}$. This results in an average value of bs_T equal to

$$\mu_T = \frac{C_{S4} \cdot \Delta V_{\mathrm{BE}}}{C_{S4} \cdot \Delta V_{\mathrm{BE}} + C_{S5} \cdot V_{\mathrm{BE}}} = \frac{\Delta V_{\mathrm{BE}}}{V_{\mathrm{Ref}}}. \tag{8}$$

The temperature T in degrees Celsius is then obtain by linearly scaling μ_T [25]

$$T = A \cdot \mu_T - B \tag{9}$$

in which, $A \approx 611$ and $B \approx 273$.

Both ADCs are operated at a sampling frequency f_S = 100 kHz. To mitigate the first integrators' offset and $1/f$ noise, CDS and low-frequency chopping (CHL) are used. All four integrators employ current-reuse amplifiers (Fig. 9) with fringe capacitors. Compared to the use of folded-cascode OTA with metal sandwich capacitors in [15], these changes help to reduce power consumption and area by $4\times$ and $2\times$, respectively.

IV. Calibration

This section describes the calibration process and the digital backend computation used in the CSS. Unlike previous precision temperature sensors [25], [26], [30], BGRs [24], [31], and CSSs [15], [22], [28], [29], neither the PTAT error in V_{BE} nor its curvature is explicitly corrected in this work. In addition, unlike [24]–[26], [30], the mismatch between the ADC's sampling capacitors is also not corrected. Instead, R_{shunt} spread and other static errors are corrected by a room-temperature calibration, while the shunt's non-linear TCR and V_{BE} curvature are corrected by a fixed polynomial established by a batch calibration. It will be shown (in Section V) that this approach effectively compensates for all the major sources of error. It significantly simplifies both the circuit implementation and the calibration of the CSS, and thus reduces its production cost.

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There are two sets of calibration data. The shunt's resistance at the calibration temperature $R_{\mathrm{shunt}}(T_0)$ is unique for each device and is referred to as individual calibration data, meaning that it is obtained by calibrating individual devices. All the other parameters (V_{Ref0}, A, B, α_1, α_2, and T_0) are common to all devices and are referred to as batch-calibration data, meaning that they are obtained by calibrating several devices and then averaging the results.

A. Calibration Process

The batch-calibration data is obtained by characterizing all samples over temperature T as follows:

1) Determining V_{Ref0}, A, and B: a known external voltage is applied to ADC_I, while the CSS produces $\mu_T(T)$ and $\mu_I(T)$. By substituting $\mu_I(T)$ in (7), $V_{\mathrm{Ref}}(T)$ can be obtained, the room-temperature value of which is defined as V_{Ref0}. During the rest of the calibration, the simplifying assumption is made that $V_{\mathrm{Ref}}(T) = V_{\mathrm{Ref0}}$. By substituting $\mu_T(T)$ in (9) and using a linear fit, A and B can be obtained.
2) Determining α_1, α_2, and T_0: a known current *I* is passed through the shunt[2], while the CSS measures $\mu_T(T)$ and $\mu_I(T)$. From (9), the shunt's temperature can be obtained, the room-temperature value of which is denoted as T_0. By substituting I, V_{Ref0}, and $\mu_I(T)$ into (7), $R_{\mathrm{shunt}}(T)$ is obtained. The temperature coefficients α_1 and α_2 are then determined by fitting $R_{\mathrm{shunt}}(T)$ to a 2^{nd}-order polynomial.

After obtaining the batch-calibrated data, all the chips are then individually calibrated at room temperature as follows:

1) Determining the shunt resistance $R_{\mathrm{shunt}}(T_0)$ at room temperature: a known current *I* is passed through the shunt, while the ADC measures $\mu_T(T_1)$ and $\mu_I(T_1)$. It should be noted that the shunt temperature T_1 will probably not be equal to the T_0 from the previous step. This is due

[2]In this work, the calibration current is chosen as 3 A for the on-chip shunt and 5 A for the lead-fame shunt.

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to the spread in the shunt's self-heating and ambient temperature variations (in order to save the calibration time and cost, this calibration step is done in an unstabilized room-temperature environment).

By substituting $\mu_T(T_1)$ into (9), the shunt temperature T_1 can be calculated. $R_{\rm shunt}(T_1)$ can also be calculated by putting I, $V_{\rm Ref0}$ and $\mu_I(T_1)$ into (7). Finally, $R_{\rm shunt}(T_0)$ can be obtained by using (1).

It should be noted that this last step is necessary as α_1 and α_2 for a given shunt, will depend on T_0.

In normal operation, I is then measured by substituting the calibration data and the ADCs' output $\mu_T(T)$ and $\mu_I(T)$ into (9), (1) and (7).

V. Calibration Evaluation

The effect of uncorrected error sources on the CSS accuracy is analyzed in this section. First these error sources are introduced as follow.

1) In ADC_I, the two sampling capacitors C_{S1} and C_{S2} are nominally equal; their mismatch, however, can be regarded as a gain error δ_g applied to the ADC_I's reference voltage

$$\frac{C_{S2}}{C_{S1}} = 1 + \delta_g. \tag{10}$$

2) Any mismatch between C_{S2} and C_{S3} leads to a spread in the α factor of ADC_I

$$\frac{C_{S2}}{C_{S3}} = \alpha \cdot (1 + \delta_{\alpha I}). \tag{11}$$

3) The same holds for the mismatch between C_{S4} and C_{S5} in ADC_T

$$\frac{C_{S4}}{C_{S5}} = \alpha \cdot (1 + \delta_{\alpha T}). \tag{12}$$

4) The spread in PNP's current density ratio, Δp, leads to a PTAT error in $\Delta V_{\rm BE}$ [23]

$$\Delta V_{\rm BE} = \frac{kT}{q}\ln(p) \cdot \Big(1 + \delta_p\Big) \qquad \Big(\delta_p \approx \frac{1}{\ln(p)}\frac{\Delta p}{p}\Big). \tag{13}$$

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5) Since analyzing the effect of curvature is rather cumbersome, we will ignore its effect for the moment, and assume that $V_{\rm BE}$ exhibits no curvature. Nevertheless, $c(T)$ will be taken into account in a follow-up MATLAB simulation, and it will be shown that it has a negligible effect on the CSS accuracy. This because $c(T)$ is constant for a given design, even over different batches [15], [31], and so it introduces a constant non-linearity in the measured *T* and $R_{\rm shunt}$. The impact of this non-linearity on the CSS accuracy can then be alleviated by appropriately adjusting α_1 and α_2.
6) Therefore, for the purpose of our analysis $V_{\rm BE}$ can be written as

$$V_{\rm BE}(T) \approx V_{g0} \cdot \Big(1 + \delta\frac{T}{T_c}\Big) - \lambda T. \tag{14}$$

At the presence of these errors, ADC_I's output can be obtained by rewriting (7)

$$\mu_I'(T) \approx \alpha\frac{R_{\rm shunt}(T)\cdot I}{V_{g0}(1-\delta_{\alpha I}+\delta_g) + \Big(\alpha\frac{k}{q}\ln(p)\delta_p + \lambda\delta_{\alpha I} + \frac{V_{g0}}{T_c}\delta\Big)T} = \frac{R_{\rm shunt}(T)\cdot I}{V_{\rm Ref0}{}'}. \tag{15}$$

In the rest of the paper, the "prime" sign, $'$, is used to indicate the *measured* value of the corresponding parameter which is corrupted by the error sources. Similarly, by rewriting (8), ADC_T's output can be expressed as

$$\mu_T'(T) \approx \frac{\alpha\frac{kT}{q}\ln(p)}{V_{g0}}\Big(1+\delta_{\alpha T}+\delta_p - \frac{\lambda T}{V_{g0}}(\delta_{\alpha T}+\delta_p) - \frac{T}{T_c}\delta\Big). \tag{16}$$

During the first step of the calibration process, $V_{\rm Ref0}$ is obtained by taking the average of the measured reference voltage of ADC_Is at room temperature. Assuming that *N* samples are measured, and considering that the error terms have a zero mean value, $V_{\rm Ref0}$ can be calculated from (15) as

$$V_{\rm Ref0} = \frac{1}{N}\sum_{i=1}^{N} V_{\rm Ref0,\mathit{i}}{}' \approx \frac{V_{g0}}{\alpha} \tag{17}$$

which is equal to its nominal value. It can also be shown that the parameters A and B, obtained from averaging the linear fit of (16), are equal to their nominal values as

$$A = \frac{V_{g0}}{\alpha\frac{k}{q}\ln(p)}, \qquad \text{and} \qquad B = -273.15°C. \tag{18}$$

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by combining (16) and (18), the measured shunt calibration temperature T_0' in Kelvin is

$$T_0' = A\mu_T'(T_0) \approx T_0\Big(1 + \delta_{\alpha T} + \delta_p - \frac{\lambda T_0}{V_{g0}}(\delta_{\alpha T} + \delta_p) - \frac{T_0}{T_c}\delta\Big) \tag{19}$$

Averaging the measured calibration temperature (19) results in[3]

$$T_0'' = \frac{1}{N}\sum_{i=1}^{N} T_{0,i}' \approx T_0 \tag{20}$$

which is equal to the nominal temperature T_0.

Similarly, it can be shown that α_1 and α_2 are not influenced by the uncalibrated error terms as their effects are averaged out. However, the individual calibration data will be impacted since they are obtained by measurement on each sample.

By using (15) and (17), the *measured* shunt value at the *measured* calibration temperature $R_{\text{shunt}}'(T_0')$ is obtained as

$$R_{\text{shunt}}'(T_0') = \frac{\mu_I'(T_0)\cdot V_{\text{Ref0}}}{I} \approx \frac{R_{\text{shunt}}(T_0)}{(1 - \delta_{\alpha I} + \delta_g) + \Big(\alpha\frac{kT_0}{q}\ln(p)\delta_p + \lambda T_0\delta_{\alpha I}\Big)\frac{1}{V_{g0}} + \frac{T_0}{T_c}\delta}. \tag{21}$$

The shunt resistor value at the averaged calibration temperature $R_{\text{shunt}}'(T_0'' = T_0)$ is then calculated

$$R_{\text{shunt}}'(T_0) = R_{\text{shunt}}'(T_0')\cdot\Big(1 + \alpha_1\cdot(T_0 - T_0')\Big) \tag{22}$$

in which, in order to simplify the analysis, only the 1^{st}-order TCR is considered.

The key to mitigating the effect of all the uncalibrated errors lies in (19) and (21). These two calibration data-points collectively absorb all the error terms and, significantly mitigate their impact during the normal operation of the CSS. This important conclusion will be clarified further in the remainder of this section.

During the normal operation, when an unknown current *I* at an unknown temperature T flows through the shunt, the two ADCs produce outputs $\mu_I'(T)$ and $\mu_T'(T)$ given by (15) and (16),

[3]For the sake of simplifying the analysis, we assume that all devices are at the same calibration temperature T_0.

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respectively. The reported current by the CSS, I', can then be written as

$$I'(T)=\frac{\mu'_I(T)\cdot V_{\mathrm{Ref0}}}{R'_{\mathrm{shunt}}(T)}=\frac{\mu'_I(T)\frac{V_{g0}}{\alpha}}{R'_{\mathrm{shunt}}(T_0)\cdot\Big(1+\alpha_1\cdot(A\mu'_T(T)-T_0)\Big)}. \tag{23}$$

The CSS gain error is

$$\epsilon(T)=\frac{I'(T)-I}{I}. \tag{24}$$

The sensitivity of this gain error to each error term over temperature can be obtained as

$$S_{\delta_i}^{\epsilon(T)}(T)=\frac{\partial\epsilon(T)}{\partial\delta_i}. \tag{25}$$

These sensitivities are plotted in Fig. 11. Considering the shunt self-heating effect, the calibration temperature is assumed to be 40°C in this plot. As shown, the error sources are significantly suppressed; for instance, the sensitivity to the capacitor mismatch is at most 0.2, meaning that the effect of this mismatch is suppressed by $> 5\times$. With a reasonable layout, the capacitor mismatch can be easily bounded to $\pm 0.3\%$ (3σ), leading to $< \pm 0.05\%$ error in the current sensing. The errors originated from the BGR are mitigated by $> 20\times$; up to $\pm 1\%$ process spread in V_{BE} and up to $\pm 1\%$ mismatch in the ratio p will cause a negligible error ($< \pm 0.05\%$) in the current sensing.

So far, for the sake of simplifying our analysis, $c(T)$ and the shunt's 2^{nd}-order TCR α_2 have been ignored. In order to evaluate their effects and to verify the validity of our analysis, we present a Monte Carlo simulation in MATLAB (10,000 runs) with the following conditions:

- V_{BE} is taken from circuit corner simulation which includes the curvature $c(T)$ (besides the spread up to $\pm 1\%$).
- The spread in the ratio p is assumed to have a Gaussian distribution with a 3σ value of 1%.
- The mismatches among various capacitors are assumed Gaussian with a 3σ value of 0.3%.
- R_{shunt} has a Gaussian distribution with a 3σ value of 15%.

After applying the proposed calibration scheme, the resulting current-sensing gain errors are plotted in Fig. 12. It is in accordance with the calculation result shown in Fig. 11 in which the

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maximum errors occur at the two temperature ends -55°C and $+125$°C. This simulation also shows a maximum 3σ error of $\sim 0.083\%$ which is very close to the calculation result ($\sim 0.089\%$).

It can be qualitatively explained that the effect of $c(T)$ propagates up to the point where α_1 and α_2 are determined. As a result, α_1 and α_2 will be slightly modified so as to account for the effect of $c(T)$. In short, the shunt's TCR absorbs $c(T)$ and suppresses its effect on the CSS accuracy [15].

VI. Measurement Results

The CSSs were realized in a standard 0.13 μm CMOS process (Fig. 13). They occupy 0.4 mm^2 (CSS_1 with lead-frame shunt) and 0.85 mm^2 (CSS_2 with on-chip shunt) and draw 13 μA from a 1.5 V supply. BGR, ADC_I and ADC_T consume 6.5 μA, 4.3 μA, and 2.2 μA, respectively. For flexibility, the digital backend and decimation filter were implemented off-chip. At a clock frequency of 100 kHz and for conversion rates up to 400 S/s, both ADCs are kT/C-noise limited. In a conversion time T_{conv} of 18 ms, ADC_I and ADC_T achieve 1.4 $\mu\mathrm{V}_{\mathrm{rms}}$ and 10 $\mathrm{mK}_{\mathrm{rms}}$ resolution, respectively.

Five samples of CSS_1 and fifteen HVQFN-packaged samples of CSS_2 were tested from -55 to $+85$°C. Before using CHL, the measured offset of both CSSs' ADC_I is less than 6 μV (Fig. 14). After using CHL, offset drops to below 110 nV (400 μA) and 40 nV (4 μA) in CSS_1 and CSS_2, respectively. The ADCs' input sampling capacitors also shows a maximum spread of up to $\pm 0.05\%$, which as explained, does not need to be explicitly corrected.

Fig. 15 depicts the nonlinearities and the spread of V_{Ref} and the temperature sensor, as well as the nonlinearity of the calibrated R_{shunt}. As described in Section IV, the spread of V_{Ref} and the temperature sensor are absorbed in the shunt calibration process, while their non-linearity, together with the shunt's TCR, are digitally compensated by a *single* 2^{nd}-order polynomial, as they are quite stable in the process used [15], [31].

Measurements show that R_{shunt} spreads up to $\pm 2.5\%$. After calibrating the lead-frame shunt (at

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+5 A and ∼25°C) and with temperature compensation, CSS_1 achieves ±0.3% gain error from −55 to +85°C, and over a ±36 A range (Fig. 16). After calibrating the on-chip shunt (at +3 A and ∼25°C) and with temperature compensation, the CSS_2 achieves a gain error of ±0.3% over a ±5 A range (Fig. 17). It should be noted that, compared to the insulating oxide, the silicon substrate is about 100× more thermally conductive. This results in an enhanced thermal design for the lead-frame shunt compared to the on-chip shunt.

The dynamic accuracy of both CSSs was evaluated with a 5 A step and at T_{conv} = 18 ms (Fig. 18). Over a 9 s of measurement time, this causes a temperature rise of ∼ 1°C and ∼ 20°C in CSS_1 and CSS_2, respectively. Unlike [15], which shows up to 0.7% additional error in transient, both CSSs maintain their accuracy throughout the current step. This demonstrates the advantage of the dual ADC design which enables continuous current and temperature sensing.

A comparison with the state-of-the-art is shown in Fig. 19. Compared to [9]–[11], CSS_1 represents a significant increase in current handling capability ($> 2\times$), accuracy ($> 2\times$) and dynamic range ($> 25\times$) despite the use of a standard (high-TCR) lead-frame shunt. These results demonstrate that by combining precision readout electronics and good thermal design, an accurate fully integrated CSS can be realized with the help of a standard lead-frame shunt. Compared to our previous work [15], CSS_2 achieves 4× lower offset and similar gain error despite using a simpler calibration scheme and 4× lower power.

VII. Conclusion

By using the lead-frame of a standard HVQFN32 plastic package as a 260 $\mu\Omega$ shunt resistor, a ±36 A integrated current-sensing system has been realized. Compared to the state-of-the-art, it significantly improves the current-sensing gain error and offset. The keys to this level of performance are 1) designing nanovolt-offset ADCs, 2) ensuring a good thermal coupling between the shunt and the temperature sensor, and 3) a simple calibration scheme which only calibrates for the shunt's

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spread and its TCR, while substantially mitigating the effect of several critical error sources of the readout electronics.

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VIII. Figure Caption

Fig. 1. Drift in on-chip R_{shunt} due to electromigration. Three samples of [15] were measured at an ambient temperature of $+85^{\circ}$C and a 5-A DC current for 24 days. (The discontinuities in the plots are due to undesired disruptions in the measurement. During such disruptions, however, the 5-A current was continuously running through the shunt.)

Fig. 2. Block diagram of the proposed shunt-based CSS.

Fig. 3. The lead-frame shunt in a standard HVQFN32 plastic package.

Fig. 4. The COMSOL simulation setup to study the thermal coupling between the lead-frame shunt and the temperature-sensing PNPs located on the surface of the silicon die.

Fig. 5. COMSOL simulation result: temperature rise at (a) the lead-frame surface, and (b) along the AA$'$ axis, at a 36A DC current.

Fig. 6. COMSOL simulation results showing the self-heating along the AA$'$ axis at a 36A DC current and under different mechanical setups.

Fig. 7. Cross section of the on-chip shunt and the temperature-sensing PNPs underneath.

Fig. 8. Simplified schematic of the BGR consisting of a bias circuit and a bipolar core.

Fig. 9. Simplified schematic of the current-sensing ADC (ADC_I).

Fig. 10. Simplified schematic of the temperature-sensing ADC (ADC_T).

Fig. 11. The sensitivity of the current-sensing gain error to various error terms.

Fig. 12. The simulated current-sensing gain error over temperature (the bold lines indicate the $\pm 3\sigma$ values).

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Fig. 13. Chip micrograph and HVQFN package.

Fig. 14. ADC_I's offset over temperature, (top) before and, (bottom) after using CHL.

Fig. 15. Error in (top) V_{Ref} and, (middle) the temperature sensor. Nonlinearity in the shunt resistor (bottom).

Fig. 16. CSS_1 (with lead-frame shunt) gain error at three ambient temperatures.

Fig. 17. CSS_2 (with on-chip shunt) gain error at three ambient temperatures.

Fig. 18. Transient temperature and gain error measurement for a 5 A current step driven through the shunt at room temperature, (top) CSS_1, and (bottom) CSS_2.

Fig. 19. Comparison with the state-of-the-art.

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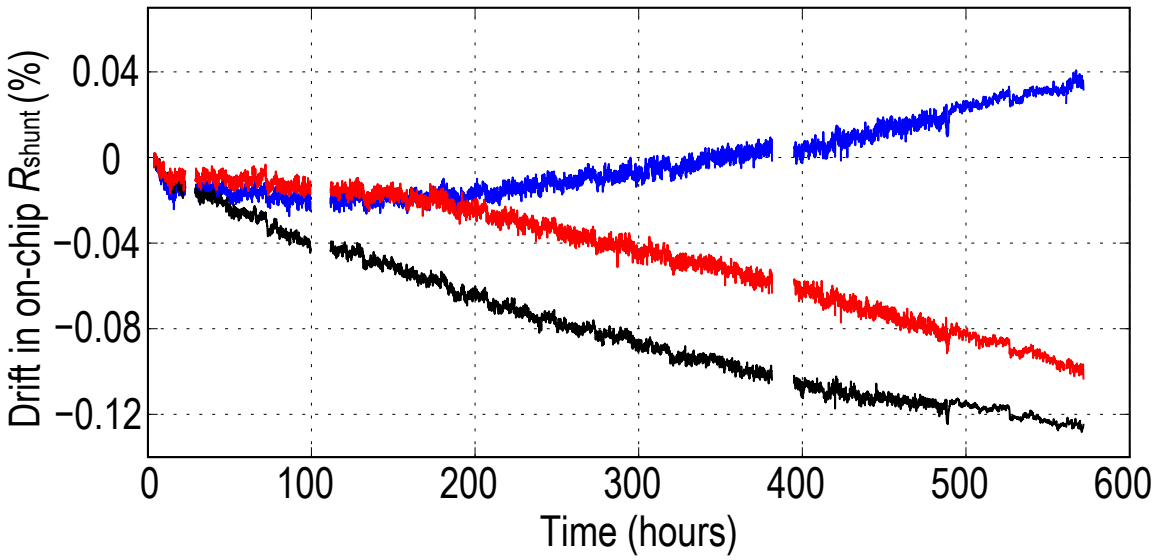

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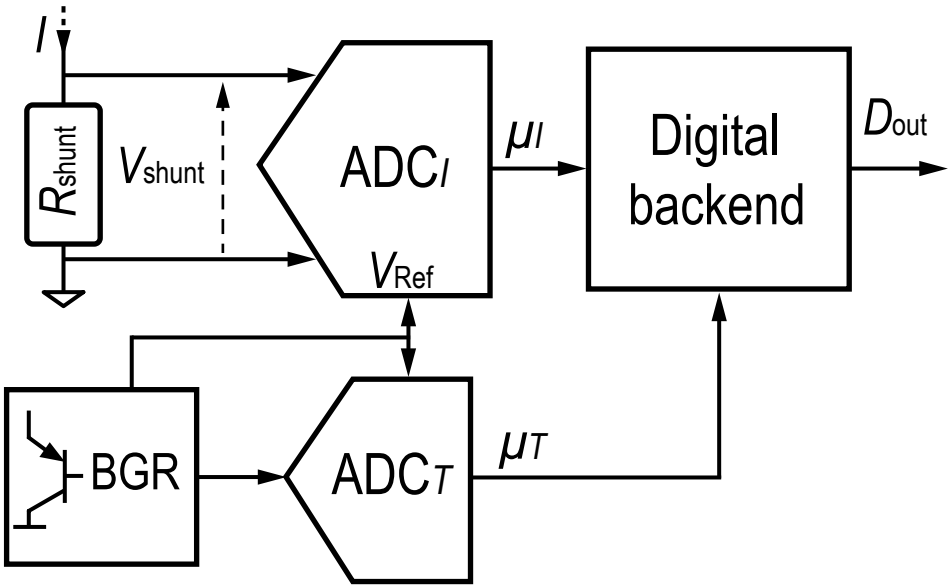

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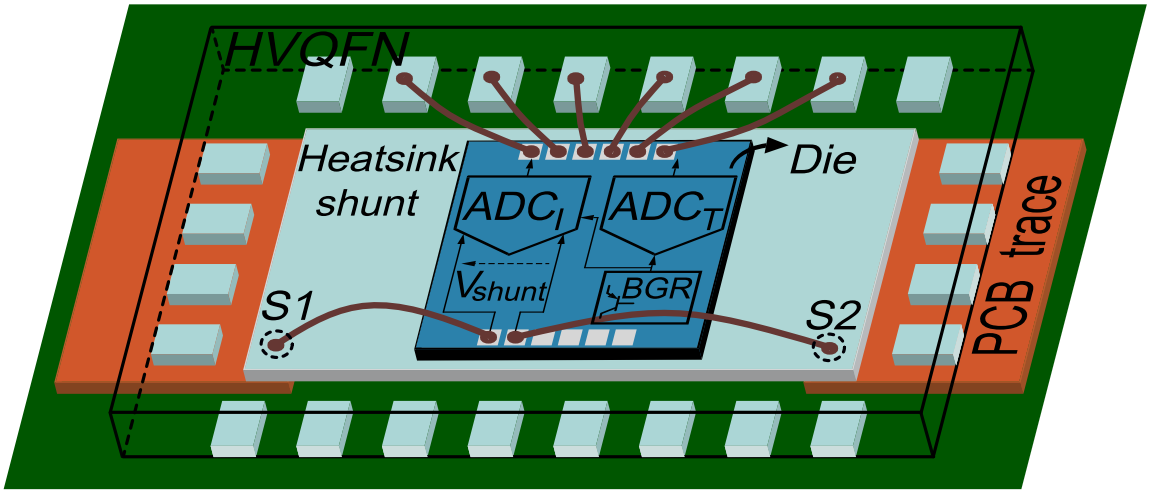

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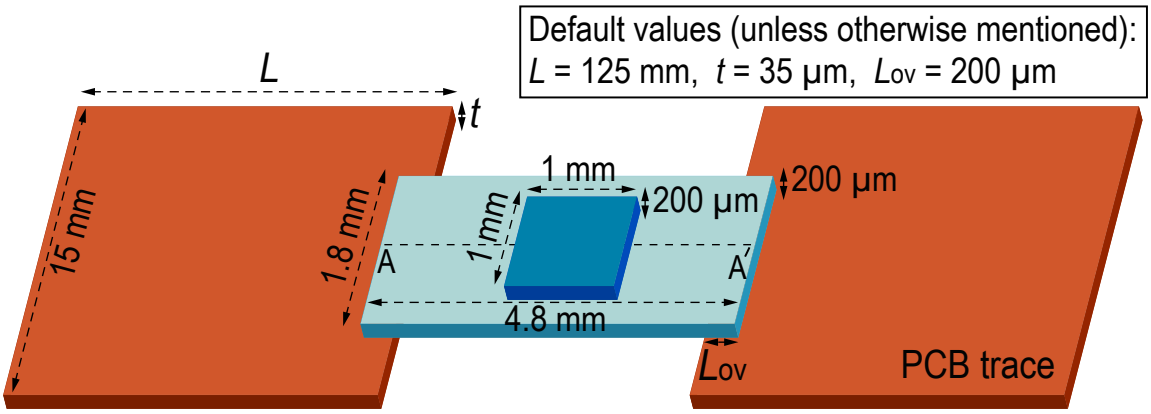

Fig. 4. The COMSOL simulation setup to study the thermal coupling between the lead-frame shunt and the temperature-sensing PNPs located on the surface of the silicon die.

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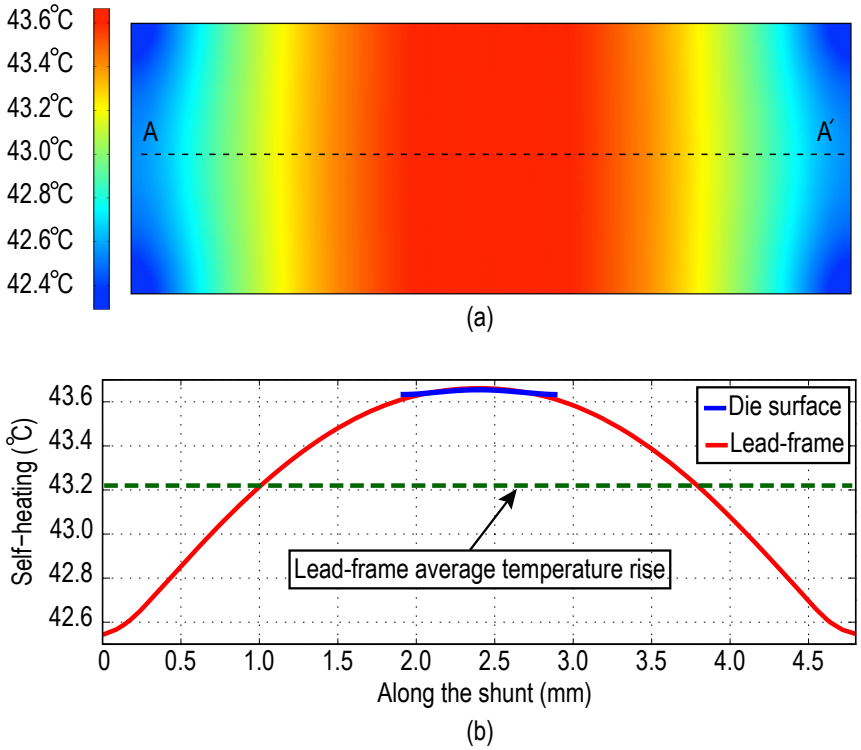

Fig. 5. COMSOL simulation result: temperature rise at (a) the lead-frame surface, and (b) along the AA′ axis, at a 36A DC current.

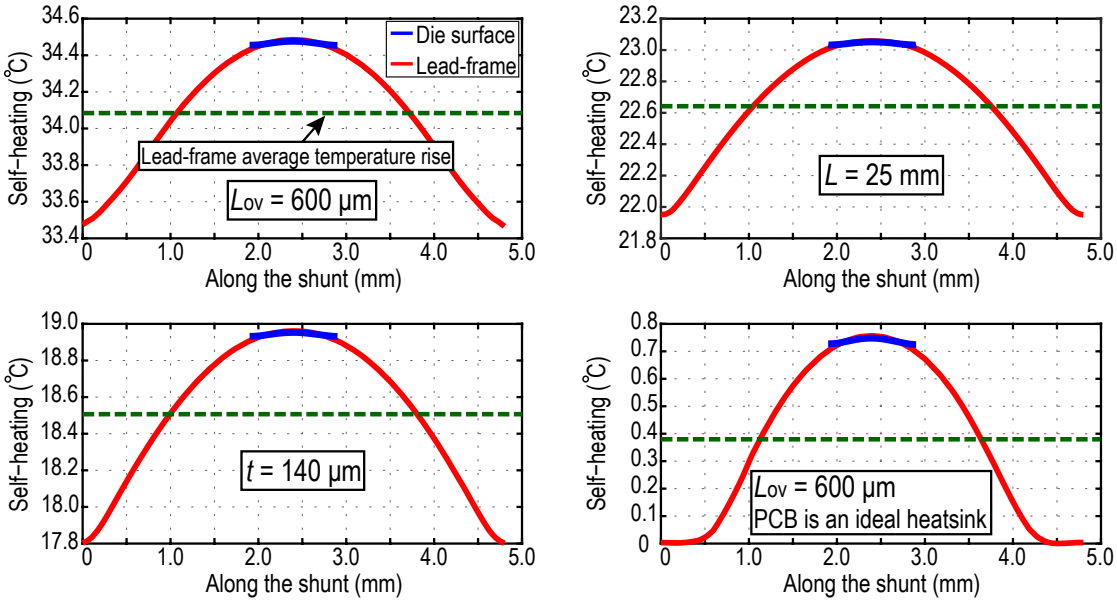

Fig. 6. COMSOL simulation results showing the self-heating along the AA′ axis at a 36A DC current and under different mechanical setups.

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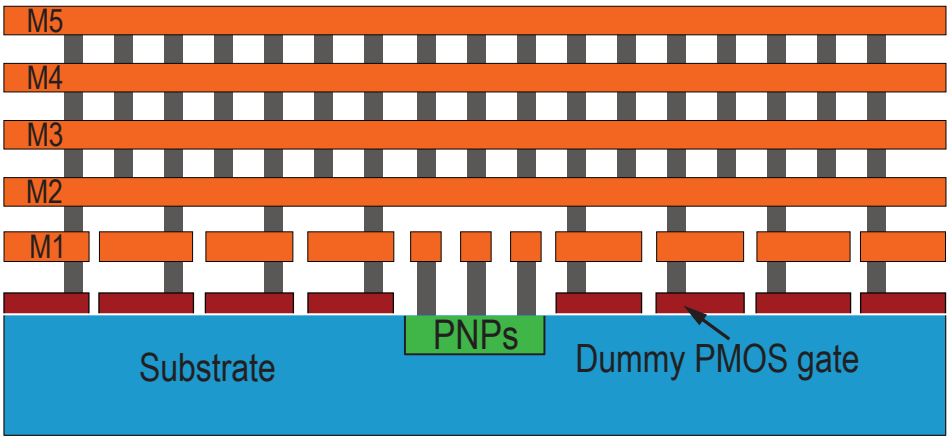
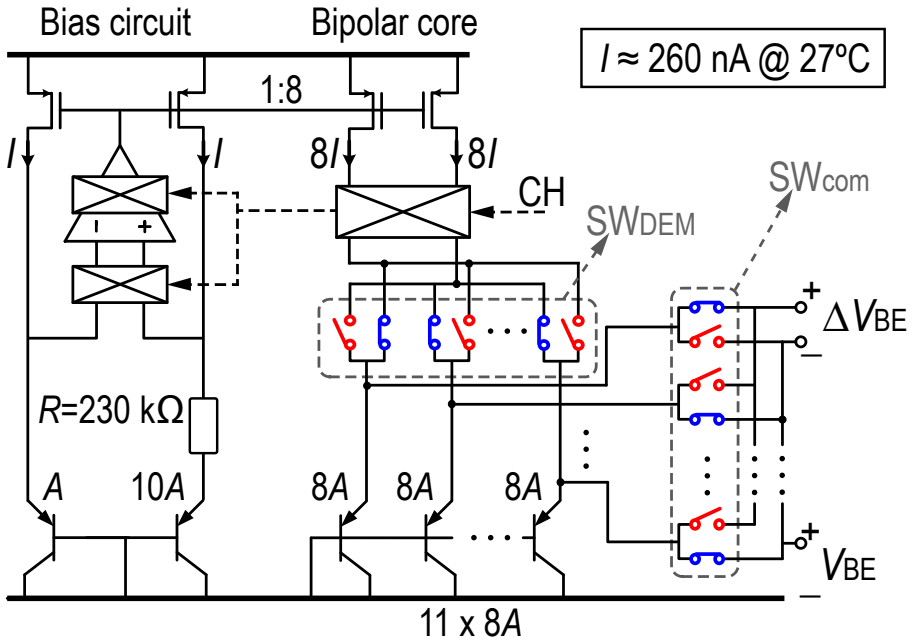


Fig. 7. Cross section of the on-chip shunt and the temperature-sensing PNPs underneath.



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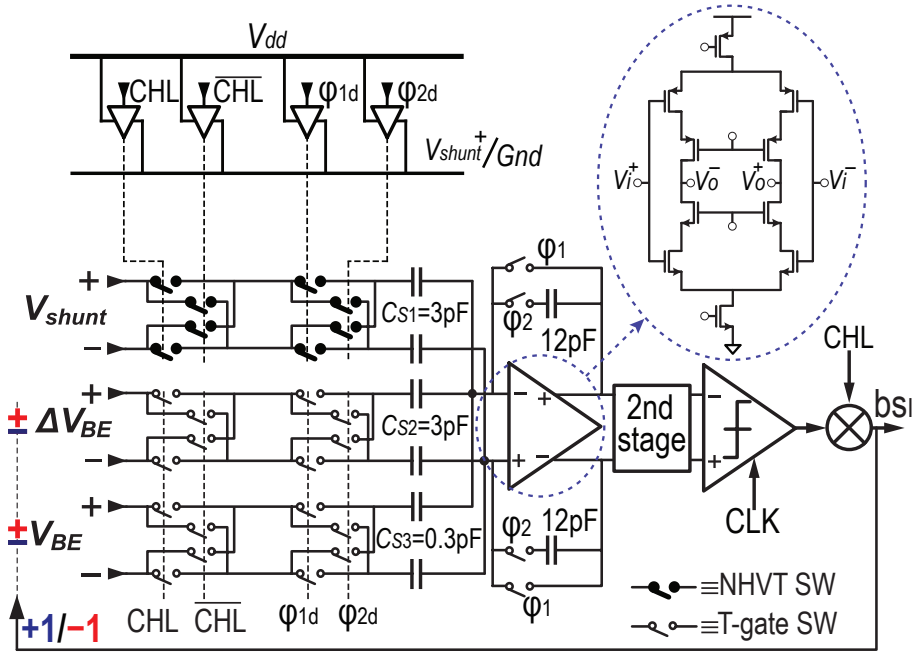

Fig. 9. Simplified schematic of the current-sensing ADC (ADC_I).

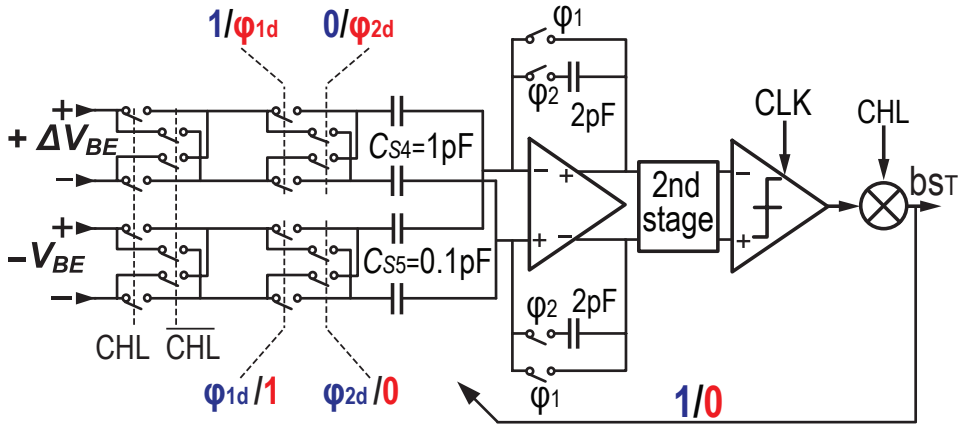

Fig. 10. Simplified schematic of the temperature-sensing ADC (ADC_T).

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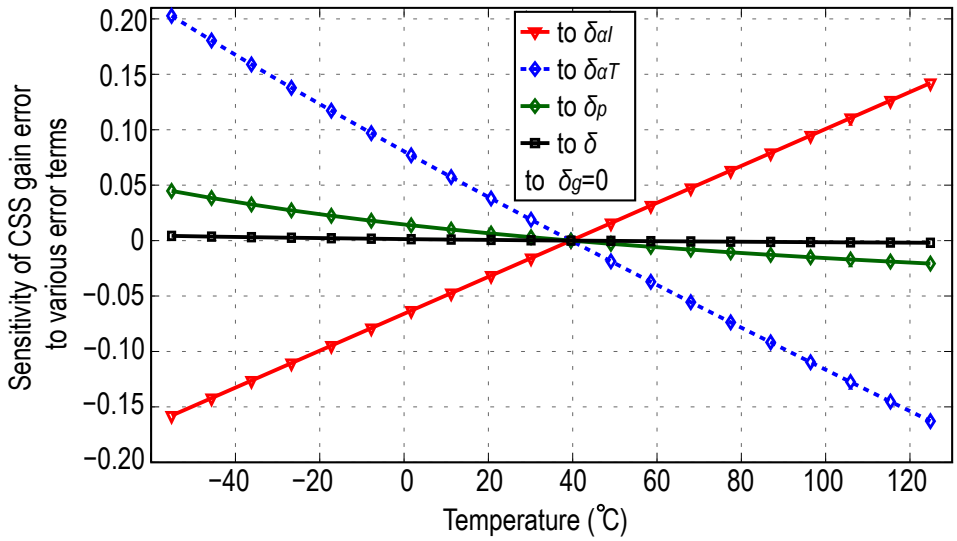

Fig. 11. The sensitivity of the current-sensing gain error to various error terms.

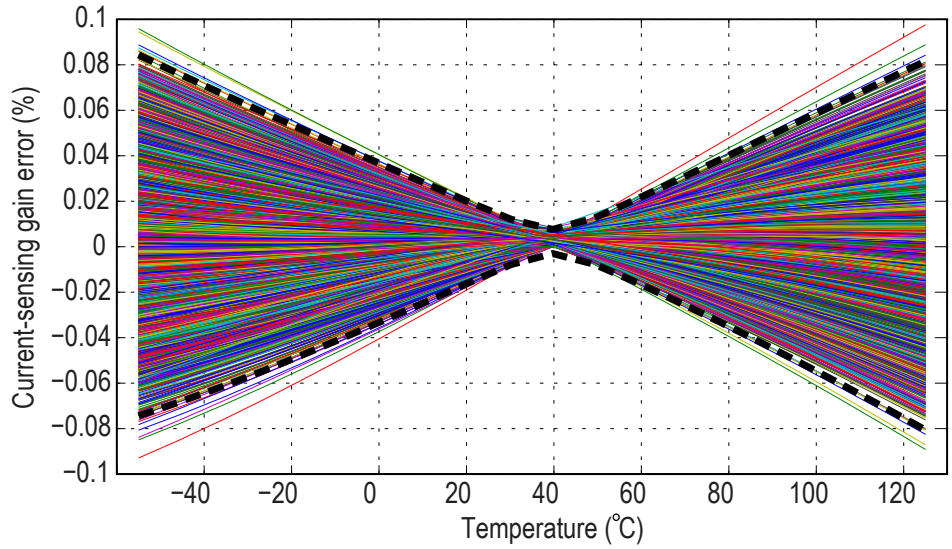

Fig. 12. The simulated current-sensing gain error over temperature (the bold lines indicate the $\pm 3\sigma$ values).

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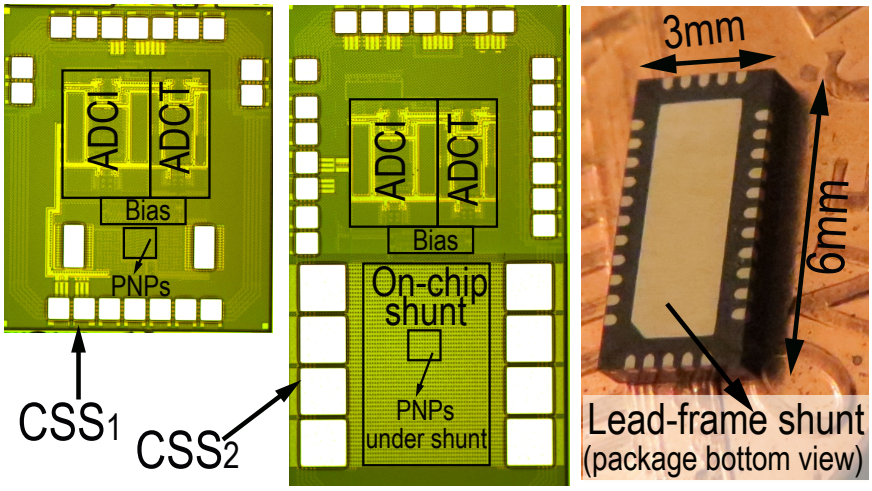

Fig. 13. Chip micrograph and HVQFN package.

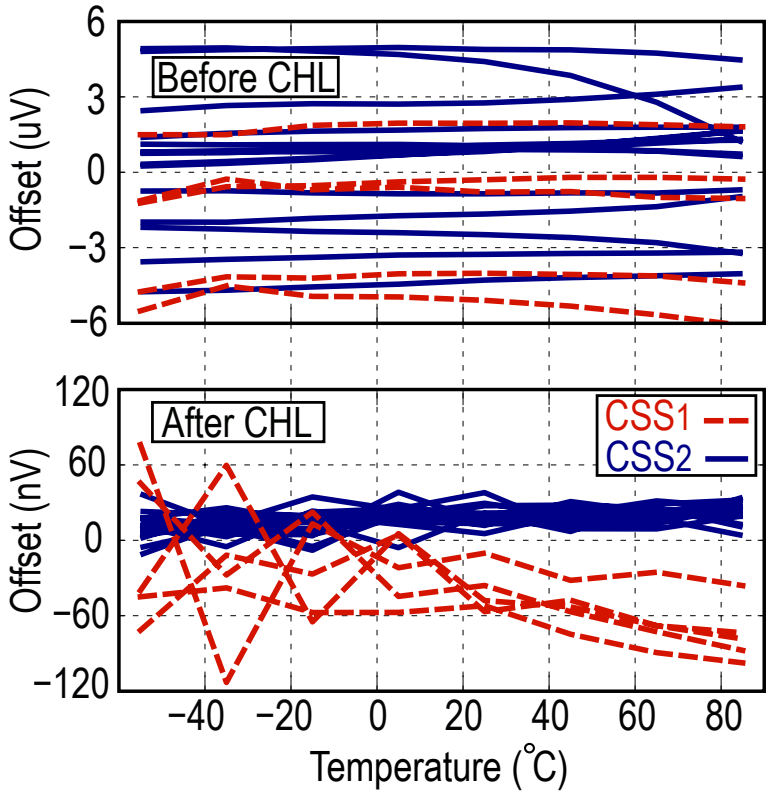

Fig. 14. ADC_I's offset over temperature, (top) before and, (bottom) after using CHL.

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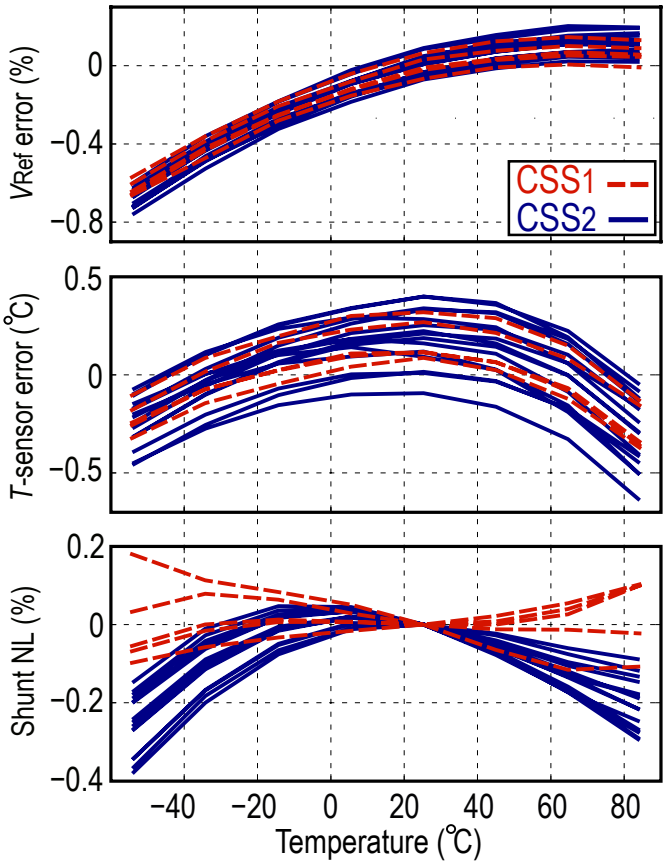

Fig. 15. Error in (top) V_{Ref} and, (middle) the temperature sensor. Nonlinearity in the shunt resistor (bottom).

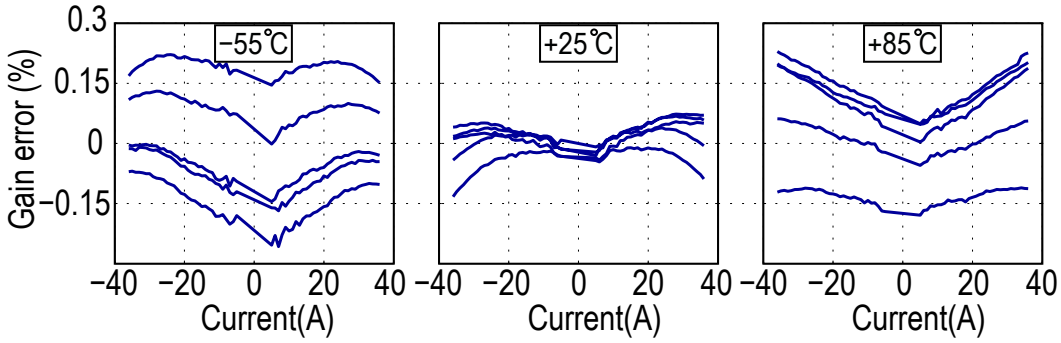

Fig. 16. CSS_1 (with lead-frame shunt) gain error at three ambient temperatures.

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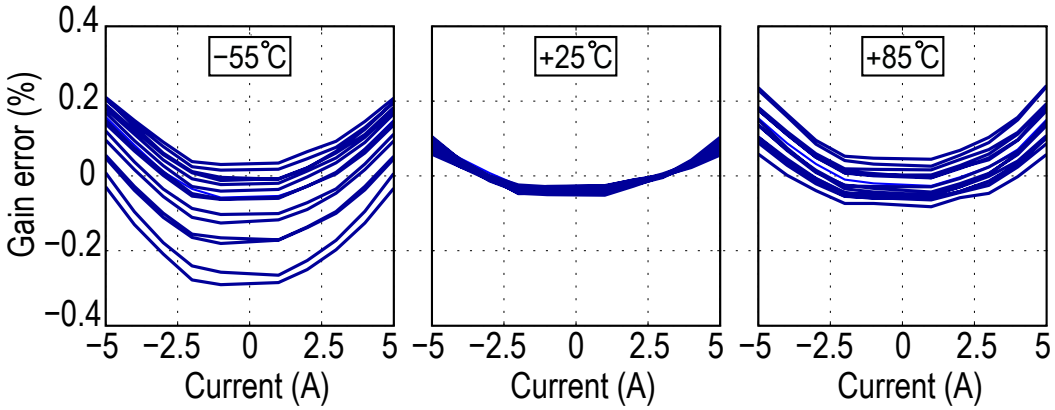

Fig. 17. CSS_2 (with on-chip shunt) gain error at three ambient temperatures.

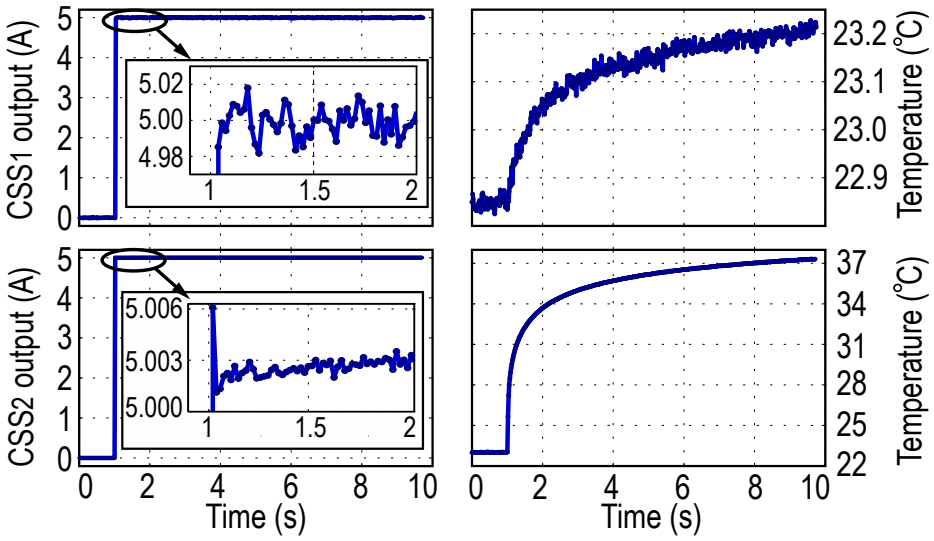

Fig. 18. Transient temperature and gain error measurement for a 5 A current step driven through the shunt at room temperature, (top) CSS_1, and (bottom) CSS_2.

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	Shunt (mΩ)	I-range	Gain error	Offset	Resolution	BW / $T_{conv.}$	Power cons.	Temp. range
CSS1	**0.26**	**±36A**	**0.3%**	**400µA**	**5.4mA**	**10ms**	**20µW**	**-55..85°C**
[3]	1.3	±15A	>3%	--	--	40MHz***	18.5mW	-40..85°C
[4]	2	±10A	0.75% *	50mA	7mA	50kHz***	1.5mW	-40..125°C
[5]	4	±7A	3%	11mA	20mA	50ms	140µW	-40..125°C
CSS2	**10**	**±5A**	**0.3%**	**4µA**	**200µA**	**10ms**	**20µW**	**-55..85°C**
[6]	10	±5A	0.35% **	16µA	150µA	25ms	83µW	-55..85°C

* Uses a custom low-TCR shunt

** Uses extra calibration

*** Analog output

Fig. 19. Comparison with the state-of-the-art.

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