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DOI
10.1109/JEDS.2024.3432283

Publication date
2024

Document Version
Final published version

Published in
IEEE Journal of the Electron Devices Society

Received 27 May 2024; revised 4 July 2024; accepted 18 July 2024. Date of publication 22 July 2024; date of current version 8 August 2024.
The review of this article was arranged by Editor P.-W. Li.

Digital Object Identifier 10.1109/JEDS.2024.3432283

Cryogenic Characterization of Low-Frequency Noise in 40-nm CMOS

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This work was supported in part by Intel Corporation, and in part by NXP Semiconductors.
This article has supplementary downloadable material available at https://doi.org/10.1109/JEDS.2024.3432283, provided by the authors.

ABSTRACT This paper presents an extensive characterization of the low-frequency noise (LFN) at room temperature (RT) and cryogenic temperature (4.2 K) of 40-nm bulk-CMOS transistors. The noise is measured over a wide range of bias conditions and geometries to generate a comprehensive overview of LFN in this technology. While the RT results are in-line with the literature and the foundry models, the cryogenic behavior diverges in many aspects. These deviations include changes with respect to RT in magnitude and bias dependence that are conditional on transistor type and geometry, and even an additional systematic Lorentzian feature that is common among individual devices. Furthermore, we find the scaling of the average LFN with the area and its variability to be similar between RT and 4.2 K, with the cryogenic scaling reported systematically for the first time. The findings suggest that, as no consistent decrease of LFN at lower temperatures is observed while the white noise is reduced, the impact of LFN for precision analog design at cryogenic temperatures gains a more predominant role.

INDEX TERMS Low frequency noise, 1/f noise, flicker noise, cryogenic electronics, Cryo-CMOS, quantum computing.

I. INTRODUCTION

Cryogenic electronics is a rapidly expanding field driven by applications such as quantum computing and space exploration [1], [2]. Significant challenges arise in designing CMOS electronics for cryogenic temperatures due to the incomplete understanding of cryogenic transistor behavior, thus causing over-design or even design failures. To address the situation, extensive characterization and modeling of DC and RF behavior have been performed, e.g., in [3], [4].

Within the cryogenic behavior, noise is generally less explored, but works on both broad-band noise and low-frequency noise have been reported. In broad-band noise characterization, the noise is scaling less than expected from a purely thermal origin, thus suggesting that shot noise dominates at cryogenic temperatures [5]. For designing systems at cryogenic temperature, LFN also plays a crucial role, e.g., for the phase noise of phase-locked loops (PLL) [6] and the input-referred noise of transimpedance amplifiers (TIA) [7]. Early work on cryogenic LFN provided evidence pointing to both carrier number and mobility fluctuations as possible origins of the noise at low temperatures [8], [9]. In [10], measurements of a modern SOI process over a range of bias points are shown to be compatible with the model including carrier number fluctuations and correlated mobility fluctuations [11]. In [12], the lack of the expected decrease of LFN at cryogenic temperatures is attributed to band-tail states acting as traps. This is corroborated by the same band-tail states possibly causing the saturation of the MOSFET sub-threshold slope at cryogenic temperatures [13], [14]. In [15], characterization and modeling of large-area devices manufactured on different crystal orientations suggest carrier number fluctuation caused by interface traps as an alternative explanation for cryogenic LFN. While these characterizations, typically only of one or few devices, have added significantly to the understanding of LFN at cryogenic temperature, they can only partially inform design decisions.

Missing in current literature is a more extensive characterization that can both guide the circuit designers with accurate predictions and help understand the physical origin of LFN. Furthermore, despite several studies focusing on the variability of DC parameters, e.g., [16] or [17] (for the same CMOS technology addressed in this work), no LFN variability analysis at cryogenic temperatures has been yet reported. To fill this gap, we measure several different geometries and characterize them over a wide range of bias voltages, as commonly required for design space explorations. Multiple individual devices with the same geometry are measured at the same bias, since statistical characterization is crucial for accurate analysis due to the large variations between individual devices, even for large-area devices [18], which are already present at RT and hence expected also at cryogenic temperatures. Such an extensive characterization enables us to also perform a systematic analysis of the scaling of LFN and its variability with device area, for the first time at cryogenic temperature. Since noise exhibits a significant spread over different devices, it has been crucial to extend our study to a significant number of samples over varying geometries to obtain a comprehensive and complete analysis.

Furthermore, the analysis of multiple equal devices enabled the discrimination of a Lorentzian feature that is unexpectedly systematic among different devices. Previous research, as seen in [5] and [19], has noted a dominant Lorentzian signature at cryogenic temperatures. However, due to the lack of a detailed and focused investigation into this signature, it has not been reported as a systematic result. For the first time, we demonstrate that this feature is dependent on device geometry, bias, and temperature, leading to increased device noise that proves detrimental to cryogenic circuits. Thus, these extensive new data both improve the understanding of low-frequency noise and enable circuit designers to get better noise estimations.

This article is organized as follows. We begin by introducing the experimental methods in Section II, then present the measurement results and analyze them in Section III, discuss the results in the light of their impact on precision analog design in Section IV and draw the conclusions in Section V.

II. METHODS

The measurement setup was designed to facilitate the characterization of many devices at cryogenic temperature, as necessary to generate the statistics for LFN. For this, a chip was fabricated in 40 nm LP CMOS bulk technology which carried 8 individual transistors for each of the several geometries, for a total of 400 heavily multiplexed devices under test (DUT) per chip. In the chip, the devices' source and drain (V_d, V_s) are connected in parallel. Multiplexing between them is implemented, similar to [20], by connecting a single device gate at a time to the gate bias (V_g), see Fig. 1 for the NMOS and PMOS schematic. For reliable rail-to-rail

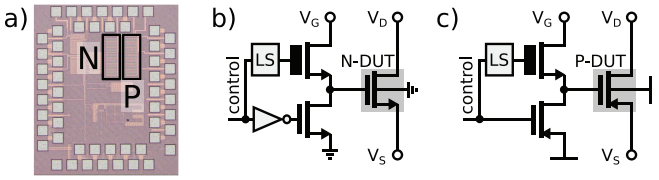

FIGURE 1. a) Micrograph of the test chip; b) Schematic of each NMOS; c) Schematic of each PMOS. The thick-oxide selection transistors are shown with a thicker-gate symbol.

operation, multiplexing of V_g is implemented with thick-oxide transistors, supplied by 2.5 V. All deselected transistors are biased with V_{gs}=0, and the source is kept at ground/V_{dd} for all NMOS/PMOS measurements. Unless otherwise noted, all measured transistors are of low-threshold-voltage (LVT) flavor.

Assembled in a DIP package, the chip is mounted on a PCB placed in a dipstick setup and submerged in liquid helium with a temperature sensor mounted close to the sample. Such a liquid cooling at 4.2 K results in a stable and accurate definition of the ambient temperature, unlike prior characterization in the vacuum environment of the typical cryogenic probe stations, which may suffer from thermalization issues. For the RT measurements, the ambient temperature was controlled to within ±2.5 K around 295 K. This setup allows for up to 5 days of continuous measurement at cryogenic temperatures using a single 100 L helium dewar, without labor-intensive thermal cycles. The sample was kept mounted in the same dipstick for both RT and cryogenic measurements. Measurements are performed via a resistive bias-T followed by a transimpedance amplifier (TIA) and digitized by an acquisition card. The resulting data is accurate over the frequency range from 1 Hz (or 5 Hz, depending on settings of the bias-T) up to 50 kHz, limited by the TIA bandwidth. The reported sweeps over V_{gs} were performed in two bias configurations: one in the linear region with fixed V_{ds}=50 mV and one in an effective "diode" connection with V_{ds}=V_{gs}. The analyzed data is filtered with a rolling median filter for better visibility. Further details about the measurement setup and the data processing can be found in the supplementary material.

All data and analysis code used for the figures in this paper is available in [21].

III. CHARACTERIZATION RESULTS

An example DC characterization of an N/PMOS with W×L=1 µm×1 µm is shown in Fig. 2. The characterization shows the typical changes in behavior when moving to cryogenic temperature: the increased threshold voltage (V_{th}) and the increased transconductance (g_m) as well as the reduced output resistance (r_o) in strong inversion [22].

Example noise spectra of eight 1 µm×1 µm devices at a single bias point V_{gs}=V_{ds}=1.1 V for both N/PMOS are shown in Fig. 3. The plots also include a conservative noise-floor estimation based on the measured noise floor of the

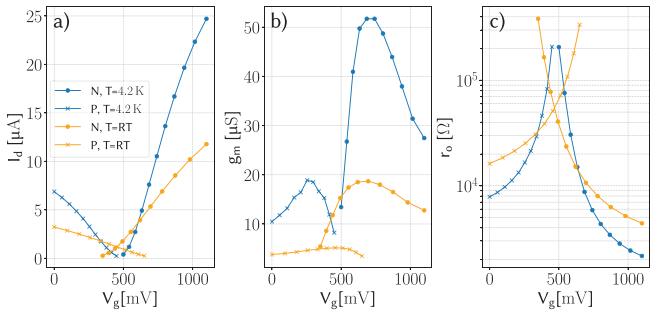

FIGURE 2. Example N/PMOS (1μm×1μm) DC-characteristics at V_{ds}=50mV: a) drain current I_d, b) transconductance g_m, c) output resistance r_o.

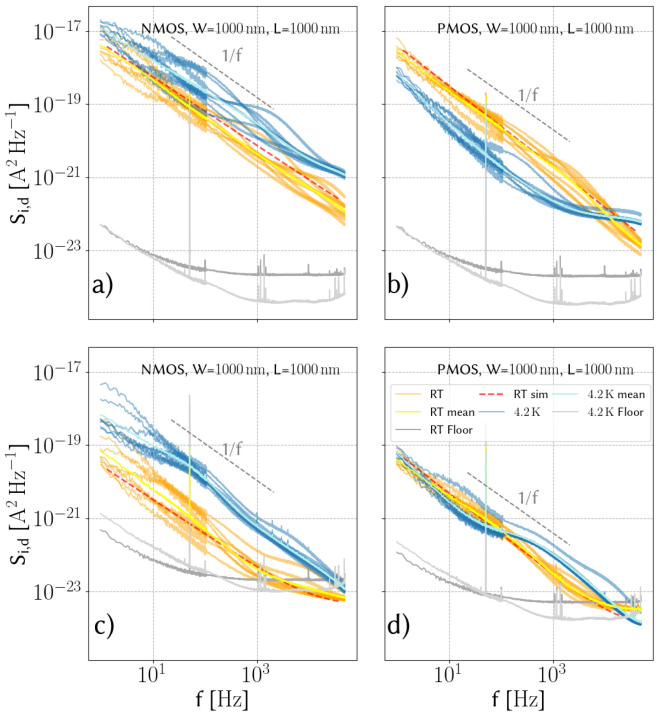

FIGURE 3. Noise spectra for NMOS (a, c) and PMOS (b, d) with W×L =1μm×1μm at V_{gs}=1.1V and V_{ds}=1.1 V (a,b) and V_{ds}=50 mV (c,d), respectively. 8 devices at the same bias points are shown.

test equipment scaled by the expected additional noise due to the transistor r_o, further discussed in the supplementary. Alongside the individual spectra, a logarithmic mean curve is shown, around which individual devices differ significantly at RT, as also reported in [18], due to the random distribution of single traps. This effect is here, for the first time, shown to persist also at cryogenic temperatures. The RT mean shows typical 1/f behavior and matches the foundry device model well. The cryogenic results differ, with the NMOS devices showing increased output-referred noise and the PMOS devices showing reduced noise. While the variability at lower frequencies is qualitatively similar to the RT results, a systematic deviation from the 1/f shape appears in the spectra at higher frequencies.

To substantiate this, we plot in Fig. 4 the mean spectra for W×L=1 µm×1 µm and W×L=1 µm×40 nm NMOS and PMOS devices for 11 logarithmically spaced overdrive-voltage biases (V_{od}=V_{gs}-V_{th}), which are color-coded in the plot. We concentrate on the mean and do not show the individual devices for better visibility of the effect. The device geometries were chosen to provide examples of typical devices preferred in analog (high intrinsic gain, long channels) and RF (high speed, short channels) circuits. For the RT results, we see again that the mean noise approximates a 1/f slope and matches well the foundry device model over a wide range of bias conditions. The 1/f slope is also visible in the cryogenic results, but a systematic Lorentzian feature appears in the mean curves at higher frequencies. Signatures of this feature are visible in all the devices (NMOS and PMOS, long and short channels) with the effect appearing at lower frequency in longer devices. As this effect appears in all the individual devices, it does not average out to a 1/f behavior as otherwise common for random traps. To understand its possible origin, we analyze this Lorentzian in more detail in the following subsection.

A. SYSTEMATIC LORENTZIAN

The systematic Lorentzian feature common to multiple devices and mentioned above has not been reported in prior works. In [23],the linear kink effect, induced by tunneling from the valence band to the conduction band, is proposed as a mechanism causing a dominant Lorentzian peak at cryogenic temperatures in bulk MOS devices. Conversely, this effect manifests as a secondary peak in the g_m figure, which is not observable in our case. Another potential mechanism for causing a dominant signature is the energy sub-band scattering at low temperatures and low drain voltages [24]. However, due to the high voltages and the absence of the proposed g_m effect, we can also rule out this mechanism. In [5], a dominant Lorentzian signature that shows a clear temperature dependence is observed at relatively high drain biases at cryogenic temperatures. In [19], two traps are identified as slow and fast. They lead to a single Lorentzian signature in low-frequency noise measurement, similar to our results. Still, noise characterization of a single device is presented in these papers, and effects are not investigated extensively and compared with different devices.

To ensure that it is not an artifact of the measurements, we performed additional verifications. As the equipment and the cabling adopted in the cryogenic setup are identical to the RT setup, for which the Lorentzian does not appear, we specifically investigate the components cooled to cryogenic temperature, including the chip itself and the associated passive components (resistors, capacitors) on the measurement board. Leakage currents from the deselected transistors are excluded by recording spectra with all transistors deselected and sweeping the drain bias. The on-chip multiplexing was tested by reducing the thick-oxide switch supply by 500 mV without measurable effects on either the DUT's DC behavior or its noise spectrum. The on-board tantalum capacitors have

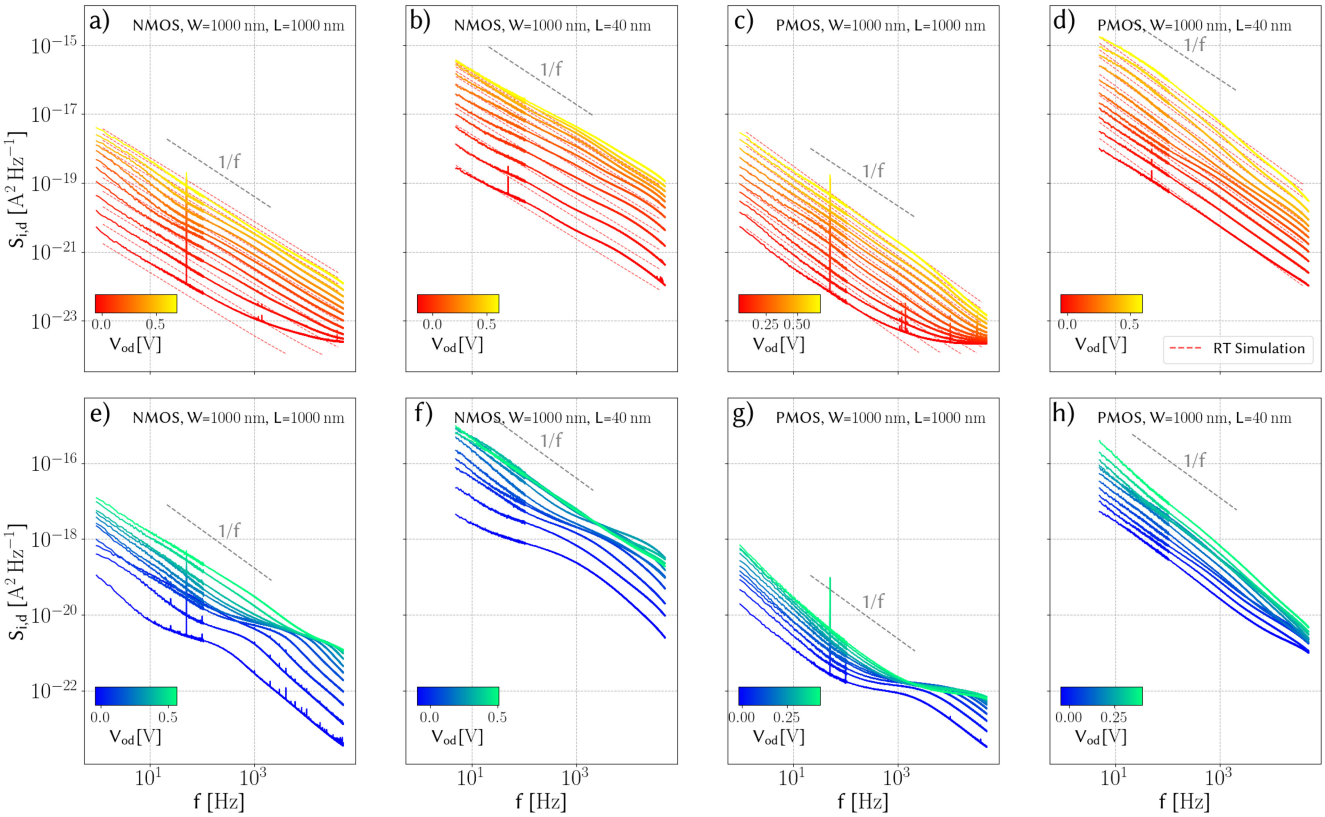

FIGURE 4. Mean noise spectra for PMOS and NMOS devices with W×L=1mm×1mm and W×L=1 mm×40nm with V_{gs}=V_{ds} for logarithmically spaced overdrive-voltage (V_{od}=V_{gs}-V_{th}) at RT (a-d) and 4.2K (e-h). Each curve represents the mean of 8 individual devices. The RT plots also show the corresponding simulations of the foundry model with dashed lines.

been excluded by measuring the DUT on a board without populating those, resulting in increased interference but the same effect visible. For testing the thin-film resistors, we replaced the chip with resistors and ran noise acquisitions under various bias conditions, without observing measurable LFN contributed by the resistors. The additional verifications are discussed in more detail in the supplementary.

To gain a deeper understanding of the Lorentzian effect, we characterized large-area (4 µm×4 µm) NMOS and PMOS devices (Fig. 5), since they show a relatively low mismatch and the Lorentzian feature appears more distinctly compared to small devices, as visible in Fig. 4. Fig. 5 shows that the Lorentzian's corner moves to higher frequencies for higher overdrive while V_{ds}=V_{gs}. As we observe negligible individual differences in these large devices concerning the Lorentzian, we performed, in the following, a more detailed series of measurements on a single device, which is shown in Fig. 6.

Fig. 6 a) shows a fine sweep of V_{od} of a single device in diode connection, from which the corner frequency $f_{C,Lorentzian}$ as function of the overdrive voltage has been extracted and plotted in Fig. 6 b). The strong dependence of the corner frequency with the bias can be attributed to barrier lowering or barrier thinning effects [25], [26].

To further investigate the nature of the effect, the temperature dependence of the trap at a given voltage bias has been measured by varying the position of the DUT mounted in the dipstick with respect to the liquid-helium surface. It is important to note that, while the temperature sensor was glued as close as possible to the sample on the ceramic package for this sweep, the accuracy in the thermalization of the DUT cannot be precisely quantified for the adopted setup above 4.2 K. When sweeping the temperature from 4.2 K to 25 K, the Lorentzian moves to higher frequencies in diode connection, see Fig. 6c). Above 12 K, the corner frequency exceeds the upper bandwidth limit of the setup.

Assuming the presence of a trap, the trap time-constant $\tau_{C,Lorentzian} = 1/(2\pi f_{C,Lorentzian})$ is extracted and plotted in Fig. 6 d) versus the inverse of the thermal energy. The saturation of the time constant at low temperatures suggests the existence of a temperature-independent contribution similar to that observed and explained in [27], [28]. As in Fig. 6 b), a decrease in the time-constant can be observed with increasing overdrive voltage. For thermally activated contribution, [29] suggests a temperature dependence of the trap time-constant according to:

$$\tau_{thermal} = \tau_0 e^{\frac{E_b}{k_b T}} \tag{1}$$

where $\tau_0 = \frac{1}{\sigma_0 v n}$ is depending on the cross-section pre-factor σ_0, the carrier velocity v and channel carrier concentration n, E_b is the energy barrier and k_b the Boltzmann constant. Assuming a temperature-independent contribution, with time

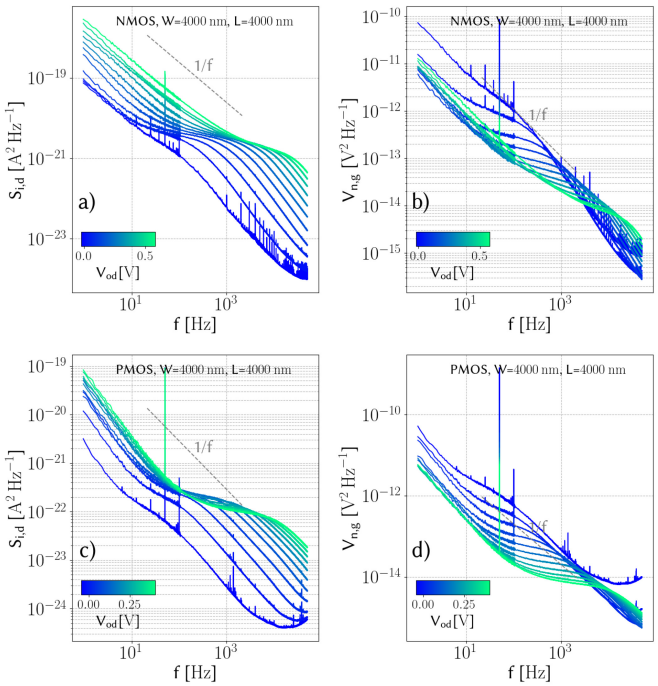

FIGURE 5. **Mean noise spectra at 4.2K. The output (a, c) and input-referred (b, d) of eight N/PMOS devices with WxL=4 mmx4mm are shown, to demonstrate the bias dependence of the systematic Lorentzian.**

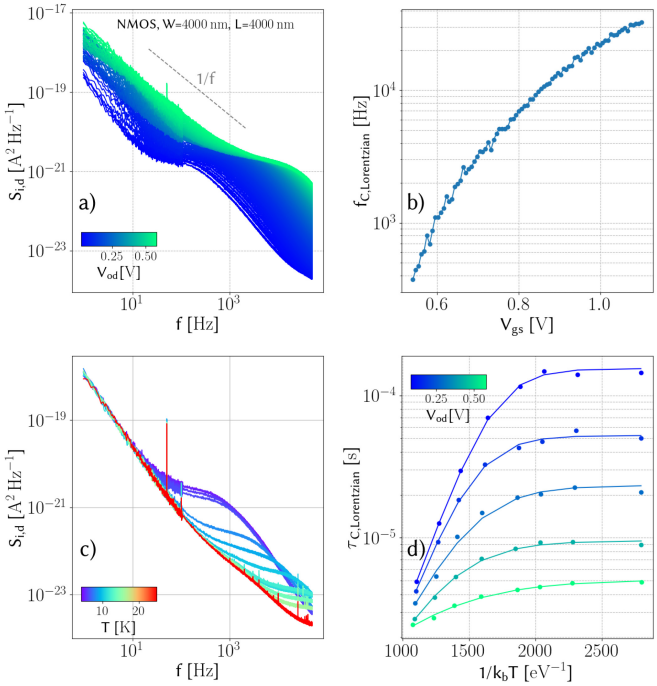

FIGURE 6. **Detailed measurements on a W×L=4mm×4mm NMOS device: a) fine bias sweep at 4.2K, b) extracted corner frequency of the Lorentzian at 4.2K, c) temperature sweep for $V_{od} = V_{gs} - V_{th}$ =80mV, d) extracted time constant of the Lorentzian.**

constant τ_{tun}, the combined effect can be described as in [25], [30]:

$$\frac{1}{\tau_{C,Lorentzian}} = \frac{1}{\tau_{thermal}} + \frac{1}{\tau_{tun}} \tag{2}$$

Fitting Eq. (2) to the measured data in Fig. 6 d) we can determine the corresponding energy barrier E_b. The extracted E_b shifts from 5.9 meV to 2.3 meV for a V_{gs} bias from 600 mV to 1100 mV. By assuming a linear field dependence of E_b as in [25], [26], E_b can be extrapolated to lie on the order of 10 meV when all terminals are at 0 V.

A possible physical cause for this phenomenon could be found in the density of states (DoS) showing an additional distinct Gaussian peak below the conduction band at a doping-dependent activation energy [31]. These extra states in the DoS enhance the probability of state occupation at the respective energy levels, thus elevating the transition rate for that energy level and creating a dominant effect. A doping density in the order of $10^{18}\,cm^{-3}$ to $10^{19}\,cm^{-3}$, which is typical doping for the lightly doped drain regions of a 40 nm bulk CMOS technology, would lead to barrier energy in the order of 10 meV [31]. This hypothesis is compatible with the observed behavior, including the commonality among different devices, the extracted barrier potential, and the increased magnitude of the effect in saturation compared to the triode (as shown by comparing Fig. 3a,b and Fig. 3c,d).

However, to gain a more comprehensive understanding of this phenomenon, further research is required, for instance by testing devices with several different precisely known doping levels and by characterizing other bulk technologies under well-controlled thermal conditions, e.g., by employing liquid helium cooling, and over significant device statistics.

B. BIAS DEPENDENCE

At low frequencies, the noise behavior is largely unaffected by the systematic Lorenzian feature and lends itself to a more traditional analysis. To this end, we sample the data in Fig. 4 at 10 Hz and plot the current noise versus the bias drain current (Fig. 7 a-d)) and the input-referred noise over V_{od} ((Fig. 7 e-h) in Fig. 7. The flicker noise is the dominant noise type in this frequency both at room temperature and 4.2 K. As expected, we observe a significant variation in the noise of the individual devices around the mean and a drop in the input-referred noise voltage with larger device size, which are analyzed in details in the next subsection. The output current noise scales with current, with proportionalities ranging from I_d to I_d^2. Generally, the NMOS results are found to scale roughly $\propto I_d$, while the PMOS results are better described with $\propto I_d^2$. The input-referred data in Fig. 7 can be qualitatively well-described by

$$S_{v,g} = \left(1 + \Omega \frac{I_d}{g_m}\right)^2 S_{fb} \tag{3}$$

with S_{fb} the flat-band voltage spectral density and Ω the coefficient of the correlated mobility fluctuation [11]. We fit Eq. (3) to the input-referred noise in Fig. 7e)-f) and report the extracted coefficients in Fig. 1.

Using the extracted S_{fb} values for the devices with W/L = 1 µm/1 µm, the trap concentrations for NMOS and PMOS

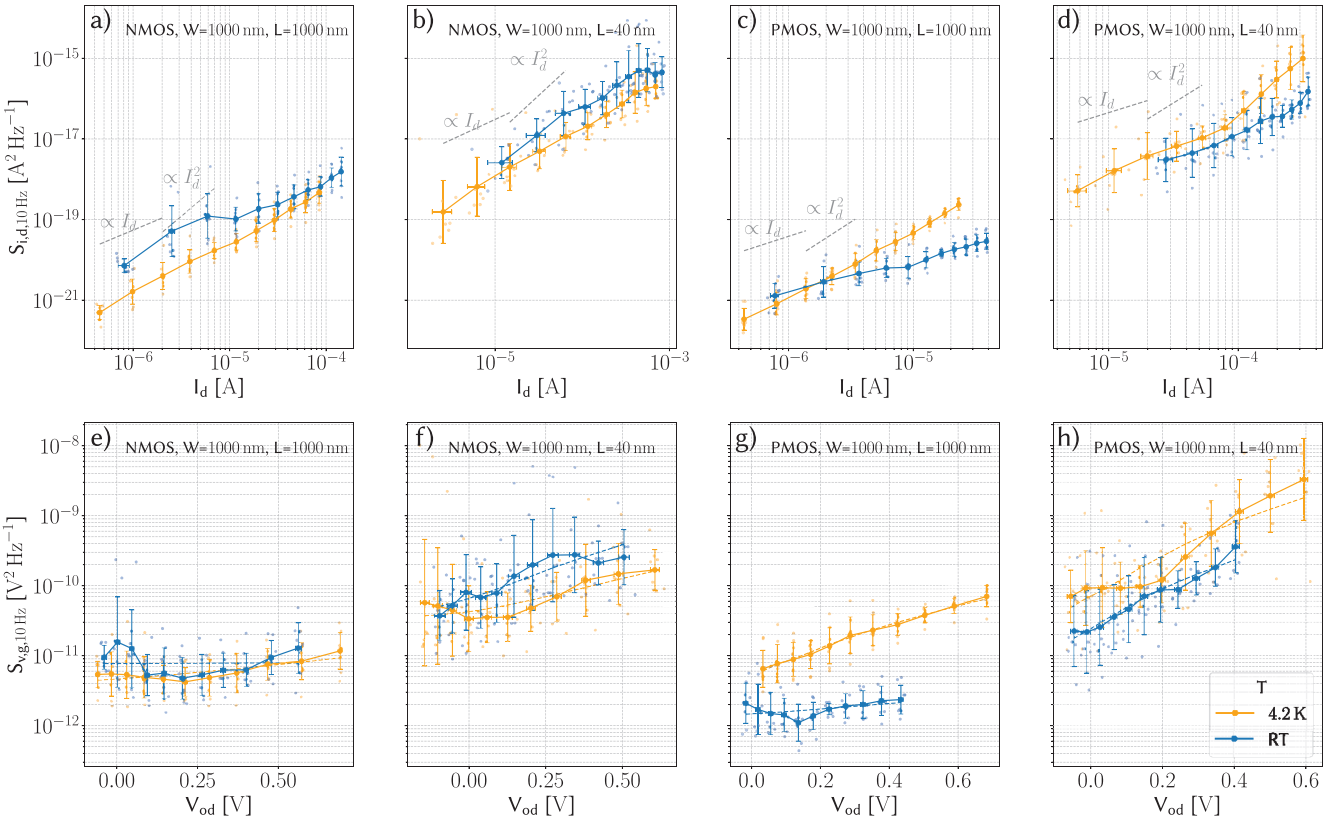

FIGURE 7. **Output-referred (a-d) and input-referred (e-h) noise power spectral density at 10Hz for N/PMOS at V_{gs}=V_{ds} over different bias. Each point represents the measurement from an individual device, while solid lines indicate the mean over the device for each voltage bias.**

TABLE 1. **Flatband voltage and correlation coefficient at RT/4.2K.**

Type	W [nm]	L [nm]	S_{fb} [$V^2\,Hz^{-1}$]	Ω [V^{-1}]
N	1000	1000	4.0e-12/7.7e-12	1.2/0
N	1000	40	3.1e-11/3.8e-11	2.0/3.6
P	1000	1000	2.1e-12/1.4e-12	11.2/0.7
P	1000	40	5.4e-12/5.7e-12	29.9/10.1

devices were calculated to be $1.2 \times 10^{17}\,cm^{-3}\,eV^{-1}$ and $0.5 \times 10^{17}\,cm^{-3}\,eV^{-1}$ at room temperature, respectively. When compared to the values reported in [32] for the closest technology node (45-nm bulk CMOS), these concentrations are slightly lower but in the same order of magnitude.

Using the Boltzmann statistics, the temperature dependence of Eq. (3), scales linearly with T. This qualitative correspondence is in-line with the observations in [10]. The extent of the correlated mobility fluctuations changes with device type and geometry. For the large-area NMOS in e) there are little correlated mobility fluctuations both at RT and cryogenic temperatures, while for the small-area PMOS in h) the effect of correlated mobility is significant at both temperatures. Furthermore, it is interesting to note the significant differences between the RT and cryogenic results for the large-area PMOS in g): the RT results show a strong correlated mobility contribution, which decreases significantly in the cryogenic results. The noise magnitude is similar at RT and 4.2 K for plots e), f) and h), with only the large-area PMOS in g) showing a significant drop in input-referred noise at the same overdrive. The differences in scaling with bias between NMOS and PMOS suggest that the noise is generated via different, possibly doping-dependent, noise mechanisms. Explaining the generally small difference between the RT and the cryogenic behavior with an increase in interface defect states would demand unlikely high values for the defect density. This again suggests band-tail states as a possible cause of the substantiated noise as discussed in [12]. A possible further explanation can be found in [33], with the conclusion that Boltzmann statistics can not be applied, and therefore an effective temperature needs to be introduced, that partially explains the reduced scaling with temperature.

In subthreshold (for negative V_{od}), we would expect a constant characteristic in e)-h), assuming the flat-band voltage spectral density is constant. Although we only probed the edge of this regime, we can observe a tendency for increased input-referred noise in the triode measurements, see the supplementary. This diverging input-referred voltage in subthreshold can be attributed to mobility fluctuations [11], which could be confirmed by further characterization in the deep-subthreshold regime.

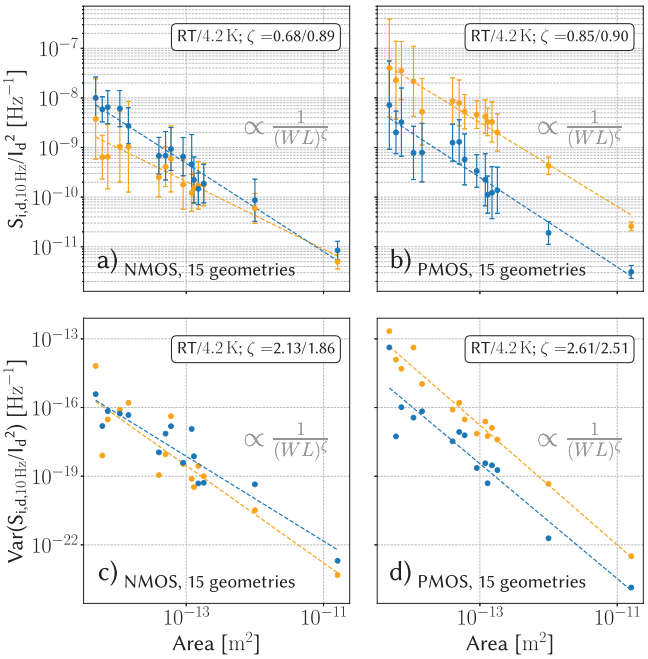

FIGURE 8. a,b) Normalized current noise versus device area for (a) NMOS and (b) PMOS at V_{ds}=V_{gs}=1.1V for 15 different geometries. c,d) Variance of normalized drain current for NMOS (c) and PMOS (d) at same bias point as in a,b.

TABLE 2. Device sizes used in area sweep.

W [nm]	L [nm]	W [nm]	L [nm]
120	40	1000	60
120	50	1000	90
120	60	1000	120
120	90	1000	150
120	120	1000	180
360	360	1000	1000
1000	40	4000	4000
1000	50		

C. AREA DEPENDENCE

At RT, it was shown in [18] that significant variability is present even in larger devices for the cases of a non-uniform channel. At cryogenic temperature, this area dependence of LFN noise has not been systematically explored before. Here we report measurements over area from 8 devices per each of 15 different geometries for both PMOS and NMOS, showing both the normalized current noise (Fig. 8 a)/b) and its variance (Fig. 8 c)/d) as a function of device area. We observe that the noise scaling of NMOS devices shows generally little behavior differences at RT and cryogenic temperature in both expected value and the variance. While we do observe a less than proportional scaling with area for the normalized noise at RT in Fig. 8 a), at 4.2 K that scaling is closer to the expected inverse proportionality. However, this difference is not highly significant in light of the device variability. In contrast to this, the PMOS devices in Fig. 8 b) show significant reduction in normalized noise and variance compared to RT. For PMOS, scaling of the noise is very similar over temperature and close to $1/WL$. For both NMOS and PMOS, the variance scaling in saturation is comparatively weak compared to the cubic dependence expected in the linear region, as explained in [18] with effects caused by the halo-implants. The variance scaling exponent with area is larger for PMOS than for NMOS. At RT, the measurements in the linear region, shown in the supplementary, are closer to the expected scaling of mean and variance with $1/(WL)$ and $1/(WL)^3$ [18], but the cryogenic results differ significantly due to influence of the systematic Lorentzian. As shown in the supplementary, different layout effects were also investigated, but neither metallization on top of the DUTs nor the presence of dummy transistors affected the results shown here.

IV. DISCUSSION

The observations made here demonstrate a wide variety of differences for transistor LFN between RT and cryogenic temperatures. The differences in behavior are strongly dependent on transistor type, geometry, and bias.

For analog designers adopting transistors in saturation, often in moderate inversion, the changes are however minute, given the radical change in temperature, with the input-referred noise being almost unaffected by temperature for most geometries. The expected scaling with temperature predicted in [11] is not observed. A minor increase in input-referred noise can be observed for the NMOS devices, while the minimum-length PMOS devices show a slight decrease. Only the long PMOS devices significantly benefit from cooling to cryogenic temperatures. However, the significant advantage in lower LFN for longer PMOS devices needs to be traded against the difficulties associated with a larger increase in threshold voltage for PMOS devices, compared to their NMOS counterparts [22], also visible in Fig. 2. As LFN is to first order invariant to temperature in most device configurations, the decrease of the white noise [5] results in an expected large increase in frequency of the flicker noise corner. This may require the adoption of techniques for LFN mitigation [34] for a wider range of frequencies than at RT.

The systematic Lorentzian further complicates the picture at cryogenic temperatures. Over a significant frequency range, the additional noise from the Lorentzian dominates the transistors noise behavior. This in turn requires changes the analysis of input-referred noise in amplifiers and the phase noise in oscillators to reflect the device behavior. Furthermore, if using techniques like auto-zeroing or chopping, the distinct spectral shape of the Lorentzian noise requires additional rejection at higher frequency than would otherwise be necessary.

V. CONCLUSION

The extensive study of LFN in MOS transistors presented in this paper, comprising a wide range of bias points and device geometries at both RT and 4.2 K, uncovers a diverse set of

effects and dependencies. Most prominently, we observed and described a systematic Lorentzian spectrum appearing at cryogenic temperatures. Apart from this, we observed remarkably constant behavior with temperature for the bias-dependence of the NMOS, and reductions in input-referred noise for the PMOS. Furthermore, the area scaling was shown to be intact at cryogenic temperature. Since the observed changes have a significant impact on analog design at cryogenic temperatures, the reported characterization will aid the designers of the next-generation cryogenic systems.

ACKNOWLEDGMENT

The authors would like to thank Europractice for MPW services, Atef Akhnoukh for technical support and Ramon Overwater for helpful discussions.

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