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Modular Multilevel Converter-based Arbitrary Wave shape Generator used for High Voltage Testing

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***Abstract*—This paper analyses different design trade-offs for a Modular Multilevel Converter (MMC)-based Arbitrary Wave shape Generator (AWG) used for High Voltage (HV) testing and certification of grid assets such as transformers, switchgear, and cables. Modulation techniques, number of submodules, output voltage levels, arm inductance, and series damping resistance play an essential role in obtaining different waveforms with good quality. Phase-Shift Carrier (PSC) modulation technique proves to be a superior modulation technique for different periodic waveforms over Nearest Level Control (NLC), even when a large number of submodules is considered. With the traditional second-order filter design strategy, proper values of the arm inductance and series resistance can be selected, guaranteeing a good quality of the generated voltage waveforms to verify different dielectric properties of grid-assets. The design of such an AWG is demonstrated with the simulations in MATLAB-Simulink.**

***Index Terms*—MMC, AWG, HV testing, PSC modulation technique, NLC modulation technique, number of output voltage levels**

I. Introduction

High Voltage (HV) equipment in the electrical power system is experiencing new electrical stresses due to the rise of Distribution Generation (DG) systems and massive renewable energy integration by power electronic converters [1,2]. For this reason, HV equipment must more often endure higher dV/dt stress due to solid-state switching and circulating high-frequency current harmonics, which can degrade the reliability of the grid asset. Conventional HV dielectric test sources, i.e., transformers (cascaded and resonant), impulse generators, and rectifier circuits face many limitations in terms of flexibility to generate different wave shapes, current rating, as well as time-consuming to build the test circuit. An alternative solution to generate arbitrary wave shapes is a function generator and HV amplifiers setup [3]. The HV power amplifiers are available with a limited bandwidth and voltage rating. Since these new electrical stresses are mainly generated by the switching mechanisms of the semiconductor devices, the same ingredient is chosen to develop a programmable HV test source for unconventional dielectric testing of various grid assets.

It is not new that the power electronic converters are used to generate arbitrary wave shapes for applications like dielectric barrier discharge plasma actuator [4-5], valve testing [6], and HV testing [7]. Mostly, Cascaded H-Bridge (CHB) converter topology or its variants with different DC source implementation are chosen to implement Arbitrary Wave shapes Generator (AWG) over Modular Multilevel Converter (MMC). Technically, MMC and CHB have similar working principles. CHB has one converter arm where each H-bridge submodule has a dedicated DC source. An MMC can be seen as two CHB converters without the distributed DC sources connected by a series DC voltage source. However, the most popular MMC implementation utilizes submodules with a half-bridge HVDC converter instead of the full-bridge of the CHB. In reality, for the AWG application, the MMC requires two DC sources rated to half of the maximum generated voltage, whereas the many CHB DC sources are rated for submodule voltage level, which will have a floating potential requiring insulation for the maximum generated voltage. Therefore, the design scalability of the CHB solution becomes challenging [4]. For the HV AWG application, this design feature is crucial for easy system maintenance and customization for different voltage levels. Hence, the MMC topology is preferred over the CHB topology for AWG HV application.

Apart from the proof of concept of a MMC-based AWG, this paper offers a detailed study of different suitable modulation techniques, namely the Phase-Shift Carrier (PSC) and Nearest Level Control (NLC); the analysis of minimal requirement on voltage-levels and number of submodules; and the design trade-offs of the second-order passive filter comprised of the arm inductance, series damping resistance, and the load capacitance. A similar analysis is done extensively for energy transmission applications in [8-12]. However, the HV testing application and different wave shapes pose additional requirements on the converter. Hence, section II identifies differences between the HV AWG application and the one of energy transmission. Section III presents the selected MMC topology and the system analytical equations. Section IV discusses the trade-offs among possible modulation techniques, the number of voltage levels, arm inductance, and series resistance and propose the most suitable option for the specified MMC-based AWG. To verify these design choices, several circuits simulations are run in MATLAB-Simulink, and the results are shown in section V. Finally, Section VI concludes the article and gives future research recommendations.

II. HV AWG APPLICATION

HV tests are used to determine the dielectric properties of the insulation materials found in grid-assets, such as dielectric strength, partial discharge, and dielectric losses. HV insulation properties can be modelled electrically as capacitance, and Fig. 1 shows a basic description of how most common HV equipment is tested. The range of the mentioned capacitance for HV equipment ranges from tens of pF to several hundreds of nF. In the EU, they are currently tested according to the IEC standards [13-16], mainly including sinusoidal and lightning impulse test waveforms [17]. This paper focuses on generating different periodic waveforms such as sinusoidal, triangular, trapezoidal, etc., required in unconventional dielectric testing [18]. The difference between HV AWG and energy transmission application is summarized below:

- *The magnitude of power transfer*: For the AWG, the mentioned capacitive load will most likely have a relatively low output current requirement, e.g., up to 5 A [17]. This small current constitutes the reactive power transfer to the capacitive load for building the stress reference voltage. Hence, ideally, the active power requirement is zero or very low and represents only the losses within the converter and test object, which significantly differs from the energy transmission application, which requires several MW power to flow.
- *Type of test object*: As mentioned before, HV test objects behave electrically as a capacitance, whereas power electronic voltage source converters are designed for an equivalent inductive load when integrated into the grid. Also, during an HV test, the breakdown or flashover of the test object is a likely phenomenon. Hence, the test source should supply the energy for the breakdown and protect itself during this fault condition.
- *Frequency of use*: Generally, a power electronic converter integrated in the grid is used for continuous operation. A test source is used only for a fixed amount of time during working hours. For dielectric tests, the typical test duration varies from 1 minute to 4 hours.
- *Performance parameter*: Losses/power efficiency of the converter is of utmost importance in energy transmission, but voltage accuracy/efficiency is important in HV testing. Since there is no active power transfer, specifications will be voltage and current capability, slew rate, small-signal, and large-signal bandwidth.

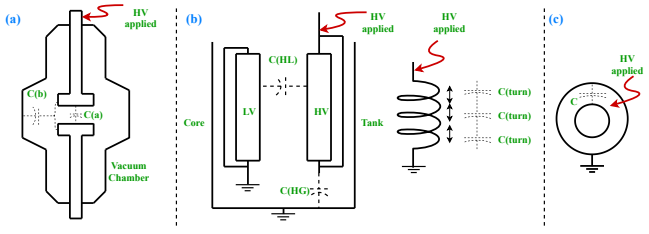

Fig. 1: (a) Vacuum circuit breaker (b) Transformer (c) Cable

III. CONVERTER TOPOLOGY AND SCHEMATIC

Fig.2(a) shows the schematic of the MMC-based HV test source, which has been adapted from the original MMC topology for power transmission application [19-20]. It has a single phase of a MMC, a split DC source, the AC filter comprising the upper and bottom arm inductance, and a capacitive load representing the equivalent electrical model of the HV equipment. In the schematic, there is a series resistance along with the arm inductance. It is not a stray element, but a real passive element to damp the oscillations generated due to the resonance between the arm inductance and the load capacitance. However, the losses in the arm resistors are closely monitored during the design process to ensure its practicability.

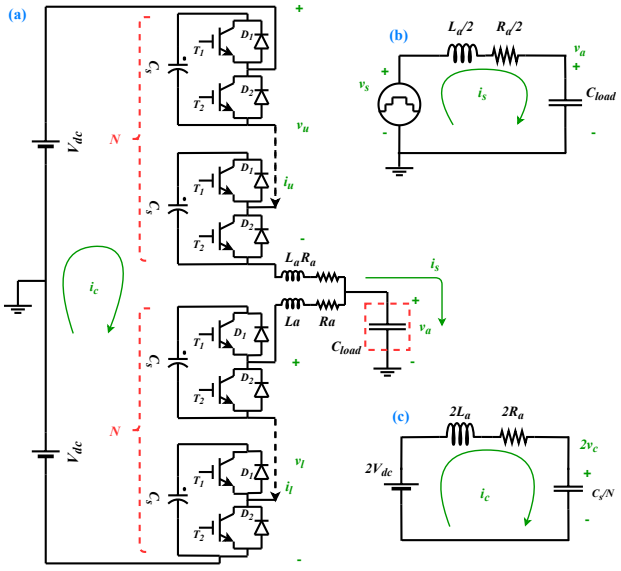

Fig. 2: (a) MMC Schematic for HV AWG application (b) Output current circuit (c) Circulating current circuit

By applying Kirchhoff's Voltage Law (KVL) in the upper and lower arm, dynamic equations of the MMC can be obtained, as shown in (1)-(8). Note that (3) can be obtained by subtracting (2) from (1), whereas (4) is derived by adding (1) and (2). Equations (3) and (4) are coupled equations with four variables v_u, v_l, i_u, and i_l, where $v_{u,l}$ are the sum of all submodule capacitor voltages in the upper and lower arms, respectively. $i_{u,l}$ is the current flowing through the upper and lower arms, respectively. By using the linear transformation shown in (5) and (6), (3) and (4) can be simplified [12]. In (5) and (6), i_s represents the output current, v_s can be understood as the inner electromotive force (emf) generated due to the switching of the submodule capacitors, i_c represents the circulating current, which is driven by the circulating voltage (v_c). After substituting (5) into (3) and (4), partially decoupled differential equations can be obtained, as shown in (7) and (8):

$$V_{dc} - v_u - R_a.i_u - L_a\frac{\mathrm{d}i_u}{\mathrm{d}t} - v_a = 0 \qquad (1)$$

$$V_{dc} - v_l - R_a i_l - L_a \frac{\mathrm{d}i_l}{\mathrm{d}t} + v_a = 0 \quad (2)$$

$$v_l - v_u + R_a(i_l - i_u) + L_a(\frac{\mathrm{d}i_l}{\mathrm{d}t} - \frac{\mathrm{d}i_u}{\mathrm{d}t}) - 2v_a = 0 \quad (3)$$

$$2V_{dc} - v_l - v_u - R_a(i_l + i_u) - L_a(\frac{\mathrm{d}i_l}{\mathrm{d}t} + \frac{\mathrm{d}i_u}{\mathrm{d}t}) = 0 \quad (4)$$

$$i_s = i_u - i_l; v_s = \frac{(v_l - v_u)}{2} \quad (5)$$

$$i_c = \frac{(i_u + i_l)}{2}; v_c = v_u + v_l \quad (6)$$

$$v_s - \frac{R_a}{2} i_s - \frac{L_a}{2} \frac{\mathrm{d}i_s}{\mathrm{d}t} - v_a = 0 \quad (7)$$

$$V_{dc} - v_c - R_a i_c - L_a \frac{\mathrm{d}i_c}{\mathrm{d}t} = 0 \quad (8)$$

Equation (7) is a differential equation in terms of output current and inner emf. It can be represented with the RLC circuit, as shown in Fig. 2(b). Similarly, equation (8) is a differential equation in terms of circulating current and circulating voltage. If (8) is multiplied by two and the circulating voltage is represented by the voltage across the inserted submodule capacitance ($C_{eqv} = C_s/N$), it is possible to represent (8) with the RLC circuit as shown, in Fig. 2(c). In the output current of the circuit, the passive network (L_a, R_a, C_{load}) acts as a filter to v_s and attenuates the harmonics across the load capacitance. The observation above is important with respect to defining design constraint on the arm inductance and series resistance, which is discussed in detail in the next section. The output current flowing through the arm inductance and resistances is responsible for building the desired voltage waveform across the load capacitance. The upper and lower arm current charge or discharge the inserted submodule capacitors over its average value. The change in the submodule capacitor voltage will change the inner emf (v_s) and, in turn, the output voltage. This is how the output current circuit and the circulating current circuit are coupled with the submodule capacitor voltage feedback. Nevertheless, it is important to simplify the complex MMC structure into these simple circuits to understand the design trade-offs and provide an optimal design of the test source, which is covered in the next section.

IV. Design Trade-offs

The following sub-sections analyze the output current of the circuit in detail and discuss the different design trade-offs. The main design elements are the suitable switch modulation techniques, the number of submodules and output voltage levels, the arm inductance, and the series damping resistance. These can be varied to attain the specified performance for given load capacitance. This section aims to provide optimal design guidelines for building the MMC-based AWG with a 100 kV voltage rating, which is required to test medium voltage class equipment. To verify AWG's main design features, the four most common periodic wave shapes, such as sinusoidal, triangular, trapezoidal, asymmetric triangular are used to showcase the performance.

A. Modulation techniques

Among the vast variety of the modulation techniques researched for MMC [20-23], performance of the PSC [22] and the NLC [23] are compared in the section below.

1) Phase Shift Carrier (PSC): In PSC, a traditional sine-triangle double edge modulation technique is used where each submodule is assigned with a different carrier signal. They are phase-shifted between them by $2\pi/N$. These phase-shifted carrier signals move the carrier harmonics to the N^{th} carrier frequency. The upper and lower arms can use the same carrier signals, or they can be phase-shifted by π/N. With π/N phase difference in the case of N is even, and 0 phase difference in the case of N is odd. This generates $(2N + 1)$ number of levels in the output voltage of the converter [22]. This further improves the harmonic spectrum of the output voltage, moving the first carrier frequency to $2N^{th}$ of the carrier frequency. This specific phase difference between the upper and the lower arm ensures that their respective submodules switch at a different time instant, generating a higher number of levels and cancelling more harmonics. Fig. 3 and 4 show the

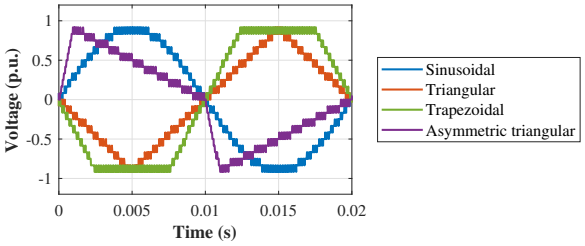

Fig. 3: Time domain waveforms with PSC

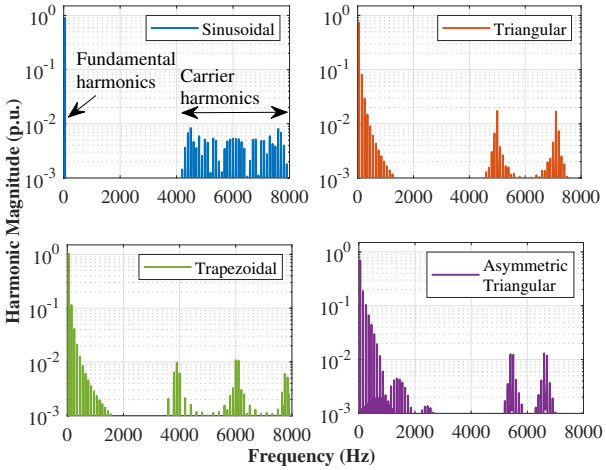

Fig. 4: Frequency domain waveforms with PSC

time and frequency domain analysis of the above mentioned periodic waveforms with 50 Hz fundamental frequency. They are generated with $N = 12$, switching frequency (F_s) equals to 252 Hz, and $(2N + 1)$ PSC modulation technique. In Fig. 4, it can be observed that the sinusoidal waveform does not have any baseband harmonics, whereas other waveforms have different baseband harmonics depending upon the frequency

spectrum of the reference waveform. Filtering these sideband harmonics would result in waveforms with a good match to that of reference waveform which is required for the HV AWG application. The THD of the sinusoidal waveform shown in Fig. 4 is 4.7 %.

2) Nearest Level Control (NLC): NLC is a carrier less modulation technique that calculates the number of submodules to be inserted using either equation (9) or (10) and assign gate pulses accordingly. Equation (9) results in $(N+1)$ number of output voltage levels [23], whereas equation (10) generates $(2N+1)$ number of output voltage levels [24].

$$n_{u,l} = round_{0.5}\left(\frac{N(V_{dc} \mp V_{ref})}{2V_{dc}}\right) \tag{9}$$

$$n_{u,l} = round_{0.25}\left(\frac{N(V_{dc} \mp V_{ref})}{2V_{dc}}\right) \tag{10}$$

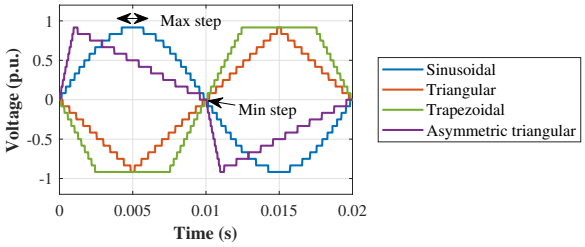

Fig. 5: Time domain waveforms with NLC

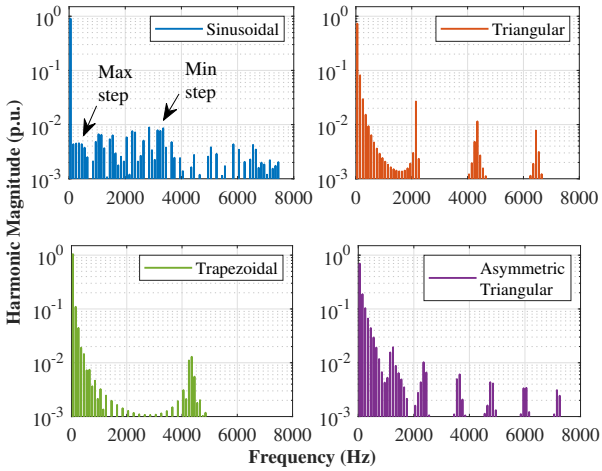

Fig. 6: Frequency domain waveforms with NLC

Fig. 5 and 6 show time and frequency domain analysis of the periodic waveforms generated with 50 Hz fundamental frequency. They are generated with the number of submodules to be $N = 12$ and $(2N+1)$ NLC modulation technique. It is found that the Fourier spectrum of the sinusoidal waveform is non-characteristics. The reason behind this is that the slope of the sinusoidal waveform changes throughout its one-quarter cycle. This changes the time step generated using the NLC modulation technique, which results in a variable frequency spectrum. With $N = 12$ and 50 Hz fundamental frequency, the time step varies between 265 µs to 1.84 ms, and corresponding equivalent frequencies are 3.77 kHz and 542.24 Hz. This analysis gives two important observations of the staircase-based sinusoidal voltage waveform. One is that the staircase waveform generated using NLC has harmonics near the fundamental frequency. Unlike PSC, these harmonics only can be moved slightly away from the fundamental frequency with a higher number of levels in the waveform. The second point is that the shortest step (265 µs) corresponds to the highest value of the harmonics spectrum (3.77 kHz). With the logarithmic scale, all the magnitudes look almost the same. When observed closely, the peak lies near 3.77 kHz. However, NLC introduces switching harmonics as low as 542.24 Hz, which is too close to the fundamental frequency. The near-fundamental switching harmonics and the difficulty to move them to higher frequencies increases filter requirement with NLC. In the case of the non-sinusoidal waveforms, the frequency-domain spectrum in Fig. 6 shows a repetitive spectrum. The frequency of the repetition is inverse of the time of step of the involved waveform. For asymmetric triangular waveform, there are two different time steps involved corresponding to two different slopes. Hence, the frequency of repetition visible in the figures corresponds to the slower slope. While designing the filter, the switching harmonics corresponding to the faster slope (farther in the right, $>$ 8 kHz) will be attenuated leaving lower harmonics in the output voltage waveform [25]. This is another problem faced by NLC modulation technique and it might alter the electric stress applied to the insulation under test [26]. The THD of the sinusoidal waveform shown in Fig. 6 is 3.3 %.

B. Number of levels in the output voltage waveform

This section discusses how the performance of each modulation technique changes as the number of output voltage levels is increased. The effect of the number of output voltage levels on the generated sinusoidal output signal using the above mentioned modulation techniques is studied in Table I with respect to THD, Highest Harmonic (HH) magnitude in per units, and the frequency at which HH occurs. From the table I, the critical observation is that the NLC and PSC have similar performance with higher values of N. The added advantage with PSC is about shifting the harmonics spectrum to higher frequencies. With NLC, as the values of N increases, the magnitude of the harmonics reduces too, and the frequency at which HH occurs increases slightly. However, it still contains lower order harmonics and, thus, the filtering effort does not reduce significantly. Unlike, switching frequency flexibility present in PSC, the frequency spectrum of NLC can not be changed for the given number of submodules. Hence, the PSC modulation technique proves to be better suitable for the accurate periodic waveforms generation.

The number of output voltage levels obtained in the MMC is directly dictated by the number of inserted submodules and the implemented modulation technique. The number of submodules depends upon the DC link voltage and the commercially available semiconductor voltage rating. For 100 kV output voltage rated test source, the required total DC link voltage is 200 kV for the half-bridge configuration depicted in Fig.

TABLE I: Number of levels of its performance for NLC and PSC

No of levels	NLC			PSC with Fs=252 Hz		
	THD	HH magnitude (p.u.)	Freq. at which HH occur (Hz)	THD	HH magnitude (p.u.)	Freq. at which HH occur (Hz)
5	17.6	$1.1e^{-1}$	550	27	$0.8e^{-1}$	750
13	6.4	$2.8e^{-2}$	1750	9.2	$1.8e^{-2}$	2150
25	3.3	$0.9e^{-2}$	3550	4.7	$1.0e^{-2}$	4300
51	1.6	$3.5e^{-3}$	7600	2.3	$4.0e^{-3}$	8850
67	1.2	$2.4e^{-3}$	9750	1.7	$2.7e^{-3}$	11700
101	0.8	$1.3e^{-3}$	15350	1.1	$1.6e^{-}3$	17750
135	0.6	$0.9e^{-3}$	20750	0.8	$1.0e^{-3}$	23400
201	0.4	$5.7e^{-4}$	31050	0.6	$6.3e^{-4}$	34950
401	0.2	$2.3e^{-4}$	62350	0.3	$2.5e^{-4}$	69750

TABLE II: Voltage rating per submodule and obtained no. of levels

N	Voltage rating per submodule (kV)	Obtained no. of output voltage levels	
		(N+1) modulation	(2N+1) modulation
12	16.7	13	25
33	6	34	67
50	4	51	101
67	3	68	135
100	2	101	201
200	1	201	401

2. The possible combinations of the number of submodules, voltage rating per submodule, and the number of output voltage levels obtained are shown in Table II.

Since the HV AWG application requires switches with low current ratings, power modules used for HVDC transmission are not suitable, and only discrete switches are an option. Discrete TO-packaged IGBTs are available with 1.7 kV, 2.5 kV, 3 kV, 3.6 kV, and 4 kV from 5 to 280 A [10,27]. Table II clearly shows that the voltage rating per submodule with 4 kV and more will need switches with a blocking capability of more than 6 kV in order to keep a reasonable safety margin for reaching a minimum reliability standard [10,28]. If the voltage rating per submodule is 2 kV or less, a complex system for control and communication is needed. Hence, a choice of 3 kV submodule rating is a practical option. With a 3 kV voltage rating per submodule, the 67 submodules can deliver 135 output voltage levels. The following subsection discusses the design of arm inductance and series resistance with the 67 number of submodules and PSC modulation technique.

C. Arm inductance and series resistance

Since the equivalent passive network load acts as a series RCL filter, it is possible to choose the correct values of L_a and R_a to remove the unwanted switching from the output voltage waveform. This is important for the HV AWG application because the waveform decides the electric stress applied to the HV equipment and the switched waveform may create unwanted higher stress in the device under test [1][26]. More sophisticated filter topologies such as the popular grid-connected LCL filter add too many full voltage components and increase the system's cost. Hence, the transfer function of the output current circuit is derived in the Laplace domain to perform the AC filter design, as shown in (11). From the same equation, (12) and (13) are written in terms of L_a and R_a to keep the fundamental and essential baseband frequencies ($n_1 f_{req}$) for non-sinusoidal wave shapes and to suppress out the highest harmonics present ($n_2 f_{req}$). In these equations, n_1 represents how many baseband harmonics to keep with 1 $\%$ error, and n_2 represents which carrier harmonic to suppress by k factor. These values of n_1 and n_2 are decided based on the frequency spectrum of v_s, which was discussed earlier in Session IV-A. Such an analysis is done for different periodic signals with 50 Hz and 1 kHz frequency for a load capacitance of 10 nF, the results with both NLC and PSC modulation techniques are summarized in Table III. From this table, it is visible that the lower switching harmonics in the frequency spectrum of NLC made the design of L_a and R_a bulkier as compared to PSC design, which is especially visible with 50 Hz fundamental frequency.

TABLE III: Values of L_a and R_a for different wave shapes

Wave shape	Mod. Technique	n_1	n_2	k	F_s (kHz)	L_a (mH)	R_a (kΩ)
Sin	PSC	5	1222	0.01	10.5	$3.2e^{-1}$	1.0
	NLC	5	415	0.01	-	$2.9e^{0}$	1.4
Tri	PSC	10	3270	0.02	1.265	$3.4e^{0}$	9.1
	NLC	10	241	0.02	-	$1.7e^{3}$	27.4
Trap	PSC	10	1166	0.01	10.5	$3.7e^{-1}$	0.6
	NLC	10	483	0.01	-	$2.2e^{0}$	1.0
Atri	PSC	15	3324	0.03	1.265	$1.9e^{0}$	6.1
	NLC	15	1213	0.03	-	$6.7e^{1}$	7.9

$$\frac{V_a[s]}{V_s[s]} = \frac{2}{s^2 L_a C_{load} + s R_a C_{load} + 2} \tag{11}$$

$$abs\left(\frac{V_a[s]}{V_s[s]}\right)_{@n_1 f_{req}} = 0.99 \tag{12}$$

$$abs\left(\frac{V_a[s]}{V_s[s]}\right)_{@n_2 f_{req}} = k \tag{13}$$

V. Simulation results

This section presents the simulation results with the parameters summarized in Table III and IV. The AWG test source employs a direct PSC modulation technique. For submodule capacitor voltage balancing with PSC modulation technique, switching frequency (F_s) is chosen as a non-integer multiple of fundamental frequency [22]. The safe operation of the AWG test source is ensured by submodule capacitor voltage feedback. In this paper, the submodule capacitance choice is not investigated and the simulation results shown are considering a capacitance of 10 µF per submodule. The output performance of the AWG for each waveform is shown with the output voltage, output current, and circulating current. Few individual submodule capacitor voltages and average submodule capacitor voltages from the upper and lower arm are selected to check if they are balancing or not. Out of 67 submodules, 1^{st} , 22^{nd}, 44^{th} and 67^{th} are chosen to display the performance of the submodule capacitor voltages. They are abbreviated as Upper Arm as UA and Lower Arm as LA, followed by the number and average in the legend. The

output characteristics are shown for only one cycle, whereas the submodule capacitor voltages are simulated for a relatively long time to verify the conversion of the steady-state voltages.

TABLE IV: System parameters

Description	Values
DC-link voltage ($2V_{DC}$)	200 kV
Modulation index (m_a)	0.9
Number of submodules per arm (N)	67
Submodule capacitance (C_s)	10 μF

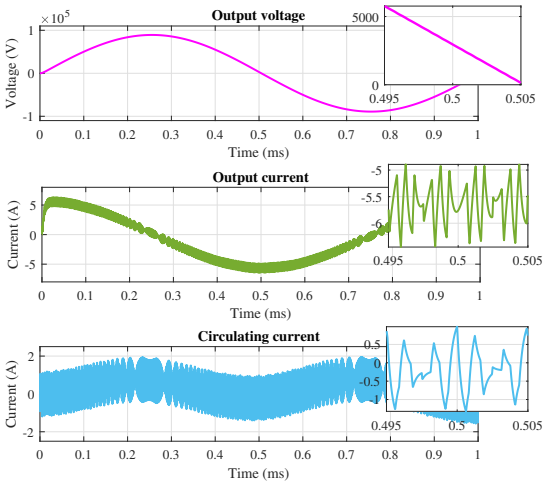

Fig. 7: Output performance of 1 kHz sinusoidal

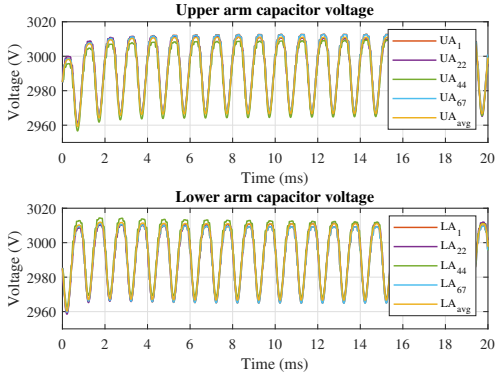

Fig. 8: Submodule capacitor voltages of 1 kHz sinusoidal

Fig. 7,9,11,13 show that the filter design works well for different waveforms with different frequencies. The quality of the generated waveforms is calculated using THD, as shown in (14) and (15) and the results are summarized in Table V. For the different waveforms, obtained THD is less than 1 %.

$$THD_{sin} = \frac{\sqrt{(\sum_{h=2}^{\infty} V_{h,out}^2 + V_{o,out}^2)}}{V_{1,out}} \tag{14}$$

$$THD_{nonsin} = \frac{\sqrt{\sum_{h=2}^{\infty}(V_{h,ref} - V_{h,out})^2 + V_{o,out}^2}}{V_{1,out}} \tag{15}$$

The next step is to pay attention to the amount of power dissipated in the arm resistance to see the feasibility of such a

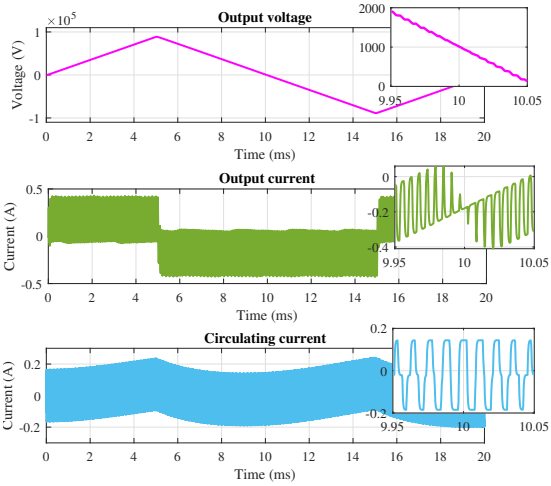

Fig. 9: Output performance of 50 Hz triangular

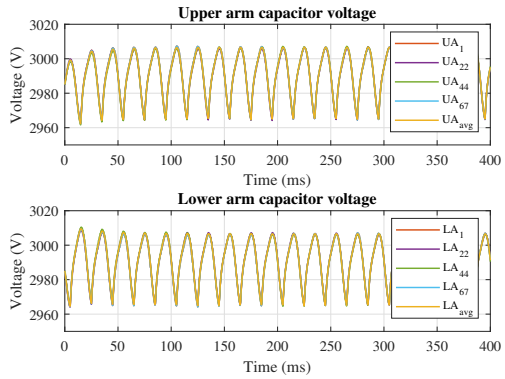

Fig. 10: Submodule capacitor voltage of 50 Hz triangular

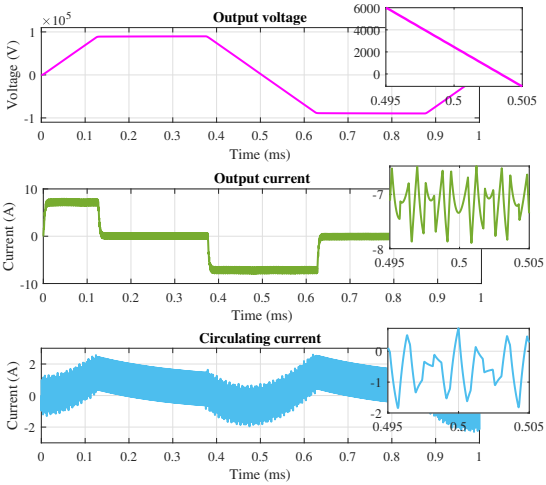

Fig. 11: Output performance of 1 kHz trapezoidal

design. Average power loss in the series arm resistor with the particular wave shape is calculated in Table V, and it is within a particular limit. Apart from the quality of the wave shape generated, it is important to pay attention to the submodule

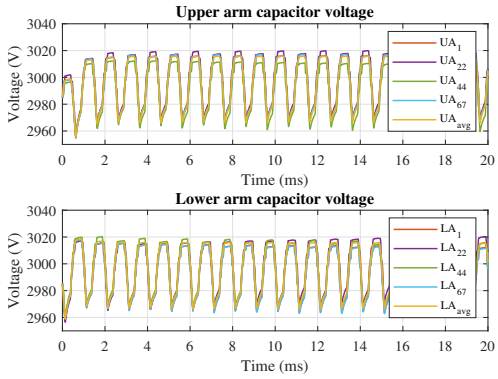

Fig. 12: Submodule capacitor voltage of 1 kHz trapezoidal

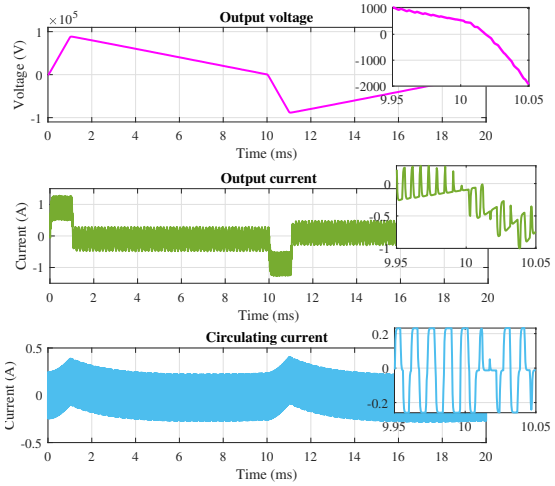

Fig. 13: Output performance of 50 Hz asymmetric triangular

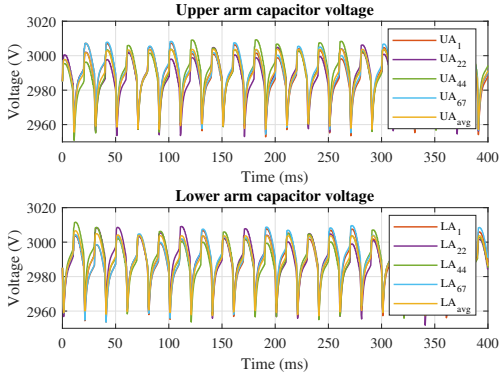

Fig. 14: Submodule capacitor voltage of 50 Hz asymmetric triangular

capacitor voltage. Fig. 8,10,12,14 show that the submodule capacitor voltages (UA_1, UA_{22}, UA_{44}, UA_{67}, UA_{avg}, LA_1, LA_{22}, LA_{44}, LA_{67}, LA_{avg}) are balanced. Here, it is important to point out that the capacitor voltage balancing is possible even with the trapezoidal wave shape, which has a constant DC part due to the capacitive load.

TABLE V: Performance of Different Wave shapes

Number	Wave shape	THD	Losses in Ra (kW)
1	1 kHz Sinusoidal	0.09	4.42
2	50 Hz Triangular	0.17	0.21
3	1 kHz Trapezoidal with 125 us rise time	0.11	4.31
4	50 Hz Asymmetric Triangular with 1 ms rise time	0.75	0.35

VI. Conclusion and Further Recommendations

Apart from demonstrating the capability of the MMC-based AWG for the HV testing application, this paper discussed different design trade-offs present in the modulation technique, number of levels, number of submodules, arm resistance, and arm inductance. It is found that the PSC modulation technique provides two additional advantages over NLC. It shifts the carrier harmonics to $2N^{th}$ of the fixed switching frequency without changing any baseband harmonics present due to non-sinusoidal wave shape. Whereas, the NLC modulation technique has a variable frequency operation which generates lower order harmonics. It interferes with the baseband harmonics of the reference waveform and increases filtering effort. As the number of output voltage levels are increased in the output voltage, NLC and PSC exhibit similar harmonic performance in terms of THD and highest harmonics present. Even with larger N, NLC contains lower order harmonics, which keeps the filtering requirement significantly high. The simulation results prove that the employed design methodology for arm resistance and arm inductance works well and generates the wave shapes with less than 1 % THD. Also, it is seen that the submodule capacitor voltage naturally balances out with the mentioned parameter in the control architecture.

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