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Aging and Sintered Layer Defect Detection of Discrete MOSFETs Using Frequency Domain Reflectometry Associated With Parasitic Resistance

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***Abstract*—Metal-oxide-semiconductor field-effect transistors (MOSFETs) undergo fatigue degradation under high thermal and electrical stresses. This process results in changes in their parasitic parameters, which can be detected using frequency domain reflectometry (FDR). Frequency domain impedance analysis is employed to characterize the various quality states of Si and SiC MOSFETs obtained from accelerated aging experiments. Results demonstrate a consistent increase in parasitic resistance as the devices degrade. By determining the drain-source parasitic resistance at the self-resonant frequency (f_{SRF}) and the drain-source on-resistance for MOSFETs with varying degradation degrees, positive linear numerical fitting equations (14)–(15) are established to predict MOSFET degradation under zero DC bias voltage. In addition, FDR technology is used to identify the drain parasitic resistance at the f_{SRF} of MOSFET samples with different sizes of defects in the sintered silver layer. These results reveal a positive correlation between the quality of the sintered silver layer and R_{D_SRF}. The proposed approach is an effective quality screening technology for power semiconductor devices without requiring power-on treatment.**

***Index Terms*—MOSFET, aging degradation, sintered silver layer, defect, two-port network, parasitic resistance.**

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I. Introduction

POWER converters are the core components responsible for power conversion in electronic systems. They are widely used in various industrial and consumer applications, such as new energy vehicles (motor drives system), smart grids (wind power, photovoltaic converters, and flexible DC converter stations), urban rail transit (traction converters), and energy conservation and environmental protection (variable-frequency drive). The metal-oxide-semiconductor field-effect transistor (MOSFET) is a critical component in power conversion systems. It encounters the demanding requirements of power converters, which necessitates its ability to withstand mechanical and thermoelectrical stresses while maintaining high reliability during long-term periodic operation. The trend toward increasing power density and efficiency in power electronic converters demands higher switching frequencies for power semiconductor devices. Emerging wide-bandgap SiC power devices have been developed to address this requirement [1], [2]. However, their ultra-fast switching characteristics (i.e., high dv/dt or di/dt) can result in severe adverse effects on the devices in practical applications, such as device breakdown, open circuits, material degradation, and bond wire fractures. All these factors lead to failures. Currently, power semiconductor devices have emerged as the most vulnerable components in power converters, and they account for nearly 31% of failures in power electronic systems due to power semiconductor degradation [3]. Consequently, enhancing the reliability of MOSFETs has initiated a surging interest, which facilitates significant research efforts in the development of degradation detection techniques.

Estimating the reliability of MOSFETs has been the subject of numerous studies in recent literature. These approaches can be categorized into three classes according to the type of degradation models used: the degradation precursor-based approach, morphology characteristic-based approach, and reflectometry signal-based approach. The quality status of MOSFET devices is typically assessed by directly identifying changes in electrical parameters between one or two terminals, which are known as precursor parameters. Commonly used degradation precursors include gate-source threshold voltage

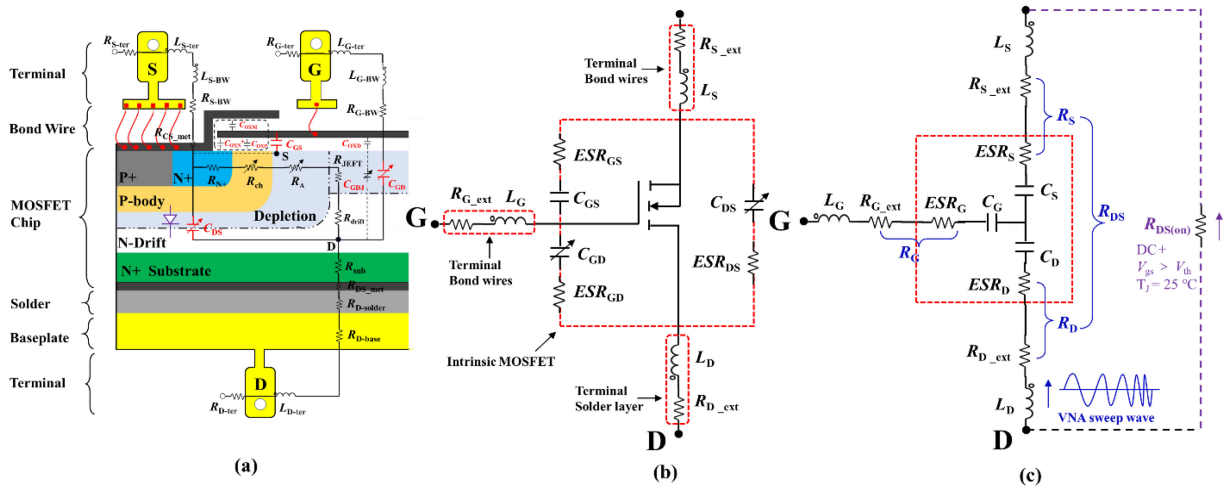


Fig. 1. Power MOSFET: (a) Cross-section of a power MOSFET. (b) MOSFET small-signal equivalent circuit model in the form of capacitor delta-connection. (c) MOSFET small-signal equivalent circuit model in the form of capacitor star-connection.

($V_{GE(TH)}$) [4], gate leakage current (I_G) [5], on-resistance ($R_{DS(on)}$) [6], drain-source current (I_D) [7], short circuit current (I_{SC}) [8], junction temperature (T_j) [9], the thermal resistance from junction to case (R_{th}) [10], turn-on time (t_{on}), and turn-off time (t_{off}) [11]. However, accuracy in measuring degradation precursors such as $R_{DS(on)}$, $V_{GE(TH)}$, I_D, I_{SC}, and R_{th} heavily relies on the die's T_j. Unfortunately, T_j cannot be directly measured, which causes difficulty in controlling stable junction temperature. Moreover, measurement accuracy (I_G and $R_{DS(on)}$) can be affected by changes in bus voltage and current, which requires strict test condition control. The switching duration of the MOSFET (t_{on}, t_{off}) can provide aging information related to gate degradation. However, accurately capturing these changes requires a high-resolution detection circuit with a high-frequency pulse width-modulated signal. Morphology characteristic-based approaches include thermal imaging technology (eddy current pulse thermal imaging and infrared imaging) [12], [13] and structural imaging (X-ray imaging, ultrasound imaging, and industrial computerized tomography) [14], [15]. Thermal imaging detects potential defects by monitoring changes in the temperature field distribution at the target location, but it necessitates opening the plastic enclosure, which compromises structural integrity. Structural imaging examines bond wire and solder layer quality by analyzing echo information from pulse signals, but the penetration ability of the pulse ray is easily affected by the degradation of other material layers. The reflectometry signal-based approach is a novel method for aging detection associated with MOSFETs [16], [17], [18], [19], [20]. It utilizes a high-frequency modulated signal as the incident wave and can determine MOSFETs' aging based on impedance changes by analyzing the reflected signal. However, this approach can only estimate power device aging when it is in the on-state, and the response results and sensitivities vary depending on drain-source currents and incident signal frequencies. This limitation poses challenges in accurately detecting small impedance changes in MOSFETs.

This study proposes a novel approach for evaluating MOSFET degradation by identifying changes in parasitic resistance. Degradation induces impedance variations in various types of devices, including power devices, which makes this characteristic usable to assess MOSFET reliability. Frequency domain reflectometry (FDR) is employed to characterize impedance variations. MOSFETs can be regarded as second-order *RLC* circuits, which consist of independent inductances, capacitances, and resistances in series, with the constructed equivalent circuit conforming to a two-port network model. Consequently, a specifically designed two-port network measurement system is utilized to accurately characterize the frequency domain impedance of the MOSFET. The rapid assessment of MOSFET quality is achievable by formulating a mapping model that associates alterations in parasitic resistance with MOSFET aging degradation and sintered silver layer defects. This approach presents considerable potential for quality screening of power devices in practical applications, which eliminates the necessity for power-on treatment.

II. Methodologies

A. MOSFET Small-Signal Equivalent Circuit

The diagram in Fig. 1(a) illustrates the cross-sectional structure of a half vertical-diffused MOSFET, along with annotations indicating the physical structures responsible for creating parasitic elements [21]. MOSFETs can be represented as voltage-controlled current sources consisting of constant and variable active components, internal parasitic capacitances, resistances, and inductances. Fig. 1(b) shows the small-signal equivalent circuit based on the physical structure of the MOSFET, including drain-source capacitance (C_{DS}), gate-source capacitance (C_{GS}), and gate-drain capacitance (C_{GD}). These capacitances are considered second-order *RC* circuits formed by a combination of parasitic capacitance and equivalent series resistance (*ESR*) in frequency impedance measurement. Each internal capacitance can be converted

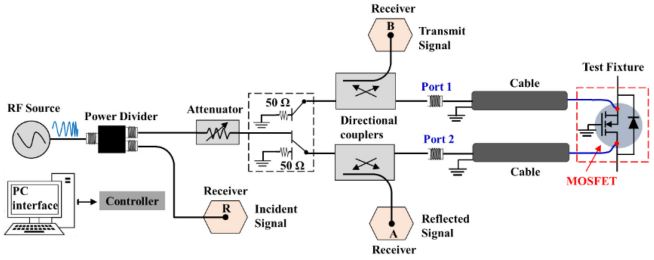


Fig. 2. Schematic of the FDR system for characterizing a MOSFET.

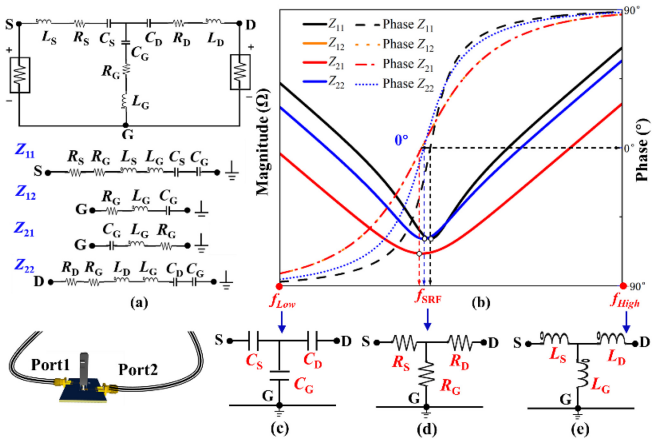


Fig. 3. Method for extracting parasitic parameters: (a) Two-port network representation of a MOSFET under zero biasing conditions, where each of the MOSFET Z-parameters Z_{11}, Z_{12}, Z_{21}, and Z_{22} demonstrates a second-order RLC circuit, (b) Impedance magnitude and phase curves of the MOSFET, (c) Equivalent representation of the two-port network for a MOSFET at low frequency, (d) Equivalent representation of the two-port network for a MOSFET at the self-resonant frequency, (e) Equivalent representation of the two-port network for a MOSFET at high frequency.

into a star-connection (C_{GD}, C_{DS}, and C_{GS}) using (1)–(3) to comply with a standard two-port network form for solving frequency domain impedance [22]. The simplified MOSFET small-signal equivalent circuit in the form of capacitor star-connection is shown in Fig. 1(c), where $R_S = ESR_S + R_{S\_ext}$, $R_G = ESR_G + R_{G\_ext}$, and $ESR_D = ESR_D + R_{D\_ext}$. The effective channel length of the MOSFET is controlled by the gate-source voltage V_{GS}. If $V_{GS} > V_{GS(TH)}$, then the MOSFET is fully conductive, with $R_{DS} = \Delta V_{DS} / \Delta I_D$.

$$C_{GS} = (C_G \cdot C_S)/(C_G + C_D + C_S), \tag{1}$$

$$C_{GD} = (C_G \cdot C_D)/(C_G + C_D + C_S), \tag{2}$$

$$C_{DS} = (C_D \cdot C_S)/(C_G + C_D + C_S). \tag{3}$$

B. Fundamentals of FDR

Time domain reflectometry (TDR) and FDR are prevalent reflectometry methods. TDR excels at detecting significant impedance mismatches, such as open or short circuit faults. However, noise and interference can affect its recognition capabilities for minor impedance variations [23]. FDR utilizes swept-frequency signals across a broad frequency range, which is typically from kilohertz (kHz) to gigahertz (GHz). It allows the extraction of magnitude and phase of reflected signals to identify impedance anomalies or minor changes at specific frequencies. A block diagram of FDR is shown in Fig. 2. Several stepped-frequency sine waves are transmitted along the transmission line. When encountering an impedance discontinuity, a portion of the signal is reflected to the source, while the rest continues along the line. By analyzing the ratios of incident, reflected, and transmitted signals, the S-parameters of the MOSFET can be determined and subsequently transformed into frequency domain impedance.

Similar to TDR, FDR characterizes impedance mismatches along a transmission path by analyzing the reflection coefficient (Γ_L) and the transmission coefficient (T_L). Γ_L and T_L can be expressed as

$$\Gamma_L = \frac{V_{reflected}}{V_{incident}} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{4}$$

$$T_L = \frac{V_{transmitted}}{V_{incident}} = 1 + \Gamma_L = \frac{2Z_L}{Z_L + Z_0}. \tag{5}$$

Here, Z_O represents the characteristic impedance of the cable connecting the source and the MOSFET, and Z_L is the discontinuity impedance. For capacitors, ESR increases as aging time progresses [24], [25]. A similar phenomenon occurs in MOSFETs [16], [17], [18], [19], [20], which have three capacitances (C_{GS}, C_{GD}, and C_{DS}) that can be affected by aging-related damages, such as gate oxide degradation, aluminum pad metallization reconstruction, and Kirkendall void formation at bond-pad and pad-attach interfaces. Aging degradation can be equivalent to additional series resistances in the source-drain loop circuit, which increases ESR and $R_{DS(on)}$. These changes are reflected in the equivalent impedance between the drain and source terminals (Z_{DS}). The difference between a healthy and an aged MOSFET can be expressed as (6).

$$\left|Z_{DS\_Hea} - Z_{DS\_Age}\right| = \Delta Z_{DS}. \tag{6}$$

where Z_{DS_Hea}, Z_{DS_Age}, and ΔZ_{DS} represent the equivalent impedances of a healthy and aged MOSFET and their difference, respectively.

FDR characterizes impedance changes by measuring the amplitude and phase values of reflected or transmitted signals at different frequencies, with high resolution to identify the small impedance changes (ΔZ_{DS}) caused by MOSFET aging.

C. Parasitic Resistance Extraction Based on FDR

The Z-impedance curves (Z_{11}, Z_{12}, Z_{21}, Z_{22}) of a typical MOSFET are displayed in Fig. 3. At the high frequency (f_{High}), the impedance phase angle is approximately 90°, which indicates that the inductive reactance due to parasitic inductance dominates. The equivalent circuit model is simplified to Fig. 3(e), with $Z_{High} = w \times L$, for calculating L. The MOSFET frequency response exhibits a minimum impedance point, and the phase angle is 0° at the self-resonant frequency (f_{SRF}) [26], as illustrated in Fig. 3(d). Consequently, the MOSFET exhibits resistive behavior, with $Z_{SRF} = R$. If L and f_{SRF} are extracted, then the parasitic capacitance C can be swiftly determined using the expression $w_{SRF} = \frac{1}{\sqrt{L \times C}}$.

The MOSFET two-port network model is shown in Fig. 3(a), with the source, drain, and gate terminal connected

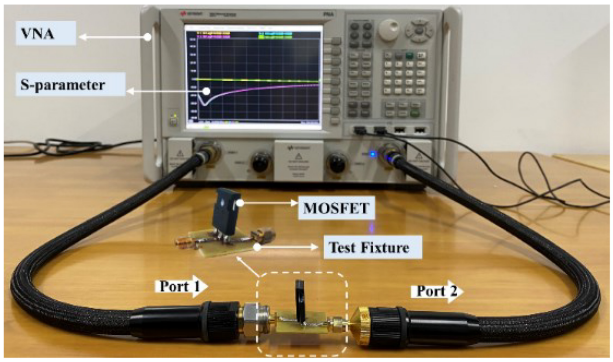


Fig. 4. Two-port network measurement system utilizing a specially designed test fixture to connect the discrete MOSFET to the VNA.

to the vector network analyzer (VNA) Ports 1, 2, and Ground, respectively. Initially, the *S*-parameters of a discrete MOSFET are measured over a frequency range of 10–300 MHz and then converted into *Z*-parameters (Z_{11}, Z_{12}, Z_{21}, Z_{22}). Z-parameters can be represented using the expressions (7)–(9), shown at the bottom of the page. The parasitic inductances L_S, L_G, and L_D, parasitic resistances R_S, R_G, and R_D, and parasitic capacitances C_{GS}, C_{DS}, and C_{GD} can be calculated from Z_{meas}.

The measurement setup of a two-port network is shown in Fig. 4. A printed circuit board (PCB) test fixture is designed to connect the MOSFET terminals to the VNA ports. The measurement plane shifts from the device port to both ends of the testing fixture due to the inclusion of the test fixture. This shift introduces additional parasitic parameters that can affect measurement accuracy. Calibration techniques are employed to counteract the influence of these parasitic parameters [27]. A Keysight 80502D calibration kit performs a Short-Open-Load de-embedding procedure. In addition, a new "Through" PCB calibration element has been designed to execute a "Through" calibration procedure. This procedure extends the measurement plane closer to the MOSFET plane.

III. Experimental Results and Discussion

A. Parasitic Parameter Extraction Verification for MOSFETs in TO-247

In this study, a 400 V N-Channel IRFP340 Si-MOSFET and a 1200 V N-Channel C2M0160120D SiC-MOSFET in a TO-247 package are selected to verify the accuracy of the parasitic resistance extraction approach and perform aging experiments. MOSFETs are installed on the designed testing fixture to connect to the VNA, which allows the extraction of Z-parameters in the frequency range of 10–300 MHz. Using the calculation approach described in Section II-B, all parasitic parameter values in the small-signal equivalent circuit model of Si-MOSFET and SiC-MOSFET are characterized from the obtained *Z*-parameters. After the parasitic parameters are extracted, they are incorporated into the constructed MOSFET two-port network model for simulation in the Advanced Design System (ADS). If the simulation results align well with the experimental data, then the effectiveness of the established small-signal equivalent circuit and the derived method for parasitic parameter extraction is confirmed. The resonance frequency expression $w_{SRF} = \frac{1}{\sqrt{L \times C}}$ indicates that the size of f_{SRF} is inversely proportional to the product of parasitic inductance L and parasitic capacitance C. Parasitic inductance L is determined by the length of the current transmission path. In the TO-247 packaging structure, using the same metal packaging framework for C2M0160120D and IRFP340 results in their similar parasitic inductance values. Therefore, C determines f_{SRF}. The critical breakdown field of SiC is 10 times that of Si. Thus, SiC devices can significantly reduce chip sizes when compared with Si devices at equivalent power levels. This reduction leads to lower parasitic capacitance. According to the datasheets provided by the packaging manufacturers for C2M0160120D and IRFP340, their respective output capacitances C_{iss} ($C_{GD} + C_{GS}$) at 1 MHz are 525 and 4500 pF, which clearly indicates the smaller junction capacitance of SiC-MOSFET. Consequently, the resonance frequency of C2M0160120D is higher than that of IRFP340, which results in faster switching speeds. Fig. 5 displays the frequency response curves of the *Z*-parameters obtained from ADS simulation and VNA experimental measurement. The resonant frequencies of each impedance curve (Z_{11}, Z_{12}, Z_{21}, and Z_{22}) for the C2M0160120D SiC-MOSFET are approximately twice as high as those of the IRFP340 Si-MOSFET. The traditional high-precision impedance analyzer, which is commonly employed, encounters challenges associated with impedance matching. Thus, the measurement frequencies are restricted to a maximum of 120 MHz. However, the two-port network measurement method proposed in this study circumvents the limitations imposed by measurement frequencies. This method is particularly well suited for the impedance characterization of SiC and GaN high-frequency devices, which allows for a swift evaluation of the switching characteristics and quality of the chip through the characterization of f_{SRF}. For the IRFP340 Si-MOSFET, the red dash-dotted lines (ADS simulation) agree well with the black solid lines (VNA measurement) for *Z*-parameters Z_{11}, Z_{12}, Z_{21}, and Z_{22}. Similarly, the green dash-dotted lines and the blue solid lines exhibit high consistency for each *Z*-parameter of the C2M0160120D SiC-MOSFET.

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} R_S+R_G+j\omega(L_S+L_G)+\frac{-1}{j\omega C_S}+\frac{-1}{j\omega C_G} & R_G+j\omega L_G+\frac{-1}{j\omega C_G} \\ R_G+j\omega L_G+\frac{-1}{j\omega C_G} & R_D+R_G+j\omega L_G+L_D+\frac{-1}{j\omega C_D}+\frac{-1}{j\omega C_G} \end{bmatrix}, \tag{7}$$

$$\begin{bmatrix} R_S+R_G & R_G \\ R_G & R_D+R_G \end{bmatrix} = \begin{bmatrix} realZ_{11} & realZ_{12} \\ realZ_{21} & realZ_{21} \end{bmatrix}, \tag{8}$$

$$\begin{bmatrix} j\omega(L_S+L_G)+\frac{-1}{j\omega C_S}+\frac{-1}{j\omega C_G} & j\omega L_G+\frac{-1}{j\omega C_G} \\ j\omega L_G+\frac{-1}{j\omega C_G} & j\omega L_G+L_D+\frac{-1}{j\omega C_D}+\frac{-1}{j\omega C_G} \end{bmatrix} = \begin{bmatrix} imagZ_{11} & imagZ_{12} \\ imagZ_{21} & imagZ_{21} \end{bmatrix}. \tag{9}$$

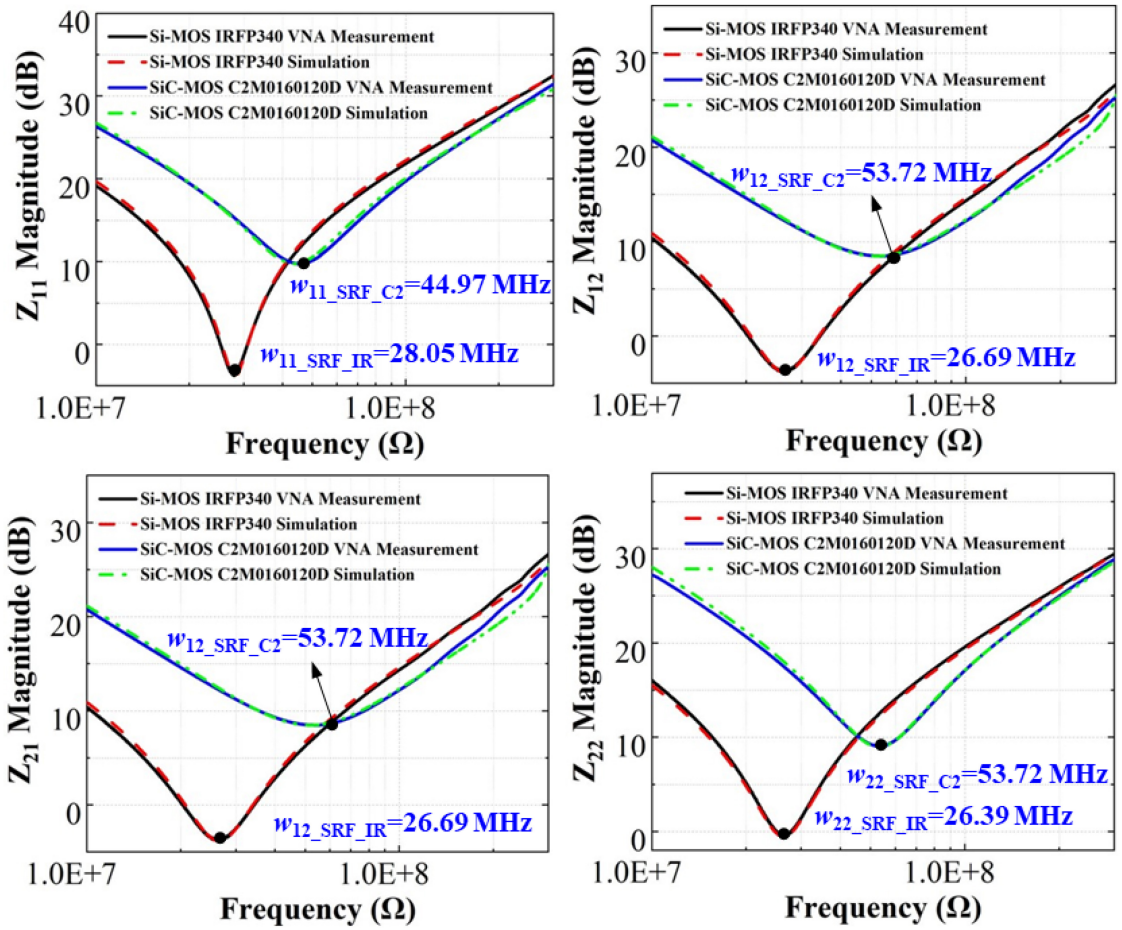


Fig. 5. Z-parameters obtained from VNA measurement and ADS simulation.

Consequently, the experimental results demonstrate that the proposed two-port network extraction approach is suitable for characterizing the parasitic parameters of the discrete MOSFET.

B. Aging Estimation With Parasitic Resistance

Prolonged exposure to high temperatures can lead to degradation of the oxide layer, aluminum pad, solder layer, and bond wires of the MOSFET due to various factors, such as electrical and thermal-mechanical stress. This degradation, which includes oxide deterioration, aluminum pad metallization reconstruction, solder layer lamination, and bond wire failure, increases $R_{DS(on)}$ [6], [28], [29], [30]. Therefore, $R_{DS(on)}$ is considered to be an important aging indicator in power MOSFETs. The block diagram of the accelerated aging setup is presented in Fig. 6. The acceleration of MOSFET degradation is achieved by controlling the chip junction temperature (T_j). However, the chip is encapsulated in epoxy molding compound (EMC), which hinders direct measurement of T_j. For TO-247 packaged MOSFETs, heat primarily dissipates through the thermal path of "chip-solder layer-Cu baseplate," with the Cu baseplate temperature closest to the chip junction temperature. A 3D model is established based on the physical structure of the MOSFET and imported into the Ansys-Icepak for simulation. According to the aging experiment, the simulation boundary conditions are set as follows: 1) Chip power dissipation $P_{chip} = 3.6$ W, 2) Ambient temperature $T_{chamber} = 100$ °C, and 3) Natural convection heat transfer. The simulation results in Fig. 6 show that, compared with the surface temperature of the EMC ($T_{EMC} = 209$ °C), the temperature of point A on the baseplate ($T_A = 217$ °C) is closer to the chip junction temperature ($T_j = 220$ °C). Therefore, point A on the surface of the exposed baseplate in the environment is selected as the temperature collection point, and T_j is reflected by measuring T_A. This approach facilitates real-time monitoring and feedback control of aging degradation temperature and $R_{DS(on)}$ measurement temperature.

The MOSFETs, namely, IRFP340 Si-MOSFET and C2M0160120D SiC-MOSFET, are placed in a temperature chamber to undergo accelerated aging tests. A k-type thermocouple is attached to the testing point A on the surface of the MOSFET baseplate to monitor the temperature during the aging procedure. The schematics of the $R_{DS(on)}$ test system and the two-port network S-parameter test system are depicted in Fig. 7. The extraction conditions for $R_{DS(on)}$ are based on the IRFP340 Si-MOSFET and C2M0160120D SiC-MOSFET device datasheets. For IRFP340, V_{GS} is set to 10 V, and I_D is selected to be 2.0 A. Meanwhile, for C2M0160120D, V_{GS} is set to 15 V, and I_D is selected to

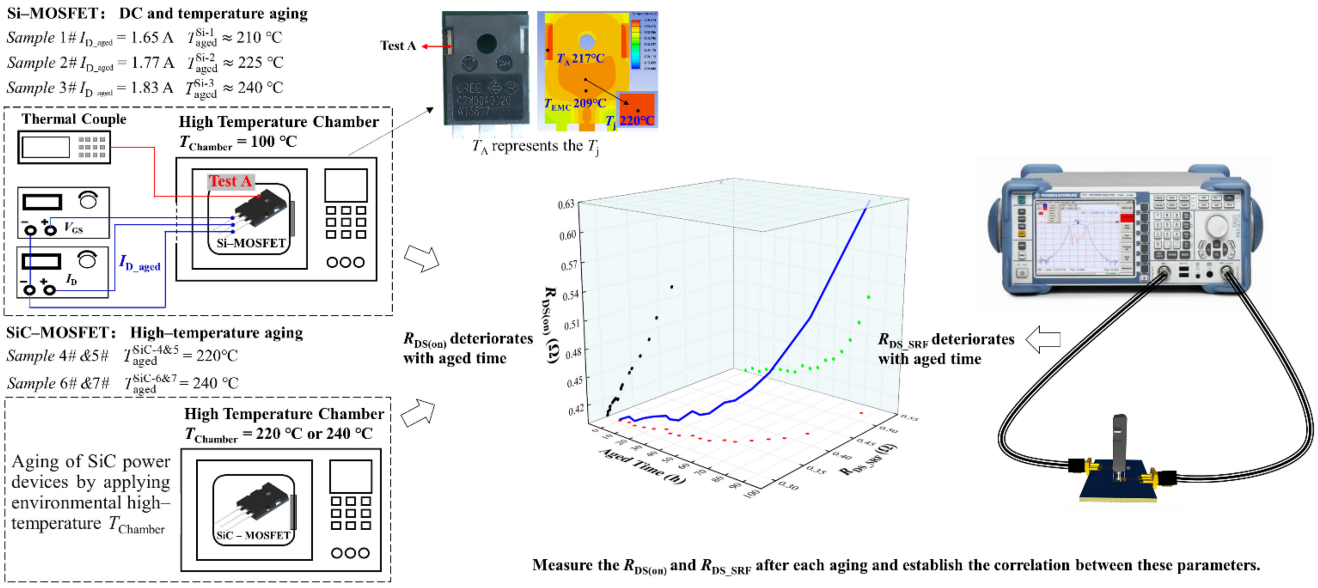


Fig. 6. Block diagram of an experimental scheme characterizing the correlation between $R_{DS(on)}$ and R_{DS_SRF} of Si-MOSFETs and SiC-MOSFETs after aging.

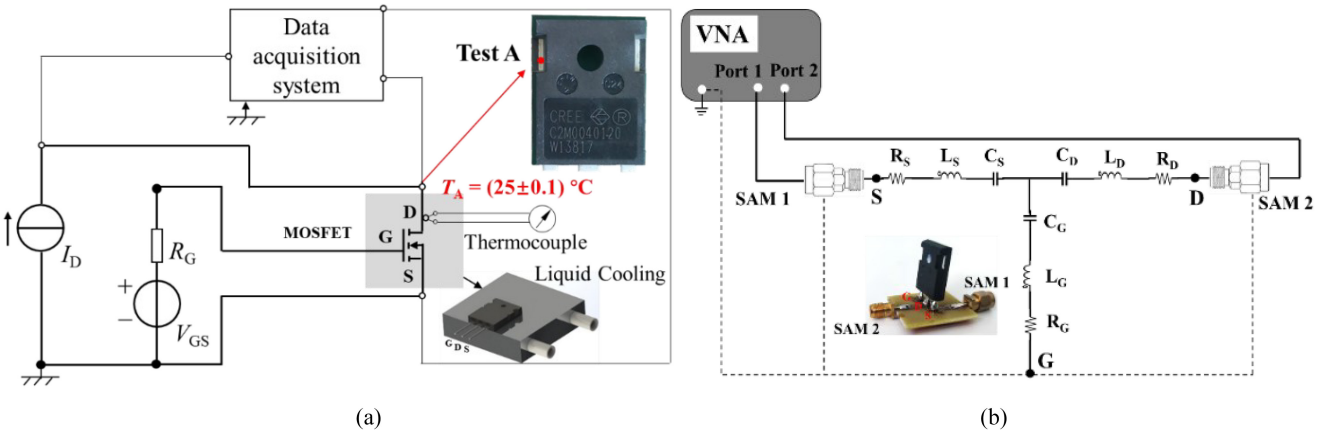


Fig. 7. Schematic of $R_{DS(on)}$ test system and two-port network S-parameter test system: (a) $R_{DS(on)}$ is measured by the data acquisition system under consistent measurement conditions, (b) Parasitic resistance R_{DS_SRF} is extracted from a two-port network measurement system.

be 3.0 A. According to the requirements of the datasheet provided by the packaging manufacturer, the $R_{DS(on)}$ value at 25 °C is determined as an indicator of device degradation. Using high-temperature thermal adhesive, the MOSFETs are affixed onto the heatsink of the liquid circulation cooling system. Power is applied to the MOSFET according to the set voltage and current test parameters. After a period of time, thermal equilibrium is reached by the MOSFET baseplate and chip. At this stage, the liquid cooling system is regulated by collecting temperature feedback from test point A to ensure that the junction temperature of the MOSFET remains stable at (25±0.1) °C during the $R_{DS(on)}$ extraction process. $R_{DS(on)}$ is calculated using V_{DS} and I_D, with $R_{DS(on)} = V_{DS} / I_D$. The failure threshold for power MOSFETs is a 25% increase in $R_{DS(ON)}$. It is calculated as the ratio of the change in $R_{DS(ON)}$ to the initial $R_{DS(ON)}$, which serves as an indicator of failure degradation [17].

The IRFP340 Si-MOSFET is placed in a temperature chamber at 100 °C. An effective V_{GS} ($V_{GS} > V_{GS(TH)}$) is applied across the G-S terminals to turn on the MOSFET completely. A constant I_{D_aged} is applied across the D–S terminals to generate the desired power stress for accelerating device degradation. Three different aging currents, I_{D_aged} (1.65 A, 1.77 A, and 1.83 A), are applied to the Si-MOSFETs (samples M1, M2, and M3) to generate different sustained thermal stresses ($T_{aged}^{Si-1} \approx (210\pm2)$ °C, ($T_{aged}^{Si-2} \approx (225\pm3)$ °C, and ($T_{aged}^{Si-3} \approx (240\pm3)$ °C). The $R_{DS(on)}$ and S-parameters of aged Si-MOSFETs are measured every 5 h.

SiC-MOSFET requires a thinner gate oxide layer than Si-MOSFET to achieve a reasonable threshold voltage. Applying a gate bias voltage of approximately 20 V results in an intrinsic electric field of 5 MV/cm in the SiO_2 layer of SiC-MOSFET. Under the same conditions, the intrinsic electric field of Si-MOSFET is only 3MV/cm. Therefore, the SiC-MOSFET is

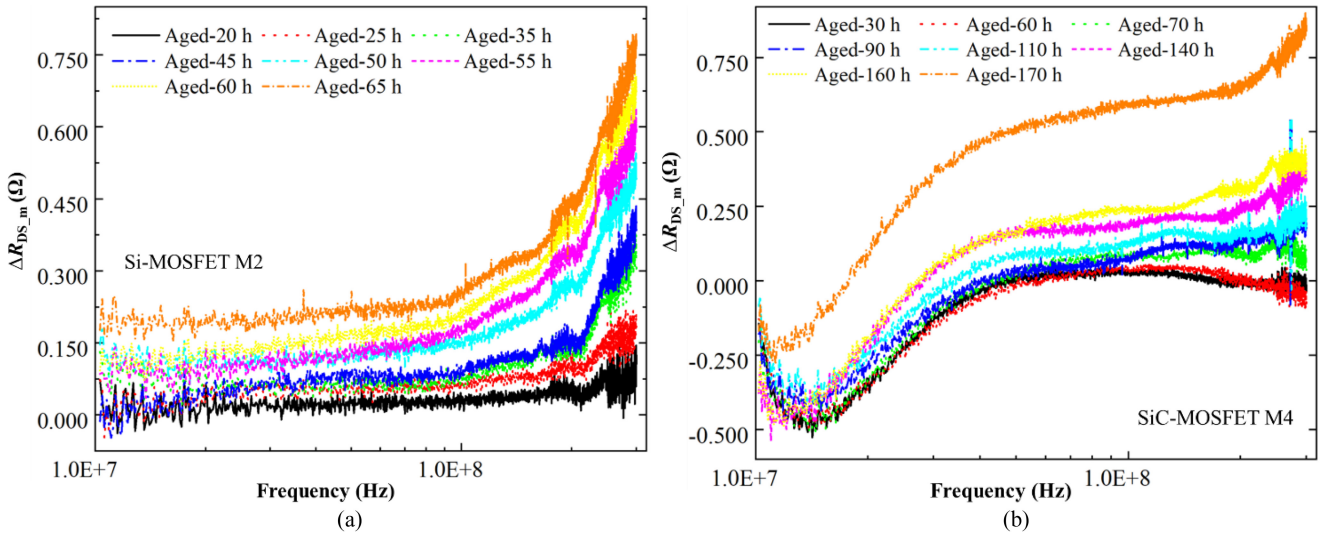


Fig. 8. Curves of ΔR_{DS_m} within the frequency domain measurement range after different aging times: (a) IRFP340 Si-MOSFET M2, (b) C2M0160120D SiC-MOSFET M4.

more prone to time-dependent dielectric breakdown under gate bias states, especially in high-temperature environments. No gate bias voltage is applied during the aging of SiC MOSFETs as a preventive measure; instead, only thermal stress is utilized. For C2M0160120D SiC-MOSFETs, samples M4 and M5 are aged in a temperature chamber at 220 °C, and samples M6 and M7 are aged in a temperature chamber at 240 °C. The $R_{DS(on)}$ and S-parameter of aged SiC-MOSFETs are measured every 10 h. To visually observe the changes in source-drain parasitic resistances R_{DS} within the measurement frequency range of 10–300 MHz, (8) can be reformulated into the following form:

$$R_{DS} = R_S + R_D = real(Z_{11}) + real(Z_{22}) - real(Z_{12})real(Z_{21}), \quad (10)$$

$$\Delta R_{DS\_m} = R_{DS\_m} - R_{DS\_0}. \quad (11)$$

where m is the cumulative aged time; R_{DS_m} is the aged source-drain parasitic resistance of the MOSFET after aging for m hours; R_{DS_0} is the initial drain-source parasitic resistance of the MOSFET before aging; and ΔR_{DS_m} is the difference between R_{DS_m} and R_{DS_0}.

Si-MOSFET M2 and SiC-MOSFET M4 samples, which exhibit significant degradation in $R_{DS(on)}$ over aging times, are selected for analysis. The frequency domain impedance values of these devices are extracted after different aging times. After 20 h of cumulative thermal-electrical stress aging, the $R_{DS(on)}$ of M2 shows degradation. When the cumulative aging time reaches 65 h, the $R_{DS(on)}$ increases from the initial 0.3982 Ω to 0.5944 Ω, which represents an increase of nearly 50%. Therefore, the ΔR_{DS_m} of M2 is calculated at each frequency point after aging for 20, 25, 35, 45, 50, 55, 60, and 65 h. Notably, ΔR_{DS_m} calculations for 30 and 40 h of aging are not performed given that $R_{DS(on)}$ insignificantly increased compared with 25 and 35 h of aging. Fig. 8(a) illustrates the ΔR_{DS_m} curves of M3 after different aging times. The $R_{DS(on)}$ of SiC-MOSFETs is 0.150 Ω, which is only 1/3 of the $R_{DS(on)}$ of IRFP340 Si-MOSFETs. Consequently, a change of less than 10 mΩ occurs under the same degree of degradation. Moreover, the increase in $R_{DS(on)}$ caused by passive aging degradation under a single constant environmental thermal stress is slow. Data analysis is based on the $R_{DS(on)}$ increment of more than 10 mΩ after each aging, and the Z-parameters of M4 are extracted after aging for 60, 70, 90, 110, 140, 160, and 170 h to calculate ΔR_{DS_m}. Fig. 8(b) shows the ΔR_{DS_m} curves of M4 after different aging times. With the degradation of Si-MOSFET and SiC-MOSFET (increase in $R_{DS(on)}$), ΔR_{DS_m} demonstrates a consistent growth trend with the degree of device degradation in the frequency domain. Although the ΔR_{DS_m} curves at each measurement frequency point are calculated using the real part of the Z-parameters and Equations (10) and (11), the process inherently encompasses measurement and computation errors (e.g., from S-parameters converted to Z-parameters). As a consequence of these errors, "±system noise" is introduced. Noise is inevitably superimposed during the computation of ΔR_{DS_m}, which leads to significant fluctuations in ΔR_{DS_m} at each frequency point, as observed in Figures 8a and 8b. Simultaneously, effectively isolating the impact of parasitic capacitance and inductance within the MOSFET in the measurement frequency domain presents a considerable challenge. The parasitic resistance frequency curve cannot be used to quantify device aging due to the noise interference stemming from various errors. Furthermore, differences in device structure, physical dimensions, packaging design, manufacturing processes, and substrate materials between Si and SiC MOSFETs result in variations in measurement outcomes and noise. These variations lead to discrepancies in the frequency response of ΔR_{DS_m}. Nevertheless, the frequency curves of ΔR_{DS_m} in Figures 8a and 8b demonstrate a positive correlation with the degree of degradation (represented by $R_{DS(on)}$), which indicates that thermal stress aging causes an increase in the parasitic resistance of the MOSFET. Therefore, power device degradation can be forecasted based on the specific value analysis of R_{DS}. The drain-source parasitic resistance at the

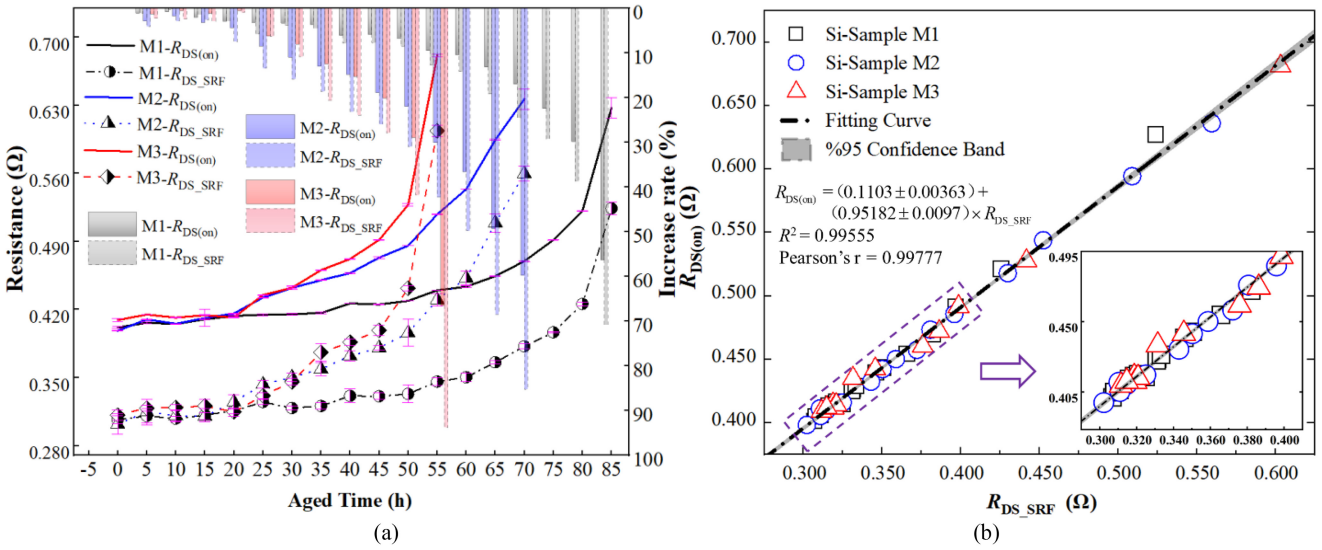


Fig. 9. Aging test results for Si-MOSFETs: (a) Measured $R_{DS(on)}$ and R_{DS_SRF} at different aging times. (b) Relationship between $R_{DS(on)}$ and R_{DS_SRF}.

f_{SRF} (R_{DS_SRF}) is proposed to construct a numerical model between the two parameters for quantifying the correlation between R_{DS} and $R_{DS(on)}$. The magnitude of Z-parameter is equal to the modulus of the real and imaginary parts of the Z-parameter. Therefore, using the magnitude for calculations can avoid the superimposition of "±system noise." In the *RLC* equivalent circuit of the MOSFET, the capacitive reactance caused by parasitic capacitance and the inductive reactance caused by parasitic resistance are completely canceled out at the f_{SRF}, which results in the characteristics of a pure resistance circuit. Consequently, at the f_{SRF}, Z_{SRF} is minimized, with a phase angle of 0°. Z_{11_SRF}, Z_{12_SRF}, Z_{21_SRF}, and Z_{22_SRF} are respectively equal to R_{SG_SRF}, R_{G_SRF}, R_{G_SRF}, and R_{DG_SRF}. R_{DS_SRF} can be extracted from (12)–(13). where R_{SG_SRF}, R_{DG_SRF}, R_{S_SRF}, R_{G_SRF}, and R_{D_SRF} respectively represent the source-gate parasitic resistance at the f_{SRF}, the drain-gate parasitic resistance at the f_{SRF}, the source parasitic resistance at the f_{SRF}, the gate parasitic resistance at the f_{SRF}, and the drain parasitic resistance at the f_{SRF}.

$$\begin{bmatrix} R_{S\_SRF}+R_{G\_SRF} & R_{G\_SRF} \\ R_{G\_SRF} & R_{D\_SRF}+R_{G\_SRF} \end{bmatrix} = \begin{bmatrix} Z_{11\_SRF} & Z_{12\_SRF} \\ Z_{21\_SRF} & Z_{21\_SRF} \end{bmatrix}, \quad (12)$$

$$R_{DS\_SRF} = Z_{11\_SRF} + Z_{22\_SRF} - Z_{12\_SRF} - Z_{21\_SRF}. \quad (13)$$

Materials or devices usually demonstrate considerable stability for a certain period before undergoing relatively rapid degradation over time. As a result, the degradation process of $R_{DS(on)}$ is divided into two stages: the delay stage (or linear stage) and the degradation stage (or nonlinear stage) [31]. In the delay stage, $R_{DS(on)}$ shows minimal change, and the MOSFET maintains stable performance. In the degradation stage, internal material damage leads to an accelerated increase in $R_{DS(on)}$ over time, which accounts for the majority of the lifetime consumption. Figures 9(a) and 10(a) illustrate the degradation curves of R_{DS_SRF} and $R_{DS(on)}$ over aging time for Si-MOSFET (M1, M2, M3) and SiC-MOSFET, respectively. The degradation of Si-MOSFETs accelerates with increased thermal and electrical stress. After 20 h of aging for M2 and M3, and 50 h of aging for M1, the $R_{DS(on)}$ has accumulated by approximately 25 mΩ compared with the pre-aging value. The change rate is about 8%, which implies that the MOSFETs have entered the degradation stage. Furthermore, after 70 h of aging for M1, 45 h for M2, and 35 h for M3, the increase in $R_{DS(on)}$ exceeds 15 mΩ within each aging interval. This condition implies significant degradation of MOSFETs. Observations show that $R_{DS(on)}$ and R_{DS_SRF} exhibit a similar positive correlation with the degree of MOSFET degradation. Fig. 9(b) is plotted using data from M1, M2, and M3, where "a" and "b" represent $R_{DS(on)}$ and R_{DS_SRF}, respectively. This relationship can be quantified, as shown in (14), using the basic fitting tool in MATLAB, where $R_{DS(on)}$ and R_{DS_SRF} exhibit a quasi-linear relationship. Equation (14) is the fitting result at a 95% confidence level, with a fitting R^2 of 0.99555 and a Pearson correlation coefficient of 0.99777, which indicates a very strong linear correlation. After the R_{DS_SRF} is extracted, the predicted $R_{DS(on)}$ after accelerated aging can be easily determined using the extracted R_{DS_SRF} and (14).

$$\begin{aligned} R_{DS(on)} &= (0.1103 \pm 0.00363) \\ &\quad + (0.95182 \pm 0.0097) \times R_{DS\_SRF} \\ R^2 &= 0.99555. \end{aligned} \quad (14)$$

For SiC-MOSFETs M4, M5, and M6, a degradation trend similar to that of Si-MOSFETs is observed. However, given that only stable thermal stress is applied, the degradation of SiC-MOSFETs occurs at a slower rate. At a thermal stress of 220 °C, M4 and M5 enter the degradation stage after aging for 60 and 70 h, respectively. Under a thermal stress of 240 °C, M6 and M7 reach the degradation stage after aging for 30 and 40 h, respectively. When M4 has aged for 140 h, M5 for 110 h, M6 for 90 h, and M7 for 90 h, the increase in $R_{DS(on)}$ for each aging interval exceeds 25 mΩ, which indicates rapid degradation of SiC-MOSFETs. Fig. 10(b) is plotted using data from M4, M5, M6, and M7. Equation (15) is fitted to describe the relationship between $R_{DS(on)}$ and R_{DS_SRF}, with a fitting R^2 of 0.9809 and a Pearson correlation coefficient of 0.99042,

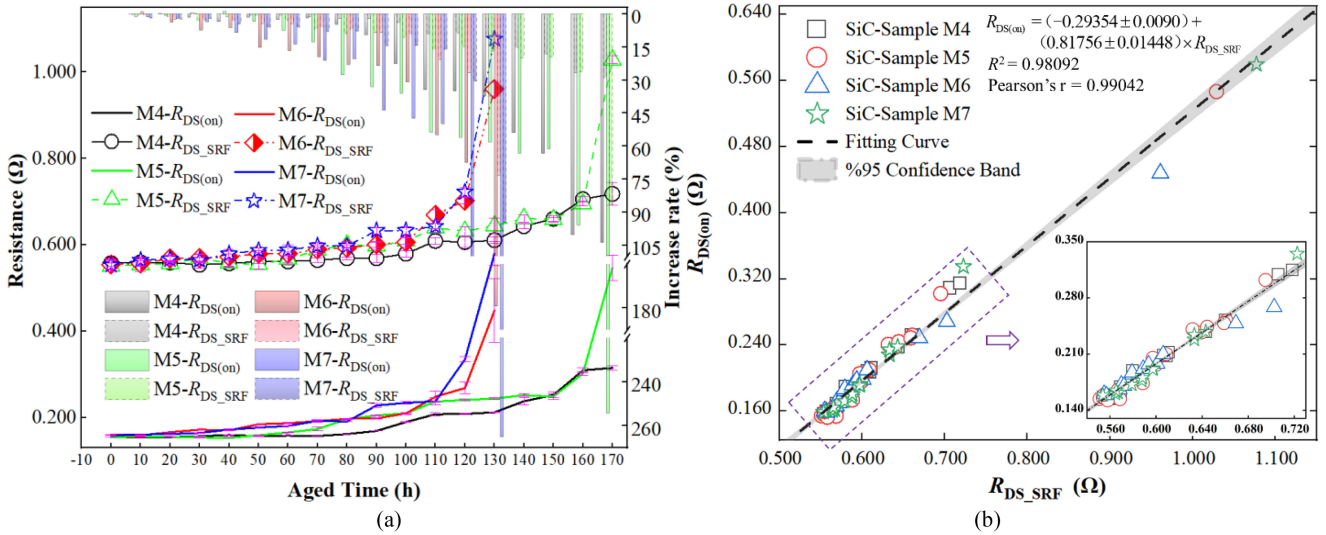


Fig. 10. Aging test results for SiC-MOSFETs: (a) Measured $R_{DS(on)}$ and R_{DS_SRF} at different aging times. (b) Relationship between $R_{DS(on)}$ and R_{DS_SRF}.

TABLE I
COMPARISON OF THE DEGRADATION PRECURSOR PARAMETERS AND FDR APPROACH

Precursor	Sensitivity with a slight fault	Sensitivity with V_{GS} or I_D	Sensitivity with T_j	Sensitivity with frequency	Sensitivity with impedance matching	Application
$R_{DS(on)}$ [6]	High	High	Middle	/	No mention	On-line
$V_{GE(th)}$ [4],[5]	Low	High	Low	/	No mention	On-line
t_{off} [11]	High	No mention	High	Low: sweep-frequency	High	On-line
SSTDR-amplitude [16], [17]	Middle	Middle	No mention	High: single-frequency	Middle	On-line
FDR-parasitic resistance	High	/: under zero bias, without V_{GS} or I_D	Low: under zero bias, without power loss	Low: sweep-frequency	High	Off-line

which shows a quasi-linear positive correlation resembling that of Si-MOSFET.

$$R_{DS(on)} = (-0.29354 \pm 0.0090) + (0.81756 \pm 0.01448) \times R_{DS\_SRF} \quad R^2 = 0.98092. \tag{15}$$

The experimental results confirm that thermal stress can induce the physical degradation of power MOSFETs, which concurrently increases $R_{DS(on)}$ and R_{DS_SRF}. $R_{DS(on)}$ is extracted within a DC circuit. Initially, the MOSFET must be biased into conduction, followed by the calculation of the drain-source voltage V_{DS} and I_D under a T_j of 25 °C. The water-cooling system needs to be adjusted to ensure the stability of the junction temperature of the chip throughout the measurement process. Consistency in the biasing voltage V_{GS} and I_D settings must be maintained for each measurement iteration. The integration of the water-cooling system and external testing circuit significantly amplifies the complexity. By contrast, R_{DS_SRF} represents an alternating current impedance parameter that can be measured under zero bias conditions using a VNA. Comparatively, the extraction process for R_{DS_SRF} is notably simpler than that of $R_{DS(on)}$. After R_{DS_SRF} is obtained, it can be directly applied to established empirical formulas, such as (14) and (15), to swiftly compute the $R_{DS(on)}$ of the MOSFET. This process facilitates a rapid assessment of the quality level of the MOSFET.

The methods based on degradation precursors have been widely used in the detection of power device degradation, all of which have demonstrated their unique advantages. Table I summarizes the differences among the precursor parameters $R_{DS(on)}$, $V_{GE(th)}$, t_{off}, SSTDR-amplitude, and the FDR approach. In contrast to electrical parameters as degradation precursors, parasitic resistance can be directly extracted by a two-port network measurement under zero bias conditions. This possibility eliminates the need for additional external test circuits (V_{GS}, I_D) and conveniently regulates the chip junction temperature. However, frequency domain measurement has high sensitivity to impedance matching, which requires consistent impedance along the transmission path. This approach places high demands on the test-fixture and is currently only suitable for offline measurement. Nevertheless, the FDR approach is well suited for the rapid quality screening of power devices, which indicates promising application prospects.

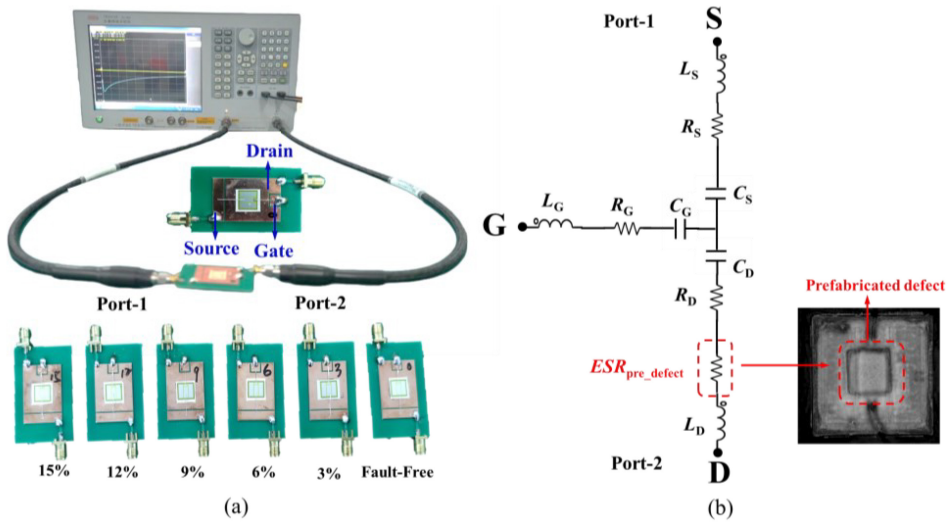
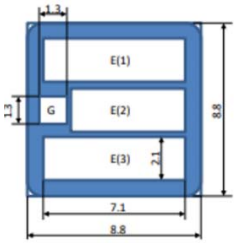
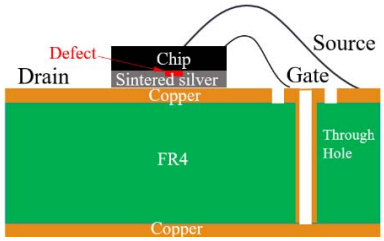


Fig. 11. Proposed FDR approach extracts the parasitic parameter of prefabricated defect MOSFETs: (a) Two-port network measurement setup and prefabricated defect samples, (b) MOSFET small-signal equivalent circuit with sintered layer prefabricated defects.

TABLE II
PREFABRICATED DEFECT MODELS AND DEFECT SIZES

Chip (mm) $L \times W \times H$	Sintered layer (mm) $L \times W \times H$	Proportion of prefabricated defect area	Prefabricated defect	
			Size (mm) $L \times W$	Photo
8.8 × 8.8 ×·0.14	8.8·× 8.8·× 0.07	0%		
		3%	1.5 × 1.5	
		6%	2.2 × 2.2	
		9%	2.6 ×·2.6	
		12%	3.0·× 3.0	
		15%	3.4·× 3.4	

C. Sintered Layer Defect Identification With Parasitic Resistance

Nanosilver is used in the packaging of third-generation semiconductor SiC-MOSFET chips as a replacement to traditional tin solder due to its excellent thermal conductivity and heat resistance. However, the interconnection layer formed after nanosilver sintering adopts a porous structure, and completely evaporating the organic components in the nanoparticles is challenging. Therefore, significant defects may arise between the silver interconnection layer formed by pressureless sintering and the SiC chip. C-SAM and X-ray equipment are typically used to directly observe the interconnection quality of the sintering interface. However, interactive verification of C-SAM and X-ray images is required to characterize defects, which results in low detection efficiency. Another evaluation approach involves push-cut testing, which requires strict control over the initial position of the push-cut point on the chip. However, the push-cut test is destructive and cannot be repeatedly demonstrated. The proposed FDR approach is introduced for the detection of sintered silver quality. Sintered silver layer samples with different degradation degrees are obtained by pre-embedding defects of different sizes in silver nanoparticle paste. Insulating tape of predetermined dimensions is pasted onto the substrate, and a nanosilver layer is created through silk screen printing. After the tape is removed, a predetermined region with air defects is introduced within the nanosilver layer. Under sintering conditions at approximately 250 °C, nanosilver undergoes solid-state diffusion between particles, which is influenced by surface energy. This process ultimately produces a sintered silver layer specimen characterized by voids of varying dimensions. They are designed as squares to facilitate the calculation of defect side length dimensions. The defect area is determined based on a specific ratio to the drain-pad area of the chip. The prefabricated defect model and dimensions (length × width) are shown in Table II.

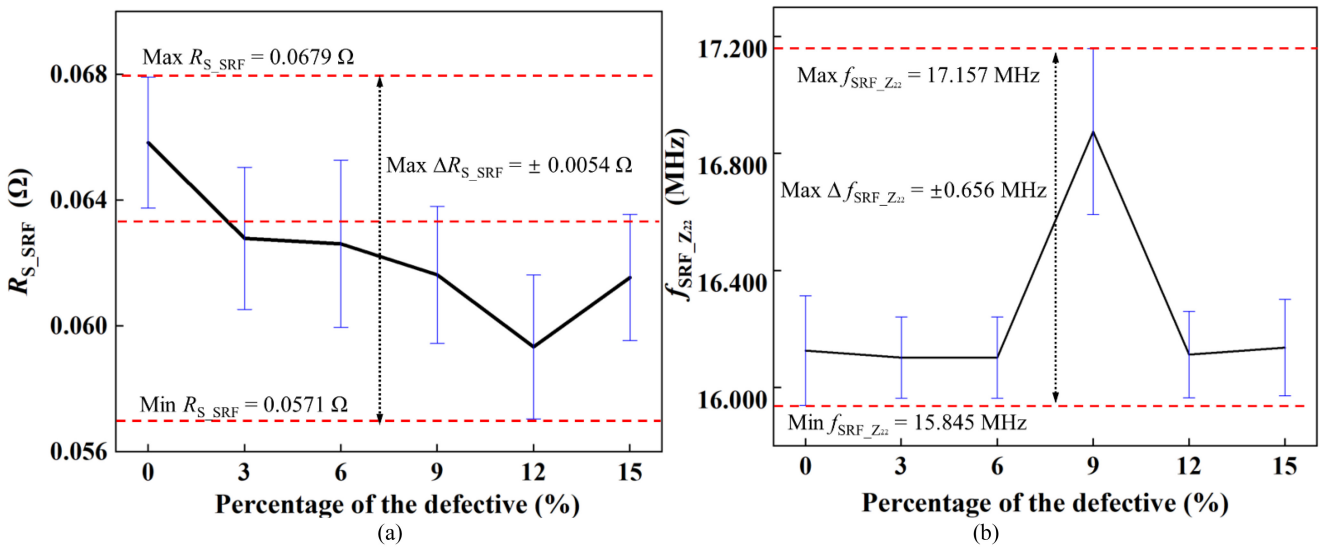


Fig. 12. Extracted R_{S_SRF} and $f_{SRF\_Z_{22}}$ from MOSFETs with different sintered silver layer defects: (a) R_{S_SRF}, (b) $f_{SRF\_Z_{22}}$.

Fig. 11 presents the experimental setup for a discrete power MOSFET containing prefabricated defects in the sintered layer. A simplified equivalent circuit is established. The degradation of the sintered layer in the circuit can be modeled as an additional series resistance, which is denoted as ESR_{pre_defect}, located within the drain region. Theoretically, these defects contribute to an increase in the parasitic resistance of the MOSFET drain while exerting minimal influence on the source and gate. The values of R_{S_SRF}, $f_{SRF\_Z_{22}}$, and R_{D_SRF} for MOSFETs with prefabricated defects of varying sizes are illustrated in Fig. 12 and Table III, respectively. Each sample is measured 10 times, and the average value is utilized for data analysis. The results indicate that the maximum and minimum differences between R_{S_SRF} and $f_{SRF\_Z_{22}}$ are 0.010 Ω and 1.312 MHz, respectively. Given disparities in the size and position of bond wires for each MOSFET source and gate, as well as unavoidable measurement errors in VNA measurements, there is no numerical correlation between the R_{S_SRF}, $f_{SRF\_Z_{22}}$, and defects. f_{SRF} is determined by C and L. Therefore, the slightly higher $f_{SRF\_Z_{22}}$ value exhibited by the sample with a 9% prefabricated defect ratio should mainly be attributed to the inherent parasitic capacitance difference of the MOSFET.

Table III shows the R_{D_SRF} values of MOSFETs, which reveal an increasing trend as the defect area expands. For MOSFETs with prefabricated defect ratios of 3%, 6%, 9%, 12%, and 15%, the R_{D_SRF} values are 1.89, 1.97, 1.91, 1.92, and 1.92 Ω, respectively. The values are 0.038, 0.120, 0.057, 0.065, and 0.066 Ω higher than those of the R_{D_SRF} values of a fault-free MOSFET. The difference in the maximum and minimum R_{D_SRF} values reaches 0.16 Ω, which indicates that the presence of defects leads to an increase in parasitic resistance within the drain region. The smallest R_{D_SRF} value occurs in MOSFETs without prefabricated defects, while the maximum R_{D_SRF} appears when the defect area comprises 6% of the sintered layer area. This observation is inconsistent with our theoretical prediction, which is potentially due to discrepancies between the actual defects formed after sintering and the pre-designed defects. We employ C-SAM and X-ray imaging to observe the actual defect morphology at the sintered silver layer interface after sintering for further investigation. Numerical calculations performed on these images reveal that MOSFETs with prefabricated defect ratios of 0%, 3%, 9%, 12%, and 15% exhibit actual defect ratios of 0%, 5.45%, 8.95%, 12.26%, and 13.85% after sintering, respectively. However, X-ray imaging shows that the MOSFET sample with a 6% prefabricated defect ratio exhibits notable highlights between the die and the sintered layer after sintering, which indicates low density and severe soldering defects in the area. Further observation using C-SAM reveals significant delamination at the interface where the prefabricated defects are located between the die and sintered layer. Therefore, the MOSFET with a 6% prefabricated defect ratio exhibits the highest R_{D_SRF} after sintering compared with other defect models. This finding demonstrates the effectiveness of the proposed drain parasitic resistance R_{D_SRF} for predicting the quality of the sintered layer.

The mechanism behind this observation is illustrated in Fig. 13. During defect prefabrication, oxygen is introduced between the die and silver nanoparticles but cannot be entirely discharged during the sintering process. This phenomenon results in oxidation of the die-pad at the defect location, which increases R_{D_SRF}. The defects can cause substantial delamination between the die and the sintered silver layer. Notably, a 5.45% minor defect can be detected compared with a fault-free sintered silver sample. This observation implies that the proposed detection approach can be employed for nondestructive testing of sintered silver layer quality and accurately estimate the severity of defects. It is suitable for rapid quality screening of sintered layers.

IV. Conclusion

This study proposes a novel approach for detecting MOSFET degradation using the FDR method. This technique is validated through aging tests on Si-MOSFET and

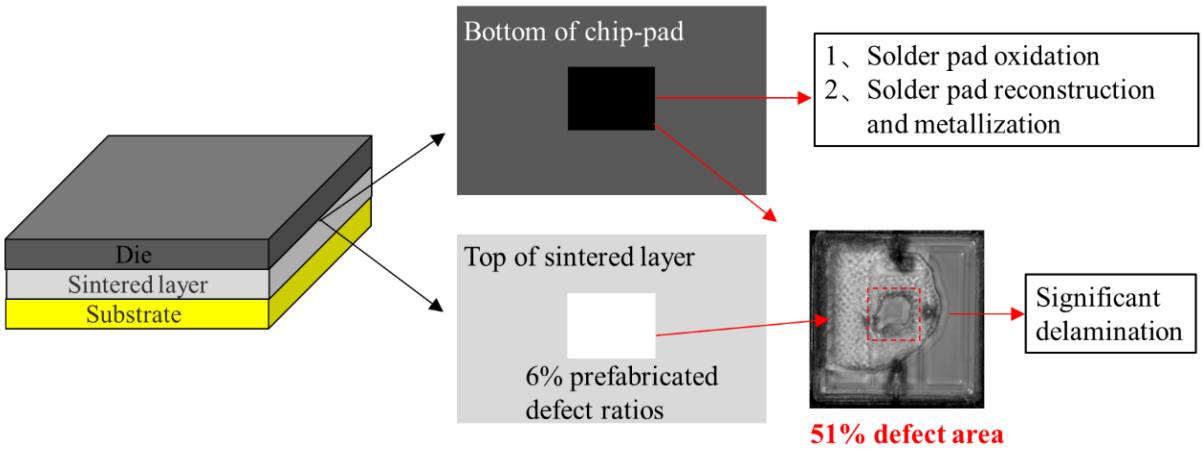
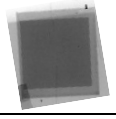
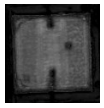
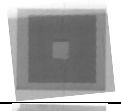
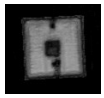
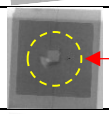
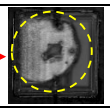
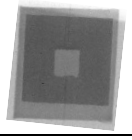
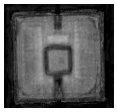
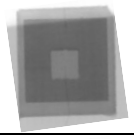
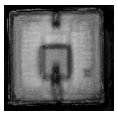
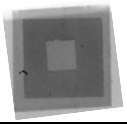
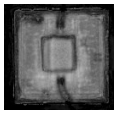


Fig. 13. Schematic of the increase in R_{D_SRF} caused by defects.

TABLE III
RD_SRF, C-SAM, AND X-RAY IMAGES OF DEFECT SAMPLES IN THE SINTERED SILVER LAYER

Proportion of prefabricated defect area	Actual defect ratio	R_{D_SRF} Ω	Max ΔR_{D_SRF} Ω	C-SAM	X-ray
0%	0%	1.85±0.02	±0.08		
3%	5.45%	1.89±0.01			
6%	51.74%	1.97±0.01			
9%	8.95%	1.91±0.01			
12%	12.26%	1.92±0.01			
15%	13.85%	1.92±0.02			

SiC-MOSFET devices, as well as experiments involving prefabricated defects in sintered silver. The accelerated aging experiments illustrate that R_{DS_SRF} increases in correlation with the degree of aging degradation and exhibits a quasi-linear positive correlation with $R_{DS(on)}$. Formulas (14) and (15) are derived to express this relationship, which enables the swift prediction of device degradation. Furthermore, an experiment involving prefabricated defects reveals that defects can lead to an increase in R_{D_SRF}. The identification of the MOSFET with the highest R_{D_SRF} value, which corresponds to a sample with a prefabricated defect ratio of 6% before sintering, confirms severe degradation in the quality of its silver sintered layer. This identification is verified through C-SAM images. The approach avoids the need to turn on the MOSFET, which prevents T_j fluctuations due to chip self-heating. Moreover, it eliminates the necessity for additional hardware circuits. Thus, the method is a potentially efficient solution for quality screening of power devices.

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