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A Thin and Low-Inductance 1200 V SiC MOSFET Fan-Out Panel-Level Packaging With Thermal Cycling Reliability Evaluation

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***Abstract*— SiC MOSFET is mainly characterized by the higher electric breakdown field, higher thermal conductivity, and lower switching loss enabling high breakdown voltage, high-temperature operation, and high switching frequency. However, their performances are considerably limited by the high parasitic inductance and poor heat dissipation capabilities associated with existing wire-bonding packaging methods. To address this challenge, a 1200 V/136 A fan-out panel-level packaging (FOPLP) SiC MOSFET with a size of 8 × 8 × 0.75 mm was proposed. The electrical parameters of the devices were characterized experimentally. Both the static and dynamic parameters of the package matched the bare die values, which confirmed the functioning of the proposed packaging method for SiC MOSFET. The package parasitic inductance, thermal resistance, and soldering stress were analyzed through simulations. The reliability of the packages was evaluated by performing the thermal cycling test. The experimental results revealed that: 1) SiC MOSFET FOPLP had 0.36 nH drain–source parasitic inductance at 100 kHz, a 96% reduction compared with a conventional wire-bonded package; 2) double-sided cooling enabled the packages to exhibit a thermal resistance as low as 0.55 °C/W; and 3) after 2000 thermal cycling cycles, drain–source ON-state resistance [$R_{DS(on)}$] increased by less than 2%, which revealed the higher reliability of the package under thermal cycling.**

***Index Terms*— Fan-out panel-level packaging (FOPLP), parasitic inductance, SiC MOSFET, thermal cycling, thermal resistance.**

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I. Introduction

SILICON carbide (SiC), as one of the wide bandgap semiconductors, exhibits a high intrinsic breakdown field and thermal conductivity. Furthermore, SiC MOSFET bare dies exhibit higher switching frequency, lower energy loss, and higher temperature resistance than those of Si-based MOSFETs [1], [2], [3], [4]. Generally, the bare die can be used in circuits to achieve the switching function only after packaging [5], [6]. High-quality packaging is essential for the accurate functioning and increased performance of SiC MOSFET bare dies. It ensures reliable electrical connections between the die and terminals, dissipates heat generated in the die, and provides mechanical robustness and protection for operation in harsh conditions. However, existing packaging for commercial SiC MOSFETs is based on wire-bonding packaging methods [6] that are typically developed for Si-semiconductor power devices, including both discrete transistor outline (TO) packages for the single die and a power module represented by parts stacking for multi-dies. The parasitic inductance of up to 10 nH was induced by the bonding wire [7], [8]. Because of the high *di/dt* in the high-frequency switching process, the voltage overshoot and voltage oscillation resulting from high parasitic inductance can cause an increasing electric energy loss, electromagnetic interference, and thermal breakdown of the die [9], [10]. Furthermore, the changes in the source voltage attributed to high source parasitic inductance considerably affect the driving voltage (gate–source voltage) of the device, which will cause errors in the switching state of the device [11]. The junction temperature for most commercial SiC- or

Si-based devices is both rated from 150 °C to 175 °C, and SiC die devices can function steadily at temperatures over 320 °C in theory [12]. Thus, a solder paste with low melting temperature used in the Si device was not suitable for the device [13]. To sum up, the SiC MOSFET package should satisfy the following requirements: 1) small packaging parasitic parameters to guarantee switching speed; 2) low package thermal resistance to facilitate rapid heat dissipation; 3) high-temperature package materials to enable the device to operate at high temperatures; and 4) high fatigue stress resistance to resist periodic temperature changes. Some of the advanced packages that have emerged so far for SiC MOSFET include wire-bondless interconnection packaging, press-pack packaging, 3-D packaging, and so on [14], [15]. A key objective of advanced packages is to reduce package parasitic parameters.

In conventional packaging, the die is soldered to copper lead frames or direct bond copper (DBC) substrates, and the gate and source are electrically connected to the terminals using bonding wires. Liang [16] proposed a wire-bondless SiC MOSFET with planar packaging, featuring a bare die sandwiched between two DBCs. Two heatsink pads were attached to these DBCs to allow double-side heat dissipation. To reduce mechanical stress caused by the rigid connection between the die and the DBC, a porous sintered silver interposer was introduced to the device. The interposer was positioned between the die and the DBC [17]. To overcome the mutual inductance between different current paths, Yang et al. [18] proposed a SiC MOSFET power module with an interleaved planar structure in which the currents of two adjacent die were in opposite directions. Another type of wire-bondless interconnection packaging is using a copper clip to replace the bonding wire [19], [20].

Fan-out panel-level packaging (FOPLP) facilitates device miniaturization. The redistribution layer (RDL) of this packaging method is critical to the electrical connection [21], [22], [23]. In a printed circuit board (PCB) embedded FOPLP, the bare die is first embedded into bismaleimide triazine (BT) laminate with almost the same thickness as the die. The gaps between BT and die were filled with photo imageable dielectric (PID) through exposure, development, and cure process. The RDL is subsequently fabricated through trepanning, copper deposition, and copper plating. Hou et al. [23] proposed a PCB-embedded FOPLP SiC MOSFET power module with laterally distributed dies. Regnat et al. [24] reported a similar packaging method but with dies distributed vertically. Fan et al. [25] proposed another, but facile FOPLP process where an epoxy molding compound (EMC) was used. In this process, first, the die was attached to the lead frame, then RDL was performed after molding. Shao et al. [26], [27] proposed single-die and dual-die MOSFETs with EMC-based FOPLP successively, realizing lower thermal resistance and ON-state resistance than wire-bonding structures. Due to the fewer and more convenient steps to finish die fixation, FOPLP using EMC exhibits lower costs and higher efficacy than PCB-embedded FOPLP.

Numerous studies have reported on novel SiC MOSFET packages and their initial electrical properties [14], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25]. However, the long-term reliability and robustness of packaging are key factors in applications [28], [29]. Because faults may generate after several years of application before causing device failure, accelerated lifetime tests (ALT) are performed to proactively verify the reliability of SiC MOSFET under various working conditions. Thermal cycling is a critical ALT reliability test in which periodic temperature stress is applied to the device under test to induce failures due to the mismatch coefficients of thermal expansion (CTE) between adjacent layers of the package [30], [31], [32]. Package failure modes during thermal cycling tests include die attachment layer voids and creaks and RDL peeling, which increased the $R_{DS(on)}$ value.

In this study, first, a SiC MOSFET with FOPLP was fabricated. Next, the performance and long-term reliability of the device were analyzed and performed in detail using both experimental and simulation methods. The remainder of this article is organized as follows. Section II introduces the SiC MOSFET FOPLP and details its packaging process. The analyses of parasitic inductance, thermal resistance, and mechanical performance are described in Section III. The initial electrical parameters and thermal cycling reliability of the package are discussed in Section IV. Finally, Section V provides concluding remarks.

II. FOPLP SiC MOSFET and Its Packaging Process

This section provides an overview of the structure and components of SiC MOSFET FOPLP followed by a detailed presentation of its packaging process.

A. Packaging Structure

The SiC MOSFET FOPLP is composed of mainly SiC MOSFET die, RDL, solder, solder pad, and molding as depicted in Fig. 1. In this study, we used SiC MOSFET die (S4601M) from ROHM semiconductor rated at 1200 V, 136 A, and 12 mΩ. The size of the SiC MOSFET die was 5 × 5 × 0.15 mm, the surface metallization of the gate and source pad contained Ni/Pd/Au, and the surface metallization of the drain contained Ti/Ni/Au. Sn5Sb solder paste was used as a die attachment material. The source and gate pads of the die were connected to corresponding solder pads through RDL. The top heatsink pad was embedded in an EMC. Thus, the heat generated in the die can be dissipated through the solder pads and top heatsink pad which results in a double-side cooling effect. The thermal and mechanical parameters of package components, including thermal conductivity (K), coefficient of thermal expansion (CTE), Young modulus (E), and Poisson's ratio (v), are listed in Table I.

B. Packaging Process

The SiC MOSFET FOPLP packaging process (see Fig. 2) is described as follows: 1) the lead frame was mounted on the

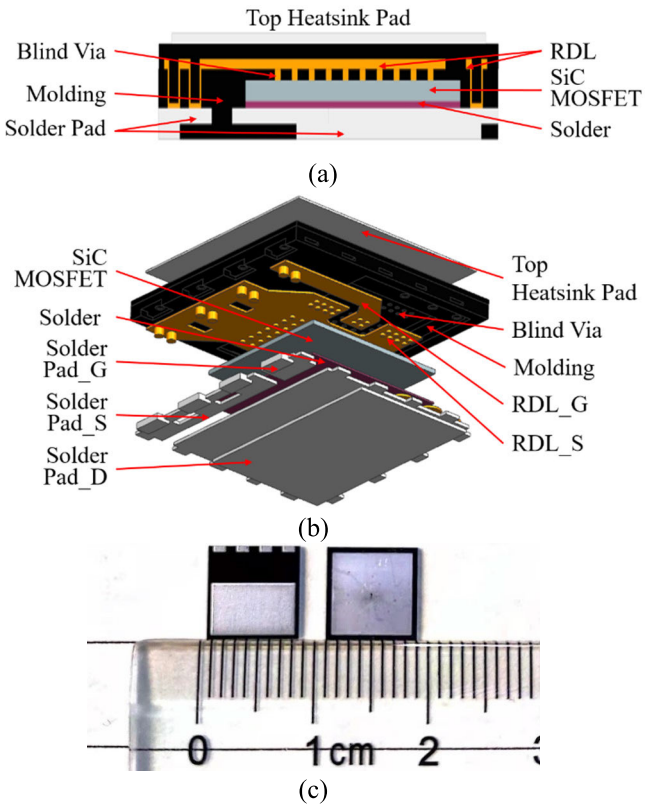

Fig. 1. SiC MOSFET FOPLP structure: (a) cross section view, (b) exploded view, and (c) photograph.

TABLE I
THERMAL AND MECHANICAL PARAMETERS OF PACKAGING MATERIALS

Component	Material	K (W/m·°C)	CTE (ppm/°C)	E (GPa)	v
RDL Solder Pad, Heatsink Pad	copper	401	18	110	0.34
SiC MOSFET die	SiC	58.6	5.1	400	0.14
Solder	Sn5Sb	70	31	49	0.38
Molding	EMC	1.5	9	15	0.38

carrier; 2) solder paste was used to solder the die to the lead frame; 3) the die was covered with EMC; 4) specific vias were prepared in EMC using laser drilling for RDL construction; 5) a copper plate of 8 μm thickness was deposited on the gate and source pads of the die, followed by filling the vias with copper using electroplating technique and forming a layer of copper on the EMC; 6) laser processing was performed to remove the extra copper layer; 7) the RDLs were encased in the EMC in the second molding process and then a top heatsink pad was mounted on the EMC; and 8) finally, the carrier was removed, and the solder pads were plated with nickel by chemical plating, which resulted in successful fabrication of an SiC MOSFET FOPLP with a dimension of 8 × 8 × 0.75 mm.

III. ELECTRICAL, THERMAL AND MECHANICAL SIMULATIONS AND ANALYSIS

Electro–thermo–mechanical analyses were performed using the simulation method to evaluate the electrical, thermal, and mechanical performances of SiC MOSFET FOPLP. First, the parasitic inductances of the package were extracted using the finite/boundary element (FBE) method in ANSYS Q3D. Next, the thermal resistances and soldering stresses were assessed using the finite element (FE) method in ANSYS Workbench.

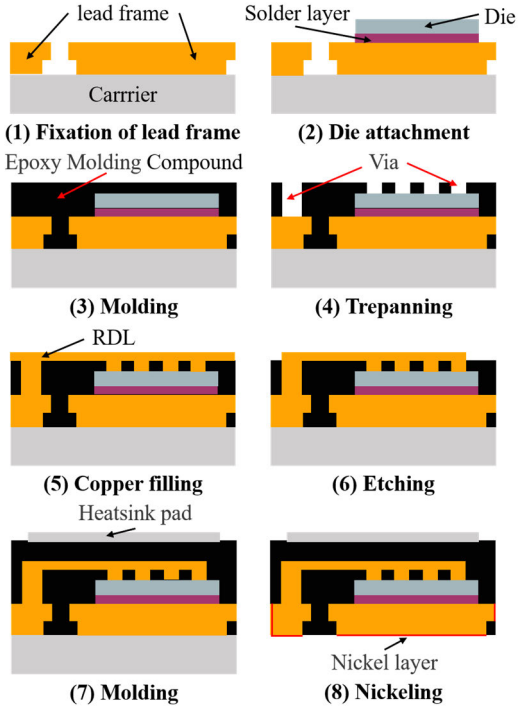

Fig. 2. Flowchart of SiC MOSFET FOPLP packaging process.

To compare with the developed SiC MOSFET FOPLP, three SiC MOSFETs were established with TO-247, TO leadless (TOLL) wire-bonding packaging, and PCB-embedded FOPLP wireless-bonding packaging. TO-247 is the most commonly used package mode in the past years, and TOLL with small size and small parasitic parameters is one of the state-of-the-art commercial SiC MOSFET packages. The TO-247 and TOLL have the same specification parameters as the FOPLP for the die, the solder layer, and the molding. In accordance with MIL-PRF-38535J, for both TO-247 and TOLL, four copper bonding wires of diameter 15 mil were selected to connect the source and source terminal, and one copper bonding wire of diameter 15 mil was used to connect the gate and gate terminal. The phase-leg SiC MOSFET module with PCB-embedded FOPLP (denoted as FOPLP_P) is from our previous work, and the materials parameters can be referred from Hou et al. [23]. The FOPLP_P contains a high-side SiC MOSFET (HS-MOS) and a low-side SiC MOSFET (LS-MOS). In this study, only HS-MOS was used to analyze.

The physical models of FOPLP, TOLL, TO-247, and FOLPL_P are displayed in Figs. 1 and 3(a)–(c), respectively, and their dimensions are shown in Fig. 3(d).

A. Parasitic Inductance Simulation

Parasitic inductance is an inherent property of a conductor and depends on both the material and structure of the conductor. SiC MOSFET switching speeds are severely limited by packaging parasitic inductance. The package parasitic

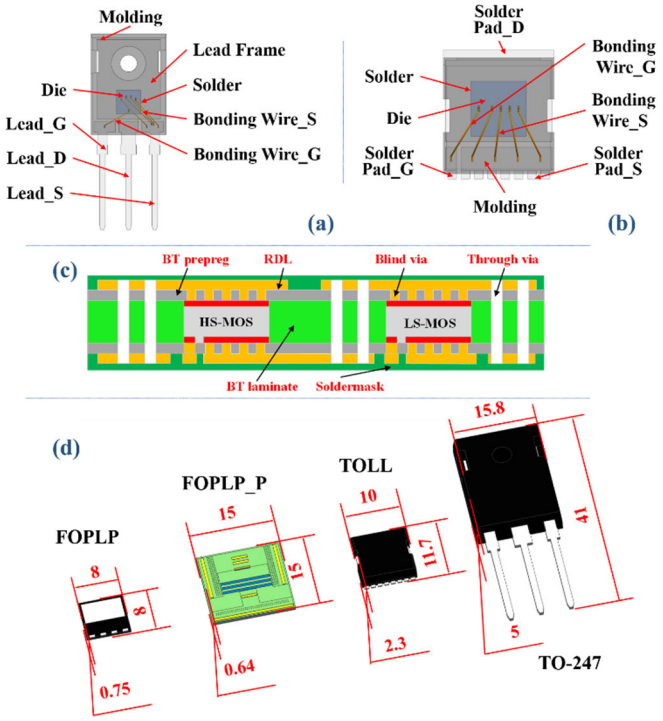

Fig. 3. SiC MOSFET (a) TO-247, (b) TOLL wire-bonding packaging structures, and (c) PCB-embedded FOPLP wireless-bonding packaging [23]. (d) Size comparison of FOPLP, FOPLP_P, TOLL, and TO-247 packages.

TABLE II
PARASITIC INDUCTANCE DEFINITIONS OF FOPLP, TOLL,TO-247, AND FOPLP_P

Package type	Symbol	Definition
FOPLP	L_D	From solder pad_D to solder
	L_S	From RDL_S to solder pad_S
	L_G	From solder pad_G to RDL_G
TOLL	L_D	From solder pad_D to solder
	L_S	From bonding wire_S to solder pad_S
	L_G	From solder pad_G to bonding wire_G
TO-247	L_D	From lead_D to solder
	L_S	From bonding wire_S to lead_S
	L_G	From lead_G to bonding wire_G
FOPLP_P	L_D	Interfaces between blind vias and HS-MOS drain
	L_S	Interfaces between blind vias and HS-MOS gate
	L_G	Interfaces between blind vias and HS-MOS source

inductance of SiC MOSFET is composed of drain inductance (L_D), source inductance (L_S), and gate inductance (L_G) (see Fig. 4). Drain–source inductance (L_{DS}) is defined as the sum of L_D and L_S. Table II lists the parasitic inductance definitions of FOPLP, TOLL, and TO-247.

In inductance extraction, the bulk conductivity of copper and Sn5Sb solder were set as 5.8e7 and 7e6 S/m, respectively, and the relative permittivity of SiC was set as 10. The sweep frequency ranged from 0 to 1000 kHz. The simulated package parasitic inductances of FOPLP, TOLL, TO-247, and FOPLP_P are shown in Fig. 5. The packaging parasitic inductance is dependent on the switching frequency. For the skin effect and proximity effect, the packaging parasitic inductance decreased with the switching frequency. However,

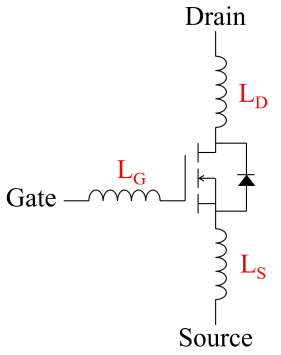

Fig. 4. Equivalent circuit diagram of the SiC MOSFET.

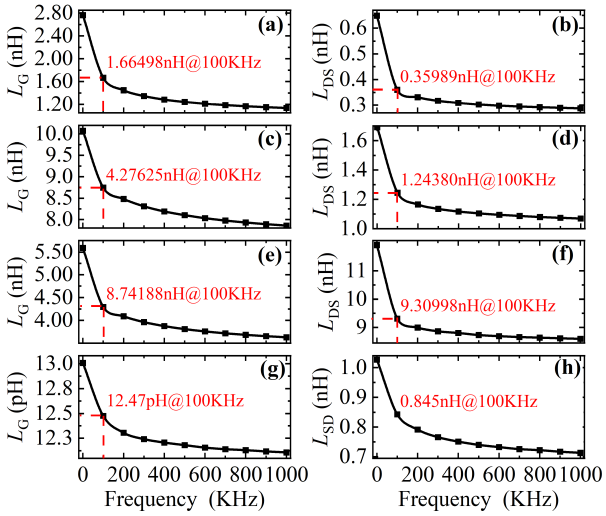

Fig. 5. Simulated package parasitic inductance versus switching frequency: (a) L_G of FOPLP, (b) L_{DS} of FOPLP, (c) L_G of TOLL, (d) L_{DS} of TOLL, (e) L_G of TO-247, (f) L_{DS} of TO-247, (g) L_G of FOPLP_P, and (h) L_{DS} of FOPLP_P.

the decrease rate continued progressively with the increase in the switching frequency.

Because of the longer conductive path and the bent in the bonding wire, the packaging parasitic inductances of TOLL and TO-247 are higher than those of FOPLP and FOPLP_P. The L_G and L_{DS} of the FOPLP at 100 kHz were 1.66 and 0.36 nH, respectively, and the L_G and L_{DS} of the FOPLP_P at 100 kHz were 12.47 pH and 0.845 nH, respectively. While the L_G and L_{DS} of TOLL at 100 kHz were 4.28 and 1.24 nH respectively, and the L_G and L_{DS} of TO-247 at 100 kHz were 8.74 and 9.31 nH respectively. Compared with TOLL, the L_G and L_{DS} of FOPLP decreased by 61.21% and 70.97%, respectively. And compared with TO-247, the L_G and L_{DS} of FOPLP decreased by 81% and 96%, respectively. Therefore, RDL, as an electrical interconnection component, provides a superior parasitic inductance reduction than the copper bonding wire.

B. Thermal Resistance Simulation

The high heating power, small size, and low thermal conductivity of EMC presented numerous thermal management challenges. Therefore, an efficient heat dissipation solution is necessary for SiC MOSFET. Double-sided cooling provided

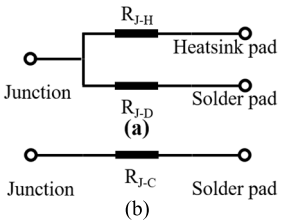

Fig. 6. Equivalent thermal network resistance: (a) double-side cooling and (b) single-side cooling.

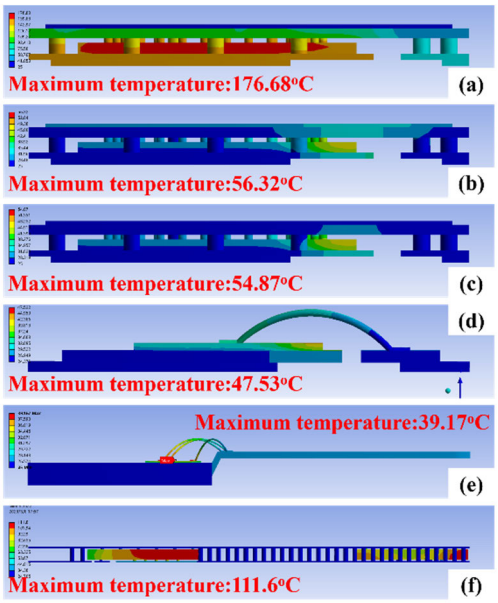

Fig. 7. Simulated temperature distribution results: (a) FOPLP using the heatsink pad for cooling, (b) FOPLP using the solder pad for cooling, (c) FOPLP with double-side cooling, (d) TOLL with single-side cooling, (e) TO-247 with single-side cooling, and (f) FOPLP_P with single-side cooling.

by the FOPLP allows higher heat dissipation than single-sided cooling does as depicted in Fig. 6.

A thermal simulation was conducted to evaluate the heat dissipation effect of the FOPLP with double-side cooling. The heating power was set at 58.8 W, for the ON-state current and ON-state resistance of 70 A and 12 mΩ, respectively. The ambient temperature of 25 °C was applied on the heat dissipation surface, and two heat dissipation surfaces were realized at double-side cooling. The thermal parameters of packaging materials used in the simulation were listed in Table I. The thermal resistance is calculated by the equation given as

$$R = \left(T_{\text{junction}} - T_{\text{ambient}}\right)/P_{\text{th}} \tag{1}$$

where T_{junction} is defined as the maximum simulated temperature for the die, T_{ambient} is the ambient temperature, and P_{th} is the internal heat power.

The simulated temperature distribution results of FOPLP under various cooling conditions are displayed in Fig. 7(a)–(c). Because the die and heatsink pad were separated by EMC with low thermal conductivity, the maximum temperature reached 176.68 °C when using only the heatsink pad for cooling [see Fig. 7(a)]. Another scenario involves attaching a solder pad to a die through RDLs. In this case, the maximum temperature reached only 56.32 °C [see Fig. 7(b)]. The best heat dissipation capability was achieved when double-sided cooling FOPLP was used, and a maximum temperature of only 54.87 °C was recorded [see Fig. 7(c)].

TABLE III
DEFINITIONS AND VALUES OF THERMAL RESISTANCE

Package types	Symbols	Definitions	Values (°C /W)
FOPLP	$R_{\text{J-H}}$	From junction to heatsink	2.58
	$R_{\text{J-S}}$	From junction to solder pad	0.53
	$R_{\text{J-C}}$	From junction to case with double side dissipation	0.51
TOLL	$R_{\text{J-C}}$	From junction to case	0.38
TO-247	$R_{\text{J-C}}$	From junction to case	0.24
FOPLP_P	$R_{\text{J-C}}$	From junction to case	1.47

Among TOLL, TO-247, and FOPLP_P, only one side was used for cooling. As displayed in Fig. 7(d)–(f), the maximum temperature of TOLL, TO-247, and FOPLP_P SiC MOSFETs under the same simulation condition as FOPLP were 47.53 °C, 39.17 °C, and 111.6 °C. The TOLL and TO-247 packages exhibit a maximum temperature lower than the FOPLP and FOPLP_P package. The thermal resistance can be calculated from the simulation results. Table III compares the thermal resistance values of the FOPLP, TOLL, TO-247, and FOPLP_P packages. It can be noted that the volumes of TOLL and TO-247 are most of the time greater than the FOPLP package. Numerically, the volumes of FOPLP, FOPLP_P TOLL, and TO-247 are 47.49, 130.54, 226.55, and 1156 mm^3, respectively, in the ratio of 1:2.74:4.77:24.34.

C. Thermo–Mechanical Simulation

In the die attachment process, the die, solder, and lead frame undergo reflow soldering at 250 °C. When the temperature decreased to room temperature (25 °C), residual stress was readily brought to the assembly, for the CTE mismatch in adjacent materials. Residual stress generated in the reflow soldering process was simulated using the FE method to investigate the thermo–mechanical properties of the assembly and the thermo-mechanical parameters of packaging materials used in the simulation are listed in Table I.

In the simulation, the temperature decreased from 250 °C to 25 °C. Remote displacement was imposed on the bottom surface of the lead frame or solder pad_D. Furthermore, the contact between the adjacent layers was assumed to be ideal, and dimension tolerances, which were dependent on the packaging process were also not considered. The simulated static thermo–mechanical performance results in FOPLP, TOLL, TO-247, and FOPLP_P packaging dies are displayed in Fig. 8. The maximum strains and stresses in both FOPLP, TOLL, TO-247, and FOPLP_P occurred in the corner of die. However, the dies in TOLL and TO-247 should withstand a larger mechanical load.

The maximum stress and strain of FOPLP were 689.47 MPa and 0.0138, respectively. The maximum stress and strain of TOLL were 926.32 MPa and 0.0189, respectively. The maximum stress and strain of TO-247 were 1475.60 MPa and 0.0301, respectively. The maximum stress and strain

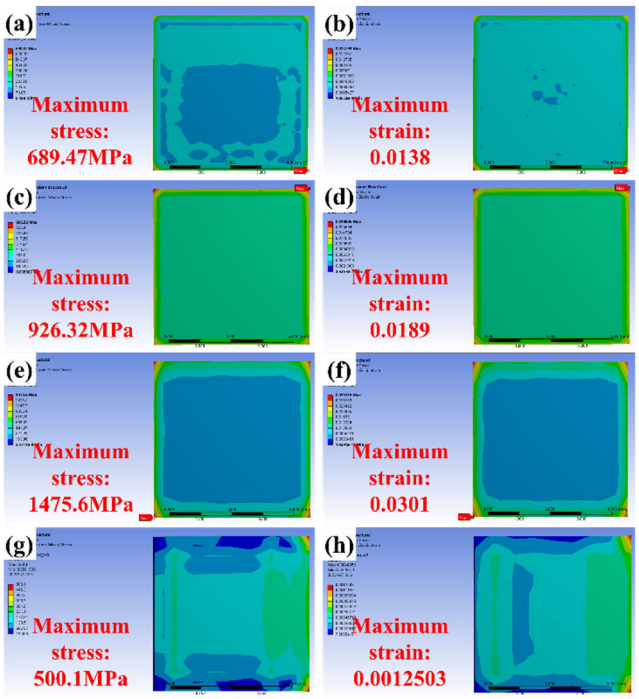

Fig. 8. Static thermo–mechanical simulation results in the dies of different packages: (a) maximum stress of FOPLP, (b) maximum strain of FOPLP, (c) maximum stress of TOLL, (d) maximum strain of TOLL, (e) maximum stress of TO-247, (f) maximum strain of TO-247, (g) maximum stress of FOPLP_P, and (h) maximum strain of FOPLP_P.

of FOPLP_P were 500.1 MPa and 0.0012503, respectively. Compared with TOLL and TO-247, the FOPLP relieved the residual stress of packaging materials and reduced their deformation. Compared to TOLL, the maximum stress and strain of FOPLP decreased by approximately 25.57% and 26.98%, respectively. Compared to TO-247, the maximum stress and strain of FOPLP decreased by approximately 53.27% and 54.15%, respectively.

Generally, as a wire-bondless interconnection packaging, RDL is used in FOPLP to replace bonding wire. So FOPLP exhibits lower parasitic inductance compared to wire-bonding TO-247 and TOLL. The miniaturization of FOPLP also reduces the thermal stress in the packaging when an unreasonable temperature change occurs. Because the source, gate, and drain are all connected by thin RDL, FOPLP_P has superior thermo–mechanical performance over FOPLP. However, thermal management challenges the application of FOPLP, for its higher power density.

IV. Initial Performance and Long-Term Reliability Characterizations of SiC MOSFET FOPLP

The initial performance of SiC MOSFET FOPLP was measured to verify its proper functionality. Next, the thermal cycling test of SiC MOSFET FOPLP was performed for long-term reliability investigation.

As shown in Fig. 9, the devices were electrically connected to the tester using a custom high-power socket for static parameters measurement; for capacitance measurement, the devices were soldered on the PCB with an edge connector.

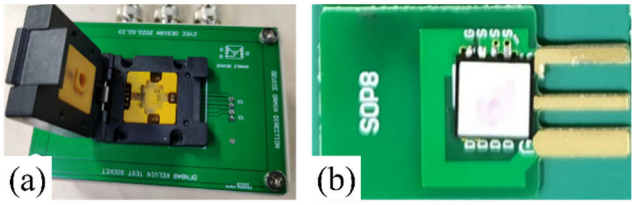

Fig. 9. (a) Custom socket for static parameter measurement and (b) PCB for capacitance measurement.

TABLE IV
Measured Static Parameters Results of SiC MOSFET FOPLP

Symbols	Conditions	Units	Mean values	Variances	Maximum values of die
I_{DSS}	V_{DS}=950V	μA	2.90	1.46	80
I_{GSS+}	V_{GS}=23V	nA	69.48	9.81	100
I_{GSS-}	V_{GS}=-2V	nA	-14.47	1.02	-100
$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=35.1mA	V	3.13	0.21	4.5
$R_{ds(on)}$	I_D=70A, V_{GS}=18V	mΩ	10.88	0.11	15

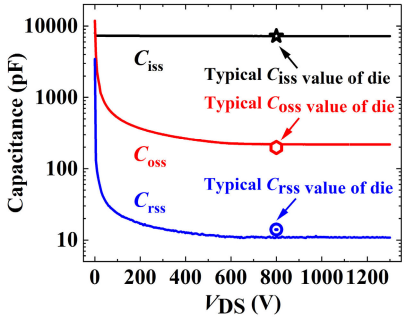

Fig. 10. Measured capacitances versus the drain–source voltage (0–1300 V).

A. Initial Performance Characterization

The static parameters of SiC MOSFET FOPLP including zero gate voltage drain current (I_{DSS}), gate–source leakage current (I_{GSS}), gate threshold voltage [$V_{GS(th)}$], and ON-state resistance [$R_{DS(on)}$] were measured by using a static parameter tester (1600A-MT, HUSTEC). The results are listed in Table IV. All static parameter values were lower than the corresponding maximum values of the die provided in the datasheet. The input capacitance (C_{iss}), output capacitance (C_{oss}), and reverse transfer capacitance (C_{rss}) were tested in a curve tracer (B1505A, Agilent) under the following test conditions: $V_{GS} = 0$ V, $f = 1$ MHz, and the test results are shown in Fig. 10. The measured C_{iss}, C_{oss}, and C_{rss} at 800 V were close to the typical values of die. The capacitances decreased with the frequency. From V_{DS} values of 0 to 100 V, the capacitances decreased notably. Capacitances gradually decreased and leveled off as the drain–source voltage increased from 100 to 1300 V.

B. Thermal Cycling Reliability Analysis

The thermal cycling test is widely used to investigate the effect of periodical temperature changes on the packaging

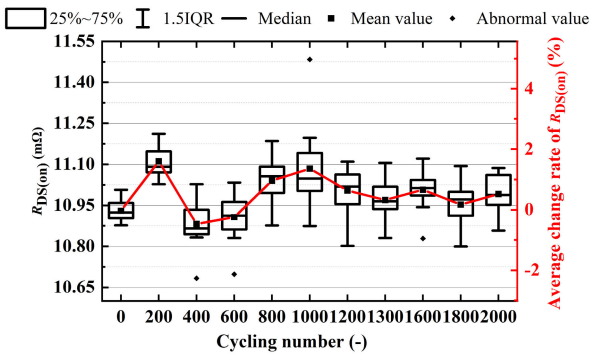

Fig. 11. Variation of $R_{DS(on)}$ during aging cycles.

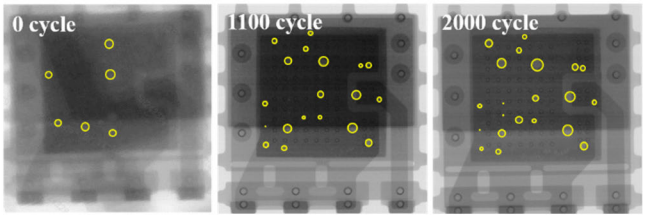

Fig. 12. X-RAY images at 0, 1100, and 2000 cycles.

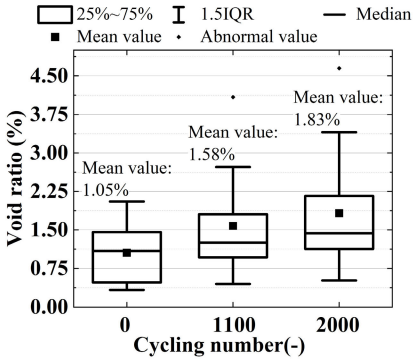

Fig. 13. Void ratios at 0, 1100, and 2000 cycles.

material interfaces. In a thermal cycling test, the device temperature is changed by varying the testing chamber temperature between the upper and lower limits. The thermal cycling test was conducted on 12 samples of SiC MOSFET FOPLPs by using an environmental chamber (EC-106MHHP, HITACHI). Test temperatures ranged from −55 °C to 125 °C, and the holding time and conversion time were 15 and 10 min, respectively.

ON-state resistance [$R_{DS(on)}$] will increase when degradation occurred in the solder or the interconnection between the die and RDL. Thus, $R_{DS(on)}$, as a degradation precursor, is typically used to determine the packaging fatigue failure occurring in thermal cycling. Here, $R_{DS(on)}$ was experimentally monitored during the test process through a static parameter tester (1600A-MT, HUSTEC). Fig. 11 displays the variation of $R_{DS(on)}$during aging cycles. The $R_{DS(on)}$value basically remained constant over the test process, and the maximum average change rate of $R_{DS(on)}$ was less than 2%. The stability of $R_{DS(on)}$ proved the high reliability of the package.

To detect the states of the solder and the interconnection between the die and RDL, X-RAY, and C-SAM tests were

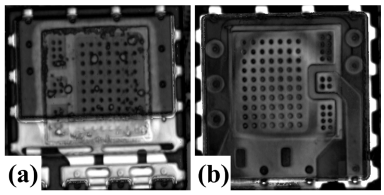

Fig. 14. C-SAM images of the sample at 2000 cycles: (a) bottom view and (b) top view.

carried out for aged samples. Nordson DAGE XD7500 was used to perform X-RAY characterization. All samples were imaged prior to cycling to provide a basis for comparison and subsequently imaged at 1100 and 2000 cycles. The X-ray images are displayed in Fig. 12. The number of voids increased with the increase in aging cycles. FiJi distribution of ImageJ was used to count the void ratio of all samples, and the voids were marked with a yellow circle. The results are depicted in Fig. 13. The mean void ratios at 0, 1100, and 2000 were recorded as 1.05%, 1.58%, and 1.83%, respectively. The increase in void ratios was related to the crack propagation that occurred during thermal cycling [33]. The C-SAM images of the sample subjected to 2000 aging cycles were captured using SHSIWI YTS-500. Fig. 14(a) illustrates the presence of voids in solder; however, no delamination was observed. Fig. 14(b) reveals that the RDL was firmly connected to the die. The increase in void or lateral crack increases $R_{DS(on)}$slightly. The delamination of the interface between various materials can result in device failure.

V. Conclusion

In this article, SiC MOSFET FOPLP was fabricated, analyzed, and characterized. The simulation method was used to investigate the high electric, thermal, and mechanical performances of SiC MOSFET FOPLP. The initial performance and long-term reliability of the device were experimentally verified. Compared with conventional wire-bonded packaging, the proposed method reduced drain–source parasitic inductance by 96% at 100 kHz. Because of double-sided cooling, the package exhibited a low thermal resistance of 0.55 °C/W. Compared with TOLL and TO-247, the soldering stress and strain were alleviated in FOPLP. The static and dynamic parameters of the package were consistent with those provided on the bare die datasheet. The drain–source ON-state resistance increased by less than 2% after 2000 thermal cycles, which revealed the durability of the packages.

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