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A 2-Mode Reconfigurable SSHI Rectifier with 3.2X Lower Cold-Start Requirement for Piezoelectric Energy Harvesting*

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***Abstract*—Synchronized switch harvesting on inductor (SSHI) rectifier has been verified as an efficient active rectifier to harvest kinetic energy in piezoelectric energy harvesting (PEH) system. Compared with passive rectifiers, active rectifiers including SSHI rectifier require a stable power supply to drive switches. However, when the system starts from the cold state, the required power supply is not available at first. For the active rectifiers, the active circuits work as a typical full bridge rectifier (FBR) until the stable power supply is built up. Unfortunately, a FBR cannot build up a stable power supply when the input open circuit voltage V_{OC} is lower than the required power supply, resulting in disabled active rectifiers. This paper proposes a 2-mode reconfigurable SSHI rectifier design for low input V_{OC}. By this method, the requirement for the input V_{OC} is 3.2X lower than a FBR. The proposed system is designed in a 0.18μm process and post-layout simulations verify the cold start-up process under low V_{OC} voltage.**

***Index Terms*—Cold start-up, voltage multiplier, piezoelectric energy harvesting, open-circuit voltage, SSHI rectifier**

I. Introduction

Wireless sensors are the key to connect objects in the internet of things (IoT) system. Typically, a battery is required for the sensors to operate. However, frequently recharge or replace the typical batteries is an impossible task because of the cost and inconvenience. Piezoelectric energy harvesting (PEH) provides a way to power wireless sensors by harvesting kinetic energy to electrical energy which is able to achieve self-powered autonomy. Unfortunately, the output from piezoelectric transducer (PT) is AC. A typical AC-DC converter is required for the energy conversion. A Full bridge rectifier (FBR) is the simplest passive rectifier, but it has low conversion efficiency. Some active designs like synchronized switch harvesting (SSH) rectifiers [1]–[3] are all developed to improve the extracted output power from the PT.

A synchronized switch harvesting on inductor (SSHI) rectifier improves the power extraction efficiency by employing an inductor to flip the voltage across the PT. However, the active rectifiers need a DC power supply (V_{DD}) to operate. Before V_{DD} is ready, the active rectifiers are performed as a passive FBR to build up the power supply. Some proposed SSHI rectifiers work after cold state is ended, which ignore the details of realising cold start-up especially when the input open-circuit voltage amplitude (V_{OC}) is lower than required power supply. Most importantly, if $V_{OC} < V_{DD}$, the FBR is not able to build up a V_{DD} successfully, resulting in a disabled SSHI rectifier due to the cold-start failure. [4] proposes a new cold start-up method by splitting a monolithic PT into 4 pieces and connect them in series during cold state. However, this method requires a customized PT which is not suitable for general PT.

This paper proposes a new reconfigurable cold start-up design by employing a voltage multiplier in mode 1 during cold state to build up a stable V_{DD} to power the active SSHI rectifier. The input V_{OC} is lowered to 3.2X smaller than the required V_{DD} in this design. When the cold state is ended, the circuit is configured to mode 2 and SSHI rectifier combined with a FBR would start to work. The post-layout simulations show that when V_{OC} is $0.5V$, the system can start working from the cold state.

This work is organised as follows: analysis of the cold start-up circuit is given in Section II. Section III shows the system architecture. Circuit implementations are given in Section IV. Post-layout simulation results are shown in Section V to show the effectiveness of the proposed design. Finally, Section VI is the conclusion.

II. Proposed Design Analysis

A. Conventional Cold Start-Up Circuit – FBR

The conventional SSHI rectifier works as a passive FBR during cold state. The equivalent circuit diagram during the cold start-up stage is shown in Fig. 1. The PT is modeled as an AC current source, I_P and in parallel with a capacitor, C_P. SSHI rectifier is disabled during cold state and a FBR is used to rectify the AC energy to build up a stable V_{DD}. C_S is a storage capacitor. Connected with C_S, a low dropout (LDO) regulator employs off-chip capacitor C_{DD} and four resistors R_1 to R_4, to generate V_{DD}. The SSHI rectifier would start operating under a stable V_{DD}, after the cold state is finished. For a FBR, the output voltage is limited by the voltage drop of the diode. If V_{OC} is lower than required V_{DD},

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the required V_{DD} would not be able to be built up, hence, the designed active rectifier would not operate. Detailed analysis are presented as follows.

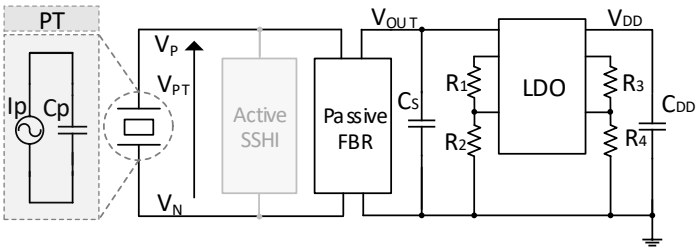

Fig. 1. Conventional cold start-up circuit

B. Proposed Cold-Startup – Voltage Multiplier

If the circuit starts with a FBR, the maximum output voltage of the FBR is

$$V_{DDmax} = V_{OC} - 2 * V_D \tag{1}$$

where V_D is the voltage drop of the diode. The smallest input open circuit voltage of the FBR V_{OCFBR} is expressed as

$$V_{OCFBR} = V_{DDmax} + 2 * V_D \tag{2}$$

However, when voltage multiplier is used during cold state, the maximum output voltage is

$$V_{DDmax} = 4 * (V_{OC} - V_D) \tag{3}$$

Thus, the smallest input open circuit voltage of the voltage multiplier V_{OCVM} can be expressed as

$$V_{OCVM} = \frac{1}{4} V_{DDmax} + V_D \tag{4}$$

From the above equations, it shows that the FBR sets a higher start-up threshold voltage for the input V_{OC} for the same V_{DD}. For the voltage multiplier, the input V_{OC} is much lower. In this work, we use sbd_dio_ga_12_3t (voltage drop: around 0.2V) as the diodes, the measured voltage drop is around 200mV. The prepared V_{DD} is 1.2V which is enough to turn on/off the low voltage transistors. Theoretically, for the voltage multiplier, the needed input V_{OC} is 0.5V while the FBR requires at least 1.6V as the input. The input V_{OC} for the voltage multiplier is 3.2X lower than the input of a FBR. Thus, FBR has limited output voltage when input V_{OC} is in low level. As shown in Fig. 2, during cold state voltage multiplier is working in mode 1. C_1 to C_4 are used to harvest the rectified energy. The output voltage of the voltage multiplier, V_{OUT}, is connected to a LDO to generate a V_{DD}.

After V_{DD} is prepared, the system changes to mode 2. The four diodes used in voltage multiplier are reconfigurable as a FBR in order to start SSHI rectifier. As is shown in Fig. 3, C_3 and C_4 are connected in series as the storage capacitor at the output end. In this stage, the SSHI rectifier is enabled during PT flipping time. The details of the connections between different sub-blocks are shown in the system architecture.

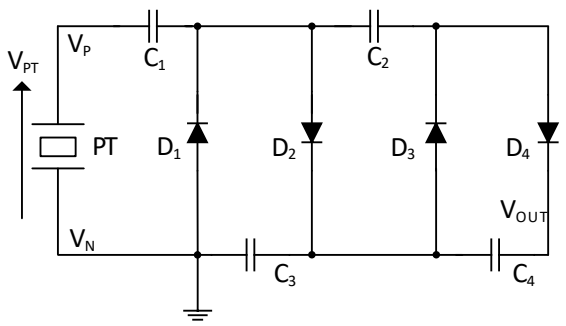

Fig. 2. Voltage multiplier rectifier working stage

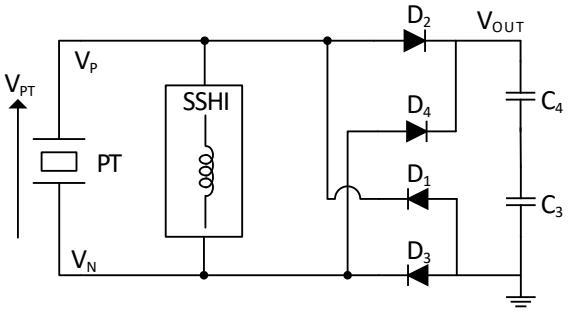

Fig. 3. SSHI rectifier and FBR working stage

III. System Architecture

Fig. 4 shows the system architecture of the proposed design. There are six blocks in the architecture, a SSHI rectifier, a FBR, a switch control block, a voltage multiplier four capacitors and a LDO. Four capacitors are used to harvest the rectified energy. A LDO is to provide a power supply V_{DD} from the voltage multiplier during cold state in mode 1. When the cold state is finished, the system changes to mode 2, hence, a 'Rdy' signal will be generated from the LDO and fed to switch control block. Then switch control block will change the connection of the diodes from voltage multiplier to a FBR combined with a SSHI rectifier. During cold stage, C_1 to C_4 are used in voltage multiplier while C_3 and C_4 are connected in series and performed as the storage capacitors.

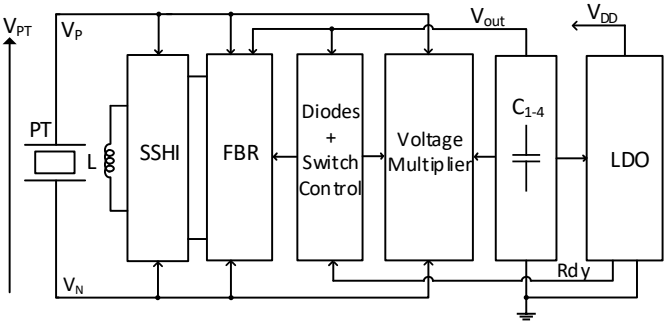

Fig. 4. System architecture of proposed design

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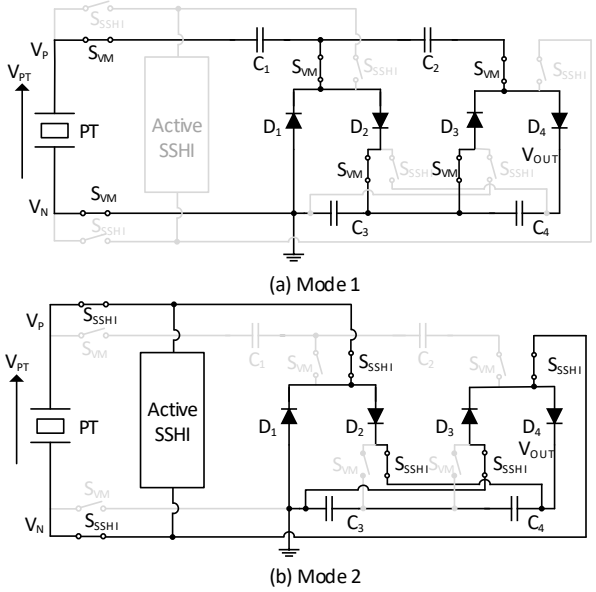

Fig. 5. Voltage multiplier and FBR connections

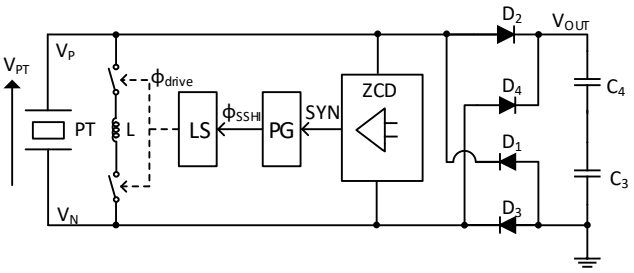

Fig. 6. SSHI rectifier working blocks

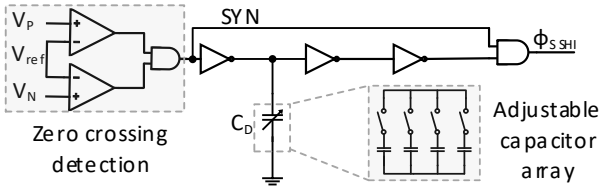

Fig. 7. Zero crossing block and pulse generation cell

IV. Circuit Implementation

Fig. 5 shows the switch control block of voltage multiplier and active rectifier in 2-mode. As shown in Fig. 5(a), during cold state, the 4 diodes are connected to form a voltage multiplier by turning on S_{VM} and turning off S_{SSHI} in mode 1. The V_N is connected to ground and V_P is connected to C_1. Fig. 5(b) shows that in mode 2 the switches controlled by S_{VM} are closed and the switches controlled by S_{SSHI} are opened. The V_P and V_N are connected to the storage capacitors as typically active rectifiers do. C_3 and C_4 are connected in series as the storage capacitor at the output. The circuit is performed as a typical SSHI rectifier and works together with a FBR.

When the SSHI rectifier is working, the corresponding working block is displayed in Fig. 6. There are three blocks to drive the SSHI rectifier. Zero crossing detection (ZCD) block is to decide the start time of the switches used in the SSHI rectifier. When it is time to start SSHI rectifier, the ZCD block generates a synchronized SYN signal and it is fed to the pulse generation (PG) block to generate the pulse ϕ_{SSHI}. Detailed circuit is also shown in Fig. 7. ZCD block consists of two comparators to compare V_P and V_N with V_{ref} which is a slightly lower voltage than the voltage drop, to generate a SYN signal to PG block. C_D is an adjustable capacitor array to adjust the generated pulses to catch the appropriate flipping time. Through a level shifter (LS) ϕ_{drive} is generated to fully drive synchronized switches in SSHI rectifier in a short time to flip the PT voltage.

V. Post-Layout Simulation Analysis

This system is designed in a 0.18-μm BCD process. Post-layout simulation system parameters are V_{OC} = 0.5V; C_P = 40nF; $F = 200Hz$; the capacitance of each used capacitor is C_1 = C_2 = C_3 = C_4 = 1μF; threshold voltage of the on-chip

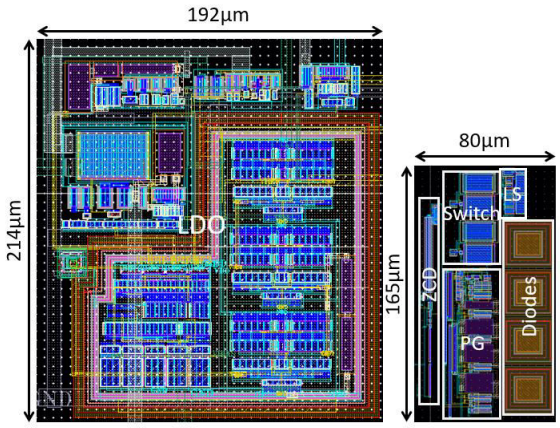

Fig. 8. Layout of LDO and proposed design

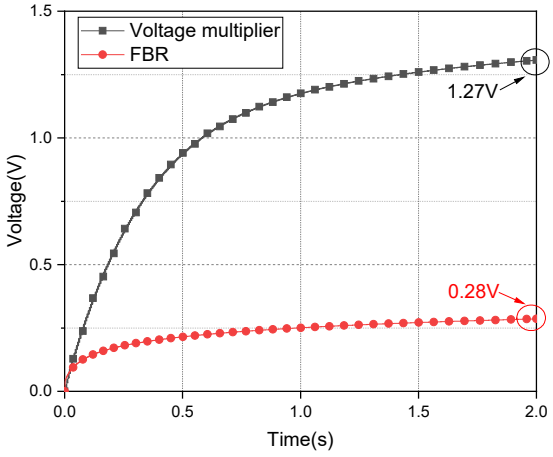

Fig. 9. Output voltage of voltage multiplier and FBR

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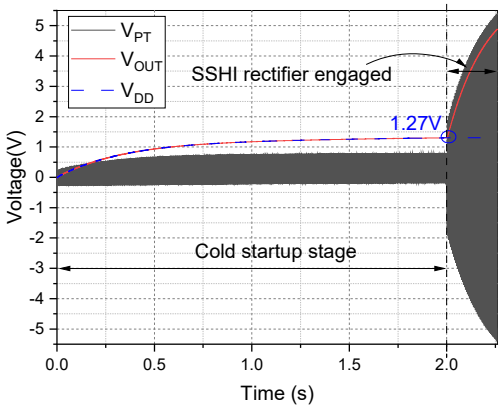

Fig. 10. Output voltage of V_{PT}, V_{OUT} and V_{DD} of the proposed design

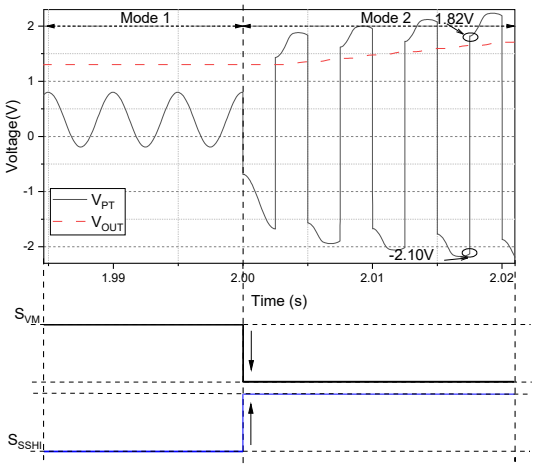

Fig. 11. Output voltage signals at reconfigurable moment

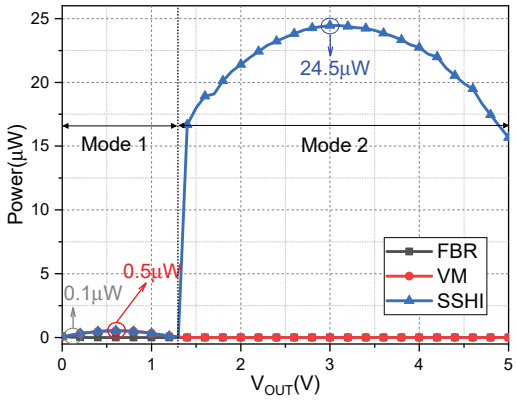

Fig. 12. Output power of the proposed design, voltage multiplier and FBR

diode is around 0.2V; prepared V_{DD} = 1.27V. Corresponding layout is shown in Fig. 8. The LDO is taped out separately. The dimension of the proposed design is $0.0132mm^2$, and the LDO is $0.04mm^2$. Details about the output performance of the designed circuit are shown in the following figures.

Fig. 9 shows the difference of the output voltage between using a FBR and using voltage multiplier. The measured voltage drop of the used diode is around 200mV. Input V_{OC} = 0.5V. Because of the voltage drop of the diodes, the maximum voltage of the FBR is approximate to 0.28V while voltage multiplier has 1.27V which is almost consistent with what we have introduced in the theoretical analysis of Section II.B. The V_{DD} in this design is 1.27V because the threshold voltage of the low voltage transistors is around 0.8V and 1.27V is high enough to turn on/off the low voltage transistors used in 0.18-μm BCD process. And the total power consumption would also be limited by a relatively lower V_{DD}.

Fig. 10 shows the output V_{OUT}, V_{DD} and V_{PT} of the proposed design. The V_{OUT} is build up from 0 to nearly 5V. V_{DD} follows V_{OUT} when the system starts from cold state and hold at 1.27V when the cold start-up is ended. Reconfigurable moment is also shown in Fig. 11. S_{VM} is high during mode 1 while S_{SSHI} turns to high when the system is configured to mode 2. At the changing moment, V_{PT} jumps largely and is flipped by the SSHI rectifier. V_{PT} is flipped from -2.10V to 1.82V which denotes 86.7% flipping efficiency.

Fig. 12 shows the output power of a FBR, voltage multiplier and an active SSHI rectifier. The output power of the FBR is $0.1\mu W$ due to low input V_{OC} and high threshold voltage of the diode. The maximum extracted power of the voltage multiplier is 0.5μ W. However, for the active SSHI rectifier, the maximum extracted power is the same as voltage multiplier before V_{DD} is prepared in mode 1. When the cold state is finished the circuit changes to mode 2, and the output power jumps to high largely and achieves peak power at 24.5μ W which is 245X higher than the typical FBR.

VI. Conclusion

This work uses 2-mode SSHI rectifier to lower the requirement of the input V_{OC} during cold start-up state. A 0.5-V V_{OC} is used as the input, and a 1.27-V V_{DD} is the output voltage. In mode 1, only passive voltage multiplier is working while in mode 2 active SSHI rectifier combined with passive FBR starts to work. The simulated maximum output power of the typical cold start-up circuit-FBR is $0.1\mu W$ due to low input V_{OC} and voltage drop of diodes. In our proposed design the output power is 24.5μW with 86.7% flipping efficiency.

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