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## RESEARCH ARTICLE

# Application of metal, metal-oxide, and silicon-oxide based intermediate reflective layers for current matching in autonomous high-voltage multijunction photovoltaic devices

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**Abstract**

A logical next step for achieving a cost price reduction per Watt peak of photovoltaics (PV) is multijunction PV devices. In two-terminal multijunction PV devices, the photo-current generated in each subcell should be matched. Intermediate reflective layers (IRLs) are widely employed in multijunction devices to increase reflection at the interface between subcells to enhance current generation in the subcell(s) positioned before the IRL, in reference to the incident light. In this work, the results of over 65 multijunction devices are presented, in order to explore the effect of different current matching approaches. The influence of variations in absorber thickness as well as thickness variations of different IRLs based on silicon-oxide, various transparent conductive oxides (TCO), and metallic layers on all-silicon multijunction PV devices is studied. Specifically, hybrid, 2-terminal, monolithically integrated silicon heterojunction (SHJ) and thin film nanocrystalline silicon (nc-Si:H) and amorphous silicon (a-Si:H) tandem and triple junction devices are processed. Based on these experiments, certain design rules for optimal current matching operation in multijunction devices are formulated. Finally, taking these design rules into account, record all-silicon multijunction devices are processed. Conversion efficiencies close 15% and  $V_{oc} \approx 2\text{ V}$  are demonstrated for triple junction SHJ/nc-Si:H/a-Si:H devices. Such conversion efficiencies for a wireless, high-voltage wafer-based all-silicon 2-terminal multijunction PV device opens the way for efficient autonomous solar-to-fuel synthesis systems as well as other wireless innovative approaches in which the multijunction solar cell is used not only as a photovoltaic current-voltage generator, but also as an ion-exchange membrane, electrochemical catalysts, and/or optical transmittance filter.

**KEYWORDS**

amorphous silicon, intermediate reflective layer, multijunction PV, nanocrystalline silicon, silicon oxide, solar to fuel, thin film silicon, transparent conductive oxide, tunnel recombination junction

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## 1 | INTRODUCTION

Multijunction photovoltaic (PV) devices have the potential to enhance spectral utilization, thereby achieving increased PV yield per area as well as reduced heating and lower temperature coefficients. Additionally, multijunction PV devices can achieve high voltages without interconnection, facilitating autonomous solar-to-fuel applications.

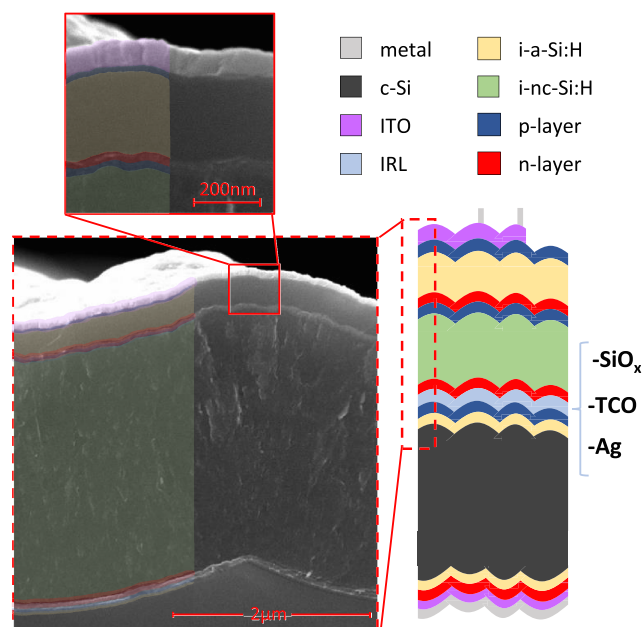
Photo-generation of charge carriers occurs in each subcell in multijunction devices. For optimal operation, in two-terminal devices, the photo-current generated in each subcell should be matched. In multijunction devices, generally, the bottom cell is not current limiting as a reflective metallic layer can be positioned at the back of the devices. For the top or middle subcell(s), the simplest means of increasing the photo-generated current is increasing the absorber thickness. However, this generally results in an increase of the series resistance, and consequently decrease of the open circuit voltage ( $V_{oc}$ ) and Fill Factor ( $FF$ ), as the recombination probability increases with the average distance a photo-generated charge carrier has to travel for collection. Such a trade-off between the short-circuit current density ( $J_{sc}$ ) and  $V_{oc}$  has been demonstrated in silicon solar cells, including devices with hydrogenated (:H) nanocrystalline (nc-) silicon (Si) absorbers,<sup>1</sup> amorphous (a-) Si-germanium (SiGe):H absorbers,<sup>2</sup> and amorphous silicon-oxide ( $\text{SiO}_x$ ):H absorbers.<sup>3</sup> For that reason, intermediate reflective layers (IRLs) are widely employed in multijunction devices,<sup>4–10</sup> to enhance current generation and/or reduce the absorber thickness. IRLs are used to increase reflection at the interface between subcells to enhance current generation in the subcells(s) positioned before the IRL, in reference to the incident light. There are different materials that can be used for such an IRL. In certain device architectures, such as a perovskite/crystalline silicon (c-Si)<sup>11</sup> and a-Si:H/CIGS,<sup>12</sup> transparent conductive oxides (TCO) are positioned in between subcells. In silicon based multijunction devices, silicon-oxide based IRLs are often employed.<sup>5,7,9,13</sup> Generally an n-type (n-)  $\text{SiO}_x$  layer is used.<sup>14</sup> The properties of n- $\text{SiO}_x$  layers are more easily adjusted to achieve characteristics desirable for an IRL, in reference to p- $\text{SiO}_x$  properties, as the device performance is very sensitive to p- $\text{SiO}_x$  characteristics like the oxide fraction and layer thickness.<sup>15</sup> In this work, in addition to silicon-oxide and TCO based IRLs, the use of a very thin metallic layer is explored.

In order to characterize the performance of the different IRLs, all-silicon multijunction PV devices are used. Specifically, a hybrid c-Si and thin film Si multijunction device is used, consisting of a silicon heterojunction (SHJ) subcell and one or two additional thin film silicon subcells based on nc-Si:H and a-Si:H absorbers. The advantage of these plasma enhanced chemical vapor deposition (PECVD) processed, 2-terminal, monolithically integrated devices, is that a  $V_{oc} \approx 2\text{V}$  can be achieved without external wiring. Given the inherent chemical stability of silicon in reference to other PV technologies,<sup>16</sup> this allows for wireless, autonomous solar-to-fuel synthesis systems,<sup>17–20</sup> and other wireless innovative approaches in which the multijunction solar cell is used not only as a photovoltaic current-voltage generator, but also as an ion-exchange membrane,<sup>21,22</sup> electrochemical catalysts, and/or optical transmittance filter.<sup>23</sup> First, in Section 3.1, the influence of the nc-Si:H absorber thickness on 1J,

SHJ/nc-Si:H (2J), and SHJ/nc-Si:H/a-Si:H (3J) device is characterized. In the following three sections, the influence of an IRL based on  $\text{SiO}_x$ , TCO, and silver (Ag) is characterized. Using the design rules obtained from these characterization, a champion autonomous high-voltage 2J and 3J device is processed, which is presented in Section 3.5.

## 2 | EXPERIMENTAL SECTION

In this work, a number of tandem PV devices are presented, consisting of a wafer-based silicon heterojunction subcell and a thin film silicon subcell with a nc-Si:H absorber. For the 3J devices an additional thin film silicon junction was processed with an a-Si:H absorber. Scanning electron microscope (SEM) images as well as a simplified schematic structure of the triple junction device are presented in Figure 1. All hydrogenated silicon(oxide) layers, doped and undoped, are processed using plasma enhanced chemical vapor deposition (PECVD). The exact configuration and deposition conditions of the PECVD processed layers, with exception of the p-layers, are reported in de Vrijer et al.<sup>15</sup> For the p-layers, a bi-layer configuration was used, consisting of a 12 nm p-nc- $\text{SiO}_x$ :H and a more highly doped 4 nm p-nc- $\text{SiO}_x$ :H<sup>+</sup> layer. The deposition conditions of these layers are reported in Table 1. Additionally, metals and TCOs are used at the front and back of the devices, as shown in Figure 1, as well as a material for the IRL in Sections 3.3 and 3.4. All TCOs are processed through RF magnetron sputtering. More information about the processing equipment and conditions of indium-oxide doped with tin (ITO) and tungsten



**FIGURE 1** Schematic structure and SEM images of a typical SHJ/nc-Si:H/a-Si:H triple junction device presented in this work. The colors in the schematic structure, as well as those added to the left half of the SEM images, represent different materials, as indicated by the top-right legend. The position of the IRL, as well as the different materials used for the IRL, are indicated on the right of the schematic

**TABLE 1** Conditions used for the p-layer depositions

	$F_{\text{SiH}_4}$ (sccm)	$F_{\text{B}_2\text{H}_6}$ (0.02%) (sccm)	$F_{\text{CO}_2}$ (sccm)	$F_{\text{H}_2}$ (sccm)
p-nc-SiO <sub>x</sub> :H	0.8	10	2.2	170
p-nc-SiO <sub>x</sub> :H <sup>+</sup>	0.8	50	2.2	170

Note: Layers are processed at  $P_{\text{RF}} = 83.3 \text{ mW} \cdot \text{cm}^{-2}$ ,  $T_{\text{S}} = 180^\circ\text{C}$  and,  $p = 2.2 \text{ mbar}$ .

(IWO) can be found in Han et al.,<sup>24</sup> while the sputtering conditions of AZO can be found in de Vrijer et al.<sup>2</sup> Aluminum contacts are processed using electron beam evaporation, while the Ag layers are evaporated using resistive heating.

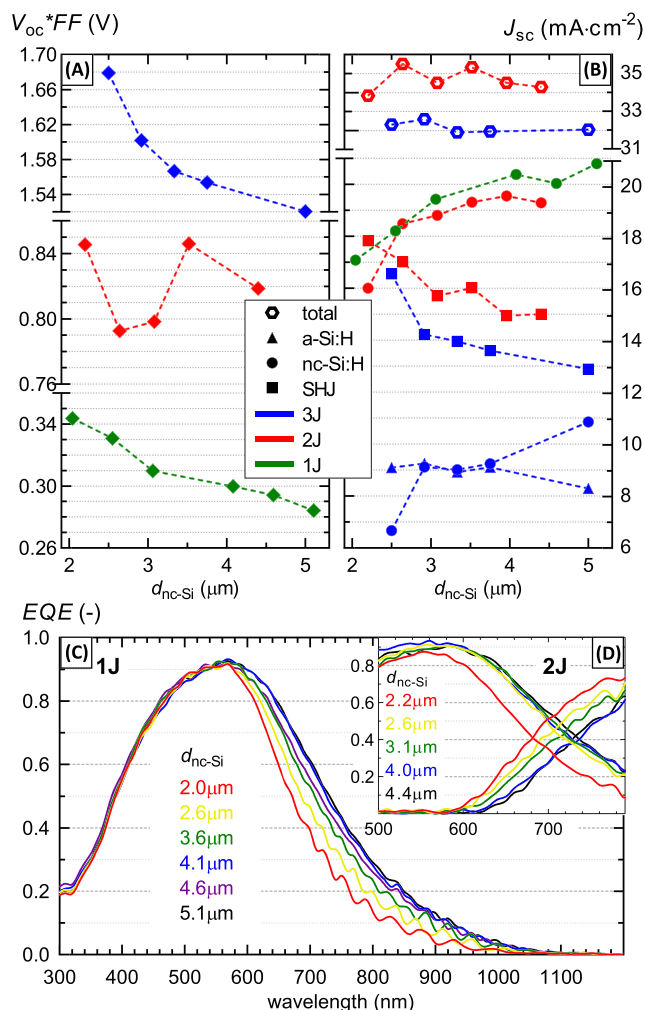
The 300  $\mu\text{m}$  thick n-type mono-crystalline silicon wafers with <100> orientation are used for processing the SHJ devices. The wafers are textured using an approach consisting of alkaline etching step followed by an acidic etching step. Both the texturing approach<sup>15</sup> and the optical behavior of the textured surface<sup>25</sup> are discussed in more detail elsewhere. The thin film silicon junctions are processed on top of the SHJ device, in n-i-p substrate configuration. Additionally, in Section 3.1, a series of single junction nc-Si:H devices are presented which are processed on textured glass. These devices are processed in n-i-p substrate configuration with a transparent aluminum-doped zinc oxide (AZO) back contact. The glass texturing procedure and processing flowchart of these single junction devices is similar to those used in de Vrijer et al.<sup>2</sup> No back reflector is used for these devices to better represent the situation when the nc-Si:H junction is used at the front or middle in a multijunction configuration.

The external quantum efficiency (EQE) of the multijunction device was obtained using an in-house EQE setup. The EQE of an individual junction in a multijunction device was obtained by saturating the other junction(s) with bias light. No bias voltage was applied during measurements. By weighing the EQE spectra with the AM1.5<sub>G</sub> solar spectrum, the short-circuit current density ( $J_{\text{sc}}$ ) of the individual junctions was obtained. The  $J$ - $V$  curves of the devices are measured at 25°C using an AM1.5<sub>G</sub> solar simulator. The open circuit voltage ( $V_{\text{oc}}$ ), fill factor ( $FF$ ), series resistance ( $R_{\text{s}}$ ), and shunt resistance ( $R_{\text{sh}}$ ) are obtained from these  $J$ - $V$  curves. On each sample, 24 individual 16 mm<sup>2</sup> cells are processed. All 24 cells are measured and the results presented in this work are the average of the five best cells. More detailed descriptions of these measurements can be found in de Vrijer et al.<sup>15</sup> The  $V_{\text{oc}}$ ,  $FF$ ,  $J_{\text{sc}}$ ,  $R_{\text{s}}$ ,  $R_{\text{sh}}$ , and conversion efficiency ( $\eta$ ) of all cells presented in this work can be found in the supporting information. Finally, the reflectance measurements were performed using a LAMBDA 1050+ Spectrophotometer from PerkinElmer.

### 3 | RESULTS AND DISCUSSION

#### 3.1 | Varying the i-nc-Si:H absorber thickness

Among the various means of distributing current over junctions in a multijunction device, a change in absorber thickness is the most



**FIGURE 2** Multijunction device characteristics as a function of  $d_{\text{nc-Si}}$ . (A) The  $V_{\text{oc}} * FF$ . (B) The  $J_{\text{sc}}$  of all the individual junctions as well as the total  $J_{\text{sc}}$ -sum of the individual subcells for the 2J and 3J devices, as obtained from EQE. The 1J device are processed on transparent substrates without back reflector. The EQE diagram of the 1J devices are presented in (C), while the relevant spectral part of the 2J devices are presented in (D)

straightforward. The product of the  $V_{\text{oc}}$  and  $FF$  ( $V_{\text{oc}} * FF$ ) and  $J_{\text{sc}}$  of a series of nc-Si:H single junction (1J) and SHJ/nc-Si:H (2J) and SHJ/nc-Si:H/a-Si:H (3J) multijunction devices are presented in Figure 2A,B. The  $J_{\text{sc}}$  of the nc-Si:H subcell shows the expected increases with nc-Si:H thickness ( $d_{\text{nc-Si}}$ ). For the 1J and 2J devices, where the nc-Si:H subcell is positioned at the front of the device, the increase follows an exponential decay, as described by the Lambert-Beer law. The  $J_{\text{sc}}$ 's of the 1J and 2J devices are roughly similar, as the 1J devices are processed on transparent substrates, which means neither device has a back reflector positioned at the rear of the nc-Si:H junction. The EQE s of Figure 2C show that the increase in  $J_{\text{sc}}$  is a result of increased absorption in the 600 nm–1050 nm wavelength region, where the photon energy is closer to the bandgap energy of the nc-Si:H absorber and the absorption probability is lower. The same effect can be observed in the EQE s of the 2J device, in Figure 2D, where it can

additionally be observed that the increased absorption in the nc-Si:H subcell results in a decrease of the *EQE* in the bottom junction in the same wavelength region. This is reflected in the  $J_{sc}$ 's of the 2J and 3J devices, where the  $J_{sc}$  increase in the nc-Si:H subcell results in a  $J_{sc}$  decrease in the SHJ. The sum of the  $J_{sc}$ 's remains relatively unchanged. The fact that the total current density of the 2J devices exceeds that of the 3J devices will be addressed in Section 3.2.

The  $V_{oc} \cdot FF$  decreases continuously with increasing  $d_{nc-Si}$  for the 1J and 3J devices. For the single junctions, this predominantly seems to be a result of  $R_{sh}$ , which continuously decreases from  $5300 \Omega \text{ m}^2$  to just under  $2000 \Omega \text{ m}^2$ . The  $V_{oc} \cdot FF$  trends observed in the multijunction devices are the results of a subtle interplay between the single junction effects and the current matching conditions between the individual junctions. Under perfect current matching conditions, simplistically, the  $FF$  can be understood to be a result of the collective resistances in the different junctions (p-(i)-n junctions, tunneling junctions and metal-semiconductor junctions) and the  $FF$  can be expected not to exceed that of its constituent junctions. However, in the case of a current mismatch this does not hold. The influence of the current matching conditions, specifically the influence of the magnitude of the current mismatch on the  $FF$ , is exemplified by the  $>80\%$   $FF$  of the 3J devices. This  $FF$  is achieved despite the fact that the initial  $FF$  of world-record a-Si:H devices is around 76%.<sup>26,27</sup> This is because the current limiting junction has a dominant influence on the  $FF$  of the overall device.<sup>4</sup> Moreover, the  $FF$  generally increases with increasing current mismatch between subcells.<sup>4,28</sup>

Such current matching related  $FF$  effects cause the  $V_{oc} \cdot FF$  trend to deviate from the near linear-relation observed in the 1J device. For both multijunction configurations, the nc-Si:H junction is current limiting for the smallest values for  $d_{nc-Si}$ . As  $d_{nc-Si}$  is increased, the SHJ in the tandem configuration and the a-Si:H junction in the 3J configuration become current limiting. In the 3J the  $FF$  continues to decrease with  $d_{nc-Si}$ , as the current mismatch between subcells decreases and the a-Si:H subcell, with the poorest  $FF$ , becomes current limiting. In the tandem configuration, the  $FF$  increases with a  $d_{nc-Si}$  increase from 2.5 to 4.5  $\mu\text{m}$ , as the current mismatch increases and the SHJ, the subcell with the highest  $FF$ , becomes the current limiting junction. At the same time, the  $V_{oc}$  continuously decreases with increasing  $d_{nc-Si}$ .

Qualitatively, the collective trends in Figure 2 suggest some design trends for the multijunction devices as a function of  $d_{nc-Si}$ . Most of the gains in  $J_{sc}$  are realized in the  $d_{nc-Si} \leq 3 \mu\text{m}$  range, while for  $d_{nc-Si} > 4 \mu\text{m}$  the gain in  $J_{sc}$  is minimal. Consequently, considering the  $V_{oc} \cdot FF$  trend of the 1J device,  $d_{nc-Si}$  should be kept  $\leq 4 \mu\text{m}$  and preferably even  $\leq 3 \mu\text{m}$ . Additionally, intentionally introducing a (small) current mismatch in which the junction with the highest  $FF$  is limiting can, in reference to a current matched design, positively affect overall device performance.

Quantitatively, the trade-off between voltage and current as a function of  $d_{nc-Si}$  can also be expressed. In Table 2, the device characteristics of the devices with the smallest  $d_{nc-Si}$  are compared with the devices with an additional  $\approx 2 \mu\text{m}$ . For the 3J, the devices with 3  $\mu\text{m}$  and 5  $\mu\text{m}$  are compared, as the device with  $d_{nc-Si} = 4.5 \mu\text{m}$  did not result in a successful deposition.

The trade-offs in the 1J and 2J devices, both with the nc-Si:H junction positioned at the front, are remarkably similar. Roughly, starting with  $d_{nc-Si} = 2\text{--}2.2 \mu\text{m}$ , the  $J_{sc}$  increase is about 19.1–20.5%, and the  $V_{oc}$  loss is about 11.7–13.8 mV per additional  $\mu\text{m}$   $d_{nc-Si}$ . Similarly, for the 3J, an increase of 2  $\mu\text{m}$ , from  $d_{nc-Si} = 3 \mu\text{m}$  to 5  $\mu\text{m}$ , result in a  $J_{sc}$  increase of 19.1%. The  $V_{oc}$  is decreased by 16.4 mV per additional  $\mu\text{m}$   $d_{nc-Si}$  in the 2.5 to 5  $\mu\text{m}$  range. Additionally, the results from Table 2 suggest that the highest conversion efficiencies are generally achieved for small  $d_{nc-Si}$ .

### 3.2 | SiOx:H based intermediate reflective layer

In the preceding section the attractiveness of an intermediate reflective layer, which could potentially yield an increase in  $J_{sc}$  without a (significant) decrease in  $V_{oc} \cdot FF$ , is demonstrated. In this section the effectiveness of an silicon-oxide based IRL is investigated.

In Figure 3B, the  $J_{sc}$  of the nc-Si:H junctions are shown to increase with increasing  $d_{n-SiOx}$ , for both the 2J and 3J series, while the  $J_{sc}$  of the SHJ decreases. The *EQE* curves of the 2J and 3J series, in Figure 3D,E, indicate that this is a result of an absorption shift from the SHJ to the nc-Si:H junction in the 650–900 nm wavelength region, as reflection at the nc-Si:H/SHJ interface is increased with increasing

**TABLE 2** External device characteristics of 1J, 2J, and 3J devices with an  $d_{nc-Si}$  difference of  $\approx 2 \mu\text{m}$

	1J		2J		3J	
$d_{nc-Si}$ ( $\mu\text{m}$ )	2	4	2.2	4.4	3	5
$V_{oc}$ (mV)	512	489	1121	1092	1983	1983
$FF$ (%)	67.1	61.3	75.4	75	80.8	76.6
$J_{sc}$ ( $\text{mA} \cdot \text{cm}^{-2}$ )	17.1	20.4	16	19.3	9.1	10.9
$\eta$ (%)	5.88	6.11	13.5	12.3	14.6	12.6
$\Delta V_{oc}$ (mV)		−23.4		−29.6		−41.4 <sup>a</sup>
$\Delta J_{sc}$ (%)		19.3		20.5		19.1

Note:  $\Delta V_{oc}$  and  $\Delta J_{sc}$  indicate the change in  $V_{oc}$  and  $J_{sc}$ , respectively, for the  $d_{nc-Si} \approx 2 \mu\text{m}$  increase.

<sup>a</sup>For the 3J- $\Delta V_{oc}$ ,  $d_{nc-Si} = 2.2 \mu\text{m}$  and  $d_{nc-Si} = 5 \mu\text{m}$  are used, as the  $V_{oc}$  of  $d_{nc-Si} = 3 \mu\text{m}$  was not indicative of the overall trend.



$d_{n\text{-SiO}_x}$ . Note that the green and blue curves in Figure 3E largely overlap. This absorption shift is in line with earlier reports.<sup>5,7,9,13</sup>

Interpretation of the  $V_{oc} \cdot FF$ , in Figure 3A, is less straightforward. The n-nc-SiO<sub>x</sub>:H layer is not exclusively an IRL, but also the n-layer in both an n-i-p subcell and p-n tunnel recombination junction. As a consequence, there are a large number of complex mechanisms involved that can have competing effects on the  $V_{oc}$  and  $FF$  of the overall device, as a function of  $d_{n\text{-SiO}_x}$ . A detailed description of the relevant mechanisms that can influence the  $V_{oc} \cdot FF$ , as a function of variations in a doped layer in Si-based multijunction devices, can be found in our earlier work.<sup>15</sup>

The observed  $V_{oc} \cdot FF$  trends can approximately be divided into three regions. Initially, for  $d_{n\text{-SiO}_x} \leq 30$  nm the  $V_{oc} \cdot FF$  increases with increasing  $d_{n\text{-SiO}_x}$ . This is likely the result of the increased  $R_{sh}$  in this range, independent of  $J_{sc}$ -mismatch, as the hole barrier functionality of the n-layer is improved with  $d_{n\text{-SiO}_x}$ . A similar "minimum-thickness-requirement" has been observed in p-nc-SiO<sub>x</sub>:H layers in TRJs in silicon based multijunction devices.<sup>15</sup> Such an effect is in line with the observed  $EQE$ , and  $J_{sc\text{-sum}}$ , increase for the 2J device from  $d_{n\text{-SiO}_x} = 10\text{--}20$  nm. It should be noted that  $R_s$  and  $R_{sh}$ , that directly influence the  $FF$ , do not directly influence the  $EQE$ , which is measured under short circuit conditions. However, if the underlying mechanisms that causes the resistances to deteriorate introduces a barrier against charge carrier collection, this mechanism then can limit both the  $EQE$  and  $J_{sc}$  as well as influence the  $FF$ .<sup>15</sup>

Notably, the initial  $V_{oc} \cdot FF$  increase for  $d_{n\text{-SiO}_x} \leq 30$  nm is consistent with two separate series of nc-Si:H/a-SiGe:H and nc-Si:H/a-Si:H tandem devices, processed at the same time undergoing the same change in  $d_{n\text{-SiO}_x}$  and exhibiting no significant change in current matching conditions. These two series also exhibit an optimum  $V_{oc} \cdot FF$  in 20–35 nm range, as shown in Figure 3F.

Following this initial increase of  $V_{oc} \cdot FF$ , a steep drop occurs for both devices in the  $d_{n\text{-SiO}_x} = 30\text{--}40$  nm range. This drop is predominantly  $FF$  related, caused by a sudden increase of  $R_s$  of about 50%. The origin of this  $R_s$  increase is not entirely clear.

Finally, for  $d_{n\text{-SiO}_x} \geq 40$  nm, the  $V_{oc} \cdot FF$  is observed to slightly increase again. It should be noted that in this range, for the 2J and 3J devices, the  $V_{oc}$  and  $FF$  trends are in competition. The  $V_{oc}$  decreases continuously, likely as a result of an increased resistance against carrier movement through the thicker n-SiO<sub>x</sub>:H layer. This can also be observed in the aforementioned nc-Si:H/a-SiGe:H and nc-Si:H/a-Si:H devices, for which  $R_s$  increases continuously with  $d_{n\text{-SiO}_x}$ , as shown in Figure 3G. For the 2J and 3J devices,  $FF$  increases in this range, likely as a result of the increased current mismatch.

Qualitatively, the observed trends can be translated into two distinct design rules. The  $J_{sc}$ 's of the subcells show that varying  $d_{n\text{-SiO}_x}$  is an effective means of transferring current between sub cells. The collective results suggest that for optimal  $V_{oc} \cdot FF$  a minimal  $d_{n\text{-SiO}_x}$  is required in the range of 20–30 nm. A further increase of  $d_{n\text{-SiO}_x}$  results in a trade-off between  $J_{sc}$  and  $V_{oc} \cdot FF$ , although this effect can be mitigated to some extent when the current matching conditions are taken into account during device design. For this reason, quantifying this trade-off for  $d_{n\text{-SiO}_x} > 20$  nm is challenging. Keeping that in mind, increasing  $d_{n\text{-SiO}_x}$  from 30 to 60 nm for the 2J and 3J devices, for

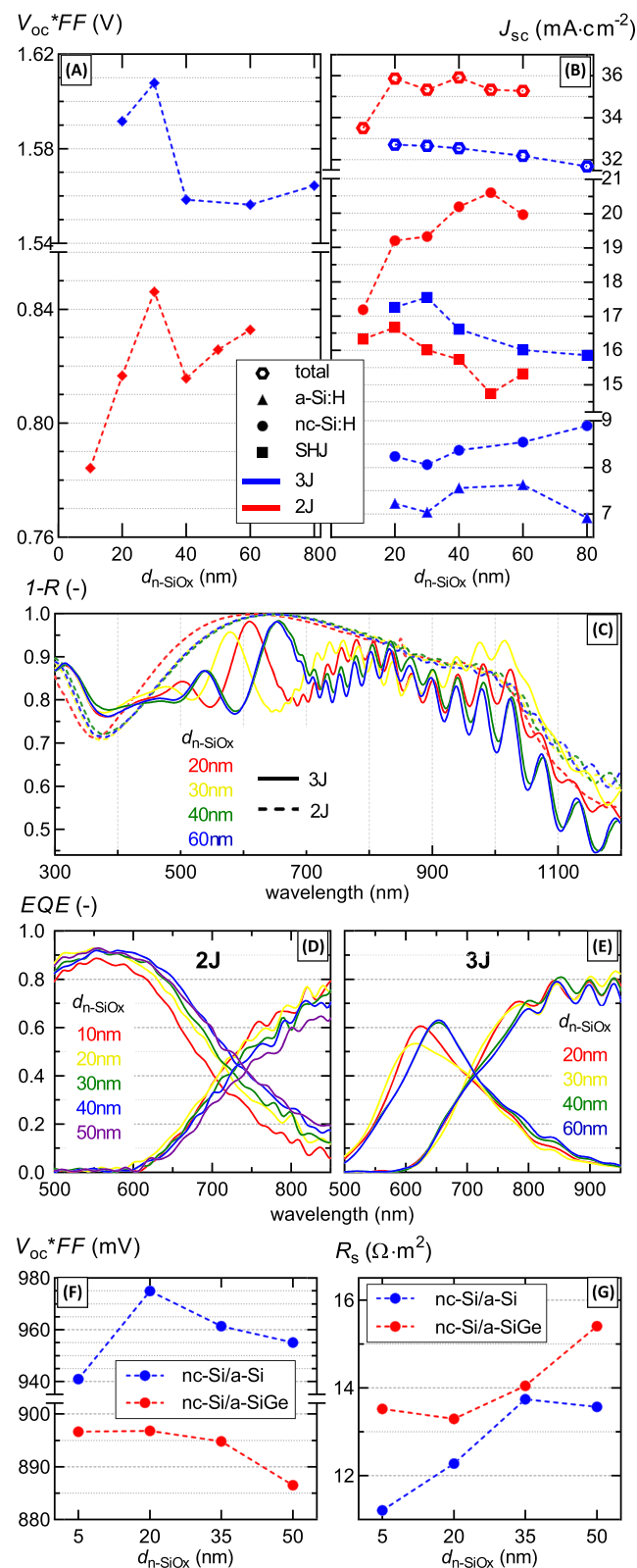
instance, result in a  $J_{sc}$  increase in the nc-Si:H subcell of 2.8–5.6% and a  $V_{oc} \cdot FF$  decrease of 13–51 mV. For the nc-Si:H/a-Si:H and nc-Si:H/a-SiGe:H devices of Figure 3F, this decrease is 14–20 mV for an  $d_{n\text{-SiO}_x}$  increase from 20–50 nm.

An additional observation can be made regarding the  $J_{sc}$ 's of the devices presented in Figure 3B. The  $J_{sc\text{-sum}}$  of the 3J devices is about  $3\text{ mA} \cdot \text{cm}^{-2}$  lower with respect to the 2J devices. This same difference is observed in the multijunction devices with different  $d_{nc\text{Si}}$  and IRLs. Reflectance measurements presented Figure 3C, in which the front reflection of 2J and 3J devices is plotted as a function of  $d_{n\text{-SiO}_x}$ , show that this  $J_{sc}$  loss is mainly an optical effect. With the introduction of the a-Si:H junction, given the typical layer thicknesses and the fact that no optimization has been performed regarding front-side anti-reflection, strong interference effects occur. These interference effects lead to the observed  $J_{sc\text{-sum}}$  loss in the 3J devices in reference to the 2J devices.

### 3.3 | TCO based intermediate reflective layer

Next, the use of a TCO as an IRL is investigated. If we consider Figure 4B, an increase of  $d_{TCO}$  does not show the expected  $J_{sc}$  increase in the nc-Si:H junction, despite a  $J_{sc}$  decrease in the SHJ for both the 2J and 3J series. The  $EQE$  curves in Figure 4C provide more insight. It seems that with increasing  $d_{TCO}$  the reflection by the IRL does increase, as absorption in the 680–820 nm wavelength range is shifted from the SHJ to the nc-Si:H. However, the overall  $EQE$  of the nc-Si:H junction is decreased. The  $EQE$  spectra of the three individual subcells, as well as the sum of the 3  $EQE$ 's and 1-R curve, of a 3J device with (Figure 4E) and without (Figure 4F) TCO as an IRL are plotted. The difference between 1-R and  $EQE\text{-sum}$  in the 650–1050 nm is minimal for the device without TCO and significant for the device with TCO.

The difference between 1-R and  $EQE\text{-sum}$  is a result of either parasitic absorption in the TCO layer, or a reduced collection efficiency resulting from the TCO introduction. A reduced collection efficiency seems most likely, since: 1. The TCO is positioned between the nc-Si:H junction and SHJ, which means it is unlikely the parasitic absorption in the TCO would significantly reduce absorption in the nc-Si:H junction, which is positioned before the TCO layer in reference to the incident light. 2. The uniform  $EQE$  decrease of  $\approx 0.2$  occurs over the entire 650–1050 nm wavelength region, where the nc-Si:H and SHJ are absorbing, is consistent with effects observed in tandems devices with a collection barrier introduced by a poorly performing TRJ.<sup>15</sup> 3. An electrical barrier against charge carrier collection is consistent with the deterioration of the electrical device characteristics observed in Figure 4A with TCO introduction. This  $V_{oc} \cdot FF$  decrease is predominantly the result of a strong decrease of the  $R_{sh}$  with increasing  $d_{TCO}$ . Figure 4D shows that the  $R_{sh}$  decreased irrespective of whether ITO, room temperature IWO or AZO was used. Moreover, the low  $R_{sh}$  persists even when shunting paths at the edges of the substrate were eliminated, through additional masking steps or by physically isolating the cell from the edges by cutting the wafer.



**FIGURE 3** Multijunction device characteristics as a function of  $d_{n-SiOx}$ . (A) The  $V_{oc} * FF$ . (B) The  $J_{sc}$  of all the individual junctions as well as the total  $J_{sc}$ -sum of the individual subcells for the 2J and 3J devices, as obtained from EQE. The 1-R curves of the 2J and 3J devices are presented in (C). The relevant spectral ranges of EQE diagrams of the 2J and 3J devices, including only the nc-Si:H junction and SHJ, are presented in (D)-(E). The  $V_{oc} * FF$  and  $R_s$  of two separate series of tandem devices, based on nc-Si:H/a-Si:H and nc-Si:H/a-SiGe:H device architectures, are shown in (F)-(G)

As the use of a TCO does not result in the desired transfer of current transfer between subcells, and the  $V_{oc} * FF$  deteriorates when a TCO is introduced, the use of a TCO as an IRL in these monolithically integrated silicon-based multijunction devices does not appear to be a desirable option.

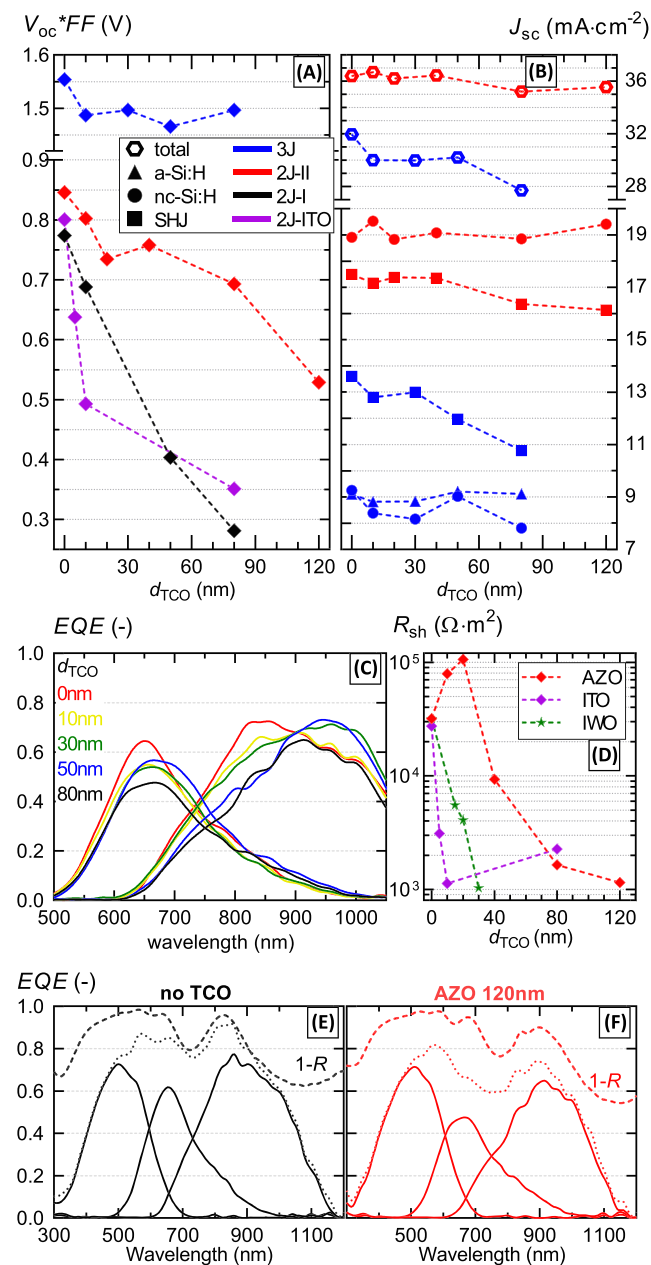
### 3.4 | Silver based intermediate reflective layer

Finally, the use of a thin metallic layer as an IRL is considered. Ag is used for its favorable reflective and conductive properties. From Figure 5A,B, two things are apparent. First, for both series the  $V_{oc} * FF$  have clear optimum for  $d_{Ag} = 2-3$  nm. This is predominantly a result of a strong increase of  $R_{sh}$  for very thin Ag layers up to 2–3 nm. Following this initial improvement, the  $V_{oc} * FF$  decreases continuously. Second, the introduction of a thin silver film does not result in the desired shift of current from the SHJ to the nc-Si:H subcell. In fact, with increasing  $d_{Ag}$ , the  $J_{sc}$  of the SHJ strongly decreases, while the  $J_{sc}$  of the nc-Si:H subcell remains relatively constant, resulting in a strong decrease of  $J_{sc}$ -sum. Figure 5C shows that this is a result of an overall decrease of the EQE of the SHJ with  $d_{Ag}$ .

Both these effects are related to the Ag growth. At the low intended thicknesses considered in this section, the Ag does not result in the formation of a uniform layer. Rather, Ag clusters are formed as can be observed in the SEM images in Figure 6. As a consequence, the reported thickness in this section are intended thicknesses. The factual average diameter ( $D$ ), and standard deviation, of these clusters are indicated in Figure 6. As a consequence of the size and shape of the Ag nanoparticles, plasmonic resonance occurs. The SEM images in Figure 6 indicate that with increasing  $d_{Ag}$ ,  $D$  increases and the particles become more ellipsoidal. This observation serves as an explanation for a number of the trends observed in the multijunction device characteristics.

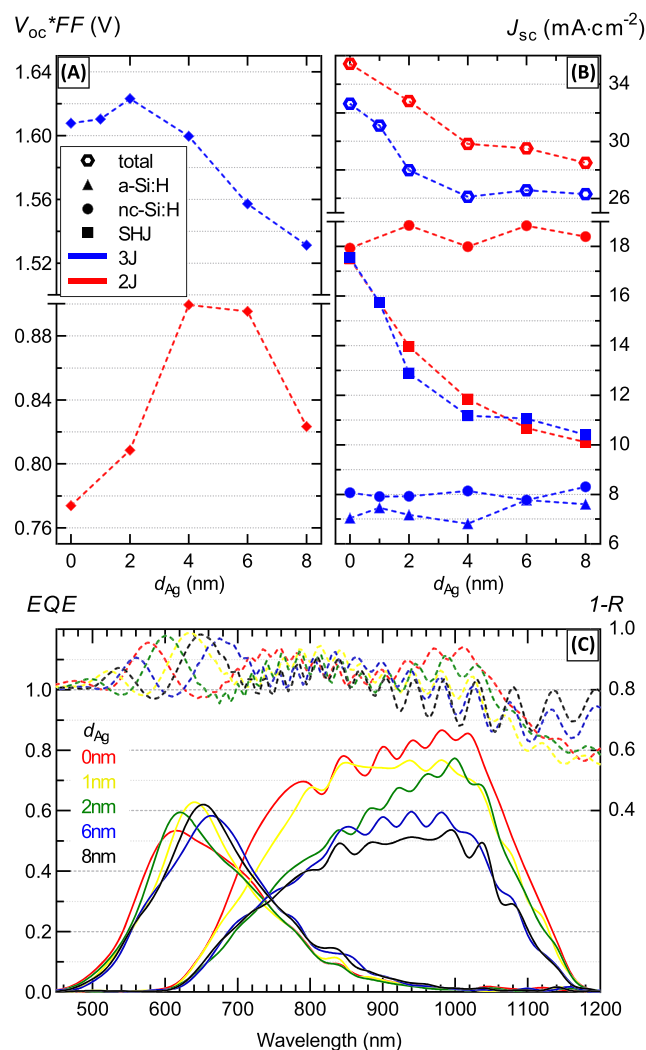
For one, the plasmon resonance, so the position of maximum attenuation, is shifted to higher wavelengths with increasing  $D$ .<sup>29-31</sup> This red-shift reportedly also occurs for increasingly ellipsoidally shaped Ag nanoparticles.<sup>32,33</sup> The absorption peak in the EQE plot of the nc-Si:H subcell in Figure 5C is observed to red-shift with increasing  $d_{Ag}$ . The 1-R inset shows that the shift of the EQE peak directly corresponds to a shift of reflection with  $d_{Ag}$ .

Additionally, considering the overall quantum efficiency decrease of the SHJ with  $d_{Ag}$ . A similar decrease has been observed before in the long-wavelength range for cells containing small nanoparticles.<sup>34</sup>



**FIGURE 4** Multijunction device characteristics as a function of  $d_{TCO}$ . (A) The  $V_{oc} * FF$ . (B) The  $J_{sc}$  of all the individual junctions as well as the total  $J_{sc}$ -sum of the individual subcells for the 2J and 3J devices, as obtained from EQE. The EQE diagram of the 3J devices, including only the nc-Si:H junction and SHJ, are presented in (C). The shunt resistance of three series of 2J devices, using an ITO, IWO and AZO IRL, are presented in (D). An EQE diagram of a 3J device, including all three subcells as well as the sum of three subcells (dotted line) and 1-R curve dashed line, is presented with (F) and without (E) TCO used as an IRL

The decrease can be attributed to reflection changes only to a small extent, as can be observed in Figure 5C. However, in the 750–950 nm wavelength range, 1-R values are roughly similar, while the quantum efficiency for devices with  $d_{Ag} \geq 2$  nm is significantly reduced. The



**FIGURE 5** Multijunction device characteristics as a function of  $d_{Ag}$ . (A) The  $V_{oc} * FF$ . (B) The  $J_{sc}$  of all the individual junctions as well as the total  $J_{sc}$ -sum of the individual subcells for the 2J and 3J devices, as obtained from EQE. The EQE diagram of the 3J devices, including only the nc-Si:H junction and SHJ, are presented in (C). The inset in (C) shows the 1-R curves of the 3J for the low-wavelength range

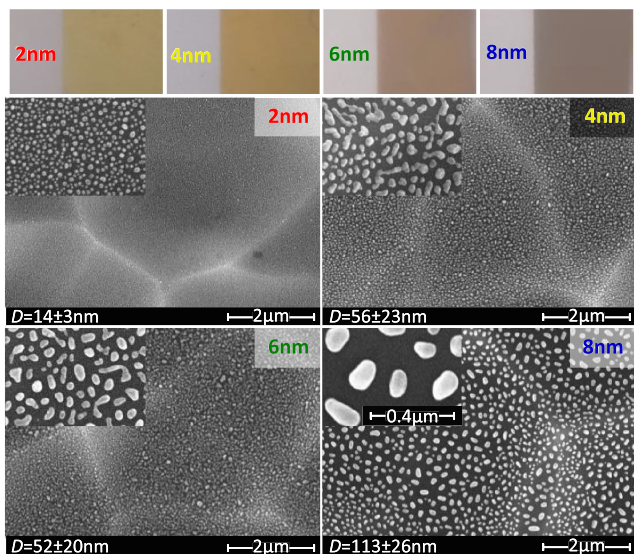
decrease therefore is a result of either increased parasitic absorption, or decreased collection efficiency as a function of increasing  $d_{Ag}$ .

Most likely both effects have an influence on the observed device performance. It is widely reported that the scattering cross section in reference to the absorption cross section of the Ag nanoparticles increases with increasing  $D$ .<sup>30,31,33,35</sup> A strong decrease of the optical transparency can also be observed for the thin Ag films on glass in Figure 6. Given these reports and the average particle size shown in Figure 6, the nanoparticles will cause significant parasitic absorption in our devices. A decrease of the collection efficiency, on the other hand, is also likely considering both the strong decrease of the  $V_{oc} * FF$  in the  $d_{Ag} = 4$ –8 nm range as well as earlier reports of a FF decreases in thin films silicon devices with increasing Ag nanoparticle size.<sup>31,33</sup> The mechanism through which the larger nanoparticles introduce the



observed decrease in  $FF$  and collection efficiency is not entirely clear. The Ag particles could negatively affect the subsequent growth of the doped and intrinsic layers, which were not optimized to facilitate particles of such size. Alternatively, considering the decrease of  $R_{sh}$ , the large particles could create additional shunting paths. This could occur either through an increase of the average lateral conductivity, facilitating the connection of spatially distributed shunting paths, or through the creation of new shunting paths.

Regardless of the mechanisms involved, the design rules resulting from the experiments presented in this section are straightforward. Introduction of a thin Ag layer does not result in the desired IRL functionality. However, evidently, a TRJ-functionality could potentially be improved, realizing a  $V_{oc} \cdot FF$  increase, by the introduction of a very thin Ag film, at the cost of current generation in the junctions positioned at the back of the device.



**FIGURE 6** Optical images (top) of Ag on glass for different  $d_{Ag}$ . SEM images of Ag on textured Si wafers for different  $d_{Ag}$ . Insets show SEM images at different magnification, as indicated by the scale in the bottom-right inset. The average nanoparticle diameter ( $D$ ) and standard deviation are indicated at the bottom of the SEM images

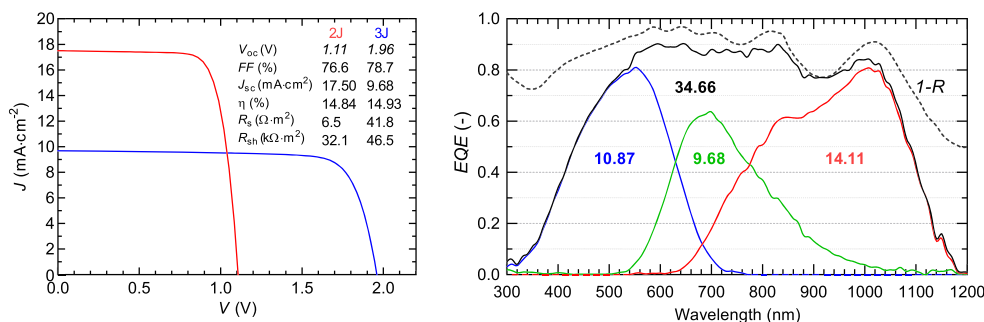
### 3.5 | Champion autonomous high-voltage device

Finally, several 2J and 3J devices were processed with high voltage and champion conversion efficiency. The  $J$ - $V$  curves of the 2J and 3J devices with the highest conversion efficiency, as well as the EQE curves of the 3J device are presented in Figure 7. Excellent  $FF$ 's in the range of 76–79% and  $V_{oc}$ 's of over 1.1V and close to 2V are realized for the 2J and 3J devices, respectively. An  $SiO_x$ -based IRL was applied at the interface between the SHJ and nc-Si:H junction, with  $d_{n-SiO_x} = 40$  nm. The suboptimal  $V_{oc}$  of the champion 3J device in Figure 7 is the result of a relatively thick wafer and relatively thick absorbers in the range of  $d_{a-Si} \approx 350$  nm and  $d_{nc-Si} \approx 4 \mu\text{m}$ .

The sum of the  $J_{sc}$ 's of the individual junctions of the 2J device is around  $36 \text{ mA} \cdot \text{cm}^{-2}$ . For the 2J device, the nc-Si:H junction is current limiting with a  $J_{sc}$  of  $17.50 \text{ mA} \cdot \text{cm}^{-2}$ . In the triple junction device, the nc-Si:H junction is also current limiting with a  $J_{sc}$  of  $9.68 \text{ mA} \cdot \text{cm}^{-2}$ . This results in conversion efficiencies in the range of  $\eta = 14.84$ – $14.93\%$ . The conversion efficiency of 14.93% is a strong improvement over earlier reported conversion efficiencies of 10.5%<sup>19</sup> and 12.7%<sup>20</sup> for such hybrid 3J c-Si/nc-Si:H/a-Si:H devices that can be used for autonomous solar-to-fuel applications. In fact, to the best of the authors knowledge, it is the highest reported conversion efficiency for an all-silicon solar cell that generates at least 1V, for which the record initial efficiency is in the range of 14.3–14.8%.<sup>36,37</sup> Note that this excludes the 3J device from United solar, which has an alloyed SiGe:H absorber.<sup>38</sup>

Finally, considering the collective results presented in this work, we can reflect on the potential of the c-Si/nc-Si:H/a-Si:H multijunction device. Regarding the  $V_{oc}$ , the best  $V_{oc}$ 's recently achieved by the authors for single junction devices is around 700 mV for the SHJ, 510 mV for the nc-Si:H junction and 910 mV for the a-Si:H junction, while using transparent rear-electrodes for the nc-Si:H and a-Si:H devices. The sum of the  $V_{oc}$ 's is round 2.13 V. Considering a voltage loss of around 15 mV per TRJ, a number that can be considered a realistic voltage drop for a well engineered TRJ<sup>39</sup> but that does not take into account concessions in  $d_{nc-Si}$  or  $d_{n-SiO_x}$  that might be required for current matching, a  $V_{oc}$  of 2.1V could realistically be achieved. In fact, among the champion devices processed a 3J was realized with  $V_{oc} = 2.04$  V and a  $FF$  80% for which unfortunately, due to technical difficulties, no EQE measurements could be obtained. Such 3J devices with  $V_{oc} \cdot FF > 1.6$  are also presented in Figures 2 and 5. Moreover, the

**FIGURE 7** The  $J$ - $V$  and EQE curves of the champion 2J and 3J devices. An EQE diagram of the champion device, including all three subcells as well as the sum of three subcells and 1-R curves dashed line is presented



$EQE$  s of the individual junctions in Figure 7 show that the photo-generated current density is not evenly distributed among the different junctions. Additionally, a large optical loss in the blue part of the spectrum in the 300–500 nm wavelength region. The 1-R curve, and the difference between the  $EQE_{sum}$  curve and the 1-R curve, indicates this to be a result of both relatively high front reflection as well as parasitic absorption losses, presumably in the front TCO and p-doped window layer. Further optimization of these layers in combination with the use of an anti-reflection coating, as well as improved current matching, could yield a current limiting  $J_{sc}$  in the range of 11–12 mA·cm<sup>-2</sup>. Therefore, with further optimization, a hybrid all-silicon SHJ/nc-Si:H/a-Si:H 3J device with  $V_{oc} > 2V$  and  $\eta > 18\%$  could realistically be achieved.

## 4 | CONCLUSION

In this work, the results of over 65 silicon-based multijunction photovoltaic devices are presented, with the purpose to explore different current matching approaches. The influence of absorber thickness as well as the thickness of different intermediate reflective layers, based on silicon-oxide, various TCOs and Ag, on the tandem SHJ/nc-Si:H and triple junction SHJ/nc-Si:H/a-Si:H device performance was characterized. Based on these experiments certain design rules can be formulated.

An increase of the nc-Si:H absorber thickness results in a continuous decrease of  $V_{oc} \cdot FF$ , while gains in  $J_{sc}$  are predominantly realized in the  $d_{nc-Si} \leq 3 \mu m$  range. Consequently, it would be advisable to keep  $d_{nc-Si} \leq 4-3 \mu m$ . Of the different IRLs, only the silicon-oxide based IRL resulted in the desired absorption shift from the SHJ to the nc-Si:H junction. For the TCO and Ag based IRLs no current gain was observed in the nc-Si:H junction, as the increased reflection by the IRL was counter-acted by a decreased charge carrier collection efficiency. However, for a very thin Ag IRL, an increase of  $V_{oc} \cdot FF$  was realized for the multijunction devices, at the cost of  $J_{sc}$  in the SHJ. Additionally, it was observed that the  $FF$  is strongly influenced by the current matching conditions. For optimal device performance, it would be advisable to intentionally introduce a minor current mismatch in which the junction with the highest  $FF$  is current limiting.

Finally, taking these design rules into account, champion devices were processed. For the triple junction SHJ/nc-Si:H/a-Si:H device a  $V_{oc} \approx 2V$  and  $\eta \approx 15\%$  are reported, which to the best of the author's knowledge is a record for an all-silicon multijunction device. Such a conversion efficiency for a high-voltage wafer-based all-silicon 2-terminal multijunction PV device opens the way for highly efficient autonomous solar-to-fuel synthesis systems.

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## DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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## SUPPORTING INFORMATION

Additional supporting information can be found online in the Supporting Information section at the end of this article.

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