Multi-parameters optimization for electromigration in WLCSP solder bumps

Du, Leiming; Deng, Shanliang; Cui, Zhen; Poelma, René ; Beelen-Hendrikx, Caroline ; Zhang, Kouchi

DOI
10.1109/EuroSimE60745.2024.10491411

Publication date
2024

Document Version
Final published version

Published in
Proceedings of the 2024 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)

Citation (APA)
Du, L., Deng, S., Cui, Z., Poelma, R., Beelen-Hendrikx, C., & Zhang, K. (2024). Multi-parameters optimization for electromigration in WLCSP solder bumps. In *Proceedings of the 2024 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)* (2024 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2024). IEEE. https://doi.org/10.1109/EuroSimE60745.2024.10491411

2024 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE) | 979-8-3503-9363-7/24/$31.00 ©2024 IEEE | DOI: 10.1109/EuroSimE60745.2024.10491411

Multi-parameters optimization for electromigration in WLCSP solder bumps

Leiming Du[1, *], Shanliang Deng[1], Zhen Cui[1], René Poelma[1, 2], Caroline Beelen-Hendrikx[2], Kouchi Zhang[1]
[1]EEMCS Faculty, Delft University of Technology, Delft, the Netherlands
[2]Nexperia, Nijmegen, the Netherlands
*Corresponding: L.Du@tudelft.nl

Abstract

In this study, we combined finite element method (FEM) based on Ansys and Noesis Optimus software to investigate the effect of bump structures and loading conditions on the electromigration properties of solder bumps in WLCSP. A numerical model considering current density, vacancy concentration, stress and temperature was utilized to calculate the vacancy concentration in solder bumps. The Optimus is an optimization software which can be used to perform the design of experiment (DOE) and sensitivity analysis. To optimize the bump structure, the DOE and response surface modeling (RSM) analysis were performed by using Noesis Optimus. The design optimization based on Noesis Optimus has three main advantages. First, the sensitivity analysis based on DOE results helps to find the most contributing factors. Second, it saves huge time because hundreds of experiments can be executed automatically. Third, it is able to perform evolutionary design optimization directly on RSM to identify the design's optimal performance point. The maximum and concentration around solder were selected as the index to evaluate the effect of parameter combination on electromigration properties.

1. Introduction

Wafer-level chip-scale packaging (WLCSP) is a workhorse in advanced packaging, which has been used in various device applications such as smartphones, wearable devices, and modern car innovations due to its good electrical performance quality and low production cost [1]. However, with the miniaturization of microelectronic devices, electromigration (EM) in solder bumps under high current density has become a critical reliability issue for future high-density WLCSP. EM damage in solder bumps has been found to have two main effects [2]. First, copper (Cu) from substrates reacts with the Sn to create an intermetallic compound (IMC). Second, when electric current flows, it pushes both Cu and Sn atoms away from the site where the electrons enter, which can lead to the formation and growth of small voids at the interface. As the void size increases, there is an increase in electrical resistance through the joint, and eventually an open circuit occurs. A common failure mode is an electrical open due to interfacial void formation induced by IMC growth at the interface between the solder and UBM [3]. It is noted that the different solder bump structures would induce different current spreading, diffuse behaviour and failure mechanisms. A full understanding of the effect of solder bump structures on EM properties is critical for quantifying EM-induced failure in WLCSP.

Many studies have reported the EM properties of solder bumps in WLCSP by considering different bump sizes, material selection and loading conditions [4-10]. For example, Christine et al [4] studied the effect of different solder metallurgy, under bump metallurgy (UBM) thickness, and redistribution layer thickness and composition on the EM properties. It is reported that thicker UBM provides a prolonging lifetime due to the lower local joule heating and greater CuSn formation. Afterwards, Christine [5] et al. reported EM results for five types of interconnects including microbump, copper pillar, thermal compression flip chip bump, lead-free bump and solder ball. The bump diameter in their study changes from 250 μm to 20 μm. They found that the EM properties depend on the solder-Cu ratios, and the lower solder-Cu ratio presents better EM performance. Moreover, the current density and temperature will directly affect the EM performance of the solder bump, in which the faster grain growth will be caused by increasing the current density and temperature [6].

Besides the experimental studies on EM of solder bump, there are a lot of studies attempting to predict the EM failure and to evaluate the EM lifetime through modeling [11-15]. The atomic flux divergence (AFD) method and atomic density integral (ADI) based on finite element models are two main methods which are popular in industry. Cai et al [13] developed a methodology to consider the diffusion of atoms in solder joints based on Multiphysics field migration to study the current redistribution influence of vias in Ball Grid Array (BGA). The AFD method in their study was based on a fully coupled model in Ansys. Recently, phase field modelling [14, 15] was proposed to study the Cu-Sn reaction during electromigration. It was revealed that vacancy transport due to the difference in intrinsic diffusion of elements in different features of the microstructure, and the severe unidirectional convective flux of atoms due to the enforced electron wind that ultimately paves the road to study nucleation of microvoids.

The aim of this work is to investigate the effect of solder bump structure on EM reliability for solder bumps in WLCSP. FEM based on Ansys and an optimization tool named Noesis Optimus were combined to establish the RSM of EM of solder bumps. The effect of passivation opening, UBM thickness, and loading condition on the EM performance of the solder bump was revealed and optimized.

979-8-3503-9363-7/24/$31.00 ©2024 IEEE

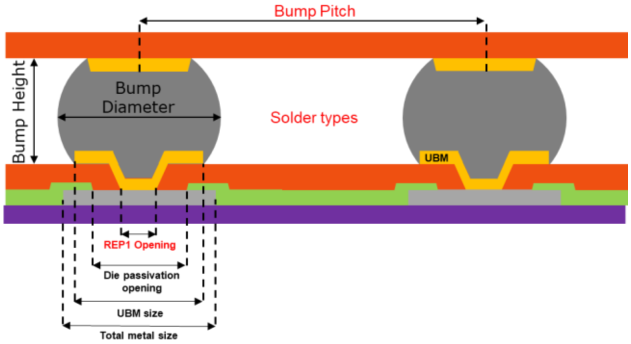


Fig. 1. Diagram of bump structure in WLCSP

2. Basic migration formulation and FEM model

Thermal, electric, stress and atomic concentration interact through the physical field sources provided by each other. In this study, the temperature gradient is ignored. Therefore, a numerical model is established for electromigration of solder joints, considering the effects of current density, stress and concentration. The atomic flux can be expressed as follows:

$$\overrightarrow{J_{Tol}} = \overrightarrow{J_{Em}} + \overrightarrow{J_S} + \overrightarrow{J_C} \qquad (1)$$

$$\overrightarrow{J_{Tol}} = \frac{cD}{kT} Z^* e \rho \vec{j} - \frac{cD}{kT} \Omega \nabla \sigma_m - D \nabla c \qquad (2)$$

where c is the atomic concentration; D is the diffusivity; k is Boltzmann's constant; T is the absolute temperature; e is the electronic charge; ρ is the resistivity which is calculated as $\rho = \rho_0(1 + \alpha(T - T_0))$, α is the temperature coefficient of the metallic material; j is the current density; D is the diffusivity; Z^* is effective charge number; Q^* is heat of transport; Ω is the atomic volume; σ_m is the local hydrostatic stress.

In this study, a double bump model is modelled in the commercial FEA software Ansys. The bottom and the top surfaces of the structure were fixed. A current of 5A is applied to the bumo structure through Cu trace for electrical connection. The temperature is set as 150°C and the total time is 1000h. The current distribution is shown in Fig. 2. It is shown that the maximum current density is located at the interface of UBM.

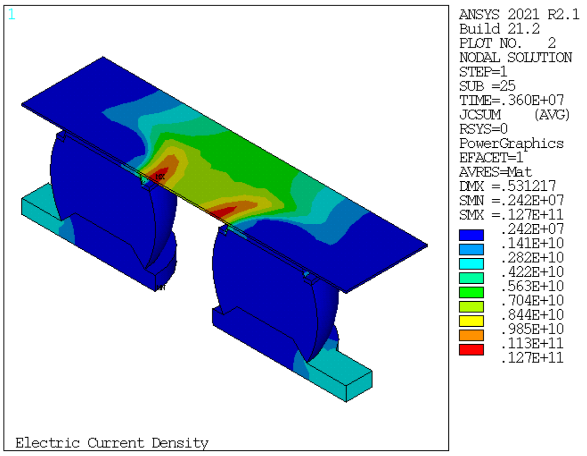


Fig. 2. Current distribution of the bump model

3. Results and Discussion

The effect of repassivation opening and UBM thickness on the EM properties were studied. It is found that both the repassivation opening and UBM thickness have a significant effect on the normalized concentration distribution. As shown in Fig. 3b, the smaller repassivation opening caused higher vacancy concentration than reference shown in Fig. 3a, which is due to the severe current crowding effect. However, the vacancy concentration decreases as the size of repassivation opening increases. It is recommended to enlarge the size of repassivation opening to reduce the earlier EM-induced failure in solder bumps in WLCSP. Fig. 3c presents the normalized concentration distribution with the thicker UBM. It is found that the maximum concentration is slightly lower than the reference shown in Fig. 3a.

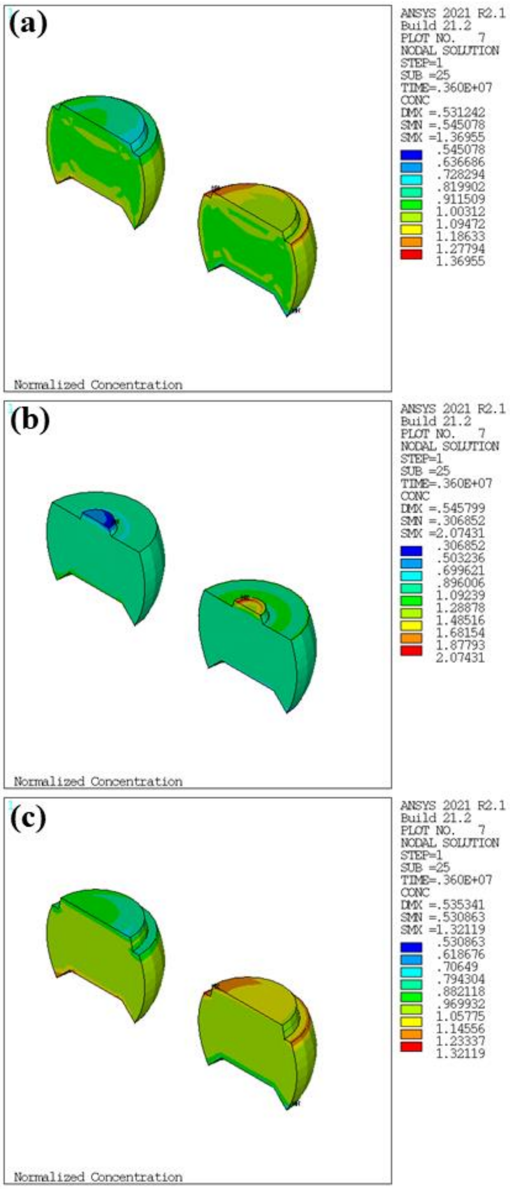
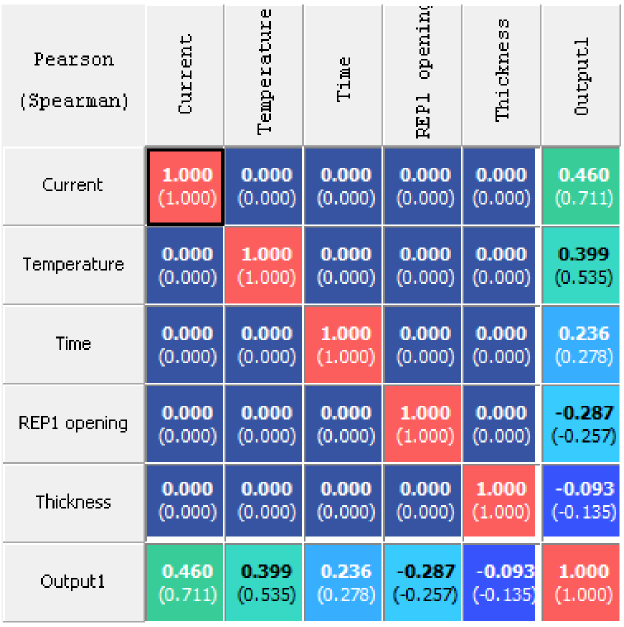


Fig. 3. Normalized concentration distribution in (a) Reference; (b) smaller repassivation; (c) thicker UBM.

To optimize the repassivation opening and the UBM thickness and perform the sensitive analysis, a DOE based on Optimus was carried out. Here, we consider the loading condition (current, temperature and time), repassivation and UBM thickness. Latin-hypercube sampling generates a set of experiments (100 groups) randomly in the design space (5 parameters), which means that 100 times of simulations were performed. The maximum concentration is selected as the index. Fig. 4 presents the table of the Pearson correlation coefficient, which is calculated based on the maximum concentration from the 100 groups of simulation. The Pearson correlation is a measure of the strength of a linear association between two variables. As shown in Fig. 4, the current, temperature, time and repassivation opening have a significant influence on the maximum concentration. While the UBM thickness has a slight influence on the maximum concentration. The results clarify that the influence sequence of individual parameters on the maximum concentration is current > temperature > repassivation opening > time >> UBM thickness. Moreover, the response surface was established as shown in Fig. 5. The repassivation opening with 160μm and the UBM thickness of 15μm will produce the smallest maximum concentration during EM. The difference between the results from the simulation and the response surface is smaller than 5%. Thus, the response surface method based on optimus and Ansys would offer a quick and reliable optimization tool for the design of bump structure.



Pearson (Spearman)	Current	Temperature	Time	REP1 opening	Thickness	Output1
Current	1.000 (1.000)	0.000 (0.000)	0.000 (0.000)	0.000 (0.000)	0.000 (0.000)	0.460 (0.711)
Temperature	0.000 (0.000)	1.000 (1.000)	0.000 (0.000)	0.000 (0.000)	0.000 (0.000)	0.399 (0.535)
Time	0.000 (0.000)	0.000 (0.000)	1.000 (1.000)	0.000 (0.000)	0.000 (0.000)	0.236 (0.278)
REP1 opening	0.000 (0.000)	0.000 (0.000)	0.000 (0.000)	1.000 (1.000)	0.000 (0.000)	-0.287 (-0.257)
Thickness	0.000 (0.000)	0.000 (0.000)	0.000 (0.000)	0.000 (0.000)	1.000 (1.000)	-0.093 (-0.135)
Output1	0.460 (0.711)	0.399 (0.535)	0.236 (0.278)	-0.287 (-0.257)	-0.093 (-0.135)	1.000 (1.000)

Fig. 4. Pearson correlation coefficient table

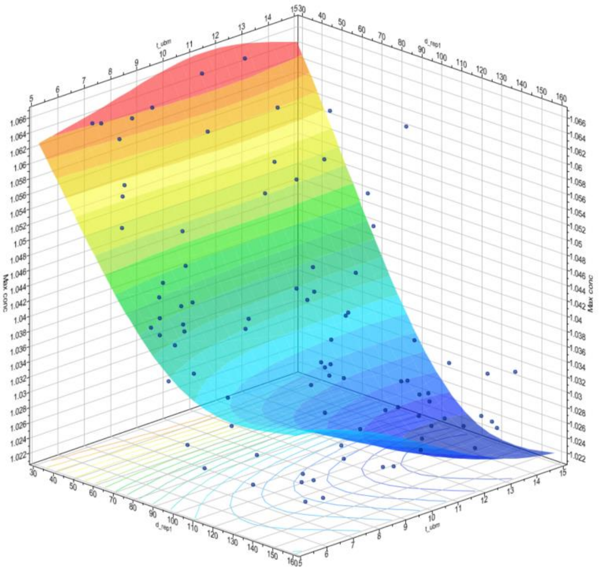


Fig. 5. Response surface of repassivation opening and UBM thickness with the maximum concentration

4. Conclusions

In this paper, the effect of repassivation opening, the ubm thickness and the loading condition (current, temperature and time) on the EM performance of solder bump was studied. A multiparameter optimization tool (Optimus) combined with Ansys was used to perform a DOE and sensitivity analysis. Results show that the influence sequence of individual parameter on the maximum concentration is current > temperature > repassivation opening > time >> UBM thickness.

Acknowledgments

This project has received funding from the Nexperia company and ECSEL Joint Undertaking (JU) under grant agreement No 876659. The JU receives support from the European Union's Horizon 2020 research and innovation program and Germany, Austria, Slovakia, Sweden, Finland, Belgium, Italy, Spain, Netherlands, Slovenia, Greece, France, Turkey.

References

1. Z. Wu et al., "Understanding and Improving Reliability for Wafer Level Chip Scale Package: A Study Based on 45nm RFSOI Technology for 5G Applications", *IEEE Journal of the Electron Devices Society* 2020, pp. 1305-1314.
2. Y.C. Chan et al, "Failure mechanisms of solder interconnects under current stressing in advanced electronic packages," *Progress in Materials Science*, Vol. 55, No. 5 (2010), pp. 428-475.
3. M.R. Jen et al, "Electromigration Test on Void Formation and Failure Mechanism of FCBGA Lead-Free Solder Joints," *IEEE Transactions on Components and Packaging Technologies*, March. 2009, pp. 79-88.

4. C. H. Riege et al, “The impact of different under bump metallurgies and redistribution layers on the electromigration of solder balls for wafer-level packaging,” *64th Electronic Components and Technology Conference (ECTC)*, May. 2014.
5. C. H. Riege et al, “Key metrics for the electromigration performance for solder and copper-based package interconnects,” *IEEE International Reliability Physics Symposium (IRPS)*, April. 2016, pp. 1938-1891.
6. F. Wang et al, “Electromigration behaviors in Sn–58Bi solder joints under different current densities and temperatures,” *Journal of Materials Science: Materials in Electronics*, Vol. 29, (2018), pp. 21157-21169.
7. X. Xu et al, “An Assessment of Electromigration in 2.5D Packaging,” *69th Electronic Components and Technology Conference (ECTC)*, May. 2019.
8. R.L.J.M. Ubachs, “Electromigration in WLCSP solder bumps,” *Microelectronics Reliability,* Vol. 50, No. 9-11, (2010), pp. 1678-1683.
9. A. Syed et al, “Electromigration reliability and current carrying capacity of various WLCSP interconnect structures,” *63rd Electronic Components and Technology Conference,* May. 2013.
10. L. Niu et al, “The Study on Electromigration of Solder Joints under Thermal Cycling Load,” *22nd International Conference on Electronic Packaging Technology (ICEPT),* Oct. 2021.
11. Y. Liu et al, “3-D modeling of electromigration combined with thermal-mechanical effect for IC device and package,” *Microelectronics Reliability*, Vol. 48, No. 6, (2008) pp. 811–824.
12. Y. Zhang, “Electromigration Failure Prediction and Reliability Evaluation of Solder Bumps for FCBGA package,” *Engineering Transactions*, Vol. 63, No. 2, (2008) pp. 215–232.
13. C. Cai et al “Electromigration Risk Assessment and Circuit Optimization using Innovative Multiphysics Modeling,” *55th International Symposium on Microelectronics*, Oct. 2022.
14. V. Attari et al “On the interfacial phase growth and vacancy evolution during accelerated electromigration in Cu/Sn/Cu microjoints,” *Acta Materialia*, Vol. 160, (2018) pp. 185–198.
15. V. Attari et al “Phase-Field Study of Thermomigration in 3-D IC Micro Interconnects,” *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Vol. 10, No. 9 (2020) pp. 1466–1473.