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Free standing interconnects for stretchable electronics

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FREE STANDING INTERCONNECTS FOR STRETCHABLE ELECTRONICS

FREE STANDING INTERCONNECTS FOR STRETCHABLE ELECTRONICS

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
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voorzitter van het College voor Promoties,
in het openbaar te verdedigen op woensdag 24 oktober 2018 om 12:30 uur.

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To my Mother and Father

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1
INTRODUCTION

In this chapter, the impact and evolution of stretchable electronics will be discussed. This fascinating and multidisciplinary area of research is based on advances in material science, unique interconnect designs, an understanding of the mechanics of stretching and in depth know how of its applications. Multiple applications, especially in the field of medical devices will be presented. Next, the literature on the most prominent existing technologies will be reviewed, followed by the motivation for this Thesis. Finally, the outline of this Thesis is presented.

1

1.1. STRETCHABLE ELECTRONICS

OVER the years electronic products have changed from bulky, space consuming equipment to smaller, lighter, thinner and portable devices. There is a constant effort to develop the best products in an ever changing market, hence new innovative ideas are being tried and tested all the time. Out of the many new technology developments, something that is catching the attention of both researchers and lay-people is the development of electronics that can be stretched. Stretchability adds a completely new feature to electronic circuits, allowing them to be applied over curved surfaces like the human body (Fig. 4.10).

The interest in stretchable electronics dates back to 1998, when researchers from Harvard University investigated the buckling phenomenon of metal thin films deposited on elastomer (polydimethylsiloxane) [2] . Some of the immediate first applications of this effect was perceived for diffraction gratings in optical devices and optical sensors. However, it was not realised then, that the buckling of the metal films would be used several years later by researchers like Stephanie Lacour [3] and John Rogers [4] for the fabrication of stretchable circuits. The definition of stretchable electronics is intuitively demonstrated by the term itself, as soft and conformable electronic systems for applications varying from healthcare to consumer lifestyle.

Stretchable electronic systems can have revolutionary implications for medical in-

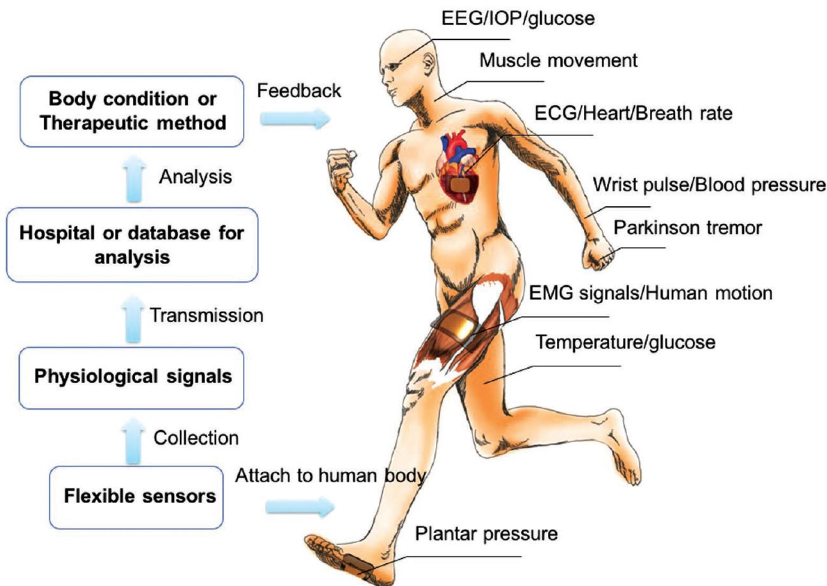

Figure 1.1: An illustration demonstrating the various wearable budy patches that can be used for measuring and further diagnosing various body parameters, without impacting the day to day lifestyle. Adapted from [1]

struments. Traditionally, rigid medical devices are being used for monitoring of bodily parameters whilst conforming to the patient in one position. In case of longer diagnosis it causes discomfort to the patient. It is envisaged that stretchable electronics will provide a platform to perform real time health monitoring without the need for a medical expert and with comfort to the patient. The monitoring of physiological parameters like blood flow, heart rate, oxygenation, blood pressure etc. has been demonstrated in the past using flexible sensors [5] [6] [7] [8]. However, in order to use these devices on more "curved" areas of the body they are required to exhibit a degree of stretchability.

1.2. IMPACT AND APPLICATIONS OF STRETCHABLE ELECTRONICS IN HEALTHCARE

1.2.1. MARKET SURVEY

An industry which is benefiting most from the research in stretchable electronics is the wearable electronics industry [9] [4] [10] [11]. Wearables electronics are defined as devices that can be applied on the body with ease and comfort. Many of them require devices which need to be in close contact with parts of the body. Depending on the body area, these devices therefore need to have some degree of stretchability in order to conform to the curvature of the human body. A study revealed that the global market for wearable devices is expected to reach a revenue of $25.19 billion by 2020, growing at a compound annual growth rate (CAGR) of about 26% (Fig. 1.2 - Frost and Sullivan, wearable report).

The global market for wearable healthcare devices is expected to reach a revenue of $18.9 billion in 2020, growing at a CAGR of about 30% (Fig. 1.2). The consumer health market, including wellness, fitness, and sport wearable segment is expected to grow at a CAGR of 27.8% (2014-2020). Medical and clinical grade wearables is the most promising product segment within healthcare wearables, and it is expected to grow with a CAGR of 32.9%.

Smart on-body conformable patches will be attractive candidates to boost the wearable healthcare market. It is envisioned that they will record a mass market proliferation in the near future due to a growing interest from end-users such as manufacturers of medical equipment, bandages and pharmaceutical companies. The market size for “traditional, non-ultra-sound” smart patches has been estimated to be in excess of $12 billion in 2015 with a CAGR of 11% (40 % North America, >25% Europe, >25% Asia Pacific). Up till now, the market segments are dominated by patches that sense: heart rate, body temperature, pressure, oxygenation, moisture, pH etc. Consolidated global market size prognoses for patches with ultra-sound sensing functionality are not available at this moment since this is basically a non-existing product. However, the expected markets predicted for such devices indicate the expected impact. A good example is bladder monitoring [12]. In the US and Europe alone, a staggering $65 billion is spend on incontinence care. A device to help juveniles train their bladder control already quickly generates a $150 million market for dedicated smart ultra-sound

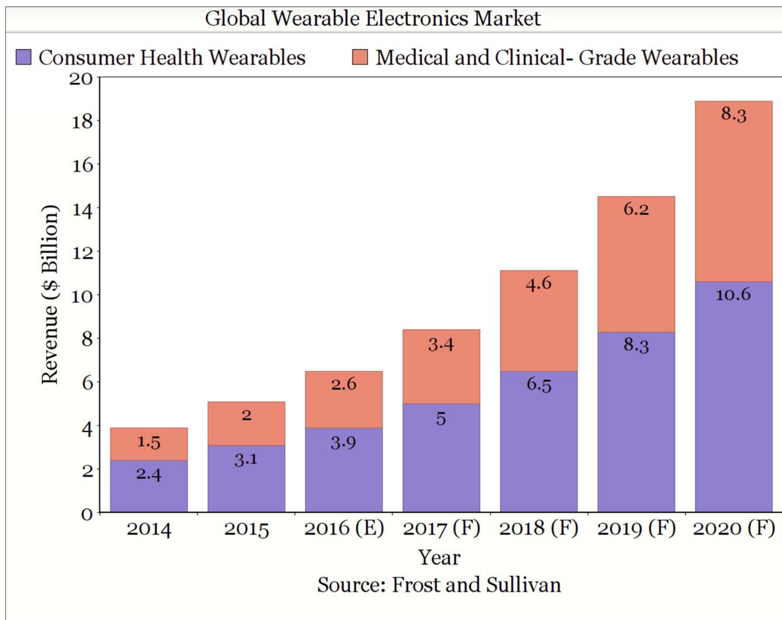

Figure 1.2: The expected growth of medical and consumer health wearables predicted with a CAGR of 26%. Source : Healthcare wearable mar*Frost and Sullivan, Wearable report, 2016.*

patches

1.2.2. ULTRASOUND APPLICATIONS

Innovations in diagnostic imaging have led to the development of the MEMS ultrasound transducers. MEMS ultrasound transducers are now leading innovation in ultrasound diagnostics. MEMS ultrasound transducers can be divided into two classes: capacitive micromachined ultrasound transducers (CMUTs) and piezo micromachined ultrasound transducers (PMUTs). PMUT devices use the flexural motion of a thin membrane coupled with a thin piezoelectric film. Whereas, CMUTs use the energy transduction due to a change in capacitance. CMUTs consist of two electrodes separated by a vacuum cavity (<1 μm). When an AC voltage is applied, the vibration of the membrane produces a sound wave. CMUTs have an advantage over PMUT's as they can be directly processed on top of CMOS application specific integrated IC's (ASIC) wafers.

There is a growing interest for the application of CMUTs in applications other than traditional diagnostic imaging. Many of them require large area ultrasound transducers that need to be in close contact with parts of the body (Fig. 1.3). Depending on the body area, these transducers therefore need to have some degree of stretchability in order to conform to the curvature of the human body. The frequency of the ultrasounds depends on the application, where lower frequencies (< 2 MHz) penetrate

deeper into the body and higher frequencies target the surface level of the body. Envisioned applications keeping these parameters in mind of ultrasound body patches are:

IMAGING

This is one of the most common applications of ultrasound, but currently the use of traditional ultrasound transducers requires the expertise of a sonographer to scan and properly interpret the image. It is envisaged that large area conformal ultrasound transducers will be able to image large parts of the body, producing detailed 3D overview images, which can be directly interpreted by the physician [14].

MONITORING

A combination of MEMS ultrasound transducers with a conformable body patch technology will bring a paradigm shift in healthcare, whereby the hospital to patient interaction will be reduced. This will not only help to reduce the healthcare cost, but also allow patients to take care of themselves. After a surgery, one of the most important and crucial follow ups is to monitor the body parameters and ensuring that they remain stable. Ultrasound body patches can be used to monitor vital body functions where the profile of a reflected ultrasound pulse, or a shift in ultrasound frequency (Doppler) is used directly to characterize the tissue or organ. Examples include: blood flow and pressure sensing, wound healing, heart rate monitoring etc. In all of these applications the body patch should be in close contact to the body; requiring it to be conformable.

THERAPY

Finally, ultrasound body patches have been proposed for different therapeutic applications including: pain relief, skincare, odor control and hyperthermia treatment [15]. Hyperthermia enhances the delivery of therapeutic agents to the tumor as well as improves tissue oxygenation, which is why it has been used as a method to treat tumors. Different strategies have been proposed to induce local, regional, and whole body hyperthermia such as: laser, radiofrequency and ultrasound radiation. Out of these, ultrasound hyperthermia therapy can be achieved using focused ultrasound transducers

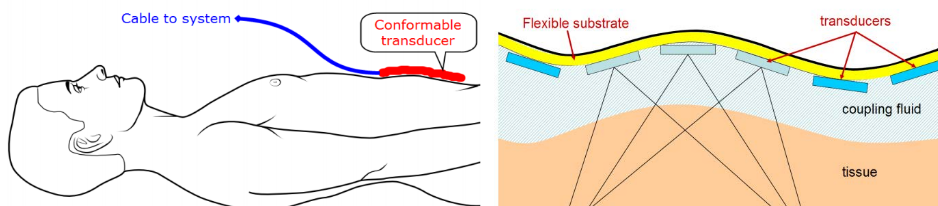

Figure 1.3: A schematic of a conformable transducer on a non- rigid human body (left). Side view of a flexible/stretchable patch with ultrasound transducers, which can be used to stitch scanned areas on a large areas of body (right). Adapted from [13]

non-invasively. These body patches will reduce the burden to the patient by allowing them to move freely around during treatment.

An imaginative example is the use of a large ultrasound phased-array for focused ultrasound stimulation through the skull [16], whereby non-invasive treatment of brain disorders were conducted with the application of ultrasound transducers on the skull while demonstrating beam steering. In this study, the transducers were individually placed at the appropriate position along with an extensive amount of wires connecting the individual devices. The complexity of such a setup can be reduced by the integration of an array of MEMS ultrasound transducers that are interconnected and conformably placed on the skull. However, in order to make such a system, the array needs to have a certain degree of stretchability. Large area stretchable electronic body patches can be of benefit for this application.

1.3. TECHNOLOGIES FOR STRETCHABLE ELECTRONICS

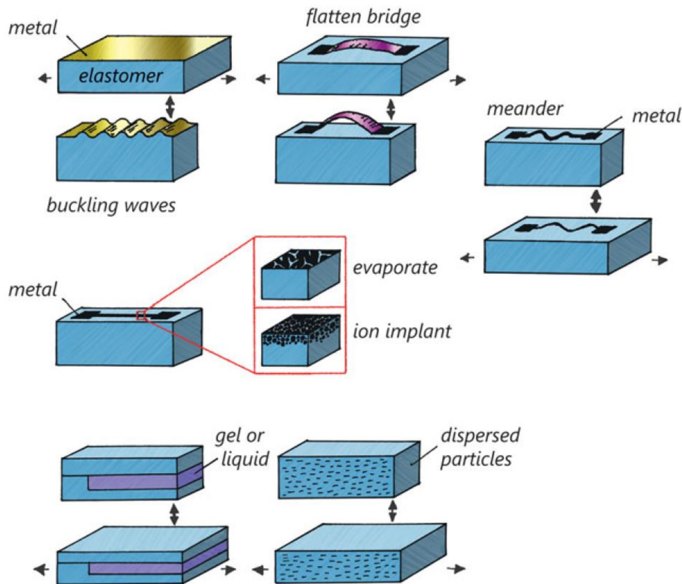

Figure 1.4: Techniques for fabricating stretchable electronics. (a) Pre-stretch elastomer approach which can be divided into two parts, one of depositing thin metal films and other using selective bonding and debonding of thin silicon or metal stripes. (b) Deposition of meander shaped metal on elastomer that can be stretched uniaxially. (c) Fabrication of stretchable conductive elastomers or inks. Source [17].

Since decades research has been conducted to develop different fabrication techniques for the realisation of stretchable electronics. Various materials and technologies have been explored, many are still in research phase while only a few are in production. Neverthless, each of these techniques is unique and have their own advantages and disadvantages. In this section, a brief review of some of the most common

technologies and materials will be presented. Figure. 1.4 by Wagner et. al. illustrates the different principles to date for the fabrication of stretchable interconnects.

1.3.1. PRE-STRETCHED ELASTOMER APPROACH

One of the methods for the fabrication of stretchable circuits is introduced by the groups of John Rogers (University of Illinois) and Stephanie Lacour (Ecole Polytechnique Fédérale de Lausanne), where they both have demonstrated the utilization of buckling of materials (Si, metal etc.) as described by Bowden et. al. on a pre stretched elastomer [2] [18] [3].

While Rogers demonstrated this by attaching thinned down Si strips on a pre stretched PDMS substrate where local adhesion sites are implemented for the adhesion of these strips on certain parts of the PDMS [19]. Upon release of the PDMS, the parts of the Si stripes that are not attached to the substrate consequently buckle out of plane. This non-linear buckling of the Si after release due to the compression stress caused by the underlying elastomeric substrate, results in a reversible uniaxial stretchability of the device. These out of plane Si "waves" act as interconnections between device components attached on top of the adhered Si notches (Fig. 1.5-b). These buckled "wavy" structures are dependent on the elastic properties of the elastomer and the thickness of the Si. Similar behavior has been demonstrated using materials like nanotubes [20], bucky gels [21] [22], inorganics nanoribbons [23] etc. on a pre stretched elastomer.

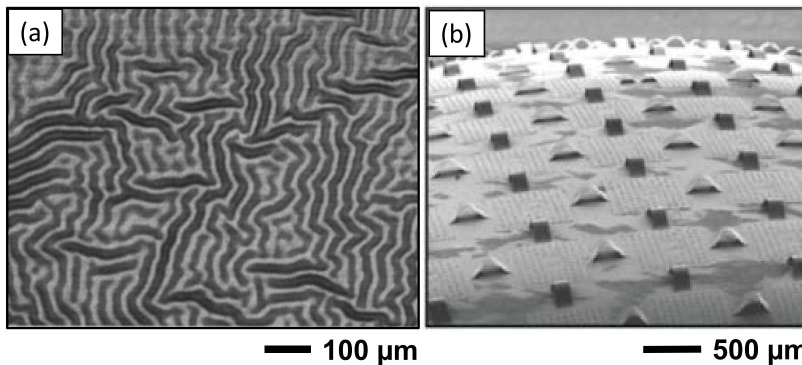

Figure 1.5: (a) SEM micrographs of gold films on relaxed PDMS substrate after their deposition on a pre-stretched substrate [18]. (b) and a magnified SEM image of the "wavy" buckled Si ribbons [3].

Stephanie Lacour demonstrated similar "wavy" behaviour using the buckling of gold metal films deposited as stripes (electron beam deposition, patterned using resist liftoff) on a pre stretched PDMS substrate (Fig. 1.5-a). The stretch of elastomer explored by their group was to a maximum of 15% before release. After the release the gold stripes formed waves/wrinkles that are stretchable and conductive uniaxially [3]. Releasing the pre-deposition stretch decreases the resistance of the patterned gold stripes, whereas stretching them again recovers the pre-stretch resistance.

Applications of such technologies are reported in electronic skins and pressure sensors [24]. Device failures utilizing this method of fabrication, is reported when the

interfacial shear forces between the devices and the substrate exceed the strength of adhesion. However, the scalability of these methods is deemed difficult and poses as a major drawback for various applications.

1.3.2. CONDUCTIVE POLYMERS AND INKS

In an attempt to combine the stretchability of elastomers and the electrical functionality of conductive materials, a new class of stretchable electronics is emerging. This is achieved by the mixing of these two materials together in order to bridge the gap between their elastic properties. Conductive materials like carbon black [25], CNT [26], graphite [27], silver metal particles etc. are mixed into elastomers using a simple mechanical process called blending. The electrical properties of such a blend depends on the matrix properties and the dispersion techniques. The concept of carbon black-based stretchable conductors has been there for several decades, with new advancements in the form of graphene and CNT's. Although carbon based nanomaterials show lower electrical conductivities in comparison to metals, this has been overcome using unique mixtures and techniques [28].

Several examples of these techniques are applied and studied in literature. The use of a conductive polymer like PEDOT:PSS as *mildly* stretchable conductors has been previously reported [31]. Chemical modifications using dimethylsulfoxide and zonyl fluorosurfactant further improves its low breaking strain of 10% to 20% [32]. Dispersing two materials to yield a final more stretchable conductor is also observed by adding more "exotic" conductors like CNT's and graphite into an elastomer mix. A stretchabil-

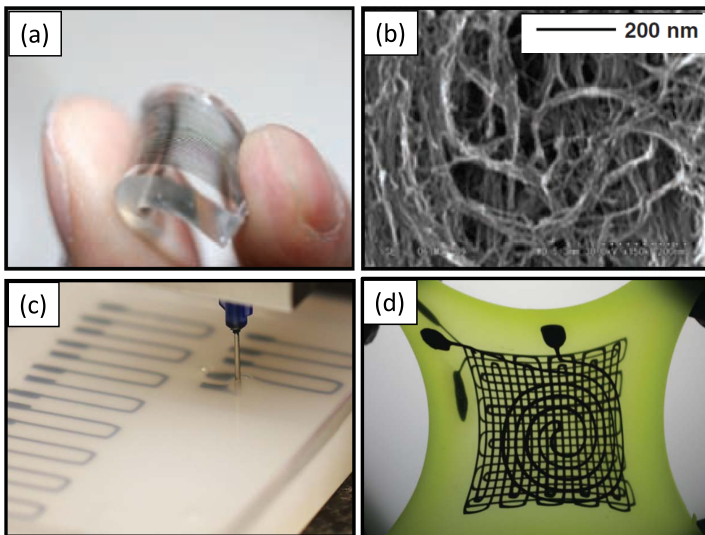

Figure 1.6: (a) SWNT based conductive lines on a stretchable slab of rubber and (b) SEM images of the SWNT's bundles providing the electrical conductivity to the elastomer [29]. (c) Printing of conductive ink on an uncured elastomer for (d) fabrication of stretchable spiral pressure sensor [30].

ity of 134 % was reported by dispersing SWCNT in ionic liquid and fluorinated copolymers named as bucky gel [21]. Materials like SWCNT and MWCNT upon embedding with elastomer yield transparent and stretchable carbon- based conductors [28].
The blended conductive elastomers can be patterned or used as conductive inks. Upon addition of photosensitizers, patternable conductive PDMS with feature sizes as small as 60 μm and 10 μm have been reported [33]. Whereas, a mixture of Ag/PDMS ink has been screen printed succesfully on PDMS substrates for soft printed circuit boards (PCB's) [34]. These methods are very promising, however, questions regarding reliability, adhesion, scalability need further investigation.

1.3.3. EMBEDDED INTERCONNECTS

Interconnects that can be flexed/bend have been succesfully developed and applied in several applications ranging from wearables to consumer lifestyle. This has been shown in technologies like F2R (Flex-to-Rigid), where CMOS devices are made flexible by interconnecting active ASIC devices using polyimde flex interconnects [35] [36]. These interconnects are fabricated by encapsulating metal with polyimide, where the polyimide adds the flexibility to the device. The F2R technology is used for the fabrication of smart catheters whereby complex electronics circuits consisting of ASICs and CMUT transducers are wrapped around or folded into the tip of a catheter. This technique is useful for devices that are bent uniaxially, whereas to impart a little bit more conformability, a biaxial stretch is needed.
Stretchability can be introduced by connecting stiff rigid islands containing devices with stretchable electrical interconnects. To make interconnects stretchable they can be designed into complex/simple meander, horshoe or mesh like structures. A study by the group of Jan Van Fleteren from Ghent University proposes the integration of rigid electronic devices that are sparsely distributed and interconnected to each other using meander shaped interconnects. The interconnects are encapsulated on both sides with polyimide, to improve their stretchability and reliability. This system is embedded in an elastomer like PDMS, such that the meander interconnects behave like "2-D" springs when stretched. The meanders are carefully designed in order to ensure that the strain in the conductor remains below the point of rupture.

Several studies on different designs of the interconnects like zigzag, sinusoidal, U-shape etc. have been reported in literature [38] [39] [40] [41] [42] [37]. Amongst these, the best stretchability was reported for horse shoe shaped interconnects. While fabricating a horse shoe shaped interconnect, certain key structural and design parameters have been discussed which rely on the angle (θ), width of the metal (W_{metal}) and radius of the metal (R_{metal}), metal thickness and the width and thickness of the encapsulating polymer layer (PI). It was shown that decreasing the width and thickness of the interconnects, reduces the stress in the conductor, eventually delaying the crack propagation while stretching. Additionally, a wider PI encapsulation layer improves stretchability. These results are adopted in this thesis in the design of the interconnects for large area patches. In Fig. 1.7 copper meander structures reported by [37] fabricated using this technique show an elongation from 40-180 % while still retaining the conduction of the interconnects. However, at a 40 % elongation, shown in Fig.

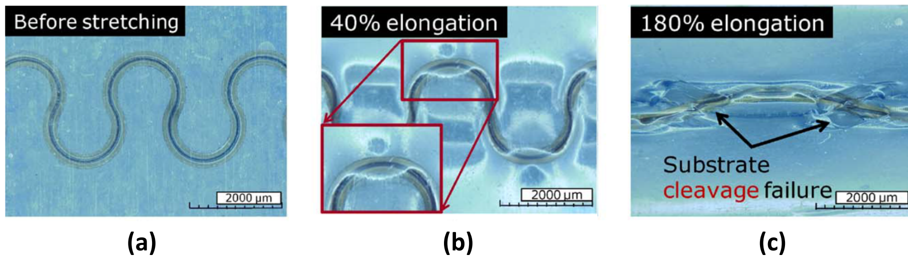

Figure 1.7: (a) Optical microscope images taken in situ while stretching of PI encapsulated Cu meander shaped interconnects embedded in PDMS with stretch varying from 0 % - 180 %. At 40 % elongation in (b) (shown in inset), a colour change is observed due to out of plane deformation of the interconnects. (c) Substrate cleavage failure is reported at a stretch of 180 % as the adhesion between the elastomer and the interconnects disrupts [37].

1.7(b), a color change was observed caused by the out of plane deformation of the structure. The elastomer surrounding the interconnects, however, restricts such a deformation to in-plane and results in an eventual interface delamination upon increase in stretching (Fig. 1.7-c).

1.4. AIM AND OUTLINE OF THIS THESIS

1.4.1. SCOPE OF THE THESIS

The research presented in this Thesis is a part of the M2i-funded “new materials for minimally invasive medically instruments (NEMESIS)” project. The aim of this multidisciplinary project follows from the observation that the technologies for stretchable and conformable circuits presented in the previous section were primarily developed for sparse array of relatively small active devices with a rather low fill factor. In other words, the rigid islands containing the circuits and sensors are relatively small compared to the part of the circuit that contains the stretchable interconnects. Additionally, the majority of the presented technologies only allows for a limited number of these interconnects in that area. There are, however a number of emerging applications, for example for large area diagnostic imaging patches, that require a much higher fill factor and high density interconnects between the rigid nodes due to the complexity of the device application. For these applications the relatively small stretchable areas containing the interconnects have to accommodate the stretching of the complete circuit. In a circuit with a fill factor of 90% for example, the stretchable interconnects have to stretch 95% in order to obtain a global stretching of only 20% (using the relation from [40]).

The goal of this Thesis is to develop a technology for stretchable circuits and patches with a high fill factor wherein the interconnects can be stretched substantially. Additionally, the technology should be compatible with standard micro-fabrication technologies to allow for the fabrication of high density interconnects. The approach followed will be based on so called free standing interconnects that are not embedded in the stretchable matrix that supports the circuit or patch to allow the interconnects to

fully bend out of plain during stretching. This new feature implies a paradigm shift in stretchable interconnect technology, and in a joint project with researchers from the technical university of Eindhoven (TU/e) the implication and advantages of this feature have been explored. The Thesis consists of two parts. In the first part a technology platform is presented that allows for the fabrication of stretchable circuits with freestanding interconnects. Although the technology is suitable for stretchable patches with a high fill factor and dense interconnects, in this first technology demonstrator a relaxed sparse design was implemented. The second part of the thesis focuses on the high density interconnects, more in particular on the development of a test methodology and test structure that will allow for the reliable and reproducible testing of micron-size interconnects that are completely freestanding.

1.4.2. OUTLINE OF THESIS

Chapter 2 comprises the first part of this Thesis, the technology for the fabrication of free standing large area interconnects is described here. This chapter comprises of the first proof of principle polyimide meanders, fabrication flow and the process optimization steps. A requirement for a good adhesion between PI and PDMS for the reliability of this device is identified and discussed in the next chapter. The knowledge of processing from this first proof of principle is utilized later in chapter 4 to integrate the metal layer and some additional technology steps together.

Chapter 3 compiles the two novel adhesion improvement techniques for the reliable adhesion of PI to PDMS. We explore the influence of surface modification of the polyimide surface on its adhesion to PDMS, as well as introduce an intermediate rubber layer as an alternative approach for adhesion.

In **Chapter 4** the integration of metal interconnects with the previous flowchart is done and several new process modules in the form of pillars and the mechanical interlocking of pillars are developed. The final test device is stretched and measured, whereby failure modes are also presented.

The second part of this Thesis starts in **Chapter 5** and introduces the ultra strechable interconnects for high density stretchable electronics. In this chapter we fabricate a test device for the fabrication and characterization of these structures. The versatile test device introduced in this chapter is also applicable for testing different geometries of interconnects structures. Important design considerations and encountered processing challenges and their solutions are discussed.

Chapter 6 addresses a crucial processing step in the dry etching of polyimide in micro technology using aluminum as hard etch mask. The detailed study of these residues after polyimide etching helps to identify their origin and an eventual residue free etch method is described and implemented.

Finally, general conclusions are discussed and further research recommendations are provided in **Chapter 7**.

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2

PROCESS MODULES FOR LARGE AREA STRETCHABLE ELECTRONICS

In this chapter the first part of this thesis, "Larger area stretchable interconnects" will be presented. Since the application of this device is planned to be on the human body, hereafter we refer to it as a body patch. Development of the patch along with the process optimization steps is discussed. Fabrication of such a patch involves technology modules like EPlaR (Electronics on Plastics by Laser Release) which will also be discussed. A new technology like this comes with a set of challenges in material and design level, an investigation and study of this is done in this chapter. The final integration of the steps is further discussed in a later chapter.

2.1. INTRODUCTION

The development of MEMS integrated CMUT (Capacitive Micro-machined ultrasound transducers) and PMUT (Piezo Micro-machined ultrasound transducers) devices has triggered the development of new applications for these transducers e.g. in smart imaging catheters and ultrasound body patches [1] [2] [3]. By integrating these MEMS ultrasound transducers in conformable substrates, the realization of body patches which can be worn unobtrusively and comfortably on the body has become feasible. These patches can “look” deep into the body to provide information about physical processes such as: blood pressure, wound condition, blood perfusion, bladder content etc.

However, the human body is not straight and rigid so in order for a body patch to be in direct contact with the human body, it has to be at least flexible and in most cases also exhibit a degree of stretchability. In order to make the ultrasound patches flexible and stretchable, the total transducer is sub-divided into separate small rigid tiles that are electrically interconnected, and embedded in the stretchable polymer-PDMS. Although this introduces some degree of compliance, the overall stretchability of this system is still limited because the interconnects undergo high local stresses when the patch is globally strained [6]. Ideally the interconnects between the rigid islands should be freestanding, so that they can behave as true spring like structures and have the possibility of bending out of plane resulting in maximum stretchability. Moreover, the previous technologies were primarily developed for sparse arrays of devices. In this chapter, we define process modules for fabrication of patches that can be integrated with high density and free standing interconnects. For simplicity, we study the technological requirements for the fabrication of such a patch and optimization of the process modules by realising free-standing polyimide meanders without interconnects.

2.2. TECHNOLOGICAL REQUIREMENTS

A fabrication process for realization of free standing large area interconnects will be described in the next sections, and a selection of materials and their selective properties is shown in Table 2.1. The choice of metal for the interconnects is AlCu (99 % Al and 1% Cu), as it is a very commonly used metal in IC fabrication due to its low resistivity, ease of deposition and possibility of dry etching. As a thin film, AlCu behaves as a bendable material and thus has been successfully used in fabrication of flexible electronics for technologies like F2R [4]. Further details on the choice of metal and mask design is presented in chapter 4.

Whereas some applications, such as hyperthermia treatment only require low to medium density interconnects between the silicon islands, other applications, especially in imaging require high density interconnects. This implies that the interconnects not only need to be freestanding, but also individually isolated. The electrical isolation material will also act as a structural material strengthening the metal layer. For these purposes, Polyimide PI-2611 (HD MicroSystems) is used as the isolating and structural polymer for the metal interconnects. It has a Young’s modulus of 8.5 GPa which makes them bendable [5]. Furthermore, PI-2611 films exhibit desirable proper-

Materials	Young's modulus	Stretchable/ Bendable	Transparency	Dielectric Constant
PI	8.5 GPa	Bendable	Low transparency	2.8-3.5
PDMS	360-870 KPa	Stretchable	High transparency (>95%)	2.9-3.2
AlCu	75 GPa*	Bendable (as thin film)	No	Good conductivity

Table 2.1: Properties of the selected stack layers for the fabrication of large area stretchable interconnects. * The value of $AlCu_{1\%}$ is not known in literature. The young's modulus is based on the composition of Al alloy 2024 which resembles the closest composition to $AlCu_{1\%}$

ties like relatively low moisture uptake (0.5%), low stress and low CTE (3 ppm).

Apart from the already mentioned flexibility and stretchability, another important issue when it comes to using patches for on body applications is that the material that is in contact with the skin should be non-allergic and wearable for hours. For this, the interface between the body patch and the skin should be biocompatible. We use PDMS which is well-known for its biocompatibility. PDMS is an elastomer which is well known for its stretchability (Table 2.1). It also has an acoustical impedance that is matched to human tissue, making it a good interface layer between the transducer and the body.

Finally, the technology needs to be compatible with large area, high volume fabrication technologies. Most stretchable technologies proposed in literature built on the existing PCB manufacturing infrastructure. Here however, the choice of materials is limited, while also the density of interconnects that can be achieved is limited. The technology proposed in this chapter uses techniques available in the manufacturing of large area displays, combining thin film processing technologies and fine pitch interconnects with large area manufacturing.

2.3. FABRICATION PROCESS

The fabrication process described next consists of two parts, the release stack and the circuit. To provide a proof of concept, the integration of the aluminum interconnects was skipped to be able to focus on the EPlaR release technology and the out of plane bending of the PI meander structures. The final patches in a later chapter will be integrated with a functional AlCu layer isolated by the PI layers.

2.3.1. RELEASE STACK

The transfer process proposed in this chapter starts with spin coating (PI 2611 diluted with 50 wt% NMP solvent, DuPont2000 rpm for 30 seconds) and curing (275 °C for 3 hours in a nitrogen ambient) of a 500 nm thick layer of polyimide on 150 mm diameter 400 μm thick AF45 glass wafers (fig. 2.2-a). This is followed by sputter coating of 200 nm of aluminum (Veeco 2 Nexus, UHV system, 2 nm/sec deposition rate)(fig. 2.2-b). These two layer constitute the release stack of the device. The release is facilitated by

a laser ablation process known as EPlaR.

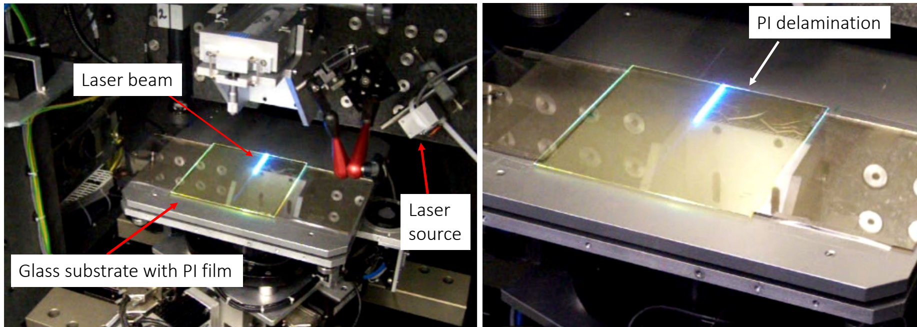


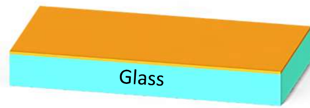
Figure 2.1: EPlaR test setup comprising of an excimer laser source (308 nm, 350 mJ/cm^2) and sample table. The laser beam is exposed through a slit as a line beam of 50 x 0.5 mm^2, that releases the underlying PI layer.

EPlaR (Electronics on Plastic by Laser Release) has been developed by Philips Research in Redhill for the fabrication of flexible displays [7]. In this process a layer of polyimide is spun on a glass wafer. After curing of the polyimide, the active circuitry can be fabricated on the polyimide layer that can withstand temperatures up to 400°C. Next, the polyimide carrier layer along with the fabricated stack is released from the glass wafer by pulses of an excimer laser (308 nm, 350 mJ/cm^2) through the glass substrate. The laser light is absorbed by the polyimide (in the first 100 nm) and breaks specific chemical bonds in the PI. This creates gaseous species at the interface between the glass substrate and the PI layer that causes the PI layer to delaminate from the glass. Since the PI is also slightly deformed, this results in a permanent delamination (Fig. 2.1).

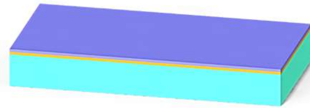
One of the major advantages in the EPlaR process is that it can be used to make flexible electronics in standard fabrication facilities that are suitable for volume production. As mentioned earlier this technology was developed for fabricating displays, which ensures that it is suitable for large area fabrication (Fig.2.1). There is no limitation in size with this technology as compared to standard silicon technology. An alternative approach is the transfer of a pre-fabricated circuit from a rigid to a stretchable substrate. Several transfer techniques have been proposed in literature including Transfer Printing Methods (TPM) [8] and Water-Assisted Nickel (WAN) release [9]. The disadvantages of these techniques are that they require either peel off, which can easily cause stress and damage to the device layer, or require the use of chemicals for the release which is not compatible with PDMS due to its high solvent uptake.

2.3.2. POLYIMIDE MEANDERS

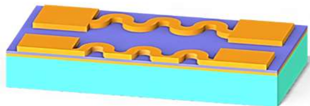
The next step after the fabrication of the release stack, is the fabrication of the circuit to be transferred. To limit the complexity of the proof of principle demonstrator, in our experiments a 5.2 μm thick layer of polyimide (PI 2611, DuPont) is spin coated at 3000 rpm for 45 seconds and cured at 275 °C for 3 hours in a nitrogen ambient (KOYO Thermo Systems Co.Ltd.)(fig. 2.2-b). Next, this layer is patterned (AZ4533 positive



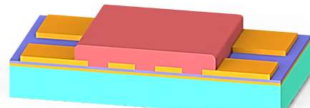
(a) Deposit first layer of polyimide on a glass substrate



(b) Deposit sacrificial spacer metal layer, forming the release stack



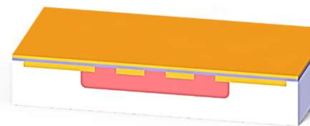
(c) Deposit, pattern and etch polyimide in meander shaped structures



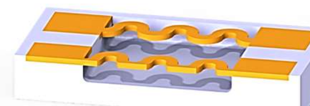
(d) Spin coat a thick layer of resist to serve as sacrificial spacer layer between PI meanders and PDMS

(e) Cast PDMS and cure

(f) Using EPlaR, release the fabricated stack



(g) Invert the stack for further processing



(h) Using dry and wet etch chemistries remove the release stack and the resist layer, rendering the interconnects free-standing

Polyimide Al Resist PDMS

Figure 2.2: Flowchart depicting the fabrication of the free standing PI meander structures.

resist, 420mJ/cm^2) and etched (RIE in STS ICP tool) to form horse-shoe shaped structures. The purpose of these horse-shoe shaped structures is to provide the necessary stretchablility which is lacking in a simple straight conducting wire. However, it has been observed in literature [6] that an embedded meander structure may still not be able to utilize its maximum stretchability. So, for a meander shaped wire to stretch completely, it needs to bend out of plane which is only possible if the interconnects are free-standing i.e. not attached to the substrate. To make the patterned PI structures free standing they are embedded in a 40 μm thick layer of resist (spin coated, AZ40XT) that will act as a spacer layer between the PI and the finally cast-deposited 1 mm thick PDMS layer (fig. 2.2-c). Calculating the amount of PDMS required for casting 1 mm elastomer, 17 g of PDMS was prepared (10:1 curing agent ratio). The PDMS layer is cured at 90°C for 20 minutes in a convection oven. After the front side processing, the backside of the wafer is irradiated with excimer laser pulses (fig. 2.2-d) and as explained in the previous section, this results in the release of the stack from the rigid glass substrate.

After EPlaR release of the structures, the sacrificial PI and Al layers are etched in dry (O_2 plasma) and wet (PES 77-19-04, consisting of phosphoric acid (H_3PO_4), nitric acid (HNO_3) and acetic acid (CH_3COOH)) chemistry respectively. The Al layer acts as an etch stop during the dry etching of sacrificial PI layer. The spacer resist layer that separates the meanders from getting embedded in the PDMS is dissolved in cold KOH (10%) leaving the meanders detached (not adhered) from PDMS substrate (fig. 2.2-d-e).

2.4. PROCESS OPTIMIZATION

The EPlaR technology allows for a simple release of large area conformable body patches. This technology requires glass wafers. In MEMS microfabrication, the technology for fabricating micron sized free standing structures is based on silicon substrates, all the processing steps are hence optimized for silicon substrate [10]. Application of similar steps on glass substrates needed optimization, which will be discussed in this section.

2.4.1. RELEASE STACK OPTIMIZATION

After the curing of the second polyimide layer (Fig.2.2-b), blisters or bumps with a diameter of approximately 50 μm were observed upon microscope inspection. These bumps were spread homogeonously over the glass substrate (Fig. 2.3-a). After the first Al layer the surface was perfectly flat. The origin of the bumps was not clear, especially the interface from which they originated, since there are two interfaces involved, one of first PI and Al and the other between Al and second PI (Fig. 2.2-b). Upon careful inspection, it appeared that immediately after spinning and soft bake of the second layer of PI, the bumps could be observed with the naked eye but were not visible underneath the microscope at this step. After curing they became visible under the light microscope as black dots (fig. 2.3-a). The initial hypothesis was that the adhesion promoter used before coating of PI was not completely soft baked, which would lead to micro-corrosion of the Al surface underneath. To test this theory, a reference wafer

with a PI-Al stack was spin coated with the adhesion promoter, soft baked and observed under the microscope. No difference of the surface topography was observed. However, upon spin coating and curing of a PI layer on top of the Al layer, the bumps appeared.

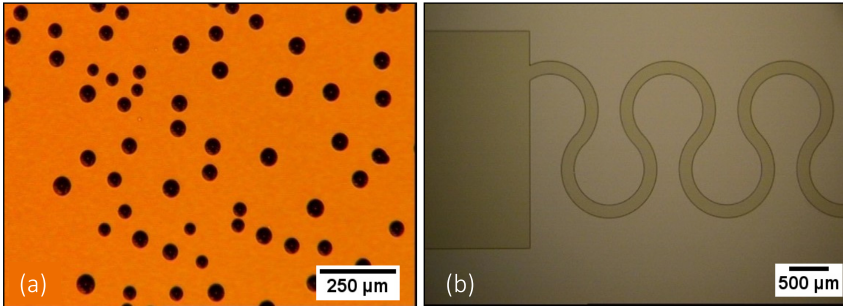


Figure 2.3: Optical microscope images of (a) a cured PI layer on top of Al with dark spots representing the formation of bubbles, and (b) bubble-free cured and etched PI meander structure as a result of longer soft baking.

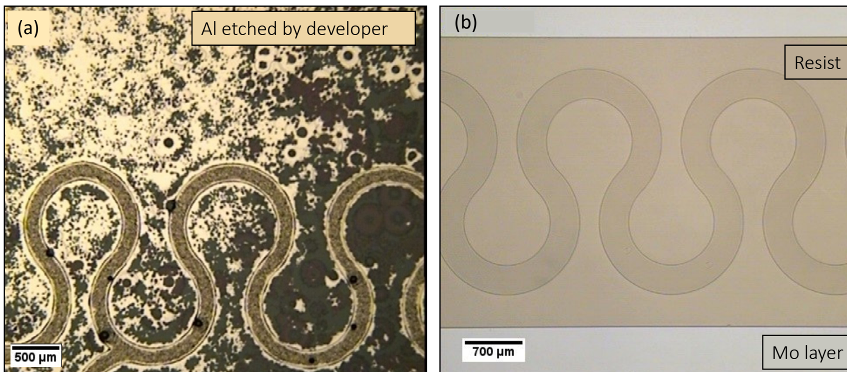


Figure 2.4: Optical microscope images of (a) an attacked/etched sacrificial Al metal layer in the release stack after the long development of resist mask, and (b) resist embedded PI meanders with Molybdenum as the etch stop layer. Molybdenum, unlike aluminum, does not get attacked by the developer chemistry used for development of resist.

Previously in our experiments using Si technology, PI was spin coated on top of aluminum without the occurrence of such bumps. To verify the role of the substrate, a 6-inch Si wafer was deposited with similar layers of PI-Al-PI as on the glass wafer. After post curing of the final PI layer, no bumps were observed. It appeared that the bumps on the glass wafer after the PI curing were caused due to the incomplete NMP-solvent evaporation due to insufficient soft baking. During soft baking, the solvent NMP evaporates and the cross linking of the monomers before complete curing is initiated. The solvent formed bubbles that resulted in bumps after curing. These bubbles were not

observed on the Si wafer as the 5 min soft bake duration was enough for the solvent to evaporate completely. However, glass is a poor thermal conductor as compared to Si [11], which leads to incomplete heat transfer to the PI layer during soft baking causing partial evaporation of NMP-solvent and finally the occurence of bubbles. This was solved by soft baking the PI spin coated glass wafers in a convection oven for 30 minutes at 125 °C, such that the heat is transferred from all the directions to the PI instead of only from the substrate on a hot plate.

Another step which was optimized in our process flow was the replacement of aluminum with molybdenum as the sacrificial metal etch stop layer (Fig. 2.2-a). This was necessary as the development of the very thick spacer resist layer (Fig. 2.2-c) was also etching the underlying Al layer. Increasing the thickness of this metal layer was also implemented as a possible solution, however the developer AZ400K for thick resist required longer durations thus etching the Al underneath. Although the purpose of the Al is to serve as a sacrificial layer, its sacrificial purpose comes of use in the end after processing EPlaR and the removal of the first PI. This layer protects the second PI from getting etched during etching of the first PI (Fig. 2.2-f), so it has to be intact and pinhole free until this final step. The metal was succesfully replaced with molybdenum (200 nm), which does not get etched by the developer and also is etched in the same wet chemistry as Al (PES) in the final steps of the process. The etching of molybdenum is two times faster than Al, thus requiring less time for the released patch to be exposed to the solvent.

2.4.2. POLYIMIDE PATTERNING

RESIST AS MASK

Initially, the second polyimide (6 μm) was patterned using resist (7 μm) as a mask. However, the profile of the etched polyimide showed peaks at the edges and an overetch in the middle of the structure (Fig. 2.5).

Theoretically, polyimide etching in an O_2 plasma with resist as a mask gives a 1:1 etch selectivity. However, upon investigation the resist etches faster (almost double) as compared to PI, which is also dependant on the conditioning of the tool prior to the etch. In order to prevent an overetch, the resist mask has to be atleast double the PI thickness which could be an issue in patterning of high resolution structures. An alternative to this approach has been discussed in Chapter 4, where aluminumis used as a hard etch mask. This is however incompatible with the process flow described in Figure 2.2, as the etch stop of the PI layer is molybdenum. After the etching of the PI using an Al hard etch mask, the removal of the hard etch mask would also etch the Mo layer.

PHOTO-PATTERNABLE POLYIMIDE

As described in the previous section, the etching of PI using resist as a mask is cumbersome. An alternative approach is to use photo patternable (negative tone) polyimide. A suitable photopatternable polyimide is the Fujifilm LTC 9300 series PI.

Some advantages that LTC 9300 series has over PI2610 are:

- It is environment health and safety (EHS) friendly due to its NMP (N-methyl-

2-pyrrolidone) free composition. N-Methylpyrrolidone (NMP) is a solvent used in a variety of industries and applications, such as paint and coating removal, petrochemical processing, engineering plastics coatings, agricultural chemicals, electronic cleaning and industrial/domestic cleaning. Most polyimides also contain NMP as solvent, which reportedly implies potential health risks to pregnant women and women of childbearing age [12]

- It is photopatternable which reduces the number of steps in processing, making the process faster. Also, the minimum feature size of this polyimide can be as small as 4 μm for a 5.2 μm thick layer and it has a large lithography process window which is substrate independent.
- The imidization reaction of the LTC 9300 series is completed at a lower temperatures (200-250 °C) as compared to other polyimdes (350 °C). This can be especially beneficial for post processing on devices with very low thermal budget.
- It provides excellent material properties like mechanical parameters, chemical resistance, adhesion performance and electrical properties at a low temperature cure.

Considering the above mentioned advantages a study in collaboration with Fujifilm was performed using the PI LTC 9305 negative polyimide.

Experimental: Short loop experiments were performed to obtain the parameters for patterning and developing the LTC 9305 polyimide, with the equipment available in the PInS (Philips Innvoations Services) cleanroom. PECVD silicon-oxide (1 μm) de-

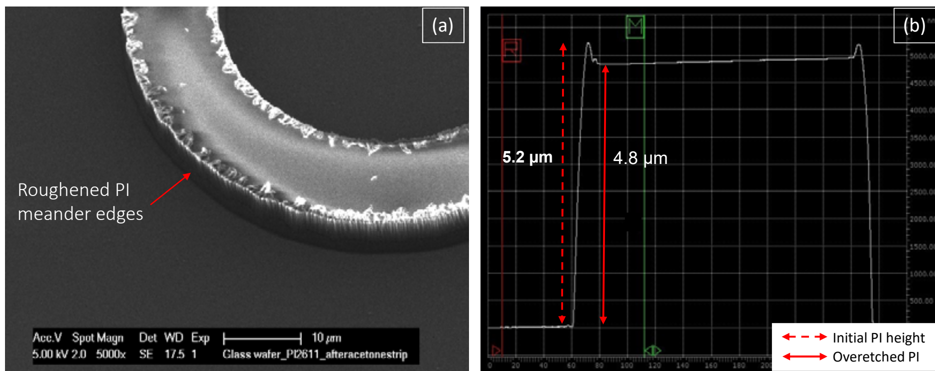


Figure 2.5: (a) SEM image of a PI meander where the homogeneity of the dry etch using resist as a mask varies through the structure. The resist mask etches in the same dry etch chemistry as PI, which at times leads to loss of mask during the PI etching process. As depicted in (b) a stylus profilometer measurement of the structure gives a variation in height. The edge of the PI remain the initial deposited height (5.2 μm) although roughened, whereas the structure height in the middle reduces by 400 nm due to over etching of PI after loss of mask.

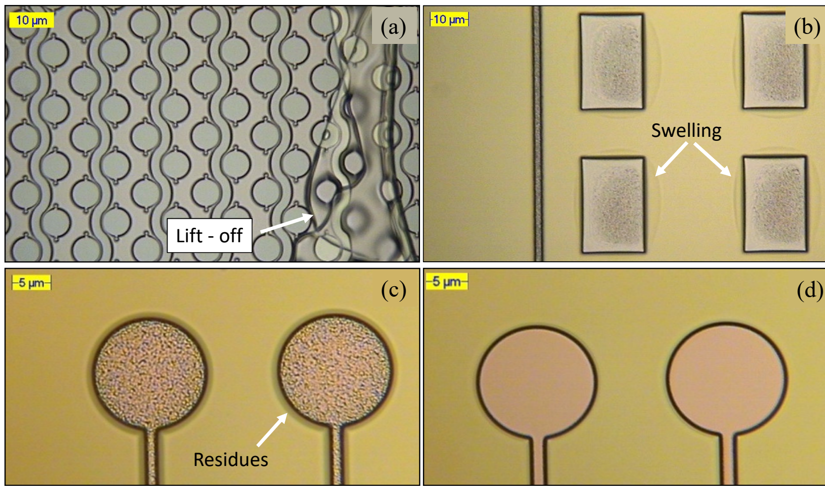


Figure 2.6: Optical microscope images of PI structures, after exposure and development. The design of the structures are not of significance, which have been created by using a re-purposed mask, in order to study the exposure and development behavior of the negative PI. (a) Liftoff of structures exposed at energy doses >400 mJ/cm^2, (b) swelling of structures after development, (c) and (d) elimination of residues formed due to lateral exposure at higher energy doses by reducing the exposure energy.

posited 6 inch Si wafers were used as substrates. These were cleaned using the RCA-1[1] process to remove organic residues and films from the substrate before processing. Next, these wafers were spin coated with LTC 9305 in a manual spin coater (3000 rpm for 30 s) and soft baked (2 mins. at 100 °C) to obtain a 5μm thick layer. Next, a mask with 12 μm wide trench structures was used for exposure. To determine the correct exposure and focus dose for a 5 μm thick layer, a focus exposure matrix and power meander were performed on an ASML PAS5500 stepper. The exposed wafers have to be developed in two steps. First step contained pure cycolopentanone and second, equal volumes of RER600 [2] and cyclopentanone. The wafers were split into three batches (A, B and C) that were developed using three different techniques.

Batch A was developed manually using a horizontal immersion bath, by periodically agitating the wafer in a horizontal motion (Fig. 2.7-a). Batch B was developed using a vertical immersion bath, by periodically agitating the wafer in a vertical motion (Fig.2.7- b). Batch C was developed on an automatic atomized spray developer which was available in the Fujifilm (Belgium) cleanroom. In the atomized spray development process, the developer is sprayed on top of the wafer along with nitrogen gas making the drops approximately atom sized (Fig. 2.7-c). After development, the wafers were soft baked at 100 °C for 2 minutes. Finally, the wafers were cured in a nitrogen ambient (KOYO oven) for 3 hours at 250 °C. A short O_2 plasma descum (600 W, 110°C, 5min) was executed after PI curing to remove any footing in the trenches.

[1] Decontamination mechanism based on sequential oxidative desorption and complexing with H_2O_2-NH_4OH-H_2O

[2] 1-Methoxy-2-propanol acetate, CAS-No. 108-65-6

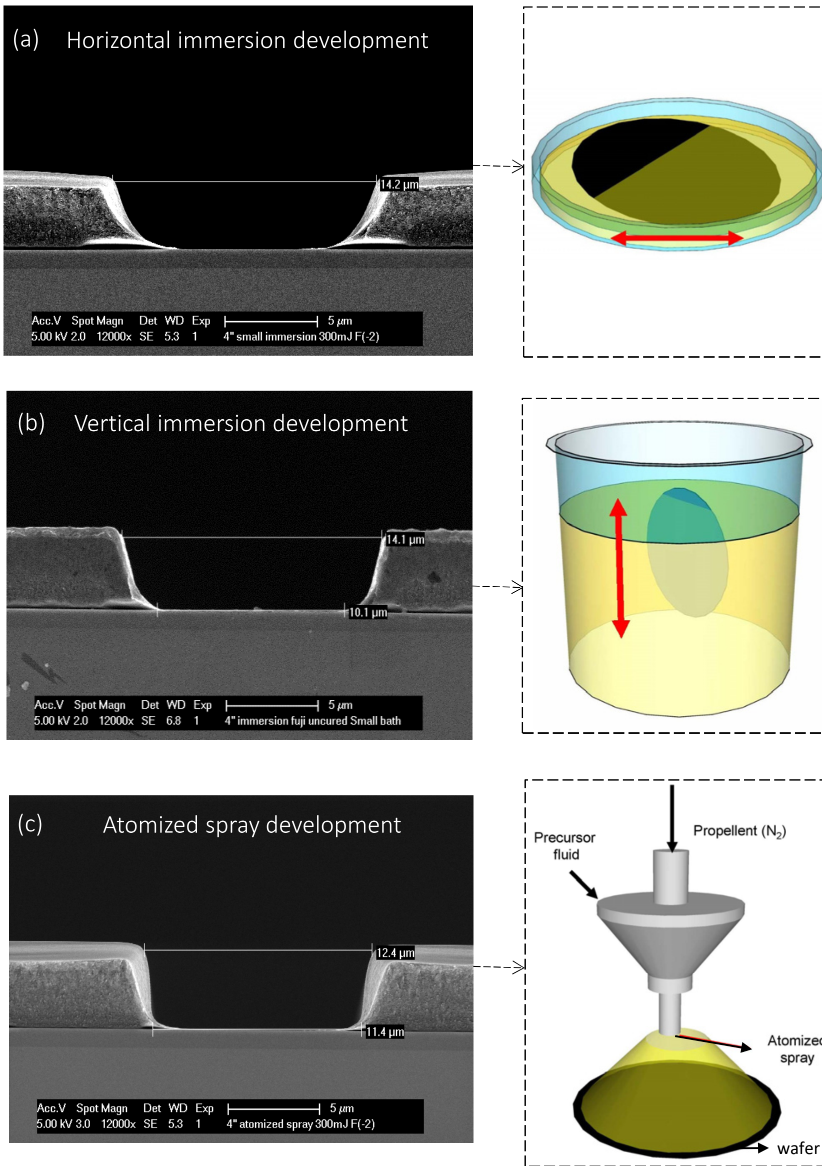


Figure 2.7: SEM micrographs of trench cross sections (on left) and development schematics (on right). (a) Batch A- horizontal immersion development, whereby the wafer is developed in a horizontal carrier by agitating in horizontal direction. The cross section presents the sloped walls of the trenches, wherein the top trench width varies greatly with the lower trench width. (b) Batch B- vertical immersion development by vertically agitating the wafer in a vertical carrier/beaker. The cross section presents the less sloped walls of the trenches, wherein the variation in top and bottom width of the trench is lesser than horizontal immersion method. (c) Batch C- atomized spray development, where developer mixed with nitrogen gas is sprayed in the form of atomized particles over the wafer. The cross section presents straight walls of the trench, as well as almost equal top and bottom width of the trenches. In the schematics on the left, the red arrows denote the agitation motion of the sample.

Results: At a lower dose of energy (100-200 mJ/cm^2), the structures were lifted off from the substrate due to under exposure of PI (Fig. 2.6-a), while at a higher energy dose (>400mJ/cm^2) residues were observed (Fig. 2.6-c). This effect is observed due to lateral dispersion of light at higher energy doses, which further exposes the masked area and is therefore cross linking the masked PI. An ideal energy dose was observed to be 300 mJ/cm^2 with a focus of -1 μm. Swelling observed on the structures after development was resolved by performing a post development bake at 100 °C for 2 minutes (Fig. 2.6- b). There were differences in the development results of the three development techniques presented in Figure. 2.7. The structures were developed homogeneously on the wafer with the atomized spray method, due to the uniform distribution of developer over the wafer. In case of both the horizontal and vertical immersion methods it was observed that the structures were very well developed in certain areas of the wafer but not equally well developed in the other areas (Fig. 2.7). In conclusion, the results from the negative PI were promising and could be applied to the device fabrication. However, due to the unavailability of the proper instruments in the cleanroom, the PI 2610 was selected in this work.

As an alternative to the resist mask, Ti was investigated as a hard etch mask for PI etching. It was selected because after etching of polyimide, the hard etch mask removal can be selective towards the molybdenum etch stop layer. Ti has not been reported as a commonly used hard etch mask for the etching of polymer in IC fabrication, so the process had to be optimized. This will be discussed in the next subsection.

Ti as hard etch mask

For Ti to be used as a hard etch mask it has to meet certain requirements. One of the requirements is the adhesion to polyimide. Since the layer is used sacrificially as a hard etch mask and not functionally, the requirement for its adhesion is that the Ti has to sustain the etching process. After sputter coating Ti on polyimide, a scotch tape test was performed. Titanium passed the peel test. Another requirement was the ease of patterning of Ti on PI. Titanium can be etched in both wet and dry chemistry. A short loop experiment with a 6-inch Si wafer with a layer of 2.5 μm thermal SiO_2 was conducted using patterned 200 nm Ti on polyimide. The Ti was patterned using a 3.6 μm thick positive resist mask (HPR 504). The hard etch mask was etched in dry chemistry using Cl_2 plasma (STS ICP, 20 seconds). The etch rate of Ti is very high using this chemistry, and it is also selective towards polyimide. For the removal of the hard etch mask after etching of the PI, the use of wet chemistry was investigated. As an etchant peroxide was selected as it does not etch the PI or the underlying Al etch stop layer, which is considered an advantage in removal of the hard etch mask after the etching of PI.

Using the Ti hard etch mask the PI is etched in an O_2 chemistry plasma (100 sccm), which is selective towards the Ti mask. However, the etching of PI did not result in a clean end point. Upon SEM inspection a high density of "grass" like structures was observed on the SiO_2 surface (Fig. 2.8-a,b). Prolongation of the etching process does not remove the grass layer. As will be later discussed in chapter-6, micromasking due to the re-deposition of atoms sputtered from the hard mask can act as a possible cause for formation of “grass” during polyimide etching in a pure O_2 plasma [13]. This was

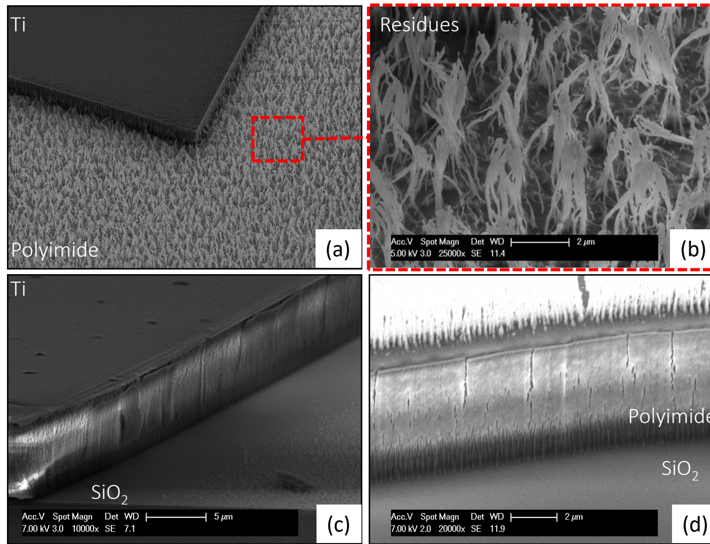


Figure 2.8: SEM images after (a) etching of polyimide using Ti as hard etch mask, whereby (b) grass-like residues cover the surface of underlying SiO_2. In (c) and (d), a residue free etch was observed after the addition of fluorine in the etching gas composition for polyimide.

suspected to play a role in the residues formed after etching with Ti as well. In order to remove the Ti micromasking, a fluorine-containing gas (CF_4) was added to the O_2 plasma, as fluorine (and chlorine) radicals etch Ti [14]. Unfortunately, this chemistry also attacks the Ti hard etch mask itself. However, fluorine is only present in very small amounts (5 sccm) in the gas mixture as compared to O_2(100 sccm). So, the etch rate of the hard etch mask is much lower than the etch rate of polyimide.

Figures 2.8-c,d show SEM pictures of the profile of a polyimide layer etched in an ICP-RIE etcher with a gas composition of 100 sccm O_2 and 5 sccm CF_4, using a 200 nm thick Ti mask and a power of 1500 W for 8 min. The etch rate of the polyimide was ca. 800 nm/min. The hard etch mask was also etched 100 nm during the process which is not of concern as in the next step the hard etch mask is removed. It was observed that even a very small amount of carbon tetrafluoride (CF_4) was sufficient to achieve residue-free etching of the polyimide.

2.5. RESULTS AND CONCLUSIONS

The fabrication of a patch consisting of PI horse-shoe meander structures was completed after implementing the previously discussed process optimization steps (Fig. 2.9-a). It is observed that the thickness of the casted PDMS plays an important role in the release behavior of the patch, whereby thinner PDMS layers result in a curled released patch (Fig. 2.9- b). After the removal of the released patch, the glass substrates are cleaned and ready to be re-used, thus illustrating the sustainability of this release process (Fig. 2.9-c). Followed by the release of the patch, a smaller patch is cut from

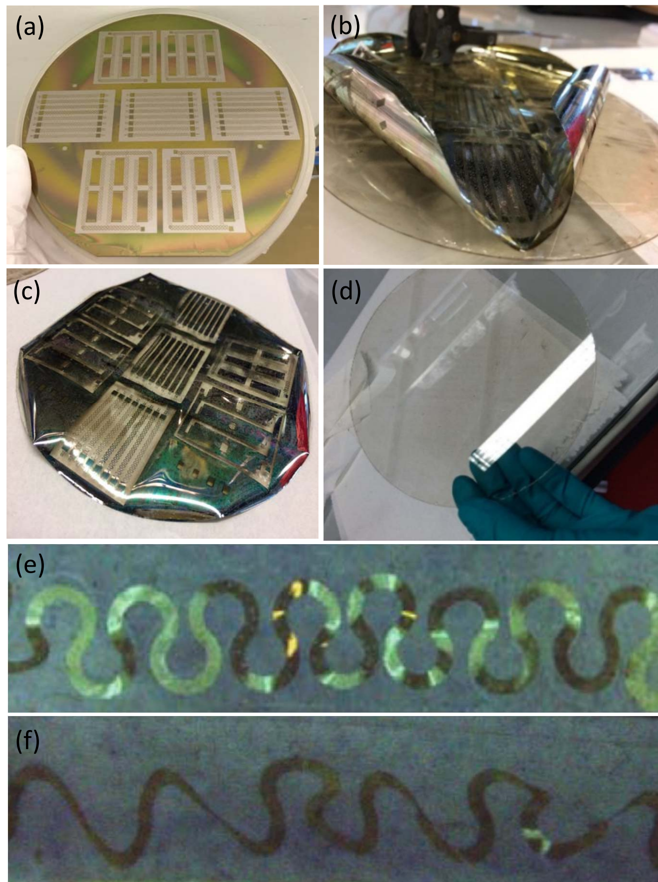


Figure 2.9: (a) 150 mm wafer with the PI meander patches embedded in PDMS, ready for final release, (b) the layer stack released using EPlaR, (c) flipped patch after the release patch for the etching of sacrificial layers and (d) glass wafer after the release and removal of the stack, completely reusable. Optical microscope images of the released PI meander structures (e) before stretching and (f) after stretching ($\approx$ 80%), where the structures shows the out of plane bending after stretch is applied.

this stack. This patch is then processed further for the removal of the release stack by using dry (sacfricial polyimide) and wet (Mo layer) chemistries. The removal of the sacrificial polyimide proved to be rather cumbersome due to the exposure of the patch in O_2 plasma, as the chemistry also slightly attacks the underlying PDMS layer. However, this did not pose as a severe problem for the succeeding steps. Subsequently, the removal of spacer resist in KOH render the large PI meanders free. The patch was stretched manually under a microscope to study the bending behavior of the meander structures. Upon stretching, the meanders bend out of plane and upon release come back to their original position. Further investigation of the amount of stretchability

were not conducted with these structures. These results however, sufficiently provide a proof principle and also throw some light on the limitations of this patch technology.

After the removal of the spacer resist layer, it was observed that the meanders were not completely free-standing, but they also do not adhere to the PDMS substrate. A drooping behavior of these structures was observed due to their weight. This was further studied and solutions in the form of “pillars” and “stitches” were developed that will be presented in chapter 4. Another limitation of this technology was observed in the form of poor adhesion between PI-PDMS. Immersion of the patch in wet chemicals for the release of the sacrificial layers further weakened the adhesion of these layers and in several case the layers delaminated after these steps. The sustenance of this patch is heavily dependent on a good interaction/adhesion between the PI and PDMS. Therefore, in the next chapter, methods for improving the adhesion between these two polymer interfaces are presented.

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3

POLYIMIDE-PDMS ADHESION

The processing of polymeric materials is gaining importance, especially for the fabrication of flexible and stretchable medical micro- fabricated devices. Although the adhesion between metal/oxide-polymer interfaces has been studied instensively, the adhesion between different polymer materials is usually less understood, and therefore less controlled. In this chapter we study and improve the adhesion between polyimide and polydimethylsiloxane (PDMS) since these materials are frequently used in conformable medical devices, and delamination of the polyimide-PDMS interface will result in the failure of these device.

Parts of this chapter have been published in Materials Advances **1**, 33-38 (2016) [1] and in proceedings of Eurosensors **1**, 307, 2017 [2].

3.1. POLYIMIDE

POLYIMIDES are a type of polymer consisting of imide monomers. This branch of polymers is attractive for use in the microelectronics industry due to properties like high thermal stability (Tg) [3], low dielectric constant [4], inertness to solvents [5] etc. The polyimides used in the microelectronics industry are usually synthesized from pyromellitic dianhydride (PMDA) or biphenyldianhydride (BPDA) with 1,4 phenylenediamine (PDA) in order to form BPDA-PDA. Synthesis with these monomers yields a polyimde that has a higher thermal stability than PI formulations consisting of C-O-C ether bonds [6]. In this thesis, we use a polyimide which is comprised of a polyamic (PAA) solution (composed of the same BPDA-PDA formuation) dissolved in an organic polar solvent N-methyl-2-pyrrolidone (NMP). The polyimide is deposited by spin coating on substrates whereby the thickness is determined by the spin speed (typically 2.5 -5.2 μm) followed by a short soft bake. Next, the wafers are hard cured at a pre defined temperature of 275 °C for 3 hours under nitrogen atmosphere. The hard cure enables the solvent to drive off completely, and complete the imidization process such that the PAA is converted into PI by the formation of imide rings (Fig. 3.1).

3.2. POLYDIMETHYLSILOXANE (PDMS)

Polydimethylsiloxane (PDMS) is a silicone that is widely used in several industries like medical, industrial, household etc. [7]. Silicones are also referred to as polysiloxanes that are mixed organic-inorganic polymers comprising of silicon and oxygen alternating in a chain, where some organic groups like methyl, ethyl and phenyl are attached to the Si atoms (Fig. 3.1). The non-toxic and inert nature of silicones makes them attractive for healthcare and medical devices. The silicone-PDMS is well known for its

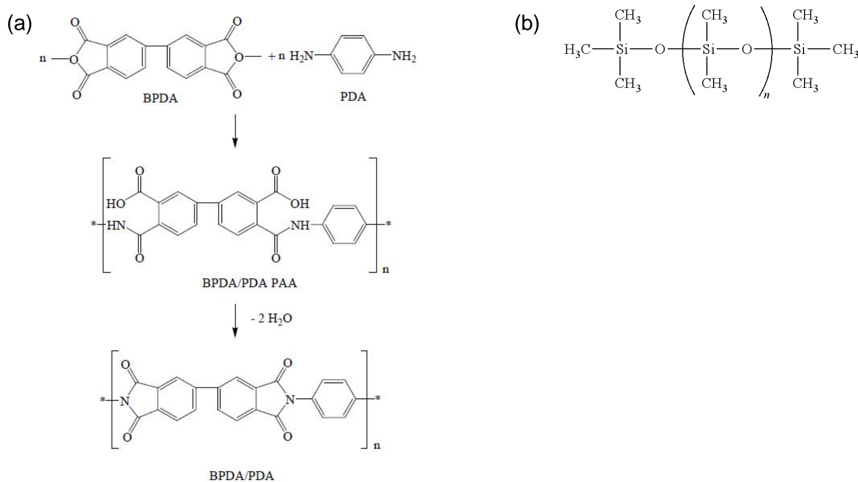

Figure 3.1: (a) Synthesis of BPDA-PDA polyimide [6] and (b) chemical structure of polydimethylsiloxane

biocompatibility and compliance, and additionally it has an acoustic impedance that is matched to human tissue making it a good interface layer for on-body applications such as smart ultra-sound body patches. It has several advantageous physical and chemical properties, it is low cost and is easy to use. Some of its properties include: thermal conductivity of 0.16 W $(m\ K)^{-1}$ [8], high gas permeability (O_2, 79 x $10^{-7}(cm^3\ cm)(s\ cm^2\ kPa)^{-1}$) [7], and a young's modulus of 750 kPa [9]. PDMS is hydrophobic in nature due to its low surface energy of 22 mJ m^{-2} [10], which results in a poor adhesion to most materials except glass. PDMS can be deposited by spin coating or casting, and it has a high replication fidelity [11].

3.3. POLYIMIDE-PDMS ADHESION

The adhesion between polydimethylsiloxane and polyimided is challenging due to the chemical inertness and hydrophobicity of PDMS. For the reliability of the body patch described in chapter 4, therefore this issue needs to be addressed and studied further. According to literature, PDMS-PDMS adhesion has been resolved by modifying the surface of cured PDMS with an oxygen plasma before applying it to another layer of cured PDMS [12], or by using an uncured layer of PDMS as an adhesive layer in between two cured PDMS substrates [13]. Adhesion of PDMS to another polymer has been less studied and understood in the literature. Some methods to improve the adhesion that have been proposed include the introduction of surface-adhesion-promoters (SAP) [14] during the PDMS curing process [15] , or by the introduction of new chemical functional groups between the PDMS-polyimide interface [16] [17]. In this chapter, we discuss two methods for improving the adhesion of PDMS to PI. These are based on:

- Surface modification of the cured PI surface
- Introduction of a new unreported intermediate layer (butyl rubber).

In the following sub sections, the application of these two methods will be explained and compared to other existing mechanisms. Selection of the final layer will be performed on the basis of its successful integration into the complete process flow.

3.4. SURFACE MODIFICATION OF POLYIMIDE BY ARGON ION SPUTTERING

3.4.1. EXPERIMENTS

Silicon-oxide deposited 6 inch Si wafers were used as substrates. All samples were spin coated with a commercial polyimide PI-2611 at 3000 rpm for 45 secs and cured at at 275 °C for 3 hours in N_2 gas atmosphere to complete the imidization process. PI 2611 was used because it is known to yield stable free standing films. The curing process converts the polyamic acid precursor into a fully aromatic, insoluble polyimide film and drives off the NMP solvent carrier. The cured PI film thickness was measured to be 5.2 μm. The samples were divided into four groups.

In group A, non-treated polyimide coated samples were taken as a reference for characterization and analysis. In group B, the samples were exposed to an oxygen plasma treatment (200 W) for 30 seconds. In group C, the samples were spin coated with an adhesion promoter VM651 (3500 rpm), which is normally used before coating of PI on Si wafer. In group D, samples were sputter etched in a 50 sccm Ar^{+} ion plasma at 600 W, 3 mTorr to modify the top surface layer of polyimide. The different sputter etch times used were 100 s, 200 s and 600 s. On polyimide the sputter depths were not measured but on aluminum these sputter durations result in 5 nm, 15 nm and 30 nm sputter depths respectively. All the samples were next over-molded with a 1 mm thick layer of PDMS (Sylgard) and cured at RT for 24 hours. Peel tests were performed with Scotch Tape. Shear measurements were conducted on a Nordson Dage Series 4000 Bondtester with a load cell of 4.9 N and scan speed of 500 μm/s. The blade on the tool pushes off the PDMS layer from the PI while measuring the amount of force required. Atomic Force Measurements (AFM) were obtained by a Bruker Dimension FastScan, using a Si probe in tapping mode in air. Each sample was scanned on two locations, with a scan range 4×4 μm^2. Before scanning the surface was cleaned with de-ionized nitrogen. Fourier Transform Infrared (FTIR) Spectroscopy results were obtained with a Bruker Hyperion 3000 IR microscope. The microscope is connected to a Bruker Tensor 27 FTIR optical bench.

3.4.2. PEEL MEASUREMENTS

There are several methods used for assessing the adhesion quality between two interfaces. The most common and widely used preliminary test is the Scotch Tape test [18], where a Scotch tape is applied to the surface and pulled off. If the tape comes off clean, the sample is considered to have passed the Scotch tape test. Although this is a rather qualitative test,it gives a first rough indication of the adhesion. A peel can be sub-divided into three categories: a complete peel, a partial peel and no peel. In case of a complete peel, the PDMS layer across a given width completely delaminates from the adhering PI surface. In a partial peel, the PDMS delaminates only from a portion of the PI adhering surface; whereas in case of no peel, the two layers fail to delaminate. In case of group A, B and C samples; a complete peel of the PDMS layer in all cases is observed. The oxygen plasma treatment in group B was done in order to increase the surface energy of the PI (contact angle changes from 75 ° to 20 ° after oxygen plasma). It was argued that the adhesion of PDMS to a hydrophilic surface would be better than to hydrophobic PI because PDMS adheres readily to a hydrophilic silicon dioxide surface, but no improvement of adhesion was observed compared to group A. Also the application of an adhesion promoter in group C did not improve the adhesion. In the case of group D samples, no peel was observed. This shows that the adhesion of the tape to the surface of PDMS is weaker than the adhesion of the PI/PDMS interface in case of group D and stronger in case of group A, B and C. Upon manual peeling of the PDMS from the PI surface, the material fragments into pieces and gives a partial peel, as a result, a 90 degree peel test couldn't be performed. Since no peeling technique could be used to characterize the adhesion quality, a shear technique method is used that gives a quantifiable result and is a "practical adhesion quantifier". This peel

technique is discussed in the next sub-section.

3.4.3. SHEAR ANALYSIS

Shear experiments were conducted on all samples. During this test, the 1 mm thick layer of PDMS is “pushed” off from the underlying 5.2 μm thick PI layer over a length of approximately 1 cm with a blade, while the shear force delaminating and deforming the PDMS layer is measured. The shear test is not a very common way of measuring the adhesive strength between interfaces. It was used as an alternative method to measure the force required to delaminate PDMS from PI in group D samples without fragmenting the PDMS. Although the samples in group A, B and C could easily be characterized with the standard peeling tests, the shear test was used for all samples in order to be able to compare the adhesion quantitatively. The shear measurements showed a 14 times increase in shear force for group D samples as compared to the samples in group A, B and C. The measured force of the delamination of groups A, B and C samples was extremely low because of the poor adhesion. Therefore, a manual

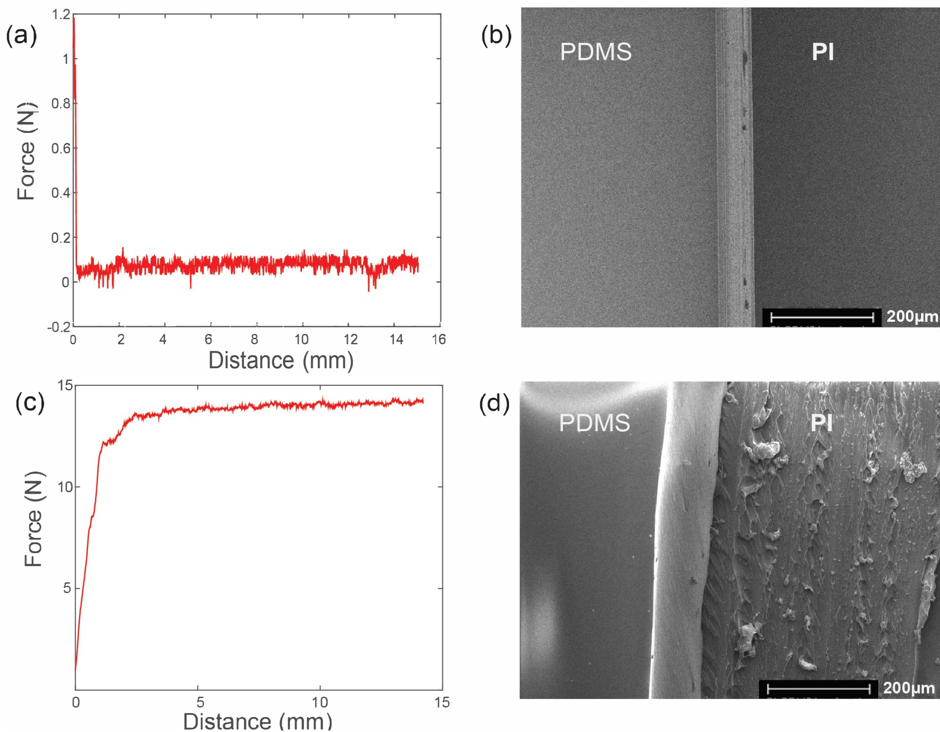

Figure 3.2: Shear test measurements and Scanning Electron Micrographs (SEM) showing (a) the force measured on samples A, B and C, (b) the clean interface of PDMS/PI after delamination, (c) the force measured for sputter etched sample D and (d) the unclean interface of PI/PDMS after delamination showing that the PDMS is still not completely delaminated.

resistance was given to the blade to start the test, which is the initial peak seen in the graph of the non-sputtered sample Figure 3.2-a
This shear force technique is predominantly used for measuring the adhesion strength of SMD components on PCB's, and is therfore not optimized. The tool to analyze changes in force that have a magnitude smaller than 1 N. This is perhaps the reason why it cannot detect changes in adhesion for increasing sputter etch times or incase the adhesion is as poor as group A, B and C. So only two extreme measurements have been reported in the graphs in Figure 3.2 that represent all the cases of group D and also for group A, B and C.

3.4.4. RESULTS AND DISCUSSIONS

SURFACE ROUGHNESS ANALYSIS

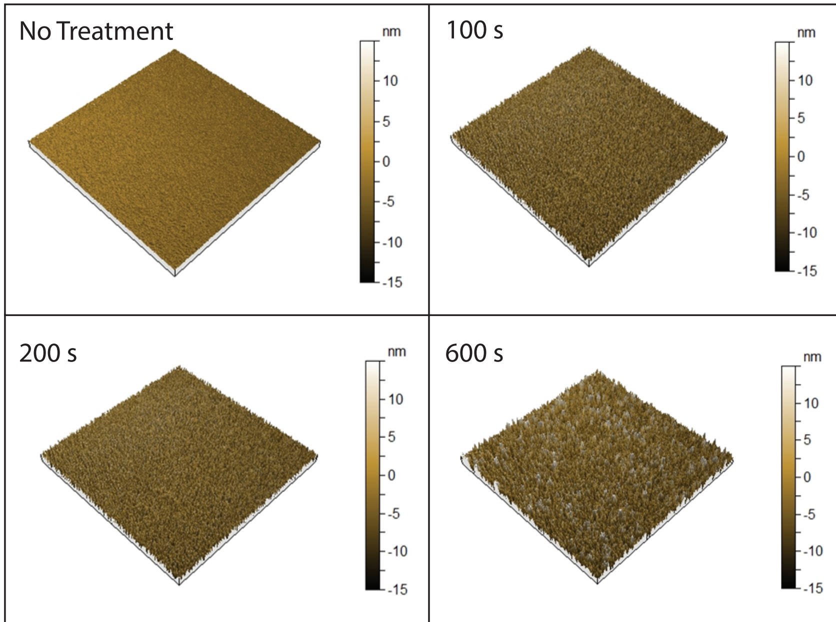

Figure 3.3: Atomic Force Measurements (AFM) of Ar^+ sputter etched PI surface samples ranging from no treatment to sputter durations of 100, 200 and 600 seconds (3 mTorr, 300 W and 50 sccm of Argon) from left to right.

Earlier studies have reported the influence of surface roughness on the adhesion improvement of polyimide to metals like copper [19]. These studies indicate that there is an increase in the interfacial strength of copper to PI with the increase in surface roughness of the metal surface. It was hypothesized that argon sputtering of the polyimide surface creates some surface topography that geometrically locks and encloses the PDMS and hence improves the adhesion Fig. 3.4. Therefore, the surface topography of each sample was characterized by AFM, and it was found that argon sputtering

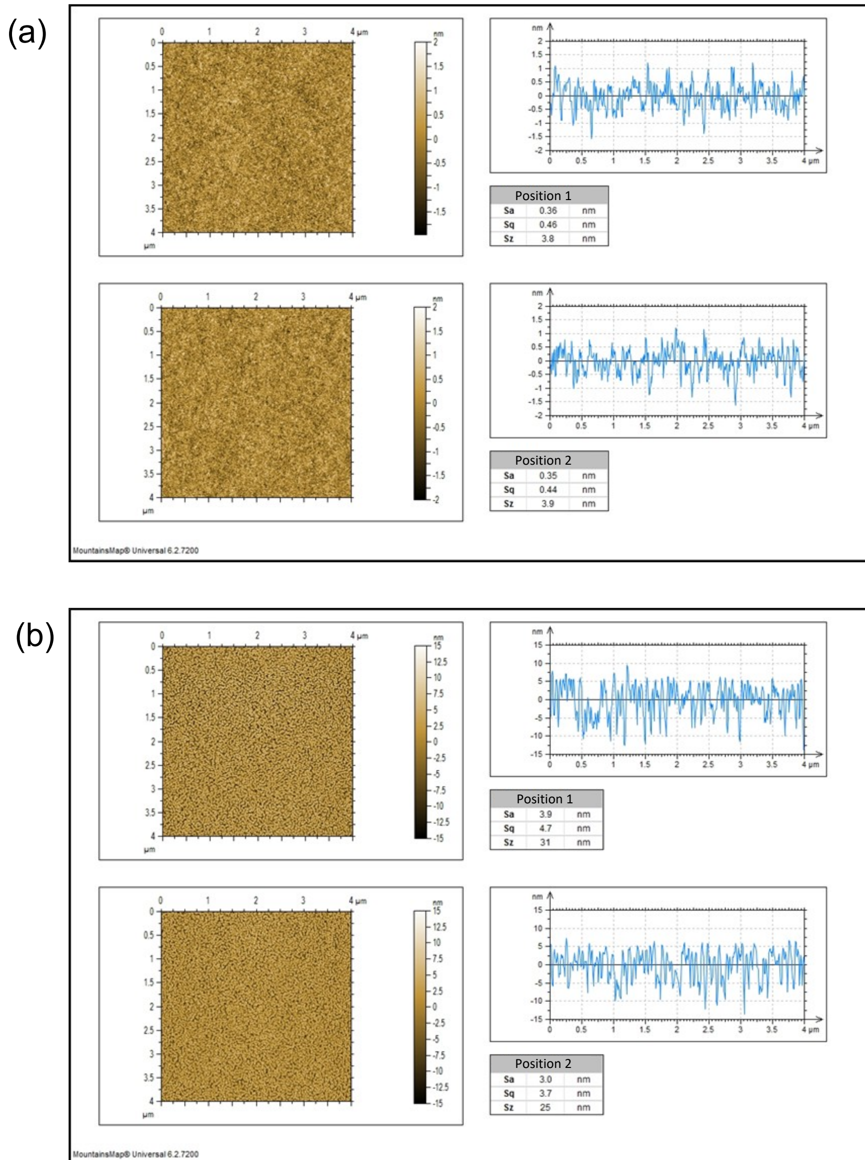

Figure 3.4: Atomic Force Measurements (AFM) topography measurements of (a) non sputtered/bare PI sample and (b) 5 nm sputtered PI sample. Here Sa denotes the arithmetic mean deviation, Sq denotes the root mean square deviation (RMS) and Sz denotes the "Ten Point height" of the surface. Each sample was scanned on two positions, with a scan range 4×4 μm^2. Before scanning the surface was cleaned with de-ionized nitrogen.

of the PI layer for 100, 200 and 600 s causes an increasing surface roughness, which may create better interlocking of the PDMS (Fig. 3.3). The "Ten Point Height" (Rz) of the surface roughnesses measured for the no treatment, 100 s, 200 s and 600 s sputter etched samples were 3.9 nm, 25 nm, 30 nm and 41 nm respectively. The difference in adhesion among the various sputter etch durations could not be measured quantitatively due to the limitation of the testing tool. However, qualitatively the adhesion was found to be consistently good.

SURFACE CHEMICAL COMPOSITIONAL ANALYSIS

Mechanical interlocking of PDMS to PI is assumed to be one of the reasons for the improved adhesion of the sputter etched samples. In order to test for other contributing factors, vibrational surface spectroscopy was done. Characterization of the surface before and after sputtering was carried out using a Fourier Transform Infrared Spectrometer (FTIR) to detect changes in the chemical composition by measuring the infrared absorption spectrum. A non-sputtered polyimide sample was taken as a reference to compare changes in the spectra of different samples after sputtering. Band assignment of residual anhydride is shown in Figure 3.5. Upon sputtering, a decrease in the anhydride peak is observed, which further reduces with the increase in the sputter duration. The initial assumption to this decrease in anhydride is considered to be the effect of temperature during sputtering which would eliminate the residual anhydride from the polymer. To test this assumption, a post thermal treatment at 275 °C for 4 hours and 8 hours was conducted on bare polyimide samples. It was however observed that post thermal treatment does not decrease the amount of anhydride

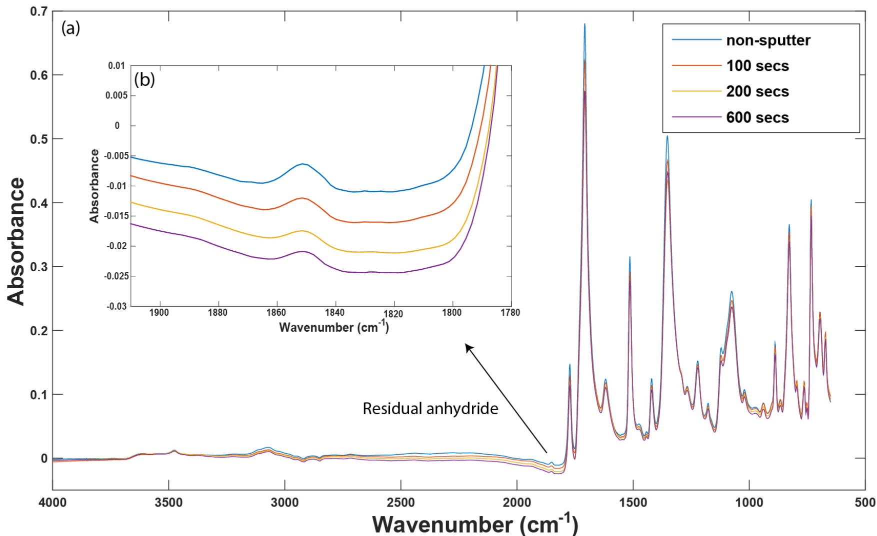

Figure 3.5: (a) a complete FTIR spectra of polyimide 2611 with different sputter durations, (b) showing a decrease in the anhydride peaks with increase in sputter time

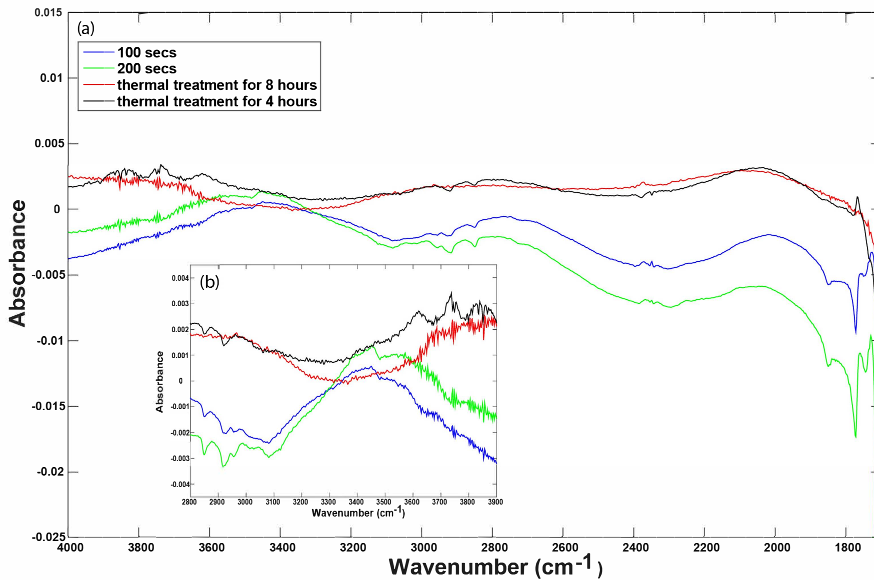

Figure 3.6: (a) Comparative study of sputtered samples with the non-sputtered thermally treated samples, where it is observed that the fringes overlap except for –OH region (>3000 cm^{-1}). In the inset (b) it is observed that there is an increase in –OH group after sputtering for 100 and 200 seconds whereas a decrease is observed with increasing thermal treatment.

groups, so temperature alone does not seem to play a role. Compared to non treated polyimide samples an increase in –OH groups was observed for the sputtered samples, while a decrease in –OH groups was observed for the non-sputtered post-thermally treated samples (Fig. 3.6). It is believed that this might be due to the presence of water vapor either on the surface of the polyimide or on the walls of the sputtering chamber which gets activated by the UV and ions in the plasma during sputtering. This mechanism has been reported in literature [20], where it was found that charged hydroxyl groups from water vapour attach themselves to the surface of a polymer and in this way activate the surface. These hydroxyl ions could also attack the anhydride groups breaking them down into di-acids, but unfortunately the peaks for these two groups can not be readily distinguished.

3.5. BUTYL RUBBER AS AN INTERMEDIATE LAYER

This section reports the use of a rubber- Polybutadiene as an intermediate adhesive layer for improving the adhesion between PI and PDMS [23]. This rubber has low permeability to gases and moisture, as well as chemicals, and is thus being exploited for its good barrier and chemical properties in applications such as packaging of electronic devices. In this section, the adhesive properties of the butyl rubber (BR) will be presented and discussed.

3.5.1. Sample Preparation

In order to test the adhesion of PDMS to PI layers 4 test substrates were prepared. A layer of 5.2 μm PI (2611, HD Microsystems) is spin coated and cured at 275 °C for 3 hours on all the test samples. The classification of these samples is shown in Table 3.1. Sample A is kept as a reference wafer without any surface modification of the PI layer, to compare the adhesion with the treated samples. All the other samples were casted with 15 g of butyl rubber (≈86% n-heptane as the solvent, 4% anti-oxidant and 10% butyl rubber) each which resulted in a 7 μm layer. From previous experiments it was known that the adhesion of PDMS to PI, using BR as the intermediate layer, strongly depends on the amount of cross linking of the BR layer. In order to address this issue, the samples B, C and D were treated differently (explained in the next sub-section). All the samples were then casted with a 10:1 ratio of 11 g PDMS (Sylgard) as a last step, and cured for 30 minutes at 90°C to achieve a thickness of ≈1 mm.

Sample Name			A	B	C	D
Polyimide			✓	✓	✓	✓
Butyl Rubber	Cross Linked			✓		✓
	Non-cross linked	Vacuum			✓	
		Atmospheric Pressure		✓		
PDMS			✓	✓	✓	✓

Table 3.1: Categorization of the samples according to the different experiments performed.

Sample B					
Time (mins)	1	60	120	240	360
Weight of wafer + Butyl Rubber (g)	44.23	39.05	36.82	33.81	31.8
Solvent dissipation rate (g/min)	0.19	0.12	0.12	0.06	
Sample C					
Weight of wafer + Butyl Rubber (g)	37.21	31.81			
Solvent dissipation rate (g/min)	0.12	0.10			

Table 3.2: Solvent evaporation rate of n-heptane with and without desiccator. Bare weight of the samples before casting 15 grams of BR is 30.23 grams.

3.5.2. Butyl Rubber Preparation

Halogenated polybutadiene rubber is used in these experiments which is formed by the polymerization of 1,3- butadiene with a few units of isoprene [24]. The catalyst used in the polymerization process can be either Nd, Co or Li, which results in a mechanically stable linear structure of the rubber. This material is typically used in the manufacturing of car tires, however, with an increase in the percentage of solvent (n-heptane), thin spreadable/spinnable layers can be obtained that can be used in MEMS applications.

In a short loop experiment, a thick layer of butyl rubber (>100 μm) was casted on sam-

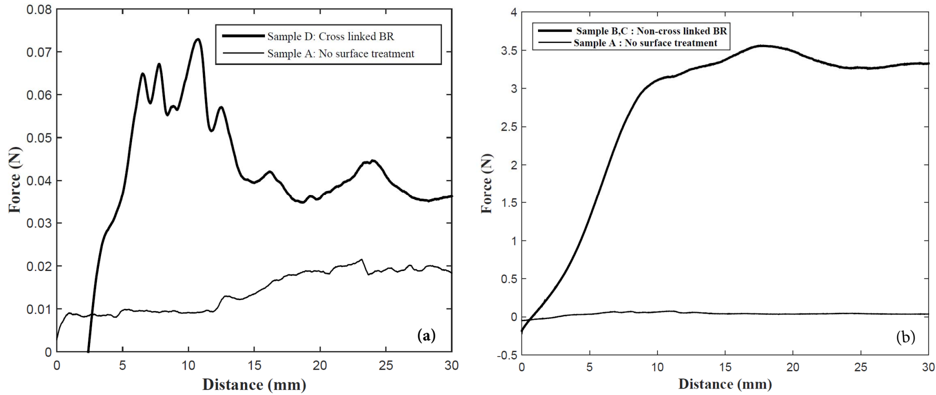

Figure 3.7: (a) Comparison of peel forces measured to peel PDMS from the PI between cross linked BR and no treatment PI surface. The negative forces in the graphs represent the stiffness of the PDMS which pushes against the load cell in the beginning before giving stable force values.(b) Comparison of peel forces measured to peel PDMS from the PI between non-cross linked BR sample and no surface treatment sample.

ples B, C and D. In future this can be replaced with thinner layers, by spin coating the BR. Once the BR is casted, the solvent n-heptane with a very low vapor pressure immediately starts diffusing out from the casted layer. After the extraction of the n-heptane, the molecules of the rubber undergo entanglement with each other, but their cross linking only occurs when the double bonds in their structure are broken by applying external energy like heat or UV. To study the difference in adhesion of PDMS with completely cross-linked BR, and non-cross linked BR, the samples B, C and D were processed differently. Sample D was completely cross linked by baking it at 90°C for 4 hours in ambient environment.

In case of samples B and C, the samples were treated just so as to extract the n-heptane solvent from them. The n-heptane solvent evaporation rate was determined by measuring the decrease in the weight of the wafer at regular intervals of time after casting the BR. This was done at atmospheric pressure (sample B) and in a vacuum desiccator (sample C), and the results are summarized in Table 3.2. From the Table 3.2, it can be seen that within 60 minutes the n- heptane has been removed from sample C, thus making vacuum desiccation the preferred method to remove the solvent from the BR. The texture of samples B and C were observed to be “tacky” after the solvent evaporation, while sample D was completely cross-linked and formed a solid “non-tacky layer” layer.

3.5.3. PEEL MEASUREMENTS

Peel measurements were carried out on a Zwick 1474 Tensile Testing Machine using a load cell of 100 N. An incision, 10 mm wide on a 1 mm thick PDMS sample was made in each sample from the PDMS side cutting through the BR interface and the underlying PI layer. The PDMS layer was peeled from the PI layer over a distance of 30 mm on

each sample with a speed of 10 mm/min. The force required to peel the PDMS from the BR/PI interface was measured for all the samples Figures 3.7 .

3.5.4. RESULTS AND DISCUSSIONS

The peel force for sample A, PI-PDMS interface without any surface treatment or intermediate layer, is measured to be 0.02 N (Fig. 3.7-b). While the force measured for samples B and C, with non-cross linked BR, increases up to ≈3.5 N. However, when the BR is completely cross linked in sample D, the force is measured to be as low as 0.06 N (Fig. 3.7-a).

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Such small forces result in smaller work of adhesion in the cases of samples A and D. The work of adhesion W (energy per unit area) is defined as the work needed to separate two adjacent surfaces. This is expressed in Equation 3.1 as formulated by Rivlin [25] for the peeling of a polymer film from a rigid substrate:

$$W = \left(\frac{F}{b}\right)^2 \times \frac{1}{4Ed} \tag{3.1}$$

Here, F is the mechanical force applied to the PDMS-BR interface to peel it from the substrate, b is the width of the peeled film, d is thickness of the film material and E is the young's modulus of the PDMS (1.84 x 106 Pa). The calculated work of adhesion for peeling PDMS from the rigid substrate is 16.64 J/m^2 for samples B and C, with the non-cross linked BR as the intermediate layer. Whereas, the value of W for the untreated samples and the cured BR samples are 5x10^{-4} J/m^2 and 4x10^{-3} J/m^2 respectively.

According to literature, there are several mechanisms that can play a role in the adhesion such as mechanical, chemical, electrostatic, diffusive and dispersive bonding [26]. The reason why the improvement in the adhesion with the BR as the intermediate layer is observed is because of the chemical and diffusive bonding.

CHEMICAL BONDING

The structure of butyl rubber as seen in Figure 3.8 has several double bonds. The double bonds get oxidized in ambient environment to form –OH groups that react with the PI layer to make polar bonds. The interaction between PI and BR is completely chemical, and hence always consistent irrespective of the crosslinked or non-cross linked state of the BR. In case of a BR-PDMS interface, there are two mechanisms, which can play a part in the adhesion. As depicted in Figure 3.8 the cross linker used in the silicone interacts with the free double bonds of the non-cross linked BR structure, while forming a bridge with the free H atoms in the vinyl terminated polydimethylsiloxane. This reaction is not be possible if the BR is cross linked, because there are no free double bonds for the linking to begin, resulting in a poor adhesion. In Fig. 3.7-a, it can be seen that the cross linked BR sample shows a poor adhesion as compared to a non-cross linked sample, yet it is still slightly better than a no-surface treated sample, likely due to the presence of a few not cross linked BR chains interacting with the cross linker, and by extension with the PDMS. However, the scale and the differences in the peel force of these two samples (cross linked sample and a no-surface treated sample) is too small to make any definitive conclusions.

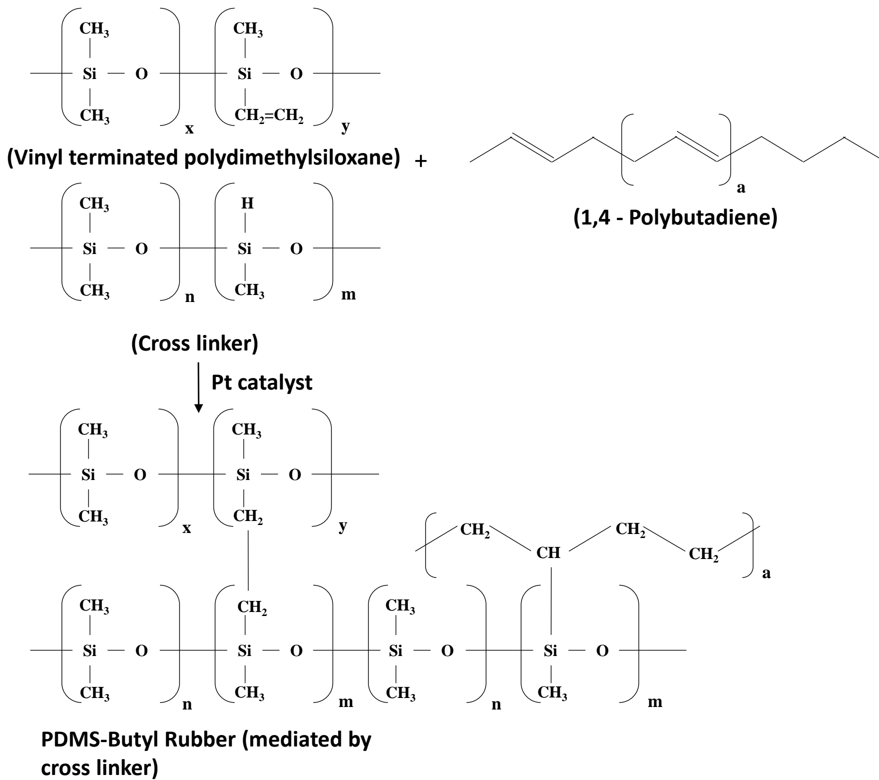

Figure 3.8: Equation depicting the cross linking mechanism between PDMS and Butyl Rubber.

DIFFUSIVE BONDING

Another mechanism that fits well with the interaction of BR-PDMS is diffusive bonding, which describes the mechanical locking between materials at a molecular level [27]. According to this bonding regime, the adhesion is a result of the interdigitation between the free chains of two polymers. This type of bonding is therefore heavily dependent on the freedom of the polymer chains to interlock with each other. In case where one of the polymers is cross linked, its ability to interdigitate is reduced, leading to a reduction in adhesion or even a poor adhesion (Fig. 3.7-a). One effect associated with diffusive bonding, which was also observed in our experiments, is the stringing effect when PDMS is peeled off from the BR-PI stack (Fig. 3.9). This effect is a result of bridge formation by the molecules of the two materials instead of crack formation when the separation begins. According to literature, stringing can apply to both chemical and diffusive bonding regimes, which complies with the two mechanisms we propose.

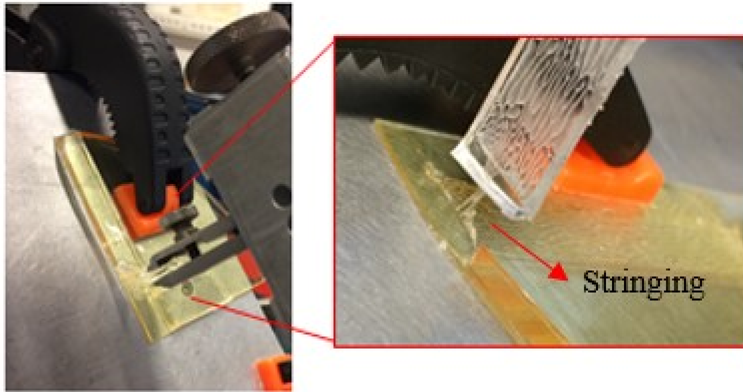

Figure 3.9: 90°C peel measurement of PDMS from BR-PI interface depicting stringing effect [27]

3.6. SUMMARY AND CONCLUSION

The adhesion between PI-PDMS plays a very important role in the fabrication of the patch device. However, due to the inherent low surface energy of PDMS it makes it extremely difficult to adhere to any surface. In this chapter, the adhesion of polyimide to PDMS was investigated and improved using two methods, surface modification and an intermediate adhesion layer. In the first part of the chapter, it was observed qualitatively that adhesion after the oxygen plasma or adhesion promoter treatment showed no significant improvement. However, a strong improvement in adhesion was observed by sputtering the samples in an Ar^+ ion plasma. This can be attributed to the mechanical interlocking of PDMS to the roughened PI surface, and increase in hydrophilicity of the substrate after sputtering, making the substrate more likely for the PDMS to adhere.

This adhesion, however, is prone to change depending on the age of the PI solution. It was observed that an aged PI solution resulted in the aforementioned adhesive property after argon ion sputtering. Upon investigation with FTIR studies (not shown here) it was revealed that the aged PI had more -OH groups from the -COOH of the precursor imide as compared to a new PI solution. Similar studies were revealed in [6] [21] [22], where a deliberate ageing of PI was conducted and the results were compared to a non aged PI. In these studies an increase in surface roughness of BPDA-PDA was observed. It was concluded that the degradation of the PI surface is related to the presence of oxygen, making it more polar and thus getting more activated upon sputtering as compared to an un-aged sample. For this reason, the sputter etch is not considered reproducible enough since the adhesion properties depend on the shelf life of the material. This effect of ageing has been reported only in the BPDA-PDA type polyimides, for certain negative polyimides the effect of such ageing is not seen [28]. Therefore, an alternative to this method was studied whereby the use of rubber— Polybutadiene (non cross linked) as an intermediate adhesive layer improves the adhesion be-

tween polyimide (PI) and silicone polydimethylsiloxane (PDMS). The adhesive bond initiated by the butyl rubber (BR), apart from being extremely strong, is also chemically resistant and mechanically stable. This was finalized as the adhesion improving technique for the complete fabrication flow in the next chapter. An other promising adhesion method which has been reported in the literature is the use of an SiC/SiO_2 intermediate adhesion layer stack [29] [30]. Although this yields a good adhesion between PI/PDMS, the interface cannot be utilized in a stretchable system and hence is not explored in this thesis.

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4

REALISATION OF FREE-STANDING INTERCONNECTS FOR STRETCHABLE BODY PATCHES

In this chapter the integration of the optimized process steps for the free standing interconnects will be implemented in the complete fabrication of the test device. Furthermore, the concept of "PDMS support pillars" will be introduced to prevent large out of plane deformation of large free standing structures, along with a novel method of mechanically interlocking interconnects to such pillars using micro channel cavities. Finally, a completely integrated test device patch is characterized and its reliability is discussed .

4.1. INTRODUCTION

To demonstrate the out-of-plane buckling of horse shoe shaped interconnects upon stretching, the process modules needed for their fabrication have been discussed and tested in the previous chapters. These modules consisted of release mechanisms, release stack selection, hard etch mask selection for polyimide etching, and finally techniques for improving the adhesion between the PI-PDMS interface. In this chapter, the integration of these modules in a final manufacturing process with metal interconnects as well as their stretchability is presented. To avoid redundancy these modules will not be elaborated further in this chapter.

Moreover, new platforms for the stability and reliability of these interconnects in the form of pillars and mechanical anchoring "stitches" will be introduced and implemented. Preliminary stretching experiments performed on these interconnects will be presented, wherein the failure of the device due to PDMS material limitations will also be discussed.

4.2. MASK DESIGN

4.2.1. INTERCONNECTS DESIGN

To test the concept of incorporating free standing interconnects on a stretchable substrate, we investigated the reliability and performance of such structures. For simplicity purposes, the horseshoe design was selected as the shape of the meander interconnects as discussed by Jan Van Fleteren et. al. [1], where it was reported that this shape provides higher stretchability than other structures like zigzag, sinusoidal, U-shape etc. in an embedded stretchable interconnect platform. The 3 cm long free- standing interconnects are designed between bondpads of 2.5 x 2.5 mm. Due to their large size, the test device is therefore referred to as a "patch" in this thesis. The complete width of the interconnect tracks is 160 μm with 100 μm of AlCu (99% Al and 1 % Cu) metal interconnect encapsulated by a 30 μm overlapping polyimide layer.

AlCu is selected as the metal alloy for these structures, as it reportedly has a higher yield strength than pure aluminum, where yield strength is defined as the specific load

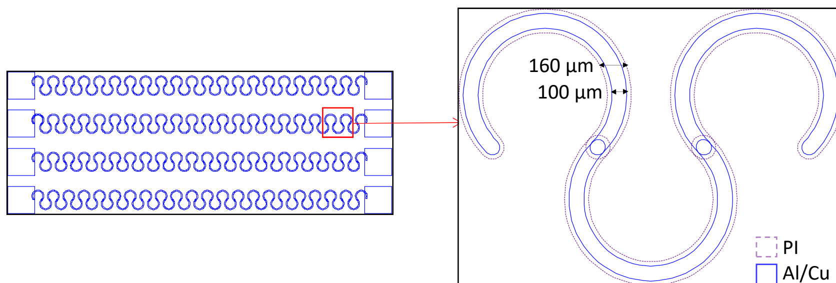


Figure 4.1: Generic horseshoe design for the test structures with 1 μm thick Al/Cu (1%) interconnects encapsulated with 5.2 μm thick polyimide. The polyimide acts as a support and isolating layer for the interconnects. These interconnects are suspended between bondpads and are effectively 3 cm in length.

where the deformations in a material become plastic. The yield strength can be increased by size effects (for very small structures) and/or by addition of other materials in the crystal lattice in the form of alloys. Aluminum copper alloy is also widely used in chip fabrication and MEMS microfabrication to improve the electromigration resistance of the metallization [2].

The metal interconnects were sputter deposited to a thickness of 1 μm. Although for high stretchabilities, due to size effects, thinner interconnects are preferred as plasticity sets in earlier in thicker interconnects. The thickness of 1 μm AlCu was selected to remain compatible with standard MEMS IC processing metallization thicknesses that are in the range of 0.5 - 1.5 μm. The effect of the metal thickness on the design has been reported in [3] and will be discussed later in chapter 5. To delay the onset of plasticity in these large interconnects upon stretching, polyimide is used as an encapsulating and isolating material around the interconnects. The stiffness of the polyimide around the metal interconnects reportedly redistributes the strain throughout the meander, instead of localizing it to a point which on repeated stretch cycles leads to failure [1].

4.2.2. SUPPORT PILLARS

Using the technology platform described in chapter 2, large area interconnects which are mechanically isolated from the substrate can be fabricated. This is done to minimize the forces exerted by the elastomeric substrate on the interconnects upon large stretching, whereby the interconnects are prone to delamination [4]. Although they are not attached to the surface of the polydimethylsiloxane (PDMS), these interconnects are expected to undergo a deflection or “drooping” considering their size and mass. At these relatively large scales "drooping" due to the weight of the interconnects is expected to be significant based on scaling laws [5].

This effect was verified using finite element (FE) simulations, where it was observed that a free standing (non supported) interconnect of 1 cm length displays a deflection effect in the z-axis of 134 μm when gravitational force (body force) is applied on the interconnect (Fig. 4.2) . The spacer resist layer in between the interconnects and the PDMS is selected to be 40 μm in thickness. This thickness can easily be varied upto 100 μm by changing the deposition and exposure parameters. However, the deflection under its own weight is still higher than the maximum resist thickness possible. Due to this drooping effect, the interconnect can stick to the substrate and rupture upon stretching leading to an early failure.

A solution in the form of support pillars for the interconnects is proposed in this section. Placement of such pillars at regular intervals along the meanders will limit the drooping and prevent the stiction of the interconnects to the PDMS substrate. Since the effect of the pillar positions (along the interconnect) on interconnect drooping and maximum stretch is not obvious without appropriate analysis, three pillar positions were considered as depicted in figure. 4.3. FE simulations were preformed to predict the drooping and the maximum elastic stretch corresponding to each of the three configurations.

The FE simulations to predict drooping under the weight of the interconnect and

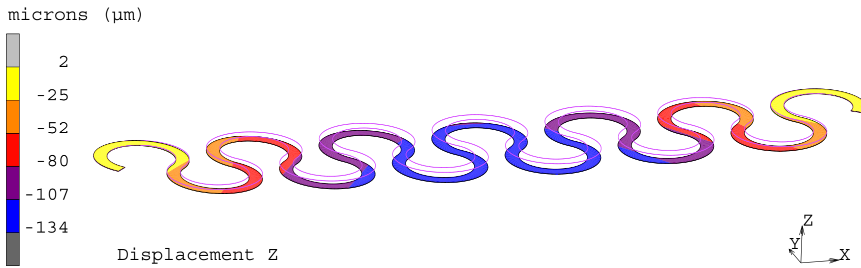
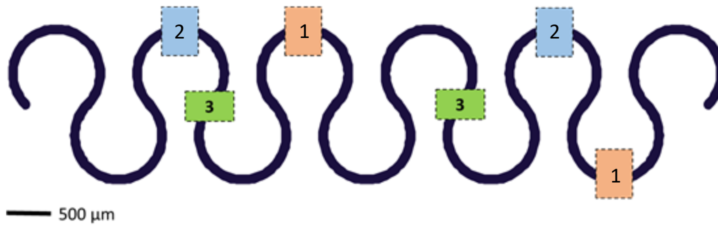


Figure 4.2: Finite element method (FEM) simulation of a 1 cm long interconnect displaying displacement in the z- direction due to drooping under its self-weight. It is to be noted that the complete structure is 3 cm long, which result in even higher drooping than already calculated here.



	Initial length (microns)	Drooping (microns)	Displacement @ stress ~ 75 MPa	Stretch @ stress = 75 MPa
Pillar position 1	3926	-14.1	3091	78.7%
Pillar position 2	4614	-22.7	3892	84.35 %
Pillar position 3	2591	-9.8	2181.72	84.2%

Figure 4.3: (Top) Depiction of pillar positions 1, 2 and 3 over the length of the interconnect placed periodically over the structure. (Bottom) Table indicating the drooping and maximum elastic stretch corresponding to each of the three pillar positions.

subsequent stretching were performed with Marc/Mentat 2014 (a commercial FE package) [1]. The structure was meshed using 20 node brick elements, with three elements through the thickness of the interconnects to capture the bending behavior accurately. The models corresponding to each of the three pillar placement configurations (see figure 4.3) consisted of the interconnect structures between two consecutive pillars. The pillars were modeled with the nodes of the interconnect where the pillars would be attached being rigidly fixed in the out-of-plane (z) direction. To simulate drooping, a body force was prescribed over the whole structure, with the two interconnect ends rigidly fixed along all three coordinate axes. Once the structure had drooped,

[1]These simulations were performed in collaboration with Technische Universiteit Eindhoven, Department of Mechanical Engineering by S.Shafqat.

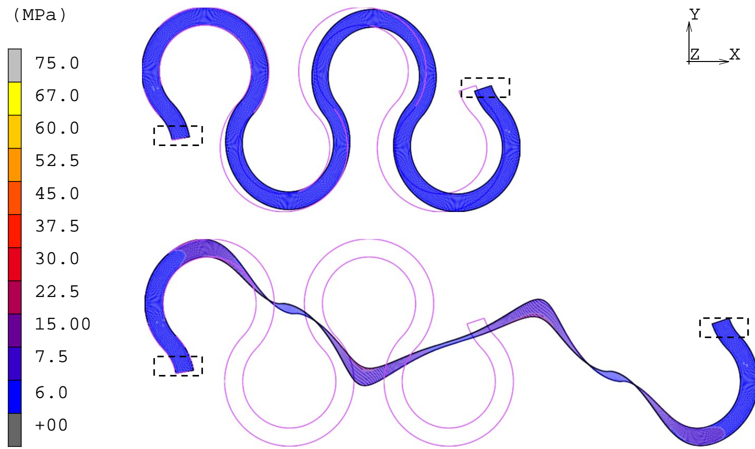


Figure 4.4: Deformation of interconnects structure with the pillars placed at the arms of the interconnects (position 3) with a defined global strain at which the maximum von Mises stress is 75 MPa. As a guide to the eye, boxes representing the pillar position 3 are traced over the simulations

the structure was stretched to calculate its elastic limit for the different pillar placement configurations by applying displacement boundary conditions to the nodes corresponding to the right pillar in the x-direction, while having the nodes corresponding to the left pillar being rigidly fixed along all three coordinate axes. In order to capture the buckling instability during stretching, first, a non-linear solution scheme was used and secondly, an imperfection in the form of a slight, out-of-plane (20 μm) displacement was applied to the right pillar. This along with an adaptive time stepping scheme was enough to capture the buckling instability for all three pillar position configurations. The interconnect deformation was modeled only in the elastic regime, and a Young's modulus and Poisson's ratio of 69 GPa and 0.33 were assumed respectively for the AlCu layer, while for the PI a linearized Young's modulus of 2.5 GPa and a Poisson's ratio of 0.34 was used [6]. In order to compare the structures on the basis of their maximum elastic stretch, a yield strength of 75 MPa was taken and the maximum elastic stretch was defined at the global strain at which the maximum von Mises stress in the structure reached 75 MPa.

The simulations predict that in all three pillar configurations the interconnects are able to buckle out-of-plane (in the same buckling mode) as originally intended. Pillar position 3 (see figure 4.3) provides the best combination with the lowest drooping i.e. 9.8 μm and the highest elastic stretch i.e. 84% (see Table 4.3). Considering the results of the FE analysis, pillar position 3 is selected hereon for fabrication and testing. These pillars are formed by selectively patterning the spacer resist layer on top of the interconnect track such that the PDMS can attach itself on these specific interconnect location (explained in section 1.3). The cross sectional area of the pillar is kept at 600 x 450 μm^2 such that there is enough area for the PDMS to attach to and form a reliable anchoring point for the interconnects. However, since the adhesion of PI with PDMS

is poor, chances of delamination on the pillar locations are high upon elongation of the elastomeric substrate. A solution for this is discussed and presented in the next section.

4.2.3. MECHANICAL ANCHORING

As discussed in the previous section, the size of the support pillars is selected such as there is large enough surface area for the contact of the PI encapsulated metal interconnects with the PDMS pillars, and simultaneously to be small enough so as not to affect the stretching deformation. This poses as a limitation to the amount of force that can be applied to the PI-PDMS interface at the pillar locations, as a result of the relatively poor PI-PDMS adhesion (as discussed in chapter 3). The strength of adhesion between two materials relies on the adhesion mechanism (mechanical, chemical, dispersive etc.) as well as the surface area over which the contact is made between the two materials. The pillars which are necessary to prevent the interconnect from drooping and consequently sticking to the substrate, naturally also constrain the in-plane and more importantly the out-of-plane displacements of the interconnect in the pillar-attached regions.

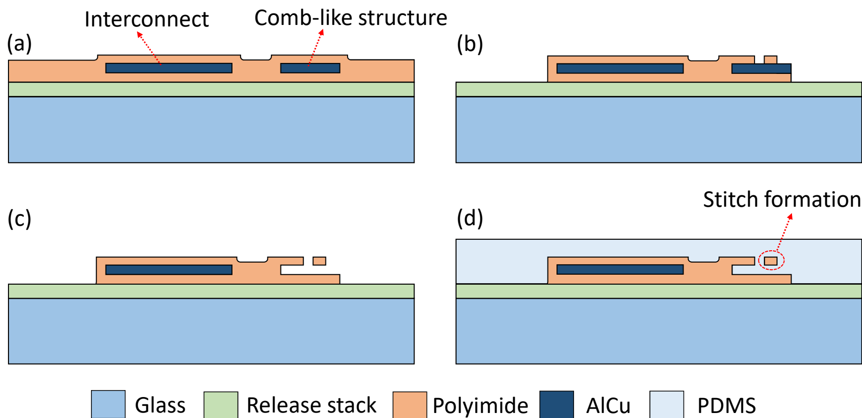


Figure 4.5: Cross sections of the crest/arm of the interconnects in the pillar region where (a) shows the PI encapsulated metal and sacrificial “comb-like” structure on the release stack (PI and Mo). (b) Patterning of the PI around the interconnects, as well as etching a hole on top of the sacrificial structure. (c) Wet etch removal of the sacrificial metal, thus creating a channel. (d) Casting of PDMS as the final step, where it forms a stitch with the fabricated channel.

Therefore, a high adhesion between the pillar and interconnect is required to ensure that the interconnect does not delaminate due to the stresses originating from the constraintment at the interconnect-pillar interface upon stretching. A design to mechanically attach/anchor the PDMS with the interconnects is presented where the simple idea is to fabricate micro channels in the PI layer at the pillar interface such that the PDMS can flow through these channels to form an anchor-like structure, referred to hereon as stitches (Fig. 5.2). In this design, sacrificial “comb-like” AlCu metal structures above the crest or arm of the interconnects are patterned and etched at

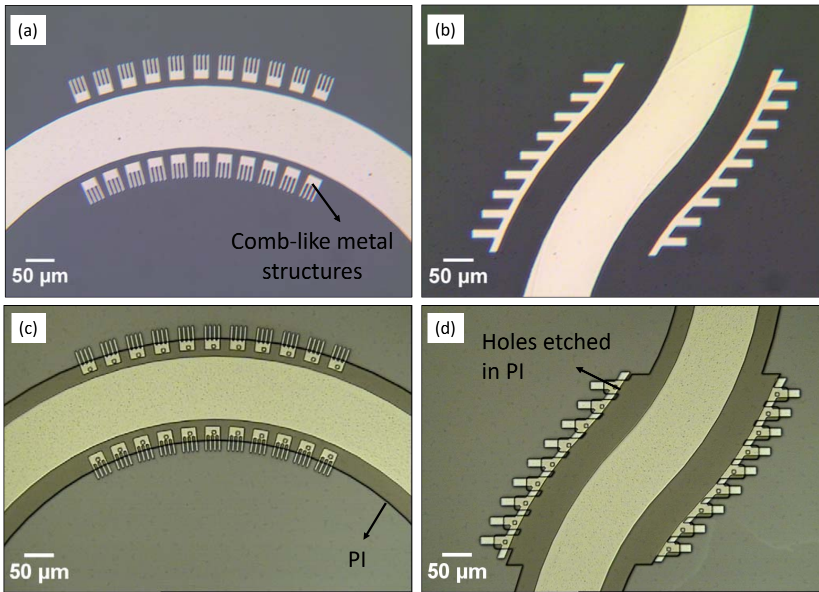


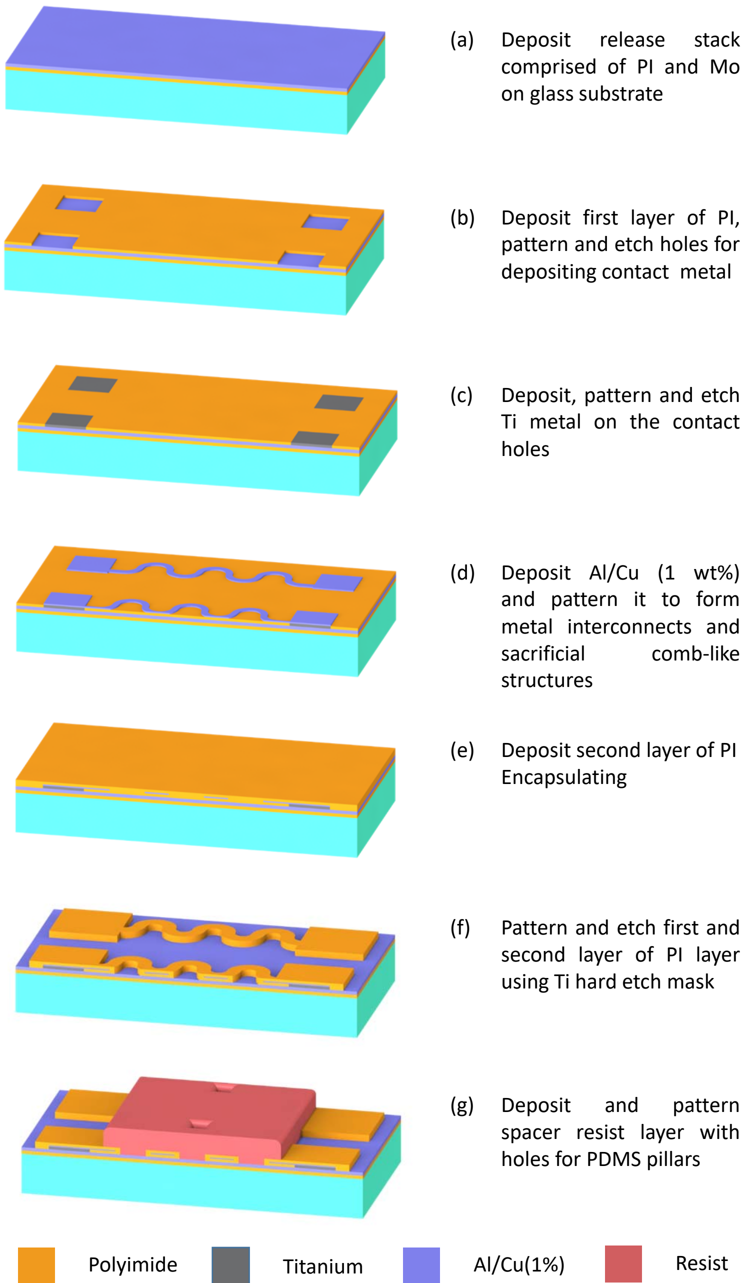
Figure 4.6: Top view optical microscope images of (a),(b) the crest and arm of the interconnects, respectively, with the “comb-like” metal structures. (c),(d) are optical microscope images of the same structures coated with second layer of PI and patterned with holes aligning to the “comb-like” structures. The sacrificial metal is etched in the next step to form channels within the PI.

the same time as the interconnects (Fig. 4.6 -a,b). These structures are embedded in between the two layers of polyimide. After patterning of the polyimide the sacrificial metal structures are automatically exposed and etched using a wet etch to form micro-channel structures (Fig. 4.6-c,d). These channels get filled with PDMS after casting, whereby the elastomer anchors itself mechanically to the PI layer to form the stitches (Fig. 5.2-d).

4.3. COMPLETE FABRICATION FLOW

The fabrication process begins with the spin coating of Polyimide (PI 2611 diluted with 50 wt% NMP, 2000 rpm for 30 seconds) on a 150 mm diameter 400 μm thick AF45 glass substrate. The spin coated PI is soft baked in a convection oven at ambient atmosphere for 20 minutes at 125 °C (for removal of solvent bubbles). Next, it is hard cured at 275 °C for 3 hours in a nitrogen ambient to form a 500 nm thick cured layer of polyimide. This is followed by sputter coating of 200 nm of molybdenum (Veeco 2 Nexus, UHV system) (Fig. 4.7-a). These two layer constitute the release stack of the device, where the introduction of molybdenum as a spacer layer will be explained later.

The next step after the fabrication of the release stack, is the fabrication of the metal interconnect stack. This begins with spin coating 2.1 μm of polyimide (PI 2611, DuPont) at 3000 rpm for 45 seconds followed by curing at 275 °C for 3 hours in a nitrogen ambient (KOYO Thermo Systems Co.Ltd.). Next, contact holes for the electrical


(a) Deposit release stack comprised of PI and Mo on glass substrate
(b) Deposit first layer of PI, pattern and etch holes for depositing contact metal
(c) Deposit, pattern and etch Ti metal on the contact holes
(d) Deposit Al/Cu (1 wt%) and pattern it to form metal interconnects and sacrificial comb-like structures
(e) Deposit second layer of PI Encapsulating
(f) Pattern and etch first and second layer of PI layer using Ti hard etch mask
(g) Deposit and pattern spacer resist layer with holes for PDMS pillars
Polyimide
Titanium
Al/Cu(1%)
Resist

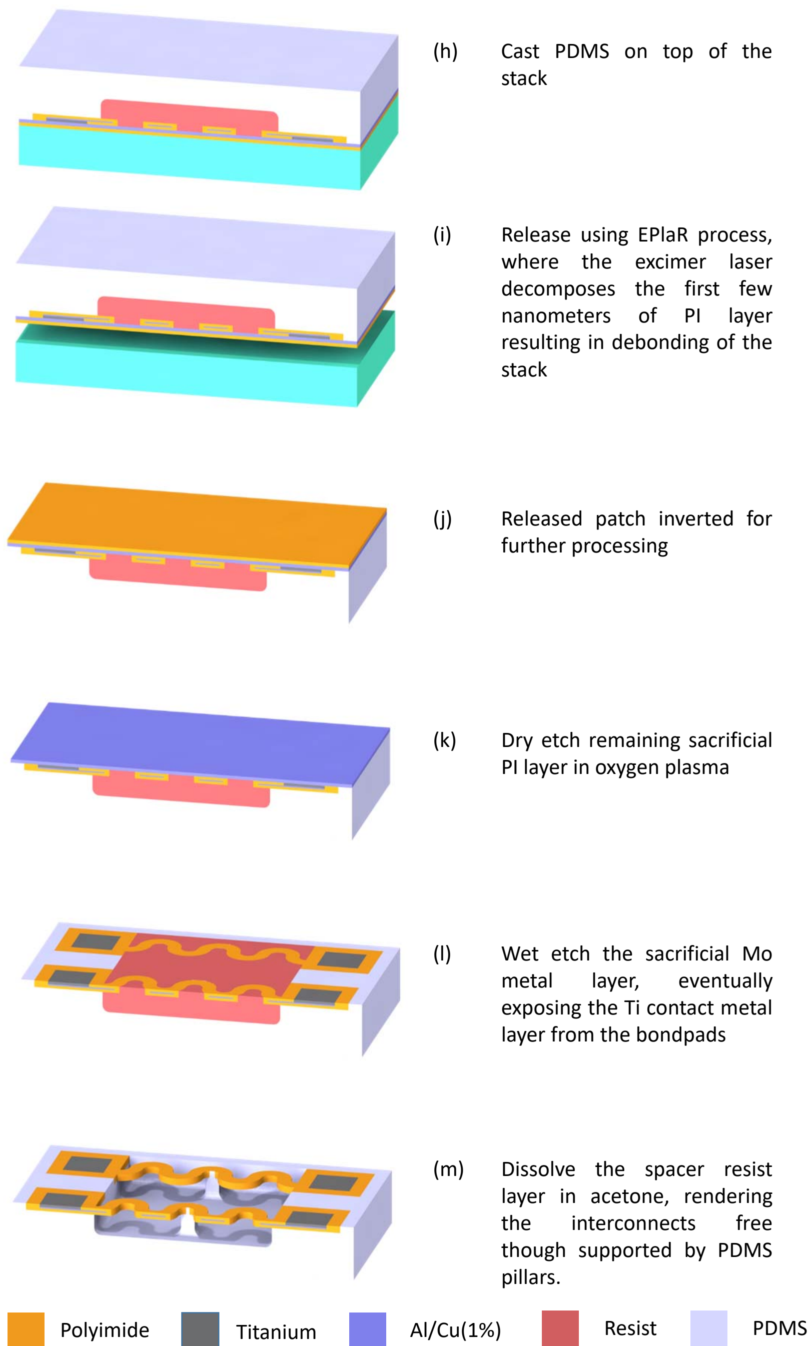


Figure 4.7: Flowchart for the fabrication of the large area interconnect patch.

measurement of the interconnects are etched in the first layer of polyimide by dry etching (ICP RIE, O_2 plasma, 3 min) (Fig. 4.7-b). A 200 nm thick layer of Ti is deposited and patterned (3.6 μm positive photoresist, Energy - 400 mJ/cm^2) such as to form a separation layer between the Mo release layer and the Al interconnects (Fig. 4.7-c). Titanium is used as as it is selective to the wet etch chemistry used to etch the spacer Mo layer in the final steps. After the definition of the contact pads, a 1 μm thick layer of AlCu is sputter deposited. This layer is patterned using positive photo resist and etched in a commercially available wet etchant PES 77-19-04 (30°C) to form the meandering horseshoe shaped interconnect structures, and the sacrificial metal comb-like structures (Fig. 4.7-d). Subsequently, the second layer of 2.1 μm thick polyimide is spin coated and cured similar to the first PI layer (Fig. 4.7-e). To pattern the PI layers, a 200 nm layer of Ti is sputter deposited after a 5 nm Ar $^+$ ion sputter etch. This layer is patterned (3.6 μm HPR photoresist, 400 mJ/cm^2) and etched (ICP RIE Cl_2 plasma, 60 sec) to form a hard etch mask for the etching of the polyimide layers. Using this mask, the polyimide is etched (O_2 plasma, 8 min) and the Ti hard etch mask is removed in HF (1%) . This completes the fabrication of the metal interconnect stack (Fig. 4.7-f).

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Next, in order to make the interconnect structures free standing they are embedded in a 40 μm thick layer of resist (AZ40XT). This resist acts as a spacer layer between the PI meanders and the PDMS layer (Fig. 4.7- g). The resist is patterned and developed to open holes for the definition of the PDMS pillars that support the interconnects. After the resist pillar definition, the metal in the "comb-like" structures (Fig. 4.6) to open the cavities for the stitches is etched in H_3PO_4 commercially available etchant (40 °C) for 15 minutes. This wet chemistry is preferred as it is selective to the molybdenum etch stop layer on the release stack . Prior to this step, an intermediate layer of butyl rubber is spin coated and cured (4 μm) to form a non-tacky layer for the interconnects after release. Second layer of butyl rubber is spin coated (7 μ m) and this layer is not cross-linked so that the PDMS can form an interlocking adhesion mechanism with it, as explained in chapter 3 (not shown here, see appendix). Subsequently, in order to cast 1 mm thick layer of PDMS, 17 g of PDMS was prepared (10:1 curing agent ratio), and casted over the wafer and cured at 90°C for 20 minutes in a convection oven (Fig. 4.7-h). After the frontside processing is completed, the backside of the wafer is irradiated with excimer laser pulses (Fig. 4.7-i) and as explained in chapter 2, this results in the release of the stack from the rigid glass substrate. The released stack is inverted and the polyimide is dry etched in an O_2 plasma (IPC Barrel). This step also *mildly* attacks the PDMS on the other side of the stack, making it rough and brittle. After the PI etching, the Mo spacer layer is etched in PES wet etchant. Finally, the spacer resist layer is dissolved in acetone and the interconnects are rendered free standing with periodic support from the PDMS pillars (Fig. 4.7-m).

4.4. RESULTS AND DISCUSSIONS

4.4.1. STITCH FORMATION

As discussed in sections 1.2.2 and 1.2.3, the pillars for supporting the interconnects and the stitches within the PI encapsulating layers are necessary for mechanical anchoring of the interconnects to the pillars. In order to fabricate these stitches, the

metal in the "comb-like" sacrificial structures (as discussed in the previous section) is etched in wet chemistry (PES etchant) followed by an extensive rinse in deionised (DI) water (Fig. 4.6).

After removal of the metal, channels in between PI-PI with a width of 5 μm and a height/gap of 1 μm are formed. Upon formation of such small micron-sized cavities made from soft and flexible materials, it is known that the capillary vaporization of water after rinsing could lead to bridging of the two surfaces by forming a meniscus [7]. Although polyimide is a relatively stiff material, it is important to confirm the accessibility of these channels for PDMS after etching to ensure a reliable anchoring. The cross section of the cavity after the metal etch as well as after PDMS casting is therefore examined using focussed ion beam (FIB) opening of the structures followed by SEM analysis. In order to visualize the layer stack, a cross-section at the desired position is prepared in the area of interest on samples before and after PDMS casting (Fig. 4.8 and 4.9). Before FIB preparation, the samples are coated with a conductive Pt/Pd-layer (nm range) to avoid charging. Subsequently, a 1 μm thick layer of Pt (I-beam induced) is deposited at the region of interest to protect the top polymer layers during the milling. By using Ga-ions a trapezoidal trench is milled in the surface to create a steep edge (oriented perpendicular to the sample surface) at the region of interest. On the samples coated with PDMS (Fig. 4.9), it was difficult or even impossible to locate the desired position due to poor visibility of the structures in the SEM. An estimation of the location of interest is made in these samples and an approximate cavity position is retrieved using manual slice and view. After focused ion beam polishing, the cross-sections are studied at a tilted angle using a Scanning Electron Microscope (FEI Nova200 NanoLab system, Small Dual Beam). Electron micrographs were recorded using secondary (SE) and/or backscatter electrons (BSE). By using SE-electrons primarily the surface structure is displayed, whereas using BSE-electrons, the difference in (electron) density of the different materials is observed. This implies that areas with a higher density and/or a larger concentration of heavier elements appear brightest, and areas with lower density material are displayed darker. The cross sections of the cavities in Figs. 4.8 and 4.9 show the 1 μm height of the channel after etching of the sacrificial metal and filled channel after being casted and filled with PDMS, respectively.

4.4.2. STRETCHING EXPERIMENTS AND ANALYSIS

To perform some preliminary resistance measurements on the free standing interconnect structures, a patch (5 x 4 cm) with the fabricated test structures reported in the previous sections is singulated from the released PDMS slab by cutting the PDMS around the structures using a scalpel. By using dry and wet etch chemistries the sacrificial release stack layer (PI and Mo) as well as the spacer resist layer were removed (Fig. 4.7- l, m). After rinsing with DI water and air drying, the patch is on two sides attached to metal fixtures/stages (Fig. 4.10). One of the fixture is provided with a metric micrometer that allows for uniaxial motion of the stage in the x-direction with a smallest displacement of 0.01 mm. The sample was attached to the fixtures using a silicone double coated adhesive tape (Teraoka 9030) (Fig. 4.10). The bondpads of the sam-

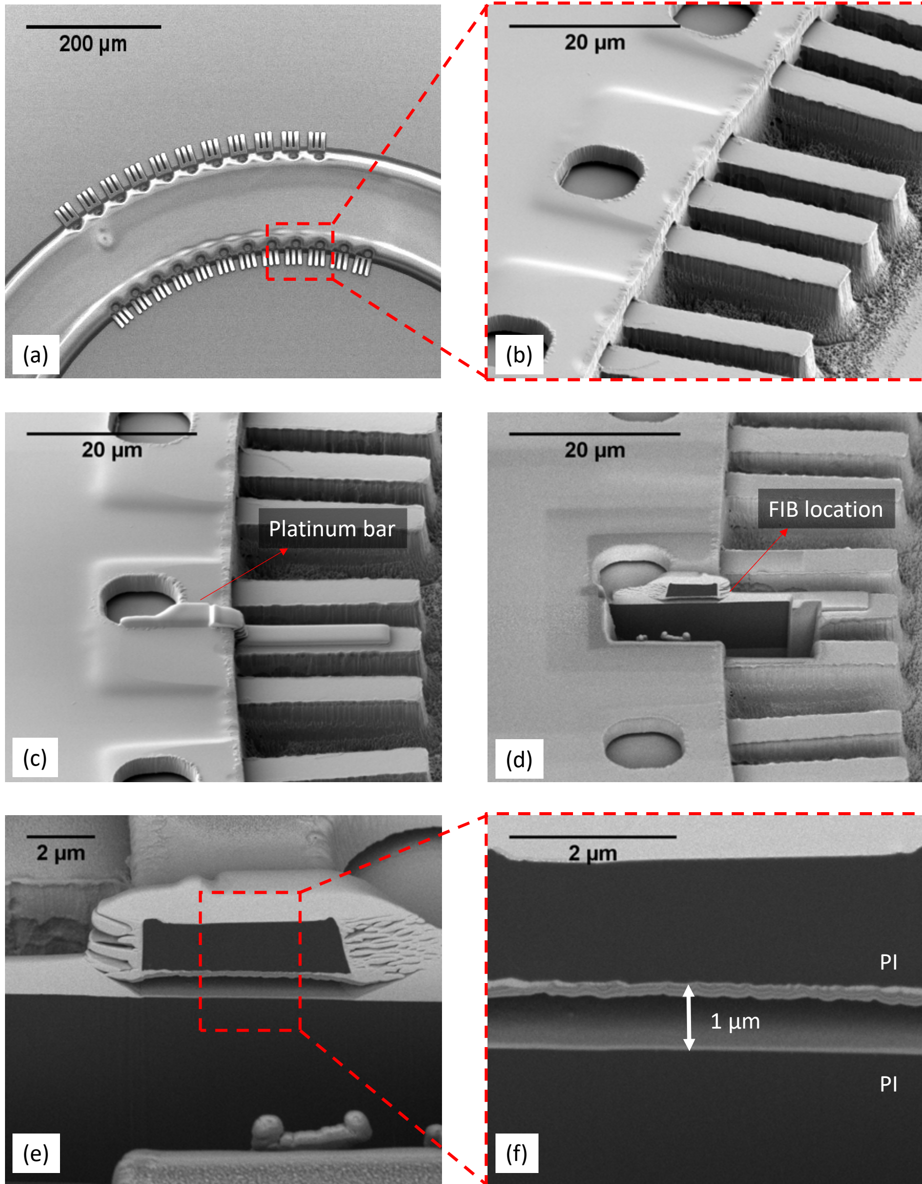

Figure 4.8: (a) SEM micrograph of a top horseshoe interconnect with micro cavities on the top and bottom of the structure. (b) Magnified view of one of the cavities from which the Al has been etched. (c) Sample preparation for FIB analysis by ion beam induced deposition of 1-2 μm Pt- layer to protect the top layer during ion milling. (d) Ion milled cross section of the cavity. (e) Closer view of the ion milled cross section with contrast between polyimide and Platinum redeposited layer in the cavit. (f) SEM micrograph showing the cavity open with height as the estimated 1 μm post etching of the sacrificial Al/Cu.

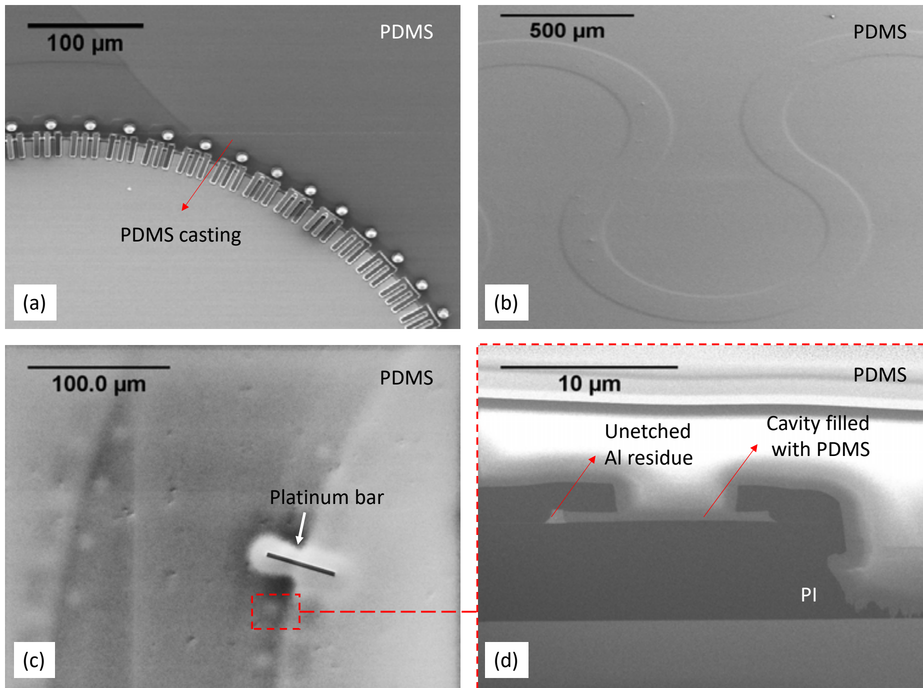

Figure 4.9: (a) SEM micrograph of a top horseshoe interconnect with micro cavities after casting of PDMS (b) Overview of the interconnect embedded in PDMS after curing (c) Sample preparation for FIB analysis by ion beam induced deposition of 1-2 μm Pt- layer bar to protect the top layer during ion milling. (d) Magnified SEM image of the ion milled cross section depicting the filling of PDMS inside the micro cavities after its casting and curing, with unetched Al residue due to shorter etch of the sacfricial metal. This residue is removed after a longer duration metal etch.

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ples were located on the rigid part of the fixture. The adhesion between the silicone of the sample and the tacky silicone of the tape is observed to be very good. In this way clamping of the sample could avoided which may deform the sample from the edges, and further deform the interconnect structures. The two metal fixtures are positioned on top of a glass plate using similar silicone adhesive tape, such as to restrict any movement of the stages during the measurement. Next, two flexible insulated wires are contacted to the bondpads with a conductive silver paint adhesive (Leitsilber 200), which is dried in air overnight. These are further connected to a digital multimeter and the resistance is recorded throughout the measurements.

The sample is stretched from one side using the revolution of the spindle on the micrometer that applies a displacement of 0.5 mm per revolution. The resistance is recorded on every 5 % stretch increase of the original length of the sample (global strain). To study the elastic stretchability, at each step with increased applied displacement, the sample is relaxed and returned to its original configuration such as to study the onset of any plasticity. No systematic shape change as well as resistance change

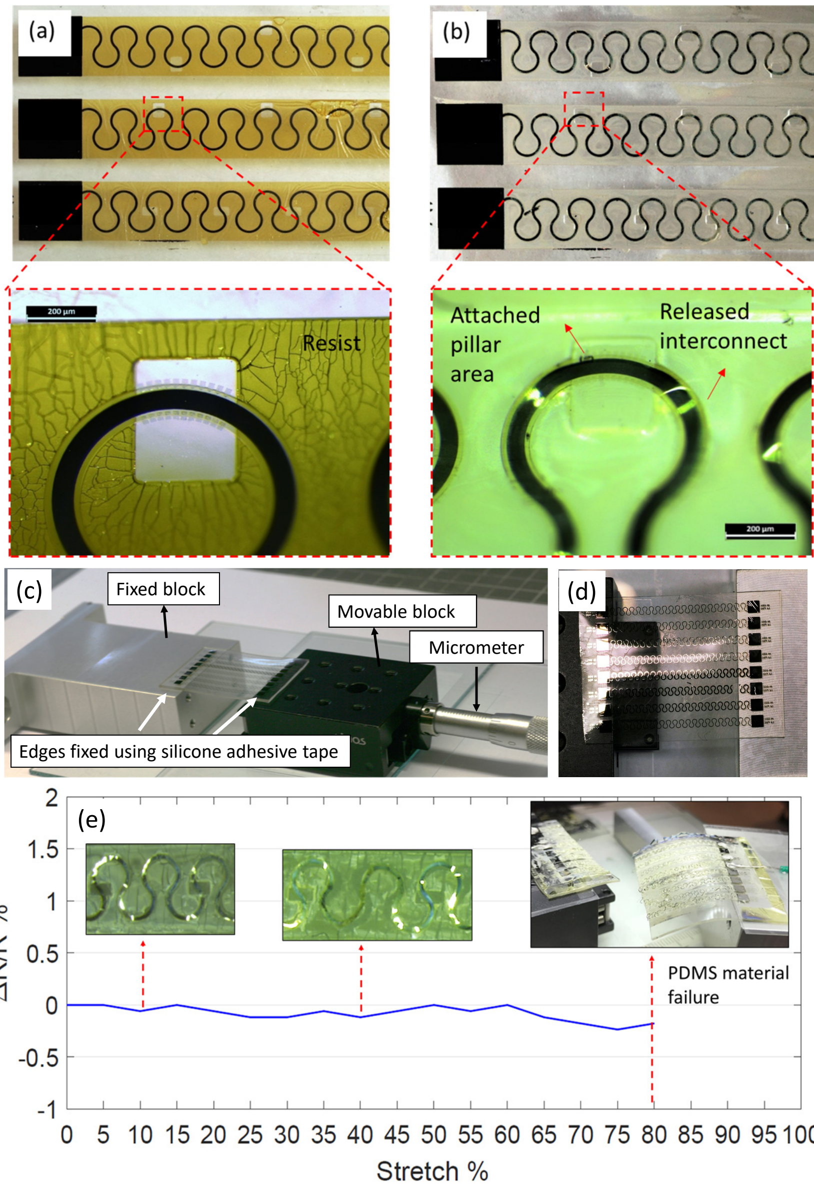

Figure 4.10: Optical microscope image of the top view of the patch where (a) the interconnects are embedded in a thick spacer resist layer which is cracked after the release and handling of the patch and (b) after the removal of the resist layer, whereby the interconnects are free from the substrate and attached only to the pillars stitches. The cracks are not detrimental to the metal interconnects tracks due to the stiff polyimide layer around it. (c) Measurement setup consisting of two metal fixtures, whereby one fixture is provided with a micrometer, using which the (fixed) sample is stretched in the x-direction. (d) Top view of the adhered sample before stretching. (e) Change in resistance versus stretching measurement portraying the >0.4% change in the resistance of the interconnects while stretching. The inset sample shows the failure of the patch device after a stretch of 80% due to cracks generated in PDMS.

is observed on the structures till 80 % of stretch. After increasing the loading beyond 80 %, the sample fractured and broke into two halves (Fig. 4.10), thus rupturing the interconnects.

In one of the final steps for the realization of the patch, polyimide is etched in an oxygen plasma (120 W, 100 °C, 90 min) before the sacrificial metal layer is wet etched. Upon microscopic inspection (not shown here), crack formation was observed on the surface of PDMS post plasma exposure. As also dicussed in the work of Catarinuzzi et. al. [8], after exposure of PDMS to oxygen plasma, height contrast images revealed a banded morphology of cracks formed on the surface. Fracture bands perpendicular to the stretch direction are prominent and are presented in their work which increase with increased strain. These fracture bands, which may be the cause of the material failure in our samples, are formed due to the densification of the PDMS surface after plasma treatment, which in turn increases the stiffness of the material. Bowden et. al. also presented formation of porous silica as a consequence of plasma oxidation, which implies significant embrittlement in terms of mechanics [9]. The premature rupturing of the PDMS on applying strains greater than 80 % can be contributed to the embrittlement of the PDMS as well as the micro crack induced at the edge of the patch as a result of the manual cutting of the sample from the total PDMS slab. However, the results shown in this chapter are limited and do not form a quantitative analysis. For future work to assess a good balance between limited embrittlement and higher stretchability of the PDMS should be performed.

4

4.5. CONCLUSIONS

Technology for the succesful realisation of free standing large area horse shoe interconnects has been presented in this chapter, whereby these interconnects demonstrate reversible stretchability upto 80 % without change in resistance. This has been demonstrated by utilizing the out of plane bending of the horseshoe design of the interconnects. To prevent drooping of the large structures, PDMS pillars are placed along these structures and “stitches” are implemented to prevent the delamination of the interconnects from the pillars on stretching.

However, it was found that although the release process “EPlaR” delivers the desired results and works well for the release of the patch, removal of the sacrificial release stack layers is not ideal. Exposure to oxygen plasma during removal of the sacrificial polyimide, also leads to surface densification of the exposed PDMS layer which causes the top surface of the PDMS to be brittle. Formation of cracks due to this surface modification leads to an early failure of the PDMS material upon stretching, leading to a device failure. Since no change was observed in the performance of the interconnects upon stretching, it can be therefore safely suggested that they may be stretched more than 80 %. For future work, it is suggested to investigate different techniques for the removal of the sacrificial PI etch after laser release. Furthermore, testing of such structures on a large area patch is not straightforward, so for the fabrication of free standing micron sized interconnects; which will be discussed next; testing is as an integral part in the design of the device.

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5

MICRON-SIZED FREE-STANDING INTERCONNECTS

A device for studying the mechanical and electrical behavior of free-standing microfabricated metal structures, subjected to a very large deformation is presented in this chapter. The free-standing structures are intended to serve as interconnects in high-density, highly stretchable electronic circuits. For an easy, damage-free handling and mounting of these free-standing structures, the device is designed to be fabricated as a single chip / unit that is separated into two independently movable parts after it is fixed in the tensile test stage. Furthermore, the fabrication method allows for test structures of different geometries to be easily fabricated on the same substrate. The utility of the device has been demonstrated by stretching the free-standing interconnect structures in excess of 1000% while simultaneously measuring their electrical resistance. Important design considerations and encountered processing challenges and their solutions are discussed in this chapter.

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5.1. INTRODUCTION

An increasing number of medical instruments are using micro-fabricated devices as the interface between machines and the human body (or living tissue in general). Examples include smart body patches [1] [2], electronic skin, implantable devices [3] [4], and organ-on-chip devices [5] [6]. While biological tissue is soft, bendable and to some extent stretchable, most micro-fabricated devices are hard, rigid, flat and have sharp edges. For the successful integration of living tissue and electronics, the electronic components need to adapt to the mechanical properties of the living tissue. By assembling electronic components on compliant substrates like PDMS or polyurethane, with mechanical properties close to human tissue, applications such as body patches, neural electrodes [7] and tunable hemispherical cameras have already been demonstrated [8]. These devices are fabricated using, what can be generally characterized as a hybrid approach towards making stretchable electronics: the combination of rigid islands that contain the required functionality attached to a stretchable substrate (Fig. 5.1). A crucial part of such devices are the stretchable interconnects between the rigid islands, since their behavior determines the maximum stretchability and reliability of the entire system.

In most of these hybrid approaches, the planar spring-like interconnects are embedded into the stretchable substrate itself [1] [9]. Although this directly isolates the interconnects from each other, it also limits their stretchability. Under large global stretching, high shear stresses build up at the interface between the embedded interconnect and the substrate, resulting in delamination and subsequent failure [10]. For high stretchability applications recent research [11] [12] [13] [14] [15] has therefore focused on completely free-standing interconnects that are fully detached from the stretchable substrate, and hence can freely bend and twist out of plane in order to accommodate much larger stretching. In order to design more compliant and reliable stretchable electronic circuits using free-standing interconnects, a better understanding of their mechanical and electrical behaviour under large global stretching is needed. The application area of the structures to be tested is not limited only to stretchable electronic circuits but can include any type of free-standing structures with different application such as for example interconnects used for mechanical isolation of material samples for cryogenic measurements [16].

For the characterization of micro-machined materials, where due to size effects mechanical properties often differ significantly from those at macro scale, test systems have been developed that perform material testing (tensile and bending test) on micron-size samples [17] [18] [19] [20]. Apart from material testing, it is important to study the deformation of the interconnect structure itself, as it would be loaded in the actual application, before fabricating the whole device. For the characterization of such structures, a testing approach is required that allows for the application of very large displacements to test structures with the same size, shape and microstructure as in the final application, while providing a solution to prevent loading of these fragile structures before the test. On-chip testing techniques are well suited for well controlled loading of fragile free-standing structures. However, the currently available on-chip testing techniques [21] do not allow the structures to be tested under very

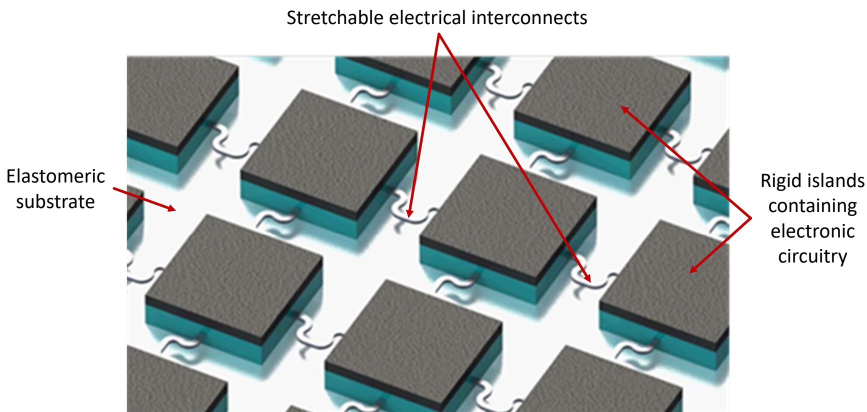

Figure 5.1: A conceptual illustration of a hybrid stretchable electronics circuit. The rigid islands that contain the electronic functionality are attached to a stretchable substrate and interconnected by (e.g. horse-shoe shaped) free-standing metal interconnects. The overall stretchability of the circuit is mainly determined by the stretchability of the free-standing interconnects.

large displacements, requiring a new type of test device and test setup.

In this paper, a test device for electrical and mechanical characterization of free-standing structures suspended over a micron-sized gap is proposed. The fabrication flow of the device allows a variety of free-standing structures with different geometries to be fabricated and tested, making it a versatile testing platform. The device consist of two beams between which the structures are suspended. When the beams are moved apart, the structures between them are loaded and the resulting deformations can be observed by means of optical microscopy, scanning electron microscopy or profilometry. For a complete characterization, the electrical resistance is measured in-situ as a function of displacement. The device is fabricated using standard silicon micromachining which allows for high precision and reproducibility of the fabrication process, while using already available manufacturing equipment. Such processes and equipment are typically used to process micron-size stretchable interconnects and structures. Large number of stretchable electronic circuits are built by using fabrication technologies different from silicon micromachining using polymer or textile substrates [22] [23]. It is important to point out that only materials that are compatible with the silicon micromachining fabrication flow can be used. This means structures built from materials such as metals that are sputtered or evaporated can be easily studied, while structures made from organic materials do not lend themselves to testing with the proposed device since they are not compatible with the fabrication flow.

5.2. CONCEPT DISCUSSION

5.2.1. REQUIREMENTS

The characterization of the mechanical properties of micron-size interconnects subjected to large global displacement, demands for the fulfillment of a combination of

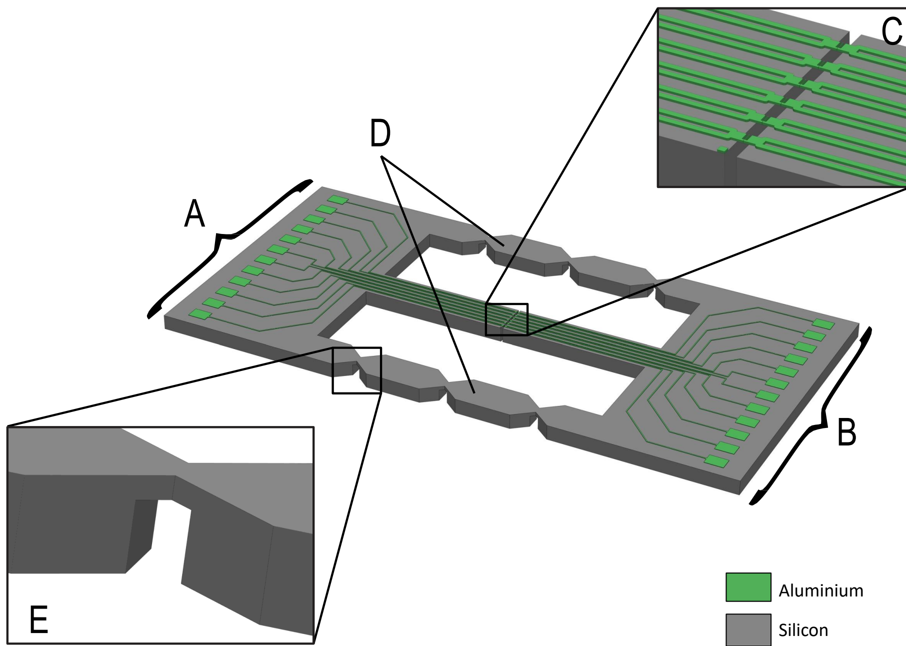

Figure 5.2: Schematic representation of the test chip. Here, A and B represent the main islands in between which the interconnects are suspended, shown in C. These interconnects are kept in place by the two temporary support beams, represented by D, each containing three v-notches. In order to break these notches easily the thickness of the Si is reduced, as shown in E.

requirements for the test setup. Upon review of the available MEMS based actuators [21], no suitable technology that can provide both the required stretchability and displacement precision was found. This eliminates the possibility of simultaneously manufacturing the test structures and actuators on the same chip, as commonly done for testing micron-scale structures. Since the size of the interconnects is very small, their direct handling is impossible without causing damage. Therefore, the test device onto which the interconnects are to be fabricated should be designed in a way that allows for safe transport and mounting in the test setup. Furthermore, a possibility to simultaneously measure the resistance of the individual interconnects needs to be integrated in the test device. Additionally, the device has to be designed such that various deformations modes of different types of structures can be explored. In order to do so, different structure geometries spanning different test gaps (free-standing lengths) need to be fabricated. Finally, the fabrication process chosen for the manufacturing of the test devices should not affect the microstructure and the resulting mechanical properties of the interconnects.

5.2.2. DESIGN

Keeping the above requirements in mind, a test device for testing of the micron-size interconnect structures is designed (Fig. 5.2). The device consists of two main islands

(A and B in Fig. 5.2) between which the free standing interconnects are suspended (C in Fig. 5.2). To perform the tensile test, the islands are fixed in a micro tensile stage, in such a way that the islands can move independently in a controlled and precise manner. On the islands, metal tracks that are connected to the interconnects are designed in such a way that electrical measurements can be carried out during the tensile test. The miniaturized design allows for 4-probe electrical resistance of all six parallel interconnects, simultaneously with applied stretch, thus conveniently allowing to study the evolution of electrical resistance during quasi-static and cyclic loading.

In order to execute the test, the two islands (A and B) need to be moved independently. However, the interconnects suspended between them are very fragile, and therefore any uncontrolled movement before the test should be avoided. To ensure safe transport and straightforward mounting into the test stage, the chip is designed as a single rigid frame where the islands A and B are connected by the temporary support beams D (Fig. 5.2) that prevent spurious motion between the main islands. After the device has been safely mounted into the test stage, the support beams D are broken off, and the chip is split into two parts that can move independently. To avoid the risk of spurious motion during fracture due to a large release of energy, notches E (Fig. 5.2) are designed in the support beams. Since the beams are weaker at these notch locations, they will break at those locations instead of at any arbitrary point in the structure of the test device. The breaking point locations have been selected in such a way as not to damage the main islands or the free standing interconnects.

5.3. EXPERIMENT

The manufacturing technology that was used for the fabrication of the test devices is based on the Flex-to-Rigid (F2R) technology [24]. The F2R platform is used in the manufacturing of smart minimally invasive surgical instruments such as intravascular ultrasound (IVUS) catheters [25], where arrays of MEMS ultra-sound transducers and driver electronics need to be packed in the very small volume available at the tip of the instrument. To allow for the manufacturing of the free-standing interconnects, the fabrication flow for the test chips has been modified compared to the fabrication flow for the F2R technology [24] [25].

The fabrication begins with the deposition of a 1μm and 5 μm thick layer of PECVD silicon oxide (Novellus PECVD concept one) on the front and back side of a 150 mm double side polished 400 μm thick Si substrate (P-doped, Boron <100>), respectively (Fig. 5.3 a). The backside SiO_2 is patterned (3.5 μm HPR504 positive resist, OCG Microelectronic Materials N.V, Energy-160 mJ/cm^2, ASML PAS5500 stepper) into a two level hard etch mask (Fig. 5.3 b-c) and etched (STS ACP tool, CF_4 plasma, 9 min).This two level hard etch mask is used towards the end of the fabrication flow to define the outer shape, the gaps underneath the freestanding interconnects, and the thinned down areas of the device. After etching of the back side oxide, the resist mask is removed in acetone. The front side processing starts with sputter deposition of 200 nm thick layer of aluminum (Veeco 2 Nexus, UHV system with 99.99999% Al target purity and 2 nm/sec deposition rate). Next, a resist layer is patterned (1.2 μm SPR660 positive resist, Energy- 160 mJ, ASML PAS5500 stepper) and developed (AZ400K de-

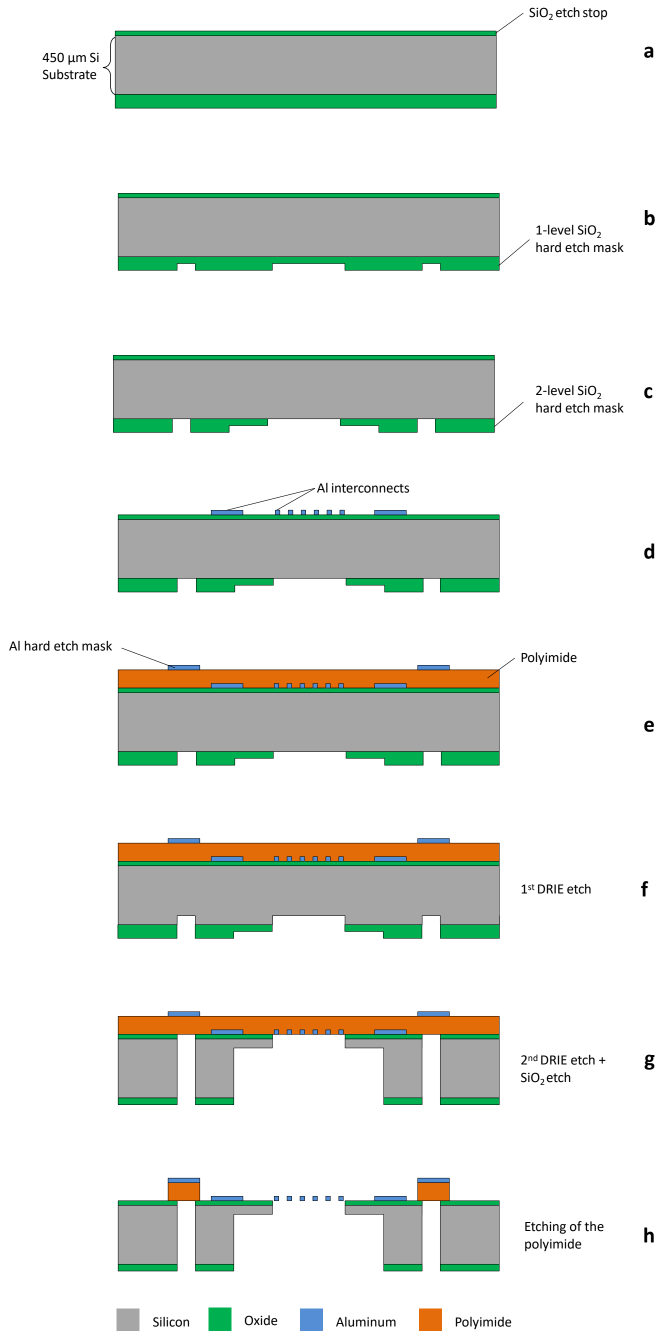

Figure 5.3: Cross-sectional view of the fabrication flow of the test device.

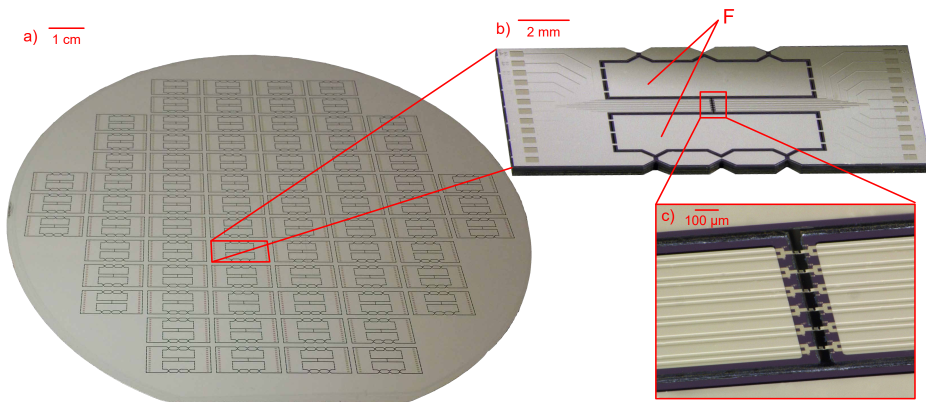

Figure 5.4: a) A photograph of a completely processed wafer containing a number of test chips, held in the wafer frame by means of PI tabs. b) A single test chip taken out of the wafer frame. The silicon areas next to the beams, denoted by F, are sacrificial and are removed before mounting. c) A magnified image of the test structures that are freely suspended between the beams of the test chip.

veloper). Using this resist mask, the aluminum is dry etched (STS ICP Clustertool, Cl_2 chemistry plasma, 5 mTorr) defining the desired interconnect patterns along with the re-routing layer and the bond pads (Fig. 5.3 d). The resist mask is removed by dry etching in a barrel by O_2 plasma (600 W, 150 °C, 15 minutes, IPC9200 from PVA Tepla). Next, a 5.2 μm thick layer of polyimide (PI 2611, DuPont) is spin coated at 3000 rpm for 45 seconds and cured at 275 °C for 3 hours in a nitrogen ambient (KOYO Thermo Systems Co.Ltd.). After curing of the polyimide a 200 nm thick layer of aluminum is sputter coated (Veeco 2 Nexus) on top of the polyimide. The Al layer is patterned (3.6 μm HPR504 positive resist, Energy- 160 mJ, ASML PAS5500 stepper) and wet etched at 30 °C in a commercially available wet etchant (PES 77-19-04) consisting of phosphoric acid (H_3PO_4), nitric acid (HNO_3) and acetic acid (CH_3COOH), with an etch rate of 95 nm/min (Fig. 5.3 e). This Al layer is used as a hard etch mask at the end of the fabrication process to etch the underlying polyimide layer. In the next step, the wafer is etched from the back side by means of Deep Reactive Ion Etching (DRIE), using the silicon oxide hard etch mask defined earlier. In order to form narrow and deep trenches, the Si etching is performed in two steps.

First, an advance etch of 200 μm is performed (SF_6+ C_4F_8 gases, 20 min in STS PEG Tool) using the first level of the hard etch mask (Fig. 5.3 f). This is followed by a short silicon oxide etch (CF_4 chemistry plasma, 9 min in STS APS Tool) which opens up the second level of the hard etch mask that defines the wider trenches. Using this second level mask, the silicon etch is continued (SF_6+ C_4F_8 gases, 20 min DRIE in STS PEG Tool) until the oxide on the front side of the wafer is reached and subsequently etched (CF_4 gas, 22 min in STS APS Tool). The trenches formed by the DRIE define the general shape (outline) of the silicon islands. This two-step approach serves two purposes. Firstly, it allows the relatively narrow trenches to be defined on the back side of the

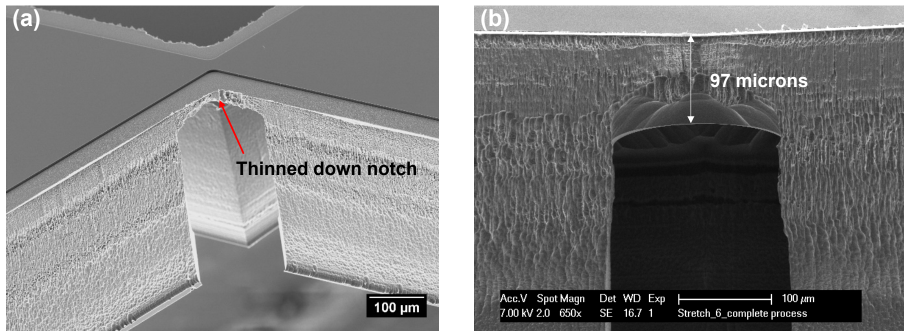

Figure 5.5: (a) SEM image of the notching points of the beams. (b) The pre-designed reduction of thickness of the temporary support beams at the v-notch points is clearly visible in the SEM cross section.

wafer, and be precisely transferred through etching to the front side. Secondly, it also allows the substrate to be thinned down at selected locations. This is especially useful in cases where the breaking points of the support beams are to be defined (notches E in Fig. 5.2). After the second and final DRIE step (Fig. 5.3 g) the test devices are completely shaped.

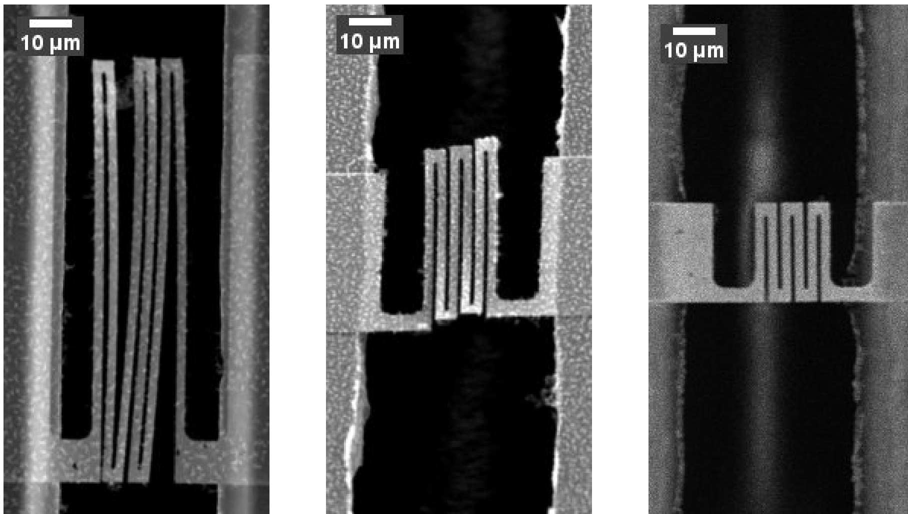

Figure 5.6: SEM pictures showing free standing test structures with different dimensions spanning a 50 μm test gap fabricated on the same substrate. The picture demonstrates that different test structures can be fabricated on the same substrate using the same fabrication process.

The polyimide (PI) layer on the front side of the wafer separates the test devices from the bulk of the wafer, and holds them into place. In the final processing step, the PI is dry etched in an oxygen plasma (6 min RIE in STS ICP tool), using the pre-patterned aluminum hard etch mask (Fig. 5.3 h). After etching the devices remain

attached to the frame of the wafer by a small number of PI tabs. By laser cutting the PI tabs, these test devices can be removed from the main frame for mounting in the test stage. The rigid temporary support beams prevent loading of the interconnects, thereby reducing the chance of damaging the delicate structures.

5.4. Results and Discussions

5.4.1. Fabrication of Test Device

To test the manufacturing feasibility of the proposed characterization platform, a number of highly-stretchable free-standing test structures with different geometries were fabricated. Other types of free-standing structures can be manufactured and tested as well. The design of the test chips allowed for 76 devices to be fabricated onto a single 150 mm diameter Si wafer (Fig. 5.4 a). At the end of the fabrication process, the test devices remain suspended to the main frame of the wafer, held in place only by means of the polyimide tabs. These PI tabs allows for easy separation and removal of the devices from the wafer without incurring damage to the test structures unlike in a dicing process.

The two step DRIE process allows for the formation of thinned down areas. This has been utilized to reduce the thickness of the supporting beams at the v-notch points (Fig. 5.5). This allows for a controlled breaking of the silicon beams without the need to use excessive force. The two step DRIE also allows for test chips with different width of the test gaps to be manufactured on the same wafer. Since both the test structure geometry and test gap widths are defined by lithography, test devices with different structures were fabricated on the same wafer (Fig. 5.6).

Various processing issues were encountered during the fabrication of the test chip. A short discussion of the most relevant issues and their solutions are described in the following section.

5.4.2. Fabrication Challenges

One of the most important issues is uncontrolled thinning of the supporting beams at the v-notch points of the device, as this affects the overall mechanical stability of the test device. If the notches are too thin, the chip will disintegrate when handled or even during processing (Fig. 5.7 a). Conversely, if the beams are too thick, too much force will be needed to break them, resulting in uncontrolled separation or elastic recoil, which may pre-deform the interconnects. Therefore, the first DRIE etch was carefully optimized in such a way that the second DRIE step stops precisely at the correct thickness of the notches. It was determined that for this design and geometry thickness of 100 μm resulted in v-notches that were easily breakable, while still being sturdy enough to sustain the handling of the device (Fig. 5.5).

The final step in the releasing of the interconnects includes the dry etching of PI in an oxygen plasma. After the etching of the PI is completed, remnants are observed on the surface and around the interconnects (Fig. 5.7 b). Remnants after etching of PI have been observed before [26] [27], and they have been traced back to PI types that include primers containing siloxane groups which cannot be etched in an oxygen plasma. In this work a polyimide (PI2611, DuPont) without primer was used, ruling out

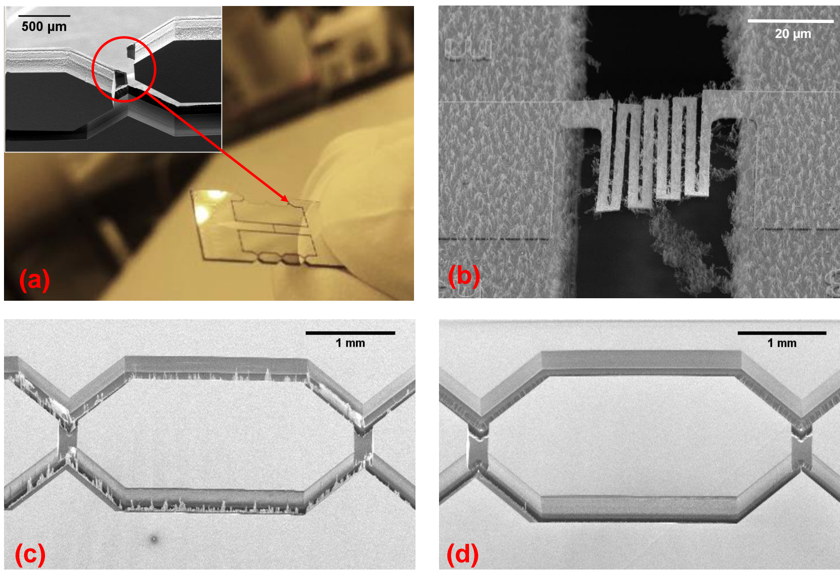

Figure 5.7: (a) A test device with a premature (directly after processing) breaking of the supporting beams at the v-notch points (see Fig.5.5) due to excessive thinning (fracture of the v-notch shown in inset). (b) Free standing interconnects after PI etch covered with residues. (c) SEM micrograph showing the back side of a test chip where remnants in the forms of spikes are visible, which are caused by the passivation that has been left over from the first step of the DRIE etch. (d) SEM micrograph of the same area of the device after an isotropic silicon etch shows the successful removal of the remnants

this possibility. An explanation was found in the combination of Al sputter deposition and the wet etching process. apparently Al metal clusters get attached on or into the PI surface which cannot be removed with wet etching (Chapter 6). Due to the small size, non-dense structure and the density of the observed remnants it is reasonable to assume that they do not have a significant effect on the working mechanism of the interconnects (Fig. 5.8). However, in order to avoid the formation of the remnants in the future, it was proposed to dry etch the Al mask before PI etching. Dry etching of Al mask with a slight overetch resulted in a residue-free PI etching. The slight overetch erodes the surface of the PI where the Al mask remnants are embedded [28].

Another issue observed during processing are "spikes" in the trenches on the back side of the wafer left after the two step DRIE (Fig. 5.7 c). Due to incomplete removal of the passivation deposited during the first step of the DRIE (etching of narrow trenches), there are areas where the silicon is not completely etched after the second DRIE, resulting in the formation of these "spikes". These residues generally do not present a problem to the functioning of the chip, but can pose a health hazard if inhaled and serve as a source of contamination for the processing equipment. The problem has been resolved by executing a short isotropic silicon etch after the anisotropic DRIE etching has been completed (Fig. 5.7 d).

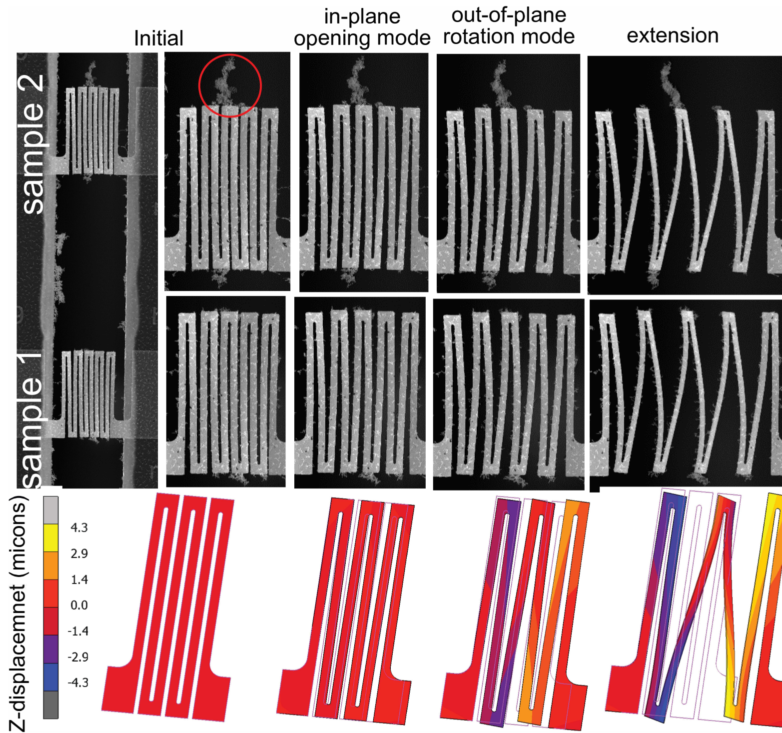

Figure 5.8: SEM images of two interconnect samples showcasing their opening mechanism. Bridging from the PI remnants is encircled in the figure on sample 2. When compared with the FEM simulation results, both samples follow the same modes as predicted by the simulation. This highlights that the influence of these residues on the basic working mechanism of the interconnect is negligible.

5.4.3. TEST SETUP AND MOUNTING

Since mounting and testing of highly stretchable free-standing structures is not trivial and the design of the test chip is aimed at addressing the handling challenges, to demonstrate the capabilities of the platform the test devices were mounted and characterized. The following description of the mounting and measurement of the test structures is meant to serve merely as a demonstration of the capabilities of the test platform and is not intended as a discussion of the properties of the specific structure. For a more detailed discussion of the design and electro-mechanical properties of the structures shown, please refer to [14].

The characterization tests are performed by first singulating test devices from the wafer by cutting the polyimide tabs. Next, this device is clamped to two acrylic blocks providing a flat top surface (Fig. 5.9). The device is attached to the blocks by gluing both ends on the top surface of the acrylic clamps with a UV-curable adhesive (Loxeal 58-11) (Fig. 5.9 b). The use of UV-curable adhesive allows to ensure a good alignment with respect to the loading direction. Once a precise alignment of the device with respect to the clamps is achieved, the adhesive is UV cured. Subsequently, the

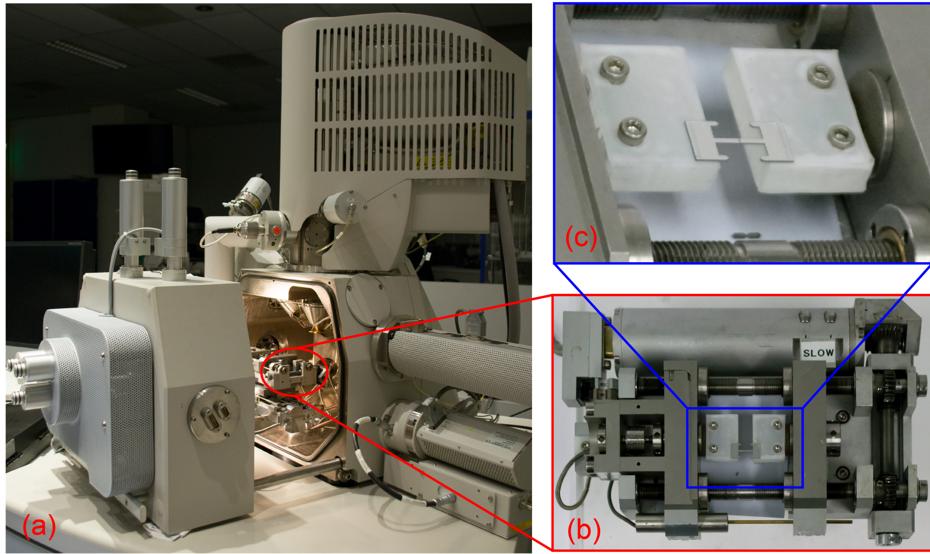

Figure 5.9: a) An SEM with a commercially available micro-tensile stage mounted in it. b) A top view of the micro-tensile test stage with the test chip mounted on it. c) A perspective view of the mounted test chip. The temporary support beams that provide mechanical stability during transport and mounting of the test chip have been removed.

silicon beams (Fig.5.2 (E)) that keep the two islands of the test-chip connected with each other, are broken to allow for free movement of the Si islands, so that the interconnects can be stretched. The crystallographic orientation of the silicon substrate (<100>) is aligned to the width of the notches to allow crack propagation along it to break the beams in a controlled fashion (Fig. 5.9 c). The notched silicon beams based test design ensures that the test device is robust with respect to in-plane loads, while a controlled small amount of downwards force applied in the center of the beams generates sufficient moment in the notches to break them. Furthermore, since the beams connect to the test interconnects through the main islands (Fig. 5.2 (A and B)), which are clamped in the test setup, the transmission of the energy released during the beam breaking to the test interconnect is minimized. After breaking the beams, the two test device islands are now only connected by the freestanding interconnects and are free to be displaced with respect to each other to perform the tensile test (Fig. 5.10). The tensile stage used in the current experiment allows the application of uniaxial stretching. In most of the applications of stretchable electronics multi-axial global strain is usually encountered. The limitation in this respect is posed by the tensile stage itself and is not an inherent limitation of the test chip. By designing a different tensile stage setup multi-axial strain can be applied to the test structures without changing the design of the test chips.

To illustrate what type of measurements can be performed with the proposed test chip platform, a high resolution in-situ mechanical test was performed inside a large

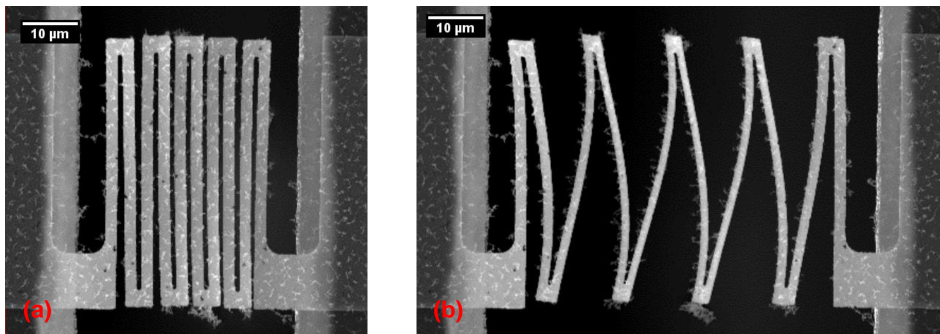

Figure 5.10: Two in-situ SEM images showing the same interconnect in (a) initial and (b) stretched condition. The images demonstrate that the test structures fabricated in the test device can be strained inside the SEM as designed.

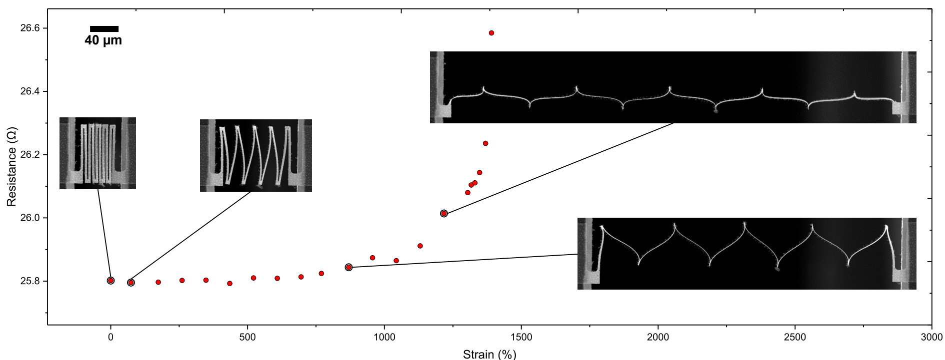

Figure 5.11: To demonstrate the capabilities of the test platform the resistance of the interconnect structure was measured as a function of applied displacement/ strain. The test was performed under an optical microscope to avoid any effects of the SEM electron beam with the electrical resistance measurements. To clearly show the deformation states of the structures SEM micrographs have been included.

chamber SEM (Fig. 5.9) to determine the maximum reversible and irreversible stretch of special free standing interconnects that were designed by partner Shafqatfrom the Eindhoven University of Technology to provide maximum stretchability by allowing the interconnect to tilt out of planed [**?**]. After each loading step (of increasingly higher stretch), the interconnects are unloaded to the initial configuration to study the effects of plastic deformation. The results show that with stretchability of up to 623% the interconnects can recover their original shape (Fig. 5.11), thus indicating that the stretch is reversible. Beyond this point the effect of plasticity can be clearly seen in the unloaded interconnect shape (Fig. 5.11). The interconnects are further stretched almost to a straight wire (Fig. 5.11), at a stretchability of 1240%, beyond which point the interconnects fracture. Furthermore, four-probe electrical resistance measurements were preformed with simultaneous mechanical loading to study the effects of deformation on the evolution of electrical resistance. The test was performed

under an optical microscope to avoid any interference of the SEM electron beam with the electrical resistance measurements. The results show that the electrical resistance stays stable even into the plastic regime, e.g. at stretchability of 1108% the electrical resistance varies by only by 0.4% with respect to the initial configuration. Only once the interconnect is completely stretched out in extreme plasticity, the electrical resistance varies by 3%. Two regimes in the electrical resistance evolution (Fig. 5.11) can be identified, as also discussed by [29], [30], [31]. In the first regime till 623%, in which the interconnect stretches elastically, the electrical resistance increase is minute. Beyond 623%, due to the onset of plasticity and possible damage accumulation (not visible in SEM images), the electrical resistance starts to increase exponentially till the interconnect fracture. For more detailed discussion on the testing of similar free-standing structures, please refer to [14]. These successful mechanical and electrical characterization tests demonstrate the utility of the test chip platform discussed in this paper.

5.5. CONCLUSION

The development of stretchable devices and circuits (by means of hybrid technology) requires accurate characterization of the mechanical and electrical properties of all the components in these systems. This is especially true for structures such as the stretchable interconnects as they form a crucial part of the system. Due to further developments in the field of stretchable electronics, there is a push towards high-density stretchable electronics devices, which requires small (micron-sized) interconnect footprints and high stretchability. The testing of such micron-sized free-standing interconnects is known to be challenging. In this paper, we present a microfabricated test device that allows highly stretchable/compliant micron-sized structures to be handled so that they can be successfully mounted and tested in a micro-tensile stage. The test device in which the structures to be tested are suspended is robust and rigid. The device is designed in such a way that after mounting it on the test set-up, it is split into two independently moving parts by the controlled removal of two supporting silicon beams. The concept was successfully demonstrated by repeatedly stretching micron-size interconnect to 2000% reversibly, while the resistance is measured simultaneously. Finally, the design of the device allows for the fabrication of free-standing test structures with different shapes, and spanning different test gaps in the same wafer. The test chip platform is generic, as it allows for the integration of various kinds of microfabricated structures such as strain gages, displacement sensors and actuators, and even active electronics.

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6

RESIDUE FREE DRY PATTERNING OF POLYIMIDE

It was found that oxygen plasma etching of polyimide (PI) with aluminum (Al) as a hard-etch mask results in lightly textured arbitrary shaped "fur-like" residues. Upon investigation, the presence of Al was detected in these residues. Ruling out several causes of metal contamination that were already reported in literature, a new theory for the presence of the metal containing residues is described. Furthermore, different methods for the residue free etching of PI using an Al hard-etch mask by using different metal deposition and patterning methods are explored. A "fur-free" procedure for the etching of PI using a one-step reactive ion etch of the metal hard-etch mask is presented.

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6.1. INTRODUCTION

Polyimides (PI) are thermosetting ring chain polymers comprising of repeating chains of imide monomers. Polyimides are extensively used in Micro-Electro-Mechanical Systems (MEMS) devices because of their outstanding properties such as excellent chemical resistance [1], high thermal stability [2], high mechanical strength [3][4] and good dielectric properties [5][6]. Polyimides are used as sacrificial layers, structural layers, isolation layers and as substrate material in flexible/stretchable electronic circuits [7]. A good example of a technology that makes use of many of the aforementioned properties of PI is the Flex-to-Rigid technology (F2R) [8]. F2R was developed to assemble complex electronic systems, such as for ultra-sound imaging, on the tip of smart-catheters. It enables the fabrication of arbitrary shaped Si islands containing sensors and electronics that are fabricated by through-wafer DRIE etching and that after etching remain suspended in the silicon wafer by tiny PI tabs (Fig. 6.1). The rigid silicon sensor islands are interconnected using stretchable metal interconnects embedded in the PI. Here the PI acts as a substrate as well as an isolation layer for the interconnects. Dry etching of this PI layer renders the embedded interconnect layer free. These free standing interconnects [9] can bend out of plane when stretched, increasing the stretchability of the device in Fig. 6.1.

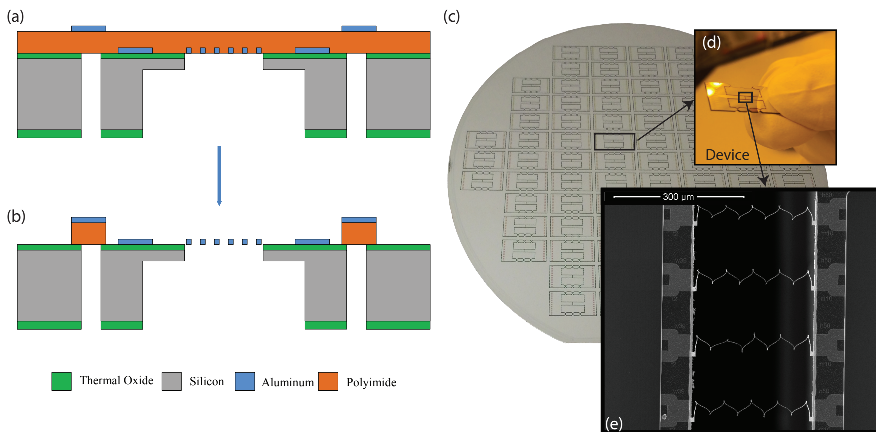

Figure 6.1: On the left, flowchart depicting the cross section of a wafer for the fabrication of free standing interconnect structures where (a) the metal interconnects are embedded in PI. After the reactive ion etch (RIE) etch of PI, (b) the interconnects are rendered free standing while the PI tabs remain. On the right, (c) a 6-inch test device wafer with the sacrificial PI tabs holding the devices together after the RIE etch. These tabs can be easily cut using laser to (d) isolate the device from the wafer. Upon stretching of the device, as seen in the SEM (e) the free standing interconnects bend out of plane to enhance the stretchability. The device is elaborately explained in the literature from Shafqat. S et. al. [9]

Polyimides can be of two types: photosensitive and non-photosensitive. In this paper, only non-photosensitive polyimides will be addressed. Patterning of the PI can be achieved by using either a resist mask or a hard-etch mask. In general, the selection

of a mask is based on firstly, the selectivity of the etch process towards the mask, and secondly, it's ease of integration as a masking material in the flowchart. Polyimide is usually dry-etched in gas mixtures primarily containing oxygen. This makes the selectivity of the etch towards resist very poor so that consecutively the mask erodes rapidly during the plasma etching. The selectivity of the PI etch with a photoresist mask is 1:1, implying that the PI and resist layers are etched at an equal rate. This requires the resist mask to be at least as thick as the underlying layer of PI. Thick resists, however, have a limitation for high resolution lithography, for both positive and negative tone resists. An alternative that has been adopted in the microfabrication industry, is the use of a hard-etch mask. In this approach, a metal layer like Al, Ti, Mo etc. is used as a mask for the patterning of the underlying PI layer, where the mask is unaffected by the plasma chemistry of the PI etch. However, according to literature [10], the adhesion of a metal layer to an untreated surface of polyimide is poor due to its low specific surface energy. For a proper adhesion of the metal mask to the PI, a short Ar^+ sputter-etch of the polymer surface is recommended [10]. The metal layer is then patterned using a resist mask in the desired shape for the etching of PI. Prior to the etching of PI, the photoresist is stripped in acetone.

The plasma chemistry used for the etching of PI consists of oxygen radicals which break the unsaturated groups within the chemical structure of the polyimide. After etching of the polyimide using an Al metal mask, residues on the etched areas were observed. These residues were arbitrary in shape, and appeared light in texture, and for ease of understanding will be referred to as "fur-like" residues in this paper. Similar residues have been reported in the literature [11][12], wherein the silicon content in the self priming and silicone modified polyimides played a role. In this paper, however, we do not use either of the polyimides, thus eliminating the cause of the aforementioned occurence of the residues after reactive ion etching. The presence of these residues is undesirable as it leads to process instability and may interfere with the subsequent microfabrication steps. An interesting outlook towards these residues could be to harness them for the formation of nanowires, black silicon. However, it will be not be discussed in this paper as it is beyond the scope of this study.

The goal of this work is to investigate the origin/nature of these "fur-like" residues and provide solutions compatible with the microfabrication of PI-based electronics. Different hypothesis explaining the origin of the fur-like residues were tested by variations in process conditions and material analysis techniques (SEM, EDX, AFM and Raman). The experimental section describes the general processing flow employed to realize the PI-based devices/structures and motivation for the several short loop experiments and hypothesis. The subsequent sections discuss results for each hypothesis. Finally, devices are demonstrated that were fabricated through improved processing conditions, which eliminated the fur-problem, while maintaining compatibility with advanced MEMS- processing flows.

6.2. EXPERIMENTS

Exper-iment	Sample	PI surface preparation	Al mask deposition	Photoresist mask	Al mask etch	Hypothesis	Residues observed
1	R	Ar 100	Sputtering	**Yes**	PES	Metal redeposition	Yes
	A	Ar 100	Sputtering	**No**	Bl. PES		Yes
2	R	**Ar 100**	Sputtering	Yes	PES	Effect of PI	Yes
	B	**N/a**	Sputtering	Yes	PES	surface preparation	No
3	R	Ar 100	Sputtering	Yes	**PES**	Metal mask inclusions	Yes
	C	Ar 100	Sputtering	Yes	**Dry**		No
4	D	N/a	**Sputtering**	Yes	PES	Mask deposition	No
	E	N/a	**Evaporation**	Yes	PES	method	No
R		Reference sample					
Ar 100		100 s Ar^+ sputter etch					
PES		Wet chemical etchant (heated etch at 30°C) consisting of H_3PO_4, HNO_3 and CH_3COOH					
Bl. PES		Blanket PES wet etch					
Dry		Reactive ion etching (RIE) in a Cl_2 chemistry (5 mTorr) with 15 s overetch					

Table 6.1: Short loop experiments designed for investigation of the PI residues with stated hypothesis and results for each experiment. Varying parameters of each experiment are depicted in red and bold text in the table.

The presence of the residues was first observed during the fabrication of a device wafer with test structures to characterize free-standing interconnects [9] (Fig. 6.1) [Chapter 5]. The wafer has a pre-defined and patterned 5 μm PECVD SiO_2 hard etch mask (Novellus PECVD concept one) on the backside. This back oxide mask is used to completely etch through 400 μm of Si (30 min in SF_6 + C_4F_8 DRIE plasma, STS ICP tool) on certain predefined locations such as to render the top metal structures free from the underlying substrate (Fig.6.1-a). These top metal structures are embedded in a 5.2 μm thick PI (Dupont 2611) layer which is spin coated at 3000 rpm for 45 seconds and cured at 275°C for 3 hours in a nitrogen oven (KOYO Thermo Systems Co.Ltd., Japan). This polyimide layer acts as both sacrificial layer to embed and protect the final free standing interconnect structures, as well as for sacrificial tabs (Fig. 6.1-b). These tabs keep the devices attached to the wafer and are released by laser or scalpel cutting (Fig. 6.1-c and d) as explained in chapter 5. To obtain a good adhesion between polyimide and Al hard etch mask, the surface of polyimide is sputter etched in an Ar^+ ion plasma (50 sccm Ar gas, 300 W, 100 s in Veeco 2 Nexus, UHV system), where the charged Ar^+ ions accelerate towards the PI surface creating micro roughness on the surface as well as chemically modifying the PI structure [13]. This is done to ensure a good chemical as well as mechanical bonding of metals like Al, Cu, Ni etc. to PI, which can be challenging due to its low surface energy [14]. Next, a 200 nm layer of Aluminum is sputter coated (Veeco 2 Nexus, UHV system with 99.99999% Al target purity and 2 nm/sec deposition rate) on top of the PI layer. This Al hard etch mask is patterned using a photoresist (PR) mask (HPR504 positive resist, OCG Microelectronic Materials n.v) with a thickness of 1.7 μm. The resist mask is spin coated on an automated spin coater (EVG 150, Austria), exposed with an energy of 160 mJ (ASML PAS5500, The Netherlands) and developed in a TMAOH based developer. The Al hard etch mask is wet etched in a commercially available wet etchant PES 77-19-04 (heated etch at 30°C) consisting of phosphoric acid H_3PO_4, nitric acid HNO_3 and acetic acid CH_3COOH with an etch rate of 95 nm/min. Subsequently, the resist mask is removed in acetone (CT60 spin coater, Gyrset). This hard etch mask is used to etch the PI in an O_2 plasma (6 min RIE in STS ICP tool). After the PI etch, "fur-like" residues were observed under the scanning electron microscope (SEM) around the free standing as well as not-free standing structures (Fig. 6.2-a and 6.2-b). This sample will be denoted as the reference sample (R) in all the preceding experiments.

For the investigation into the origin of these residues four different experiments are prepared. Each experiment is tested for a different hypothesis. The sample substrates in all the experiments were 6- inch Si wafers coated with 1 μm of plasma enhanced chemical vapor deposited (PECVD) SiO_2 (Novellus PECVD concept one). In all the experiments, the samples have been spin coated with 5.2 μm PI and the PI is etched with similar conditions as the reference sample. The process variations for different experiments along with the hypothesis and their consecutive results are listed in table 6.1. The choice for these process variations and their stated hypothesis is elaborated further in the discussion section. Each experiment is repeated three times. The results were the same for each.

In the first experiment, the formation of residues due to metal redeposition is

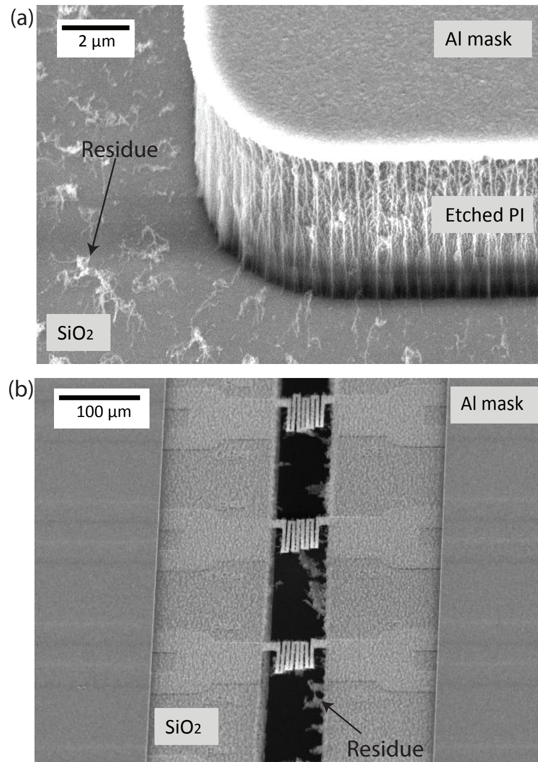

Figure 6.2: (a) Residue covered SiO_2 surface after reactive ion etch of PI with Al metal as the mask. (b) Free standing metal interconnect structures on the same wafer covered with "fur-like" residues after the PI etch.

tested. The Al hard etch mask in the sample A is processed without a PR mask and blanket wet etched in PES (heated at 30 °C). This sample is compared with the reference sample (R) after dry etching of PI. Presence of residues in sample A after the PI etch contradicts with the first hypothesis. Since the residues are not formed due to metal redeposition, the role of sputter etch in PI sample preparation is next investigated. Therefore, in the second experiment two samples with and without surface treatment are compared with each other. The first sample is processed similar to the reference wafer and the second sample (B) is prepared without the PI surface preparation. No residues are observed in the sample B after the dry etching of PI contrary to the reference sample. The role of Ar^+ sputter etch is hence confirmed for the presence of these residues, where omitting this etch could be a simple and straightforward solution. However, as reported in literature [10][15], surface treatment of PI is necessary to obtain good adhesion with metal layers. The accelerated Ar^+ ions create roughness by sputter etching the top few nms of the PI layer. This roughened PI layer is coated with the Al metal mask layer and some metal particles possibly remain embedded even after the wet etching. To test this hypothesis of "metal inclusions", a third

experiment is conducted with two samples. The first sample is prepared similar to the reference sample (R) and in the second sample (C) the hard etch Al mask is dry etched (Cl_2 plasma, SPTS CPX clustertool) with an overetch of 15 s to remove any residues from the top surface of the PI. Residues are not observed in the sample C after PI etch. To further test the role of metal deposition method in the formation of the residues, a fourth experiment is conducted. Both the samples in this experiment are processed similarly without PI surface preparation, except the method of metal deposition. The metal mask in the first sample (D) is sputter deposited while the mask is deposited using evaporation on the second sample (E). No residues are observed post etching on both the samples D and E.

The samples are investigated by means of Scanning Electron Microscopy in combination with X-ray Microanalysis (SEM/EDX). Electron micrographs were recorded with a FEI Nova600 NanoSEM microscope (voltage: 500-30 keV, resolution: 1.2 nm at 30 keV) using secondary (SE) and/or backscattered electrons (BSE). Additionally EDX spectra and element-mappings were recorded using the Oxford Xmax 80 EDX system. Polyimide layers with after a 5 nm sputter treatment was analyzed with atomic force microscopy (AFM) to determine the surface roughness. The measurements were performed with a Bruker Dimension FastScan, using a Si probe in the tapping mode in air. Data processing was performed with MountainsMap 6.0 from Digital surf. The sample was scanned on two locations, scan range 4 x 4 μm^2. Before scanning the surface was cleaned using a nitrogen gun. Raman spectra of the residues were recorded using a Renishaw InVia Raman spectrometer, with 514 nm excitation (Coherent Innova 70C laser). Laser intensities varying from 100 mW up to 500 mW were used, in combination with a 100x magnification with a numerical apperture of 0.85. Plasma etching of PI and Al was conducted in an inductively coupled plasma-reactive ion etching (ICP –RIE chamber with He backside cooling) machine (SPTS CPX clustertool).

6.3. RESULTS AND DISCUSSIONS

To begin the investigation, the composition of the residues in the reference sample was determined (Fig. 6.3-a). This was done using an energy dispersive x-ray analysis (EDX), which is an elemental analysis technique that uses x-ray energies given off by the atomic structure of the emitting elements to determine the composition of the present elements [16]. The analysis showed that next to Si, O_2, F, C etc. from the substrate underneath, an additional peak of Al was present (Fig. 6.3-b). The result of the analysis leads to an immediate and first theory of metal redeposition from the Al hard etch mask during the plasma etching of PI. According to this theory, the Al metal mask gets bombarded by ions during plasma etching and redeposits on the surface of the PI resulting in micromasking which can lead to grass formation. Previously, in literature [17][18], the presence of these “grass-like” residues could only be observed in the proximity of Al structures. However, in the reference experiment the residues were observed to be homogeneously distributed over the etched areas, and even on areas that were distant from the metal mask (Fig. 6.2). To challenge this theory, sample A in experiment 1 was processed the same way as the reference sample except that the metal hard etch mask was completely removed by wet etching and the PI was blanket etched

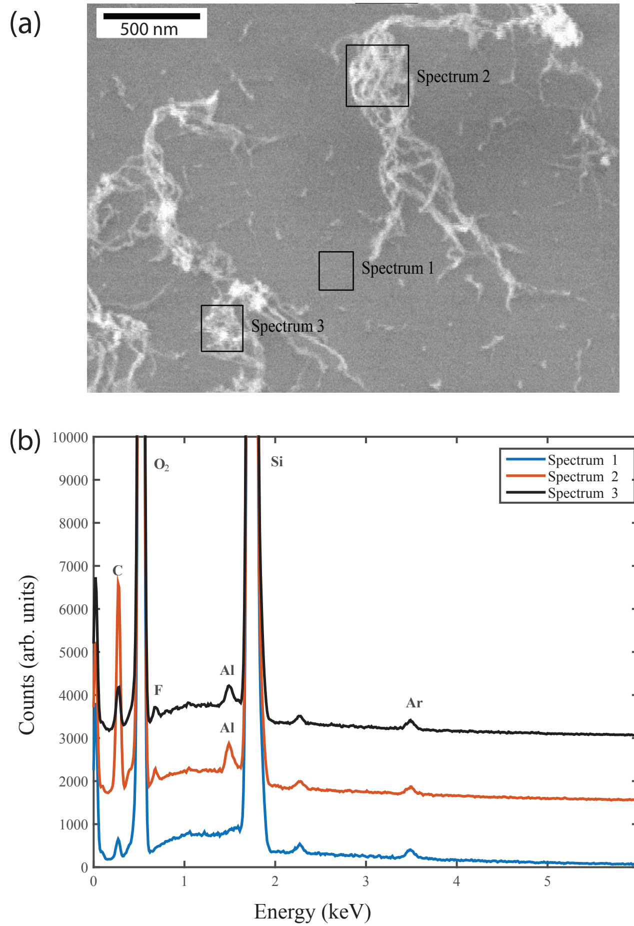

Figure 6.3: (a) A close up SEM image of the “fur-like” residues obtained after the PI etch in sample R with back overlaid rectangles representing the region of interest used for EDX scan of the corresponding spectrum, and (b) EDX analysis and comparison of residue free and covered areas depicting the presence of Al peaks for spectrum with residues. The spectra have been offset for clarity.

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(Table 6.1). This excludes the possibility of the mask being redeposited on PI. However, SEM inspection again showed the presence residues over the SiO_2 surface on both the samples. Upon EDX analysis, the presence of Al was again confirmed in the residues. This dismisses the redeposition and micromasking theory. Another possible explanation for the residues is that the metal hard etch mask is not completely etched during the wet etching. Increasing the temperature or duration of the wet etch (200% over-etch) of metal mask did not change the results. To remove these residues the substrate was immersed in a PES etch shortly after the PI was etched by RIE. Upon inspection it was observed that the residues had been removed. This is one of the methods to eradicate the residues. However, this approach is not suitable for test device like structures as mentioned previously with free standing exposed metallic structures. Any kind of wet etchant leads to loss of the free standing structures due to the viscous forces acting upon them. This method is therefore only suitable for samples with no free standing structures and no exposed and active metal areas.

The etched mask area of the PI after the removal of the residues with PES etchant was studied under the SEM and a “sparkly” formation was observed on the PI (Fig. 6.4-a). Materials like polyimide are electrically non-conducting and normally show charging in a SEM. To prevent charging usually, a conducting surface coat must be applied to provide a path for the incident electrons to flow to ground. Unlike a normal polyimide, the polyimide at the locations of the metal mask did not show any charging, suggesting signs of certain metal inclusions on the top surface. The sparkles and the substrate underneath (PI) it was investigated with an EDX analysis, and traces of Al were again measured in the spectra (Fig. 6.4-b).

A second hypothesis based on these results was drawn; the formation of micro/nano pockets on the surface of the PI where the Al gets deposited while sputtering. These pockets/roughness is created during the Ar^+ ion sputter etch to improve adhesion of the metal to PI [13].

Upon wet etching of the patterned metal, the metal in these pockets is not etched due to the low surface energy of PI, like most of the polymers [19][20][21]. Increasing the duration of the wet etch in such a situation had no effect. This polyimide when etched in an oxygen plasma, gets etched except the pockets of Al which may act as micro-masks and eventually form “fur-like” residues in the end. The sputter etch is suspected to play a role in the formation of such pockets. To determine the role of sputter etch, sample B in experiment 2 is coated with 200 nm Al deposited by sputtering without sputter etch. This sample is blanket etched in wet etchant, followed by a blanket etch of the PI. Inspection of the samples in the SEM showed no residues. This confirms the second hypothesis, that the Ar^+ ion sputter etch does play a role in the residue formation.

In order to determine the cause of the formation of these residues, two more explanations were investigated. In the first theory, it is assumed that the surface of PI forms activated carbon after a short sputter etch in an Ar^+ plasma. This active carbon can react with the sputtered Al of the mask and form aluminum carbide (Al_4C_3). It is hypothesized that this compound does not get etched in the O_2 plasma etching of the PI and forms Al_4C_3 containing residues.

To detect the presence of Al_4C_3, Raman spectra of the residues in the reference

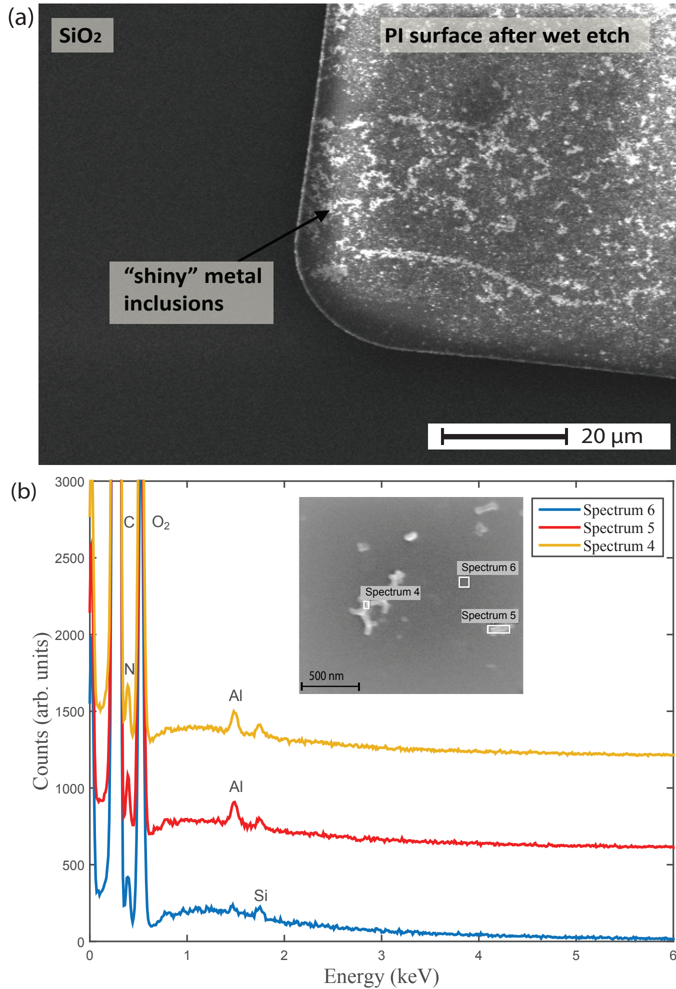

Figure 6.4: (a) Polyimide surface under the SEM after removal of the metal mask depicting sparkly inclusions in sample B. (b) EDX analysis of the shiny (spectrum 4 and 5) and non shiny (spectrum 6) areas on the PI represented in the inset image, depicting the presence of Al in small amounts. It is to be noted that the signal for EDX of these inclusions is very weak as the Al is possibly embedded within the PI. The spectra have been offset for clarity.

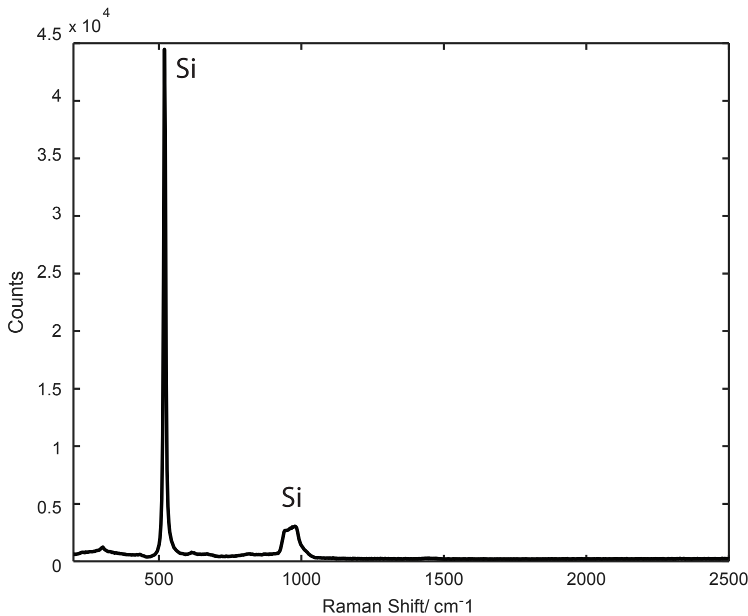

Figure 6.5: Raman bands for Al_4C_3 are reported for 532 nm excitation at 252.85 cm^{-1}, 288.65 cm^{-1}, 340.86 cm^{-1}, 493.00 cm^{-1}, 718.22 cm^{-1} and 864.40 cm^{-1} wavelengths [22][23]. However, Raman spectra of the residues show only the Si peaks from the substrate for sample A.

sample were studied. According to literature, Raman bands for Al_4C_3 are reported for 532 nm excitation at 252.85 cm^{-1}, 288.65 cm^{-1}, 340.86 cm^{-1}, 493.00 cm^{-1}, 718.22 cm^{-1} and 864.40 cm^{-1} wavelengths [22][23]. Using similar excitation, and varying the laser intensities from 100 mW up to 500 mW (0.85 N/A), spectra for the residues and the substrate (SiO_2) underneath were obtained (Fig.6.5). No bands related to Al_4C_3 or carbon were detected, only bands related to silicon from the substrate are visible in the spectra, refuting this theory.

In another theory, the surface roughness of the PI created after Ar^+ ion sputtering is speculated to encompass Al inclusions within the roughened PI grooves. The roughness is measured with an atomic force microscope (AFM) where the root mean square (RMS) deviation of the surface is measured to be 0.5 nm and 4.7 nm before and after 100 s sputter etch, respectively (Fig. 6.6-a). The reference plane for the calculation of this parameter is the mean plane of the measured surface. The metal inclusions in the grooves do not get etched in the Al etch as the wettability of PI is low, making wetting of the grooves difficult during the PES etch (Fig. 6.6-b). In order to support this theory, the metal mask is dry etched in a Cl_2 chemistry plasma (5 mTorr) instead of the wet etchant. An over etch of 15 s is used to ensure the removal of the entrapped Al in the roughened PI. This does not effect the underlying PI layer. In the next step the PI is etched in exactly the same way as in the previous experiments and the surface is inspected in the SEM. SEM analysis showed no presence of residues on the surface,

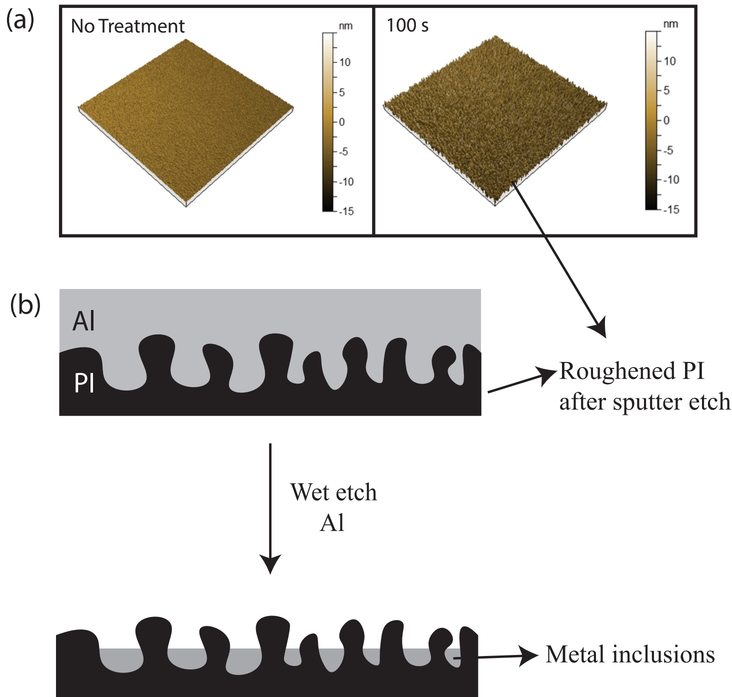

Figure 6.6: (a)Atomic force measurement (AFM) images of polyimide surface before and after 100 s Ar^{+} sputtering with the root mean square (RMS) deviation of the surface being 0.5 nm and 4.7 nm, respectively. (b)Schematic of a rough PI surface with aluminum layer on top and the metal inclusions inside the roughened pockets of PI that remain after a wet etch due to partial wettability with the PES wet etchant.

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confirming this theory. This final result was tested on the sample C reported in experiment 3 (Table 6.1), where all the fabrication steps remained the same as the reference sample except the patterning of Al mask on top of PI. After the PI etch, the results show "fur free" free standing interconnect structures as shown in Fig. 6.7.

The role of metal mask deposition method was also studied in experiment 4. In this experiment sample E was prepared by depositing metal mask via evaporation instead of sputtering (sample D). After the PI etch, no residues were observed in the SEM. However, the sample surface has no sputter etch prior to the mask deposition as this cannot be incorporated in the metal evaporation tool. Although this is a solution, the metal- PI adhesion issue cannot be addressed using this deposition technique. Hence, this was not considered as a desirable solution.

6.4. CONCLUSIONS

In this paper, residues formed after dry etching of polyimide using Al hard etch mask have been investigated. Generally, according to literature [10], a short sputter etch is

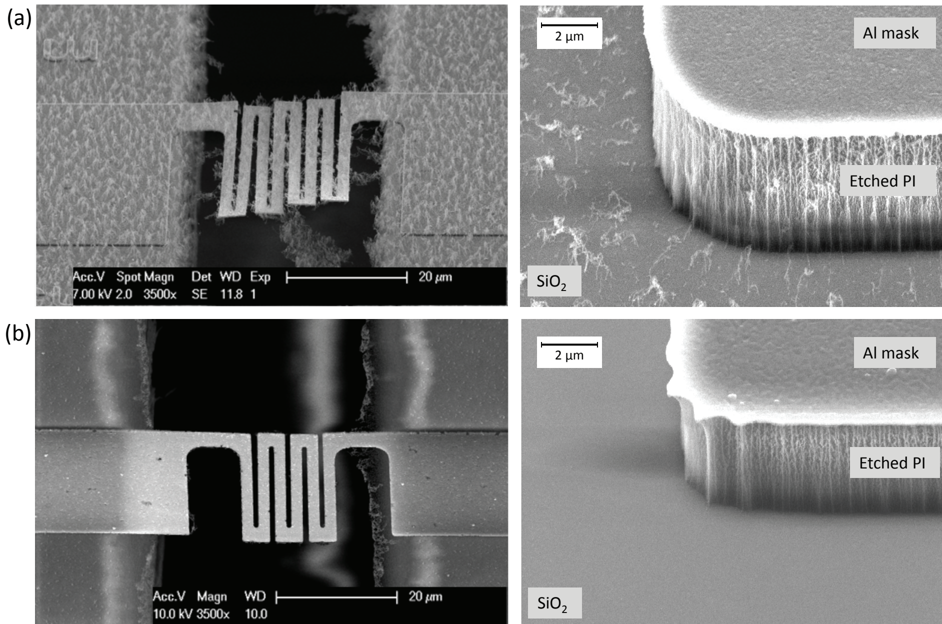

Figure 6.7: SEM image comparison of (a) sample R with residue covered free standing as well as not free standing structures after PI etch, with (b) free standing as well as not free standing structures of sample C after PI etch using dry etching of PI.

used on the surface of PI before depositing Al as a hard etch mask for a better adhesion. We conlcude that the metal mask deposited after the sputter etch forms metal "inclusions" on the top roughened PI layer. These inclusions do not get etched in the wet etch of the metal mask due to the low surface energy of PI [15]. This leads to the formation of metal containing residues after the PI etch. The residues can be removed using wet etchant like PES, but this approach becomes unfeasible if there are exposed active metal structures. A one-step dry etch of the metal mask solution has been investigated in this paper using a slight overetch. This slight overetch is enough to erode the top layer of the PI and remove the metal inclusions, thus enabling a "fur-free" PI etch.

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7

Conclusions and Recommendations

7.1. CONCLUSIONS

Stretchable electronics is a fascinating and multidisciplinary area of research based on advances in material science, unique interconnect designs and an understanding of the mechanics of stretching. Research in stretchable electronics previously, has resulted in a variety of materials and/or designs that can be stretched to a certain limit. However, challenges like high density circuit integration, scalability and manufacturability of these techniques still need to be addressed. In this Thesis, new technologies for fabrication of stretchable interconnects that address these challenges have been presented. This has been demonstrated in two parts by following the approach of so called free standing interconnects, whereby the interconnects can fully bend out of plane during stretching. In the first part a technology platform that is suitable for large stretchable patches with a high fill factor and high density interconnects. As a proof of principle, a relaxed sparse design was implemented. In the second part of this Thesis, a device for studying the mechanical and electrical behavior of free-standing micro-fabricated metal structures, subjected to a very large deformation is presented. The main contribution to the field are stated below.

Contribution I

For a stretchable device with meandering interconnects between the rigid islands, ideally the interconnects should be freestanding, so that they can behave as true spring like structures and have the possibility to bend out of plane resulting in maximum stretchability. In Chapter 2, the process modules for the fabrication of large area free standing structures is presented, whereby, process optimization for different layers is implemented. The work in this chapter resulted in a better understanding of the most important design parameters for the fabrication of large area stretchable patches. The integration of different layers with each other is refined, and a platform for the final metal layer integration is presented.

Contribution II

An important observation from Chapter 2 is the unreliable adhesion between polyimide (PI) and silicone polydimethylsiloxane (PDMS). In Chapter 3, various methods of improving the PI-PDMS adhesion are discussed. The role of surface modificaton using Ar^+ sputter etch on polyimide in enhancing the adhesion is studied. An increase in adhesion after the surface modification of up to 15 times is observed, due to the mechanical interlocking of PDMS to the roughened PI surface, and increase in hydrophilicity of the substrate after sputtering. However, it was found that the effectiveness of this method also strongly depends on other factors such as type of polyimide (non-photoimageable versus photoimageable) and ageing of the polyimide precursor. Therefore, an alternative to this method was studied whereby the use of a rubber—Polybutadiene (non cross linked) as an intermediate adhesive layer also resulted in an improved PI-PDMS adhesion. The adhesive bond initiated by the butyl rubber

(BR), apart from being extremely strong due to the interplay between chemical and diffusive bonding, is also chemically resistant and mechanically stable.

Contribution III

In Chapter 4, the integration of optimized process steps for free standing interconnects were implemented in the complete fabrication of the test device patch. It was found in Chapter 2, that such large structures tend to droop under their weight after they are rendered free standing. To overcome this issue, a concept of PDMS pillars was introduced and implemented in large free standing structures, along with a novel method of mechanically interlocking interconnects to such pillars using micro channel cavities. Preliminary stretching experiments were performed on these interconnects, which resulted in an 80% reversible elastic stretchability. However, a material disadvantage in the form of PDMS cracking beyond 80% stretch was observed during characterization, which provided a good insight into the limitations of this technology and also the need for reliable test devices for these interconnects.

Contribution IV

Future advanced stretchable medical electronic devices e.g. large area body conformable ultrasound imaging devices, will require high-density stretchable interconnects with micron-scale footprints. In chapter 5, the fabrications process for micron sized free standing interconnects is discussed. An important aspect of reliable testing of such fragile structures in the form of a unique test device is presented. This testing approach allows for the application of very large displacements to test structures with the same size, shape and microstructure as in the final application, while providing a solution to prevent undesired mechanical loading of these fragile structures before the test. Standard micromachining which allows for high precision and reproducibility of the fabrication process is used. The concept was successfully demonstrated by repeatedly stretching micron-size interconnects to 2000% reversibly, while the resistance is measured simultaneously. The performance and reproducibility of these free-standing structures with an elastic stretch beyond 2000% and ultimate (plastic) stretch beyond 3000%, with <0.3% resistance change, and >10 million cycles at 1000% stretch with <1% resistance change has been reported.

Contribution V

"Fur-like" residue formation was observed after dry etching of polyimide using an Al hard etch mask in the fabrication of micron-sized free-standing interconnects. The presence of these residues is undesirable as it leads to process instability and may interfere with the subsequent microfabrication steps. In Chapter 6, an investigation into the origin of these residues is performed and various approaches to prevent them have been tested. A "fur-free" procedure for the etching of PI using a one-step reactive ion etch of the metal hard-etch mask is presented. Finally, devices are demonstrated that were fabricated with the optimized process that were free of residues and were still

fully compatibility with advanced MEMS- processing flows.

7.2. RECOMMENDATIONS

The results and technological advances presented in this Thesis bring us a step closer to the development of reliable technologies for fabrication of the free-standing interconnects to achieve improved stretchability in devices. However, further research and development is needed in order to obtain a fully mature technology platform. Important topics for future research and potential applications are listed in this Section.

- In this Thesis, in Chapter 2 and 3, the importance of a good adhesion between PI and PDMS has been discussed. The reliability of this or any device using these two polymers greatly depends on their adhesion. We proposed mechanisms to improve this adhesion by surface modification and by using an intermediate layer. However, there was a lack of reliable characterization techniques to test the adhesion between these materials. Many methods presented in literature are not quantitative enough to measure this parameter. Therefore, the development of characterization techniques that can more easily and reliably quantify the adhesion strength between polyimide and silicone or between two thin film polymer layers in general is suggested.
- The micron-sized interconnects that were presented in Chapter 5, can be fabricated in multiple layers above each other for various applications that require high density interconnects. In this scenario, it is important to electrically isolated these interconnects. A thin layer of parylene, conformally deposited on the free standing interconnects is suggested as a solution. This requires a verification of the quality (pinholes, crystallinity etc.) of parylene when deposited as a thin layer (<500 nm) with appropriate characterization techniques. Furthermore, an investigation of the effect of such a layer on the mechanical behavior and eventually the stretchability of the interconnects should be conducted.
- Although EPlaR has been reported as a very effective, easy and sustainable release method, the removal of sacrificial polyimide layer after the release from the substrate in Chapter 4 needs further improvement. The removal of this sacrificial polyimide layer by dry etching has shown to negatively effect the PDMS. Due to exposure to the oxygen plasma, the surface embrittlement of PDMS is likely to cause an early material failure in the device upon stretching. An alternative solution for this could be a metal layer (Al/Mo) deposited on top of the PDMS as a final step before releasing of the patch. This layer will subsequently protect the underlying PDMS layer during the dry etching of the sacrficial PI. An easy removal of this layer can be integrated in the next step of metal release layer removal together in the wet PES etching, which thus not impact the consequent processing steps.

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APPENDIX

8.1. LARGE AREA INTERCONNECTS BODY PATCH

Step	Step name	code	Parameters / recipe name	Comments
Wafer preparation				
1	Engrave numbers	NIL	Engraving tool/ Diamond scriber	Easier with diamond scriber; make less deep marks
2	Cleaning	C2-06	Standard cleaning Piranha + HF Dip + Scrubbing	
3	Tape Backside	C2-04	Use a dummy laminated wafer underneath to reduce contamination	Use primer while spin coating as it aids in the proper deposition of oxide
Release stack				
Polyimide coating				
4	VM651 primer	C4-02	0.5% in DI water ; 1ml in 200ml water	make it fresh
5	Spin primer	F136	open 500rpm 10s; closed 3000rpm 45s	do a dynamic dispense while 500rpm spin
6	Soft bake	hot plate	120 deg 1:30 min	
7	Spinning PI	F136	PI2611 + NMP (50% vol); open 500 rpm 10s; closed 2000 rpm 30 s acc 200 rpm/sec	~0.5 microns after cure
8	Soft baking PI	O59	vacccum oven - 10min+ 15 mins oven bake at 125°C	Immediately after the soft bake take off the foil on the back
9	PI curing	O24	prog 10: rise to 275°C in 1hr56m (2.2°C/min), 3hr at 275°C, drop to RT in 3 hr	Check prog 10 one time for parameters
Mo Deposition				
10	Dehydration bake	O58	temp : 125°C, time - 30 mins.	
11	Sputtering Mo	S31	200 nm Mo (STD parameters)	
Contact Hole definition				
PI definition				
PI deposition layer 1				
12	VM651 primer	C4-02	0.5% in DI water ; 1ml in 200ml water	make it fresh
13	Spin primer	F136	open 500rpm 10s; closed 3000rpm 45s	do a dynamic dispense while 500rpm spin
14	Soft bake	hot plate	120 deg 2 min	
15	Spinning PI	F136	PI2610; open 500rpm 8s; closed 2000rpm 45s,3000rpm 2s	~2.6 microns after cure
16	Soft baking PI	O59	soft bake for 5 mins + 30 mins oven bake at 125°C	
17	PI curing	O24	prog 10: rise to 275°C in 1hr56m (2.2°C/min), 3hr at 275°C, drop to RT in 3 hr	

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18	Resist spinning	F78/F83	AZ4533 3.9 microns soft bake at 110°C	
19	Exposure	B30	Recipe name : Stretch test; Energy : 400 mJ Contact mode; Open window soft mask	
20	Develop	F83	Develop_AZ4533 (normal)	
21	Dry etching	E32	ICP Par 02 [do a Tdesc of 4 minutes before etch], endpoint + 20 seconds	keep a check on etch with respect to resist thickness
22	Resist removal	N38	5 min first bath+ 5 min second bath+ 5 min IPA+ 10 min water	
Ti Contact layer Deposition				
23	Dehydration bake	O58	125°C for 30 minutes	
24	Sputtering	S31	Deposit 100 nm Ti + 5nm sputter etch	Always ask for prechange of targets as it is not a commonly used one
25	Resist spinning	F78/F83	AZ4533 3.9 microns soft bake at 110°C	
26	Exposure	B30	Recipe name : Stretch test; Energy : 400 mJ Contact mode; Closed window soft mask	
27	Develop	F83	Develop_AZ4533 (normal)	
28	Dry etching	E28	Recipe name : ICP Ti02; run at end point + 20 seconds OE; Total time is 50 seconds	Ask for a Tdesc of 4 minute before the etch
29	Resist removal	N38	5 min first bath+ 5 min second bath+ 5 min IPA+ 10 min water	
Al Cu (1%) Deposition				
30	Dehydration bake	O58	O58	
31	Sputtering	S31	1 micron + 5nm sputter etch	
32	Resist spinning	F78	SPR 1.2 microns; soft bake at 110°C	
33	Exposure	B30	80 mJ/cm2, Recipe: Al-PI-Handles	
34	Develop	F78	Develop_PEB_SPR	
35	Wet etching	LFB	PES etch 30°C, etch rate : 100 nm/min; visual endpoint + 10 seconds (approx. 8 minutes)	
Verteq Rinse Dry				
PI deposition layer 2				
36	Spinning PI	F136	PI2610; open 500rpm 8s; closed 2000rpm 45s,3000rpm 2s	

37	Soft baking PI	O59	soft bake for 5 mins + 30 mins oven bake at 125°C	
38	PI curing	O24	prog 10: rise to 275°C in 1hr56m (2.2°C/min), 3hr at 275°C, drop to RT in 3 hr	
Ti hard etch mask deposition				
39	Deposition of TI	S31	Deposit 200 nm Ti + 5nm sputter etch	
40	Resist spinning	F86	AZ4533 5.9 microns SB 110C	
41	Exposure	B30	PI_BODYPATCH exposure dosage : 150 mj/cm2 vaccuum contact	
42	Develop	F86	develop AZ thick recipe	
Visual inspection of features				
43	Hard bake resist	ULTRA CLEAN OVEN	125 °C 30 minutes	
PI Etching				
44	Dry etching	E32	ICP PAR02, ask for end point + 20 secs (approx. 6 minutes sometimes less)	1 mu per minute etch rate; two end points seen
Dektak measurement of the PI structures				
Butyl Rubber preparation				
Cured BR				
45	Spinning BR	F136	Butyl rubber (83% n-heptane); closed 400 rpm at 500 rpm/s 10 s; closed 2000 rpm at 500 rpm/s 25 s	7 mu thickness
46	Removing solvent	LFB	Keep 8 hours with a slightly open glass cover lid	To prevent bubbles
47	UV Curing	LFB	150 watt UV lamp exposure for 1 hour	3 mu thickness
Uncured BR				
48	Spinning BR	F136	Butyl rubber (83% n-heptane); closed 400 rpm at 500 rpm/s 10 s; closed 2000 rpm at 500 rpm/s 25 s	7 mu thickness
49	Removing solvent	LFB	Keep 8 hours with a slightly open glass cover lid	To prevent bubbles
50	RT cure	LFB	Longer RT cure for solvent removal; not cross linked	4 mu thickness
Resist pillar definition				
51	Manual coat resist	LFB	AZ 40XT; open 500rpm 8s; closed 2000rpm 45s,3000rpm 2s	
52	Soft bake	O59	4 min @100 C + end the process with 30 minute bake @ 100 C	

53	Expose	B30	PI_AZ40XT; exposure dosage : 450 mj/cm2 vaccuum contact	
54	Develop	Manual bath	Develop in OPD5262 for 8 mins	
Removal of the Al-Cu sacrificial metal from stitches				
55	PES Etch	LFB	PES etch 30 degrees, etch rate: 100nm/min; check visual endpoint + 10 secs extra	
Microscopic as well as SEM inspection for the openings in the PI layer				
56	Cast PDMS	LFB	Cast 16 g of 10:1 PDMS and RT cure for 24 hours	
EPlaR the Wafer				
Backside Processing				
57	Etch sacrificial PI from back	Barrel	125 deg C for 1 hour	Check for colour change
58	PES Etch	LFB	Etch sacrificial Mo (200 nm) in 3 mins in manual bath	
59	Acetone	LFB	Sacrificial resist removal ; 5 mins	

8.2. MICRON-SIZED STRETCHABLE INTERCONNECTS

Step	Step name	Code	Parameters / recipe name	Comments
Wafer Preparation				
1	Cintillio Cleaning + Organic	R72	FZplusHCL + HZ-plus36min	Check the wafers after cleaning to check for any debris
2	Spin rinser	F40	STD program	
3	Spin coat resist	F06	150 mm_TMSDEA_HPR504_4000_rpm_EBR	
4	Allignment marks Exposure	B22	Diversen\SMEA_V2; Layer: 3D_MARKS; Dosis: 150 mJ/mm2 ; Focus: 0	
5	Developing	F06	HPR/ 150mm_develop	
6	Etching	E28	Recipe : APS-MRK01 , depth :140 nm ; Mask : HPR504@4000rpm	
7	Numbering wafer	P17	recipe: double thickness	
8	Cintillio resist	R72	HZplus36min	
9	Bow Measurement	Flexus	First film	
10	Cintillio clean	R72	FZplusHCL	
Definition of backside DRIE1 and DRIE2				
11	Deposit PECVD oxid FS	C03	deposition 1000nm zero stress PECVD plasma oxide	"zero" stress oxide at 400 degrees. Under special section
12	Deposit PECVD oxide BS	C03	deposition 5000nm zero stress PECVD plasma oxide	"zero" stress oxide at 400 degrees. Under special section
13	Resist spinning BS	F06/50	HMDS_HPR504_2000nm_BSR (2µm)	
14	Exposure	B22	Expose (Diversen/TUtens/layer_drie1_a), 160 mJ, Focus - 0 (backside)	TU/TENS-1 reticle
15	Develop	F06/50	PLSI 1:1 laktrack	
17	Dry etch oxide	E28A	DRIE1 definition in back oxide APS SiO01 (2500nm, 9 min 15sec) //etch measurements	
18	Strip resist in Barrel/ Fusion	E01	O2 plasma, 1000W, 30min / PR STR 250C 10min.rcp	
20	Resist spinning	F06/50	TMSDEA + AZ4533 + EBR, 3500rpm, 3.9 µm (backside)	
21	Expose	B22	Expose (Diversen/TUtens/layer_drie2), 160mJ , Focus- 0	
22	Develop	F06/50	PLSI 1:1 laktrack	
23	Dry etch oxide	E28A	DRIE 2 definition in oxide APS SiO01 till EPD	
24	Strip resist in Barrel	E01	O2 plasma, 1000W, 130C 90 minutes	
26	Cintillio Cleaning	R72	recipe: FZplusHCL	check after 60 minutes if all the resist is gone or not

Depositing Aluminium structures: Processing on Front side !!!				
27	Sputter Al	S31	300 nm , STD(standard parameters) - cold	
28	Spin coat resist (EV-track)	F06/50	150mm\Shipley SPR660 1.2 µm	
29	Exposure	B22	Expose (Diversen/TUtens/layer_inf_a), 170mJ , Focus - 0	Reticle: TU/TENS-2
30	Developing (EV-track)	F06/50	Develop PEB	
31	Dry etching	E28	ICP Al 01 (standard recipe): 45 seconds + 5min N2H2 passivation	the passivation gives a relief from the immediate water quench step and removes the water step
Transfer in water bath				
32	Strip Resist	F40	O2 plasma, 1000 W, 130C 30 minutes	
Optical inspection				
Depositing PI				
33	Descum	F40	90 deg 2 min Fusion / 600W 110deg 2 min	
34	VM651 primer	LFB	0.5% in DI water ; 1ml in 200ml water	
35	Spin primer	F136	open 500rpm 10s; closed 3000rpm 45s	
36	Soft bake	hot plate	120 deg 2 min	
37	Spinning PI	F136	PI2611; open 500rpm 10s; closed 3000rpm 45s	
38	Vacuum oven	C1-07	15 min at RT	
39	Soft baking PI	F136	15 in in ultraclean oven 125 deg	
40	PI curing	O24	prog 10: rise to 275°C in 1hr56m (2.2°C/min), 3hr at 275°C, drop to RT in 3 hr;	
Depositing and patterning Al				
41	Dehydration bake	C1-09	30 min 125 deg oven	
42	Deposit Al	S31	200 nm Al low power (1 kW) + sputter etch 5 nm	
43	Resist spinning	F06/50	HPR504 2500rpm 1.7 µm	
44	Expose	B22	Expose (Diversen/TUtens/layer_PI), Energy 160 mJ/cm2 , Focus 0	
45	Develop	F06/50	STD program	
46	Dry etch	E32	ICP Al01 etch; EDP (18sec) + 15 sec (80-90% OE); start close coupled	
47	Verteq rinse dry	C2-08		close coupled
48	Microstrip	C1-11	Bath 1 (5min) : Bath 2 (5 min): IPA (5 min) : water (10 mins)	check if the baths are good to use or make manual baths
49	Verteq rinse dry	C2-08		close coupled

Before starting with the DRIE etch cover the edges of the wafer with HPR resist (paintbrush) and the flat of the wafer (BS) with Kapton to prevent chipping				
Backside two step etching				
50	First head start etch	E28C	PEGC01H 250 µm advance (10µm/min) 25 minutes	250 µm depth; check with microscope;
Inspect under the microscope for thickness variations; especially in the hinges of the frame (critical area) also hoogtmeter				
51	Second mask oxide etch	E28A	APS SiO01 (end point visible) 9 minutes	etch rate is 0.25µm/minute : after 20 mins DRIE etch ~1.7µm oxide left
Inspect under the microscope for thickness variations; especially in the hinges of the frame (critical area)				
52	Final DRIE	E28C	PEGC01H; ~20 minutes for 200µm ; visual end point	check under the thickness measuring microscope; maybe 30 minutes at once is too much ?
53	Isotropic etching step	E28C	PEG I01 isotropic etch : 1min + 1min (complete removal of curtains)	to remove some spikes and curtains formed while anisotropic etch
54	Oxide etch	E28	Recipe: ICP_SiO_01 ; when BuO-1.7µm ~22mins	
55	Laminate the backside	C1-11	use laminator next to the sawing lab; use UV release foil	ask for special less adhesion foil fom the foil engineer
56	PI dry etching	E28	ICP PAR02, 6 minutes (4min end point + 2min overetch)	
57	Inspection	I16	check if PI etching is completed	

SUMMARY

Advancements in stretchable electronic systems have changed the way modern electronics interact with their target systems, by their conformability to more complex shapes as compared to conventional rigid or flexible electronics. By utilizing this, limitless applications in the field of healthcare can be realized, such as wearable and implantable electronics. Medical devices that can be stretched/conformed to a certain limit, will reduce the effort by physicians and improve the user experience by providing enhanced dynamic shaping and matching mechanical properties to that of the human body. In literature, many methods for the realization of stretchable electronic systems are presented. In this Thesis, the design and micro fabrication of free-standing stretchable interconnect technologies for both large and small area devices is presented. Free-standing interconnects have the freedom to bend out of plane during stretching, thus enabling an increase in stretchability. This Thesis presents a reliable microfabrication technology for stretchable electronic circuits with high density interconnects, that can be considerably stretched even in densely packed/high fill-factor circuits. To fabricate and study the free standing interconnects, a demonstrator patch with a sparse horse-shoe shaped interconnect design is presented in the first part of the Thesis. To render such large structures free standing, several technology modules needed to be developed. After the first proof of principle showing free standing polyimide meander structures, the poor adhesion of polyimide (PI) and polydimethylsiloxane (PDMS) led to failure of the devices. Therefore, two methods involving surface modification of polyimide, and using an intermediate adhesion layer for improving the adhesion between PI and PDMS, were tested and assessed. Finally, butyl rubber as an intermediate layer was selected and implemented in the final fabrication process. The adhesive bond initiated by the butyl rubber (BR), apart from being extremely strong, is also chemically resistant and mechanically stable. For the final fabrication flow of these structures with metal interconnects, technological modules like PDMS pillars to prevent drooping of the large horse-shoe shaped interconnects and PI-PDMS "stitches" to ensure a reliable adhesion of the pillars to the interconnects were developed and implemented. A demonstrator patch with reversible stretchability of 80% is presented. However, it was observed that the testing of such large free-standing structures on a patch is not straightforward. In the second part of the thesis, testing was made an integral part in the design of the device. A device with a high fill factor i.e. densely packed rigid islands, allows only for a very small footprint of the interconnects. Therefore, a sub-micron interconnect design that can be realized with standard fine-pitch photolithography based IC techniques was developed, and an interconnect pattern based on a design presented by S. Shafqat et. al was implemented. In the second part of this Thesis, a test device for the micro tensile testing of these micron sized free standing structures is designed and fabricated for their easy, damage- free

handling and mounting in a test setup. The device is fabricated as a single chip that can be separated into two movable parts after fixing it on the micro tensile test stage. The test device successfully demonstrated the tensile testing of the micron sized free standing structures that show reversible stretchability up to 2000%, while simultaneously measuring the resistance. Moreover, the generic design of the device allows the implementation and testing of different size and shape free-standing structures. After the fabrication of the micron sized free standing structures, several "fur-like" residues were observed after the oxygen plasma etching of polyimide using aluminum as a hard etch mask. Therefore, different methods for the residue free etching of the polyimide were explored and a "fur-free" procedure for the etching of PI using a one-step reactive ion etch of the metal hard-etch mask is presented. In conclusion, the results and technological advances presented in this PhD Thesis have led to an increased understanding of the technologies for the reliable fabrication of free standing interconnect structures and have resulted in an improved stretchability in conformal electronic devices.

SAMENVATTING

De ontwikkeling van rekbare elektronica heeft de manier veranderd waarop elektronische systemen zich kunnen aanpassen aan hun omgeving. In vergelijking met rigide en flexibele schakelingen kunnen zij zich door hun rek- en plooibaarheid beter voegen naar complexe vormen. Door gebruik te maken van deze eigenschap kunnen vele toepassingen op het gebied van de gezondheidszorg, zoals draagbare en implanteerbare elektronica, worden gerealiseerd. Medisch applicaties die in zekere mate kunnen rekken en zich dynamisch naar het lichaam kunnen voegen, zijn door de arts makkelijker te gebruiken en verhogen het comfort voor de patiënt. In de literatuur worden diverse manieren voor de fabricage van dergelijke rekbare elektronische circuits voorgesteld. In dit proefschrift wordt het ontwerp en de micro-fabricage van een technologie met vrijstaande rekbare elektrische verbindingen gepresenteerd die geschikt is voor zowel grote als kleine circuits. Vrijstaande elektrische verbindingen hebben het voordeel dat ze zich tijdens het rekken in de derde dimensie kunnen plooien, hetgeen de rekbaarheid vergroot.

In dit proefschrift wordt een betrouwbare microfabricagetechnologie gepresenteerd voor de fabricage van rekbare elektronische circuits met elektrische verbindingen met een hoge dichtheid die zelfs voor ontwerpen met een hoge vulfactor nog een aanzienlijke rekbaarheid mogelijk maken. Om de vrijstaande elektrische verbindingen te kunnen bestuderen worden ze in het eerste gedeelte van dit proefschrift gedemonstreerd aan de hand van een “patch” met hoefijzervormige elektrische verbindingen. Om de fabricage van dit soort vrij grote vrijstaande structuren mogelijk te maken, moesten diverse technologiemodules worden ontwikkeld. Zo toonden de eerste experimenten aan dat een goede hechting tussen polyimide (PI) en polydimethylsiloxaan (PDMS) essentieel is voor een betrouwbaar device. Twee verschillende methodes om de hechting te verbeteren werden geïmplementeerd en geëvalueerd. De eerste methode berust op de oppervlaktemodificatie van het polyimide, de tweede op de introductie van een butyl rubber hechtingslaag. Deze laatste oplossing werd geselecteerd voor de fabricage van het uiteindelijke device omdat de hechting van het butyl rubber zeer goed is en omdat het chemisch inert en mechanisch stabiel is. In het uiteindelijke fabricageproces werden verder een aantal nieuwe technologiemodules geïmplementeerd zoals PDMS-pilaren of steunpunten die voorkomen dat de vrijstaande verbindingen gaan hangen en die voorzien zijn van “hechtingen” waarmee de elektrische verbindingen mechanisch aan de PDMS pilaren worden verankerd. De demonstratie patch vertoonde een rekbaarheid van 80%. Tijdens het onderzoek werd duidelijk dat het testen van dit soort rekbare structuren niet eenvoudig is.

In het tweede gedeelte van het proefschrift was testbaarheid daarom een integraal onderdeel van het ontwerp. In rekbare circuits met een hoge vulfactor, d.w.z. met dicht op elkaar gepakte rigide eilanden, blijft er maar weinig ruimte over voor de elektrische

verbindingen. Om deze toch te realiseren werd een submicron-verbindingstechnologie ontwikkeld met een design gebaseerd op een ontwerp door S. Shafqat. Een speciale teststructuur werd ontwikkeld en gefabriceerd waarmee structuren met micrometer afmetingen mechanisch kunnen worden gekarakteriseerd zonder dat ze beschadigd kunnen worden door handmatige manipulaties. Het test device wordt als één geheel gefabriceerd en nadat het in de meetopstelling is gemonteerd gesplitst in twee onafhankelijk bewegende delen. Met dit test device kon worden gedemonstreerd dat de nieuwe sub-micron verbindingstechnologie 2000% kan worden gerekt terwijl tegelijkertijd de elektrische weerstand werd gemeten. Behalve voor het testen van elektrische verbindingen kan deze generieke methode gebruikt worden voor de mechanische en elektrische evaluatie van andere zeer kleine fragiele structuren. Tijdens de fabricage van de vrijstaande structuren werden na het etsen van het polyimide met een aluminium hard-ets masker in een zuurstofplasma haarvormige residuen waargenomen. Diverse methoden voor het etsen van polyimide met een hard etsmasker werden onderzocht en een geschikte methode die gebruik maakt van één-stap-reactieve-ionenets wordt beschreven.

Samenvattend, de resultaten en de technologische ontwikkelingen welke beschreven zijn in dit proefschrift hebben geleid tot een beter begrip van de technologieën die noodzakelijk zijn voor de betrouwbare fabricage van vrijstaande verbindingsstructuren en hebben geresulteerd in een verbeterde rekbaarheid van rek- en plooibare elektronica.

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List of Publications

Journal articles

1. A.M. Savov*, **S. Joshi***, S. Shafqat, J.P.M. Hoefnagels, M. Louwerse, R. Stoute, R. Dekker, *A Platform for Mechano(-Electrical) Characterizationof Free-Standing Micron-Sized Structuresand Interconnects*, Micromachines 9, no. 1, pp. 39 (2018) **These authors should be regarded as joint first author.*

2. **S. Joshi**, A.M. Savov, S. Shafqat, R. Dekker, *Investigation of "Fur-like" Residues Post Dry Etching of Polyimide Using Aluminum Hard Etch Mask*, Material Science in Semiconductor Processing, 75, pp. 130-135 (2017)

3. S.Shafqat*, J.P.M. Hoefnagels*, A. Savov, **S.Joshi**, R. Dekker, M.G.D. Geers, *Ultra-Stretchable Interconnects for High-Density Stretchable Electronics*,Micromachines 8, no.9, pp. 277 (2017) **These authors should be regarded as joint first author.*

4. **S.Joshi**, W. De Haas, A.M. Savov, A.H.M Van Loon, R. Dekker, *"Adhesion Improvement of Polyimide / PDMS Interface by Polyimide Surface Modification"*, MRS Advances 1, pp. 33−38 (2016)

Conference Proceedings

1. **S. Joshi**, R. Bagani, L. Beckers, R. Dekker, *Novel Method for Adhesion between PI-PDMS Using Butyl Rubber for Large Area Flexible Body Patches*, in Multidisciplinary Digital Publishing Institute Proceedings (MDPI), vol. 1, no. 4 (2017)

2. P. Hammelmann, M. Mischi, R. Vullings, A.F. Kolen, L. Schmitt, **S. Joshi**, J.V. Laar, J.W.M. Bergmans, *Flexible sensor matrix with dynamic channel weighting for improved estimation of the fetal heart rate by Doppler ultrasound*, Ultrasonics Symposium (IUS), 2017 IEEE International, pp. 1-4 (2017)

3. **S. Joshi**, A.M. Savov, R. Dekker, *Substrate Transfer Technology for Stretchable Electronics*, Procedia Engineering, 168, pp. 1555-1558 (2016)

4. **S. Joshi**, S. Yazadi, V. Henneken, R. Sanders, R. Dekker, *Conformable body patches for ultrasound applications* , in Electronics Packaging and Technology Conference (EPTC), IEEE 17th, pp. 1-4 (2015)

5. A.M. Savov, S.K. Pakazad, **S. Joshi**, V. Henneken, R. Dekker, *A post processing approach for manufacturing high-density stretchable sensor arrays*, in IEEE Sensors, pp. 1703-1705 (2014)

Recognitions

1. Shivani Joshi, *Best Poster Award*, International Conference on Flexible and Printed Electronics (ICFPE), Seoul, South Korea, 2017
2. Shivani Joshi, *Best Innovative Research Value Poster Award*, Annual Materials Research meeting (M2i), Utrecht, The Netherlands, 2017

Biography

Shivani Joshi was born in Delhi, India in 1990. She received her BTech. and MTech. combined degree from Amity University, Noida, India in Nanotechnology in 2014. For her master thesis she worked on microfabrication of free standing interconnects at Microsystem and Devices group in Philips Research, Eindhoven, The Netherlands. She started her Ph.D. in 2014 at Department of Microelectronics, Delft University of Technology, The Netherlands. She was working on free standing interconnects for stretchable electronics. She conducted her research in Philips research as a guest researcher. Her PhD research was funded by M2i. During her PhD, she also worked as the chairperson of "Philips PhD community" from 2016-2017.

She is currently working as a design engineer in System Management and Verification Department at ASML, Veldhoven.