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Cryogenic Comparator Characterization and Modeling for a Cryo-CMOS 7b 1-GSa/s SAR ADC

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***Abstract*—This paper reports the experimental characterization and modelling of a stand-alone StrongARM comparator at both room temperature (RT) and cryogenic temperature (4.2 K). The observed 6-dB improvement in the comparator input noise at 4.2 K is attributed to the reduction of the thermal noise and to the suppressed shot noise in the MOS transistors becoming dominant at cryogenic temperature. The proposed model is employed in the design of a loop-unrolled 2× time-interleaved 1-GSa/s 7b SAR ADC for spin-qubit readout. As predicted by the comparator model, the ADC is noise-limited at RT to a SNDR of 38.2 dB at Nyquist input, while this improves to 41.1 dB at 4.2 K, now limited by distortion, thus resulting in the state-of-the-art FoM_W for cryo-CMOS ADC of 20.9 fJ/conv-step.**

***Index Terms*—Cryo-CMOS, SAR, ADC, latching comparator, strongARM, noise measurement**

I. Introduction

Quantum computers based on cryogenically cooled spin qubits in semiconductors offer a promising scaling route towards the very large number of qubits required for practical quantum applications [1]. While the core of these cryogenic computers is operating based on quantum mechanics, the algorithm execution is controlled by classical electronics typically operating at room temperature (RT). This poses a significant cabling bottleneck when increasing the qubit count, projected to grow well beyond a few thousands. To address this, a cryogenic CMOS (cryo-CMOS) electronic interface targeted to operate in the same cryostat as the qubits has been proposed [2].

The readout of semiconductor spin qubits can be performed using capacitive or resistive sensors. Their impedance can be remotely monitored by measuring the reflection coefficient at a 50-Ω line connected to the sensor via a matching network, thus achieving state-of-the-art readout speeds and allowing for frequency multiplexing of several qubit channels [3]. In such an RF readout, an RF tone weak enough to not disturb the qubit is reflected, amplified, and subsequently digitized. Due to the large bandwidth necessary for frequency multiplexing, a low-power high-speed ADC with medium resolution (6-8b) is required, thus making capacitive-DAC SAR ADCs the ideal candidates [3], [4].

The noise of such medium-resolution SAR ADCs is typically dominated by the comparator noise, which would be expected to drop by $\approx 70\times$ when reducing the temperature from RT to 4.2 K, if purely thermal in nature. However, characterization of various circuits at cryogenic temperatures suggests that this noise scaling is not achieved. For example, the noise figure of the LNA in [5] showed only an improvement from 2.5 dB to 0.6 dB, much less than predicted by assuming pure thermal noise. The absence of a comprehensive noise model for cryo-CMOS devices and the lack of direct noise measurements of dynamic latching circuits at cryogenic temperatures hinder the optimization of cryo-CMOS ADCs. To fill this gap, we report, for the first time, the measurement and the analysis of the noise and offset of a latching comparator at cryogenic temperatures. Based on those findings, we optimized the design of a prototype 7b 1-GSa/s SAR ADC, thus verifying the validity of the comparator characterization and modelling in a practical application.

In the following, Section II describes the proposed StrongARM comparator implementation, results and analysis. Section III covers the circuit design of the prototype ADC chip, concluding with its experimental validation.

*These authors contributed equally to the work.

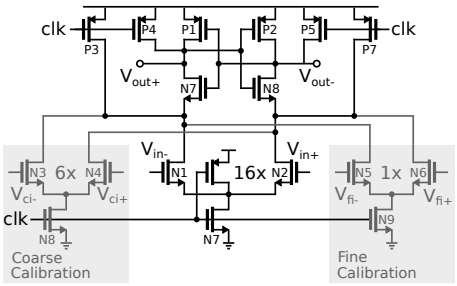

Figure 1. Comparator schematic; N3-4 (N5-6) is the coarse (fine) offset-calibration pair with input $V_{ci+,-}$ ($V_{fi+,-}$) provided by the ADC calibration circuit.

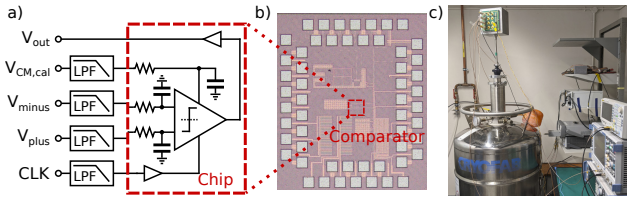

Figure 2. Test-chip for comparator characterization: a) schematic, b) chip micrograph, c) measurement setup.

II. Dynamic Comparator

The StrongARM comparator is a common choice in medium-resolution ADCs for its high speed, power efficiency

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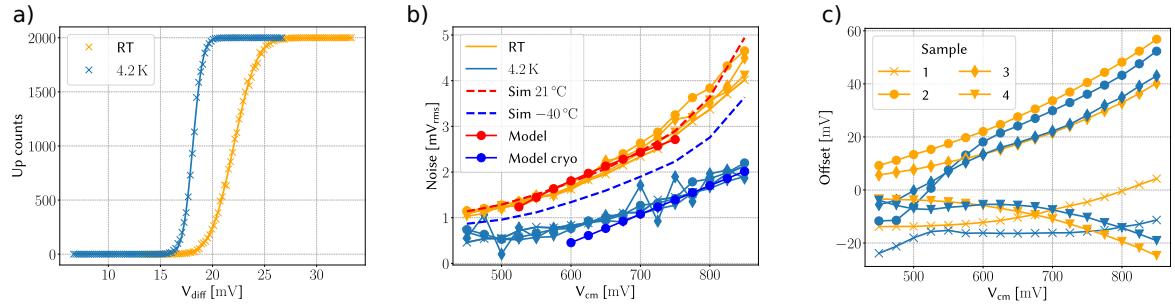

Figure 3. Comparator characterization: a) example measurement; b) noise voltage over input CM (V_{cm}) for four measured samples, simulations using the foundry device model, and the model in Eq. (5); c) measured offset over V_{cm} for four samples. Symbols for each sample are the same in b) and c).

and compactness. The proposed implementation (Fig. 1) comprises two additional coarse and fine calibration pairs to allow for an efficient foreground calibration [4]. In the following, a model for this circuit's noise and offset – relevant comparator parameters for ADC design – are derived and compared with experimental results. A specific focus is put on the behavior over input common-mode (CM), as this changes significantly due to both threshold-voltage increase at cryogenic temperature and CM variations on the capacitive DAC during a typical SAR conversion.

A. Measurements

The stand-alone comparator in Fig. 1 has been fabricated in a 40-nm CMOS process (Fig. 2b). All transistors are implemented as minimum length devices. On-chip input capacitors of 200 fF have been used to minimize the kT/C noise present at the input. A dip-stick setup employing liquid He (Fig. 2c) is used for cryogenic characterization, adopting the fixture shown in Fig. 2a. All DC input lines are filtered to reject interference coupling to the long cables in the dip-stick and are driven by 18b battery-operated RT DAC modules. We sweep the differential input voltage for a given CM and record the comparator decision statistics, from which we extract input noise and offset (Fig. 3a). On all sweeps, the CM voltage of the input and calibration pairs is the same.

When increasing the CM voltage at RT for four samples (Fig. 3b), we observe a monotonic increase of noise that is captured by the room-temperature simulation. When cooling down to 4.2 K, the transistor threshold voltage increases by about 80 mV, resulting in a shift of the curve towards a higher common-mode voltage. Compared to RT, the input noise voltage is about 2× lower and also significantly lower from simulations at −40 °C, the edge of the validity of the foundry supplied model.

The offset voltage (Fig. 3c) also shows a strong dependence on input CM, but no significant change is observed from RT to 4.2 K.

B. Model derivation

Previous analytical derivations for the noise of regenerative comparators assuming thermal-noise sources suggest that the input-referred noise power scales with absolute temperature [6], [7]:

$$\sigma_{in}^2 \propto T \tag{1}$$

However, the experimental characterization does not show the predicted large difference in noise power between RT and 4.2 K. To address the mismatch between the experimental results and the commonly accepted theory, we derive the input-referred noise by assuming the transistor noise to be a combination of thermal noise and suppressed shot noise [8].

First, we calculate the gain of the input pair during its amplification phase. This phase lasts from the positive clock edge till the input and calibration pair transistors, N1-N6, have discharged the parasitic capacitance C_p at their drains enough for the latch NMOS transistors (N7 and N8 in Fig. 1) to turn on, initiating exponential latching. The amplification time T_{amp} can be computed considering operation around common-mode as:

$$T_{amp} = \frac{2V_{th,N}C_p}{g_{m,all}V_{od}} \tag{2}$$

where $V_{th,N}$ is the NMOS device threshold voltage, $g_{m,all}$ is the combined transconductance of the input and calibration pairs, $V_{od} = V_{gs} - V_{th,N}$ is the input-pair overdrive voltage, and we assume strong-inversion operation for the input transistors. The gain of the input pair can then be written as:

$$A = \frac{g_m}{C_p}T_{amp} = \frac{2W_{in}V_{th,N}}{W_{all}V_{od}} \tag{3}$$

where W_{in} and $W_{all} = W_{in} + W_{cal}$ are the width of the input pair and the combined width of input and calibration pairs, respectively. We neglect the MOS output impedance. The power spectral density of the current noise in each half of the comparator is dominated by thermal and suppressed shot noise and it is given by:

$$S_{id} = 2qFI_{CM,all} + 4k_bT\gamma g_{m,all} \tag{4}$$

with q is the elementary charge, F the Fano factor, $I_{CM,all}$ the combined common-mode current, k_b the Boltzmann constant and T the absolute temperature. The input-referred noise in the amplification phase is then given by

$$\sigma_{in}^2 = \frac{qFW_{in}V_{od}^2}{2C_pW_{all}V_{th,N}} + \frac{2k_bT\gamma W_{in}V_{od}}{W_{all}C_pV_{th,N}} \tag{5}$$

This expression clearly show the increase of the input-referred noise with the input common-mode $V_{cm} = V_{od} + V_{th,N}$ that we observe in the measurement.

According to our model, while thermal noise dominates at RT by contributing 84% of the total noise for $V_{cm} = 650\,\mathrm{mV}$, it becomes negligible at cryogenic temperatures. At $4.2\,\mathrm{K}$, the noise behavior is mainly determined by the shift in threshold voltage and the temperature dependence of the Fano factor. The threshold voltage (extracted from DC characterization of individual transistors) increases from $450\,\mathrm{mV}$ at RT to $530\,\mathrm{mV}$ at $4.2\,\mathrm{K}$, decreasing the overdrive voltage and therefore also lowering the noise. In practice, the $V_{th,N}$ change results in a shift of the noise curve towards higher V_{cm}.

When assuming a mix of thermal noise with $\gamma = 1$ and shot noise with $F = 0.1$ at RT, we achieve in good fitting between the foundry device model and Eq. (4) in transistor noise simulation. As shown in Fig. 3b, this also results in good match between the proposed model and the experimental data. The region of validity of our model is bounded by the subthreshold region towards lower V_{cm} and by the latch noise becoming relevant for higher V_{cm} as the input-pair gain decreases, as predicted in Eq. (3).

Using the model we can achieve a good fit for the dependency of the noise on V_{cm} even at $4.2\,\mathrm{K}$. However, here the Fano factor must be increased to $F = 0.25$ (only at $4.2\,\mathrm{K}$) to achieve an acceptable match with experimental data. Such an increase in the suppression factor could be attributed to the device behaving closer to an ideal ballistic device at lower temperatures, e.g., due to a decrease in carrier scattering in the channel. Although the shot-noise in nanometer CMOS devices have been extensively studied at RT [9], no comprehensive data on the behavior of F at cryogenic temperatures is available, thus pointing to the need for further cryogenic device characterization and physical modelling. As an outcome, the proposed model successfully captures the circuit noise behavior within the CM region, which is mainly relevant for high-speed ADC design, shown in Section III.

The comparator offset due to the input and calibration pairs can be calculated:

$$\Delta V_{in,os} = \left(\Delta V_{th,in} + \frac{\Delta\beta}{\beta}\frac{V_{od,in}}{2}\right)\sqrt{1 + \frac{W_{cal}}{W_{in}}} \qquad (6)$$

where β is the device current gain, $\Delta V_{th,in}$, $\Delta\beta$ are the standard deviation of mismatch in threshold voltage and current gain of the input pair respectively. As reported in [10], the mismatch in threshold voltage shows a negligible variation at cryogenic temperature while the mismatch in β is expected to increase by 25%, thus explaining the little observed change in Fig. 3c.

III. Cryo-CMOS ADC

A. Circuit design

We verify the StrongARM comparator model in a prototype ADC tested at both RT and $4.2\,\mathrm{K}$. Similar to [4], the circuit is a $2\times$ time-interleaved loop-unrolled (LU) 7b SAR ADC. The 6b capacitive-DAC (CDAC) employs top-plate sampling and is implemented using custom $0.5\,\mathrm{fF}$ unit cells. Since the ADC is intended for integration with an input on-chip driver in the target qubit-readout system, non-switched capacitors connected to ground are included in the CDAC to reduce the input range of the ADC to 600 $\mathrm{mV_{pp}}$, thus easing the output swing specifications of the input driver. To further facilitate the input driver, the ADC also implements a reset to V_{cm} before sampling, followed by a DAC switching similar to [4]. This provides higher V_{cm} for the comparators after the MSB decision to compensate for the increased $\mathrm{V_{th}}$ at cryogenic temperature.

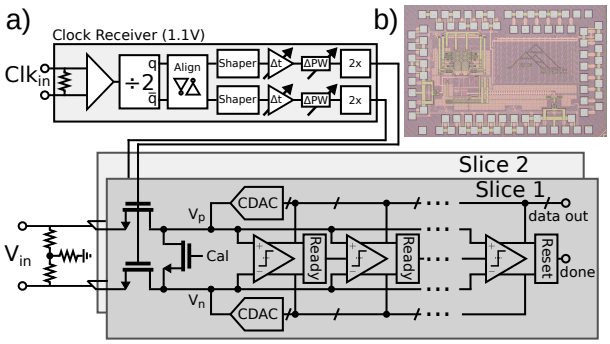

Figure 4. ADC protoype: a) block diagram; b) micrograph.

To improve power efficiency compared to [4], the entire sampling clock chain has been implemented using thin-oxide devices. At the end of the clock chain, thin-oxide NMOS switches with $2\times$ boosted control voltage are used to sample the input signal. A pulse shaper in the clock chain tunes the duty-cycle of the sampling clock to provide more than 50% of the clock period for conversion. The $2\times$ time-interleaved ADC suffers from interleaving artifacts caused by timing mismatch. To calibrate these, a pair of digitally controlled delay lines are designed to adjust the delay of the sampling clock provided to each slice.

The StrongARM comparator measured and analyzed in Section II is used in the LU-SAR loop. The comparator design is optimized for speed and the ADC is targeted to be comparator-noise limited at RT. Since the comparator offset causes distortion for LU-SAR, the input voltages of the fine and coarse differential pair in Fig. 1 are generated by a resistive DAC to calibrate the offset, similar to [4] but with an optimized scheme with 5b (coarse) and 6b (fine) resolution. During foreground calibration, a switch with boosted static gate voltage is activated to short $\mathrm{V_p}$ and $\mathrm{V_n}$ (Fig. 4a) to calibrate every comparator at the correct $\mathrm{V_{CM}}$ level. Resetting the comparator tail node (drain node of N7 in Fig. 1) eliminates any signal-dependant offset, which would otherwise limit the achievable calibration accuracy, as was the case in [4].

B. Measurement

The chip is implemented in a 40-nm process, see the micrograph in Fig. 4b. Five sample dies have been bonded to the test PCBs and characterized in the same dip-stick environment as the comparator.

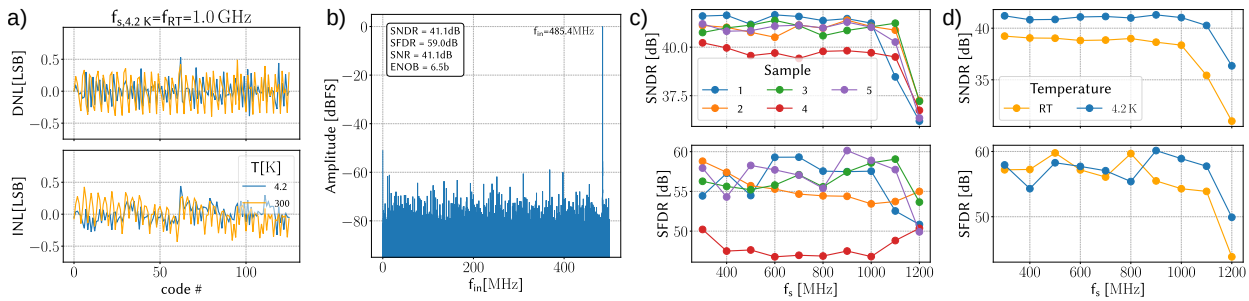

Figure 5. ADC characterization: a) INL and DNL for worst sample (sample 4) ; b) output spectrum at 1 GS/s and 4.2 K (sample 5); c) SNDR and SFDR at 4.2 K for all measured samples. SFDR does not include the TI-induced spur at $f_s/2$ d) SNDR and SFDR at RT and 4.2 K for a typical sample (sample 5).

Table I
COMPARISON TABLE

	This work		[4]		Kull, ISSCC 2013	Kull, ISSCC 2017
Temperature [K]	300	4.2	300	4.2	300	300
Architecture	TI SAR		TI SAR		SAR	PP-SAR
Max f_s[MS/s]	1000		900	1000	1300	950
Resolution [bit]	7		6-8		8	10
Technology [nm]	40		40		32	14
Supplies [V]	1.1		1.1(core), 2.5(clock)		1	0.7
Input range [Vpp]	0.6		0.7	0.7	0.5	0.5
SNDR@Nyquist [dB]	38.2[2]	41.1[2]	33.4	36.2	39.3	50
SFDR [dB]	>50[2]	>50[2]	48.4	48.5	49.6	58
Power [mW]	1.94[1]		10.3[1]	10.6[1]	3.1	2.26
FoM_w[fJ/c.step]	29.2[1, 2]	20.9[1, 2]	260[1]	200[1]	28	8.9
Core area [mm^2]	0.042[1]		0.045[1]		0.0015	0.0016

[1]Full ADC, including clock receiver [2]typical sample

The comparator offset calibration based on binary search and the timing skew calibration are implemented off-chip. To optimize the linearity, manual calibration fine-tuning is done besides binary search for samples 1 and 3.

In Fig. 5a, the static performance of the worst-case sample (sample 4) is reported. Unlike [4], no signal-dependent residual offset appears and the maximum INL/DNL is below 0.55 LSB for both RT and 4.2 K. The Nyquist-rate input measurement in Fig. 5b shows an SNDR of 41.1dB. Combined with the 1.94 mW power drawn from the nominal 1.1-V supply, this results in a typical Walden FOM_W of 20.9 fJ/conv·step (including the clock receiver), a 10× improvement compared to [4], see Table I. All tested samples reach 1 GSa/s before dropping in SNDR value, see Fig. 5c. The dynamic performance of sample 4 is limited by the accuracy of the offset calibration. The higher sampling rates at 4.2 K are attributed to the increased speed of the comparator and the digital circuitry in the SAR loop.

Comparing the dynamic performance at RT and 4.2 K in Fig. 5d, reveals an improvement of 2-dB SNDR at 4.2 K. At 4.2 K harmonic distortion is not limiting the performance as indicated by the measured SFDR, and the SNDR is in line with the quantization-noise-limited performance of an ADC with 0.5-LSB INL. Therefore, the 6-dB improvement in comparator noise measurements at 4.2 K (Fig. 3b) makes the comparator noise negligible at cryogenic temperature.

IV. CONCLUSION

We have reported the first direct noise and offset measurements and modelling on a latching comparator at cryogenic temperatures. The gathered evidence points towards a relatively small improvement in white noise at cryogenic temperature, due to the white noise originating from a mix of thermal and shot noise. The proposed model has been applied to the design of a high-speed cryo-CMOS SAR ADC for spin-qubit readout, resulting in state-of-the-art performance compared to previously reported cryo-CMOS ADCs.

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